FORESEE®

e-MMC
Specification

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Rev.	Date	Changes	Remark
A0	10/16/2010	Basic spec and architecture	
A1	03/05/2011	Updated the Features section	
A2	07/18/2011	Updated the Function Description section	
A3	11/06/2011	Updated the Function Description section	
A4	02/10/2012	Updated several descriptions	Preliminary

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1. INTRODUCTION

1.1 Overview

FORESEE Embedded MultiMedia Card (e·MMC) is an embedded memory solution designed to support host processors with MMC bus. FORESEE e·MMC is consisted of SMI controller and advanced NAND flash memory ranging from 2GB to 16GB. The MMC interface is compliant with JEDEC e·MMC4.41 standard, which is backward compatible with e·MMC4.2, e·MMC4.3 and e·MMC4.4. Moreover, new functions of Background Operation, Enhance Reliable Write and High Priority Write are provided to meet the designs of nowadays mobile platforms. To best support portable devices which requires low power consumption, the e·MMC supports dual voltage where 3.3V is for NAND flash core while 1.8V and 1.2V are for the controller. In this e·MMC device, NAND flash memory is managed by Controller, which manages ECC, wear leveling and bad block management. FORESEE e·MMC provides easy integration with the host process that all flash management hassles are invisible to the host.

1.2 Features

- Complies with e·MMC specification Ver. 4.41, and backward compatible with e·MMC4.2, eMMC4.3 and eMMC4.4.
- Supports three data bus width modes: 1-bit (default), 4-bit, and 8-bit
- Support (Alternate) Boot Operation Mode to provide a simple boot sequence method.
- Enhanced Reliable Write
- Supports High Priority Interrupt (HPI)
- Background operation
- Enhanced Write Protection with Permanent and Partial protection options.
- Introduces hardware reset signal.
- Support Relay Protected Memory Block (RPMB)
- Class 0 (basic), Class 2 (block read), Class 4 (block write), Class 5 (erase), Class 6 (write protection), Class 7 (lock/unlock)
- High speed, double data rate boot support
- Variable clock rate 0~20MHz, 0~26MHz or 0~52MHz. Supports High-Speed dual data rate transfer Multimedia card @52MHz
- Dynamic power management technology, quick standby, auto-suspend, and sleep operation.

1.3. Function Description

FORESEE e·MMC contains an intelligent e·MMC controller with JEDEC e·MMC

v4.41, will achieve the highest data transfer rate and provides many new features not found in other types of storage devices:

- Support Multiple User Data Partition with Enhanced User Data Area options
- Signed access to a replay Protected Memory Block
- Support dual data rate transfer
- High speed boot
- Enhanced Write Protection with Permanent and Partial protection options
- Support hardware reset signal
- Optional high priority interrupt mechanism

1.4. Independent Technology

e·MMC v4.41 specification defines the communication protocol between host and advice. The protocol is independent of the NAND Flash features included the e·MMC controller can manages wear leveling, bad block management and ECC. So the host system will not need to update their hardware or software to support the new process flash, this is very important since the NAND flash is becoming increasingly complies with current advanced NAND process. Which means that host system will be able to access e·MMC devices built with new flash technology without having to update their host hardware or software。

1.5. Defect and Error Management

FORESEE e·MMC incorporates advanced technology for defect and error management. If a defective block is identified, e·MMC completely replaces the defective block with 1 of the spare blocks. This process is invisible to the host and generally does not affect data space allocated for the user.
e·MMC also includes a built-in error correction code(ECC) to maintain data integrity.

2. PRODUCT SPECIFICATIONS

2.1Product list

Capacity (GB)	Part ID	Capacity	Capacity [Bytes]	Package Size	Pin Configuration
4GB	NCEMBS41-04G	3.71GB	3,992, 977,408	12x16x1.2 (mm)	FBGA169

Note: 1 gigabytes (1GB) = 1 billion bytes. Some capacity is not available for data storage.

2.2 Performance (Typical value) 8bit@52MHz

Capacities	Sequential Write	Sequential Read	Random Write	Random Read
4GB	8MB/s	28MB/s	4MB/s	26MB/s

Test condition: Intel Core2 2.4GHz CPU, 2GB DDRII, Intel G45 Chipset, USB2.0 host, Window 7 OS, GL822 Card reader.
Test tool: HD Bench V3.40 Software.

2.3Power Supply and Power Consumption

Power Supply:

Parameter	Symbol	Min	Max
Supply voltage（NAND）	Vcc	2.7 V	3.6 V
Supply voltage（I/O）	VccQ	2.7 V	3.6 V
Supply power-up for 3.3V	tPRUH	——	35 ms
Supply power-up for 1.8V	tPRUL	——	25 ms
Supply power-up for 1.2V	tPRUV	——	20 ms

Power Consumption:

Status	Max Value	Average Value
Auto Sleep mode	100uA	80uA
Sleep	30uA	25uA
Read	100mA	50mA
Write	100mA	60mA

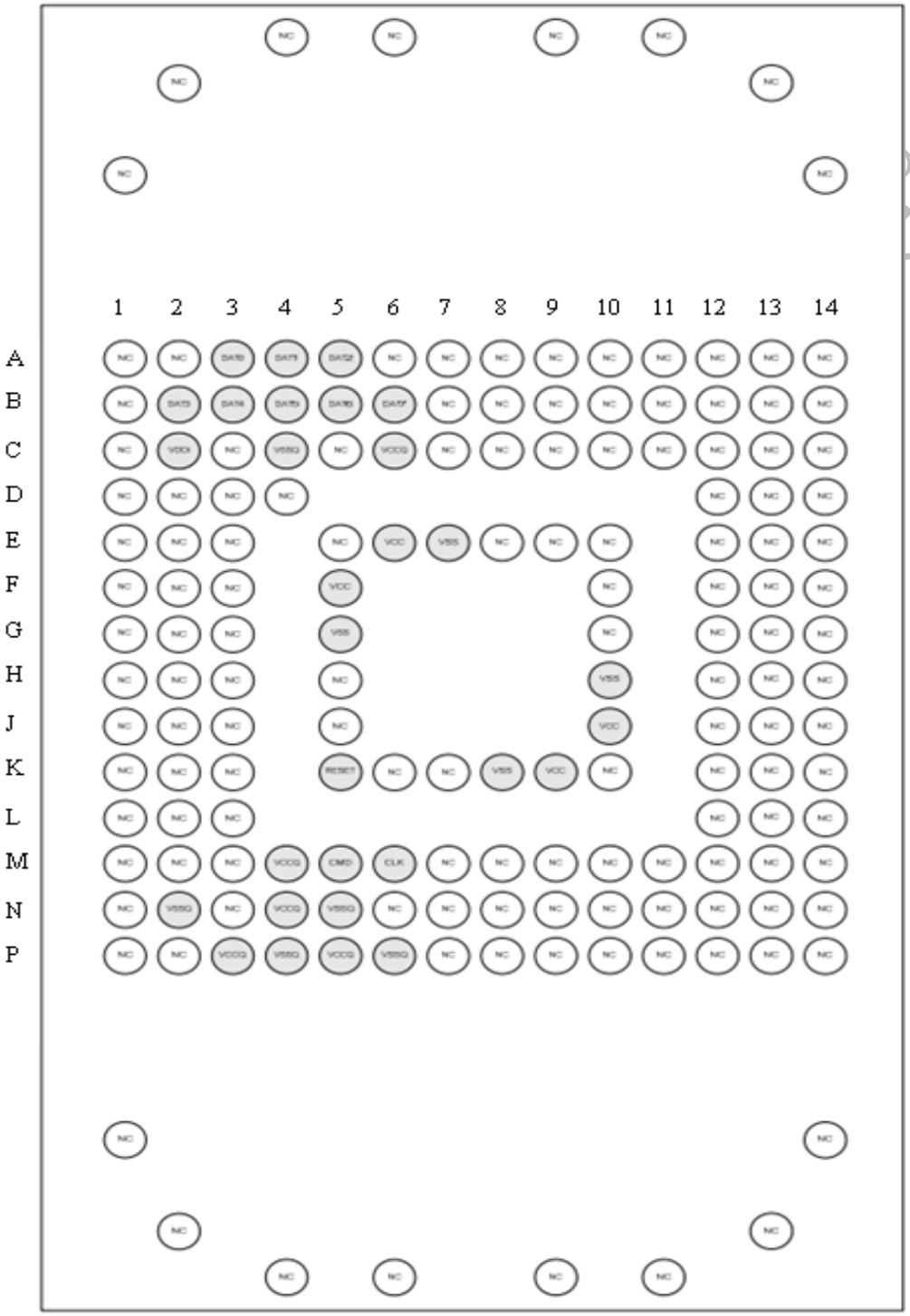
Test condition: 8bit bus width, 52MHz clock, Current measurements are average over 100mSecs（Ta=25°C@3.3V）.

2.4 Operational Environment

Operating mode: -10° C to 85° C
Storage mode: -25° C to 85° C

3. Pin assignments

3.1 Ball Array view



169 balls - Ball Array (Top View)

3.2 Pin Assignment

Signal	Description
CLOCK (CLK)	Each cycle of the clock directs a transfer on the command line and on the data lines. The frequency can vary between the minimum and the maximum clock frequency.
COMMAND (CMD)	This signal is a bidirectional command channel used for device initialization and command transfer. The CMD Signal has 2 operation modes: open drain, for initialization, and push-pull, for command transfer. Commands are sent from the MMC host to the device, and responses are sent from the device to the host.
DATA (DAT0-DAT7)	These are bidirectional data signal. The DAT signals operate in push-pull mode. By default, after power-up or RESET, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer wither using DAT [3:0](4bit mode)or DAT[7:0](8bit mode). Includes internal pull-up resistors for data lines DAT[7:1].Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT1 and DAT2 lines.(The DAT3 line internal pull-up is left connected.)Upon entering the 8bit mode, the device disconnects the internal pull-up on the DAT1, DAT2, and DAT[7:4]lines.
RST_n	Hardware Reset Input
VCCQ	VCCQ is the power supply line for host interface, have two power mode: High power mode:2.7V~3.6V; Lower power mode:1.7V~1.95V
VCC	VCC is the power supply line for internal flash memory, its power voltage range is:2.7V~3.6V
VDDi	VDDi is internal power node, not the power supply. Connect 0.1uF capacitor VDDi to ground
VSS,VSSQ	Ground lines.

Note: All other pins are not connected [NC] and can be connected to GND or left floating.

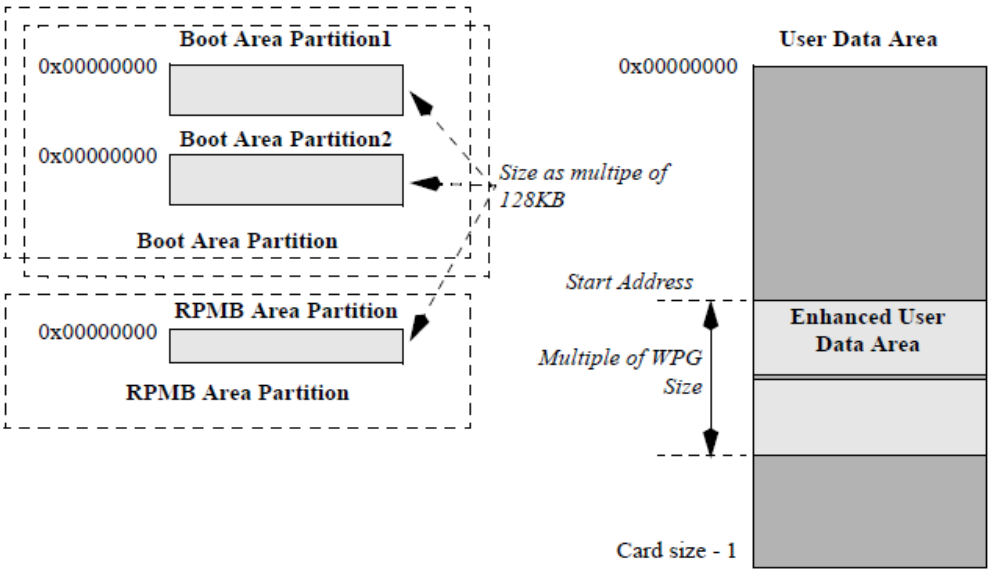
4. e·MMC4.41 Function Description

(For more details, please refer to to JEDEC standard document No. 84-A441)

4.1 Partition Management

The embedded device offers also the possibility of configuring by the host additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Default size of each Boot Area Partition is 128 KB and can be changed by Vendor Command as multiple of 128KB. Boot area partition size is calculated as (128KB * BOOT_SIZE_MULTI) The size of Boot Area Partition 1 and 2 cannot be set independently and is set as same value Boot area partition which is enhanced partition. Therefore memory block area scan is classified as follows:

- ✧ Factory configuration supplies boot partitions, implemented as enhanced storage media and one RPMB partitioning of 128KB in size.
- ✧ The host is free to configure one segment in the User Data Area to be implemented as enhanced storage media, and to specify its starting location and size in terms of Write Protect Groups. The attributes of this Enhanced User Data Area can be programmed only once during the device life-cycle (one-time programmable).
- ✧ Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size and attributes can be programmed once in device life-cycle (one-time programmable). Each of the General Purpose Area Partitions can be implemented with enhanced technological features.

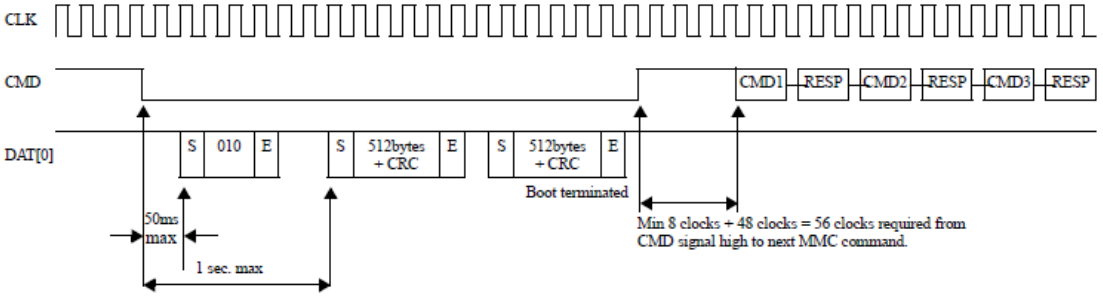


Partitions and user data area configuration

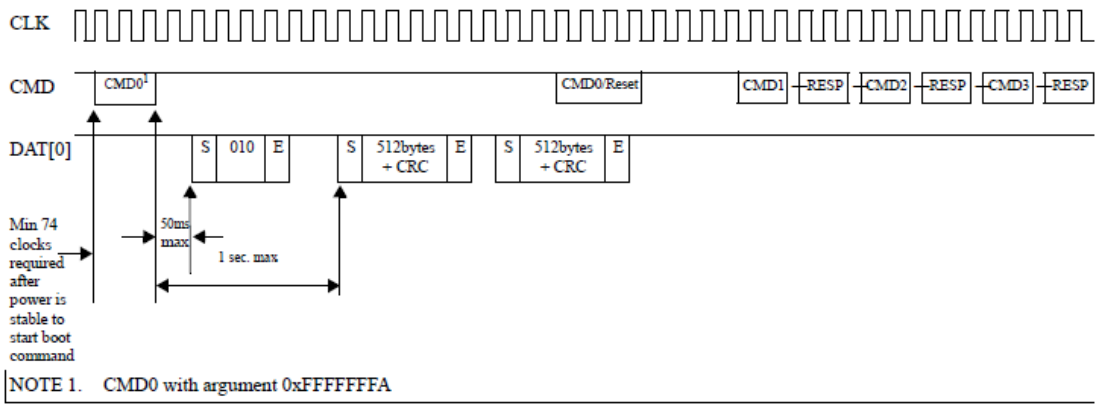
4.2 Boot operation

In boot operation mode, the master (MultiMediaCard host) can read boot data from the slave (MMC device) by keeping CMD line low or sending CMD0 with

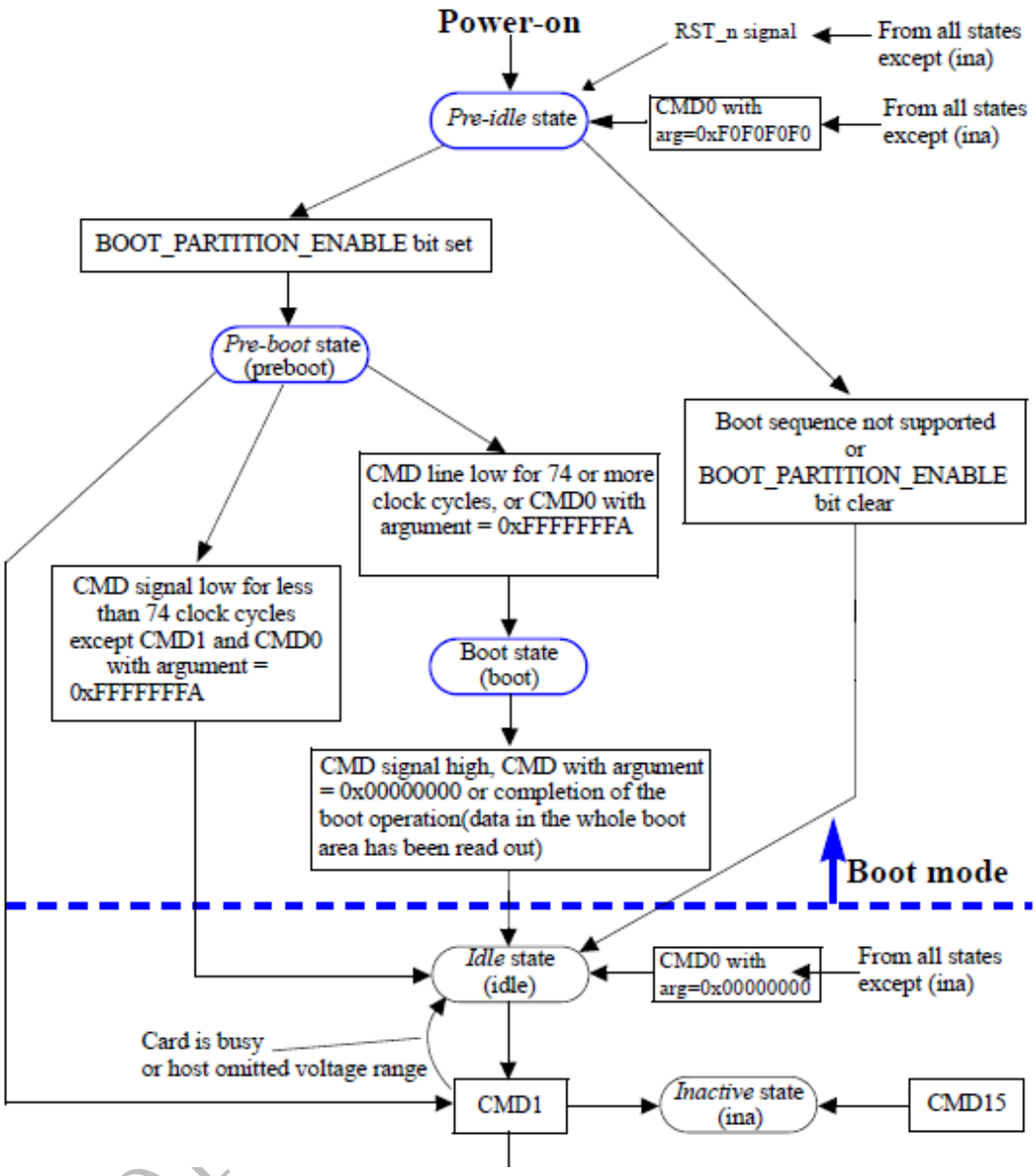
argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting.



MultiMediaCard state diagram (boot mode)



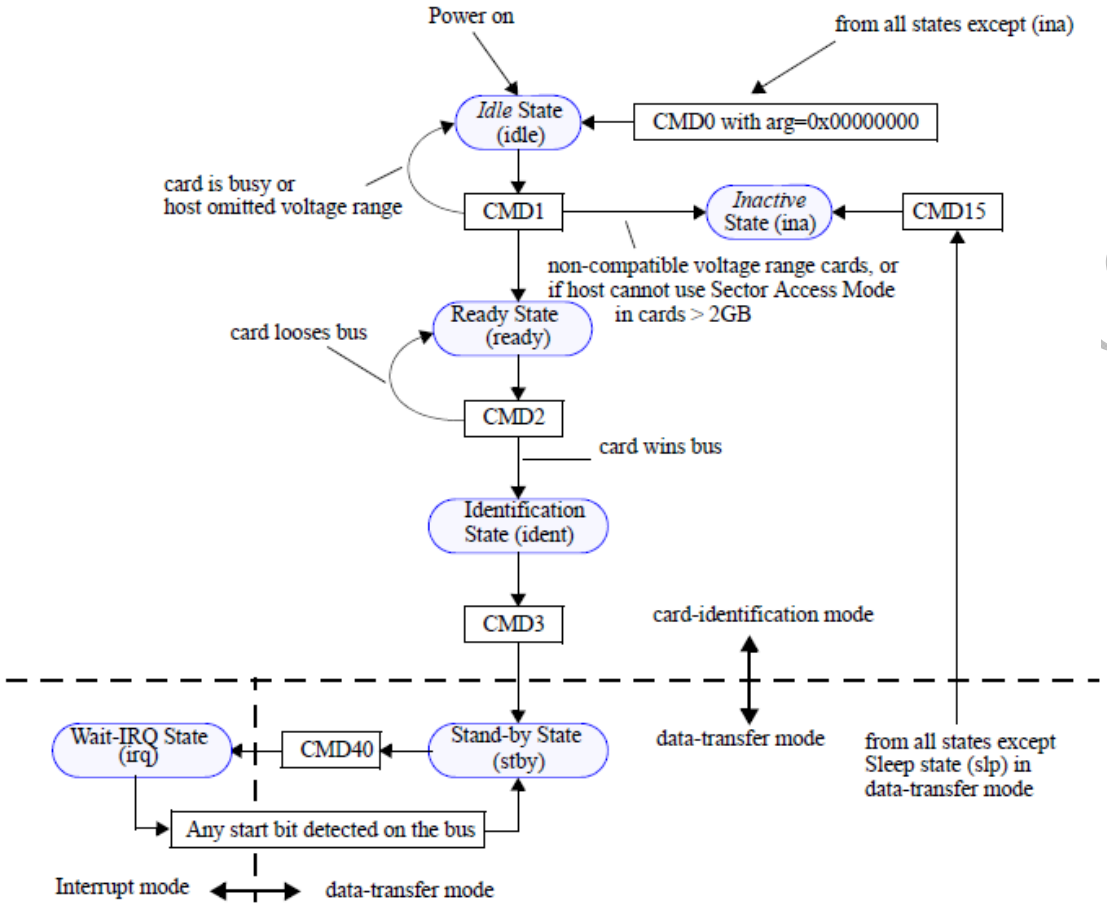
MultiMediaCard state diagram (alternative boot mode)



MultiMediaCard state diagram (boot mode)

4.3 Card identification mode

While in card identification mode the host resets the card, validates operation voltage range and access mode, identifies the card and assigns a Relative Card Address (RCA) to the card on the bus. All data communication in the Card Identification Mode uses the command line (CMD) only.



MultiMediaCard state diagram (card identification mode)

4.4 Automatic Sleep Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption. At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion. The below table explains the condition to enter and exit Auto Power Saving Mode

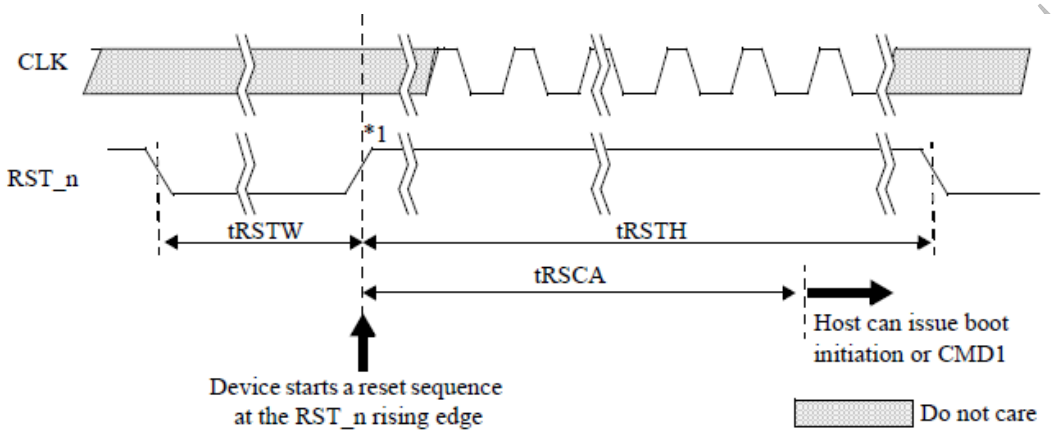
4.5 Sleep (CMD5)

A card may be switched between a Sleep state and a Standby state by SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized. In this state the memory device reacts only to the commands RESET (CMD0 with argument of either 0x00000000 or 0xF0F0F0F0 or H/W reset) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device. The timeout for state transitions between Standby state and Sleep state is defined in the EXT_CSD register S_A_timeout. The maximum current consumptions during the Sleep state are defined in the EXT_CSD

registers S_A_VCC and S_A_VCCQ. Sleep command: The bit 15 as set to 1 in SLEEP/ AWAKE (CMD5) argument. A wake command: The bit 15 as set to 0 in SLEEP/AWAKE (CMD5) argument.

4.6 H/W Reset operation

Device will detect the rising edge of RST_n signal to trigger internal reset sequence



H/W reset waveform

4.7 Enhanced Reliable Write

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

4.8 Secure Erase

In addition to the standard erase command, the e·MMC supports the optional Secure Erase command5. The Secure Erase command differs from the basic Erase command in that it requires the e·MMC to execute the erase operation on the memory array when the command is issued and requires the e·MMC and host to wait until the operation is complete before moving to the next e·MMC operation.

The secure erase command requires the e·MMC to perform a secure purge operation on the erase groups, and copy items identified for erase, in those erase groups. A purge operation is defined as overwriting addressable locations with a single character and then performing an erase. This new command meets high security application requirements (e,g, those used by military and government customers) that once data has been erased, it can no longer be

retrieved from the device.

4.9 Secure Trim

The Secure Trim 6 command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups. The size of a write block in the e·MMC device is 512B.

4.10 Trim

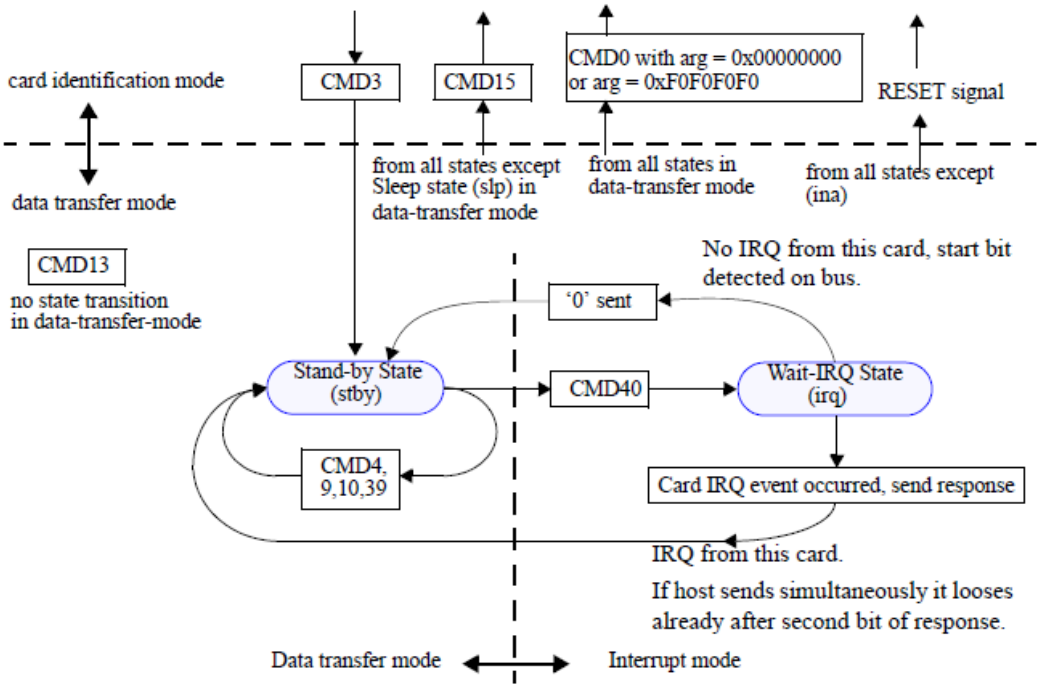
The Trim function is similar to the Erase command but applies the erase operation to write blocks instead of erase groups. The size of a write block in the INAND device is 512B.

4.11 Enhanced Write Protection

To allow the host to protect data against erase or write, the e·MMC supports two levels of write protect command8: The entire e·MMC (including the Boot Area Partitions, General Purpose Area Partition, and User/Enhanced User Data Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD. Specific segments of the e·MMC may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register.

4.12 Interrupt mode

The interrupt mode on the MultiMediaCard system enables the master (MultiMediaCard host) to grant the transmission allowance to the slaves (card) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a card request for service. Supporting MultiMediaCard interrupt mode is an option, both for the host and the card.



MultiMediaCard state transition diagram, interrupt mode

4.13 High Priority Interrupt

The high priority interrupt (HPI) mechanism enables servicing high priority requests, by allowing the device to interrupt a lower priority operation before it is actually completed, within OUT_OF_INTERRUPT_BUSY_TIME timeout. Host may need to repeat the interrupted operation or part of it to complete the original request. The HPI command may have one of two implementations in the device:

• CMD12 – based on STOP_TRANSMISSION command when the HPI bit in its argument is set.

• CMD13 – based on SEND_STATUS command when the HPI bit in its argument is set.

Host shall check the read-only HPI_IMPLEMENTATION bit in HPI_FEATURES (EXT_CSD byte [503]) and use the appropriate command index accordingly.

CMD Index	Name	Interruptible	Restrictions
CMD24	WRITE_BLOCK	Yes	
CMD25	WRITE_MULTIPLE_BLOCK	Yes	
CMD38	ERASE	Yes	
CMD6	SWITCH	Yes	Only interruptible when writing to the BKOPS_START field in EXT_CSD

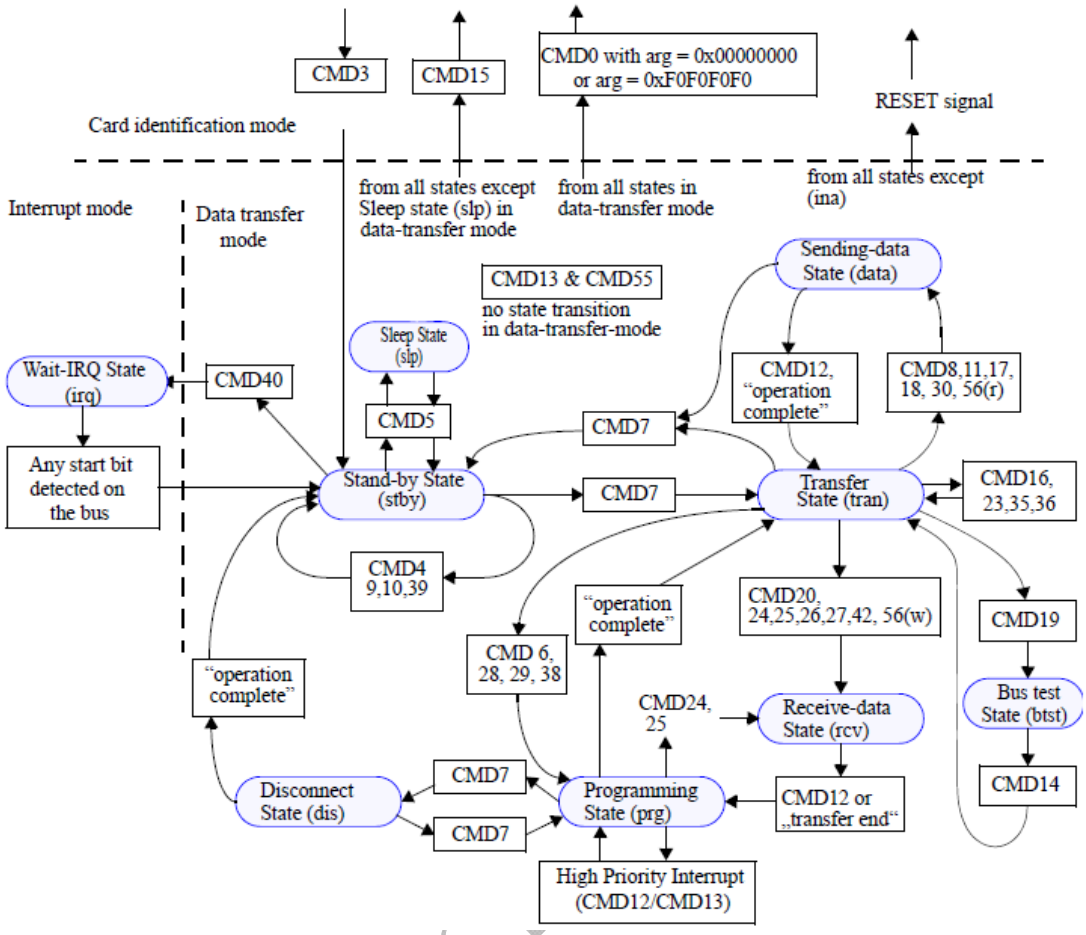
All others	No	

4.14 Data transfer mode

All data communication in the Data Transfer Mode is point-to point between the host and the selected card (using addressed commands). All addressed commands get acknowledged by a response on the CMD line.

While the card is in *Stand-by* State, CMD7 is used to select the card and put it into the *Transfer* State by including card's relative address in the argument. If the card was previously selected and was in *Transfer* State its connection with the host is released and it will move back to the *Stand-by* State when deselected by CMD7 with any address in the argument that is not equal to card's own relative address. When CMD7 is issued with the reserved relative card address "0x0000", the card is put back to *Stand-by* State. Reception of CMD7 with card's own relative address while the card is in *Transfer* State is ignored by the card and may be treated as an Illegal Command. After the card is assigned an RCA it will not respond to identification commands — CMD1, CMD2, or CMD3.

While the card is in *Disconnect* State, CMD7 is used to select the card and put it into the Programming State by including card's relative address in the argument. If the card was previously selected and was in *Programming* State its connection with the host is released and it will move back to the *Disconnect* State when deselected by CMD7 with any address in the argument that is not equal to card's own relative address. Reception of CMD7 with card's own relative address while the card is in Programming State is ignored by the card and may be treated as an Illegal Command.



MultiMediaCard state diagram (data transfer mode)

4.15 Background Operations

Devices have various maintenance operations need to perform internally. In order to reduce latencies during time critical operations like read and write, it is better to execute maintenance operations in other times - when the host is not being serviced. Operations are then separated into two types:

- ✧ Foreground operations – operations that the host needs serviced such as read or write commands;
- ✧ Background operations – operations that the device executes while not servicing the host; In order for the device to know when the host does not need it and it can execute background operations, host shall write any value to BKOPS_START (EXT_CSD byte [164]) to manually start background operations. Device will stay busy till no more background processing is needed.

At the Idle state (Host does not access to device), Host can do certain operation by using "Background Operation" command. In this case, the operation which takes long time to complete can be handled later when host ensure enough idle time (In Back ground operation) Background Operation Sequence is the

following

4.16 High-speed mode selection

After the host verifies that the card complies with version 4.0, or higher, of this standard, it has to enable the high speed mode timing in the card, before changing the clock frequency to a frequency higher than 20MHz. For the host to change to a higher clock frequency, it has to enable the high speed interface timing. The host uses the SWITCH command to write 0x01 to the HS_TIMING byte, in the Modes segment of the EXT_CSD register.

4.17 Bus width selection

After the host has verified the functional pins on the bus it should change the bus width configuration accordingly, using the SWITCH command. The bus width configuration is changed by writing to the BUS_WIDTH byte in the Modes Segment of the EXT_CSD register (using the SWITCH command to do so). After power-on, or software reset, the contents of the BUS_WIDTH byte is 0x00.

4.18 Card lock/unlock operation

The password protection feature enables the host to lock the card by providing a password, which later will be used for unlocking the card. The password and its size are kept in a 128 bit PWD and 8 bit PWD_LEN registers, respectively. These registers are non-volatile so that a power cycle will not erase them. The password protection feature can be disabled permanently by setting the permanent password disable bit in the extended CSD (PERM_PSWD_DIS bit in the EXT_CSD byte [171]). If the host attempts to permanently disable CMD42 features on an *e*·MMC having a password set, the action will fail and the ERROR (bit 19) error bit will be set by the memory device in the card status register It is recommended to disable the password protection feature on the card, if it is not required, to prevent it being set unintentionally or maliciously. An attempt to use password protection features (CMD42) on a card having password permanently disabled will fail and the LOCK_UNLOCK_FAILED (bit 24) error bit will be set in the status register.

4.19 CID register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase (MultiMediaCard protocol). Every individual flash or I/O card shall have an unique identification number. Every type of MultiMediaCard ROM cards (defined by content) shall have a unique identification number. The structure of the CID register is defined in the following sections.

Name	Field	Width	CID-slice

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
Reserved	-	6	[119:114]
Card/BGA	CBX	2	[113:112]
OEM/Application ID	OID	8	[111:104]
Product name	PNM	48	[103:56]
Product revision	PRV	8	[55:48]
Product serial number	PSN	32	[47:16]
Manufacturing date	MDT	8	[15:8]
CRC7 checksum	CRC	7	[7:1]
Not used, always '1'	-	1	[0:0]

4.20 CSD register

The Card-Specific Data (CSD) register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the CSD Registry entries coded as follows:

Name	Field	Width	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	R	[127:126]
System specification version	SPEC_VERS	4	R	[125:122]
Reserved	-	2	R	[121:120]
Data read access-time 1	TAAC	8	R	[119:112]
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]
Card command classes	CCC	12	R	[95:84]
Max. read data block length	READ_BL_LEN	4	R	[83:80]
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]
DSR implemented	DSR_IMP	1	R	[76:76]
Reserved	-	2	R	[75:74]
Device size	C_SIZE	12	R	[73:62]
Max. read current @ V_{DD} min	VDD_R_CURR_MIN	3	R	[61:59]
Max. read current @ V_{DD} max	VDD_R_CURR_MAX	3	R	[58:56]

Name	Field	Width	Cell Type	CSD-slice
Max. write current @ V_{DD} min	VDD_W_CURR_MIN	3	R	[55:53]
Max. write current @ V_{DD} max	VDD_W_CURR_MAX	3	R	[52:50]
Device size multiplier	C_SIZE_MULT	3	R	[49:47]
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]
Write protect group size	WP_GRP_SIZE	5	R	[36:32]
Write protect group enable	WP_GRP_MULT	1	R	[31:31]
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]
Write speed factor	R2W_FACTOR	3	R	[28:26]
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]
Reserved	-	4	R	[20:17]
Content protection application	CONTENT_PROT_APP	1	R	[16:16]
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]
Copy flag(OTP)	COPY	1	R/W	[14:14]
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]
File format	FILE_FORMAT	2	R/W	[11:10]
ECC code	ECC	2	R/W/E	[9:8]
CRC	CRC	7	R/W/E	[7:1]
Not used, always '1'	-	1	-	[0:0]

4.21 Extended CSD register

The Extended CSD register defines the card properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the card capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the card is working in. These modes can be changed by the host by means of the SWITCH command.

Name	Field	Size	Type	Slice [bytes]	Value	Description
Reserved		7		[511:505]	0h	
Supported Command Sets	S_CMD_SET	1	R	[504]	1h	Allocated by MMCA
HPI Features	HPI_FEATURES	1	R	[503]	3h	HPI type CMD12
Background operations support	BKOPS_SUPPORT	1	R	[502]	1h	BKOPS supported
Reserved		255		[501:247]	0h	
Background operations status	BKOPS_STATUS	1	R	[246]	0h	No operations required
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0h	
First Initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	Ah	initial time out 1s
Reserved		2		[237:236]	0h	
Power class for 52Mhz,DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0h	rms 100 mA, peak 200 mA
Power class for 52Mhz,DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0h	rms 65 mA, peak 130 mA
Reserved		2		[237:236]	0h	
Minimum write performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0h	For cards not reaching the 4.8 MB/s value
Minimum read performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0h	For cards not reaching the 4.8MB/s value
Reserved		1		[233]	0h	
TRIM Multiplier	TRIM_MULT	1	R	[232]	1h	trim time out 300ms

Name	Field	Size	Type	Slice [bytes]	Value	Description
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	15h	1. Support the secure and insecure trim operations. 2. Support the automatic secure purge operation on retired defective portions of the array. 3. Secure purge operations are supported.
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	Ah	secure erase time out 3s
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	Ah	secure trim time out 3s
Boot Information	BOOT_INFO	1	R	[228]	7h	1. Support high speed timing boot. 2. Support DDR boot. 3. Support alternative boot method.
Reserved		1		[227]	0h	
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	4h	boot partition 512KB
Access size	ACC_SIZE	1	R	[225]	7h	super page 32KB
High-capacity Erase unit size	HC_ERASE_GROUP_SIZE	1	R	[224]	1h	hc erase group size 512KB
High-capacity Erase time out	ERASE_TIMEOU_MULT	1	R	[223]	1h	hc erase time out 300ms
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	1h	1 sector
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	8h 10h	hc wp group size 4KB or 8KB

Name	Field	Size	Type	Slice [bytes]	Value	Description
Sleep current[VCC]	S_C_VCC	1	R	[220]	8h	128μA
Sleep current[VCCQ]	S_C_VCCQ	1	R	[219]	7h	128μA
Reserved		1	R	[218]	0h	
Sleep/Awake time out	S_A_TIMEOUT		R	[217]	TBD*	sleep/awake time out
Reserved		1		[216]	0h	
Sector count	SEC_COUNT	4	R	[215:212]		depend on density
Reserved		1		[211]	0h	
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	R	[210]	0h	For cards not reaching the 2.4MB/s value
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	R	[209]	0h	For cards not reaching the 2.4MB/s value
Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h	For cards not reaching the 2.4MB/s value
Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0h	For cards not reaching the 2.4MB/s value
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[206]	0h	For cards not reaching the 2.4MB/s value
Minimum Read Performance for 4bit @26MHz	MIN_PERF_R_4_26	1	R	[205]	0h	For cards not reaching the 2.4MB/s value
Reserved		1		[204]	0h	
Power Class for 26MHz @3.6V	PWR_CL_26_360	1	R	[203]	0h	rms 100 mA, peak 200 mA
Power Class for 52MHz @3.6V	PWR_CL_52_360	1	R	[202]	0h	rms 100 mA, peak 200 mA
Power Class for 26MHz @1.95V	PWR_CL_26_195	1	R	[201]	0h	rms 65 mA, peak 130 mA

Name	Field	Size	Type	Slice [bytes]	Value	Description
Power Class for 52MHz @1.95V	PWR_CL_52_195	1	R	[200]	0h	rms 65 mA, peak 130 mA
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	2h	partition switch time 20 ms
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	2h	HPI time out 20 ms
Reserved		1		[197]	0h	
Card Type	CARD_TYPE	1	R	[196]	7h	DDR 52 @ 1.8/3.3V
Reserved		1		[195]	0h	
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	2h	CSD version No. 1.2
Reserved		1		[193]	0h	
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	5h	Revision 1.5 (for MMC v4.41)
Command Set	CMD_SET	1	R/W/E_P	[191]	0h	
Reserved		1		[190]	0h	
Command set revision	CMD_SET_REV	1	R	[189]	0h	v4.0
Reserved		1		[188]	0h	
Power class	POWER_CLASS	1	R/W/E_P	[187]	0h	
Reserved		1		[186]	0h	
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0h	
Reserved		1		[184]	0h	
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0h	
Reserved		1		[182]	0h	
Erased memory range	ERASE_MEM_CONT	1		[181]	0h	
Reserved		1		[180]	0h	
Partition Configuration	PARTITION_CONFIG	1	R/W/E R/W/E_P	[179]	0h	

Name	Field	Size	Type	Slice [bytes]	Value	Description
Boot config protection	BOOT_CONFIG_PROT	1	R/W R/W/C_P	[178]	0h	
Boot bus width1	BOOT_BUS_WIDTH	1	R/W/E	[177]	0h	
Reserved		1		[176]	0h	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0h	
Reserved		1		[174]	0h	
Boot area write protect register	BOOT_WP	1	R/W R/W/C_P	[173]	0h	
Reserved		1		[172]	0h	
User area write protect register	USER_WP	1	R/W R/W/C_P R/W/E_P	[171]	0h	
Reserved		1		[170]	0h	
FW Configuration	FW_CONFIG	1	R/W	[169]	0h	
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	1h	RPMB size 128KB
Write reliability setting register	WR_REL_SET	1	R/W	[167]	1Fh	
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	5h	
Reserved		1		[165]	0h	
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0h	
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0h	
H/W reset function	RST_n_FUNCTION	1	R	[162]	0h	

Name	Field	Size	Type	Slice [bytes]	Value	Description
Reserved		1		[161]	0h	
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	3h	1. Enhanced technological features in partitions and user data area. 2. Device supports partitioning features
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	1C4h	4GB
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0h	
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0h	
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0h	
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0h	
Reserved		1		[135]	0h	
Secure Bad Block Management Mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0h	
Reserved		134		[133:0]	0h	

Notes: 1. R= Read-olny
R/W=One-Time Programmable and readable
R/W/E=Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable
TBD=To Be Defined.
2. Reserved bits should be read as 0.

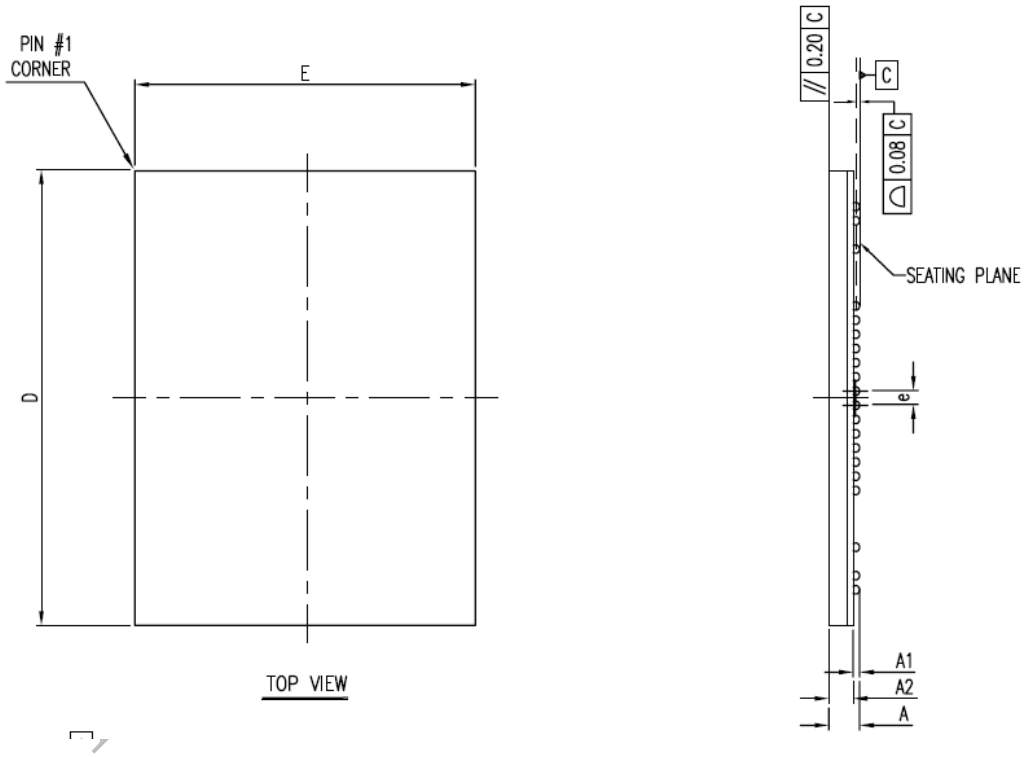
4.22 OCR Register

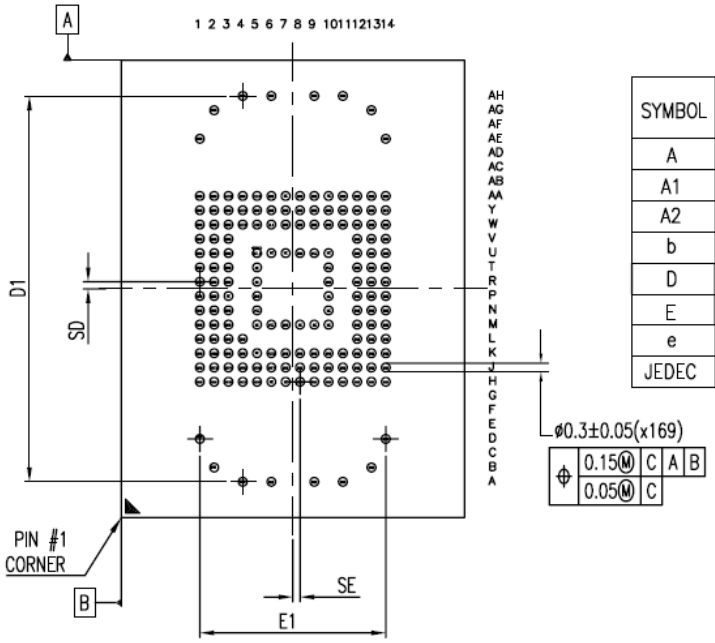
The 32-bit operation conditions register stores the VCCQ voltage profile of the e·MMC. In addition, this register includes a status information bit. This status bit is set if the e·MMC power up procedure has been finished. The OCR register shall be implemented by e·MMC.

OCR bit	Vccq voltage window	e·MMC
[6:0]	Reserved	000 0000b
[7]	1.7–1.95	1b
[14:8]	2.0–2.6	000 0000b
[23:15]	2.7–3.6	1 1111 1111b
[28:24]	Reserved	000 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[31]	power up status bit (busy)*	

Note*: This bit is set to LOW if the e·MMC has not finished the power up routine. The supported voltage range is coded as shown in table.

5. Package Dimension

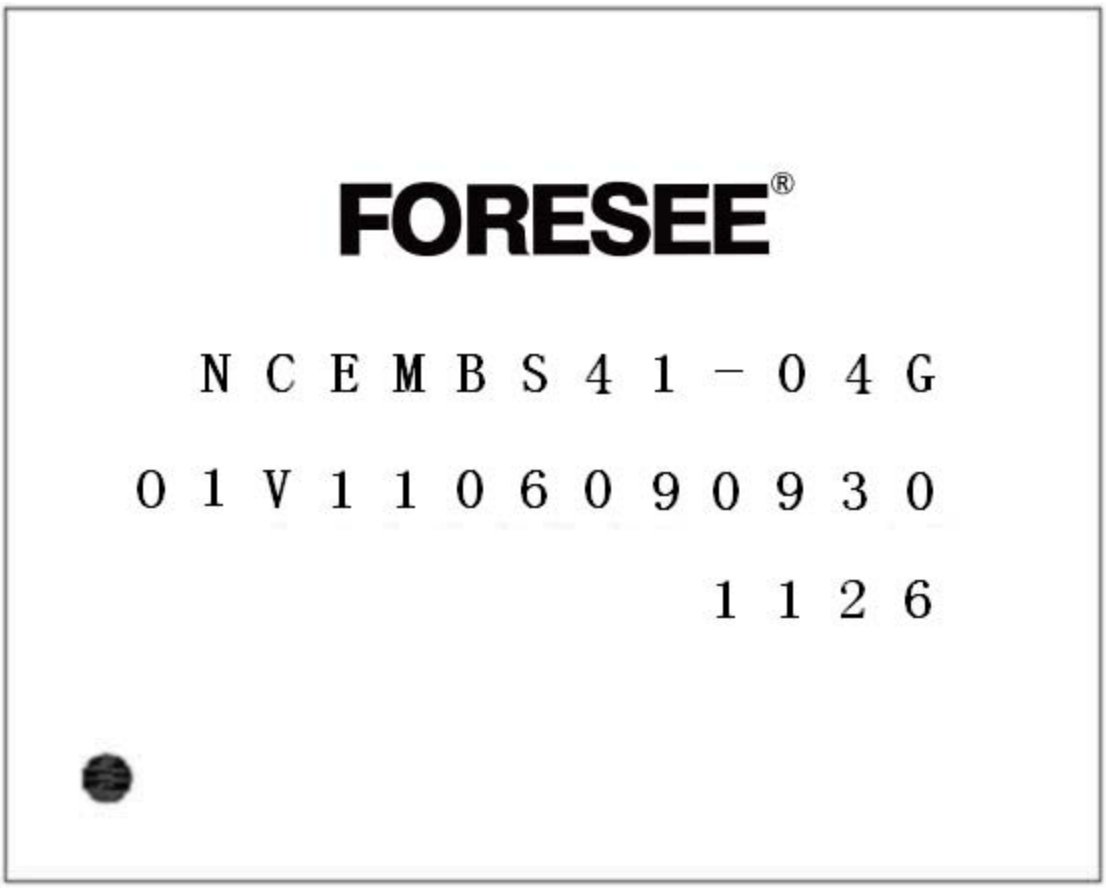




SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	---	---	1.20	---	---	0.047
A1	0.15	---	---	0.006	---	---
A2	---	---	0.92	---	---	0.036
b	0.25	0.30	0.35	0.010	0.012	0.014
D	15.90	16.00	16.10	0.626	0.630	0.634
E	11.90	12.00	12.10	0.469	0.472	0.476
e	0.5 BSC.			0.020 BSC.		
JEDEC	MO-276					

12mm x 16mm x 1.2mm Package Dimension

6. MARKING



First row: FORESEE Logo
FORESEE is a registered trademark owned by NETCOM
Second row: Ordering information/ Sales item
Third row: Variant Code
Fourth row: Date code