

A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. Segment B has an arrow pointing to it from the left.

C

B

- A**

A vertical number line with four points labeled A, B, C, and D from bottom to top. An arrow points to point C.

C

B

- 1A

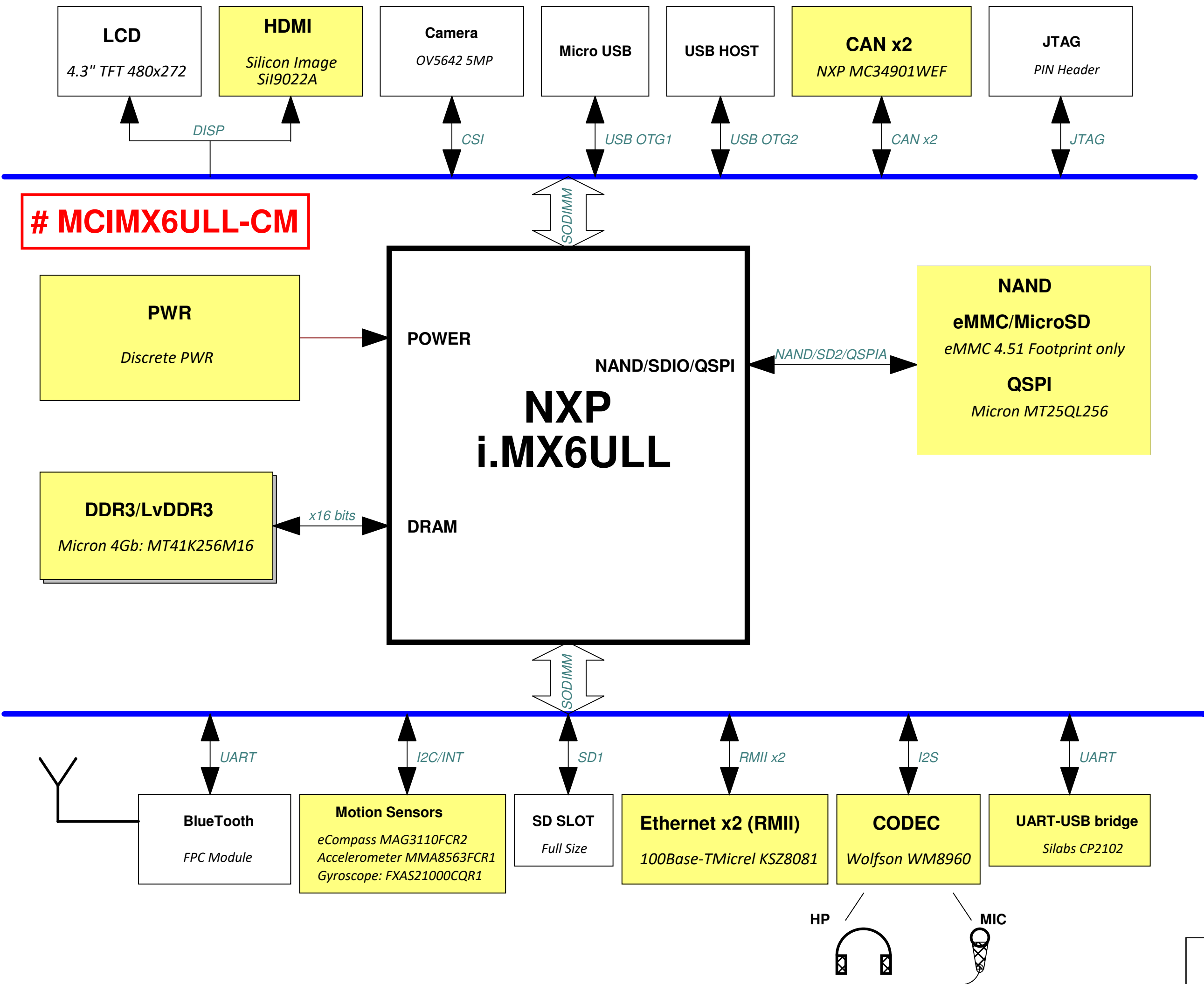
1A

i.MX6ULL EVK Block Diagram

Blcok Diagram Rev 1.0

MCIMX6ULL-BB

MPN: MCIMX6ULL-BB
MPN: MCIMX6ULL-CM
Agile No: 28616
Agile No: 29364

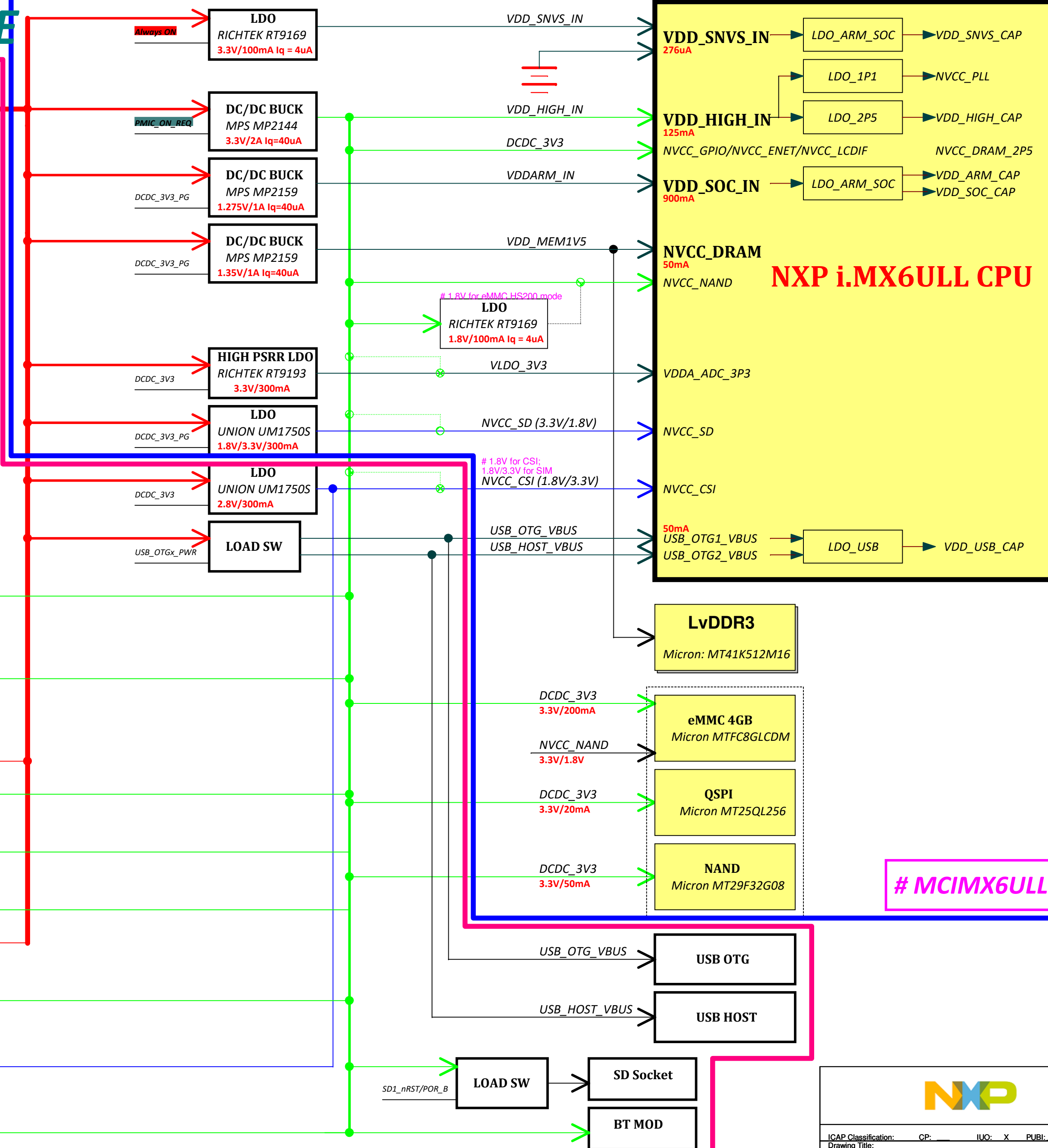
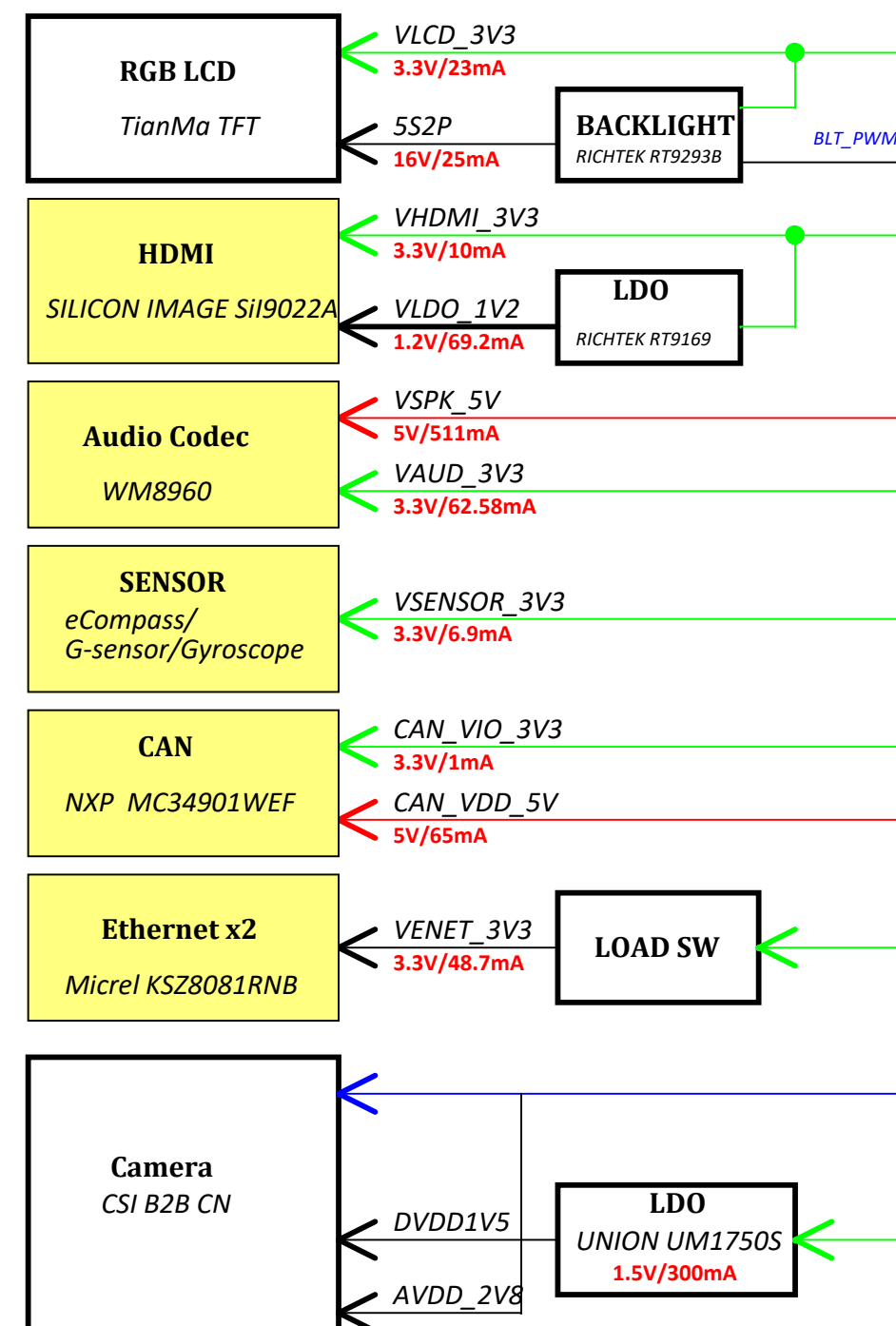


ICAP Classification: CP: IUC: X PUBI:			
Drawing Title: MCIMX6ULL-CM			
Page Title: Block Diagram			
Size C	Document Number	SCH-29364 PDF: SPF-29364	Rev A1
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i.MX6ULL EVK PWR TREE

WALL Adapter: 5V/3A

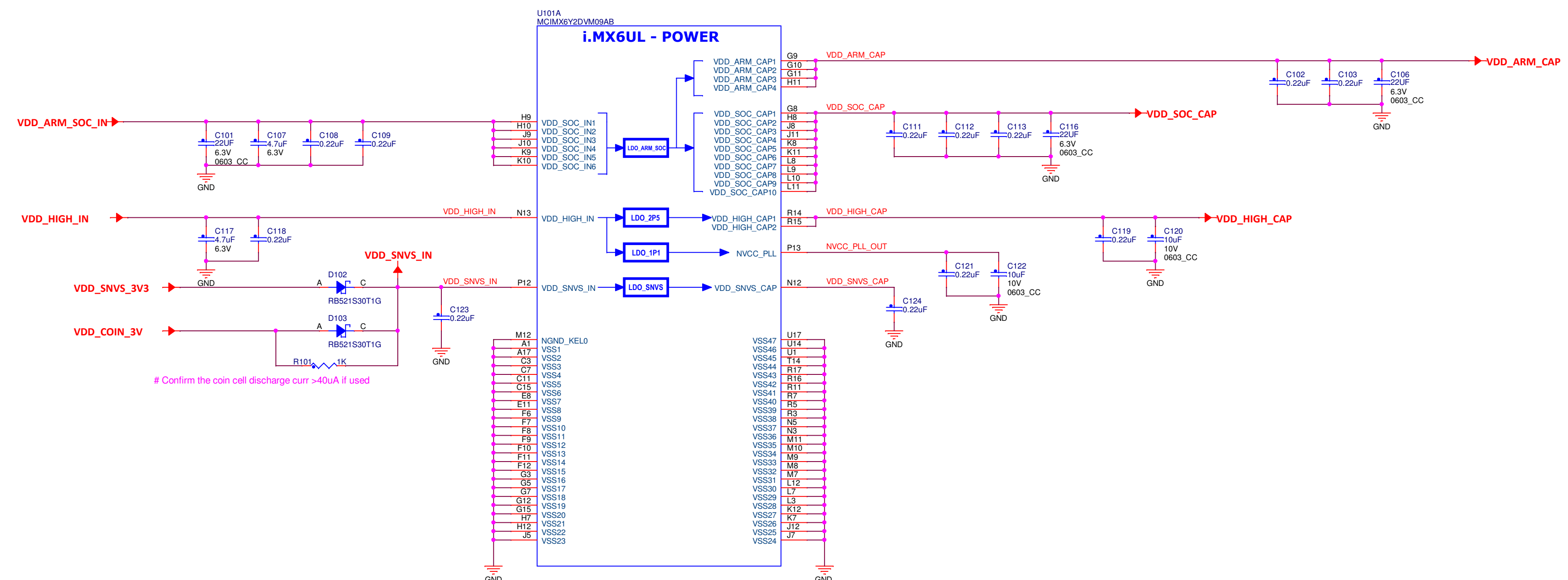
MCIMX6ULL-BB



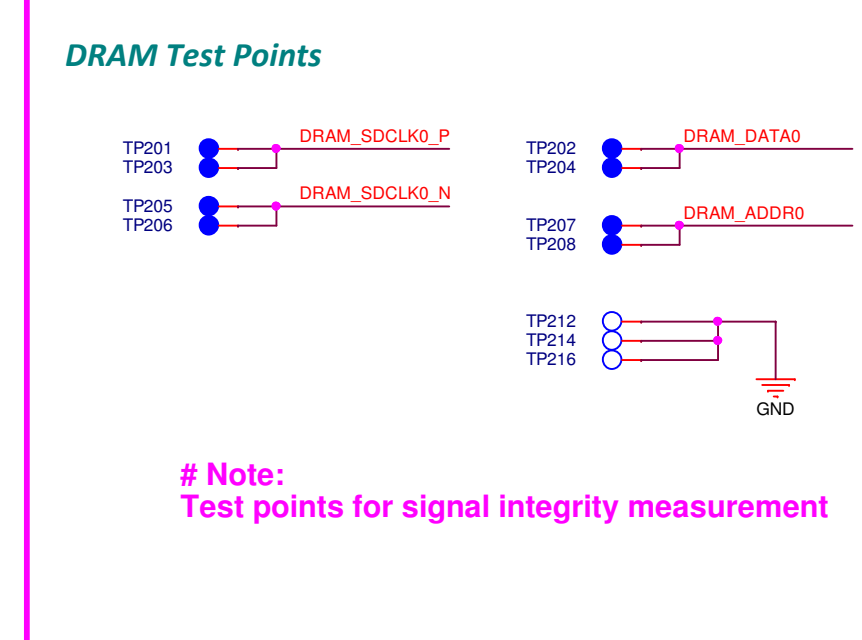
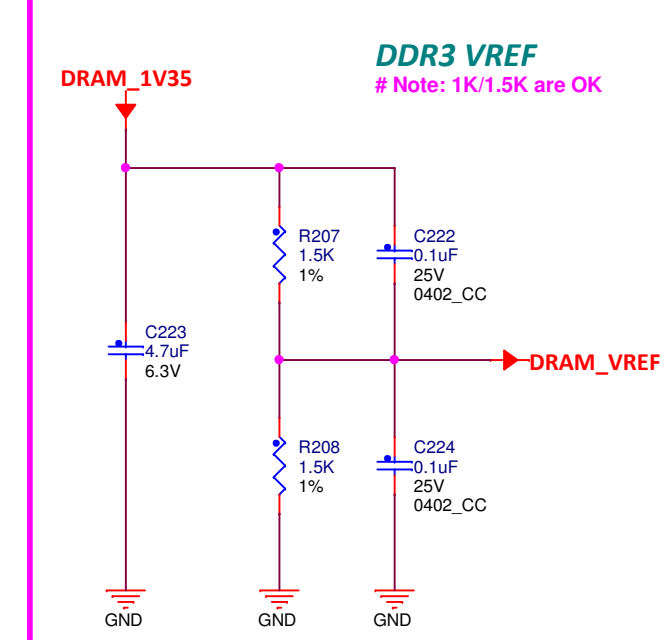
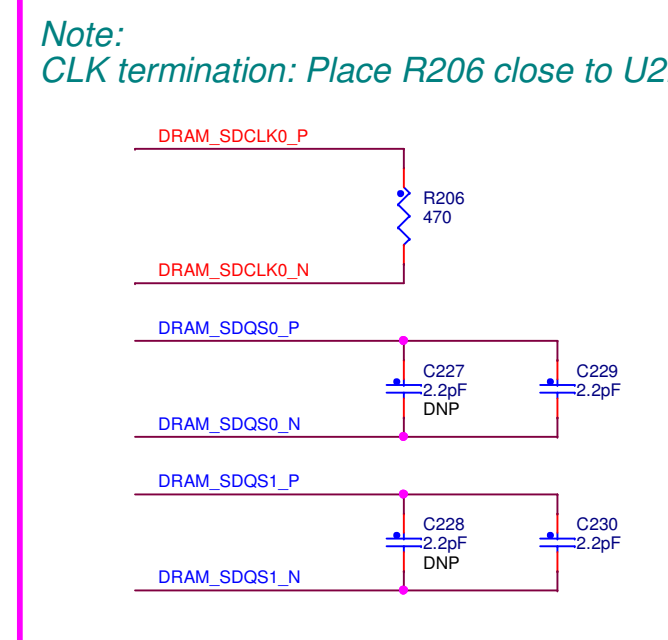
MCIMX6ULL-CM

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Drawing Title:	MCIMX6ULL-CM		
Page Title:	PWR TREE		
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i.MX6ULL PWR



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Page Title: CPU PWR			
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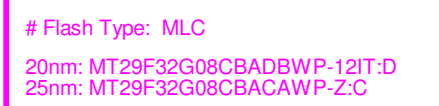


Option 2



eMMC: MTFC8GACAAAM-1M WT

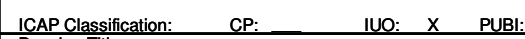
Option 1



Option 3



Option 2



ICAP Classification: CP: IUO: X PUBI:

Drawing Title: **MCIMX6ULL-CM**

Page Title: FLASH

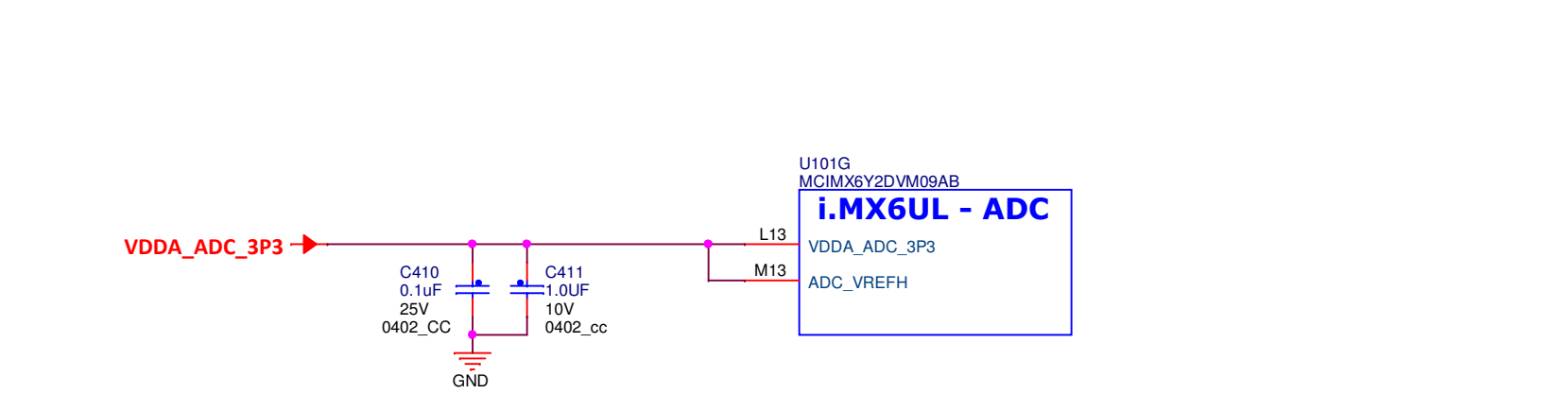
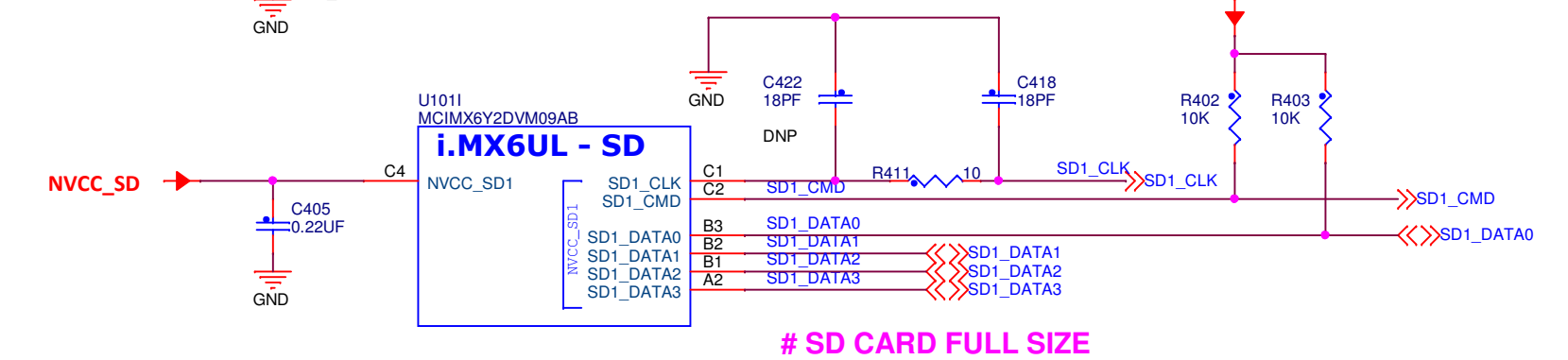
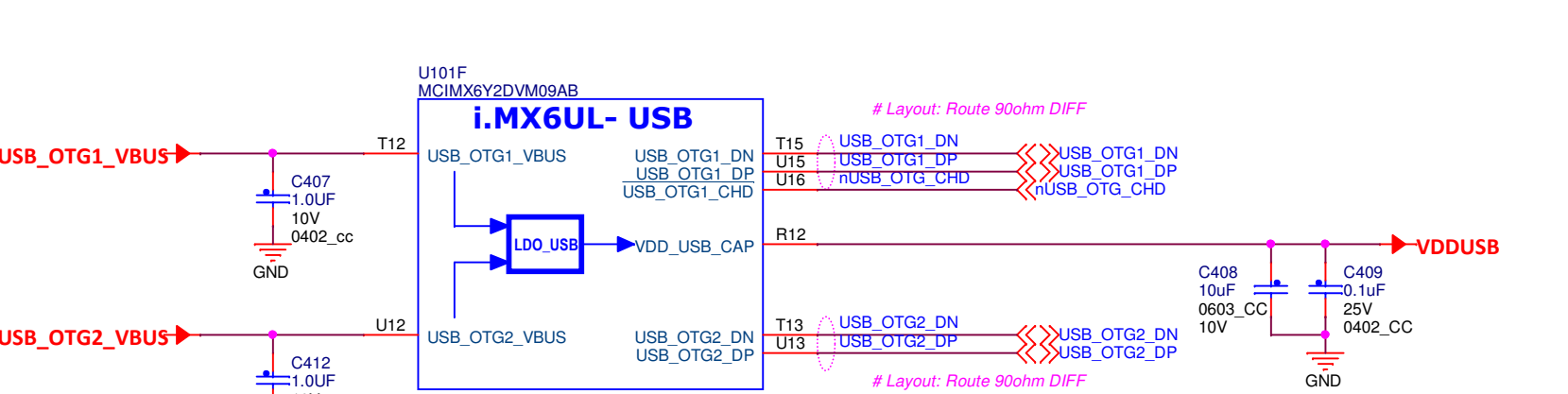
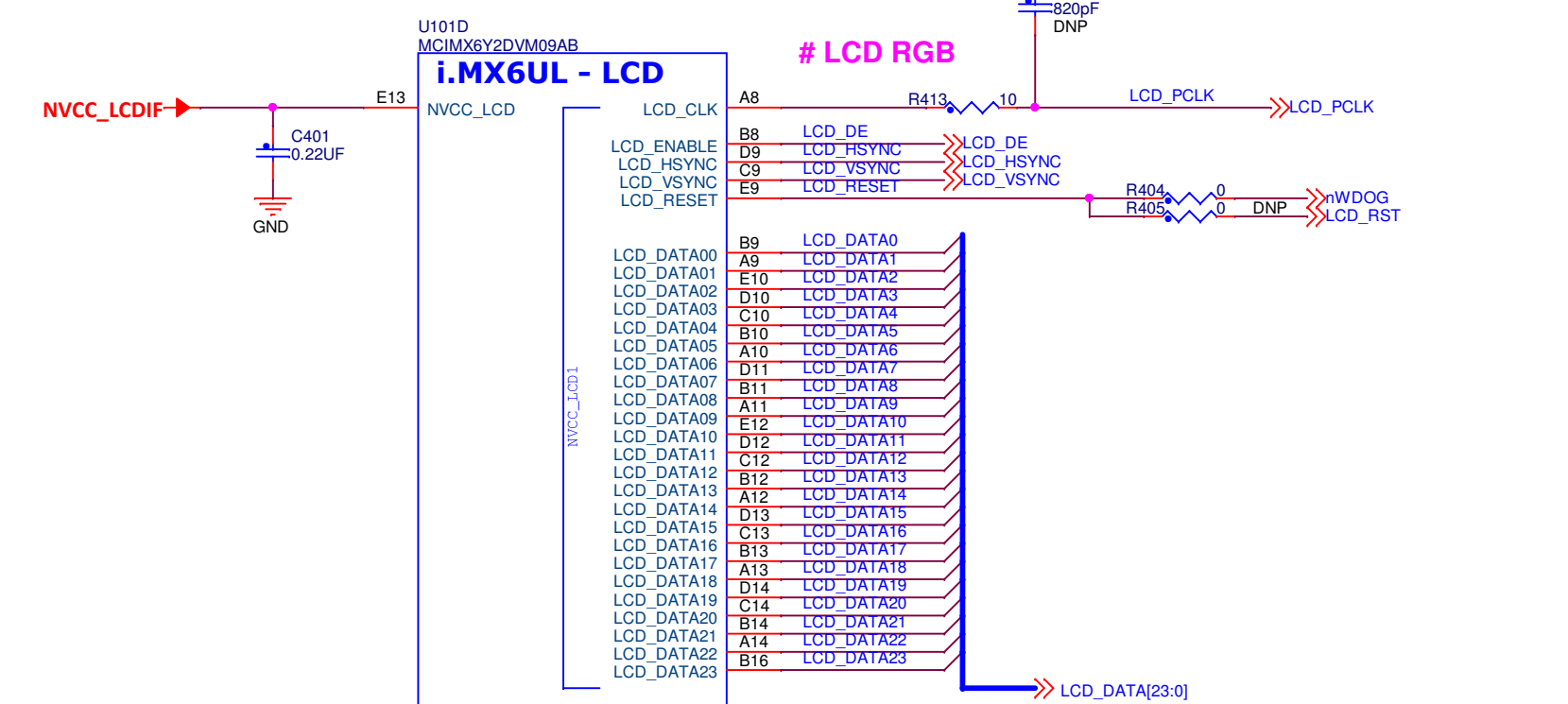
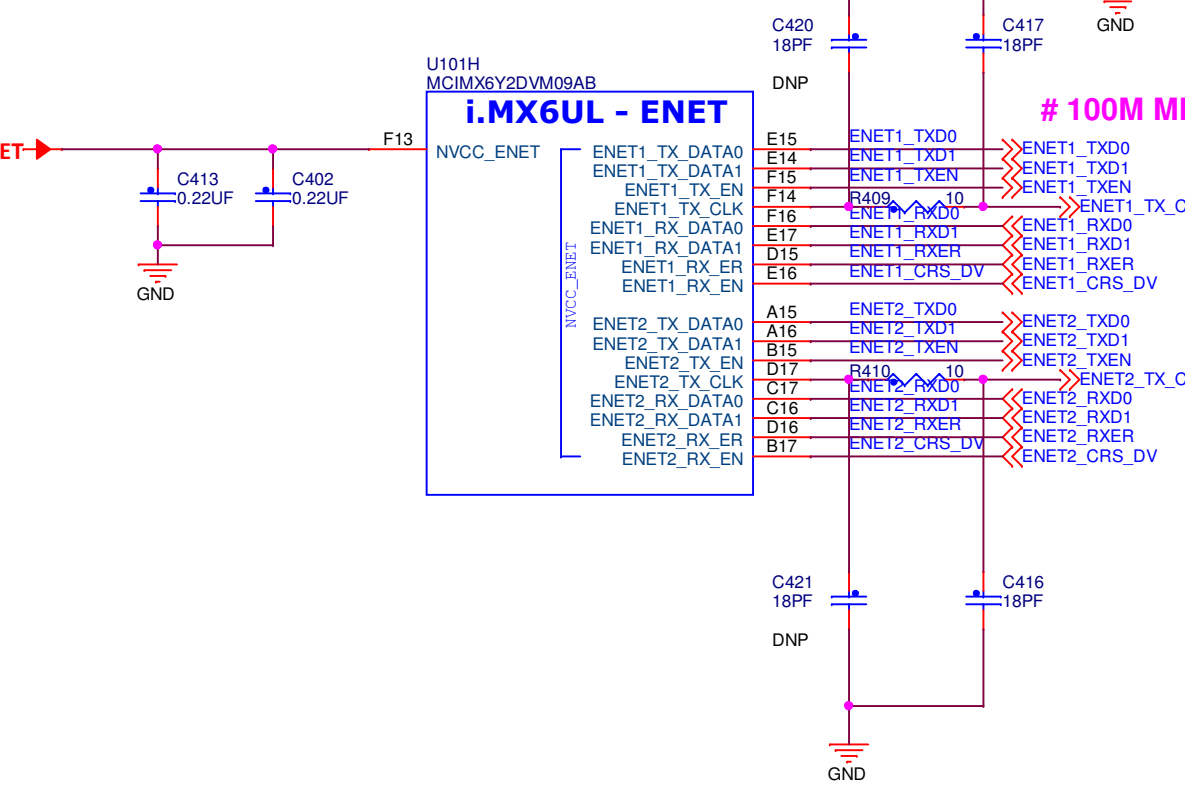
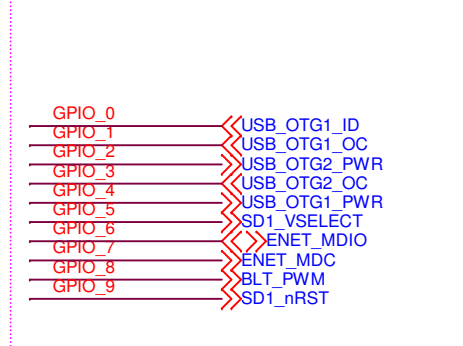
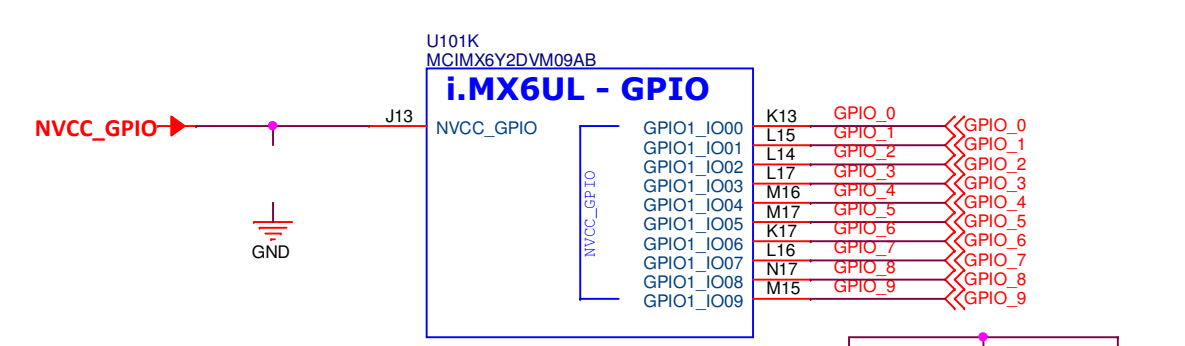
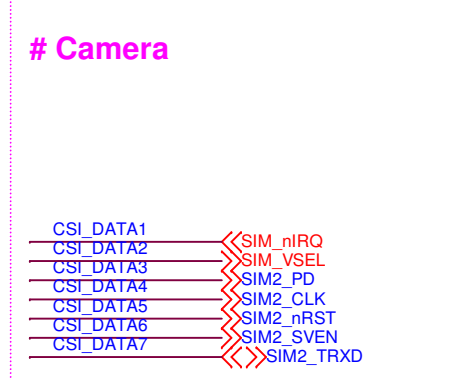
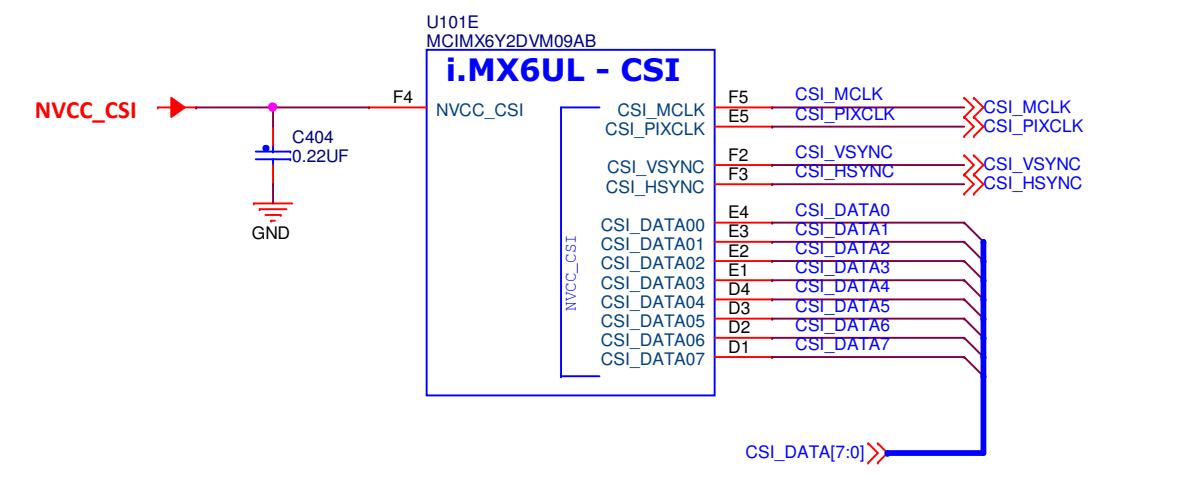
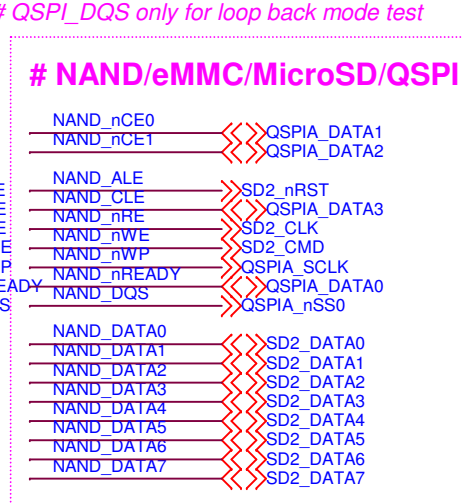
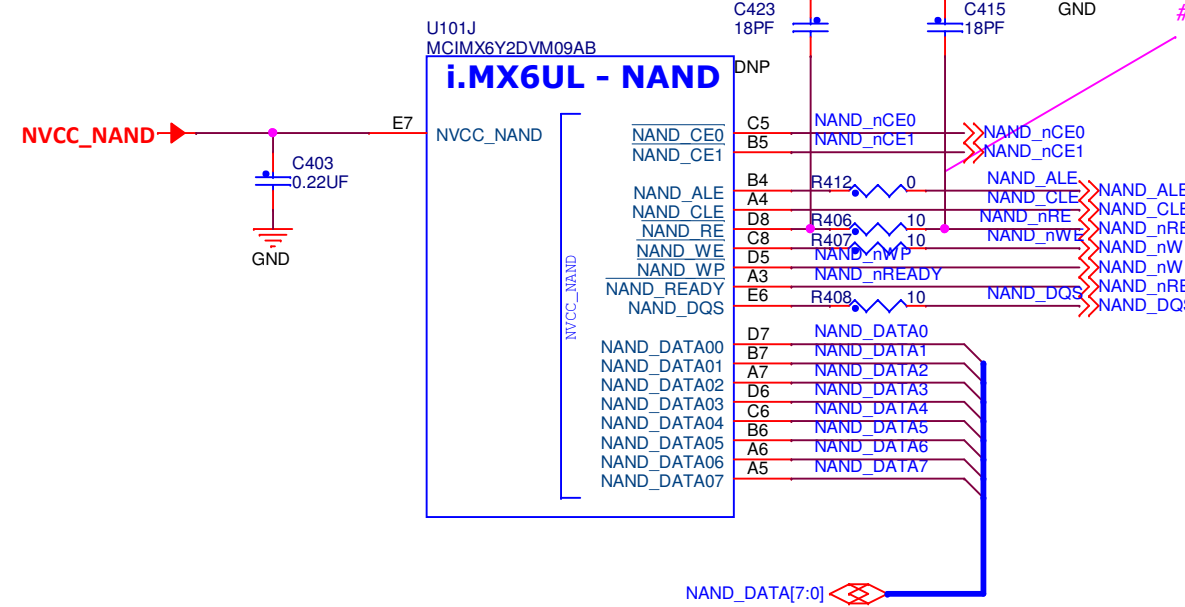
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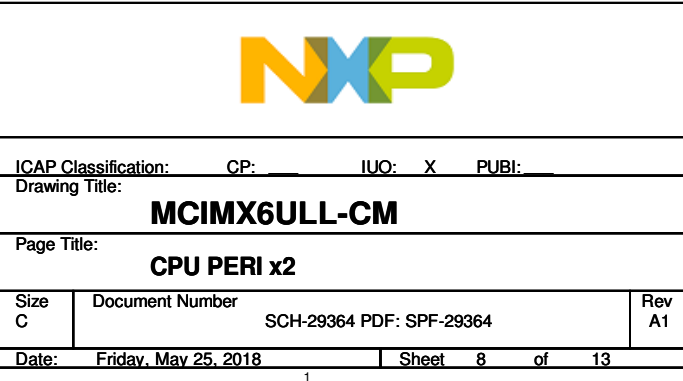
Date: Friday, May 25, 2018

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	Re A1
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MX6ULL PERI





FUSE MAP

<Default: QSPI BOOT>

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved		DDRSMP: "000": Default "001-111"	
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDHC_RST pad (USDHC3 & 4 only)	SD Loopback Clock Source Select (SDR50 and SDR104 only) 0 - through SD pad 1 - direct	
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDHC_RST pad (USDHC3 & 4 only)	SD Loopback Clock Source Select (SDR50 and SDR104 only) 0 - through SD pad 1 - direct
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256	Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved	Nand Row Address Bytes: 00 - 3 01 - 2 10 - 4 11 - 8			

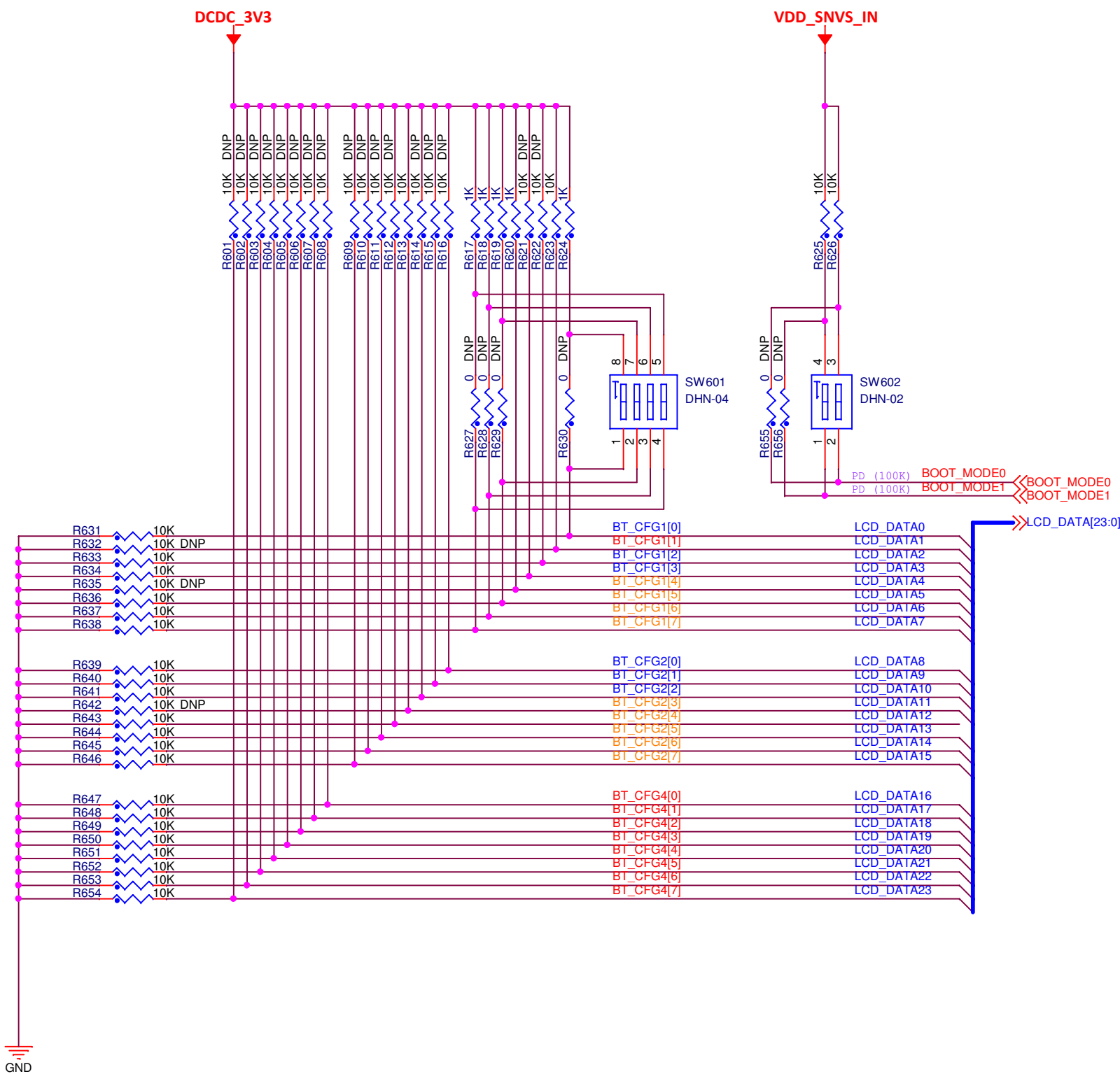
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS: Half Speed Phase Selection 0 - select sampling at non-inverted clock 1 - select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 - one clock delay 1 - two clock delay	SPHS: Full Speed Phase Selection 0 - select sampling at non-inverted clock 1 - select sampling at inverted clock	PSDLY: Full Speed Delay selection 0 - one clock delay 1 - two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11 - Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step "00" - 1 TBD	Bus Width: 0 - 1-bit 1 - 4-bit		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Reserved
NAND	Toggle Mode SDR Mode Preamble Delay, Read Latency: 000 - 16 GPMICLK cycles 001 - 1 GPMICLK cycles 010 - 3 GPMICLK cycles 011 - 3 GPMICLK cycles 100 - 4 GPMICLK cycles 101 - 5 GPMICLK cycles 110 - 6 GPMICLK cycles 111 - 7 GPMICLK cycles			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time 0 - 12ms 1 - 22ms (LBA NAND)	Reserved	Reserved

TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	EEPROM Recovery Enable "0" - Disabled "1" - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3	SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSP1 001 - eCSP2 010 - eCSP3 011 - eCSP4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved		
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE "0" - Disabled "1" - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDRAM Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPRI_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	BLSDHC_IOMUX_SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_DE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR - Bus) "00" - LPB Disable "01" - 1 GHz (def freq) "10" - Div by 2 "11" - Div by 4		BT_LPB_POLARITY (GPIO polarity)		POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)		
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

NAND MT29F32G08CBACA

1 page = (4K + 224 bytes)
1 block = (4K + 224) bytes x 256 pages
= (1024K + 56K) bytes
1 plane = (1024K + 56K) bytes x 2048 blocks
= 17,280Mb
1 LUN = 17,280Mb x 2 planes
= 34,560Mb

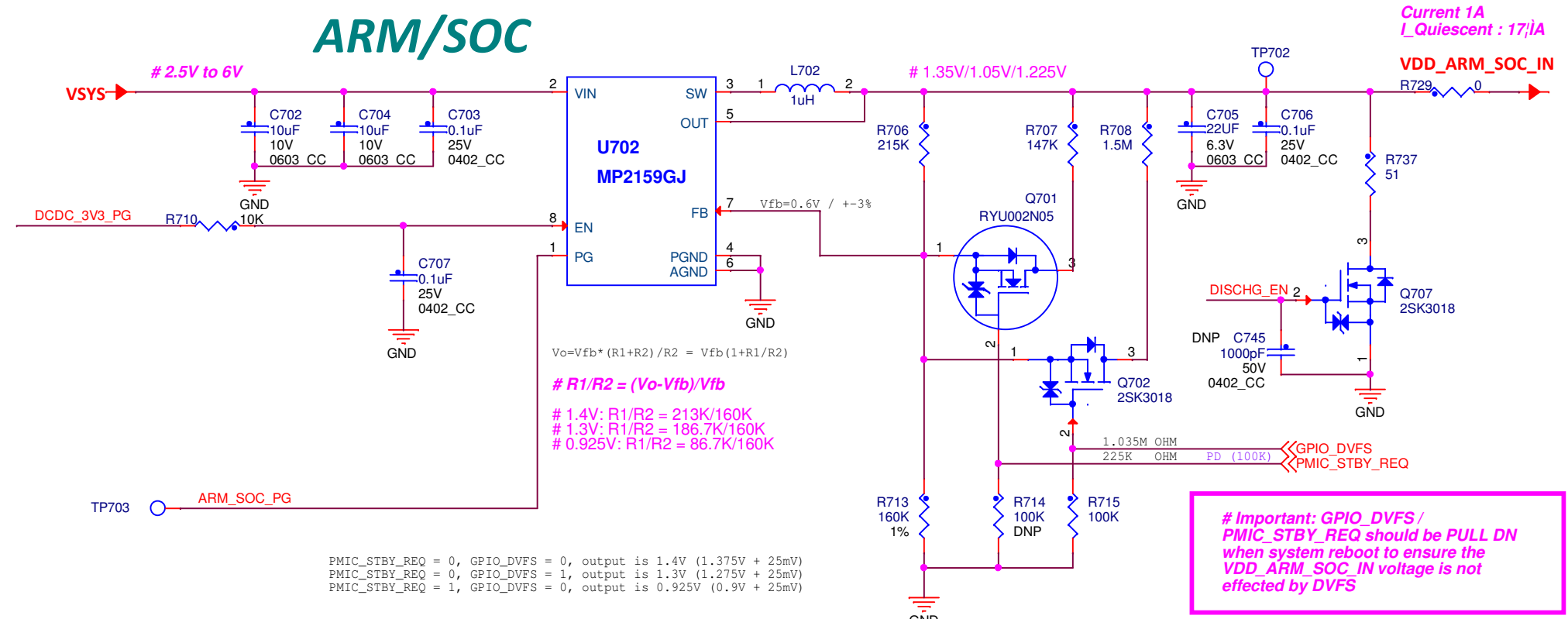
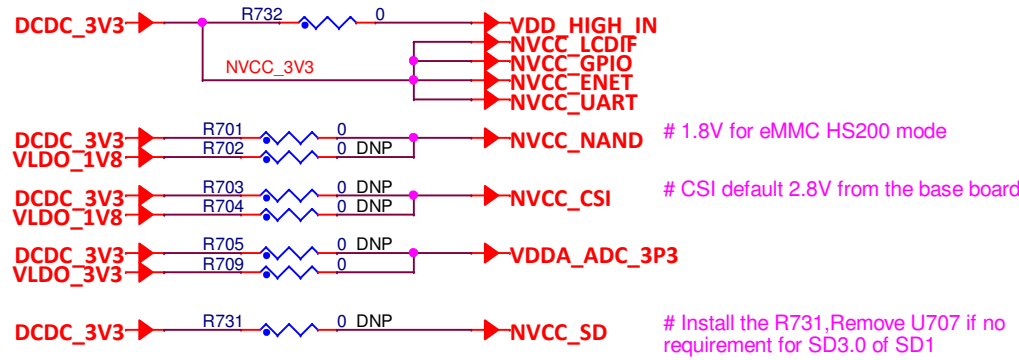
Boot Configuration



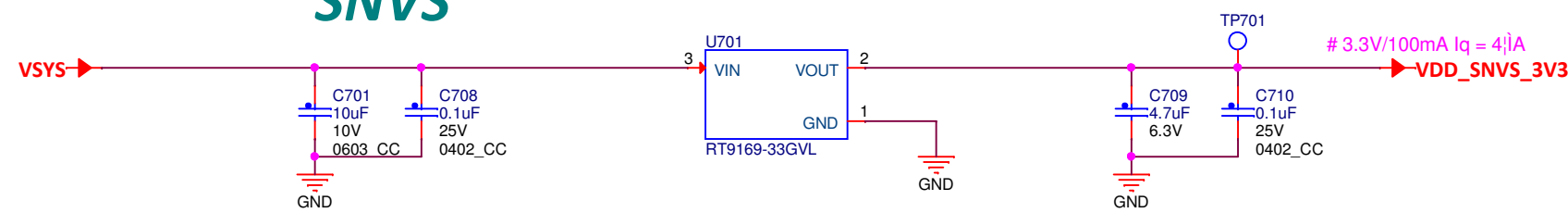
BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved



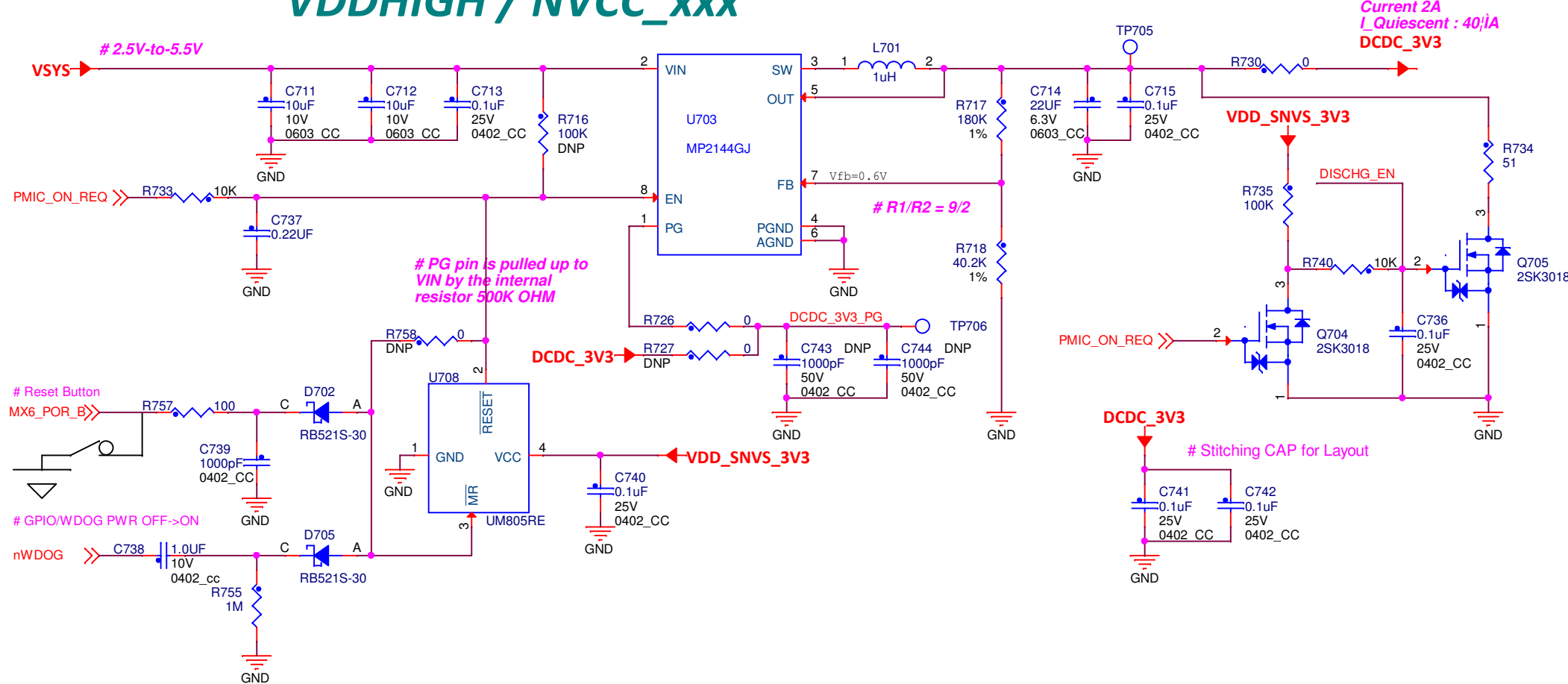
i.MX6ULL PWR				
Power Rail	MIN	TYP	MAX	CURR
VDD_SNVS_IN	2.4	3	3.6	276uA
VDD_HIGH_IN	2.8	3	3.6	125mA
VDD_ARM_IN	0.9	1.275	1.5	400mA
VDD_SOC_IN	0.9	1.275	1.5	500mA
NVCC_DRAM	1.425	1.5	1.575	50mA
	1.283	1.35	1.45	
	1.14	1.2	1.3	
NVCC_XXX	1.65	1.8/2.5/3.3	3.6	
VDDA_ADC_3P3	3	3.3	3.6	
USB_OTG1_VBUS	4.4	5	5.25	50mA
USB_OTG2_VBUS				



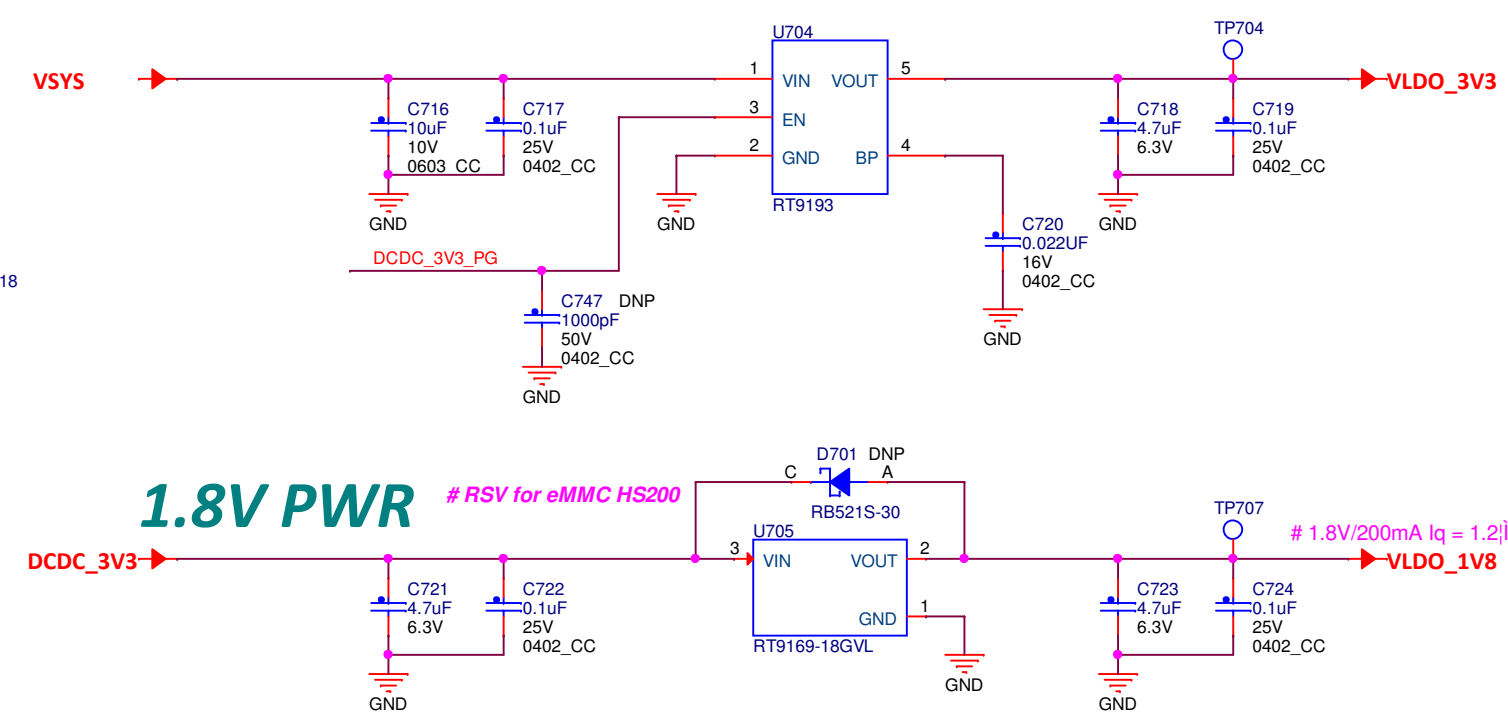
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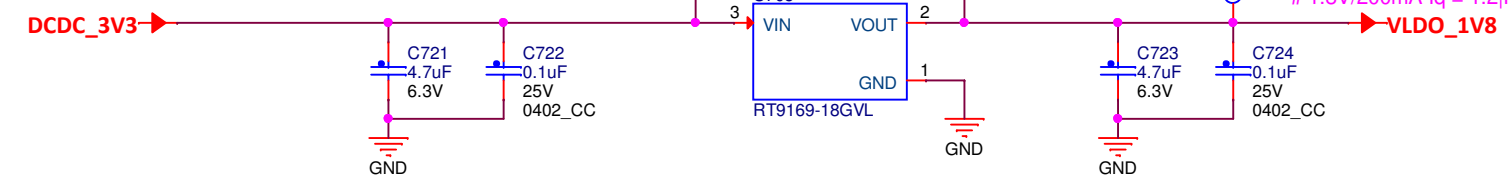
VDDHIGH / NVCC_XXX



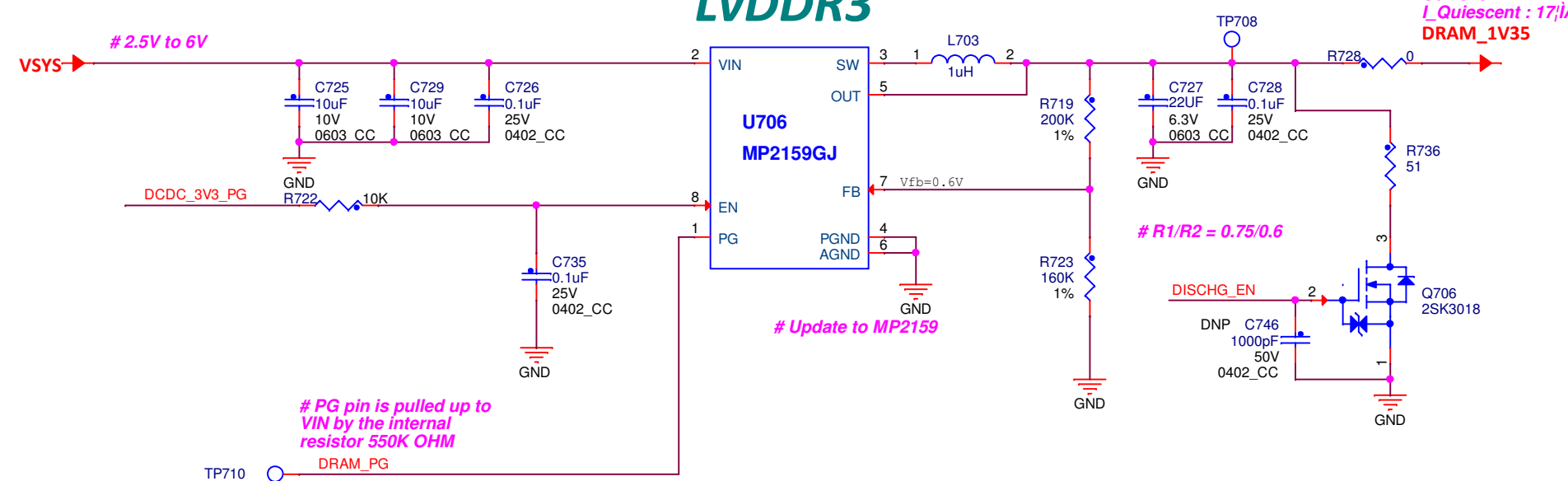
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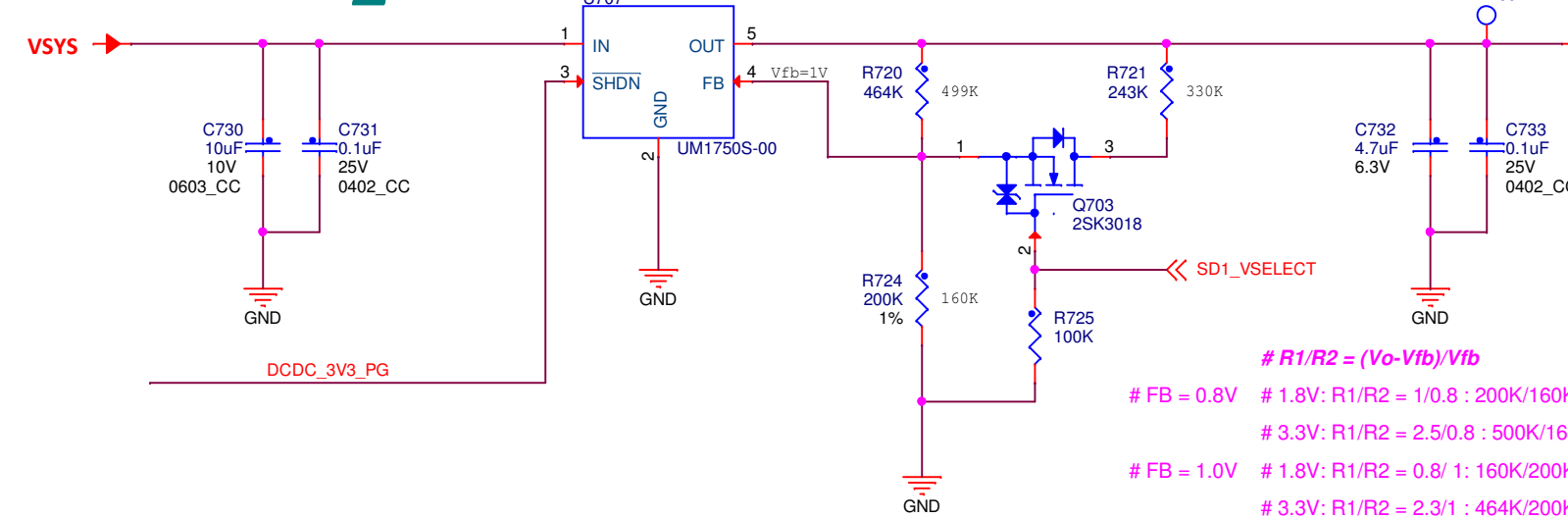
1.8V PWR



LvDDR3



NVCC_SD <SD3.0>



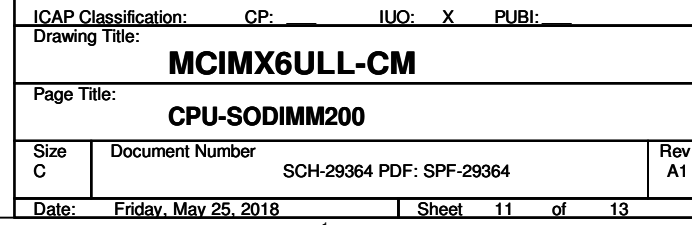
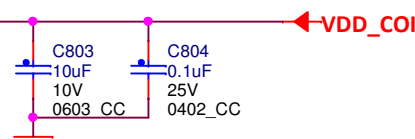
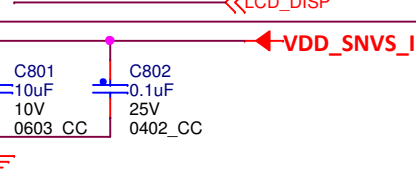
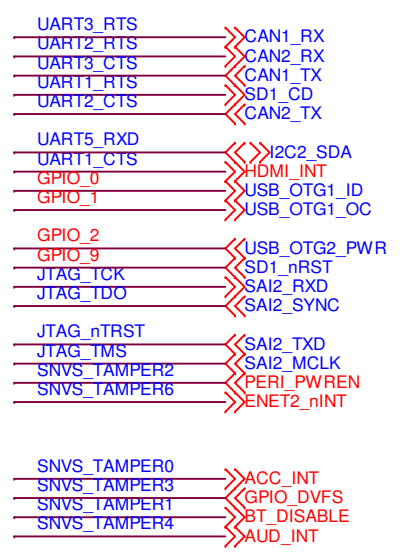
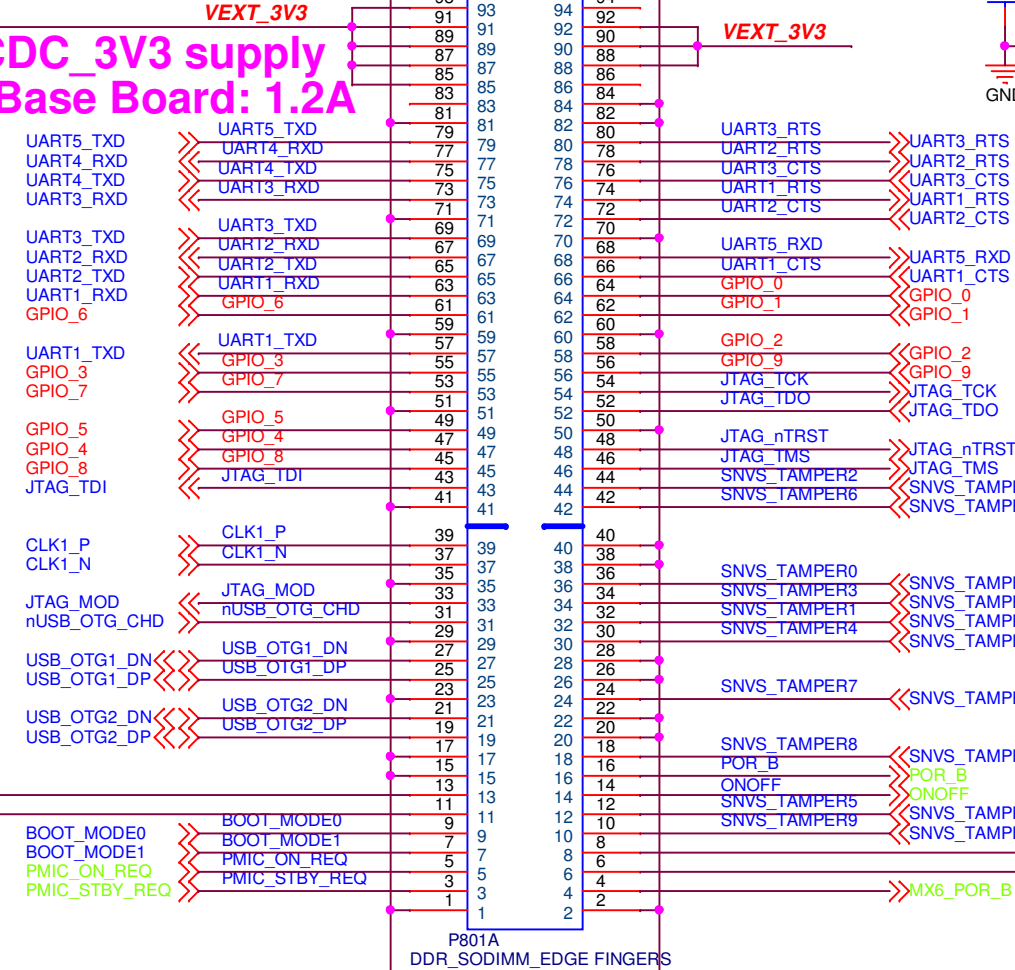
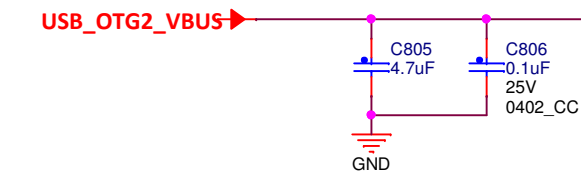
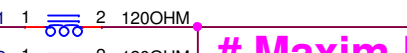
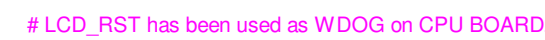
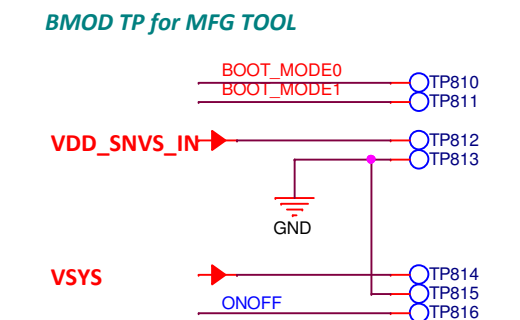
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Drawing Title: MCIMX6ULL-CM	
Page Title: PWR MGR	
Size C	Document Number SCH-29364 PDF: SPF-29364
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CPU SODIMM TST/DBG

Connections:

- CDC3_3V3** (Red arrow) to **TP801**
- UART1_TXD** (Blue line) to **TP802**
- UART1_RXD** (Red line) to **TP803**
- TP804** (Purple line) to **TP805**
- TP805** (Purple line) to **TP806**
- USB_OTG1_DN** (Blue line) to **TP807**
- USB_OTG1_DP** (Blue line) to **TP808**
- TP808** (Blue line) to **TP809**
- USB_OTG1_VBUS** (Red line) to **TP809**
- GND** (Ground symbol) to **TP801**

The schematic diagram illustrates the CSI interface connections. On the left, several signal lines are shown: CSI_DATA[7:0] (blue), LCD_DATA[23:0] (blue), and CSI_VSYNC (purple). These lines are connected to the CSI block. The CSI block is also connected to a power supply network. A 10V supply is connected to the CSI block via a 0.1uF capacitor (C809). A 25V supply is connected to the CSI block via a 0.1uF capacitor (C818). The power supply network is labeled NVCC_CSI. The ground connection is labeled GND.



NOTE:

All pins using ~reset as harden :

PAD	Default State	Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	0 in real silicon
LCD_DATA00~LCD_DATA23	100K pull down + input enable during reset --> Output keeper + Input enable after reset done (this is boot option, we don't need change)	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	sjc.ipt_jta_active --> PAD	0 in real silicon
		(note : sjc.ipt_jta_active also connected to snvs_hp.sec_vio_in_1. This is security related, we don't plan to change it.)	ALT7

All pins using ~src.en_system_clk as harden :

PAD	Default State	Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	PAD --> ccmsrcmix. src_tester_ack	0 in real silicon
		This is the requirement of TE test	ALT7

All pins using snvs_hp.snvs_sec_vio_in_5_en as harden :

PAD	Default State	Simulation Value
CSI_PIXCLK	Output keeper + Input enable (snvs_sec_vio_in_5_en is 1j~ b0 in normal state, so harden is not triggerd in normal state). snvs_sec_vio_in_5_en is controlled by SNVS register. It can be disable or enable.	X (0 or 1 in real silicon)

i.MX6ULL IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	PAD DPU
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE										100K PD
POR_B	src.POR_B	src.POR_B										100K PU
ONOFF	src.RESET_B	src.RESET_B										100K PU
SNVS_PMIC_ON_REQ	snvs_ip_wrapper.SNVS_WAKEUP_ALARM	snvs_ip_wrapper.SNVS_WAKEUP_ALARM										100K PU
CCM_PMIC_STBY_REQ	ccm.PMIC_VSTBY_REQ	ccm.PMIC_VSTBY_REQ										100K PD
BOOT_MODE0	src.BOOT_MODE[0]	src.BOOT_MODE[0]										100K PD
BOOT_MODE1	src.BOOT_MODE[1]	src.BOOT_MODE[1]										100K PD
SNVS_TAMPER0	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[0]										100K PU
SNVS_TAMPER1	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[1]										100K PU
SNVS_TAMPER2	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[2]										100K PU
SNVS_TAMPER3	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[3]										100K PU
SNVS_TAMPER4	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[4]										100K PU
SNVS_TAMPER5	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[5]										100K PU
SNVS_TAMPER6	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[6]										100K PU
SNVS_TAMPER7	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[7]										100K PU
SNVS_TAMPER8	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[8]										100K PU
SNVS_TAMPER9	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[9]										100K PU
JTAG_MOD	src.MOD	src.MOD										100K PU
JTAG_TMS	src.TMS	src.TMS										100K PU
JTAG_TDO	src.TDO	src.TDO										100K PU
JTAG_TDI	src.TDI	src.TDI										100K PU
JTAG_TCK	src.TCK	src.TCK										100K PU
JTAG_TRST_B	src.TRSTB	src.TRSTB										100K PU
GPIO1_I000	gpio1.I0[0]	gpio1.I0[0]										100K PU
GPIO1_I001	gpio1.I0[1]	gpio1.I0[1]										100K PU
GPIO1_I002	gpio1.I0[2]	gpio1.I0[2]										100K PU
GPIO1_I003	gpio1.I0[3]	gpio1.I0[3]										100K PU
GPIO1_I004	gpio1.I0[4]	gpio1.I0[4]										100K PU
GPIO1_I005	gpio1.I0[5]	gpio1.I0[5]										100K PU
GPIO1_I006	gpio1.I0[6]	gpio1.I0[6]										100K PU
GPIO1_I007	gpio1.I0[7]	gpio1.I0[7]										100K PU
GPIO1_I008	gpio1.I0[8]	gpio1.I0[8]										100K PU
GPIO1_I009	gpio1.I0[9]	gpio1.I0[9]										100K PU
UART1_TXD	uart1.TX	uart1.TX										100K PU
UART1_RXD	uart1.RX	uart1.RX										100K PU
UART1_CTS	uart1.CTS	uart1.CTS										100K PU
UART1_RTS	uart1.RTS	uart1.RTS										100K PU
UART2_TXD	uart2.TX	uart2.TX										100K PU
UART2_RXD	uart2.RX	uart2.RX										100K PU
UART2_CTS	uart2.CTS	uart2.CTS										100K PU
UART2_RTS	uart2.RTS	uart2.RTS										100K PU
UART3_TXD	uart3.TX	uart3.TX										100K PU
UART3_RXD	uart3.RX	uart3.RX										100K PU
UART3_CTS	uart3.CTS	uart3.CTS										100K PU
UART3_RTS	uart3.RTS	uart3.RTS										100K PU
UART4_TXD	uart4.TX	uart4.TX										100K PU
UART4_RXD	uart4.RX	uart4.RX										100K PU
UART5_TXD	uart5.TX	uart5.TX										100K PU
UART5_RXD	uart5.RX	uart5.RX										100K PU
ENET1_RXD0	enet1.RXDATA[0]	enet1.RXDATA[0]										100K PU
ENET1_RXD1	enet1.RXDATA[1]	enet1.RXDATA[1]										100K PU
ENET1_CRS	enet1.CRS	enet1.CRS										100K PU
ENET1_TXD0	enet1.TXDATA[0]	enet1.TXDATA[0]										100K PU
ENET1_TXD1	enet1.TXDATA[1]	enet1.TXDATA[1]										100K PU
ENET1_TXD2	enet1.TXDATA[2]	enet1.TXDATA[2]										100K PU
ENET1_TXD3	enet1.TXDATA[3]	enet1.TXDATA[3]										100K PU
ENET1_TXD4	enet1.TXDATA[4]	enet1.TXDATA[4]										100K PU
ENET1_TXD5	enet1.TXDATA[5]	enet1.TXDATA[5]										100K PU
ENET1_TXD6	enet1.TXDATA[6]	enet1.TXDATA[6]										100K PU
ENET1_TXD7	enet1.TXDATA[7]	enet1.TXDATA[7]										100K PU
ENET1_TXD8	enet1.TXDATA[8]	enet1.TXDATA[8]										100K PU
ENET1_TXD9	enet1.TXDATA[9]	enet1.TXDATA[9]										100K PU
ENET1_TXD10	enet1.TXDATA[10]	enet1.TXDATA[10]										100K PU
ENET1_TXD11	enet1.TXDATA[11]	enet1.TXDATA[11]										100K PU
ENET1_TXD12	enet1.TXDATA[12]	enet1.TXDATA[12]										100K PU
ENET1_TXD13	enet1.TXDATA[13]	enet1.TXDATA[13]										100K PU
ENET1_TXD14	enet1.TXDATA[14]	enet1.TXDATA[14]										100K PU
ENET1_TXD15	enet1.TXDATA[15]	enet1.TXDATA[15]										100K PU
ENET1_TXD16	enet1.TXDATA[16]	enet1.TXDATA[16]										100K PU
ENET1_TXD17	enet1.TXDATA[17]	enet1.TXDATA[17]										100K PU
ENET1_TXD18	enet1.TXDATA[18]	enet1.TXDATA[18]										100K PU
ENET1_TXD19	enet1.TXDATA[19]	enet1.TXDATA[19]										100K PU
ENET1_TXD20	enet1.TXDATA[20]	enet1.TXDATA[20]										100K PU
ENET1_TXD21	enet1.TXDATA[21]	enet1.TXDATA[21]										100K PU
ENET1_TXD22	enet1.TXDATA[22]	enet1.TXDATA[22]										100K PU
ENET1_TXD23	enet1.TXDATA[23]	enet1.TXDATA[23]										100K PU
ENET1_TXD24	enet1.TXDATA[24]	enet1.TXDATA[24]										100K PU
ENET1_TXD25	enet1.TXDATA[25]	enet1.TXDATA[25]										100K PU
ENET1_TXD26	enet1.TXDATA[26]	enet1.TXDATA[26]										100K PU
ENET1_TXD27	enet1.TXDATA[27]	enet1.TXDATA[27]										100K PU
ENET1_TXD28	enet1.TXDATA[28]	enet1.TXDATA[28]										100K PU
ENET1_TXD29	enet1.TXDATA[29]	enet1.TXDATA[29]										100K PU
ENET1_TXD30	enet1.TXDATA[30]	enet1.TXDATA[30]										100K PU
ENET1_TXD31	enet1.TXDATA[31]	enet1.TXDATA[31]										100K PU
ENET1_TXD32	enet1.TXDATA[32]	enet1.TXDATA[32]										100K PU
ENET1_TXD33	enet1.TXDATA[33]	enet1.TXDATA[33]										100K PU
ENET1_TXD34	enet1.TXDATA[34]	enet1.TXDATA[34]										100K PU
ENET1_TXD35	enet1.TXDATA[35]	enet1.TXDATA[35]										100K PU
ENET1_TXD36	enet1.TXDATA[36]	enet1.TXDATA[36]										100K PU
ENET1_TXD37	enet1.TXDATA[37]	enet1.TXDATA[37]										100K PU
ENET1_TXD38	enet1.TXDATA[38]	enet1.TXDATA[38]										100K PU
ENET1_TXD39	enet1.TXDATA[39]	enet1.TXDATA[39]										100K PU
ENET1_TXD40	enet1.TXDATA[40]	enet1.TXDATA[40]										100K PU
ENET1_TXD41	enet1.TXDATA[41]	enet1.TXDATA[41]										100K PU
ENET1_TXD42	enet1.TXDATA[42]	enet1.TXDATA[42]										100K PU
ENET1_TXD43	enet1.TXDATA[43]	enet1.TXDATA[43]										100K PU
ENET1_TXD44	enet1.TXDATA[44]	enet1.TXDATA[44]										100K PU
ENET1_TXD45	enet1.TXDATA[45]	enet1.TXDATA[45]										100K PU
ENET1_TXD46	enet1.TXDATA[46]	enet1.TXDATA[46]										100K PU
ENET1_TXD47	enet1.TXDATA[47]	enet1.TXDATA[47]										100K PU
ENET1_TXD48	enet1.TXDATA[48]	enet1.TXDATA[48]										100K PU
ENET1_TXD49	enet1.TXDATA[49]	enet1.TXDATA[49]										100K PU
ENET1_TXD50	enet1.TXDATA[50]	enet1.TXDATA[50]										100K PU
ENET1_TXD51	enet1.TXDATA[51]	enet1.TXDATA[51]										100K PU
ENET1_TXD52	enet1.TXDATA[52]	enet1.TXDATA[52]										100K PU
ENET1_TXD53	enet1.TXDATA[53]	enet1.TXDATA[53]										100K PU
ENET1_TXD54	enet1.TXDATA[54]	enet1.TXDATA[54]										100K PU
ENET1_TXD55	enet1.TXDATA[55]	enet1.TXDATA[55]										100K PU
ENET1_TXD56	enet1.TXDATA[56]	enet1.TXDATA[56]										100K PU
ENET1_TXD57	enet1.TXDATA[57]	enet1.TXDATA[57]										100K PU
ENET1_TXD58	enet1.TXDATA[58]	enet1.TXDATA[58]										100K PU
ENET1_TXD59	enet1.TXDATA[59]	enet1.TXDATA[59]										100K PU
ENET1_TXD60	enet1.TXDATA[60]	enet1.TXDATA[60]										100K PU
ENET1_TXD61	enet1.TXDATA[61]	enet1.TXDATA[61]										100K PU
ENET1_TXD62	enet1.TXDATA[62]	enet1.TXDATA[62]										100K PU
ENET1_TXD63	enet1.TXDATA[63]	enet1.TXDATA[63]										100K PU
ENET1_TXD64	enet1.TXDATA[64]	enet1.TXDATA[64]										100K PU
ENET1_TXD65	enet1.TXDATA[65]	enet1.TXDATA[65]										100K PU
ENET1_TXD66	enet1.TXDATA[66]	enet1.TXDATA[66]										100K PU
ENET1_TXD67	enet1.TXDATA[67]	enet1.TXDATA[67]										100K PU
ENET1_TXD68	enet1.TXDATA[68]	enet1.TXDATA[68]										100K PU
ENET1_TXD69	enet1.TXDATA[69]	enet1.TXDATA[69]										100K PU
ENET1_TXD70	enet1.TXDATA[70]	enet1.TXDATA[70]										100K PU
ENET1_TXD71	enet1.TXDATA[71]	enet1.TXDATA[71]										100K PU
ENET1_TXD72	enet1.TXDATA[72]	enet1.TXDATA[72]										100K PU
ENET1_TXD73	enet1.TXDATA[73]	enet1.TXDATA[73]										100K PU
ENET1_TXD74	enet1.TXDATA[74]	enet1.TXDATA[74]										100K PU
ENET1_TXD75	enet1.TXDATA[75]	enet1.TXDATA[75]										100K PU
ENET1_TXD76	enet1.TXDATA[76]	enet1.TXDATA[76]										100K PU
ENET1_TXD77	enet1.TXDATA[77]	enet1.TXDATA[77]										100K PU
ENET1_TXD78	enet1.TXDATA[78]	enet1.TXDATA[78]										100K PU
ENET1_TXD79	enet1.TXDATA[79]	enet1.TXDATA[79]										100K PU
ENET1_TXD80	enet1.TXDATA[80]	enet1.TXDATA[80]										100K PU
ENET1_TXD81	enet1.TXDATA[81]	enet1.TXDATA[81]										100K PU
ENET1_TXD82	enet1.TXDATA[82]	enet1.TXDATA[82]										100K PU
ENET1_TXD83	enet1.TXDATA[83]	enet1.TXDATA[83]										100K PU
ENET1_TXD84	enet1.TXDATA[84]	enet1.TXDATA[84]										100K PU
ENET1_TXD85	enet1.TXDATA[85]	enet1.TXDATA[85]										100K PU
ENET1_TXD86	enet1.TXDATA[86]	enet1.TXDATA[86]										100K PU
ENET1_TXD87	enet1.TXDATA[87]	enet1.TXDATA[87]										100K PU
ENET1_TXD88	enet1.TXDATA[88]	enet1.TXDATA[88]										100K PU
ENET1_TXD89	enet1.TXDATA[89]	enet1.TXDATA[89]										100K PU
ENET1_TXD90	enet1.TXDATA[90]	enet1.TXDATA[90]										100K PU
ENET1_TXD91	enet1.TXDATA[91]	enet1.TXDATA[9										