Rockchip
RK3576
Technical Reference Manual
(Part 1)

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Revision History

Date	Revision	Description
2024-06-24	1.2	Reorganize the oder of chapters; Update the following chapters: System Overview, CRU, GRF, PMU, MCU, WDT, PDM, PWM, SPI, I2C, FlexBUS.
2024-04-02	1.1	Update GRF. NPU, Mobile Storage Host Controller, CRU chapters
2024-03-18	1.0	Initial Release

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Chapter 1 System Overview

1.1 Address Mapping

RK3576 boot from internal BOOTROM, which supports remap function by software programming. Remap is controlled by PMU_SGRF_SOC_CON2[1:0]. When remap is set to 2'b01, the BOOTROM is un-accessible and PMU_SRAM is mapped to address 0x00000000. When remap is set to 2'b10, the BOOTROM is un-accessible and SYSTEM_SRAM is mapped to address 0x00000000.

Table 1-1 Address Mapping

Module	Start Address	Size	Module	Start Address	Size
DSMC_MEM	0x10000000	256MB	DDRMON0	0x2A000000	64KB
PCIE0_S	0x20000000	16MB	DDRMON1	0x2A010000	64KB
PCIE1_S	0x21000000	16MB	DDRPHY0	0x2A020000	64KB
PCIE0_DBI	0x22000000	4MB	DDRPHY1	0x2A030000	64KB
PCIE1_DBI	0x22400000	4MB	DDR_WDT	0x2A040000	64KB
DAP_ROM	0x22800000	4MB	DDR_TIMER(2CH)	0x2A050000	64KB
USB0	0x23000000	4MB	HWLP0	0x2A060000	64KB
USB1	0x23400000	4MB	HWLP1	0x2A070000	64KB
MCU_TCM	0x23800000	64KB	AHB2APB	0x2A080000	64KB
MCU_CACHE	0x23810000	64KB	DMA2DDR	0x2A100000	64KB
MCU_RAM_TEST	0x23820000	64KB	PCIE0_APB	0x2A200000	64KB
PMU0_SGRF	0x26000000	8KB	PCIE1_APB	0x2A210000	64KB
PMU1_SGRF	0x26002000	4KB	GMAC0	0x2A220000	64KB
FW_PMUSGRF	0x26003000	4KB	GMAC1	0x2A230000	64KB
SYS_SGRF	0x26004000	4KB	SATA0	0x2A240000	64KB
FW_SYSSGRF	0x26005000	4KB	SATA1	0x2A250000	64KB
SYS_GRF	0x2600A000	8KB	MMU0	0x2A260000	64KB
BIGCORE_GRF	0x2600C000	8KB	MMU1	0x2A270000	64KB
LITCORE_GRF	0x2600E000	8KB	DSMC_CFG	0x2A280000	64KB
CCI_GRF	0x26010000	8KB	MMU2	0x2A2C0000	64KB
DDR_GRF	0x26012000	8KB	UFSHC_AXIS	0x2A2D0000	64KB
CENTER_GRF	0x26014000	8KB	UFSHC_APBS	0x2A2E0000	64KB

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Module	Start Address	Size	Module	Start Address	Size
GPU_GRF	0x26016000	8KB	FLEXBUS	0x2A2F0000	64KB
NPU_GRF	0x26018000	8KB	FSPI1	0x2A300000	64KB
VO0_GRF	0x2601A000	8KB	SDMMC	0x2A310000	64KB
USB_GRF	0x2601E000	4KB	SDIO	0x2A320000	64KB
PHP_GRF	0x26020000	8KB	EMMC	0x2A330000	64KB
VOP_GRF	0x26022000	8KB	FSPI0	0x2A340000	64KB
PMU0_GRF	0x26024000	8KB	NSCRYPTO	0x2A400000	64KB
PMU1_GRF	0x26026000	8KB	RKRNG_NS	0x2A410000	64KB
COMBO_PIPE_PHY0_GRF	0x26028000	8KB	KEYLAD	0x2A420000	64KB
COMBO_PIPE_PHY1_GRF	0x2602A000	8KB	SCRYPTO	0x2A430000	64KB
USBDPPHY_GRF	0x2602C000	8KB	RKRNG_S	0x2A440000	64KB
USB2PHY0_GRF	0x2602E000	8KB	OTPC_S	0x2A480000	64KB
USB2PHY1_GRF	0x26030000	8KB	TIMER_S_0(6CH)	0x2A4A0000	64KB
HDPTXPHY_GRF	0x26032000	8KB	TIMER_S_1(6CH)	0x2A4B0000	64KB
DCPHY_GRF	0x26034000	8KB	WDT_S	0x2A4C0000	64KB
VO1_GRF	0x26036000	8KB	OTPMASK	0x2A4D0000	64KB
SDGMAC_GRF	0x26038000	8KB	JTAG_LOCK	0x2A4E0000	64KB
CSIDPHY0_GRF	0x2603A000	8KB	OTPC_NS	0x2A580000	64KB
MPHY_GRF	0x2603C000	8KB	SAI0	0x2A600000	64KB
PMU0_IOC	0x26040000	8KB	SAI1	0x2A610000	64KB
PMU1_IOC	0x26042000	8KB	SAI2	0x2A620000	64KB
TOP_IOC	0x26044000	8KB	SAI3	0x2A630000	64KB
VCCIO_IOC	0x26046000	8KB	SAI4	0x2A640000	64KB
VCCIO6_IOC	0x2604A000	4KB	SPDIF_RX0	0x2A650000	64KB
VCCIO7_IOC	0x2604B000	4KB	SPDIF_RX1	0x2A660000	64KB
CSIDPHY1_GRF	0x2604C000	8KB	SPDIF_TX0	0x2A670000	64KB
CRU	0x27200000	32KB	SPDIF_TX1	0x2A680000	64KB

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Module	Start Address	Size	Module	Start Address	Size
PPLL_CRU	0x27208000	32KB	ASRC4CH_0	0x2A690000	64KB
SECURE_CRU	0x27210000	32KB	ASRC4CH_1	0x2A6A0000	64KB
PMU1_CRU	0x27220000	32KB	ASRC2CH_0	0x2A6B0000	64KB
DDR0_CRU	0x27228000	32KB	ASRC2CH_1	0x2A6C0000	64KB
DDR1_CRU	0x27230000	32KB	ACDCDIG_DSM	0x2A6D0000	64KB
BIGCORE_CRU	0x27238000	32KB	PDM1	0x2A6E0000	64KB
LITCORE_CRU	0x27240000	32KB	GIC400	0x2A700000	4MB
CCI_CRU	0x27248000	32KB	SPINLOCK	0x2AB00000	64KB
CCI_PVTPLL	0x27250000	32KB	DMAC0_S	0x2AB80000	64KB
BIGCORE_PVTPLL	0x27258000	32KB	DMAC0_NS	0x2AB90000	64KB
LITCORE_PVTPLL	0x27260000	32KB	DMAC1_S	0x2ABA0000	64KB
GPU_PVTPLL	0x27268000	32KB	DMAC1_NS	0x2ABB0000	64KB
NPU_PVTPLL	0x27270000	32KB	DMAC2_S	0x2ABC0000	64KB
CRU_PVTPLL	0x27278000	32KB	DMAC2_NS	0x2ABD0000	64KB
DDR_PVTPLL	0x27280000	32KB	I3C0	0x2ABE0000	64KB
I2C0	0x27300000	64KB	I3C1	0x2ABF0000	64KB
UART1	0x27310000	64KB	CAN0	0x2AC00000	64KB
GPIO0	0x27320000	64KB	CAN1	0x2AC10000	64KB
PWM0_2CH	0x27330000	64KB	DECOM	0x2AC30000	64KB
PMU_WDT	0x27340000	64KB	I2C1	0x2AC40000	64KB
PMU_TIMER(2CH)	0x27350000	64KB	I2C2	0x2AC50000	64KB
PMU	0x27360000	64KB	I2C3	0x2AC60000	64KB
PDM0	0x273B0000	64KB	I2C4	0x2AC70000	64KB
VDMA	0x273C0000	64KB	I2C5	0x2AC80000	64KB
OSC_CHK	0x273D0000	64KB	I2C6	0x2AC90000	64KB
SCRAMBLE_KEY	0x273E0000	64KB	I2C7	0x2ACA0000	64KB
PMU_PVTM	0x273F0000	64KB	I2C8	0x2ACB0000	64KB

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Module	Start Address	Size	Module	Start Address	Size
HPTIMER	0x27400000	64KB	TIMER_NS_0(6CH)	0x2ACC0000	64KB
CCI	0x27500000	1MB	TIMER_NS_1(6CH)	0x2ACD0000	64KB
RKNN TOP	0x27700000	64KB	WDT_NS	0x2ACE0000	64KB
RKNN_NSP	0x27710000	64KB	SPI0	0x2ACF0000	64KB
NPU_WDT	0x27780000	64KB	SPI1	0x2AD00000	64KB
NPU_TIMER(2CH)	0x27790000	64KB	SPI2	0x2AD10000	64KB
GPU	0x27800000	128KB	SPI3	0x2AD20000	64KB
EBC	0x27900000	64KB	SPI4	0x2AD30000	64KB
JPEG	0x27910000	64KB	UART0	0x2AD40000	64KB
RGA0	0x27920000	64KB	UART2	0x2AD50000	64KB
RGA1	0x27930000	64KB	UART3	0x2AD60000	64KB
VDPP	0x27960000	64KB	UART4	0x2AD70000	64KB
VEPU0	0x27A00000	64KB	UART5	0x2AD80000	64KB
VEPU1	0x27A10000	64KB	UART6	0x2AD90000	64KB
RKVDEC	0x27B00000	64KB	UART7	0x2ADA0000	64KB
ISP	0x27C00000	64KB	UART8	0x2ADB0000	64KB
VICAP	0x27C10000	128KB	UART9	0x2ADC0000	64KB
VPSS	0x27C30000	64KB	PWM1_6CH	0x2ADD0000	64KB
CSIHOST0	0x27C80000	64KB	PWM2_8CH	0x2ADE0000	64KB
CSIHOST1	0x27C90000	64KB	SARADC	0x2AE00000	64KB
CSIHOST2	0x27CA0000	64KB	GPIO1	0x2AE10000	64KB
CSIHOST3	0x27CB0000	64KB	GPIO2	0x2AE20000	64KB
CSIHOST4	0x27CC0000	64KB	GPIO3	0x2AE30000	64KB
VOP	0x27D00000	64KB	GPIO4	0x2AE40000	64KB
HDCP0_MMU	0x27D10000	64KB	MAILBOX	0x2AE50000	64KB
SPDIF_TX2	0x27D20000	64KB	TSADC	0x2AE70000	64KB
SPDIF_RX2	0x27D30000	64KB	I2C9	0x2AE80000	64KB

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Module	Start Address	Size	Module	Start Address	Size
SAI5	0x27D40000	64KB	INTMUX2PMU (MCU_PMU)	0x2AE90000	64KB
SAI6	0x27D50000	64KB	INTMUX2DDR (MCU_DDR)	0x2AEA0000	64KB
DSIHOST	0x27D80000	64KB	BUS_WDT	0x2AEB0000	64KB
HDCP0	0x27D90000	64KB	INTMUX2BUS (MCU_BUS)	0x2AEC0000	64KB
HDMITX	0x27DA0000	128KB	UART10	0x2AFC0000	64KB
eDP	0x27DC0000	64KB	UART11	0x2AFD0000	64KB
HDCP0_TRNG	0x27DD0000	64KB	HDPTXPHY	0x2B000000	64KB
HDCP0_KEY	0x27E00000	64KB	USBDPPHY	0x2B010000	64KB
eDP_S	0x27E20000	64KB	DCPHY	0x2B020000	64KB
HDCP1_KEY	0x27E30000	64KB	CSIDPHY0	0x2B030000	64KB
DP	0x27E40000	192KB	MPHY	0x2B040000	64KB
HDCP1	0x27E70000	64KB	COMBO_PIPE_PHY0	0x2B050000	64KB
HDCP1_TRNG	0x27E80000	64KB	COMBO_PIPE_PHY1	0x2B060000	64KB
HDCP1_MMU	0x27E90000	64KB	CSIDPHY1	0x2B070000	64KB
SPDIF_TX3	0x27EA0000	64KB	PMU_SRAM	0x3fe70000	32KB
SPDIF_TX4	0x27EB0000	64KB	CBUF	0x3fe80000	1MB
SPDIF_TX5	0x27EC0000	64KB	SYSTEM_SRAM	0x3ff80000	512KB
SAI7	0x27ED0000	64KB	PCIE0_S	0x900000000	2048MB
SAI8	0x27EE0000	64KB	PCIE1_S	0x980000000	2048MB
SAI9	0x27EF0000	64KB	PCIE0_DBI	0xA00000000	4MB
INTERCONNECT	0x27F00000	512KB	PCIE1_DBI	0xA00400000	4MB
DDRCTL0	0x28000000	16MB	MSCH_DDR_PORT	0x40000000	16G
DDRCTL1	0x29000000	16MB			

The following table shows the boot address before remap and after remap

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Table 1-2 Address Remapping

remap[1:0]=2'b00		remap[1:0]=2'b01		remap[1:0]=2'b10	
		not accessible	BOOTROM(32KB)	not accessible	BOOTROM(32KB)
0x00000000	BOOTROM(32KB)	0x00000000	PMU_SRAM(32KB)	0x00000000	SYSTEM_SRAM (512KB)
0x3FE70000	PMU_SRAM(32KB)	0x3FE70000	PMU_SRAM(32KB)	0x3FE70000	PMU_SRAM(32KB)
0x3FF80000	SYSTEM_SRAM (512KB)	0x3FF80000	SYSTEM_SRAM (512KB)	0x3FF80000	SYSTEM_SRAM (512KB)

1.2 System Boot

RK3576 provides system boot from off-chip devices such as SDMMC card, eMMC memory, serial Nand or Nor flash, UFS. When boot code is not ready in these devices, the system code can also be downloaded to these devices through the USB OTG interface. All of the boot code will be stored in internal BOOTROM. The following is the whole boot procedure for boot code, which will be stored in BOOTROM in advance.
The following features are supported.

- Support system boot from the following device:
  - Serial Nor Flash, 1bit, 4bits or 8bits data width(device layout in FSPI IO)
  - Serial Nand Flash, 1bit, 4bits or 8bits data width(device layout in FSPI IO)
  - eMMC Interface, 8bits data width
  - SDMMC Card, 4bits data width
  - UFS Device
- Support system code download by USB OTG
- Support cryptographic algorithms: AES-128, SM4, SHA-256, SM3, SM2, RSA-4096, RSA-2048

1.3 System Interrupt Connection

RK3576 provides an general interrupt controller (GIC) for CPU, which has 480 SPI (shared peripheral interrupt) sources and 4 PPI(Private peripheral interrupt) sources. The triggered type for each SPI interrupt is high level sensitive, and triggered type for each PPI interrupt is low level sensitive, not programmable. The detailed interrupt sources connection is in the following table.

Table 1-3 RK3576 Interrupt Connection List

Number	Source	Polarity	Number	Source	Polarity
0~15	NA	SGI	222	irq_sai3	High level
16~24	NA	PPI	223	irq_sai4	High level
25	NA		224	irq_sai5	High level
26	hypervisor timer		225	irq_sai6	High level
27	virtual timer		226	irq_sai7	High level
28	NA		227	irq_spdif_tx0	High level
29	secure physical timer		228	irq_spdif_tx1	High level
30	non-secure physical timer		229	irq_spdif_tx2	High level
31	NA		230	irq_spdif_tx3	High level
32	~npmuirq_0	High level	231	irq_spdif_rx0	High level
33	~npmuirq_1	High level	232	irq_spdif_rx1	High level

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Number	Source	Polarity	Number	Source	Polarity
34	~npmuirq_2	High level	233	irq_spdif_rx2	High level
35	~npmuirq_3	High level	234	irq_pdm0	High level
36	~npmuirq_4	High level	235	irq_pdm1	High level
37	~npmuirq_5	High level	236	irq_vdma	High level
38	~npmuirq_6	High level	237	irq_asrc_4ch_0	High level
39	~npmuirq_7	High level	238	irq_asrc_4ch_1	High level
40	NA	High level	239	irq_asrc_2ch_0	High level
41	NA	High level	240	irq_asrc_2ch_1	High level
42	NA	High level	241	irq_dma2ddr	High level
43	NA	High level	242	irq_ddr_arpoison_0_ch0	High level
44	NA	High level	243	irq_ddr_awpoison_0_ch0	High level
45	NA	High level	244	irq_ddr_arpoison_1_ch0	High level
46	NA	High level	245	irq_ddr_awpoison_1_ch0	High level
47	NA	High level	246	irq_ddr_arpoison_2_ch0	High level
48	~ncommirq0	High level	247	irq_ddr_awpoison_2_ch0	High level
49	~ncommirq1	High level	248	irq_ddr_arpoison_3_ch0	High level
50	~ncommirq2	High level	249	irq_ddr_awpoison_3_ch0	High level
51	~ncommirq3	High level	250	irq_ddr_arpoison_4_ch0	High level
52	~ncommirq4	High level	251	irq_ddr_awpoison_4_ch0	High level
53	~ncommirq5	High level	252	irq_derate_temp_limit_ch0	High level
54	~ncommirq6	High level	253	irq_ddrmon0	High level
55	~ncommirq7	High level	254	irq_ddr_arpoison_0_ch1	High level
56	~exterrirq0	High level	255	irq_ddr_awpoison_0_ch1	High level
57	~exterrirq1	High level	256	irq_ddr_arpoison_1_ch1	High level
58	~ninterrirq0	High level	257	irq_ddr_awpoison_1_ch1	High level
59	~ninterrirq1	High level	258	irq_ddr_arpoison_2_ch1	High level
60	NA	High level	259	irq_ddr_awpoison_2_ch1	High level
61	NA	High level	260	irq_ddr_arpoison_3_ch1	High level
62	NA	High level	261	irq_ddr_awpoison_3_ch1	High level
63	NA	High level	262	irq_ddr_arpoison_4_ch1	High level
64	irq_dmac0	High level	263	irq_ddr_awpoison_4_ch1	High level
65	irq_dmac0_abort	High level	264	irq_derate_temp_limit_ch1	High level

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Number	Source	Polarity	Number	Source	Polarity
66	irq_dmac1	High level	265	irq_ddrmon1	High level
67	irq_dmac1_abort	High level	266	irq_ahb2apb	High level
68	irq_dmac2	High level	267	irq_fw_center2ddr_main	High level
69	irq_dmac2_abort	High level	268	irq_fw_cci2ddr_main	High level
70	irq_decom	High level	269	irq_bus_mcu_cache	High level
71	irq_wdt_s	High level	270	irq_cci_error	High level
72	irq_wdt_ns	High level	271	irq_nevntcntoverflow_cci_0	High level
73	irq_pmu_wdt	High level	272	irq_nevntcntoverflow_cci_1	High level
74	irq_ddr_wdt	High level	273	irq_nevntcntoverflow_cci_2	High level
75	irq_npu_wdt	High level	274	irq_nevntcntoverflow_cci_3	High level
76	irq_bus_wdt	High level	275	irq_nevntcntoverflow_cci_4	High level
77	irq_timer_ns_0_ch0	High level	276	irq_nevntcntoverflow_cci_5	High level
78	irq_timer_ns_0_ch1	High level	277	irq_nevntcntoverflow_cci_6	High level
79	irq_timer_ns_0_ch2	High level	278	irq_nevntcntoverflow_cci_7	High level
80	irq_timer_ns_0_ch3	High level	279	irq_rknn_core0	High level
81	irq_timer_ns_0_ch4	High level	280	irq_rknn_core1	High level
82	irq_timer_ns_0_ch5	High level	281	irq_npu_mcu_cache	High level
83	irq_timer_ns_1_ch0	High level	282	irq_sdmmc_detectn_grf	High level
84	irq_timer_ns_1_ch1	High level	283	irq_sdmmc	High level
85	irq_timer_ns_1_ch2	High level	284	irq_sdio	High level
86	irq_timer_ns_1_ch3	High level	285	irq_emmc	High level
87	irq_timer_ns_1_ch4	High level	286	irq_fspi0	High level
88	irq_timer_ns_1_ch5	High level	287	irq_fspi1	High level
89	irq_timer_s_0_ch0	High level	288	irq_usb1_lfps_beacon	High level
90	irq_timer_s_0_ch1	High level	289	irq_mmu0	High level
91	irq_timer_s_0_ch2	High level	290	irq_mmu1	High level
92	irq_timer_s_0_ch3	High level	291	irq_mmu2	High level
93	irq_timer_s_0_ch4	High level	292	irq_usb1	High level
94	irq_timer_s_0_ch5	High level	293	irq_usb0	High level
95	irq_timer_s_1_ch0	High level	294	irq_sata0	High level
96	irq_timer_s_1_ch1	High level	295	irq_sata1	High level
97	irq_timer_s_1_ch2	High level	296	irq_pcie1_err	High level

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Number	Source	Polarity	Number	Source	Polarity
98	irq_timer_s_1_ch3	High level	297	irq_pcie1_msg_rx	High level
99	irq_timer_s_1_ch4	High level	298	irq_pcie1_legacy	High level
100	irq_timer_s_1_ch5	High level	299	irq_pcie1_sys	High level
101	irq_pmu_timer_ch0	High level	300	irq_pcie1_pmc	High level
102	irq_pmu_timer_ch1	High level	301	irq_pcie1_msi_ctrl	High level
103	irq_ddr_timer_ch0	High level	302	irq_pcie1_msi_ctrl_int_vec_0	High level
104	irq_ddr_timer_ch1	High level	303	irq_pcie1_msi_ctrl_int_vec_1	High level
105	irq_npu_timer_ch0	High level	304	irq_pcie1_msi_ctrl_int_vec_2	High level
106	irq_npu_timer_ch1	High level	305	irq_pcie1_msi_ctrl_int_vec_3	High level
107	irq_hptimer	High level	306	irq_pcie1_msi_ctrl_int_vec_4	High level
108	irq_uart0	High level	307	irq_pcie1_msi_ctrl_int_vec_5	High level
109	irq_uart1	High level	308	irq_pcie1_msi_ctrl_int_vec_6	High level
110	irq_uart2	High level	309	irq_pcie1_msi_ctrl_int_vec_7	High level
111	irq_uart3	High level	310	irq_pcie0_err	High level
112	irq_uart4	High level	311	irq_pcie0_msg_rx	High level
113	irq_uart5	High level	312	irq_pcie0_legacy	High level
114	irq_uart6	High level	313	irq_pcie0_sys	High level
115	irq_uart7	High level	314	irq_pcie0_pmc	High level
116	irq_uart8	High level	315	irq_pcie0_msi_ctrl	High level
117	irq_uart9	High level	316	irq_pcie0_msi_ctrl_int_vec_0	High level
118	irq_uart10	High level	317	irq_pcie0_msi_ctrl_int_vec_1	High level
119	irq_uart11	High level	318	irq_pcie0_msi_ctrl_int_vec_2	High level
120	irq_i2c0	High level	319	irq_pcie0_msi_ctrl_int_vec_3	High level
121	irq_i2c1	High level	320	irq_pcie0_msi_ctrl_int_vec_4	High level
122	irq_i2c2	High level	321	irq_pcie0_msi_ctrl_int_vec_5	High level
123	irq_i2c3	High level	322	irq_pcie0_msi_ctrl_int_vec_6	High level
124	irq_i2c4	High level	323	irq_pcie0_msi_ctrl_int_vec_7	High level
125	irq_i2c5	High level	324	irq_gmac0_lpi	High level
126	irq_i2c6	High level	325	irq_gmac0_sbd	High level
127	irq_i2c7	High level	326	irq_gmac0_sbd_perch_tx_0	High level
128	irq_i2c8	High level	327	irq_gmac0_sbd_perch_tx_1	High level
129	irq_i2c9	High level	328	irq_gmac0_sbd_perch_rx_0	High level

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Number	Source	Polarity	Number	Source	Polarity
130	irq_i3c0	High level	329	irq_gmac0_sbd_perch_rx_1	High level
131	irq_i3c1	High level	330	irq_gmac0_pmt	High level
132	irq_pwm0_2ch_0	High level	331	irq_gmac0_mcgr_dma_req	High level
133	irq_pwm0_2ch_1	High level	332	irq_gmac1_lpi	High level
134	irq_pwm1_6ch_0	High level	333	irq_gmac1_sbd	High level
135	irq_pwm1_6ch_1	High level	334	irq_gmac1_sbd_perch_tx_0	High level
136	irq_pwm1_6ch_2	High level	335	irq_gmac1_sbd_perch_tx_1	High level
137	irq_pwm1_6ch_3	High level	336	irq_gmac1_sbd_perch_rx_0	High level
138	irq_pwm1_6ch_4	High level	337	irq_gmac1_sbd_perch_rx_1	High level
139	irq_pwm1_6ch_5	High level	338	irq_gmac1_pmt	High level
140	irq_pwm2_8ch_0	High level	339	irq_gmac1_mcgr_dma_req	High level
141	irq_pwm2_8ch_1	High level	340	irq_rkvdec_dec	High level
142	irq_pwm2_8ch_2	High level	341	irq_rkvdec_mmu	High level
143	irq_pwm2_8ch_3	High level	342	irq_vepu0	High level
144	irq_pwm2_8ch_4	High level	343	irq_vepu0_mmu	High level
145	irq_pwm2_8ch_5	High level	344	irq_csihost0_1	High level
146	irq_pwm2_8ch_6	High level	345	irq_csihost0_2	High level
147	irq_pwm2_8ch_7	High level	346	irq_csihost1_1	High level
148	irq_spi0	High level	347	irq_csihost1_2	High level
149	irq_spi1	High level	348	irq_csihost2_1	High level
150	irq_spi2	High level	349	irq_csihost2_2	High level
151	irq_spi3	High level	350	irq_vicap	High level
152	irq_spi4	High level	351	irq_vicap_mmu	High level
153	irq_can0	High level	352	irq_vicap_ddr	High level
154	irq_can1	High level	353	irq_isp_mipi	High level
155	irq_tsadc	High level	354	irq_isp_mi	High level
156	irq_saradc	High level	355	irq_isp	High level
157	irq_mailbox_ap0	High level	356	irq_isp_mmu	High level
158	irq_mailbox_ap1	High level	357	irq_vpss_mi	High level
159	irq_mailbox_ap2	High level	358	irq_vpss	High level
160	irq_mailbox_ap3	High level	359	irq_vpss_mmu	High level
161	irq_mailbox_ap4	High level	360	irq_rga0	High level

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Number	Source	Polarity	Number	Source	Polarity
162	irq_mailbox_ap5	High level	361	irq_rga1	High level
163	irq_mailbox_ap6	High level	362	irq_jpeg_enc	High level
164	irq_mailbox_ap7	High level	363	irq_jpeg_dec	High level
165	irq_mailbox_ap8	High level	364	irq_jpeg_mmu	High level
166	irq_mailbox_ap9	High level	365	irq_vdpp	High level
167	irq_mailbox_ap10	High level	366	irq_ebc	High level
168	irq_mailbox_ap11	High level	367	irq_hdcp0_hpi	High level
169	irq_mailbox_ap12	High level	368	irq_hdcp1_hpi	High level
170	irq_mailbox_ap13	High level	369	irq_dp	High level
171	irq_mailbox_bb0	High level	370	irq_hdmitx_oavp	High level
172	irq_mailbox_bb1	High level	371	irq_hdmitx_ocec	High level
173	irq_mailbox_bb2	High level	372	irq_hdmitx_oearcrx	High level
174	irq_mailbox_bb3	High level	373	irq_hdmitx_omain	High level
175	irq_mailbox_bb4	High level	374	irq_vop	High level
176	irq_mailbox_bb5	High level	375	irq_vop_ddr	High level
177	irq_mailbox_bb6	High level	376	irq_vop_lb	High level
178	irq_mailbox_bb7	High level	377	irq_dsihost	High level
179	irq_mailbox_bb8	High level	378	irq_gpu_event	High level
180	irq_mailbox_bb9	High level	379	irq_gpu_job	High level
181	irq_mailbox_bb10	High level	380	irq_gpu_mmu	High level
182	irq_mailbox_bb11	High level	381	irq_gpu	High level
183	irq_mailbox_bb12	High level	382	irq_usb0_bvalid	High level
184	irq_mailbox_bb13	High level	383	irq_usb0_id	High level
185	irq_gpio0[0]	High level	384	irq_usb0_linestate	High level
186	irq_gpio0[1]	High level	385	irq_usb0_disconnect	High level
187	irq_gpio0[2]	High level	386	irq_usb1_bvalid	High level
188	irq_gpio0[3]	High level	387	irq_usb1_id	High level
189	irq_gpio1[0]	High level	388	irq_usb1_linestate	High level
190	irq_gpio1[1]	High level	389	irq_usb1_disconnect	High level
191	irq_gpio1[2]	High level	390	irq_usb0_lfps_beacon	High level
192	irq_gpio1[3]	High level	391	irq_pre3a_done	High level
193	irq_gpio2[0]	High level	392	irq_dsmc	High level

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Number	Source	Polarity	Number	Source	Polarity
194	irq_gpio2[1]	High level	393	irq_ufshc_sinterrupt	High level
195	irq_gpio2[2]	High level	394	irq_ufshc_fe	High level
196	irq_gpio2[3]	High level	395	irq_unipro	High level
197	irq_gpio3[0]	High level	396	irq_fw_vop2ddr_main	High level
198	irq_gpio3[1]	High level	397	irq_edp	High level
199	irq_gpio3[2]	High level	398	irq_mphy_pcs	High level
200	irq_gpio3[3]	High level	399	irq_hdmitx_hpd	High level
201	irq_gpio4[0]	High level	400	irq_ddrmcu_freqdone	High level
202	irq_gpio4[1]	High level	401	irq_flexbus	High level
203	irq_gpio4[2]	High level	402	irq_spdif_tx4	High level
204	irq_gpio4[3]	High level	403	irq_spdif_tx5	High level
205	irq_pmu_mcu_cache	High level	404	irq_sai8	High level
206	irq_pmu_pvtm	High level	405	irq_sai9	High level
207	irq_pmic	High level	406	irq_osc_chk_rst_req	High level
208	irq_crc_chk_rst_req_sgrf	High level	407	irq_jtag_lock_rst_req	High level
209	irq_nscrypto	High level	408	irq_otg0_vbusvalid	High level
210	irq_scrypto	High level	409	irq_otg1_vbusvalid	High level
211	irq_keylad	High level	410	irq_mainTimeout	High level
212	irq_rkrng_s	High level	411	irq_vop_vp0	High level
213	irq_rkrng_ns	High level	412	irq_vop_vp1	High level
214	irq_hdcp0_trng	High level	413	irq_vop_vp2	High level
215	irq_hdcp1_trng	High level	414	irq_ufs_state	High level
216	irq_otpmask	High level	415	irq_csihost3_1	High level
217	irq_otpc_ns	High level	416	irq_csihost3_2	High level
218	irq_otpc_s	High level	417	irq_csihost4_1	High level
219	irq_sai0	High level	418	irq_csihost4_2	High level
220	irq_sai1	High level	419	irq_vepu1	High level
221	irq_sai2	High level	420	irq_vepu1_mmu	High level

1.4 System DMA Hardware Request Connection

RK3576 provides three DMA controller (DMAC) inside the system, the following tables are the DMA hardware request list.

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Table 1-4 DMAC Request Mapping Table

DMAC0		
Req Number	**Source**	**Polarity**
0	sai0_tx	High level
1	sai0_rx	High level
2	sai1_tx	High level
3	sai1_rx	High level
4	pdm0	High level
5	spdif_tx0	High level
6	uart0 tx	High level
7	uart0 rx	High level
8	uart1 tx	High level
9	uart1 rx	High level
10	uart2 tx	High level
11	uart2 rx	High level
12	uart3 tx	High level
13	uart3 rx	High level
14	spi0_tx	High level
15	spi0_rx	High level
16	spi1_tx	High level
17	spi1_rx	High level
18	\	High level
19	\	High level
20	can0_rx	High level
21	\	High level
22	i3c0_rx	High level
23	i3c0_tx	High level
24	i3c0_ibi	High level
25	spdif_tx5	High level
26	sai9_tx	High level
27	asrc2ch_0_rx	High level
28	asrc2ch_0_tx	High level
29	\	High level
30	dsmc_0	High level
31	dsmc_1	High level
DMAC1		
Req Number	**Source**	**case cover**
0	sai2_tx	High level
1	sai2_rx	High level
2	sai3_tx	High level
3	sai3_rx	High level
4	pdm1	High level

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5	spdif_tx1	High level
6	spdif_tx4	High level
7	sai8_tx	High level
8	spdif_rx0	High level
9	uart4 tx	High level
10	uart4 rx	High level
11	uart5 tx	High level
12	uart5 rx	High level
13	uart6 tx	High level
14	uart6 rx	High level
15	spi2_tx	High level
16	spi2_rx	High level
17	spi3_tx	High level
18	spi3_rx	High level
19	\	High level
20	\	High level
21	can1_rx	High level
22	i3c1_rx	High level
23	i3c1_tx	High level
24	i3c1_ibi	High level
25	\	High level
26	\	High level
27	asrc2ch_1_rx	High level
28	asrc2ch_1_tx	High level
29	\	High level
30	\	High level
31	\	High level
DMAC2		
Req Number	**Source**	**case cover**
0	sai4_tx	High level
1	sai4_rx	High level
2	\	High level
3	sai5_rx	High level
4	sai6_tx	High level
5	sai6_rx	High level
6	uart7 tx	High level
7	uart7 rx	High level
8	uart8 tx	High level
9	uart8 rx	High level
10	uart9 tx	High level
11	uart9 rx	High level
12	spi4_tx	High level

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13	spi4_rx	High level
14	\	High level
15	\	High level
16	spdif_rx1	High level
17	asrc4ch_0_rx	High level
18	asrc4ch_0_tx	High level
19	sai7_tx	High level
20	\	High level
21	uart10 tx	High level
22	uart10 rx	High level
23	uart11 tx	High level
24	uart11 rx	High level
25	asrc4ch_1_rx	High level
26	asrc4ch_1_tx	High level
27	spdif_rx2	High level
28	spdif_tx2	High level
29	spdif_tx3	High level
30	\	High level
31	\	High level

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Chapter 2 Clock and Reset Unit (CRU)

2.1 Overview

The CRU is an APB slave module that is designed for generating all of the internal and system clocks, resets in the chip. The CRU generates system clocks from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset, software resets or temperature sensor reset.
The CRU is located at several addresses.

	Description	Base Address
CRU	Used for always on system.	0x27200000
PPLL_CRU	Used for ppll system.	0x27208000
SECURE_CRU	Used for secure system.	0x27210000
PMU1_CRU	Used for pmu system.	0x27220000
DDR0_CRU	Used for DDR0 phy.	0x27228000
DDR1_CRU	Used for DDR1 phy.	0x27230000
BIGCORE_CRU	Used for pd bigcore system.	0x27238000
LITCORE_CRU	Used for pd litcore system.	0x27240000
CCI_CRU	Used for pd cci system.	0x27248000

The CRU supports the following features:

- Compliance with AMBA APB interface
- Embedded with 4 fractional PLLs, 3 integer PLLs and 5 DDR PLLs in different CRUs, which is shown below:

PLL TYPE / PD	FRACPLL	DDRPLL	INTPLL
CRU	VPLL,AUPLL,CPLL,GPLL		BPLL
BIGCORE_CRU			
LITCORE_CRU			
CCI_CRU			LPLL
SECURE_CRU			SPLL
DDR0_CRU		D0APLL,D0BPLL	
DDR1_CRU		D1APLL,D1BPLL	
PPLL_CRU		PPLL	

- Flexible selection of clock source
- Support dividing clock separately
- Support gating clock separately
- Support software reset for each module separately

2.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

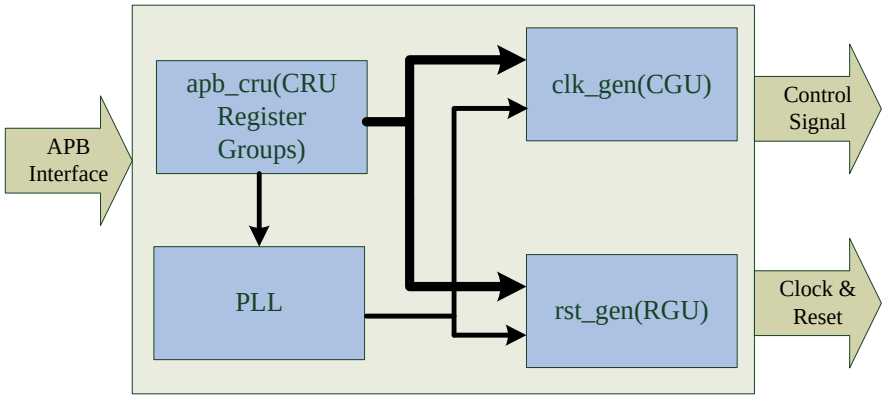

Fig 2-1 CRU Block Diagram

2.3 Function Description

2.3.1 System Clock Solution

All R3576 PLLs receive 24MHz or 26MHz oscillator as input reference clock. GPLL, VPLL, AUPLL, CPLL, SPLL, LPLL and BPLL can be set to three work modes: normal mode, slow mode and deep slow mode. Before power on, power off or changing PLL setting, you must program PLL into slow mode or deep slow mode.

To maximize the flexibility, some of clocks can select divider source from multiple PLLs. To provide some specific frequency, another solution is integrated: fractional divider. Divfree50 divider and Divfree NP5 divider are also provided for some modules. All clocks can be gated by software.

The basic units for clock generation are:

- Gating
- MUX(multiplexer)
- Divfree(Glitch free divider)
  - clk_out_freq=clk_in_freq/divisor.
  - When divisor is even, the clock duty cycle of clk_out is 50%.
  - When divisor is odd, the clock duty cycle of clk_out is not 50%.
- Fracdiv(Fractional divider)
  - clk_out_freq=clk_in_freq*numerator/denominator, both numerator and denominator are 16 bits.
- Divfree50(Glitch free divider for duty cycle 50%)
  - clk_out_freq=clk_in_freq/divisor.
  - Whether divisor is even or odd, the clock duty cycle of clk_out is 50%.
- DivFreeNP5(Glitch free divider for null point 5)
  - clk_out_freq= clk_in_freq/(div_con+1.5).
  - The clock duty cycle of clk_out is not 50%.

The settings of all basic units are controlled by CRU registers.

2.3.2 System Reset Solution

Almost all modules have these reset sources as the following figure shows. The ‘xxx’ in the figure is the module name.

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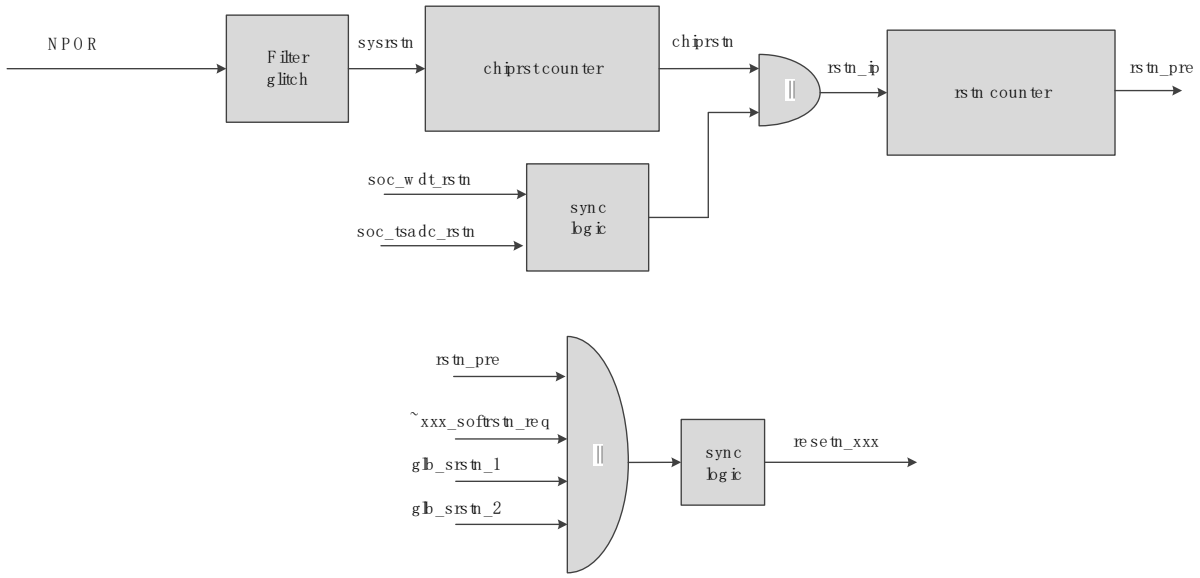

Fig 2-2 Reset Architecture Diagram

Reset source of each reset signal includes:

- NPOR: External power on reset.
- soc_wdt_rstn: Reset from WDT module.
- soc_tsadc_rstn: Reset from TSADC module.
- softrstn_req: Software reset request by programming CRU_SOFTRST_CON.
- glb_srstn_1: First global software reset by programming CRU_GLB_SRST_FST as 0xfdb9.
- glb_srstn_2: Second global software reset by programming CRU_GLB_SRST_SND as 0xeca8.

2.3.3 PLL Introduction

PLL is a 1.8V/0.75V dual supply-voltage phase locked loop (PLL) with a wide-output-frequency-range for frequency synthesis.

	FRACPLL		DDRPLL		INTPLL	
Parameter	MIN	MAX	MIN	MAX	MIN	MAX
Fin	4.5	300	6	300	4.5	300
p	1	63	1	63	1	63
m	64	1023	64	1023	64	1023
s	0	6	0	6	0	6
Fref(MHz)=Fin/p	6	30	6	30	4.5	12
Fvco(MHz)=(m*Fref)/p	2250	4500	3300	6600	2250	4500
Fout(MHz)	35.2	4500	51.6	6600	35.2	4500
Duty cycle	48~52%		45~55%		47~53%	
Input Period Jitter	±200ps		±200ps		±200ps	
PLL Period Jitter(Tjp)	Fvco<3G:±2% of Tfvco		Fvco<3G:±2% of Tfvco		Fvco<3G:±1.5% of Tfvco	
	Fvco>3G:±1% of Tfvco		Fvco>3G:±1% of Tfvco		Fvco>3G:±0.75% of Tfvco	
Lock Time(Fin/p cycles)	-	500	-	500	-	150
Modulation Method	up/down/center		up/down/center		-	

2.3.3.1 FRACPLL Introduction

FRACPLL block diagram is shown below.

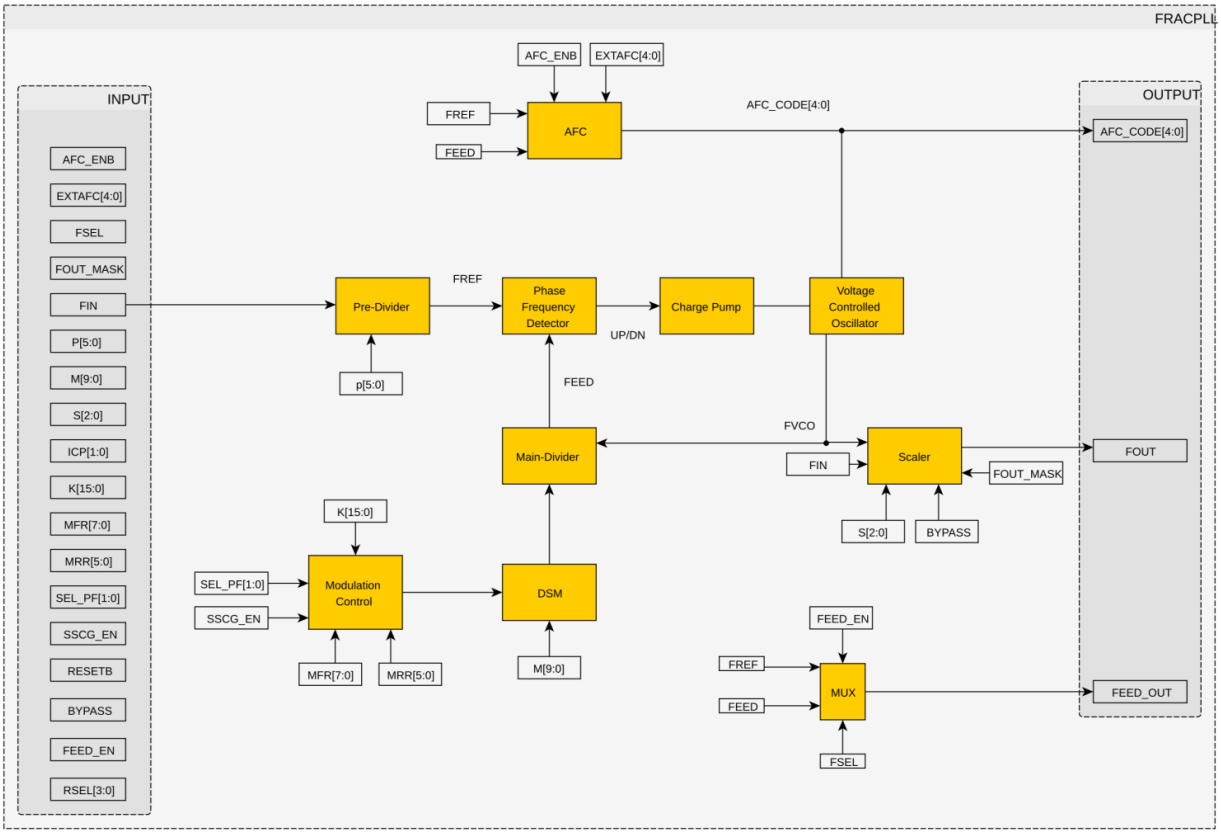

Fig 2-3 FRACPLL Block Diagram

2.3.3.2 INTPLL Introduction

INTPLL block diagram is shown below.

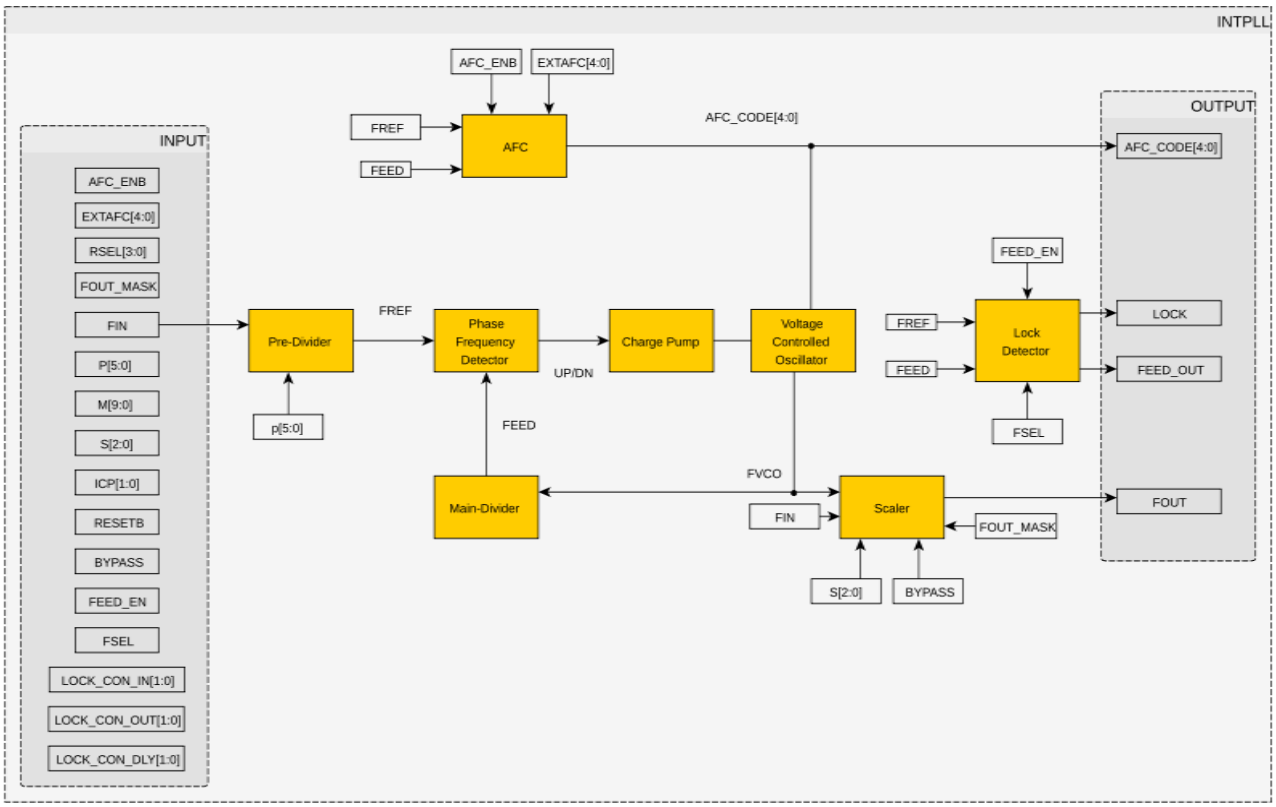

Fig 2-4 INTPLL Block Diagram

2.3.3.3 DDRPLL Introduction

DDRPLL block diagram is shown below.

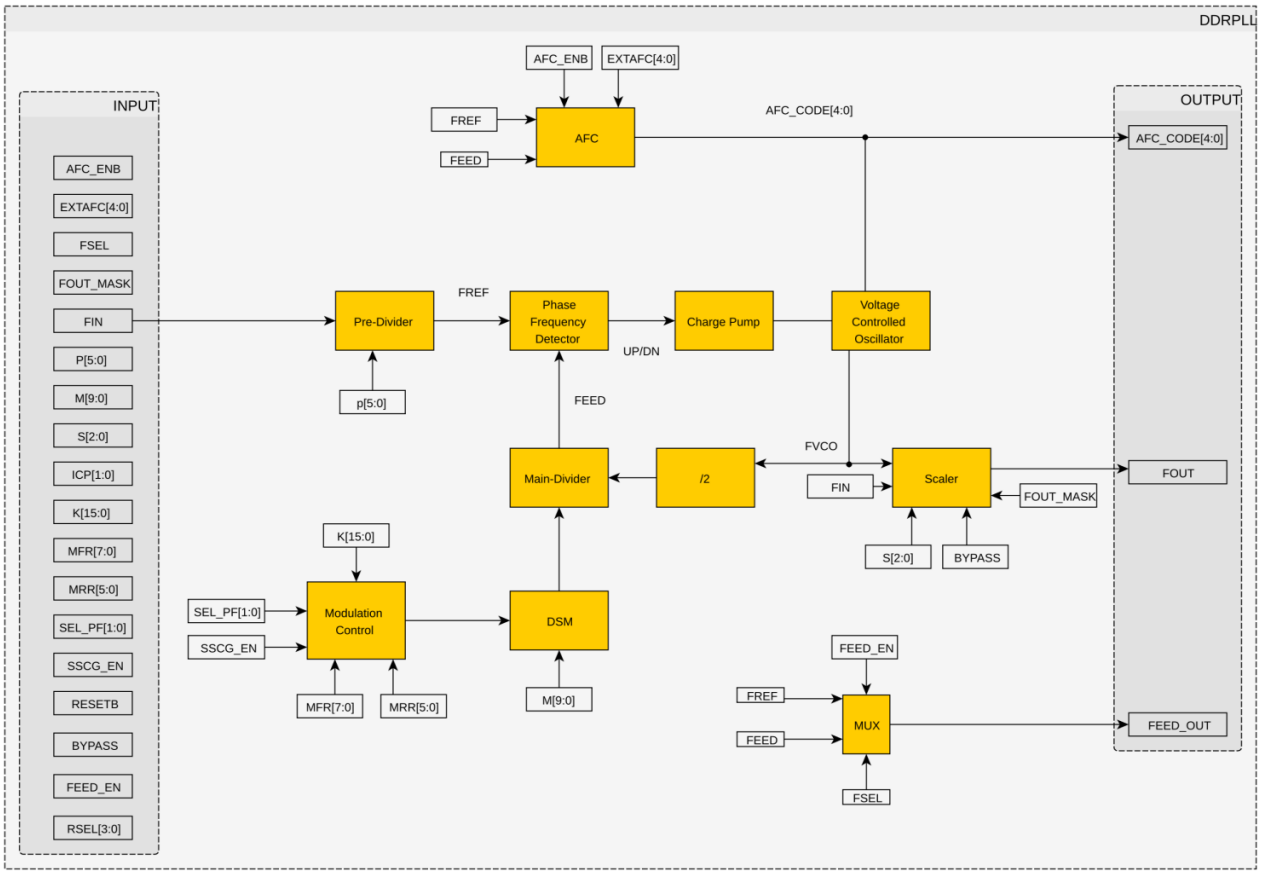

Fig 2-5 DDRPLL Block Diagram

2.4 CRU Register Description(register of autocs is internel only, secure register is internal only)

2.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_BPLL_CON0	0x0000	W	0x00000190	BPLL configuration register 0
CRU_BPLL_CON1	0x0004	W	0x00000083	BPLL configuration register 1
CRU_BPLL_CON4	0x0010	W	0x00000002	BPLL configuration register 4
CRU_BPLL_CON5	0x0014	W	0x000007E0	BPLL configuration register 5
CRU_BPLL_CON6	0x0018	W	0x00000000	BPLL configuration register 6
CRU_VPLL_CON0	0x0160	W	0x000000C6	VPLL configuration register 0
CRU_VPLL_CON1	0x0164	W	0x00000082	VPLL configuration register 1
CRU_VPLL_CON2	0x0168	W	0x00000000	VPLL configuration register 2
CRU_VPLL_CON3	0x016C	W	0x00000000	VPLL configuration register 3
CRU_VPLL_CON4	0x0170	W	0x00000000	VPLL configuration register 4
CRU_VPLL_CON5	0x0174	W	0x00000000	VPLL configuration register 5
CRU_VPLL_CON6	0x0178	W	0x00000000	VPLL configuration register 6
CRU_AUPLL_CON0	0x0180	W	0x00000083	AUPLL configuration register 0
CRU_AUPLL_CON1	0x0184	W	0x000000C1	AUPLL configuration register 1
CRU_AUPLL_CON2	0x0188	W	0x0000126F	AUPLL configuration register 2
CRU_AUPLL_CON3	0x018C	W	0x00000000	AUPLL configuration register 3

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Name	Offset	Size	Reset Value	Description
CRU_AUPLL_CON4	0x0190	W	0x00000000	AUPLL configuration register 4
CRU_AUPLL_CON5	0x0194	W	0x00000000	AUPLL configuration register 5
CRU_AUPLL_CON6	0x0198	W	0x00000000	AUPLL configuration register 6
CRU_CPLL_CON0	0x01A0	W	0x000001F4	CPLL configuration register 0
CRU_CPLL_CON1	0x01A4	W	0x000000C3	CPLL configuration register 1
CRU_CPLL_CON2	0x01A8	W	0x00000000	CPLL configuration register 2
CRU_CPLL_CON3	0x01AC	W	0x00000000	CPLL configuration register 3
CRU_CPLL_CON4	0x01B0	W	0x00000000	CPLL configuration register 4
CRU_CPLL_CON5	0x01B4	W	0x00000000	CPLL configuration register 5
CRU_CPLL_CON6	0x01B8	W	0x00000000	CPLL configuration register 6
CRU_GPLL_CON0	0x01C0	W	0x000000C6	GPLL configuration register 0
CRU_GPLL_CON1	0x01C4	W	0x00000082	GPLL configuration register 1
CRU_GPLL_CON2	0x01C8	W	0x00000000	GPLL configuration register 2
CRU_GPLL_CON3	0x01CC	W	0x00000000	GPLL configuration register 3
CRU_GPLL_CON4	0x01D0	W	0x00000000	GPLL configuration register 4
CRU_GPLL_CON5	0x01D4	W	0x00000000	GPLL configuration register 5
CRU_GPLL_CON6	0x01D8	W	0x00000000	GPLL configuration register 6
CRU_MODE_CON00	0x0280	W	0x00000000	Internal PLL mode select register 0
CRU_CLKSEL_CON00	0x0300	W	0x00000A73	Internal clock select and division register 0
CRU_CLKSEL_CON01	0x0304	W	0x00000147	Internal clock select and division register 1
CRU_CLKSEL_CON02	0x0308	W	0x000000E3	Internal clock select and division register 2
CRU_CLKSEL_CON03	0x030C	W	0x00000141	Internal clock select and division register 3
CRU_CLKSEL_CON04	0x0310	W	0x00000840	Internal clock select and division register 4
CRU_CLKSEL_CON05	0x0314	W	0x00000001	Internal clock select and division register 5
CRU_CLKSEL_CON06	0x0318	W	0x00000040	Internal clock select and division register 6
CRU_CLKSEL_CON08	0x0320	W	0x00000000	Internal clock select and division register 8
CRU_CLKSEL_CON09	0x0324	W	0x000000C0	Internal clock select and division register 9
CRU_CLKSEL_CON10	0x0328	W	0x00000802	Internal clock select and division register 10
CRU_CLKSEL_CON11	0x032C	W	0x00000003	Internal clock select and division register 11
CRU_CLKSEL_CON12	0x0330	W	0x001403DE	Internal clock select and division register 12
CRU_CLKSEL_CON13	0x0334	W	0x00000000	Internal clock select and division register 13
CRU_CLKSEL_CON14	0x0338	W	0x03355460	Internal clock select and division register 14
CRU_CLKSEL_CON15	0x033C	W	0x00000000	Internal clock select and division register 15
CRU_CLKSEL_CON16	0x0340	W	0x002103DE	Internal clock select and division register 16
CRU_CLKSEL_CON17	0x0344	W	0x00000000	Internal clock select and division register 17

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON18	0x0348	W	0x002103DE	Internal clock select and division register 18
CRU_CLKSEL_CON19	0x034C	W	0x00000200	Internal clock select and division register 19
CRU_CLKSEL_CON21	0x0354	W	0x001403DE	Internal clock select and division register 21
CRU_CLKSEL_CON22	0x0358	W	0x00000000	Internal clock select and division register 22
CRU_CLKSEL_CON23	0x035C	W	0x03355460	Internal clock select and division register 23
CRU_CLKSEL_CON24	0x0360	W	0x00000000	Internal clock select and division register 24
CRU_CLKSEL_CON25	0x0364	W	0x002103DE	Internal clock select and division register 25
CRU_CLKSEL_CON26	0x0368	W	0x000003FC	Internal clock select and division register 26
CRU_CLKSEL_CON27	0x036C	W	0x00006FE3	Internal clock select and division register 27
CRU_CLKSEL_CON28	0x0370	W	0x00001D2B	Internal clock select and division register 28
CRU_CLKSEL_CON29	0x0374	W	0x00000001	Internal clock select and division register 29
CRU_CLKSEL_CON30	0x0378	W	0x00001C00	Internal clock select and division register 30
CRU_CLKSEL_CON31	0x037C	W	0x00000027	Internal clock select and division register 31
CRU_CLKSEL_CON32	0x0380	W	0x00000001	Internal clock select and division register 32
CRU_CLKSEL_CON33	0x0384	W	0x0000001F	Internal clock select and division register 33
CRU_CLKSEL_CON34	0x0388	W	0x0000001F	Internal clock select and division register 34
CRU_CLKSEL_CON35	0x038C	W	0x0000001F	Internal clock select and division register 35
CRU_CLKSEL_CON36	0x0390	W	0x0000A7A7	Internal clock select and division register 36
CRU_CLKSEL_CON37	0x0394	W	0x00001600	Internal clock select and division register 37
CRU_CLKSEL_CON38	0x0398	W	0x00000000	Internal clock select and division register 38
CRU_CLKSEL_CON39	0x039C	W	0x00000000	Internal clock select and division register 39
CRU_CLKSEL_CON40	0x03A0	W	0x00000000	Internal clock select and division register 40
CRU_CLKSEL_CON41	0x03A4	W	0x00000004	Internal clock select and division register 41
CRU_CLKSEL_CON42	0x03A8	W	0x00000A14	Internal clock select and division register 42
CRU_CLKSEL_CON43	0x03AC	W	0x000020C1	Internal clock select and division register 43
CRU_CLKSEL_CON44	0x03B0	W	0x00000001	Internal clock select and division register 44
CRU_CLKSEL_CON45	0x03B4	W	0x000010A1	Internal clock select and division register 45

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON46	0x03B8	W	0x00000001	Internal clock select and division register 46
CRU_CLKSEL_CON47	0x03BC	W	0x00000001	Internal clock select and division register 47
CRU_CLKSEL_CON48	0x03C0	W	0x00000001	Internal clock select and division register 48
CRU_CLKSEL_CON49	0x03C4	W	0x00000001	Internal clock select and division register 49
CRU_CLKSEL_CON50	0x03C8	W	0x0000001F	Internal clock select and division register 50
CRU_CLKSEL_CON51	0x03CC	W	0x0000000B	Internal clock select and division register 51
CRU_CLKSEL_CON52	0x03D0	W	0x00000001	Internal clock select and division register 52
CRU_CLKSEL_CON53	0x03D4	W	0x00000001	Internal clock select and division register 53
CRU_CLKSEL_CON55	0x03DC	W	0x00000020	Internal clock select and division register 55
CRU_CLKSEL_CON56	0x03E0	W	0x00000183	Internal clock select and division register 56
CRU_CLKSEL_CON57	0x03E4	W	0x00000000	Internal clock select and division register 57
CRU_CLKSEL_CON58	0x03E8	W	0x000003B0	Internal clock select and division register 58
CRU_CLKSEL_CON59	0x03EC	W	0x0000000B	Internal clock select and division register 59
CRU_CLKSEL_CON60	0x03F0	W	0x0000037F	Internal clock select and division register 60
CRU_CLKSEL_CON61	0x03F4	W	0x0000037F	Internal clock select and division register 61
CRU_CLKSEL_CON62	0x03F8	W	0x0000037F	Internal clock select and division register 62
CRU_CLKSEL_CON63	0x03FC	W	0x0000037F	Internal clock select and division register 63
CRU_CLKSEL_CON64	0x0400	W	0x0000037F	Internal clock select and division register 64
CRU_CLKSEL_CON65	0x0404	W	0x0000037F	Internal clock select and division register 65
CRU_CLKSEL_CON66	0x0408	W	0x0000037F	Internal clock select and division register 66
CRU_CLKSEL_CON67	0x040C	W	0x0000037F	Internal clock select and division register 67
CRU_CLKSEL_CON68	0x0410	W	0x0000037F	Internal clock select and division register 68
CRU_CLKSEL_CON69	0x0414	W	0x0000037F	Internal clock select and division register 69
CRU_CLKSEL_CON70	0x0418	W	0x0000037F	Internal clock select and division register 70
CRU_CLKSEL_CON71	0x041C	W	0x00004200	Internal clock select and division register 71
CRU_CLKSEL_CON72	0x0420	W	0x00001061	Internal clock select and division register 72
CRU_CLKSEL_CON73	0x0424	W	0x00000020	Internal clock select and division register 73

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON74	0x0428	W	0x000000A0	Internal clock select and division register 74
CRU_CLKSEL_CON75	0x042C	W	0x00000000	Internal clock select and division register 75
CRU_CLKSEL_CON76	0x0430	W	0x00000085	Internal clock select and division register 76
CRU_CLKSEL_CON77	0x0434	W	0x00001061	Internal clock select and division register 77
CRU_CLKSEL_CON78	0x0438	W	0x00000102	Internal clock select and division register 78
CRU_CLKSEL_CON80	0x0440	W	0x00000000	Internal clock select and division register 80
CRU_CLKSEL_CON82	0x0448	W	0x00000000	Internal clock select and division register 82
CRU_CLKSEL_CON86	0x0458	W	0x00000100	Internal clock select and division register 86
CRU_CLKSEL_CON87	0x045C	W	0x00000404	Internal clock select and division register 87
CRU_CLKSEL_CON88	0x0460	W	0x0000000C	Internal clock select and division register 88
CRU_CLKSEL_CON89	0x0464	W	0x00000502	Internal clock select and division register 89
CRU_CLKSEL_CON90	0x0468	W	0x00000000	Internal clock select and division register 90
CRU_CLKSEL_CON92	0x0470	W	0x00000030	Internal clock select and division register 92
CRU_CLKSEL_CON93	0x0474	W	0x00009393	Internal clock select and division register 93
CRU_CLKSEL_CON103	0x049C	W	0x0000000C	Internal clock select and division register 103
CRU_CLKSEL_CON104	0x04A0	W	0x00002F02	Internal clock select and division register 104
CRU_CLKSEL_CON105	0x04A4	W	0x0000012F	Internal clock select and division register 105
CRU_CLKSEL_CON106	0x04A8	W	0x00000502	Internal clock select and division register 106
CRU_CLKSEL_CON107	0x04AC	W	0x00000142	Internal clock select and division register 107
CRU_CLKSEL_CON108	0x04B0	W	0x00000005	Internal clock select and division register 108
CRU_CLKSEL_CON110	0x04B8	W	0x00000284	Internal clock select and division register 110
CRU_CLKSEL_CON111	0x04BC	W	0x00000020	Internal clock select and division register 111
CRU_CLKSEL_CON115	0x04CC	W	0x000000E5	Internal clock select and division register 115
CRU_CLKSEL_CON118	0x04D8	W	0x00000020	Internal clock select and division register 118
CRU_CLKSEL_CON119	0x04DC	W	0x00000060	Internal clock select and division register 119
CRU_CLKSEL_CON120	0x04E0	W	0x00000120	Internal clock select and division register 120
CRU_CLKSEL_CON121	0x04E4	W	0x00000020	Internal clock select and division register 121

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON122	0x04E8	W	0x03355460	Internal clock select and division register 122
CRU_CLKSEL_CON123	0x04EC	W	0x00000013	Internal clock select and division register 123
CRU_CLKSEL_CON124	0x04F0	W	0x00004008	Internal clock select and division register 124
CRU_CLKSEL_CON128	0x0500	W	0x00000201	Internal clock select and division register 128
CRU_CLKSEL_CON129	0x0504	W	0x00000041	Internal clock select and division register 129
CRU_CLKSEL_CON130	0x0508	W	0x00000800	Internal clock select and division register 130
CRU_CLKSEL_CON144	0x0540	W	0x00000060	Internal clock select and division register 144
CRU_CLKSEL_CON145	0x0544	W	0x00000001	Internal clock select and division register 145
CRU_CLKSEL_CON146	0x0548	W	0x00000003	Internal clock select and division register 146
CRU_CLKSEL_CON147	0x054C	W	0x00000007	Internal clock select and division register 147
CRU_CLKSEL_CON149	0x0554	W	0x00000002	Internal clock select and division register 149
CRU_CLKSEL_CON151	0x055C	W	0x0000A502	Internal clock select and division register 151
CRU_CLKSEL_CON152	0x0560	W	0x00000000	Internal clock select and division register 152
CRU_CLKSEL_CON154	0x0568	W	0x00000004	Internal clock select and division register 154
CRU_CLKSEL_CON155	0x056C	W	0x00000001	Internal clock select and division register 155
CRU_CLKSEL_CON156	0x0570	W	0x00002101	Internal clock select and division register 156
CRU_CLKSEL_CON157	0x0574	W	0x00000001	Internal clock select and division register 157
CRU_CLKSEL_CON158	0x0578	W	0x00000002	Internal clock select and division register 158
CRU_CLKSEL_CON159	0x057C	W	0x00000001	Internal clock select and division register 159
CRU_CLKSEL_CON160	0x0580	W	0x00000001	Internal clock select and division register 160
CRU_CLKSEL_CON161	0x0584	W	0x00000049	Internal clock select and division register 161
CRU_CLKSEL_CON162	0x0588	W	0x00000001	Internal clock select and division register 162
CRU_CLKSEL_CON163	0x058C	W	0x00000001	Internal clock select and division register 163
CRU_CLKSEL_CON164	0x0590	W	0x00000001	Internal clock select and division register 164
CRU_CLKSEL_CON165	0x0594	W	0x00000040	Internal clock select and division register 165
CRU_CLKSEL_CON166	0x0598	W	0x00000000	Internal clock select and division register 166
CRU_CLKSEL_CON167	0x059C	W	0x00000000	Internal clock select and division register 167

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON168	0x05A0	W	0x00000060	Internal clock select and division register 168
CRU_CLKSEL_CON178	0x05C8	W	0x00000000	Internal clock select and division register 178
CRU_CLKSEL_CON180	0x05D0	W	0x00001002	Internal clock select and division register 180
CRU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
CRU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
CRU_GATE_CON02	0x0808	W	0x00000B00	Internal clock gate and division register 2
CRU_GATE_CON03	0x080C	W	0x00000000	Internal clock gate and division register 3
CRU_GATE_CON04	0x0810	W	0x00000000	Internal clock gate and division register 4
CRU_GATE_CON05	0x0814	W	0x00000000	Internal clock gate and division register 5
CRU_GATE_CON06	0x0818	W	0x00000000	Internal clock gate and division register 6
CRU_GATE_CON07	0x081C	W	0x00000000	Internal clock gate and division register 7
CRU_GATE_CON08	0x0820	W	0x00000000	Internal clock gate and division register 8
CRU_GATE_CON09	0x0824	W	0x00000000	Internal clock gate and division register 9
CRU_GATE_CON10	0x0828	W	0x00000000	Internal clock gate and division register 10
CRU_GATE_CON11	0x082C	W	0x00000000	Internal clock gate and division register 11
CRU_GATE_CON12	0x0830	W	0x00000000	Internal clock gate and division register 12
CRU_GATE_CON13	0x0834	W	0x00000000	Internal clock gate and division register 13
CRU_GATE_CON14	0x0838	W	0x00000000	Internal clock gate and division register 14
CRU_GATE_CON15	0x083C	W	0x00000000	Internal clock gate and division register 15
CRU_GATE_CON16	0x0840	W	0x00000000	Internal clock gate and division register 16
CRU_GATE_CON17	0x0844	W	0x00000000	Internal clock gate and division register 17
CRU_GATE_CON18	0x0848	W	0x00000000	Internal clock gate and division register 18
CRU_GATE_CON19	0x084C	W	0x00000000	Internal clock gate and division register 19
CRU_GATE_CON20	0x0850	W	0x00000000	Internal clock gate and division register 20
CRU_GATE_CON21	0x0854	W	0x00000000	Internal clock gate and division register 21
CRU_GATE_CON22	0x0858	W	0x00000000	Internal clock gate and division register 22
CRU_GATE_CON23	0x085C	W	0x00000000	Internal clock gate and division register 23

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Name	Offset	Size	Reset Value	Description
CRU_GATE_CON25	0x0864	W	0x00000000	Internal clock gate and division register 25
CRU_GATE_CON26	0x0868	W	0x00000000	Internal clock gate and division register 26
CRU_GATE_CON27	0x086C	W	0x00000000	Internal clock gate and division register 27
CRU_GATE_CON28	0x0870	W	0x00000000	Internal clock gate and division register 28
CRU_GATE_CON29	0x0874	W	0x00000000	Internal clock gate and division register 29
CRU_GATE_CON31	0x087C	W	0x00000000	Internal clock gate and division register 31
CRU_GATE_CON32	0x0880	W	0x00000000	Internal clock gate and division register 32
CRU_GATE_CON33	0x0884	W	0x00000000	Internal clock gate and division register 33
CRU_GATE_CON34	0x0888	W	0x00000000	Internal clock gate and division register 34
CRU_GATE_CON35	0x088C	W	0x00000000	Internal clock gate and division register 35
CRU_GATE_CON36	0x0890	W	0x00000000	Internal clock gate and division register 36
CRU_GATE_CON37	0x0894	W	0x00000000	Internal clock gate and division register 37
CRU_GATE_CON38	0x0898	W	0x00000000	Internal clock gate and division register 38
CRU_GATE_CON39	0x089C	W	0x00000000	Internal clock gate and division register 39
CRU_GATE_CON40	0x08A0	W	0x00000000	Internal clock gate and division register 40
CRU_GATE_CON42	0x08A8	W	0x00000000	Internal clock gate and division register 42
CRU_GATE_CON43	0x08AC	W	0x00000000	Internal clock gate and division register 43
CRU_GATE_CON45	0x08B4	W	0x00000000	Internal clock gate and division register 45
CRU_GATE_CON47	0x08BC	W	0x00000000	Internal clock gate and division register 47
CRU_GATE_CON48	0x08C0	W	0x00000000	Internal clock gate and division register 48
CRU_GATE_CON49	0x08C4	W	0x00000000	Internal clock gate and division register 49
CRU_GATE_CON50	0x08C8	W	0x00000000	Internal clock gate and division register 50
CRU_GATE_CON51	0x08CC	W	0x00000000	Internal clock gate and division register 51
CRU_GATE_CON53	0x08D4	W	0x00000000	Internal clock gate and division register 53
CRU_GATE_CON54	0x08D8	W	0x00000000	Internal clock gate and division register 54
CRU_GATE_CON59	0x08EC	W	0x00000000	Internal clock gate and division register 59
CRU_GATE_CON61	0x08F4	W	0x00000000	Internal clock gate and division register 61

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Name	Offset	Size	Reset Value	Description
CRU_GATE_CON62	0x08F8	W	0x00000000	Internal clock gate and division register 62
CRU_GATE_CON63	0x08FC	W	0x00000000	Internal clock gate and division register 63
CRU_GATE_CON64	0x0900	W	0x00000000	Internal clock gate and division register 64
CRU_GATE_CON65	0x0904	W	0x00000000	Internal clock gate and division register 65
CRU_GATE_CON66	0x0908	W	0x00000000	Internal clock gate and division register 66
CRU_GATE_CON67	0x090C	W	0x00000000	Internal clock gate and division register 67
CRU_GATE_CON68	0x0910	W	0x00000000	Internal clock gate and division register 68
CRU_GATE_CON69	0x0914	W	0x00000000	Internal clock gate and division register 69
CRU_GATE_CON72	0x0920	W	0x00000000	Internal clock gate and division register 72
CRU_GATE_CON78	0x0938	W	0x00000000	Internal clock gate and division register 78
CRU_GATE_CON79	0x093C	W	0x00000000	Internal clock gate and division register 79
CRU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1
CRU_SOFTRST_CON02	0x0A08	W	0x00000000	Internal clock reset register 2
CRU_SOFTRST_CON06	0x0A18	W	0x00000000	Internal clock reset register 6
CRU_SOFTRST_CON07	0x0A1C	W	0x00000000	Internal clock reset register 7
CRU_SOFTRST_CON08	0x0A20	W	0x00000000	Internal clock reset register 8
CRU_SOFTRST_CON09	0x0A24	W	0x00000000	Internal clock reset register 9
CRU_SOFTRST_CON11	0x0A2C	W	0x00000000	Internal clock reset register 11
CRU_SOFTRST_CON12	0x0A30	W	0x00000000	Internal clock reset register 12
CRU_SOFTRST_CON13	0x0A34	W	0x00000000	Internal clock reset register 13
CRU_SOFTRST_CON14	0x0A38	W	0x00000000	Internal clock reset register 14
CRU_SOFTRST_CON15	0x0A3C	W	0x00000000	Internal clock reset register 15
CRU_SOFTRST_CON16	0x0A40	W	0x00000000	Internal clock reset register 16
CRU_SOFTRST_CON17	0x0A44	W	0x00000000	Internal clock reset register 17
CRU_SOFTRST_CON18	0x0A48	W	0x00000000	Internal clock reset register 18
CRU_SOFTRST_CON19	0x0A4C	W	0x00001000	Internal clock reset register 19
CRU_SOFTRST_CON20	0x0A50	W	0x00000000	Internal clock reset register 20
CRU_SOFTRST_CON21	0x0A54	W	0x00000040	Internal clock reset register 21
CRU_SOFTRST_CON22	0x0A58	W	0x00008004	Internal clock reset register 22
CRU_SOFTRST_CON23	0x0A5C	W	0x00000000	Internal clock reset register 23
CRU_SOFTRST_CON25	0x0A64	W	0x00000000	Internal clock reset register 25
CRU_SOFTRST_CON26	0x0A68	W	0x00000000	Internal clock reset register 26
CRU_SOFTRST_CON27	0x0A6C	W	0x00000000	Internal clock reset register 27
CRU_SOFTRST_CON28	0x0A70	W	0x00000000	Internal clock reset register 28
CRU_SOFTRST_CON29	0x0A74	W	0x00000000	Internal clock reset register 29
CRU_SOFTRST_CON31	0x0A7C	W	0x00000000	Internal clock reset register 31
CRU_SOFTRST_CON32	0x0A80	W	0x00000082	Internal clock reset register 32
CRU_SOFTRST_CON33	0x0A84	W	0x00000000	Internal clock reset register 33
CRU_SOFTRST_CON34	0x0A88	W	0x00008000	Internal clock reset register 34
CRU_SOFTRST_CON35	0x0A8C	W	0x00000000	Internal clock reset register 35
CRU_SOFTRST_CON36	0x0A90	W	0x00000200	Internal clock reset register 36
CRU_SOFTRST_CON37	0x0A94	W	0x00000000	Internal clock reset register 37

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Name	Offset	Size	Reset Value	Description
CRU_SOFTRST_CON40	0x0AA0	W	0x00000000	Internal clock reset register 40
CRU_SOFTRST_CON42	0x0AA8	W	0x00000000	Internal clock reset register 42
CRU_SOFTRST_CON43	0x0AAC	W	0x00000000	Internal clock reset register 43
CRU_SOFTRST_CON45	0x0AB4	W	0x00000000	Internal clock reset register 45
CRU_SOFTRST_CON47	0x0ABC	W	0x00000000	Internal clock reset register 47
CRU_SOFTRST_CON48	0x0AC0	W	0x00000000	Internal clock reset register 48
CRU_SOFTRST_CON49	0x0AC4	W	0x00000000	Internal clock reset register 49
CRU_SOFTRST_CON50	0x0AC8	W	0x00000000	Internal clock reset register 50
CRU_SOFTRST_CON51	0x0ACC	W	0x00000000	Internal clock reset register 51
CRU_SOFTRST_CON53	0x0AD4	W	0x00000000	Internal clock reset register 53
CRU_SOFTRST_CON54	0x0AD8	W	0x00000000	Internal clock reset register 54
CRU_SOFTRST_CON59	0x0AEC	W	0x00000000	Internal clock reset register 59
CRU_SOFTRST_CON61	0x0AF4	W	0x00000000	Internal clock reset register 61
CRU_SOFTRST_CON62	0x0AF8	W	0x00000000	Internal clock reset register 62
CRU_SOFTRST_CON63	0x0AFC	W	0x00000000	Internal clock reset register 63
CRU_SOFTRST_CON64	0x0B00	W	0x00000000	Internal clock reset register 64
CRU_SOFTRST_CON65	0x0B04	W	0x00000000	Internal clock reset register 65
CRU_SOFTRST_CON66	0x0B08	W	0x00000000	Internal clock reset register 66
CRU_SOFTRST_CON67	0x0B0C	W	0x00000000	Internal clock reset register 67
CRU_SOFTRST_CON68	0x0B10	W	0x00000000	Internal clock reset register 68
CRU_SOFTRST_CON69	0x0B14	W	0x00000000	Internal clock reset register 69
CRU_SOFTRST_CON72	0x0B20	W	0x00000000	Internal clock reset register 72
CRU_SOFTRST_CON75	0x0B2C	W	0x00000000	Internal clock reset register 75
CRU_SOFTRST_CON78	0x0B38	W	0x00000000	Internal clock reset register 78
CRU_SOFTRST_CON79	0x0B3C	W	0x00000000	Internal clock reset register 79
CRU_GLB_CNT_TH	0x0C00	W	0x00000064	System control register
CRU_GLBRST_ST	0x0C04	W	0x00000000	System control register
CRU_GLB_SRST_FST_VALUE	0x0C08	W	0x00000000	System control register
CRU_GLB_SRST_SND_VALUE	0x0C0C	W	0x00000000	System control register
CRU_GLB_RST_CON	0x0C10	W	0x00000000	System control register
CRU_GLBRST_ST_NCLR	0x0C14	W	0x00000000	System control register
CRU_CRU_NON_SECURE_GATING_CON00	0x0C48	W	0x00000000	System control register
CRU_QCHANNEL_CON01	0x0CA4	W	0x00000000	Qchannel control register 1
CRU_SMOTH_DIVFREE_CON00	0x0CC0	W	0x0200C003	Smoothdiv control register
CRU_SMOTH_DIVFREE_CON01	0x0CC4	W	0x0200C003	Smoothdiv control register
CRU_SMOTH_DIVFREE_CON02	0x0CC8	W	0x0200C003	Smoothdiv control register
CRU_HIGH16BIT_AUDIO_FRAC_0	0x0CD4	W	0x00000000	Fracdiv 24bit control register
CRU_HIGH16BIT_AUDIO_FRAC_1	0x0CD8	W	0x00000000	Fracdiv 24bit control register
CRU_HIGH16BIT_AUDIO_FRAC_2	0x0CDC	W	0x00000000	Fracdiv 24bit control register
CRU_HIGH16BIT_AUDIO_FRAC_3	0x0CE0	W	0x00000000	Fracdiv 24bit control register
CRU_AUTOCS_HCLK_TOP_BIU_CON0	0x0D10	W	0x00A00047	auto clock switch control 0

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Name	Offset	Size	Reset Value	Description
CRU_AUTOCS_HCLK_TOP_BIU_CON1	0x0D14	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_BUS_ROOT_CON0	0x0D20	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_BUS_ROOT_CON1	0x0D24	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_BUS_ROOT_CON0	0x0D28	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_BUS_ROOT_CON1	0x0D2C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_RKNN_ROOT_CON0	0x0D38	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_RKNN_ROOT_CON1	0x0D3C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_NVM_ROOT_CON0	0x0D40	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_NVM_ROOT_CON1	0x0D44	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_PHP_ROOT_CON0	0x0D48	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_PHP_ROOT_CON1	0x0D4C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_RKVDEC_ROOT_CON0	0x0D50	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_RKVDEC_ROOT_CON1	0x0D54	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_USB_ROOT_CON0	0x0D68	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_USB_ROOT_CON1	0x0D6C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_VPU_ROOT_CON0	0x0D70	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_VPU_ROOT_CON1	0x0D74	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_VPU_LOW_ROOT_CON0	0x0D78	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_VPU_LOW_ROOT_CON1	0x0D7C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_JPEG_ROOT_CON0	0x0D80	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_JPEG_ROOT_CON1	0x0D84	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_VEPU0_ROOT_CON0	0x0D88	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_VEPU0_ROOT_CON1	0x0D8C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_VI_ROOT_CON0	0x0D98	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_VI_ROOT_CON1	0x0D9C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_VOP_ROOT_CON0	0x0DA0	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_VOP_ROOT_CON1	0x0DA4	W	0x00000000	auto clock switch control 1

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Name	Offset	Size	Reset Value	Description
CRU_AUTOCS_ACLK_VPU_MID_ROOT_CON0	0x0DB0	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_VPU_MID_ROOT_CON1	0x0DB4	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_TOP_BIU_CON0	0x0DB8	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_TOP_BIU_CON1	0x0DBC	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_CENTER_ROOT_CON0	0x0DE8	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_CENTER_ROOT_CON1	0x0DEC	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_CENTER_LOW_ROOT_CON0	0x0DF0	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_CENTER_LOW_ROOT_CON1	0x0DF4	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_BUS_CM0_ROOT_CON0	0x0E18	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_BUS_CM0_ROOT_CON1	0x0E1C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_NPUTOP_ROOT_CON0	0x0E20	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_NPUTOP_ROOT_CON1	0x0E24	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_NPU_CM0_ROOT_CON0	0x0E28	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_NPU_CM0_ROOT_CON1	0x0E2C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_NVM_ROOT_CON0	0x0E30	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_NVM_ROOT_CON1	0x0E34	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_PHP_ROOT_CON0	0x0E38	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_PHP_ROOT_CON1	0x0E3C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_RKVDEC_ROOT_CON0	0x0E48	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_RKVDEC_ROOT_CON1	0x0E4C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_TOP_ROOT_CON0	0x0E58	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_TOP_ROOT_CON1	0x0E5C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_USB_ROOT_CON0	0x0E70	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_USB_ROOT_CON1	0x0E74	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_VPU_ROOT_CON0	0x0E78	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_VPU_ROOT_CON1	0x0E7C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_VEPU0_ROOT_CON0	0x0E80	W	0x00A00047	auto clock switch control 0

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Name	Offset	Size	Reset Value	Description
CRU_AUTOCS_HCLK_VEPU0_ROOT_CON1	0x0E84	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_VI_ROOT_CON0	0x0E90	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_VI_ROOT_CON1	0x0E94	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_VI_ROOT_CON0	0x0E98	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_VI_ROOT_CON1	0x0E9C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_VOP_ROOT_CON0	0x0EA8	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_VOP_ROOT_CON1	0x0EAC	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_VOP_ROOT_CON0	0x0EB0	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_VOP_ROOT_CON1	0x0EB4	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_VO0_ROOT_CON0	0x0EB8	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_VO0_ROOT_CON1	0x0EBC	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_TOP_MID_BIU_CON0	0x0EE0	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_TOP_MID_BIU_CON1	0x0EE4	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_VO1_ROOT_CON0	0x0EE8	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_VO1_ROOT_CON1	0x0EEC	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_VO1_ROOT_CON0	0x0EF0	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_VO1_ROOT_CON1	0x0EF4	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_DDR_ROOT_CON0	0x0F00	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_DDR_ROOT_CON1	0x0F04	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_CENTER_ROOT_CON0	0x0F08	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_CENTER_ROOT_CON1	0x0F0C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_DDR_ROOT_CON0	0x0F10	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_DDR_ROOT_CON1	0x0F14	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_VO1_ROOT_CON0	0x0F18	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_VO1_ROOT_CON1	0x0F1C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_CENTER_ROOT_CON0	0x0F20	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_CENTER_ROOT_CON1	0x0F24	W	0x00000000	auto clock switch control 1

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Name	Offset	Size	Reset Value	Description
CRU_AUTOCS_CLK_GPU_INNER_CON0	0x0F30	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_CLK_GPU_INNER_CON1	0x0F34	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_AUDIO_ROOT_CON0	0x0F40	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_AUDIO_ROOT_CON1	0x0F44	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_PCLK_DDR_ROOT_CON0	0x0F50	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_PCLK_DDR_ROOT_CON1	0x0F54	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_CLK_ISP0_CORE_ROOT_CON0	0x0F58	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_CLK_ISP0_CORE_ROOT_CON1	0x0F5C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_CLK_VEPU0_CORE_ROOT_CON0	0x0F60	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_CLK_VEPU0_CORE_ROOT_CON1	0x0F64	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_ACLK_VEPU1_ROOT_CON0	0x0F68	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_ACLK_VEPU1_ROOT_CON1	0x0F6C	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_HCLK_VEPU1_ROOT_CON0	0x0F70	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_HCLK_VEPU1_ROOT_CON1	0x0F74	W	0x00000000	auto clock switch control 1
CRU_AUTOCS_CLK_VEPU1_CORE_ROOT_CON0	0x0F78	W	0x00A00047	auto clock switch control 0
CRU_AUTOCS_CLK_VEPU1_CORE_ROOT_CON1	0x0F7C	W	0x00000000	auto clock switch control 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.3 Detail Registers Description

CRU_BPLL_CON0

Address: Operational Base(0x27200000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bpll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x190	bpll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

CRU_BPLL_CON1

Address: Operational Base(0x27200000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	bpll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x2	bpll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x03	bpll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

CRU_BPLL_CON4

Address: Operational Base(0x27200000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bpll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	bpll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	bpll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	bpll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RW	0x1	bpll_icp Charge-pump current control signal.
0	RO	0x0	reserved

CRU_BPLL_CON5

Address: Operational Base(0x27200000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:9	RW	0x3	bpll_lock_con_dly LOCK_CON_DLY: Lock detector setting of the detection resolution.
8:7	RW	0x3	bpll_lock_con_out LOCK_CON_OUT: Lock detector setting of the output margin.
6:5	RW	0x3	bpll_lock_con_in LOCK_CON_IN: Lock detector setting of the input margin.
4:1	RO	0x0	reserved
0	RW	0x0	bpll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

CRU_BPLL_CON6

Address: Operational Base(0x27200000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	bpll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	bpll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

CRU_VPLL_CON0

Address: Operational Base(0x27200000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	vpll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x0c6	vpll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

CRU_VPLL_CON1

Address: Operational Base(0x27200000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13	RW	0x0	vpll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x2	vpll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x02	vpll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

CRU_VPLL_CON2

Address: Operational Base(0x27200000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	vpll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

CRU_VPLL_CON3

Address: Operational Base(0x27200000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	vpll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.
13:8	RW	0x00	vpll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	vpll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

CRU_VPLL_CON4

Address: Operational Base(0x27200000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	vpll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.

Bit	Attr	Reset Value	Description
14	RW	0x0	vpll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	vpll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	vpll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	vpll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

CRU_VPLL_CON5

Address: Operational Base(0x27200000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	vpll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

CRU_VPLL_CON6

Address: Operational Base(0x27200000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	vpll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	vpll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

CRU_AUPLL_CON0

Address: Operational Base(0x27200000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	aupll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x083	aupll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

CRU_AUPLL_CON1

Address: Operational Base(0x27200000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	aupll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x3	aupll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x01	aupll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

CRU_AUPLL_CON2

Address: Operational Base(0x27200000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x126f	aupll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

CRU_AUPLL_CON3

Address: Operational Base(0x27200000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	aupll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	aupll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	aupll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

CRU_AUPLL_CON4

Address: Operational Base(0x27200000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	aupll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	aupll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	aupll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	aupll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	aupll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

CRU_AUPLL_CON5

Address: Operational Base(0x27200000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	aupll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

CRU_AUPLL_CON6

Address: Operational Base(0x27200000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	aupll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	aupll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

CRU_CPLL_CON0

Address: Operational Base(0x27200000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	cpll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x1f4	cpll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

CRU_CPLL_CON1

Address: Operational Base(0x27200000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	cpll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x3	cpll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x03	cpll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

CRU_CPLL_CON2

Address: Operational Base(0x27200000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	cpll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

CRU_CPLL_CON3

Address: Operational Base(0x27200000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	cpll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.
13:8	RW	0x00	cpll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	cpll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

CRU_CPLL_CON4

Address: Operational Base(0x27200000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	cpll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	cpll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	cpll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	cpll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	cpll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

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CRU_CPLL_CON5

Address: Operational Base(0x27200000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

CRU_CPLL_CON6

Address: Operational Base(0x27200000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	cpll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	cpll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

CRU_GPLL_CON0

Address: Operational Base(0x27200000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gpll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x0c6	gpll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

CRU_GPLL_CON1

Address: Operational Base(0x27200000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	gpll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x2	gpll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x02	gpll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

CRU_GPLL_CON2

Address: Operational Base(0x27200000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	gpll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

CRU_GPLL_CON3

Address: Operational Base(0x27200000) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.
13:8	RW	0x00	gpll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	gpll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

CRU_GPLL_CON4

Address: Operational Base(0x27200000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gpll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.

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Bit	Attr	Reset Value	Description
14	RW	0x0	gpll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	gpll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	gpll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	gpll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

CRU_GPLL_CON5

Address: Operational Base(0x27200000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	gpll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

CRU_GPLL_CON6

Address: Operational Base(0x27200000) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	gpll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	gpll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

CRU_MODE_CON00

Address: Operational Base(0x27200000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	clk_cpll_mode clk_cpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_cpll 2'b10: clk_deepslow
7:6	RW	0x0	clk_aupll_mode clk_aupll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_aupll 2'b10: clk_deepslow
5:4	RW	0x0	clk_vpll_mode clk_vpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_vpll 2'b10: clk_deepslow
3:2	RW	0x0	clk_gpll_mode clk_gpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll 2'b10: clk_deepslow
1:0	RO	0x0	reserved

CRU_CLKSEL_CON00

Address: Operational Base(0x27200000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x1	clk_cpll_div10_src_sel clk_cpll_div10_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
10:6	RW	0x09	clk_cpll_div10_src_div Divide clk_cpll_div10_src by (div_con + 1).
5	RW	0x1	clk_cpll_div20_src_sel clk_cpll_div20_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x13	clk_cpll_div20_src_div Divide clk_cpll_div20_src by (div_con + 1).

CRU_CLKSEL_CON01

Address: Operational Base(0x27200000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	clk_gpll_div6_src_sel clk_gpll_div6_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux

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Bit	Attr	Reset Value	Description
10:6	RW	0x05	clk_gpll_div6_src_div Divide clk_gpll_div6_src by (div_con + 1).
5	RW	0x0	clk_gpll_div8_src_sel clk_gpll_div8_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x07	clk_gpll_div8_src_div Divide clk_gpll_div8_src by (div_con + 1).

CRU_CLKSEL_CON02

Address: Operational Base(0x27200000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	clk_gpll_div4_src_sel clk_gpll_div4_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
10:6	RW	0x03	clk_gpll_div4_src_div Divide clk_gpll_div4_src by (div_con + 1).
5	RW	0x1	clk_cpll_div4_src_sel clk_cpll_div4_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x03	clk_cpll_div4_src_div Divide clk_cpll_div4_src by (div_con + 1).

CRU_CLKSEL_CON03

Address: Operational Base(0x27200000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_gpll_div3_src_sel clk_gpll_div3_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
11:7	RW	0x02	clk_gpll_div3_src_div Divide clk_gpll_div3_src by (div_con + 1).
6:5	RW	0x2	clk_spll_div2_src_sel clk_spll_div2_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_spll_mux 2'b11: clk_bpll_src
4:0	RW	0x01	clk_spll_div2_src_div Divide clk_spll_div2_src by (div_con + 1).

CRU_CLKSEL_CON04

Address: Operational Base(0x27200000) + offset (0x0310)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x1	clk_cpll_div2_src_sel clk_cpll_div2_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
10:6	RW	0x01	clk_cpll_div2_src_div Divide clk_cpll_div2_src by (div_con + 1).
5:0	RO	0x00	reserved

CRU_CLKSEL_CON05

Address: Operational Base(0x27200000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_gpll_div2_src_sel clk_gpll_div2_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x01	clk_gpll_div2_src_div Divide clk_gpll_div2_src by (div_con + 1).

CRU_CLKSEL_CON06

Address: Operational Base(0x27200000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:5	RW	0x2	clk_spll_div1_src_sel clk_spll_div1_src clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_spll_mux 3'b011: clk_bpll_src 3'b100: clk_lpll_src
4:0	RW	0x00	clk_spll_div1_src_div Divide clk_spll_div1_src by (div_con + 1).

CRU_CLKSEL_CON08

Address: Operational Base(0x27200000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:7	RW	0x0	pclk_top_root_sel pclk_top_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
6:0	RO	0x00	reserved

CRU_CLKSEL_CON09

Address: Operational Base(0x27200000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_lpll_src_sel clk_lpll_src clock mux. 1'b0: clk_lpll 1'b1: xin_osc0_func
11:7	RW	0x01	clk_lpll_src_div Divide clk_lpll_src by (div_con + 1).
6:5	RW	0x2	aclk_top_biu_sel aclk_top_biu clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux
4:0	RW	0x00	aclk_top_biu_div Divide aclk_top_biu by (div_con + 1).

CRU_CLKSEL_CON10

Address: Operational Base(0x27200000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:11	RW	0x1	aclk_secure_high_biu_sel aclk_secure_high_biu clock mux. 3'b000: clk_gpll_mux 3'b001: clk_spll_mux 3'b010: clk_aupll_mux 3'b011: clk_bpll_src 3'b100: clk_lpll_src
10:6	RW	0x00	aclk_secure_high_biu_div Divide aclk_secure_high_biu by (div_con + 1).
5	RW	0x0	aclk_top_mid_biu_sel aclk_top_mid_biu clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x02	aclk_top_mid_biu_div Divide aclk_top_mid_biu by (div_con + 1).

CRU_CLKSEL_CON11

Address: Operational Base(0x27200000) + offset (0x032C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_bpll_src_sel clk_bpll_src clock mux. 1'b0: clk_bpll 1'b1: xin_osc0_func
4:0	RW	0x03	clk_bpll_src_div Divide clk_bpll_src by (div_con + 1).

CRU_CLKSEL_CON12

Address: Operational Base(0x27200000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:0	RW	0x001403de	clk_matrix_audio_frac_0_div clk_matrix_audio_frac_0 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON13

Address: Operational Base(0x27200000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	clk_matrix_audio_frac_0_sel clk_matrix_audio_frac_0 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON14

Address: Operational Base(0x27200000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:0	RW	0x03355460	clk_matrix_audio_frac_1_div clk_matrix_audio_frac_1 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON15

Address: Operational Base(0x27200000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	clk_matrix_audio_frac_1_sel clk_matrix_audio_frac_1 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON16

Address: Operational Base(0x27200000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RW	0x002103de	clk_matrix_audio_frac_2_div clk_matrix_audio_frac_2 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON17

Address: Operational Base(0x27200000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	clk_matrix_audio_frac_2_sel clk_matrix_audio_frac_2 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON18

Address: Operational Base(0x27200000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31:0	RW	0x002103de	clk_matrix_audio_frac_3_div clk_matrix_audio_frac_3 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON19

Address: Operational Base(0x27200000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	aclk_vo0vop_channel_biu_sel aclk_vo0vop_channel_biu clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_lpll_src 2'b11: clk_bpll_src
11:8	RW	0x2	aclk_vo0vop_channel_biu_div Divide aclk_vo0vop_channel_biu by (div_con + 1).

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	hclk_vo0vop_channel_biu_sel hclk_vo0vop_channel_biu clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
5:4	RO	0x0	reserved
3:2	RW	0x0	hclk_top_biu_sel hclk_top_biu clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
1:0	RW	0x0	clk_matrix_audio_frac_3_sel clk_matrix_audio_frac_3 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON21

Address: Operational Base(0x27200000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:0	RW	0x001403de	clk_matrix_uart_frac_0_div clk_matrix_uart_frac_0 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON22

Address: Operational Base(0x27200000) + offset (0x0358)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	clk_matrix_uart_frac_0_sel clk_matrix_uart_frac_0 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON23

Address: Operational Base(0x27200000) + offset (0x035C)

Bit	Attr	Reset Value	Description
31:0	RW	0x03355460	clk_matrix_uart_frac_1_div clk_matrix_uart_frac_1 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON24

Address: Operational Base(0x27200000) + offset (0x0360)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	clk_matrix_uart_frac_1_sel clk_matrix_uart_frac_1 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON25

Address: Operational Base(0x27200000) + offset (0x0364)

Bit	Attr	Reset Value	Description
31:0	RW	0x002103de	clk_matrix_uart_frac_2_div clk_matrix_uart_frac_2 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON26

Address: Operational Base(0x27200000) + offset (0x0368)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:11	RW	0x0	clk_testout_sel clk_testout clock mux. 3'b000: clk_testout_grp0 3'b001: clk_testout_pvtpll_bigcore 3'b010: clk_testout_pvtpll_litcore 3'b011: clk_testout_hdmiphy_dbg 3'b100: 1'b0
10:8	RW	0x3	clk_testout_top_sel clk_testout_top clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: clk_spll_mux 3'b100: clk_deepslow
7:2	RW	0x3f	clk_testout_top_div Divide clk_testout_top by (div_con + 1).
1:0	RW	0x0	clk_matrix_uart_frac_2_sel clk_matrix_uart_frac_2 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON27

Address: Operational Base(0x27200000) + offset (0x036C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x3	clk_uart1_src_top_sel clk_uart1_src_top clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
12:5	RW	0x7f	clk_uart1_src_top_div Divide clk_uart1_src_top by (div_con + 1).
4:3	RO	0x0	reserved
2:0	RW	0x3	clk_testout_grp0_sel clk_testout_grp0 clock mux. 3'b000: clk_pvtmpmu_clkout_measure 3'b001: clk_testout_top 3'b010: clk_testout_pvtpll_gpu 3'b011: clk_testout_pvtpll_npu 3'b100: clk_testout_pvtpll_cci 3'b101: clk_testout_pvtpll_ddr

CRU_CLKSEL_CON28

Address: Operational Base(0x27200000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x07	clk_matrix_audio_int_2_div Divide clk_matrix_audio_int_2 by (div_con + 1).
9:5	RW	0x09	clk_matrix_audio_int_1_div Divide clk_matrix_audio_int_1 by (div_con + 1).
4:0	RW	0x0b	clk_matrix_audio_int_0_div Divide clk_matrix_audio_int_0 by (div_con + 1).

CRU_CLKSEL_CON29

Address: Operational Base(0x27200000) + offset (0x0374)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:9	RW	0x0	clk_pdm0_src_top_sel clk_pdm0_src_top clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
8:0	RW	0x001	clk_pdm0_src_top_div Divide clk_pdm0_src_top by (div_con + 1).

CRU_CLKSEL_CON30

Address: Operational Base(0x27200000) + offset (0x0378)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x07	clk_matrix_gmac0_125m_src_div Divide clk_matrix_gmac0_125m_src by (div_con + 1).
9:0	RO	0x000	reserved

CRU_CLKSEL_CON31

Address: Operational Base(0x27200000) + offset (0x037C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	lclk_asrc_src_0_sel lclk_asrc_src_0 clock mux. 2'b00: clk_matrix_audio_frac_0 2'b01: clk_matrix_audio_frac_1 2'b10: clk_matrix_audio_frac_2 2'b11: clk_matrix_audio_frac_3
9:5	RW	0x01	lclk_asrc_src_0_div Divide lclk_asrc_src_0 by (div_con + 1).
4:0	RW	0x07	clk_matrix_gmac1_125m_src_div Divide clk_matrix_gmac1_125m_src by (div_con + 1).

CRU_CLKSEL_CON32

Address: Operational Base(0x27200000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Bit	Attr	Reset Value	Description
6:5	RW	0x0	lclk_asrc_src_1_sel lclk_asrc_src_1 clock mux. 2'b00: clk_matrix_audio_frac_0 2'b01: clk_matrix_audio_frac_1 2'b10: clk_matrix_audio_frac_2 2'b11: clk_matrix_audio_frac_3
4:0	RW	0x01	lclk_asrc_src_1_div Divide lclk_asrc_src_1 by (div_con + 1).

CRU_CLKSEL_CON33

Address: Operational Base(0x27200000) + offset (0x0384)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	ref_clk0_out_pll_sel ref_clk0_out_pll clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_spll_mux 3'b011: clk_aupll_mux 3'b100: clk_lpll_src 3'b101: xin_osc0_func_mux
7:0	RW	0x1f	ref_clk0_out_pll_div Divide ref_clk0_out_pll by (div_con + 1).

CRU_CLKSEL_CON34

Address: Operational Base(0x27200000) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	ref_clk1_out_pll_sel ref_clk1_out_pll clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_spll_mux 3'b011: clk_aupll_mux 3'b100: clk_lpll_src 3'b101: xin_osc0_func_mux
7:0	RW	0x1f	ref_clk1_out_pll_div Divide ref_clk1_out_pll by (div_con + 1).

CRU_CLKSEL_CON35

Address: Operational Base(0x27200000) + offset (0x038C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	ref_clk2_out_pll_sel ref_clk2_out_pll clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_spll_mux 3'b011: clk_aupll_mux 3'b100: clk_lpll_src 3'b101: xin_osc0_func_mux
7:0	RW	0x1f	ref_clk2_out_pll_div Divide ref_clk2_out_pll by (div_con + 1).

CRU_CLKSEL_CON36

Address: Operational Base(0x27200000) + offset (0x0390)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	refclko25m_gmac1_out_sel refclko25m_gmac1_out clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
14:8	RW	0x27	refclko25m_gmac1_out_div Divide refclko25m_gmac1_out by (div_con + 1).
7	RW	0x1	refclko25m_gmac0_out_sel refclko25m_gmac0_out clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:0	RW	0x27	refclko25m_gmac0_out_div Divide refclko25m_gmac0_out by (div_con + 1).

CRU_CLKSEL_CON37

Address: Operational Base(0x27200000) + offset (0x0394)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x05	clk_bisrintf_pllsrc_div Divide clk_bisrintf_pllsrc by (div_con + 1). not, minimum value is 0x5 , max output freq is 166M; need to ensure clk_bisrintf_pllsrc is duty cycle 50%.
9:8	RW	0x2	clk_cifout_out_sel clk_cifout_out clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func_mux 2'b11: clk_spll_mux
7:0	RW	0x00	clk_cifout_out_div Divide clk_cifout_out by (div_con + 1).

CRU_CLKSEL_CON38

Address: Operational Base(0x27200000) + offset (0x0398)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	clk_mipi_cameraout_m0_sel clk_mipi_cameraout_m0 clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_spll_mux 2'b10: clk_gpll_mux 2'b11: clk_cpll_mux
7:0	RW	0x00	clk_mipi_cameraout_m0_div Divide clk_mipi_cameraout_m0 by (div_con + 1).

CRU_CLKSEL_CON39

Address: Operational Base(0x27200000) + offset (0x039C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	clk_mipi_cameraout_m1_sel clk_mipi_cameraout_m1 clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_spll_mux 2'b10: clk_gpll_mux 2'b11: clk_cpll_mux
7:0	RW	0x00	clk_mipi_cameraout_m1_div Divide clk_mipi_cameraout_m1 by (div_con + 1).

CRU_CLKSEL_CON40

Address: Operational Base(0x27200000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x00	reserved
12	RW	0x0	CRU_OSC_sel osc select flag for software 1'b0: sel 24M OSC 1'b1: sel 26M OSC
11	RO	0x0	reserved
10	RW	0x0	xin_osc0_func_mux_sel xin_osc0_func_mux clock mux. 1'b0: xin_osc0_func 1'b1: xin_osc0_pll_usbphy
9:8	RW	0x0	clk_mipi_cameraout_m2_sel clk_mipi_cameraout_m2 clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_spll_mux 2'b10: clk_gpll_mux 2'b11: clk_cpll_mux

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	clk_mipi_cameraout_m2_div Divide clk_mipi_cameraout_m2 by (div_con + 1).

CRU_CLKSEL_CON41

Address: Operational Base(0x27200000) + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:7	RW	0x0	mclk_pdm0_src_top_sel mclk_pdm0_src_top clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
6:2	RW	0x01	mclk_pdm0_src_top_div Divide mclk_pdm0_src_top by (div_con + 1).
1:0	RO	0x0	reserved

CRU_CLKSEL_CON42

Address: Operational Base(0x27200000) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_asrc_2ch_1_sel clk_asrc_2ch_1 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux
13:9	RW	0x05	clk_asrc_2ch_1_div Divide clk_asrc_2ch_1 by (div_con + 1).
8:7	RW	0x0	clk_asrc_2ch_0_sel clk_asrc_2ch_0 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux
6:2	RW	0x05	clk_asrc_2ch_0_div Divide clk_asrc_2ch_0 by (div_con + 1).
1:0	RW	0x0	hclk_audio_root_sel hclk_audio_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON43

Address: Operational Base(0x27200000) + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	clk_asrc_4ch_1_sel clk_asrc_4ch_1 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux
11:7	RW	0x01	clk_asrc_4ch_1_div Divide clk_asrc_4ch_1 by (div_con + 1).
6:5	RW	0x2	clk_asrc_4ch_0_sel clk_asrc_4ch_0 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux
4:0	RW	0x01	clk_asrc_4ch_0_div Divide clk_asrc_4ch_0 by (div_con + 1).

CRU_CLKSEL_CON44

Address: Operational Base(0x27200000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:11	RW	0x0	mclk_sai0_sel mclk_sai0 clock mux. 2'b00: mclk_sai0_src 2'b01: sai0_mclkin 2'b10: sai1_mclkin
10:8	RW	0x0	mclk_sai0_src_sel mclk_sai0_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai0_src_div Divide mclk_sai0_src by (div_con + 1).

CRU_CLKSEL_CON45

Address: Operational Base(0x27200000) + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x1	mclk_spdif_rx1_sel mclk_spdif_rx1 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux
11:7	RW	0x01	mclk_spdif_rx1_div Divide mclk_spdif_rx1 by (div_con + 1).
6:5	RW	0x1	mclk_spdif_rx0_sel mclk_spdif_rx0 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux
4:0	RW	0x01	mclk_spdif_rx0_div Divide mclk_spdif_rx0 by (div_con + 1).

CRU_CLKSEL_CON46

Address: Operational Base(0x27200000) + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	mclk_sai1_sel mclk_sai1 clock mux. 1'b0: mclk_sai1_src 1'b1: sai1_mclkin
10:8	RW	0x0	mclk_sai1_src_sel mclk_sai1_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai1_src_div Divide mclk_sai1_src by (div_con + 1).

CRU_CLKSEL_CON47

Address: Operational Base(0x27200000) + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:11	RW	0x0	mclk_sai2_sel mclk_sai2 clock mux. 2'b00: mclk_sai2_src 2'b01: sai2_mclkin 2'b10: sai1_mclkin

Bit	Attr	Reset Value	Description
10:8	RW	0x0	mclk_sai2_src_sel mclk_sai2_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai2_src_div Divide mclk_sai2_src by (div_con + 1).

CRU_CLKSEL_CON48

Address: Operational Base(0x27200000) + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:11	RW	0x0	mclk_sai3_sel mclk_sai3 clock mux. 2'b00: mclk_sai3_src 2'b01: sai3_mclkin 2'b10: sai1_mclkin
10:8	RW	0x0	mclk_sai3_src_sel mclk_sai3_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai3_src_div Divide mclk_sai3_src by (div_con + 1).

CRU_CLKSEL_CON49

Address: Operational Base(0x27200000) + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:11	RW	0x0	mclk_sai4_sel mclk_sai4 clock mux. 2'b00: mclk_sai4_src 2'b01: sai4_mclkin 2'b10: sai1_mclkin

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	mclk_sai4_src_sel mclk_sai4_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai4_src_div Divide mclk_sai4_src by (div_con + 1).

CRU_CLKSEL_CON50

Address: Operational Base(0x27200000) + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:9	RW	0x0	clk_pdm1_sel clk_pdm1 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
8:0	RW	0x01f	clk_pdm1_div Divide clk_pdm1 by (div_con + 1).

CRU_CLKSEL_CON51

Address: Operational Base(0x27200000) + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:5	RW	0x0	mclk_pdm1_sel mclk_pdm1 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
4:0	RW	0x0b	mclk_pdm1_div Divide mclk_pdm1 by (div_con + 1).

CRU_CLKSEL_CON52

Address: Operational Base(0x27200000) + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	mclk_spdif_tx0_sel mclk_spdif_tx0 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_spdif_tx0_div Divide mclk_spdif_tx0 by (div_con + 1).

CRU_CLKSEL_CON53

Address: Operational Base(0x27200000) + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	mclk_spdif_tx1_sel mclk_spdif_tx1 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_spdif_tx1_div Divide mclk_spdif_tx1 by (div_con + 1).

CRU_CLKSEL_CON55

Address: Operational Base(0x27200000) + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	aclk_bus_root_sel aclk_bus_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
8:4	RW	0x02	aclk_bus_root_div Divide aclk_bus_root by (div_con + 1).

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	pclk_bus_root_sel pclk_bus_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
1:0	RW	0x0	hclk_bus_root_sel hclk_bus_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON56

Address: Operational Base(0x27200000) + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	clk_can1_sel clk_can1 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
11:7	RW	0x03	clk_can1_div Divide clk_can1 by (div_con + 1).
6:5	RW	0x0	clk_can0_sel clk_can0 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
4:0	RW	0x03	clk_can0_div Divide clk_can0 by (div_con + 1).

CRU_CLKSEL_CON57

Address: Operational Base(0x27200000) + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_i2c8_sel clk_i2c8 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
13:12	RW	0x0	clk_i2c7_sel clk_i2c7 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	clk_i2c6_sel clk_i2c6 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
9:8	RW	0x0	clk_i2c5_sel clk_i2c5 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
7:6	RW	0x0	clk_i2c4_sel clk_i2c4 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
5:4	RW	0x0	clk_i2c3_sel clk_i2c3 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
3:2	RW	0x0	clk_i2c2_sel clk_i2c2 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
1:0	RW	0x0	clk_i2c1_sel clk_i2c1 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON58

Address: Operational Base(0x27200000) + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_saradc_sel clk_saradc clock mux. 1'b0: clk_gpll_mux 1'b1: xin_osc0_func
11:4	RW	0x3b	clk_saradc_div Divide clk_saradc by (div_con + 1).
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	clk_i2c9_sel clk_i2c9 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON59

Address: Operational Base(0x27200000) + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:0	RW	0x0b	clk_tsadc_div Divide clk_tsadc by (div_con + 1).

CRU_CLKSEL_CON60

Address: Operational Base(0x27200000) + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart0_sel sclk_uart0 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart0_div Divide sclk_uart0 by (div_con + 1).

CRU_CLKSEL_CON61

Address: Operational Base(0x27200000) + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart2_sel sclk_uart2 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2

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Bit	Attr	Reset Value	Description
7:0	RW	0x7f	sclk_uart2_div Divide sclk_uart2 by (div_con + 1).

CRU_CLKSEL_CON62

Address: Operational Base(0x27200000) + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart3_sel sclk_uart3 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart3_div Divide sclk_uart3 by (div_con + 1).

CRU_CLKSEL_CON63

Address: Operational Base(0x27200000) + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart4_sel sclk_uart4 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart4_div Divide sclk_uart4 by (div_con + 1).

CRU_CLKSEL_CON64

Address: Operational Base(0x27200000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x3	sclk_uart5_sel sclk_uart5 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart5_div Divide sclk_uart5 by (div_con + 1).

CRU_CLKSEL_CON65

Address: Operational Base(0x27200000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart6_sel sclk_uart6 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart6_div Divide sclk_uart6 by (div_con + 1).

CRU_CLKSEL_CON66

Address: Operational Base(0x27200000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart7_sel sclk_uart7 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart7_div Divide sclk_uart7 by (div_con + 1).

CRU_CLKSEL_CON67

Address: Operational Base(0x27200000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart8_sel sclk_uart8 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart8_div Divide sclk_uart8 by (div_con + 1).

CRU_CLKSEL_CON68

Address: Operational Base(0x27200000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart9_sel sclk_uart9 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart9_div Divide sclk_uart9 by (div_con + 1).

CRU_CLKSEL_CON69

Address: Operational Base(0x27200000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x3	sclk_uart10_sel sclk_uart10 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2

Bit	Attr	Reset Value	Description
7:0	RW	0x7f	sclk_uart10_div Divide sclk_uart10 by (div_con + 1).

CRU_CLKSEL_CON70

Address: Operational Base(0x27200000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x0	clk_spi0_sel clk_spi0 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_gpll_div8_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func
12:11	RO	0x0	reserved
10:8	RW	0x3	sclk_uart11_sel sclk_uart11 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: xin_osc0_func_mux 3'b100: clk_matrix_uart_frac_0 3'b101: clk_matrix_uart_frac_1 3'b110: clk_matrix_uart_frac_2
7:0	RW	0x7f	sclk_uart11_div Divide sclk_uart11 by (div_con + 1).

CRU_CLKSEL_CON71

Address: Operational Base(0x27200000) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	clk_timer0_root_sel clk_timer0_root clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
13:10	RO	0x0	reserved
9:8	RW	0x2	clk_pwm1_sel clk_pwm1 clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
7:6	RW	0x0	clk_spi4_sel clk_spi4 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_gpll_div8_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	clk_spi3_sel clk_spi3 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_gpll_div8_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func
3:2	RW	0x0	clk_spi2_sel clk_spi2 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_gpll_div8_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func
1:0	RW	0x0	clk_spi1_sel clk_spi1 clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_gpll_div8_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON72

Address: Operational Base(0x27200000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x1	clk_timer7_sel clk_timer7 clock mux. 2'b00: clk_cpll_div10_src 2'b01: xin_osc0_func 2'b10: lclk_asrc_src_0
11:7	RW	0x00	clk_timer7_div Divide clk_timer7 by (div_con + 1).
6	RW	0x1	clk_timer1_root_sel clk_timer1_root clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
5	RW	0x1	dclk_decom_sel dclk_decom clock mux. 1'b0: clk_gpll_mux 1'b1: clk_spll_mux
4:0	RW	0x01	dclk_decom_div Divide dclk_decom by (div_con + 1).

CRU_CLKSEL_CON73

Address: Operational Base(0x27200000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:13	RW	0x0	hclk_bus_cm0_root_sel hclk_bus_cm0_root clock mux. 2'b00: clk_gpll_div3_src 2'b01: clk_gpll_div6_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func
12:7	RO	0x00	reserved
6:5	RW	0x1	clk_timer8_sel clk_timer8 clock mux. 2'b00: clk_cpll_div10_src 2'b01: xin_osc0_func 2'b10: lclk_asrc_src_1
4:0	RW	0x00	clk_timer8_div Divide clk_timer8 by (div_con + 1).

CRU_CLKSEL_CON74

Address: Operational Base(0x27200000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:11	RW	0x0	clk_counter_pwm1_sel clk_counter_pwm1 clock mux. 3'b000: sai0_mclkin 3'b001: sai1_mclkin 3'b010: sai2_mclkin 3'b011: sai3_mclkin 3'b100: sai4_mclkin 3'b101: sai_sclkin_counter
10:8	RW	0x0	clk_freq_pwm1_sel clk_freq_pwm1 clock mux. 3'b000: sai0_mclkin 3'b001: sai1_mclkin 3'b010: sai2_mclkin 3'b011: sai3_mclkin 3'b100: sai4_mclkin 3'b101: sai_sclkin_freq
7:6	RW	0x2	clk_pwm2_sel clk_pwm2 clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
5	RW	0x1	clk_bus_cm0_rtc_sel clk_bus_cm0_rtc clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
4:0	RW	0x00	clk_bus_cm0_rtc_div Divide clk_bus_cm0_rtc by (div_con + 1).

CRU_CLKSEL_CON75

Address: Operational Base(0x27200000) + offset (0x042C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:3	RW	0x0	sai_sclkin_counter_sel sai_sclkin_counter clock mux. 3'b000: sai0_sclk_in 3'b001: sai1_sclk_in 3'b010: sai2_sclk_in 3'b011: sai3_sclk_in 3'b100: sai4_sclk_in
2:0	RW	0x0	sai_sclkin_freq_sel sai_sclkin_freq clock mux. 3'b000: sai0_sclk_in 3'b001: sai1_sclk_in 3'b010: sai2_sclk_in 3'b011: sai3_sclk_in 3'b100: sai4_sclk_in

CRU_CLKSEL_CON76

Address: Operational Base(0x27200000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	aclk_ddr_root_sel aclk_ddr_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
11:7	RW	0x01	aclk_ddr_root_div Divide aclk_ddr_root by (div_con + 1).
6:5	RW	0x0	pclk_ddr_root_sel pclk_ddr_root clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
4:0	RW	0x05	pclk_ddr_root_div Divide pclk_ddr_root by (div_con + 1).

CRU_CLKSEL_CON77

Address: Operational Base(0x27200000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	clk_ddr_cm0_rtc_sel clk_ddr_cm0_rtc clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow

Bit	Attr	Reset Value	Description
11:7	RW	0x00	clk_ddr_cm0_rtc_div Divide clk_ddr_cm0_rtc by (div_con + 1).
6	RW	0x1	clk_ddr_timer_root_sel clk_ddr_timer_root clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
5	RW	0x1	hclk_ddr_root_sel hclk_ddr_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x01	hclk_ddr_root_div Divide hclk_ddr_root by (div_con + 1).

CRU_CLKSEL_CON78

Address: Operational Base(0x27200000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	clk_i3c1_sel clk_i3c1 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: clk_spll_mux
11:7	RW	0x02	clk_i3c1_div Divide clk_i3c1 by (div_con + 1).
6:5	RW	0x0	clk_i3c0_sel clk_i3c0 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: clk_spll_mux
4:0	RW	0x02	clk_i3c0_div Divide clk_i3c0 by (div_con + 1).

CRU_CLKSEL_CON80

Address: Operational Base(0x27200000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	mbist_clk_aclk_rknn0_sel mbist_clk_aclk_rknn0 clock mux. 1'b0: mbist_clk_npu 1'b1: clk_npu_pvtpll_src

CRU_CLKSEL_CON82

Address: Operational Base(0x27200000) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	mbist_clk_aclk_rknn1_sel mbist_clk_aclk_rknn1 clock mux. 1'b0: mbist_clk_npu 1'b1: clk_npu_pvtpll_src

CRU_CLKSEL_CON86

Address: Operational Base(0x27200000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_rknn_dsu0_sel clk_rknn_dsu0 clock mux. 1'b0: clk_rknn_dsu0_src_t 1'b1: clk_npu_pvtpll_src
14:10	RW	0x00	clk_rknn_dsu0_div Divide clk_rknn_dsu0 by (div_con + 1).
9	RW	0x0	clk_npu_pvtpll_src_sel clk_npu_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_npu_pvtpll
8:7	RW	0x2	clk_rknn_dsu0_src_t_sel clk_rknn_dsu0_src_t clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: clk_spll_mux
6:2	RW	0x00	clk_rknn_dsu0_src_t_div Divide clk_rknn_dsu0_src_t by (div_con + 1).
1:0	RW	0x0	hclk_rknn_root_sel hclk_rknn_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON87

Address: Operational Base(0x27200000) + offset (0x045C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	mbist_clk_aclk_rknntop_sel mbist_clk_aclk_rknntop clock mux. 1'b0: mbist_clk_npu 1'b1: clk_npu_pvtpll_src

Bit	Attr	Reset Value	Description
10	RW	0x1	clk_npu_cm0_rtc_sel clk_npu_cm0_rtc clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
9:5	RW	0x00	clk_npu_cm0_rtc_div Divide clk_npu_cm0_rtc by (div_con + 1).
4:3	RW	0x0	hclk_npu_cm0_root_sel hclk_npu_cm0_root clock mux. 2'b00: clk_gpll_div3_src 2'b01: clk_gpll_div6_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func
2	RW	0x1	clk_nputimer_root_sel clk_nputimer_root clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
1:0	RW	0x0	pclk_nputop_root_sel pclk_nputop_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func

CRU_CLKSEL_CON88

Address: Operational Base(0x27200000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	aclk_nvm_root_sel aclk_nvm_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:2	RW	0x03	aclk_nvm_root_div Divide aclk_nvm_root by (div_con + 1).
1:0	RW	0x0	hclk_nvm_root_sel hclk_nvm_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON89

Address: Operational Base(0x27200000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	cclk_src_emmc_sel cclk_src_emmc clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func

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Bit	Attr	Reset Value	Description
13:8	RW	0x05	cclk_src_emmc_div DT50 division register. Divide cclk_src_emmc by (div_con + 1).
7:6	RW	0x0	sclk_fspi_x2_sel sclk_fspi_x2 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
5:0	RW	0x02	sclk_fspi_x2_div DT50 division register. Divide sclk_fspi_x2 by (div_con + 1).

CRU_CLKSEL_CON90

Address: Operational Base(0x27200000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	bclk_emmc_sel bclk_emmc clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON92

Address: Operational Base(0x27200000) + offset (0x0470)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	aclk_php_root_sel aclk_php_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
8:4	RW	0x03	aclk_php_root_div Divide aclk_php_root by (div_con + 1).
3:2	RO	0x0	reserved
1:0	RW	0x0	pclk_php_root_sel pclk_php_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func

CRU_CLKSEL_CON93

Address: Operational Base(0x27200000) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x1	clk_rxoob1_sel clk_rxoob1 clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
14:8	RW	0x13	clk_rxoob1_div Divide clk_rxoob1 by (div_con + 1).
7	RW	0x1	clk_rxoob0_sel clk_rxoob0 clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:0	RW	0x13	clk_rxoob0_div Divide clk_rxoob0 by (div_con + 1).

CRU_CLKSEL_CON103

Address: Operational Base(0x27200000) + offset (0x049C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	pclk_sdgmac_root_sel pclk_sdgmac_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
7	RW	0x0	aclk_sdgmac_root_sel aclk_sdgmac_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:2	RW	0x03	aclk_sdgmac_root_div Divide aclk_sdgmac_root by (div_con + 1).
1:0	RW	0x0	hclk_sdgmac_root_sel hclk_sdgmac_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON104

Address: Operational Base(0x27200000) + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x1	clk_gmac1_ptp_ref_src_sel clk_gmac1_ptp_ref_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: gmac1_ptp_refclk_in
12:8	RW	0x0f	clk_gmac1_ptp_ref_src_div Divide clk_gmac1_ptp_ref_src by (div_con + 1).

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	cclk_src_sdio_sel cclk_src_sdio clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
5:0	RW	0x02	cclk_src_sdio_div DT50 division register. Divide cclk_src_sdio by (div_con + 1).

CRU_CLKSEL_CON105

Address: Operational Base(0x27200000) + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x0	cclk_src_sdmmc0_sel cclk_src_sdmmc0 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
12:7	RW	0x02	cclk_src_sdmmc0_div DT50 division register. Divide cclk_src_sdmmc0 by (div_con + 1).
6:5	RW	0x1	clk_gmac0_ptp_ref_src_sel clk_gmac0_ptp_ref_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: gmac0_ptp_refclk_in
4:0	RW	0x0f	clk_gmac0_ptp_ref_src_div Divide clk_gmac0_ptp_ref_src by (div_con + 1).

CRU_CLKSEL_CON106

Address: Operational Base(0x27200000) + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	aclk_dsmc_root_sel aclk_dsmc_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
12:8	RW	0x05	aclk_dsmc_root_div Divide aclk_dsmc_root by (div_con + 1).
7:6	RW	0x0	sclk_fspi1_x2_sel sclk_fspi1_x2 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
5:0	RW	0x02	sclk_fspi1_x2_div DT50 division register. Divide sclk_fspi1_x2 by (div_con + 1).

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CRU_CLKSEL_CON107

Address: Operational Base(0x27200000) + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:11	RW	0x0	clk_flexbus_tx_sel clk_flexbus_tx clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
10:6	RW	0x05	clk_flexbus_tx_div Divide clk_flexbus_tx by (div_con + 1).
5	RW	0x0	clk_dsmc_sys_sel clk_dsmc_sys clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x02	clk_dsmc_sys_div DT50 division register. Divide clk_dsmc_sys by (div_con + 1).

CRU_CLKSEL_CON108

Address: Operational Base(0x27200000) + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:5	RW	0x0	clk_flexbus_rx_sel clk_flexbus_rx clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
4:0	RW	0x05	clk_flexbus_rx_div Divide clk_flexbus_rx by (div_con + 1).

CRU_CLKSEL_CON110

Address: Operational Base(0x27200000) + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	aclk_rkvdec_root_bak_sel aclk_rkvdec_root_bak clock mux. 2'b00: clk_cpll_mux 2'b01: clk_vpll_mux 2'b10: clk_lpll_src 2'b11: clk_bpll_src
13:9	RW	0x01	aclk_rkvdec_root_bak_div Divide aclk_rkvdec_root_bak by (div_con + 1).

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Bit	Attr	Reset Value	Description
8:7	RW	0x1	aclk_rkvdec_root_pre_sel aclk_rkvdec_root_pre clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_spll_mux
6:2	RW	0x01	aclk_rkvdec_root_pre_div Divide aclk_rkvdec_root_pre by (div_con + 1).
1:0	RW	0x0	hclk_rkvdec_root_sel hclk_rkvdec_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON111

Address: Operational Base(0x27200000) + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:5	RW	0x1	clk_rkvdec_hevc_ca_sel clk_rkvdec_hevc_ca clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_lpll_src 2'b11: clk_bpll_src
4:0	RW	0x00	clk_rkvdec_hevc_ca_div Divide clk_rkvdec_hevc_ca by (div_con + 1).

CRU_CLKSEL_CON115

Address: Operational Base(0x27200000) + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	pclk_usb_root_sel pclk_usb_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
11	RW	0x0	aclk_usb_root_sel aclk_usb_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
10:6	RW	0x03	aclk_usb_root_div Divide aclk_usb_root by (div_con + 1).
5	RW	0x1	aclk_ufs_root_sel aclk_ufs_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux

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Bit	Attr	Reset Value	Description
4:0	RW	0x05	aclk_ufs_root_div Divide aclk_ufs_root by (div_con + 1).

CRU_CLKSEL_CON118

Address: Operational Base(0x27200000) + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	hclk_vpu_root_sel hclk_vpu_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
9:8	RW	0x0	aclk_vpu_mid_root_sel aclk_vpu_mid_root clock mux. 2'b00: clk_gpll_div2_src 2'b01: clk_gpll_div3_src 2'b10: clk_gpll_div4_src 2'b11: xin_osc0_func
7:5	RW	0x1	aclk_vpu_root_sel aclk_vpu_root clock mux. 3'b000: clk_gpll_mux 3'b001: clk_spll_mux 3'b010: clk_cpll_mux 3'b011: clk_bpll_src 3'b100: clk_lpll_src
4:0	RW	0x00	aclk_vpu_root_div Divide aclk_vpu_root by (div_con + 1).

CRU_CLKSEL_CON119

Address: Operational Base(0x27200000) + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8:7	RW	0x0	aclk_vpu_low_root_sel aclk_vpu_low_root clock mux. 2'b00: clk_gpll_div3_src 2'b01: clk_gpll_div6_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func
6:5	RW	0x3	aclk_jpeg_root_sel aclk_jpeg_root clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux 2'b11: clk_spll_mux
4:0	RW	0x00	aclk_jpeg_root_div Divide aclk_jpeg_root by (div_con + 1).

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CRU_CLKSEL_CON120

Address: Operational Base(0x27200000) + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_core_vdpp_sel clk_core_vdpp clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
12:8	RW	0x01	clk_core_vdpp_div Divide clk_core_vdpp by (div_con + 1).
7:5	RW	0x1	clk_core_rga2e_0_sel clk_core_rga2e_0 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_spll_mux 3'b010: clk_cpll_mux 3'b011: clk_bpll_src 3'b100: clk_lpll_src
4:0	RW	0x00	clk_core_rga2e_0_div Divide clk_core_rga2e_0 by (div_con + 1).

CRU_CLKSEL_CON121

Address: Operational Base(0x27200000) + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:5	RW	0x1	clk_core_rga2e_1_sel clk_core_rga2e_1 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_spll_mux 3'b010: clk_cpll_mux 3'b011: clk_bpll_src 3'b100: clk_lpll_src
4:0	RW	0x00	clk_core_rga2e_1_div Divide clk_core_rga2e_1 by (div_con + 1).

CRU_CLKSEL_CON122

Address: Operational Base(0x27200000) + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x03355460	dclk_ebc_frac_src_div dclk_ebc_frac_src fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON123

Address: Operational Base(0x27200000) + offset (0x04EC)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	dclk_ebc_sel dclk_ebc clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_vpll_mux 3'b011: clk_aupll_mux 3'b100: clk_lpll_src 3'b101: dclk_ebc_frac_src 3'b110: xin_osc0_func
11:3	RW	0x002	dclk_ebc_div Divide dclk_ebc by (div_con + 1).
2:0	RW	0x3	dclk_ebc_frac_src_sel dclk_ebc_frac_src clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_vpll_mux 3'b011: clk_aupll_mux 3'b100: xin_osc0_func

CRU_CLKSEL_CON124

Address: Operational Base(0x27200000) + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x2	clk_vepu0_core_sel clk_vepu0_core clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_spll_mux 3'b011: clk_lpll_src 3'b100: clk_bpll_src
12:8	RW	0x00	clk_vepu0_core_div Divide clk_vepu0_core by (div_con + 1).
7	RW	0x0	aclk_vepu0_root_sel aclk_vepu0_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:2	RW	0x02	aclk_vepu0_root_div Divide aclk_vepu0_root by (div_con + 1).
1:0	RW	0x0	hclk_vepu0_root_sel hclk_vepu0_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON128

Address: Operational Base(0x27200000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	pclk_vi_root_sel pclk_vi_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
9:8	RW	0x2	hclk_vi_root_sel hclk_vi_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: aclk_vi_root_inter 2'b11: xin_osc0_func
7:5	RW	0x0	aclk_vi_root_sel aclk_vi_root clock mux. 3'b000: clk_gpll_mux 3'b001: clk_spll_mux 3'b010: clk_isp_pvtpll_src 3'b011: clk_bpll_src 3'b100: clk_lpll_src
4:0	RW	0x01	aclk_vi_root_div Divide aclk_vi_root by (div_con + 1).

CRU_CLKSEL_CON129

Address: Operational Base(0x27200000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:11	RW	0x0	clk_isp0_core_sel clk_isp0_core clock mux. 3'b000: clk_gpll_mux 3'b001: clk_spll_mux 3'b010: clk_isp_pvtpll_src 3'b011: clk_bpll_src 3'b100: clk_lpll_src
10:6	RW	0x01	clk_isp0_core_div Divide clk_isp0_core by (div_con + 1).
5	RW	0x0	dclk_vicap_sel dclk_vicap clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x01	dclk_vicap_div Divide dclk_vicap by (div_con + 1).

CRU_CLKSEL_CON130

Address: Operational Base(0x27200000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:10	RW	0x2	aclk_vi_root_inter_div Divide aclk_vi_root_inter by (div_con + 1).
9	RW	0x0	clk_isp_pvtpll_src_sel clk_isp_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clksp_pvtpll
8:7	RW	0x0	iclk_csihost01_sel iclk_csihost01 clock mux. 2'b00: clk_gpll_div3_src 2'b01: clk_gpll_div6_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func
6:0	RO	0x00	reserved

CRU_CLKSEL_CON144

Address: Operational Base(0x27200000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	pclk_vop_root_sel pclk_vop_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
11:10	RW	0x0	hclk_vop_root_sel hclk_vop_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
9:8	RO	0x0	reserved
7:5	RW	0x3	aclk_vop_root_sel aclk_vop_root clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: clk_spll_mux 3'b100: clk_lpll_src
4:0	RW	0x00	aclk_vop_root_div Divide aclk_vop_root by (div_con + 1).

CRU_CLKSEL_CON145

Address: Operational Base(0x27200000) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	dclk_vp0_src_sel dclk_vp0_src clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_vpll_mux 3'b011: clk_bpll_src 3'b100: clk_lpll_src
7:0	RW	0x01	dclk_vp0_src_div Divide dclk_vp0_src by (div_con + 1).

CRU_CLKSEL_CON146

Address: Operational Base(0x27200000) + offset (0x0548)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	dclk_vp1_src_sel dclk_vp1_src clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_vpll_mux 3'b011: clk_bpll_src 3'b100: clk_lpll_src
7:0	RW	0x03	dclk_vp1_src_div Divide dclk_vp1_src by (div_con + 1).

CRU_CLKSEL_CON147

Address: Operational Base(0x27200000) + offset (0x054C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	dclk_vp2_sel dclk_vp2 clock mux. 1'b0: dclk_vp2_src 1'b1: clk_hdmiphy_pixel0_o
12	RW	0x0	dclk_vp1_sel dclk_vp1 clock mux. 1'b0: dclk_vp1_src 1'b1: clk_hdmiphy_pixel0_o
11	RW	0x0	dclk_vp0_sel dclk_vp0 clock mux. 1'b0: dclk_vp0_src 1'b1: clk_hdmiphy_pixel0_o

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	dclk_vp2_src_sel dclk_vp2_src clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_vpll_mux 3'b011: clk_bpll_src 3'b100: clk_lpll_src
7:0	RW	0x07	dclk_vp2_src_div Divide dclk_vp2_src by (div_con + 1).

CRU_CLKSEL_CON149

Address: Operational Base(0x27200000) + offset (0x0554)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:11	RW	0x0	pclk_vo0_root_sel pclk_vo0_root clock mux. 2'b00: clk_gpll_div8_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
10:9	RO	0x0	reserved
8:7	RW	0x0	hclk_vo0_root_sel hclk_vo0_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
6:5	RW	0x0	aclk_vo0_root_sel aclk_vo0_root clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_lpll_src 2'b11: clk_bpll_src
4:0	RW	0x02	aclk_vo0_root_div Divide aclk_vo0_root by (div_con + 1).

CRU_CLKSEL_CON151

Address: Operational Base(0x27200000) + offset (0x055C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_hdmitx0_arc_sel clk_hdmitx0_arc clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
14:10	RW	0x09	clk_hdmitx0_arc_div Divide clk_hdmitx0_arc by (div_con + 1).

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Bit	Attr	Reset Value	Description
9:7	RW	0x2	clk_dsihost0_sel clk_dsihost0 clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_spll_mux 3'b011: clk_vpll_mux 3'b100: clk_bpll_src 3'b101: clk_lpll_src
6:0	RW	0x02	clk_dsihost0_div Divide clk_dsihost0 by (div_con + 1).

CRU_CLKSEL_CON152

Address: Operational Base(0x27200000) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2:1	RW	0x0	clk_edp0_200m_sel clk_edp0_200m clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
0	RO	0x0	reserved

CRU_CLKSEL_CON154

Address: Operational Base(0x27200000) + offset (0x0568)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	mclk_sai5_sel mclk_sai5 clock mux. 1'b0: mclk_sai5_src 1'b1: sai1_mclkin
12:10	RW	0x0	mclk_sai5_src_sel mclk_sai5_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
9:2	RW	0x01	mclk_sai5_src_div Divide mclk_sai5_src by (div_con + 1).
1:0	RO	0x0	reserved

CRU_CLKSEL_CON155

Address: Operational Base(0x27200000) + offset (0x056C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	mclk_sai6_sel mclk_sai6 clock mux. 1'b0: mclk_sai6_src 1'b1: sai1_mclkin
10:8	RW	0x0	mclk_sai6_src_sel mclk_sai6_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai6_src_div Divide mclk_sai6_src by (div_con + 1).

CRU_CLKSEL_CON156

Address: Operational Base(0x27200000) + offset (0x0570)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x1	mclk_spdif_rx2_sel mclk_spdif_rx2 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_aupll_mux
12:8	RW	0x01	mclk_spdif_rx2_div Divide mclk_spdif_rx2 by (div_con + 1).
7:5	RW	0x0	mclk_spdif_tx2_sel mclk_spdif_tx2 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
4:0	RW	0x01	mclk_spdif_tx2_div Divide mclk_spdif_tx2 by (div_con + 1).

CRU_CLKSEL_CON157

Address: Operational Base(0x27200000) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	mclk_sai8_sel mclk_sai8 clock mux. 1'b0: mclk_sai8_src 1'b1: sai1_mclkin
10:8	RW	0x0	mclk_sai8_src_sel mclk_sai8_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai8_src_div Divide mclk_sai8_src by (div_con + 1).

CRU_CLKSEL_CON158

Address: Operational Base(0x27200000) + offset (0x0578)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:9	RW	0x0	pclk_vo1_root_sel pclk_vo1_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
8:7	RW	0x0	hclk_vo1_root_sel hclk_vo1_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
6:5	RW	0x0	aclk_vo1_root_sel aclk_vo1_root clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_lpll_src 2'b11: clk_bpll_src
4:0	RW	0x02	aclk_vo1_root_div Divide aclk_vo1_root by (div_con + 1).

CRU_CLKSEL_CON159

Address: Operational Base(0x27200000) + offset (0x057C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	mclk_sai7_sel mclk_sai7 clock mux. 1'b0: mclk_sai7_src 1'b1: sai1_mclkin
10:8	RW	0x0	mclk_sai7_src_sel mclk_sai7_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai7_src_div Divide mclk_sai7_src by (div_con + 1).

CRU_CLKSEL_CON160

Address: Operational Base(0x27200000) + offset (0x0580)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	mclk_spdif_tx3_sel mclk_spdif_tx3 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_spdif_tx3_div Divide mclk_spdif_tx3 by (div_con + 1).

CRU_CLKSEL_CON161

Address: Operational Base(0x27200000) + offset (0x0584)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:0	RW	0x49	clk_aux16mhz_0_div Divide clk_aux16mhz_0 by (div_con + 1).

CRU_CLKSEL_CON162

Address: Operational Base(0x27200000) + offset (0x0588)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	mclk_sai9_sel mclk_sai9 clock mux. 1'b0: mclk_sai9_src 1'b1: sai1_mclkin
10:8	RW	0x0	mclk_sai9_src_sel mclk_sai9_src clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_sai9_src_div Divide mclk_sai9_src by (div_con + 1).

CRU_CLKSEL_CON163

Address: Operational Base(0x27200000) + offset (0x058C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	mclk_spdif_tx4_sel mclk_spdif_tx4 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_spdif_tx4_div Divide mclk_spdif_tx4 by (div_con + 1).

CRU_CLKSEL_CON164

Address: Operational Base(0x27200000) + offset (0x0590)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	mclk_spdif_tx5_sel mclk_spdif_tx5 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_matrix_audio_frac_0 3'b010: clk_matrix_audio_frac_1 3'b011: clk_matrix_audio_frac_2 3'b100: clk_matrix_audio_frac_3 3'b101: clk_matrix_audio_int_0 3'b110: clk_matrix_audio_int_1 3'b111: clk_matrix_audio_int_2
7:0	RW	0x01	mclk_spdif_tx5_div Divide mclk_spdif_tx5 by (div_con + 1).

CRU_CLKSEL_CON165

Address: Operational Base(0x27200000) + offset (0x0594)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	clk_gpu_pvtpll_src_sel clk_gpu_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_gpu_pvtpll
8	RW	0x0	clk_gpu_inner_sel clk_gpu_inner clock mux. 1'b0: clk_gpu_src 1'b1: clk_gpu_pvtpll_src
7:5	RW	0x2	clk_gpu_src_pre_sel clk_gpu_src_pre clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_aupll_mux 3'b011: clk_spll_mux 3'b100: clk_lpll_src
4:0	RW	0x00	clk_gpu_src_pre_div Divide clk_gpu_src_pre by (div_con + 1).

CRU_CLKSEL_CON166

Address: Operational Base(0x27200000) + offset (0x0598)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	pclk_gpu_root_sel pclk_gpu_root clock mux. 2'b00: clk_cpll_div10_src 2'b01: clk_cpll_div20_src 2'b10: xin_osc0_func
9:5	RW	0x00	aclk_m0_gpu_biu_div Divide aclk_m0_gpu_biu by (div_con + 1).

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	aclk_s_gpu_biu_div Divide aclk_s_gpu_biu by (div_con + 1).

CRU_CLKSEL_CON167

Address: Operational Base(0x27200000) + offset (0x059C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:9	RW	0x00	aclk_center_root_div Divide aclk_center_root by (div_con + 1).
8:0	RO	0x000	reserved

CRU_CLKSEL_CON168

Address: Operational Base(0x27200000) + offset (0x05A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	pclk_center_root_sel pclk_center_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
11:10	RW	0x0	hclk_center_root_sel hclk_center_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
9:8	RW	0x0	aclk_center_low_root_sel aclk_center_low_root clock mux. 2'b00: clk_cpll_div2_src 2'b01: clk_cpll_div4_src 2'b10: clk_cpll_div10_src 2'b11: xin_osc0_func
7:5	RW	0x3	aclk_center_root_sel aclk_center_root clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_spll_mux 3'b011: clk_aupll_mux 3'b100: clk_bpll_src
4:0	RO	0x00	reserved

CRU_CLKSEL_CON178

Address: Operational Base(0x27200000) + offset (0x05C8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	hclk_vepu1_root_sel hclk_vepu1_root clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func

CRU_CLKSEL_CON180

Address: Operational Base(0x27200000) + offset (0x05D0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:11	RW	0x2	clk_vepu1_core_sel clk_vepu1_core clock mux. 3'b000: clk_gpll_mux 3'b001: clk_cpll_mux 3'b010: clk_spll_mux 3'b011: clk_lpll_src 3'b100: clk_bpll_src
10:6	RW	0x00	clk_vepu1_core_div Divide clk_vepu1_core by (div_con + 1).
5	RW	0x0	aclk_vepu1_root_sel aclk_vepu1_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:0	RW	0x02	aclk_vepu1_root_div Divide aclk_vepu1_root by (div_con + 1).

CRU_GATE_CON00

Address: Operational Base(0x27200000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_spll_div1_src_en clk_spll_div1_src clock gating control. When high, disable clock
11	RO	0x0	reserved
10	RW	0x0	clk_gpll_div2_src_en clk_gpll_div2_src clock gating control. When high, disable clock
9	RW	0x0	clk_cpll_div2_src_en clk_cpll_div2_src clock gating control. When high, disable clock
8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	clk_gpll_div3_src_en clk_gpll_div3_src clock gating control. When high, disable clock
6	RW	0x0	clk_spll_div2_src_en clk_spll_div2_src clock gating control. When high, disable clock
5	RW	0x0	clk_gpll_div4_src_en clk_gpll_div4_src clock gating control. When high, disable clock
4	RW	0x0	clk_cpll_div4_src_en clk_cpll_div4_src clock gating control. When high, disable clock
3	RW	0x0	clk_gpll_div6_src_en clk_gpll_div6_src clock gating control. When high, disable clock
2	RW	0x0	clk_gpll_div8_src_en clk_gpll_div8_src clock gating control. When high, disable clock
1	RW	0x0	clk_cpll_div10_src_en clk_cpll_div10_src clock gating control. When high, disable clock
0	RW	0x0	clk_cpll_div20_src_en clk_cpll_div20_src clock gating control. When high, disable clock

CRU_GATE_CON01

Address: Operational Base(0x27200000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	hclk_top_biu_en hclk_top_biu clock gating control. When high, disable clock
13	RW	0x0	clk_matrix_audio_frac_3_en clk_matrix_audio_frac_3 clock gating control. When high, disable clock
12	RW	0x0	clk_matrix_audio_frac_2_en clk_matrix_audio_frac_2 clock gating control. When high, disable clock
11	RW	0x0	clk_matrix_audio_frac_1_en clk_matrix_audio_frac_1 clock gating control. When high, disable clock
10	RW	0x0	clk_matrix_audio_frac_0_en clk_matrix_audio_frac_0 clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	clk_bpll_src_en clk_bpll_src clock gating control. When high, disable clock
7	RW	0x0	aclk_secure_high_biu_en aclk_secure_high_biu clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	aclk_low_top_root_en aclk_top_mid_biu clock gating control. When high, disable clock
5	RW	0x0	pclk_top_biu_en pclk_top_biu clock gating control. When high, disable clock
4	RW	0x0	clk_lpll_src_en clk_lpll_src clock gating control. When high, disable clock
3	RW	0x0	aclk_top_biu_en aclk_top_biu clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	pclk_top_root_en pclk_top_root clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON02

Address: Operational Base(0x27200000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_matrix_audio_int_1_en clk_matrix_audio_int_1 clock gating control. When high, disable clock
14	RW	0x0	clk_matrix_audio_int_0_en clk_matrix_audio_int_0 clock gating control. When high, disable clock
13	RW	0x0	clk_uart1_src_top_en clk_uart1_src_top clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x1	clk_testout_grp0_en clk_testout_grp0 clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x1	clk_testout_en clk_testout clock gating control. When high, disable clock
8	RW	0x1	clk_testout_top_en clk_testout_top clock gating control. When high, disable clock
7	RW	0x0	clk_matrix_uart_frac_2_en clk_matrix_uart_frac_2 clock gating control. When high, disable clock
6	RW	0x0	clk_matrix_uart_frac_1_en clk_matrix_uart_frac_1 clock gating control. When high, disable clock
5	RW	0x0	clk_matrix_uart_frac_0_en clk_matrix_uart_frac_0 clock gating control. When high, disable clock
4:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	aclk_vo0vop_channel_biu_en aclk_vo0vop_channel_biu clock gating control. When high, disable clock
0	RW	0x0	hclk_vo0vop_channel_biu_en hclk_vo0vop_channel_biu clock gating control. When high, disable clock

CRU_GATE_CON03

Address: Operational Base(0x27200000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	lclk_asrc_src_1_en lclk_asrc_src_1 clock gating control. When high, disable clock
10	RW	0x0	lclk_asrc_src_0_en lclk_asrc_src_0 clock gating control. When high, disable clock
9:8	RO	0x0	reserved
7	RW	0x0	clk_matrix_gmac1_125m_src_en clk_matrix_gmac1_125m_src clock gating control. When high, disable clock
6	RW	0x0	clk_matrix_gmac0_125m_src_en clk_matrix_gmac0_125m_src clock gating control. When high, disable clock
5	RW	0x0	clk_pdm1_out_en clk_pdm1_out clock gating control. When high, disable clock
4:3	RO	0x0	reserved
2	RW	0x0	clk_pdm0_src_top_en clk_pdm0_src_top clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	clk_matrix_audio_int_2_en clk_matrix_audio_int_2 clock gating control. When high, disable clock

CRU_GATE_CON04

Address: Operational Base(0x27200000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	ref_clk2_out_pll_en ref_clk2_out_pll clock gating control. When high, disable clock
2	RW	0x0	ref_clk1_out_pll_en ref_clk1_out_pll clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	ref_clk0_out_pll_en ref_clk0_out_pll clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON05

Address: Operational Base(0x27200000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_otpc_auto_rd_en clk_otpc_auto_rd_g clock gating control. When high, disable clock
14	RW	0x0	clk_gmac1_rmii_cru_en clk_gmac1_rmii_cru clock gating control. When high, disable clock
13	RW	0x0	clk_gmac0_rmii_cru_en clk_gmac0_rmii_cru clock gating control. When high, disable clock
12	RW	0x0	clk_cifout_out_en clk_cifout_out clock gating control. When high, disable clock
11	RW	0x0	refclko25m_eth1_out_en refclko25m_gmac1_out clock gating control. When high, disable clock
10	RW	0x0	refclko25m_eth0_out_en refclko25m_gmac0_out clock gating control. When high, disable clock
9:0	RO	0x000	reserved

CRU_GATE_CON06

Address: Operational Base(0x27200000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	mclk_pdm0_src_top_en mclk_pdm0_src_top clock gating control. When high, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	clk_mipi_cameraout_m2_en clk_mipi_cameraout_m2 clock gating control. When high, disable clock
4	RW	0x0	clk_mipi_cameraout_m1_en clk_mipi_cameraout_m1 clock gating control. When high, disable clock
3	RW	0x0	clk_mipi_cameraout_m0_en clk_mipi_cameraout_m0 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	clk_bisrintf_en clk_bisrintf clock gating control. When high, disable clock
1	RW	0x0	clk_bisrintf_pllsrc_en clk_bisrintf_pllsrc clock gating control. When high, disable clock
0	RW	0x0	clk_otp_phy_en clk_otp_phy_g clock gating control. When high, disable clock

CRU_GATE_CON07

Address: Operational Base(0x27200000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mclk_spdif_rx0_en mclk_spdif_rx0 clock gating control. When high, disable clock
14	RW	0x0	hclk_spdif_rx0_en hclk_spdif_rx0 clock gating control. When high, disable clock
13	RW	0x0	hclk_sai0_en hclk_sai0 clock gating control. When high, disable clock
12	RW	0x0	mclk_sai0_en mclk_sai0 clock gating control. When high, disable clock
11	RW	0x0	mclk_sai0_src_en mclk_sai0_src clock gating control. When high, disable clock
10	RW	0x0	clk_asrc_4ch_1_en clk_asrc_4ch_1 clock gating control. When high, disable clock
9	RW	0x0	clk_asrc_4ch_0_en clk_asrc_4ch_0 clock gating control. When high, disable clock
8	RW	0x0	clk_asrc_2ch_1_en clk_asrc_2ch_1 clock gating control. When high, disable clock
7	RW	0x0	clk_asrc_2ch_0_en clk_asrc_2ch_0 clock gating control. When high, disable clock
6	RW	0x0	hclk_asrc_4ch_1_en hclk_asrc_4ch_1 clock gating control. When high, disable clock
5	RW	0x0	hclk_asrc_4ch_0_en hclk_asrc_4ch_0 clock gating control. When high, disable clock
4	RW	0x0	hclk_asrc_2ch_1_en hclk_asrc_2ch_1 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	hclk_asrc_2ch_0_en hclk_asrc_2ch_0 clock gating control. When high, disable clock
2	RW	0x0	hclk_audio_biu_en hclk_audio_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_audio_root_en hclk_audio_root clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON08

Address: Operational Base(0x27200000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mclk_sai4_src_en mclk_sai4_src clock gating control. When high, disable clock
14	RW	0x0	hclk_sai3_en hclk_sai3 clock gating control. When high, disable clock
13	RO	0x0	reserved
12	RW	0x0	mclk_sai3_en mclk_sai3 clock gating control. When high, disable clock
11	RW	0x0	mclk_sai3_src_en mclk_sai3_src clock gating control. When high, disable clock
10	RW	0x0	hclk_sai2_en hclk_sai2 clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	mclk_sai2_en mclk_sai2 clock gating control. When high, disable clock
7	RW	0x0	mclk_sai2_src_en mclk_sai2_src clock gating control. When high, disable clock
6	RW	0x0	hclk_sai1_en hclk_sai1 clock gating control. When high, disable clock
5	RW	0x0	mclk_sai1_en mclk_sai1 clock gating control. When high, disable clock
4	RW	0x0	mclk_sai1_src_en mclk_sai1_src clock gating control. When high, disable clock
3:2	RO	0x0	reserved
1	RW	0x0	mclk_spdif_rx1_en mclk_spdif_rx1 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
0	RW	0x0	hclk_spdif_rx1_en hclk_spdif_rx1 clock gating control. When high, disable clock

CRU_GATE_CON09

Address: Operational Base(0x27200000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_sai3_mclkout_en clk_sai3_mclkout clock gating control. When high, disable clock
14	RW	0x0	clk_sai2_mclkout_en clk_sai2_mclkout clock gating control. When high, disable clock
13	RW	0x0	clk_sai1_mclkout_en clk_sai1_mclkout clock gating control. When high, disable clock
12	RW	0x0	mclk_spdif_tx1_en mclk_spdif_tx1 clock gating control. When high, disable clock
11	RW	0x0	hclk_spdif_tx1_en hclk_spdif_tx1 clock gating control. When high, disable clock
10	RW	0x0	mclk_spdif_tx0_en mclk_spdif_tx0 clock gating control. When high, disable clock
9	RW	0x0	hclk_spdif_tx0_en hclk_spdif_tx0 clock gating control. When high, disable clock
8	RW	0x0	mclk_pdm1_en mclk_pdm1 clock gating control. When high, disable clock
7	RW	0x0	hclk_pdm1_en hclk_pdm1 clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	clk_pdm1_en clk_pdm1 clock gating control. When high, disable clock
4	RW	0x0	mclk_acdcdig_dsm_en mclk_acdcdig_dsm clock gating control. When high, disable clock
3	RW	0x0	hclk_acdcdig_dsm_en hclk_acdcdig_dsm clock gating control. When high, disable clock
2	RW	0x0	hclk_sai4_en hclk_sai4 clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	mclk_sai4_en mclk_sai4 clock gating control. When high, disable clock

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CRU_GATE_CON10

Address: Operational Base(0x27200000) + offset (0x0828)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	clk_sai0_mclkout_en clk_sai0_mclkout clock gating control. When high, disable clock
0	RW	0x0	clk_sai4_mclkout_en clk_sai4_mclkout clock gating control. When high, disable clock

CRU_GATE_CON11

Address: Operational Base(0x27200000) + offset (0x082C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_key_shift_en clk_key_shift clock gating control. When high, disable clock
14	RW	0x0	hclk_bus_biu_en hclk_bus_biu clock gating control. When high, disable clock
13	RW	0x0	pclk_vccio_ioc_en pclk_vccio_ioc clock gating control. When high, disable clock
12	RW	0x0	pclk_intmux2bus_en pclk_intmux2bus clock gating control. When high, disable clock
11:10	RO	0x0	reserved
9	RW	0x0	clk_can1_en clk_can1 clock gating control. When high, disable clock
8	RW	0x0	hclk_can1_en hclk_can1 clock gating control. When high, disable clock
7	RW	0x0	clk_can0_en clk_can0 clock gating control. When high, disable clock
6	RW	0x0	hclk_can0_en hclk_can0 clock gating control. When high, disable clock
5	RW	0x0	pclk_cru_en pclk_cru clock gating control. When high, disable clock
4	RW	0x0	pclk_bus_biu_en pclk_bus_biu clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	aclk_bus_biu_en aclk_bus_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_bus_root_en aclk_bus_root clock gating control. When high, disable clock
1	RW	0x0	pclk_bus_root_en pclk_bus_root clock gating control. When high, disable clock
0	RW	0x0	hclk_bus_root_en hclk_bus_root clock gating control. When high, disable clock

CRU_GATE_CON12

Address: Operational Base(0x27200000) + offset (0x0830)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_i2c4_en clk_i2c4 clock gating control. When high, disable clock
14	RW	0x0	clk_i2c3_en clk_i2c3 clock gating control. When high, disable clock
13	RW	0x0	clk_i2c2_en clk_i2c2 clock gating control. When high, disable clock
12	RW	0x0	clk_i2c1_en clk_i2c1 clock gating control. When high, disable clock
11	RW	0x0	aclk_gic_en aclk_gic clock gating control. When high, disable clock
10	RW	0x0	tclk_wdt_busmcu_en tclk_wdt_busmcu clock gating control. When high, disable clock
9	RW	0x0	pclk_wdt_busmcu_en pclk_wdt_busmcu clock gating control. When high, disable clock
8	RW	0x0	pclk_i2c9_en pclk_i2c9 clock gating control. When high, disable clock
7	RW	0x0	pclk_i2c8_en pclk_i2c8 clock gating control. When high, disable clock
6	RW	0x0	pclk_i2c7_en pclk_i2c7 clock gating control. When high, disable clock
5	RW	0x0	pclk_i2c6_en pclk_i2c6 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
4	RW	0x0	pclk_i2c5_en pclk_i2c5 clock gating control. When high, disable clock
3	RW	0x0	pclk_i2c4_en pclk_i2c4 clock gating control. When high, disable clock
2	RW	0x0	pclk_i2c3_en pclk_i2c3 clock gating control. When high, disable clock
1	RW	0x0	pclk_i2c2_en pclk_i2c2 clock gating control. When high, disable clock
0	RW	0x0	pclk_i2c1_en pclk_i2c1 clock gating control. When high, disable clock

CRU_GATE_CON13

Address: Operational Base(0x27200000) + offset (0x0834)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_uart6_en pclk_uart6 clock gating control. When high, disable clock
14	RW	0x0	pclk_uart5_en pclk_uart5 clock gating control. When high, disable clock
13	RW	0x0	pclk_uart4_en pclk_uart4 clock gating control. When high, disable clock
12	RW	0x0	pclk_uart3_en pclk_uart3 clock gating control. When high, disable clock
11	RW	0x0	pclk_uart2_en pclk_uart2 clock gating control. When high, disable clock
10	RW	0x0	pclk_uart0_en pclk_uart0 clock gating control. When high, disable clock
9	RW	0x0	clk_tsadc_en clk_tsadc clock gating control. When high, disable clock
8	RW	0x0	pclk_tsadc_en pclk_tsadc clock gating control. When high, disable clock
7	RW	0x0	clk_saradc_en clk_saradc clock gating control. When high, disable clock
6	RW	0x0	pclk_saradc_en pclk_saradc clock gating control. When high, disable clock
5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	clk_i2c9_en clk_i2c9 clock gating control. When high, disable clock
3	RW	0x0	clk_i2c8_en clk_i2c8 clock gating control. When high, disable clock
2	RW	0x0	clk_i2c7_en clk_i2c7 clock gating control. When high, disable clock
1	RW	0x0	clk_i2c6_en clk_i2c6 clock gating control. When high, disable clock
0	RW	0x0	clk_i2c5_en clk_i2c5 clock gating control. When high, disable clock

CRU_GATE_CON14

Address: Operational Base(0x27200000) + offset (0x0838)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sclk_uart5_en sclk_uart5 clock gating control. When high, disable clock
14:13	RO	0x0	reserved
12	RW	0x0	sclk_uart4_en sclk_uart4 clock gating control. When high, disable clock
11:10	RO	0x0	reserved
9	RW	0x0	sclk_uart3_en sclk_uart3 clock gating control. When high, disable clock
8:7	RO	0x0	reserved
6	RW	0x0	sclk_uart2_en sclk_uart2 clock gating control. When high, disable clock
5	RW	0x0	sclk_uart0_en sclk_uart0 clock gating control. When high, disable clock
4	RW	0x0	pclk_uart11_en pclk_uart11 clock gating control. When high, disable clock
3	RW	0x0	pclk_uart10_en pclk_uart10 clock gating control. When high, disable clock
2	RW	0x0	pclk_uart9_en pclk_uart9 clock gating control. When high, disable clock
1	RW	0x0	pclk_uart8_en pclk_uart8 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
0	RW	0x0	pclk_uart7_en pclk_uart7 clock gating control. When high, disable clock

CRU_GATE_CON15

Address: Operational Base(0x27200000) + offset (0x083C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_spi2_en pclk_spi2 clock gating control. When high, disable clock
14	RW	0x0	pclk_spi1_en pclk_spi1 clock gating control. When high, disable clock
13	RW	0x0	pclk_spi0_en pclk_spi0 clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x0	sclk_uart11_en sclk_uart11 clock gating control. When high, disable clock
10	RW	0x0	sclk_uart10_en sclk_uart10 clock gating control. When high, disable clock
9	RW	0x0	sclk_uart9_en sclk_uart9 clock gating control. When high, disable clock
8	RW	0x0	sclk_uart8_en sclk_uart8 clock gating control. When high, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	sclk_uart7_en sclk_uart7 clock gating control. When high, disable clock
4:3	RO	0x0	reserved
2	RW	0x0	sclk_uart6_en sclk_uart6 clock gating control. When high, disable clock
1:0	RO	0x0	reserved

CRU_GATE_CON16

Address: Operational Base(0x27200000) + offset (0x0840)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_rc_pwm1_en clk_rc_pwm1 clock gating control. When high, disable clock
14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	clk_osc_pwm1_en clk_osc_pwm1 clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x0	clk_pwm1_en clk_pwm1 clock gating control. When high, disable clock
10	RW	0x0	pclk_pwm1_en pclk_pwm1 clock gating control. When high, disable clock
9	RW	0x0	pclk_sys_grf_en pclk_sys_grf clock gating control. When high, disable clock
8	RW	0x0	tclk_wdtpmu_en tclk_wdtpmu clock gating control. When high, disable clock
7	RW	0x0	pclk_wdtpmu_en pclk_wdtpmu clock gating control. When high, disable clock
6	RW	0x0	clk_spi4_en clk_spi4 clock gating control. When high, disable clock
5	RW	0x0	clk_spi3_en clk_spi3 clock gating control. When high, disable clock
4	RW	0x0	clk_spi2_en clk_spi2 clock gating control. When high, disable clock
3	RW	0x0	clk_spi1_en clk_spi1 clock gating control. When high, disable clock
2	RW	0x0	clk_spi0_en clk_spi0 clock gating control. When high, disable clock
1	RW	0x0	pclk_spi4_en pclk_spi4 clock gating control. When high, disable clock
0	RW	0x0	pclk_spi3_en pclk_spi3 clock gating control. When high, disable clock

CRU_GATE_CON17

Address: Operational Base(0x27200000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_gpio1_en pclk_gpio1 clock gating control. When high, disable clock
14	RO	0x0	reserved
13	RW	0x0	pclk_mailbox0_en pclk_mailbox0 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
12	RW	0x0	pclk_busioc_en pclk_busioc clock gating control. When high, disable clock
11	RW	0x0	clk_timer5_en clk_timer5 clock gating control. When high, disable clock
10	RW	0x0	clk_timer4_en clk_timer4 clock gating control. When high, disable clock
9	RW	0x0	clk_timer3_en clk_timer3 clock gating control. When high, disable clock
8	RW	0x0	clk_timer2_en clk_timer2 clock gating control. When high, disable clock
7	RW	0x0	clk_timer1_en clk_timer1 clock gating control. When high, disable clock
6	RW	0x0	clk_timer0_en clk_timer0 clock gating control. When high, disable clock
5	RW	0x0	clk_timer0_root_en clk_timer0_root clock gating control. When high, disable clock
4	RW	0x0	pclk_bustimer1_en pclk_bustimer1 clock gating control. When high, disable clock
3	RW	0x0	pclk_bustimer0_en pclk_bustimer0 clock gating control. When high, disable clock
2:0	RO	0x0	reserved

CRU_GATE_CON18

Address: Operational Base(0x27200000) + offset (0x0848)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_timer10_en clk_timer10 clock gating control. When high, disable clock
14	RW	0x0	clk_timer9_en clk_timer9 clock gating control. When high, disable clock
13	RW	0x0	clk_timer8_en clk_timer8 clock gating control. When high, disable clock
12	RW	0x0	clk_timer7_en clk_timer7 clock gating control. When high, disable clock
11	RW	0x0	clk_timer6_en clk_timer6 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
10	RW	0x0	clk_timer1_root_en clk_timer1_root clock gating control. When high, disable clock
9	RW	0x0	dclk_decom_en dclk_decom clock gating control. When high, disable clock
8	RW	0x0	pclk_decom_en pclk_decom clock gating control. When high, disable clock
7	RW	0x0	aclk_decom_en aclk_decom clock gating control. When high, disable clock
6	RW	0x0	dbclk_gpio4_en dbclk_gpio4 clock gating control. When high, disable clock
5	RW	0x0	pclk_gpio4_en pclk_gpio4 clock gating control. When high, disable clock
4	RW	0x0	dbclk_gpio3_en dbclk_gpio3 clock gating control. When high, disable clock
3	RW	0x0	pclk_gpio3_en pclk_gpio3 clock gating control. When high, disable clock
2	RW	0x0	dbclk_gpio2_en dbclk_gpio2 clock gating control. When high, disable clock
1	RW	0x0	pclk_gpio2_en pclk_gpio2 clock gating control. When high, disable clock
0	RW	0x0	dbclk_gpio1_en dbclk_gpio1 clock gating control. When high, disable clock

CRU_GATE_CON19

Address: Operational Base(0x27200000) + offset (0x084C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_pmu2_en pclk_pmu2 clock gating control. When high, disable clock
14	RW	0x0	clk_bus_cm0_rtc_en clk_bus_cm0_rtc clock gating control. When high, disable clock
13	RO	0x0	reserved
12	RW	0x0	fclk_bus_cm0_core_en fclk_bus_cm0_core clock gating control. When high, disable clock
11	RW	0x0	hclk_bus_cm0_biu_en hclk_bus_cm0_biu clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
10	RW	0x0	hclk_bus_cm0_root_en hclk_bus_cm0_root clock gating control. When high, disable clock
9	RW	0x0	hclk_i3c1_en hclk_i3c1 clock gating control. When high, disable clock
8	RO	0x0	reserved
7	RW	0x0	hclk_i3c0_en hclk_i3c0 clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	clk_ref_pvtpll_bus_en clk_ref_pvtpll_bus clock gating control. When high, disable clock
4	RW	0x0	aclk_spinlock_en aclk_spinlock clock gating control. When high, disable clock
3	RW	0x0	aclk_dmac2_en aclk_dmac2 clock gating control. When high, disable clock
2	RW	0x0	aclk_dmac1_en aclk_dmac1 clock gating control. When high, disable clock
1	RW	0x0	aclk_dmac0_en aclk_dmac0 clock gating control. When high, disable clock
0	RW	0x0	clk_timer11_en clk_timer11 clock gating control. When high, disable clock

CRU_GATE_CON20

Address: Operational Base(0x27200000) + offset (0x0850)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_i3c1_en clk_i3c1 clock gating control. When high, disable clock
12	RW	0x0	clk_i3c0_en clk_i3c0 clock gating control. When high, disable clock
11	RW	0x0	sai_sclkin_counter_en sai_sclkin_counter clock gating control. When high, disable clock
10	RW	0x0	sai_sclkin_freq_en sai_sclkin_freq clock gating control. When high, disable clock
9	RW	0x0	clk_counter_pwm1_en clk_counter_pwm1 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
8	RW	0x0	clk_freq_pwm1_en clk_freq_pwm1 clock gating control. When high, disable clock
7	RW	0x0	clk_osc_pwm2_en clk_osc_pwm2 clock gating control. When high, disable clock
6	RW	0x0	clk_rc_pwm2_en clk_rc_pwm2 clock gating control. When high, disable clock
5	RW	0x0	clk_pwm2_en clk_pwm2 clock gating control. When high, disable clock
4	RW	0x0	pclk_pwm2_en pclk_pwm2 clock gating control. When high, disable clock
3	RW	0x0	pclk_pvtpll_bus_en pclk_pvtpll_bus clock gating control. When high, disable clock
2	RW	0x0	clk_extref_timeout_bus_en clk_extref_timeout_bus clock gating control. When high, disable clock
1	RW	0x0	pclk_intmux2ddr_en pclk_intmux2ddr clock gating control. When high, disable clock
0	RW	0x0	pclk_intmux2pmu_en pclk_intmux2pmu clock gating control. When high, disable clock

CRU_GATE_CON21

Address: Operational Base(0x27200000) + offset (0x0854)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_ddr_hwlp_ch1_en pclk_ddr_hwlp_ch1 clock gating control. When high, disable clock
14	RW	0x0	pclk_ddr_mon_ch1_en pclk_ddr_mon_ch1 clock gating control. When high, disable clock
13	RW	0x0	pclk_ddr_hwlp_ch0_en pclk_ddr_hwlp_ch0 clock gating control. When high, disable clock
12:11	RO	0x0	reserved
10	RW	0x0	clk_ddr_mon_ch0_en clk_ddr_mon_ch0 clock gating control. When high, disable clock
9	RW	0x0	aclk_ddr_root_en aclk_ddr_root clock gating control. When high, disable clock
8:7	RO	0x0	reserved
6	RW	0x0	clk_dfi_ch0_en clk_dfi_ch0 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
5	RW	0x0	aclk_ddr_biu_en aclk_ddr_biu clock gating control. When high, disable clock
4	RW	0x0	tmclk_ddr_mon_ch0_en tmclk_ddr_mon_ch0 clock gating control. When high, disable clock
3	RW	0x0	pclk_ddr_upctl_ch0_en pclk_ddr_upctl_ch0 clock gating control. When high, disable clock
2	RW	0x0	pclk_ddr_biu_en pclk_ddr_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_ddr_mon_ch0_en pclk_ddr_mon_ch0 clock gating control. When high, disable clock
0	RW	0x0	pclk_ddr_root_en pclk_ddr_root clock gating control. When high, disable clock

CRU_GATE_CON22

Address: Operational Base(0x27200000) + offset (0x0858)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	fclk_ddr_cm0_core_en fclk_ddr_cm0_core clock gating control. When high, disable clock
14	RW	0x0	hclk_ddr_biu_en hclk_ddr_biu clock gating control. When high, disable clock
13	RW	0x0	hclk_ahb2apb_en hclk_ahb2apb clock gating control. When high, disable clock
12	RW	0x0	pclk_ahb2apb_en pclk_ahb2apb clock gating control. When high, disable clock
11	RW	0x0	hclk_ddr_root_en hclk_ddr_root clock gating control. When high, disable clock
10	RW	0x0	clk_ddr_scramble_ch1_en clk_ddr_scramble_ch1 clock gating control. When high, disable clock
9	RW	0x0	clk_ddr_scramble_ch0_en clk_ddr_scramble_ch0 clock gating control. When high, disable clock
8	RW	0x0	pclk_ddrphy_src_ch1_en pclk_ddrphy_src_ch1 clock gating control. When high, disable clock
7	RW	0x0	pclk_ddrphy_src_ch0_en pclk_ddrphy_src_ch0 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
6	RW	0x0	clk_ddr_mon_ch1_en clk_ddr_mon_ch1 clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	aclk_ddr01_msch1_en aclk_ddr01_msch1 clock gating control. When high, disable clock
3	RW	0x0	aclk_ddr01_msch0_en aclk_ddr01_msch0 clock gating control. When high, disable clock
2	RW	0x0	clk_dfi_ch1_en clk_dfi_ch1 clock gating control. When high, disable clock
1	RW	0x0	tmclk_ddr_mon_ch1_en tmclk_ddr_mon_ch1 clock gating control. When high, disable clock
0	RW	0x0	pclk_ddr_upctl_ch1_en pclk_ddr_upctl_ch1 clock gating control. When high, disable clock

CRU_GATE_CON23

Address: Operational Base(0x27200000) + offset (0x085C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	pclk_ddr_grf_en pclk_ddr_grf clock gating control. When high, disable clock
10	RW	0x0	clk_ddr_cm0_rtc_en clk_ddr_cm0_rtc clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	pclk_timer_en pclk_timer clock gating control. When high, disable clock
7	RW	0x0	pclk_wdt_ddr_en pclk_wdt_ddr clock gating control. When high, disable clock
6	RW	0x0	tclk_wdt_ddr_en tclk_wdt_ddr clock gating control. When high, disable clock
5	RW	0x0	clk_ddr_timer1_en clk_ddr_timer1 clock gating control. When high, disable clock
4	RW	0x0	clk_ddr_timer0_en clk_ddr_timer0 clock gating control. When high, disable clock
3	RW	0x0	clk_ddr_timer_root_en clk_ddr_timer_root clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	pclk_ddr01_msch1_en pclk_ddr01_msch1 clock gating control. When high, disable clock
1	RW	0x0	pclk_ddr01_msch0_en pclk_ddr01_msch0 clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON25

Address: Operational Base(0x27200000) + offset (0x0864)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	aclk_ddr_upctl_4_ch0_en aclk_ddr_upctl_4_ch0 clock gating control. When high, disable clock
5	RW	0x0	aclk_ddr_upctl_3_ch0_en aclk_ddr_upctl_3_ch0 clock gating control. When high, disable clock
4	RW	0x0	aclk_ddr_upctl_2_ch0_en aclk_ddr_upctl_2_ch0 clock gating control. When high, disable clock
3	RW	0x0	aclk_ddr_upctl_1_ch0_en aclk_ddr_upctl_1_ch0 clock gating control. When high, disable clock
2	RW	0x0	aclk_ddr_upctl_0_ch0_en aclk_ddr_upctl_0_ch0 clock gating control. When high, disable clock
1	RW	0x0	clk_ddr_upctl_ch0_en clk_ddr_upctl_ch0 clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON26

Address: Operational Base(0x27200000) + offset (0x0868)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	aclk_ddr_upctl_4_ch1_en aclk_ddr_upctl_4_ch1 clock gating control. When high, disable clock
5	RW	0x0	aclk_ddr_upctl_3_ch1_en aclk_ddr_upctl_3_ch1 clock gating control. When high, disable clock
4	RW	0x0	aclk_ddr_upctl_2_ch1_en aclk_ddr_upctl_2_ch1 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
3	RW	0x0	aclk_ddr_upctl_1_ch1_en aclk_ddr_upctl_1_ch1 clock gating control. When high, disable clock
2	RW	0x0	aclk_ddr_upctl_0_ch1_en aclk_ddr_upctl_0_ch1 clock gating control. When high, disable clock
1	RW	0x0	clk_ddr_upctl_ch1_en clk_ddr_upctl_ch1 clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON27

Address: Operational Base(0x27200000) + offset (0x086C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	pclk_pvtpll_ddr_en pclk_pvtpll_ddr clock gating control. When high, disable clock
0	RW	0x0	clk_ref_pvtpll_ddr_en clk_ref_pvtpll_ddr clock gating control. When high, disable clock

CRU_GATE_CON28

Address: Operational Base(0x27200000) + offset (0x0870)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	lclk_rknn0_biu_en lclk_rknn0_biu clock gating control. When high, disable clock
11	RW	0x0	aclk_rknn0_biu_en aclk_rknn0_biu clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	aclk_rknn0_en aclk_rknn0 clock gating control. When high, disable clock
8:0	RO	0x000	reserved

CRU_GATE_CON29

Address: Operational Base(0x27200000) + offset (0x0874)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	lclk_rknn1_biu_en lclk_rknn1_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_rknn1_biu_en aclk_rknn1_biu clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	aclk_rknn1_en aclk_rknn1 clock gating control. When high, disable clock

CRU_GATE_CON31

Address: Operational Base(0x27200000) + offset (0x087C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	tclk_npu_wdt_en tclk_npu_wdt clock gating control. When high, disable clock
14	RW	0x0	pclk_npu_wdt_en pclk_npu_wdt clock gating control. When high, disable clock
13	RW	0x0	clk_nputimer1_en clk_nputimer1 clock gating control. When high, disable clock
12	RW	0x0	clk_nputimer0_en clk_nputimer0 clock gating control. When high, disable clock
11	RW	0x0	clk_nputimer_root_en clk_nputimer_root clock gating control. When high, disable clock
10	RW	0x0	pclk_npu_timer_en pclk_npu_timer clock gating control. When high, disable clock
9	RW	0x0	pclk_nputop_biu_en pclk_nputop_biu clock gating control. When high, disable clock
8	RW	0x0	pclk_nputop_root_en pclk_nputop_root clock gating control. When high, disable clock
7	RW	0x0	clk_rknn_dsu0_en clk_rknn_dsu0 clock gating control. When high, disable clock
6	RW	0x0	clk_npu_pvtpll_src_en clk_npu_pvtpll_src clock gating control. When high, disable clock
5	RW	0x0	clk_rknn_dsu0_df_en clk_rknn_dsu0_src_t clock gating control. When high, disable clock
4	RW	0x0	hclk_rknn_root_en hclk_rknn_root clock gating control. When high, disable clock
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	lclk_npusubsys_biu_en lclk_npusubsys_biu clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON32

Address: Operational Base(0x27200000) + offset (0x0880)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	hclk_rknntop_biu_en hclk_rknntop_biu clock gating control. When high, disable clock
12	RW	0x0	hclk_rknn_cbuf_en hclk_rknn_cbuf clock gating control. When high, disable clock
11	RW	0x0	aclk_rknntop_biu_en aclk_rknntop_biu clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	clk_npu_cm0_rtc_en clk_npu_cm0_rtc clock gating control. When high, disable clock
8	RO	0x0	reserved
7	RW	0x0	fclk_npu_cm0_core_en fclk_npu_cm0_core clock gating control. When high, disable clock
6	RW	0x0	hclk_npu_cm0_biu_en hclk_npu_cm0_biu clock gating control. When high, disable clock
5	RW	0x0	hclk_npu_cm0_root_en hclk_npu_cm0_root clock gating control. When high, disable clock
4	RW	0x0	clk_ref_pvtpll_npu_en clk_ref_pvtpll_npu clock gating control. When high, disable clock
3	RW	0x0	pclk_pvtpll_npu_en pclk_pvtpll_npu clock gating control. When high, disable clock
2	RW	0x0	pclk_npu_grf_en pclk_npu_grf clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	aclk_rknn_cbuf_en aclk_rknn_cbuf clock gating control. When high, disable clock

CRU_GATE_CON33

Address: Operational Base(0x27200000) + offset (0x0884)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_extref_timeout_nvm_en clk_extref_timeout_nvm clock gating control. When high, disable clock
12	RW	0x0	tclk_emmc_en tclk_emmc clock gating control. When high, disable clock
11	RW	0x0	bclk_emmc_en bclk_emmc clock gating control. When high, disable clock
10	RW	0x0	aclk_emmc_en aclk_emmc clock gating control. When high, disable clock
9	RW	0x0	hclk_emmc_en hclk_emmc clock gating control. When high, disable clock
8	RW	0x0	cclk_src_emmc_en cclk_src_emmc clock gating control. When high, disable clock
7	RW	0x0	hclk_fspi_en hclk_fspi clock gating control. When high, disable clock
6	RW	0x0	sclk_fspi_x2_en sclk_fspi_x2 clock gating control. When high, disable clock
5:4	RO	0x0	reserved
3	RW	0x0	aclk_nvm_biu_en aclk_nvm_biu clock gating control. When high, disable clock
2	RW	0x0	hclk_nvm_biu_en hclk_nvm_biu clock gating control. When high, disable clock
1	RW	0x0	aclk_nvm_root_en aclk_nvm_root clock gating control. When high, disable clock
0	RW	0x0	hclk_nvm_root_en hclk_nvm_root clock gating control. When high, disable clock

CRU_GATE_CON34

Address: Operational Base(0x27200000) + offset (0x0888)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	aclk_pcie0_mst_en aclk_pcie0_mst clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
14	RW	0x0	clk_pcie0_aux_en clk_pcie0_aux clock gating control. When high, disable clock
13	RW	0x0	pclk_pcie0_en pclk_pcie0 clock gating control. When high, disable clock
12:10	RO	0x0	reserved
9	RW	0x0	aclk_php_biu_en aclk_php_biu clock gating control. When high, disable clock
8	RO	0x0	reserved
7	RW	0x0	aclk_php_root_en aclk_php_root clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	pclk_php_biu_en pclk_php_biu clock gating control. When high, disable clock
4:2	RO	0x0	reserved
1	RW	0x0	pclk_grf_en pclk_grf clock gating control. When high, disable clock
0	RW	0x0	pclk_php_root_en pclk_php_root clock gating control. When high, disable clock

CRU_GATE_CON35

Address: Operational Base(0x27200000) + offset (0x088C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	aclk_mmu1_en aclk_mmu1 clock gating control. When high, disable clock
13	RW	0x0	aclk_slv_mmu0_en aclk_slv_mmu0 clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x0	aclk_mmu0_en aclk_mmu0 clock gating control. When high, disable clock
10:6	RO	0x00	reserved
5	RW	0x0	clk_suspend_usb3otg1_en clk_suspend_usb3otg1 clock gating control. When high, disable clock
4	RW	0x0	clk_ref_usb3otg1_en clk_ref_usb3otg1 clock gating control. When high, disable clock
3	RW	0x0	aclk_usb3otg1_en aclk_usb3otg1 clock gating control. When high, disable clock
2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	aclk_pcie0_dbi_en aclk_pcie0_dbi clock gating control. When high, disable clock
0	RW	0x0	aclk_pcie0_slv_en aclk_pcie0_slv clock gating control. When high, disable clock

CRU_GATE_CON36

Address: Operational Base(0x27200000) + offset (0x0890)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	aclk_pcie1_dbi_en aclk_pcie1_dbi clock gating control. When high, disable clock
10	RW	0x0	aclk_pcie1_slv_en aclk_pcie1_slv clock gating control. When high, disable clock
9	RW	0x0	aclk_pcie1_mst_en aclk_pcie1_mst clock gating control. When high, disable clock
8	RW	0x0	clk_pcie1_aux_en clk_pcie1_aux clock gating control. When high, disable clock
7	RW	0x0	pclk_pcie1_en pclk_pcie1 clock gating control. When high, disable clock
6:3	RO	0x0	reserved
2	RW	0x0	clk_extref_timeout_php_en clk_extref_timeout_php clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	aclk_slv_mmu1_en aclk_slv_mmu1 clock gating control. When high, disable clock

CRU_GATE_CON37

Address: Operational Base(0x27200000) + offset (0x0894)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	clk_asic0_en clk_asic0 clock gating control. When high, disable clock
6	RW	0x0	clk_asic1_en clk_asic1 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
5	RW	0x0	aclk_sata1_en aclk_sata1 clock gating control. When high, disable clock
4	RW	0x0	aclk_sata0_en aclk_sata0 clock gating control. When high, disable clock
3	RW	0x0	clk_pmalive1_en clk_pmalive1 clock gating control. When high, disable clock
2	RW	0x0	clk_pmalive0_en clk_pmalive0 clock gating control. When high, disable clock
1	RW	0x0	clk_rxoob1_en clk_rxoob1 clock gating control. When high, disable clock
0	RW	0x0	clk_rxoob0_en clk_rxoob0 clock gating control. When high, disable clock

CRU_GATE_CON38

Address: Operational Base(0x27200000) + offset (0x0898)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	clk_usb3otg1_utmi_en clk_usb3otg1_utmi clock gating control. When high, disable clock
0	RW	0x0	clk_usb3otg1_pipe_pclk_en clk_usb3otg1_pipe_pclk clock gating control. When high, disable clock

CRU_GATE_CON39

Address: Operational Base(0x27200000) + offset (0x089C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	clk_usb3otg0_utmi_en clk_usb3otg0_utmi clock gating control. When high, disable clock
0	RW	0x0	clk_usb3otg0_pipe_pclk_en clk_usb3otg0_pipe_pclk clock gating control. When high, disable clock

CRU_GATE_CON40

Address: Operational Base(0x27200000) + offset (0x08A0)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	pclk_csidphy1_en pclk_csidphy1 clock gating control. When high, disable clock Note: pclk_csidphy1_apb2asb and pclk_csidphy1_grf use same clk.
1:0	RO	0x0	reserved

CRU_GATE_CON42

Address: Operational Base(0x27200000) + offset (0x08A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_gmac1_ptp_ref_src_en clk_gmac1_ptp_ref_src clock gating control. When high, disable clock
14	RW	0x0	clk_gmac0_ptp_ref_en clk_gmac0_ptp_ref clock gating control. When high, disable clock
13	RW	0x0	clk_gmac1_ptp_ref_en clk_gmac1_ptp_ref clock gating control. When high, disable clock
12	RW	0x0	hclk_sdio_en hclk_sdio clock gating control. When high, disable clock
11	RW	0x0	cclk_src_sdio_en cclk_src_sdio clock gating control. When high, disable clock
10	RW	0x0	pclk_gmac1_en pclk_gmac1 clock gating control. When high, disable clock
9	RW	0x0	pclk_gmac0_en pclk_gmac0 clock gating control. When high, disable clock
8	RW	0x0	aclk_gmac1_en aclk_gmac1 clock gating control. When high, disable clock
7	RW	0x0	aclk_gmac0_en aclk_gmac0 clock gating control. When high, disable clock
6	RW	0x0	hclk_sdgmac_biu_en hclk_sdgmac_biu clock gating control. When high, disable clock
5	RW	0x0	aclk_sdgmac_biu_en aclk_sdgmac_biu clock gating control. When high, disable clock
4	RW	0x0	pclk_sdgmac_biu_en pclk_sdgmac_biu clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	pclk_sdgmac_grf_en pclk_sdgmac_grf clock gating control. When high, disable clock
2	RW	0x0	pclk_sdgmac_root_en pclk_sdgmac_root clock gating control. When high, disable clock
1	RW	0x0	aclk_sdgmac_root_en aclk_sdgmac_root clock gating control. When high, disable clock
0	RW	0x0	hclk_sdgmac_root_en hclk_sdgmac_root clock gating control. When high, disable clock

CRU_GATE_CON43

Address: Operational Base(0x27200000) + offset (0x08AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_extref_timeout_sdgmac_en clk_extref_timeout_sdgmac clock gating control. When high, disable clock
13	RW	0x0	aclk_flexbus_en aclk_flexbus clock gating control. When high, disable clock
12	RW	0x0	clk_flexbus_rx_en clk_flexbus_rx clock gating control. When high, disable clock
11	RW	0x0	clk_flexbus_tx_en clk_flexbus_tx clock gating control. When high, disable clock
10	RW	0x0	hclk_flexbus_en hclk_flexbus clock gating control. When high, disable clock
9	RW	0x0	clk_dsmc_sys_en clk_dsmc_sys clock gating control. When high, disable clock
8	RW	0x0	pclk_dsmc_en pclk_dsmc clock gating control. When high, disable clock
7	RW	0x0	aclk_dsmc_en aclk_dsmc clock gating control. When high, disable clock
6	RW	0x0	aclk_dsmc_biu_en aclk_dsmc_biu clock gating control. When high, disable clock
5	RW	0x0	aclk_dsmc_root_en aclk_dsmc_root clock gating control. When high, disable clock
4	RW	0x0	hclk_fspi1_en hclk_fspi1 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
3	RW	0x0	sclk_fspi1_x2_en sclk_fspi1_x2 clock gating control. When high, disable clock
2	RW	0x0	hclk_sdmmc0_en hclk_sdmmc0 clock gating control. When high, disable clock
1	RW	0x0	cclk_src_sdmmc0_en cclk_src_sdmmc0 clock gating control. When high, disable clock
0	RW	0x0	clk_gmac0_ptp_ref_src_en clk_gmac0_ptp_ref_src clock gating control. When high, disable clock

CRU_GATE_CON45

Address: Operational Base(0x27200000) + offset (0x08B4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	clk_rkvdec_core_en clk_rkvdec_core clock gating control. When high, disable clock
8	RW	0x0	clk_rkvdec_hevc_ca_en clk_rkvdec_hevc_ca clock gating control. When high, disable clock
7	RW	0x0	aclk_rkvdec_root_en aclk_rkvdec_root clock gating control. When high, disable clock
6	RW	0x0	aclk_rkvdec_biu_en aclk_rkvdec_biu clock gating control. When high, disable clock
5	RW	0x0	hclk_rkvdec_biu_en hclk_rkvdec_biu clock gating control. When high, disable clock
4	RO	0x0	reserved
3	RW	0x0	hclk_rkvdec_en hclk_rkvdec clock gating control. When high, disable clock
2	RW	0x0	aclk_rkvdec_root_bak_en aclk_rkvdec_root_bak clock gating control. When high, disable clock
1	RW	0x0	aclk_rkvdec_root_pre_en aclk_rkvdec_root_pre clock gating control. When high, disable clock
0	RW	0x0	hclk_rkvdec_root_en hclk_rkvdec_root clock gating control. When high, disable clock

CRU_GATE_CON47

Address: Operational Base(0x27200000) + offset (0x08BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	aclk_ufs_sys_en aclk_ufs_sys clock gating control. When high, disable clock
14	RO	0x0	reserved
13	RW	0x0	aclk_slv_mmu2_en aclk_slv_mmu2 clock gating control. When high, disable clock
12	RW	0x0	aclk_mmu2_en aclk_mmu2 clock gating control. When high, disable clock
11	RO	0x0	reserved
10	RW	0x0	aclk_ufs_biu_en aclk_ufs_biu clock gating control. When high, disable clock
9:8	RO	0x0	reserved
7	RW	0x0	clk_suspend_usb3otg0_en clk_suspend_usb3otg0 clock gating control. When high, disable clock
6	RW	0x0	clk_ref_usb3otg0_en clk_ref_usb3otg0 clock gating control. When high, disable clock
5	RW	0x0	aclk_usb3otg0_en aclk_usb3otg0 clock gating control. When high, disable clock
4	RW	0x0	pclk_usbufs_biu_en pclk_usbufs_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_usb_biu_en aclk_usb_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_usb_root_en pclk_usb_root clock gating control. When high, disable clock
1	RW	0x0	aclk_usb_root_en aclk_usb_root clock gating control. When high, disable clock
0	RW	0x0	aclk_ufs_root_en aclk_ufs_root clock gating control. When high, disable clock

CRU_GATE_CON48

Address: Operational Base(0x27200000) + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	clk_extref_timeout_usb_en clk_extref_timeout_usb clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
2	RW	0x0	pclk_ufs_grf_en pclk_ufs_grf clock gating control. When high, disable clock
1	RW	0x0	pclk_usbufs_grf_en pclk_usbufs_grf clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON49

Address: Operational Base(0x27200000) + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_core_rga2e_0_en clk_core_rga2e_0 clock gating control. When high, disable clock
14	RW	0x0	aclk_rga2e_0_en aclk_rga2e_0 clock gating control. When high, disable clock
13	RW	0x0	hclk_rga2e_0_en hclk_rga2e_0 clock gating control. When high, disable clock
12	RW	0x0	aclk_ebc_biu_en aclk_ebc_biu clock gating control. When high, disable clock
11	RW	0x0	aclk_vdpp_biu_en aclk_vdpp_biu clock gating control. When high, disable clock
10	RW	0x0	aclk_rga_biu_en aclk_rga_biu clock gating control. When high, disable clock
9:8	RO	0x0	reserved
7	RW	0x0	aclk_jpeg_biu_en aclk_jpeg_biu clock gating control. When high, disable clock
6	RW	0x0	hclk_vpu_biu_en hclk_vpu_biu clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	aclk_vpu_low_root_en aclk_vpu_low_root clock gating control. When high, disable clock
3	RW	0x0	aclk_jpeg_root_en aclk_jpeg_root clock gating control. When high, disable clock
2	RW	0x0	hclk_vpu_root_en hclk_vpu_root clock gating control. When high, disable clock
1	RW	0x0	aclk_vpu_mid_root_en aclk_vpu_mid_root clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
0	RW	0x0	aclk_vpu_root_en aclk_vpu_root clock gating control. When high, disable clock

CRU_GATE_CON50

Address: Operational Base(0x27200000) + offset (0x08C8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	dclk_ebc_en dclk_ebc clock gating control. When high, disable clock
11	RW	0x0	aclk_ebc_en aclk_ebc clock gating control. When high, disable clock
10	RW	0x0	hclk_ebc_en hclk_ebc clock gating control. When high, disable clock
9	RW	0x0	dclk_ebc_frac_src_en dclk_ebc_frac_src clock gating control. When high, disable clock
8	RO	0x0	reserved
7	RW	0x0	clk_core_rga2e_1_en clk_core_rga2e_1 clock gating control. When high, disable clock
6	RW	0x0	aclk_rga2e_1_en aclk_rga2e_1 clock gating control. When high, disable clock
5	RW	0x0	hclk_rga2e_1_en hclk_rga2e_1 clock gating control. When high, disable clock
4	RW	0x0	clk_core_vdpp_en clk_core_vdpp clock gating control. When high, disable clock
3	RW	0x0	aclk_vdpp_en aclk_vdpp clock gating control. When high, disable clock
2	RW	0x0	hclk_vdpp_en hclk_vdpp clock gating control. When high, disable clock
1	RW	0x0	hclk_jpeg_en hclk_jpeg clock gating control. When high, disable clock
0	RW	0x0	aclk_jpeg_en aclk_jpeg clock gating control. When high, disable clock

CRU_GATE_CON51

Address: Operational Base(0x27200000) + offset (0x08CC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	clk_vepu0_core_en clk_vepu0_core clock gating control. When high, disable clock
5	RW	0x0	aclk_vepu0_en aclk_vepu0 clock gating control. When high, disable clock
4	RW	0x0	hclk_vepu0_en hclk_vepu0 clock gating control. When high, disable clock
3	RW	0x0	aclk_vepu0_biu_en aclk_vepu0_biu clock gating control. When high, disable clock
2	RW	0x0	hclk_vepu0_biu_en hclk_vepu0_biu clock gating control. When high, disable clock
1	RW	0x0	aclk_vepu0_root_en aclk_vepu0_root clock gating control. When high, disable clock
0	RW	0x0	hclk_vepu0_root_en hclk_vepu0_root clock gating control. When high, disable clock

CRU_GATE_CON53

Address: Operational Base(0x27200000) + offset (0x08D4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	aclk_vpss_en aclk_vpss clock gating control. When high, disable clock
14	RO	0x0	reserved
13	RW	0x0	hclk_isp0_en hclk_isp0 clock gating control. When high, disable clock
12	RW	0x0	aclk_isp0_en aclk_isp0 clock gating control. When high, disable clock
11	RW	0x0	clk_isp0_core_vicap_en clk_isp0_core_vicap clock gating control. When high, disable clock
10	RW	0x0	clk_isp0_core_marvin_en clk_isp0_core_marvin clock gating control. When high, disable clock
9	RW	0x0	clk_isp0_core_en clk_isp0_core clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
8	RW	0x0	hclk_vicap_en hclk_vicap clock gating control. When high, disable clock
7	RW	0x0	aclk_vicap_en aclk_vicap clock gating control. When high, disable clock
6	RW	0x0	dclk_vicap_en dclk_vicap clock gating control. When high, disable clock
5	RW	0x0	pclk_vi_biu_en pclk_vi_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_vi_biu_en hclk_vi_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_vi_biu_en aclk_vi_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_vi_root_en pclk_vi_root clock gating control. When high, disable clock
1	RW	0x0	hclk_vi_root_en hclk_vi_root clock gating control. When high, disable clock
0	RW	0x0	aclk_vi_root_en aclk_vi_root clock gating control. When high, disable clock

CRU_GATE_CON54

Address: Operational Base(0x27200000) + offset (0x08D8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	aclk_vi_root_inter_en aclk_vi_root_inter clock gating control. When high, disable clock
12	RW	0x0	clk_isp_pvtpll_src_en clk_isp_pvtpll_src clock gating control. When high, disable clock
11	RW	0x0	iclk_csihost0_en iclk_csihost0 clock gating control. When high, disable clock
10	RW	0x0	iclk_csihost01_en iclk_csihost01 clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	pclk_csi_host_4_en pclk_csi_host_4 clock gating control. When high, disable clock
7	RW	0x0	pclk_csi_host_3_en pclk_csi_host_3 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	pclk_csi_host_2_en pclk_csi_host_2 clock gating control. When high, disable clock
5	RW	0x0	pclk_csi_host_1_en pclk_csi_host_1 clock gating control. When high, disable clock
4	RW	0x0	pclk_csi_host_0_en pclk_csi_host_0 clock gating control. When high, disable clock
3:2	RO	0x0	reserved
1	RW	0x0	clk_core_vpss_en clk_core_vpss clock gating control. When high, disable clock
0	RW	0x0	hclk_vpss_en hclk_vpss clock gating control. When high, disable clock

CRU_GATE_CON59

Address: Operational Base(0x27200000) + offset (0x08EC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_vicap_i4clk_en clk_vicap_i4clk clock gating control. When high, disable clock
4	RW	0x0	clk_vicap_i3clk_en clk_vicap_i3clk clock gating control. When high, disable clock
3	RW	0x0	clk_vicap_i2clk_en clk_vicap_i2clk clock gating control. When high, disable clock
2	RW	0x0	clk_vicap_i1clk_en clk_vicap_i1clk clock gating control. When high, disable clock
1	RW	0x0	clk_vicap_i0clk_en clk_vicap_i0clk clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON61

Address: Operational Base(0x27200000) + offset (0x08F4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	dclk_vp0_en dclk_vp0 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
12	RW	0x0	dclk_vp2_src_en dclk_vp2_src clock gating control. When high, disable clock
11	RW	0x0	dclk_vp1_src_en dclk_vp1_src clock gating control. When high, disable clock
10	RW	0x0	dclk_vp0_src_en dclk_vp0_src clock gating control. When high, disable clock
9	RW	0x0	aclk_vop_en aclk_vop clock gating control. When high, disable clock
8	RW	0x0	hclk_vop_en hclk_vop clock gating control. When high, disable clock
7	RW	0x0	pclk_vop_biu_en pclk_vop_biu clock gating control. When high, disable clock
6	RW	0x0	hclk_vop_biu_en hclk_vop_biu clock gating control. When high, disable clock
5	RW	0x0	aclk_vop2_biu_en aclk_vop2_biu clock gating control. When high, disable clock
4	RW	0x0	aclk_vop_biu_en aclk_vop_biu clock gating control. When high, disable clock
3	RW	0x0	pclk_vop_root_en pclk_vop_root clock gating control. When high, disable clock
2	RW	0x0	hclk_vop_root_en hclk_vop_root clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	aclk_vop_root_en aclk_vop_root clock gating control. When high, disable clock

CRU_GATE_CON62

Address: Operational Base(0x27200000) + offset (0x08F8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	pclk_vopgrf_en pclk_vopgrf clock gating control. When high, disable clock
2	RW	0x0	pclk_vop2_biu_en pclk_vop2_biu clock gating control. When high, disable clock
1	RW	0x0	dclk_vp2_en dclk_vp2 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
0	RW	0x0	dclk_vp1_en dclk_vp1 clock gating control. When high, disable clock

CRU_GATE_CON63

Address: Operational Base(0x27200000) + offset (0x08FC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pclk_hdcp0_en pclk_hdcp0 clock gating control. When high, disable clock
13	RW	0x0	hclk_hdcp0_en hclk_hdcp0 clock gating control. When high, disable clock
12	RW	0x0	aclk_hdcp0_en aclk_hdcp0 clock gating control. When high, disable clock
11	RO	0x0	reserved
10	RW	0x0	pclk_vo0_grf_en pclk_vo0_grf clock gating control. When high, disable clock
9	RW	0x0	aclk_hdcp0_biu_en aclk_hdcp0_biu clock gating control. When high, disable clock
8	RO	0x0	reserved
7	RW	0x0	pclk_vo0_biu_en pclk_vo0_biu clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	hclk_vo0_biu_en hclk_vo0_biu clock gating control. When high, disable clock
4	RO	0x0	reserved
3	RW	0x0	pclk_vo0_root_en pclk_vo0_root clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	hclk_vo0_root_en hclk_vo0_root clock gating control. When high, disable clock
0	RW	0x0	aclk_vo0_root_en aclk_vo0_root clock gating control. When high, disable clock

CRU_GATE_CON64

Address: Operational Base(0x27200000) + offset (0x0900)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	clk_edp0_200m_en clk_edp0_200m clock gating control. When high, disable clock
14	RW	0x0	clk_edp0_24m_en clk_edp0_24m clock gating control. When high, disable clock
13	RW	0x0	pclk_edp0_en pclk_edp0 clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x0	clk_extref_timeout_vo0_en clk_extref_timeout_vo0 clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	clk_hdmitx0_ref_en clk_hdmitx0_ref clock gating control. When high, disable clock
8	RW	0x0	clk_hdmitx0_arc_en clk_hdmitx0_arc clock gating control. When high, disable clock
7	RW	0x0	pclk_hdmitx0_en pclk_hdmitx0 clock gating control. When high, disable clock
6	RW	0x0	clk_dsihost0_en clk_dsihost0 clock gating control. When high, disable clock
5	RW	0x0	pclk_dsihost0_en pclk_dsihost0 clock gating control. When high, disable clock
4	RW	0x0	clk_trng0_skp_en clk_trng0_skp clock gating control. When high, disable clock
3:0	RO	0x0	reserved

CRU_GATE_CON65

Address: Operational Base(0x27200000) + offset (0x0904)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mclk_spdif_rx2_en mclk_spdif_rx2 clock gating control. When high, disable clock
14	RW	0x0	hclk_spdif_rx2_en hclk_spdif_rx2 clock gating control. When high, disable clock
13	RW	0x0	mclk_spdif_tx2_en mclk_spdif_tx2 clock gating control. When high, disable clock
12:11	RO	0x0	reserved
10	RW	0x0	hclk_spdif_tx2_en hclk_spdif_tx2 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
9	RW	0x0	hclk_sai6_en hclk_sai6 clock gating control. When high, disable clock
8	RW	0x0	mclk_sai6_en mclk_sai6 clock gating control. When high, disable clock
7	RW	0x0	mclk_sai6_src_en mclk_sai6_src clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	hclk_sai5_en hclk_sai5 clock gating control. When high, disable clock
4	RW	0x0	mclk_sai5_en mclk_sai5 clock gating control. When high, disable clock
3	RW	0x0	mclk_sai5_src_en mclk_sai5_src clock gating control. When high, disable clock
2:0	RO	0x0	reserved

CRU_GATE_CON66

Address: Operational Base(0x27200000) + offset (0x0908)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	mclk_sai8_en mclk_sai8 clock gating control. When high, disable clock
1	RW	0x0	mclk_sai8_src_en mclk_sai8_src clock gating control. When high, disable clock
0	RW	0x0	hclk_sai8_en hclk_sai8 clock gating control. When high, disable clock

CRU_GATE_CON67

Address: Operational Base(0x27200000) + offset (0x090C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_aux16mhz_0_en clk_aux16mhz_0 clock gating control. When high, disable clock
14	RW	0x0	mclk_spdif_tx3_en mclk_spdif_tx3 clock gating control. When high, disable clock
13	RW	0x0	hclk_spdif_tx5_en hclk_spdif_tx5 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
12	RW	0x0	hclk_spdif_tx4_en hclk_spdif_tx4 clock gating control. When high, disable clock
11	RW	0x0	hclk_spdif_tx3_en hclk_spdif_tx3 clock gating control. When high, disable clock
10	RW	0x0	hclk_sai7_en hclk_sai7 clock gating control. When high, disable clock
9	RW	0x0	mclk_sai7_en mclk_sai7 clock gating control. When high, disable clock
8	RW	0x0	mclk_sai7_src_en mclk_sai7_src clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	pclk_vo1_biu_en pclk_vo1_biu clock gating control. When high, disable clock
5	RW	0x0	hclk_vo1_biu_en hclk_vo1_biu clock gating control. When high, disable clock
4	RO	0x0	reserved
3	RW	0x0	pclk_vo1_root_en pclk_vo1_root clock gating control. When high, disable clock
2	RW	0x0	hclk_vo1_root_en hclk_vo1_root clock gating control. When high, disable clock
1	RW	0x0	aclk_vo1_root_en aclk_vo1_root clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON68

Address: Operational Base(0x27200000) + offset (0x0910)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	mclk_spdif_tx5_en mclk_spdif_tx5 clock gating control. When high, disable clock
12	RW	0x0	mclk_spdif_tx4_en mclk_spdif_tx4 clock gating control. When high, disable clock
11	RW	0x0	mclk_sai9_en mclk_sai9 clock gating control. When high, disable clock
10	RW	0x0	mclk_sai9_src_en mclk_sai9_src clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
9	RW	0x0	hclk_sai9_en hclk_sai9 clock gating control. When high, disable clock
8	RO	0x0	reserved
7	RW	0x0	clk_trng1_skp_en clk_trng1_skp clock gating control. When high, disable clock
6	RW	0x0	pclk_hdcp1_en pclk_hdcp1 clock gating control. When high, disable clock
5	RW	0x0	hclk_hdcp1_en hclk_hdcp1 clock gating control. When high, disable clock
4	RW	0x0	aclk_hdcp1_en aclk_hdcp1 clock gating control. When high, disable clock
3	RW	0x0	aclk_hdcp1_biu_en aclk_hdcp1_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_vo1_grf_en pclk_vo1_grf clock gating control. When high, disable clock
1	RW	0x0	pclk_dp0_en pclk_dp0 clock gating control. When high, disable clock
0	RW	0x0	aclk_dp0_en aclk_dp0 clock gating control. When high, disable clock

CRU_GATE_CON69

Address: Operational Base(0x27200000) + offset (0x0914)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_pvtpll_gpu_en pclk_pvtpll_gpu clock gating control. When high, disable clock
14	RW	0x0	clk_ref_pvtpll_gpu_en clk_ref_pvtpll_gpu clock gating control. When high, disable clock
13	RW	0x0	pclk_gpu_grf_en pclk_gpu_grf clock gating control. When high, disable clock
12:10	RO	0x0	reserved
9	RW	0x0	pclk_gpu_biu_en pclk_gpu_biu clock gating control. When high, disable clock
8	RW	0x0	pclk_gpu_root_en pclk_gpu_root clock gating control. When high, disable clock
7	RW	0x0	aclk_m0_gpu_biu_en aclk_m0_gpu_biu clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	aclk_s_gpu_biu_en aclk_s_gpu_biu clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	clk_gpu_pvtpll_src_en clk_gpu_pvtpll_src clock gating control. When high, disable clock
3	RW	0x0	clk_gpu_en clk_gpu clock gating control. When high, disable clock
2	RW	0x0	clk_gpu_inner_en clk_gpu_inner clock gating control. When high, disable clock
1	RW	0x0	clk_gpu_src_pre_en clk_gpu_src_pre clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON72

Address: Operational Base(0x27200000) + offset (0x0920)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	pclk_center_biu_en pclk_center_biu clock gating control. When high, disable clock
11	RW	0x0	pclk_sharemem_en pclk_sharemem clock gating control. When high, disable clock
10	RW	0x0	pclk_dma2ddr_en pclk_dma2ddr clock gating control. When high, disable clock
9	RW	0x0	pclk_center_grf_en pclk_center_grf clock gating control. When high, disable clock
8	RW	0x0	hclk_center_biu_en hclk_center_biu clock gating control. When high, disable clock
7	RW	0x0	aclk_ddr_sharemem_biu_en aclk_ddr_sharemem_biu clock gating control. When high, disable clock
6	RW	0x0	aclk_ddr_sharemem_en aclk_ddr_sharemem clock gating control. When high, disable clock
5	RW	0x0	aclk_dma2ddr_en aclk_dma2ddr clock gating control. When high, disable clock
4	RW	0x0	aclk_center_biu_en aclk_center_biu clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
3	RW	0x0	pclk_center_root_en pclk_center_root clock gating control. When high, disable clock
2	RW	0x0	hclk_center_root_en hclk_center_root clock gating control. When high, disable clock
1	RW	0x0	aclk_center_low_root_en aclk_center_low_root clock gating control. When high, disable clock
0	RW	0x0	aclk_center_root_en aclk_center_root clock gating control. When high, disable clock

CRU_GATE_CON78

Address: Operational Base(0x27200000) + offset (0x0938)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	hclk_vepu1_root_en hclk_vepu1_root clock gating control. When high, disable clock

CRU_GATE_CON79

Address: Operational Base(0x27200000) + offset (0x093C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_vepu1_core_en clk_vepu1_core clock gating control. When high, disable clock
4	RW	0x0	aclk_vepu1_en aclk_vepu1 clock gating control. When high, disable clock
3	RW	0x0	hclk_vepu1_en hclk_vepu1 clock gating control. When high, disable clock
2	RW	0x0	aclk_vepu1_biu_en aclk_vepu1_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_vepu1_biu_en hclk_vepu1_biu clock gating control. When high, disable clock
0	RW	0x0	aclk_vepu1_root_en aclk_vepu1_root clock gating control. When high, disable clock

CRU_SOFTRST_CON01

Address: Operational Base(0x27200000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	hresetn_top_biu When high, reset relative logic
13:8	RO	0x00	reserved
7	RW	0x0	aresetn_secure_high_biu When high, reset relative logic
6	RW	0x0	aresetn_top_mid_biu When high, reset relative logic
5	RW	0x0	presetn_top_biu When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	aresetn_top_biu When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON02

Address: Operational Base(0x27200000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	aresetn_vo0vop_channel_biu When high, reset relative logic
0	RW	0x0	hresetn_vo0vop_channel_biu When high, reset relative logic

CRU_SOFTRST_CON06

Address: Operational Base(0x27200000) + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	resetn_bisrintf When high, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON07

Address: Operational Base(0x27200000) + offset (0x0A1C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mresetn_spdif_rx0 When high, reset relative logic
14	RW	0x0	hresetn_spdif_rx0 When high, reset relative logic

Bit	Attr	Reset Value	Description
13	RW	0x0	hresetn_sai0 When high, reset relative logic
12	RW	0x0	mresetn_sai0 When high, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	resetn_asrc_4ch_1 When high, reset relative logic
9	RW	0x0	resetn_asrc_4ch_0 When high, reset relative logic
8	RW	0x0	resetn_asrc_2ch_1 When high, reset relative logic
7	RW	0x0	resetn_asrc_2ch_0 When high, reset relative logic
6	RW	0x0	hresetn_asrc_4ch_1 When high, reset relative logic
5	RW	0x0	hresetn_asrc_4ch_0 When high, reset relative logic
4	RW	0x0	hresetn_asrc_2ch_1 When high, reset relative logic
3	RW	0x0	hresetn_asrc_2ch_0 When high, reset relative logic
2	RW	0x0	hresetn_audio_biu When high, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON08

Address: Operational Base(0x27200000) + offset (0x0A20)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	hresetn_sai3 When high, reset relative logic
13	RO	0x0	reserved
12	RW	0x0	mresetn_sai3 When high, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	hresetn_sai2 When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	mresetn_sai2 When high, reset relative logic
7	RO	0x0	reserved
6	RW	0x0	hresetn_sai1 When high, reset relative logic
5	RW	0x0	mresetn_sai1 When high, reset relative logic
4:2	RO	0x0	reserved
1	RW	0x0	mresetn_spdif_rx1 When high, reset relative logic
0	RW	0x0	hresetn_spdif_rx1 When high, reset relative logic

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CRU_SOFTRST_CON09

Address: Operational Base(0x27200000) + offset (0x0A24)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	mresetn_spdif_tx1 When high, reset relative logic
11	RW	0x0	hresetn_spdif_tx1 When high, reset relative logic
10	RW	0x0	mresetn_spdif_tx0 When high, reset relative logic
9	RW	0x0	hresetn_spdif_tx0 When high, reset relative logic
8	RW	0x0	mresetn_pdm1 When high, reset relative logic
7	RW	0x0	hresetn_pdm1 When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	resetn_pdm1 When high, reset relative logic
4	RW	0x0	mresetn_acdcdig_dsm When high, reset relative logic
3	RW	0x0	hresetn_acdcdig_dsm When high, reset relative logic
2	RW	0x0	hresetn_sai4 When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	mresetn_sai4 When high, reset relative logic

CRU_SOFTRST_CON11

Address: Operational Base(0x27200000) + offset (0x0A2C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_key_shift When high, reset relative logic
14	RW	0x0	hresetn_bus_biu When high, reset relative logic
13	RW	0x0	presetn_vccio_ioc When high, reset relative logic
12	RW	0x0	presetn_intmux2bus When high, reset relative logic
11:10	RO	0x0	reserved
9	RW	0x0	resetn_can1 When high, reset relative logic
8	RW	0x0	hresetn_can1 When high, reset relative logic
7	RW	0x0	resetn_can0 When high, reset relative logic

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Bit	Attr	Reset Value	Description
6	RW	0x0	hresetn_can0 When high, reset relative logic
5	RW	0x0	presetn_cru When high, reset relative logic
4	RW	0x0	presetn_bus_biu When high, reset relative logic
3	RW	0x0	aresetn_bus_biu When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON12

Address: Operational Base(0x27200000) + offset (0x0A30)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_i2c4 When high, reset relative logic
14	RW	0x0	resetn_i2c3 When high, reset relative logic
13	RW	0x0	resetn_i2c2 When high, reset relative logic
12	RW	0x0	resetn_i2c1 When high, reset relative logic
11	RW	0x0	aresetn_gic When high, reset relative logic
10	RW	0x0	tresetn_wdt_busmcu When high, reset relative logic
9	RW	0x0	presetn_wdt_busmcu When high, reset relative logic
8	RW	0x0	presetn_i2c9 When high, reset relative logic
7	RW	0x0	presetn_i2c8 When high, reset relative logic
6	RW	0x0	presetn_i2c7 When high, reset relative logic
5	RW	0x0	presetn_i2c6 When high, reset relative logic
4	RW	0x0	presetn_i2c5 When high, reset relative logic
3	RW	0x0	presetn_i2c4 When high, reset relative logic
2	RW	0x0	presetn_i2c3 When high, reset relative logic
1	RW	0x0	presetn_i2c2 When high, reset relative logic
0	RW	0x0	presetn_i2c1 When high, reset relative logic

CRU_SOFTRST_CON13

Address: Operational Base(0x27200000) + offset (0x0A34)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_uart6 When high, reset relative logic
14	RW	0x0	presetn_uart5 When high, reset relative logic
13	RW	0x0	presetn_uart4 When high, reset relative logic
12	RW	0x0	presetn_uart3 When high, reset relative logic
11	RW	0x0	presetn_uart2 When high, reset relative logic
10	RW	0x0	presetn_uart0 When high, reset relative logic
9	RW	0x0	resetn_tsadc When high, reset relative logic
8	RW	0x0	presetn_tsadc When high, reset relative logic
7	RW	0x0	resetn_saradc When high, reset relative logic
6	RW	0x0	presetn_saradc When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	resetn_i2c9 When high, reset relative logic
3	RW	0x0	resetn_i2c8 When high, reset relative logic
2	RW	0x0	resetn_i2c7 When high, reset relative logic
1	RW	0x0	resetn_i2c6 When high, reset relative logic
0	RW	0x0	resetn_i2c5 When high, reset relative logic

CRU_SOFTRST_CON14

Address: Operational Base(0x27200000) + offset (0x0A38)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sresetn_uart5 When high, reset relative logic
14:13	RO	0x0	reserved
12	RW	0x0	sresetn_uart4 When high, reset relative logic
11:10	RO	0x0	reserved
9	RW	0x0	sresetn_uart3 When high, reset relative logic
8:7	RO	0x0	reserved
6	RW	0x0	sresetn_uart2 When high, reset relative logic

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Bit	Attr	Reset Value	Description
5	RW	0x0	sresetn_uart0 When high, reset relative logic
4	RW	0x0	presetn_uart11 When high, reset relative logic
3	RW	0x0	presetn_uart10 When high, reset relative logic
2	RW	0x0	presetn_uart9 When high, reset relative logic
1	RW	0x0	presetn_uart8 When high, reset relative logic
0	RW	0x0	presetn_uart7 When high, reset relative logic

CRU_SOFTRST_CON15

Address: Operational Base(0x27200000) + offset (0x0A3C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_spi2 When high, reset relative logic
14	RW	0x0	presetn_spi1 When high, reset relative logic
13	RW	0x0	presetn_spi0 When high, reset relative logic
12	RO	0x0	reserved
11	RW	0x0	sresetn_uart11 When high, reset relative logic
10	RW	0x0	sresetn_uart10 When high, reset relative logic
9	RW	0x0	sresetn_uart9 When high, reset relative logic
8	RW	0x0	sresetn_uart8 When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	sresetn_uart7 When high, reset relative logic
4:3	RO	0x0	reserved
2	RW	0x0	sresetn_uart6 When high, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON16

Address: Operational Base(0x27200000) + offset (0x0A40)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	resetn_pwm1 When high, reset relative logic
10	RW	0x0	presetn_pwm1 When high, reset relative logic

Bit	Attr	Reset Value	Description
9	RW	0x0	presetn_sys_grf When high, reset relative logic
8	RW	0x0	tresetn_wdtpmu When high, reset relative logic
7	RW	0x0	presetn_wdtpmu When high, reset relative logic
6	RW	0x0	resetn_spi4 When high, reset relative logic
5	RW	0x0	resetn_spi3 When high, reset relative logic
4	RW	0x0	resetn_spi2 When high, reset relative logic
3	RW	0x0	resetn_spi1 When high, reset relative logic
2	RW	0x0	resetn_spi0 When high, reset relative logic
1	RW	0x0	presetn_spi4 When high, reset relative logic
0	RW	0x0	presetn_spi3 When high, reset relative logic

CRU_SOFTRST_CON17

Address: Operational Base(0x27200000) + offset (0x0A44)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_gpio1 When high, reset relative logic
14	RO	0x0	reserved
13	RW	0x0	presetn_mailbox0 When high, reset relative logic
12	RW	0x0	presetn_busioc When high, reset relative logic
11	RW	0x0	resetn_timer5 When high, reset relative logic
10	RW	0x0	resetn_timer4 When high, reset relative logic
9	RW	0x0	resetn_timer3 When high, reset relative logic
8	RW	0x0	resetn_timer2 When high, reset relative logic
7	RW	0x0	resetn_timer1 When high, reset relative logic
6	RW	0x0	resetn_timer0 When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	presetn_bustimer1 When high, reset relative logic
3	RW	0x0	presetn_bustimer0 When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON18

Address: Operational Base(0x27200000) + offset (0x0A48)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_timer10 When high, reset relative logic
14	RW	0x0	resetn_timer9 When high, reset relative logic
13	RW	0x0	resetn_timer8 When high, reset relative logic
12	RW	0x0	resetn_timer7 When high, reset relative logic
11	RW	0x0	resetn_timer6 When high, reset relative logic
10	RO	0x0	reserved
9	RW	0x0	dresetn_decom When high, reset relative logic
8	RW	0x0	presetn_decom When high, reset relative logic
7	RW	0x0	aresetn_decom When high, reset relative logic
6	RW	0x0	dbresetn_gpio4 When high, reset relative logic
5	RW	0x0	presetn_gpio4 When high, reset relative logic
4	RW	0x0	dbresetn_gpio3 When high, reset relative logic
3	RW	0x0	presetn_gpio3 When high, reset relative logic
2	RW	0x0	dbresetn_gpio2 When high, reset relative logic
1	RW	0x0	presetn_gpio2 When high, reset relative logic
0	RW	0x0	dbresetn_gpio1 When high, reset relative logic

CRU_SOFTRST_CON19

Address: Operational Base(0x27200000) + offset (0x0A4C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	tresetn_bus_cm0_jtag When high, reset relative logic
12	RW	0x1	fresetn_bus_cm0_core When high, reset relative logic
11	RW	0x0	hresetn_bus_cm0_biu When high, reset relative logic
10	RO	0x0	reserved
9	RW	0x0	hresetn_i3c1 When high, reset relative logic
8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	hresetn_i3c0 When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	resetn_ref_pvtpll_bus When high, reset relative logic
4	RW	0x0	aresetn_spinlock When high, reset relative logic
3	RW	0x0	aresetn_dmac2 When high, reset relative logic
2	RW	0x0	aresetn_dmac1 When high, reset relative logic
1	RW	0x0	aresetn_dmac0 When high, reset relative logic
0	RW	0x0	resetn_timer11 When high, reset relative logic

CRU_SOFTRST_CON20

Address: Operational Base(0x27200000) + offset (0x0A50)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_i3c1 When high, reset relative logic
12	RW	0x0	resetn_i3c0 When high, reset relative logic
11:10	RO	0x0	reserved
9	RW	0x0	resetn_counter_pwm1 When high, reset relative logic
8	RW	0x0	resetn_freq_pwm1 When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	resetn_pwm2 When high, reset relative logic
4	RW	0x0	presetn_pwm2 When high, reset relative logic
3	RW	0x0	presetn_pvtpll_bus When high, reset relative logic
2	RO	0x0	reserved
1	RW	0x0	presetn_intmux2ddr When high, reset relative logic
0	RW	0x0	presetn_intmux2pmu When high, reset relative logic

CRU_SOFTRST_CON21

Address: Operational Base(0x27200000) + offset (0x0A54)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_ddr_hwlp_ch1 When high, reset relative logic

Bit	Attr	Reset Value	Description
14	RW	0x0	presetn_ddr_mon_ch1 When high, reset relative logic
13	RW	0x0	presetn_ddr_hwlp_ch0 When high, reset relative logic
12:11	RO	0x0	reserved
10	RW	0x0	resetn_ddr_mon_ch0 When high, reset relative logic
9:7	RO	0x0	reserved
6	RW	0x1	resetn_dfi_ch0 When high, reset relative logic
5	RW	0x0	aresetn_ddr_biu When high, reset relative logic
4	RW	0x0	tmresetn_ddr_mon_ch0 When high, reset relative logic
3	RW	0x0	presetn_ddr_upctl_ch0 When high, reset relative logic
2	RW	0x0	presetn_ddr_biu When high, reset relative logic
1	RW	0x0	presetn_ddr_mon_ch0 When high, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST_CON22

Address: Operational Base(0x27200000) + offset (0x0A58)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	fresetn_ddr_cm0_core When high, reset relative logic
14	RW	0x0	hresetn_ddr_biu When high, reset relative logic
13	RW	0x0	hresetn_ahb2apb When high, reset relative logic
12	RW	0x0	presetn_ahb2apb When high, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	resetn_ddr_scramble_ch1 When high, reset relative logic
9	RW	0x0	resetn_ddr_scramble_ch0 When high, reset relative logic
8:7	RO	0x0	reserved
6	RW	0x0	resetn_ddr_mon_ch1 When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	aresetn_ddr01_msch1 When high, reset relative logic
3	RW	0x0	aresetn_ddr01_msch0 When high, reset relative logic
2	RW	0x1	resetn_dfi_ch1 When high, reset relative logic
1	RW	0x0	tmresetn_ddr_mon_ch1 When high, reset relative logic

Bit	Attr	Reset Value	Description
0	RW	0x0	presetn_ddr_upctl_ch1 When high, reset relative logic

CRU_SOFTRST_CON23

Address: Operational Base(0x27200000) + offset (0x0A5C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	presetn_ddr_grf When high, reset relative logic
10	RO	0x0	reserved
9	RW	0x0	tresetn_ddr_cm0_jtag When high, reset relative logic
8	RW	0x0	presetn_timer When high, reset relative logic
7	RW	0x0	presetn_wdt_ddr When high, reset relative logic
6	RW	0x0	tresetn_wdt_ddr When high, reset relative logic
5	RW	0x0	resetn_ddr_timer1 When high, reset relative logic
4	RW	0x0	resetn_ddr_timer0 When high, reset relative logic
3	RO	0x0	reserved
2	RW	0x0	presetn_ddr01_msch1 When high, reset relative logic
1	RW	0x0	presetn_ddr01_msch0 When high, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST_CON25

Address: Operational Base(0x27200000) + offset (0x0A64)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	aresetn_ddr_upctl_4_ch0 When high, reset relative logic
5	RW	0x0	aresetn_ddr_upctl_3_ch0 When high, reset relative logic
4	RW	0x0	aresetn_ddr_upctl_2_ch0 When high, reset relative logic
3	RW	0x0	aresetn_ddr_upctl_1_ch0 When high, reset relative logic
2	RW	0x0	aresetn_ddr_upctl_0_ch0 When high, reset relative logic
1	RW	0x0	resetn_ddr_upctl_ch0 When high, reset relative logic
0	RO	0x0	reserved

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CRU_SOFTRST_CON26

Address: Operational Base(0x27200000) + offset (0x0A68)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	aresetn_ddr_upctl_4_ch1 When high, reset relative logic
5	RW	0x0	aresetn_ddr_upctl_3_ch1 When high, reset relative logic
4	RW	0x0	aresetn_ddr_upctl_2_ch1 When high, reset relative logic
3	RW	0x0	aresetn_ddr_upctl_1_ch1 When high, reset relative logic
2	RW	0x0	aresetn_ddr_upctl_0_ch1 When high, reset relative logic
1	RW	0x0	resetn_ddr_upctl_ch1 When high, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST_CON27

Address: Operational Base(0x27200000) + offset (0x0A6C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	presetn_pvtpll_ddr When high, reset relative logic
0	RW	0x0	resetn_ref_pvtpll_ddr When high, reset relative logic

CRU_SOFTRST_CON28

Address: Operational Base(0x27200000) + offset (0x0A70)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	lresetn_rknn0_biu When high, reset relative logic
11	RW	0x0	aresetn_rknn0_biu When high, reset relative logic
10	RO	0x0	reserved
9	RW	0x0	aresetn_rknn0 When high, reset relative logic
8:0	RO	0x000	reserved

CRU_SOFTRST_CON29

Address: Operational Base(0x27200000) + offset (0x0A74)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	lresetn_rknn1_biu When high, reset relative logic
2	RW	0x0	aresetn_rknn1_biu When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	aresetn_rknn1 When high, reset relative logic

CRU_SOFTRST_CON31

Address: Operational Base(0x27200000) + offset (0x0A7C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	tresetn_npu_wdt When high, reset relative logic
14	RW	0x0	presetn_npu_wdt When high, reset relative logic
13	RW	0x0	resetn_nputimer1 When high, reset relative logic
12	RW	0x0	resetn_nputimer0 When high, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	presetn_npu_timer When high, reset relative logic
9	RW	0x0	presetn_nputop_biu When high, reset relative logic
8:2	RO	0x00	reserved
1	RW	0x0	lresetn_npusubsys_biu When high, reset relative logic
0	RW	0x0	resetn_npu_dap When high, reset relative logic

CRU_SOFTRST_CON32

Address: Operational Base(0x27200000) + offset (0x0A80)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	hresetn_rknntop_biu When high, reset relative logic
12	RW	0x0	hresetn_rknn_cbuf When high, reset relative logic
11	RW	0x0	aresetn_rknntop_biu When high, reset relative logic
10:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	tresetn_npu_cm0_jtag When high, reset relative logic
7	RW	0x1	fresetn_npu_cm0_core When high, reset relative logic
6	RW	0x0	hresetn_npu_cm0_biu When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	resetn_npu_pvtpll When high, reset relative logic
3	RW	0x0	presetn_pvtpll_npu When high, reset relative logic
2	RW	0x0	presetn_npu_grf When high, reset relative logic
1	RW	0x1	aresetn_rvcore0 When high, reset relative logic
0	RW	0x0	aresetn_rknn_cbuf When high, reset relative logic

CRU_SOFTRST_CON33

Address: Operational Base(0x27200000) + offset (0x0A84)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	tresetn_emmc When high, reset relative logic
11	RW	0x0	bresetn_emmc When high, reset relative logic
10	RW	0x0	aresetn_emmc When high, reset relative logic
9	RW	0x0	hresetn_emmc When high, reset relative logic
8	RW	0x0	cresetn_emmc When high, reset relative logic
7	RW	0x0	hresetn_fspi When high, reset relative logic
6	RW	0x0	sresetn_fspi When high, reset relative logic
5:4	RO	0x0	reserved
3	RW	0x0	aresetn_nvm_biu When high, reset relative logic
2	RW	0x0	hresetn_nvm_biu When high, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON34

Address: Operational Base(0x27200000) + offset (0x0A88)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x1	resetn_pcie0_power_up When high, reset relative logic
14	RO	0x0	reserved
13	RW	0x0	presetn_pcie0 When high, reset relative logic
12:10	RO	0x0	reserved
9	RW	0x0	aresetn_php_biu When high, reset relative logic
8:6	RO	0x0	reserved
5	RW	0x0	presetn_php_biu When high, reset relative logic
4:2	RO	0x0	reserved
1	RW	0x0	presetn_grf When high, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST_CON35

Address: Operational Base(0x27200000) + offset (0x0A8C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	aresetn_mmu1 When high, reset relative logic
13	RW	0x0	aresetn_slv_mmu0 When high, reset relative logic
12	RO	0x0	reserved
11	RW	0x0	aresetn_mmu0 When high, reset relative logic
10:4	RO	0x00	reserved
3	RW	0x0	aresetn_usb3otg1 When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON36

Address: Operational Base(0x27200000) + offset (0x0A90)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x1	resetn_pcie1_power_up When high, reset relative logic
8	RO	0x0	reserved
7	RW	0x0	presetn_pcie1 When high, reset relative logic
6:1	RO	0x00	reserved
0	RW	0x0	aresetn_slv_mmu1 When high, reset relative logic

CRU_SOFTRST_CON37

Address: Operational Base(0x27200000) + offset (0x0A94)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	resetn_asic0 When high, reset relative logic
6	RW	0x0	resetn_asic1 When high, reset relative logic
5	RW	0x0	aresetn_sata1 When high, reset relative logic
4	RW	0x0	aresetn_sata0 When high, reset relative logic
3	RW	0x0	resetn_pmalive1 When high, reset relative logic
2	RW	0x0	resetn_pmalive0 When high, reset relative logic
1	RW	0x0	resetn_rxoob1 When high, reset relative logic
0	RW	0x0	resetn_rxoob0 When high, reset relative logic

CRU_SOFTRST_CON40

Address: Operational Base(0x27200000) + offset (0x0AA0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scanresetn_csidphy1 When high, reset relative logic
2	RW	0x0	presetn_csidphy1 When high, reset relative logic Note: presetn_csidphy1_grf and presetn_csidphy1_apb2asb use same rst
1:0	RO	0x0	reserved

CRU_SOFTRST_CON42

Address: Operational Base(0x27200000) + offset (0x0AA8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	hresetn_sdio When high, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	presetn_gmac1 When high, reset relative logic
9	RW	0x0	presetn_gmac0 When high, reset relative logic
8	RW	0x0	aresetn_gmac1 When high, reset relative logic

Bit	Attr	Reset Value	Description
7	RW	0x0	aresetn_gmac0 When high, reset relative logic
6	RW	0x0	hresetn_sdgmac_biu When high, reset relative logic
5	RW	0x0	aresetn_sdgmac_biu When high, reset relative logic
4	RW	0x0	presetn_sdgmac_biu When high, reset relative logic
3	RW	0x0	presetn_sdgmac_grf When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON43

Address: Operational Base(0x27200000) + offset (0x0AAC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	aresetn_flexbus When high, reset relative logic
12	RO	0x0	reserved
11	RW	0x0	resetn_flexbus When high, reset relative logic
10	RW	0x0	hresetn_flexbus When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	presetn_dsmc When high, reset relative logic
7	RW	0x0	aresetn_dsmc When high, reset relative logic
6	RW	0x0	aresetn_dsmc_biu When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	hresetn_fspi1 When high, reset relative logic
3	RW	0x0	sresetn_fspi1 When high, reset relative logic
2	RW	0x0	hresetn_sdmmc0 When high, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON45

Address: Operational Base(0x27200000) + offset (0x0AB4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	resetn_rkvdec_core When high, reset relative logic
8	RW	0x0	resetn_rkvdec_hevc_ca When high, reset relative logic

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Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6	RW	0x0	aresetn_rkvdec_biu When high, reset relative logic
5	RW	0x0	hresetn_rkvdec_biu When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	hresetn_rkvdec When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON47

Address: Operational Base(0x27200000) + offset (0x0ABC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	aresetn_ufs_sys When high, reset relative logic
14	RO	0x0	reserved
13	RW	0x0	aresetn_slv_mmu2 When high, reset relative logic
12	RW	0x0	aresetn_mmu2 When high, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	aresetn_ufs_biu When high, reset relative logic
9:6	RO	0x0	reserved
5	RW	0x0	aresetn_usb3otg0 When high, reset relative logic
4	RW	0x0	presetn_usbufs_biu When high, reset relative logic
3	RW	0x0	aresetn_usb_biu When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON48

Address: Operational Base(0x27200000) + offset (0x0AC0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	presetn_ufs_grf When high, reset relative logic
1	RW	0x0	presetn_usbufs_grf When high, reset relative logic
0	RW	0x0	aresetn_ufs When high, reset relative logic

CRU_SOFTRST_CON49

Address: Operational Base(0x27200000) + offset (0x0AC4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_core_rga2e_0 When high, reset relative logic
14	RW	0x0	aresetn_rga2e_0 When high, reset relative logic
13	RW	0x0	hresetn_rga2e_0 When high, reset relative logic
12	RW	0x0	aresetn_ebc_biu When high, reset relative logic
11	RW	0x0	aresetn_vdpp_biu When high, reset relative logic
10	RW	0x0	aresetn_rga_biu When high, reset relative logic
9:8	RO	0x0	reserved
7	RW	0x0	aresetn_jpeg_biu When high, reset relative logic
6	RW	0x0	hresetn_vpu_biu When high, reset relative logic
5:0	RO	0x00	reserved

CRU_SOFTRST_CON50

Address: Operational Base(0x27200000) + offset (0x0AC8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	dresetn_ebc When high, reset relative logic
11	RW	0x0	aresetn_ebc When high, reset relative logic
10	RW	0x0	hresetn_ebc When high, reset relative logic
9:8	RO	0x0	reserved
7	RW	0x0	resetn_core_rga2e_1 When high, reset relative logic
6	RW	0x0	aresetn_rga2e_1 When high, reset relative logic
5	RW	0x0	hresetn_rga2e_1 When high, reset relative logic
4	RW	0x0	resetn_core_vdpp When high, reset relative logic
3	RW	0x0	aresetn_vdpp When high, reset relative logic
2	RW	0x0	hresetn_vdpp When high, reset relative logic
1	RW	0x0	hresetn_jpeg When high, reset relative logic
0	RW	0x0	aresetn_jpeg When high, reset relative logic

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CRU_SOFTRST_CON51

Address: Operational Base(0x27200000) + offset (0x0ACC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	resetn_vepu0_core When high, reset relative logic
5	RW	0x0	aresetn_vepu0 When high, reset relative logic
4	RW	0x0	hresetn_vepu0 When high, reset relative logic
3	RW	0x0	aresetn_vepu0_biu When high, reset relative logic
2	RW	0x0	hresetn_vepu0_biu When high, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON53

Address: Operational Base(0x27200000) + offset (0x0AD4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	resetn_isp0_vicap When high, reset relative logic
10	RW	0x0	resetn_isp0 When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	hresetn_vicap When high, reset relative logic
7	RW	0x0	aresetn_vicap When high, reset relative logic
6	RW	0x0	dresetn_vicap When high, reset relative logic
5	RW	0x0	presetn_vi_biu When high, reset relative logic
4	RW	0x0	hresetn_vi_biu When high, reset relative logic
3	RW	0x0	aresetn_vi_biu When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON54

Address: Operational Base(0x27200000) + offset (0x0AD8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	presetn_csi_host_4 When high, reset relative logic
7	RW	0x0	presetn_csi_host_3 When high, reset relative logic
6	RW	0x0	presetn_csi_host_2 When high, reset relative logic
5	RW	0x0	presetn_csi_host_1 When high, reset relative logic
4	RW	0x0	presetn_csi_host_0 When high, reset relative logic
3:2	RO	0x0	reserved
1	RW	0x0	resetn_core_vpss When high, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST_CON59

Address: Operational Base(0x27200000) + offset (0x0AEC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	resetn_vicap_i4clk When high, reset relative logic
4	RW	0x0	resetn_vicap_i3clk When high, reset relative logic
3	RW	0x0	resetn_vicap_i2clk When high, reset relative logic
2	RW	0x0	resetn_vicap_i1clk When high, reset relative logic
1	RW	0x0	resetn_vicap_i0clk When high, reset relative logic
0	RW	0x0	resetn_cifin When high, reset relative logic

CRU_SOFTRST_CON61

Address: Operational Base(0x27200000) + offset (0x0AF4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	dresetn_vp0 When high, reset relative logic
12:10	RO	0x0	reserved
9	RW	0x0	aresetn_vop When high, reset relative logic
8	RW	0x0	hresetn_vop When high, reset relative logic
7	RW	0x0	presetn_vop_biu When high, reset relative logic
6	RW	0x0	hresetn_vop_biu When high, reset relative logic

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Bit	Attr	Reset Value	Description
5	RW	0x0	aresetn_vop2_biu When high, reset relative logic
4	RW	0x0	aresetn_vop_biu When high, reset relative logic
3:0	RO	0x0	reserved

CRU_SOFTRST_CON62

Address: Operational Base(0x27200000) + offset (0x0AF8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	presetn_vopgrf When high, reset relative logic
2	RW	0x0	presetn_vop2_biu When high, reset relative logic
1	RW	0x0	dresetn_vp2 When high, reset relative logic
0	RW	0x0	dresetn_vp1 When high, reset relative logic

CRU_SOFTRST_CON63

Address: Operational Base(0x27200000) + offset (0x0AFC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	resetn_hdcp0 When high, reset relative logic
13	RW	0x0	hresetn_hdcp0 When high, reset relative logic
12	RW	0x0	aresetn_hdcp0 When high, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	presetn_vo0_grf When high, reset relative logic
9	RW	0x0	aresetn_hdcp0_biu When high, reset relative logic
8	RO	0x0	reserved
7	RW	0x0	presetn_vo0_biu When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	hresetn_vo0_biu When high, reset relative logic
4:0	RO	0x00	reserved

CRU_SOFTRST_CON64

Address: Operational Base(0x27200000) + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	resetn_edp0_24m When high, reset relative logic
13	RW	0x0	presetn_edp0 When high, reset relative logic
12:10	RO	0x0	reserved
9	RW	0x0	resetn_hdmitx0_ref When high, reset relative logic
8	RO	0x0	reserved
7	RW	0x0	presetn_hdmitx0 When high, reset relative logic
6	RW	0x0	resetn_dsihost0 When high, reset relative logic
5	RW	0x0	presetn_dsihost0 When high, reset relative logic
4:0	RO	0x00	reserved

CRU_SOFTRST_CON65

Address: Operational Base(0x27200000) + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mresetn_spdif_rx2 When high, reset relative logic
14	RW	0x0	hresetn_spdif_rx2 When high, reset relative logic
13	RW	0x0	mresetn_spdif_tx2 When high, reset relative logic
12:11	RO	0x0	reserved
10	RW	0x0	hresetn_spdif_tx2 When high, reset relative logic
9	RW	0x0	hresetn_sai6 When high, reset relative logic
8	RW	0x0	mresetn_sai6 When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	hresetn_sai5 When high, reset relative logic
4	RW	0x0	mresetn_sai5 When high, reset relative logic
3:0	RO	0x0	reserved

CRU_SOFTRST_CON66

Address: Operational Base(0x27200000) + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:3	RO	0x0000	reserved
2	RW	0x0	mresetn_sai8 When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	hresetn_sai8 When high, reset relative logic

CRU_SOFTRST_CON67

Address: Operational Base(0x27200000) + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	mresetn_spdif_tx3 When high, reset relative logic
13	RW	0x0	hresetn_spdif_tx5 When high, reset relative logic
12	RW	0x0	hresetn_spdif_tx4 When high, reset relative logic
11	RW	0x0	hresetn_spdif_tx3 When high, reset relative logic
10	RW	0x0	hresetn_sai7 When high, reset relative logic
9	RW	0x0	mresetn_sai7 When high, reset relative logic
8:7	RO	0x0	reserved
6	RW	0x0	presetn_vo1_biu When high, reset relative logic
5	RW	0x0	hresetn_vo1_biu When high, reset relative logic
4:0	RO	0x00	reserved

CRU_SOFTRST_CON68

Address: Operational Base(0x27200000) + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	mresetn_spdif_tx5 When high, reset relative logic
12	RW	0x0	mresetn_spdif_tx4 When high, reset relative logic
11	RW	0x0	mresetn_sai9 When high, reset relative logic
10	RO	0x0	reserved
9	RW	0x0	hresetn_sai9 When high, reset relative logic
8:7	RO	0x0	reserved
6	RW	0x0	resetn_hdcp1 When high, reset relative logic

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Bit	Attr	Reset Value	Description
5	RW	0x0	hresetn_hdcp1 When high, reset relative logic
4	RW	0x0	aresetn_hdcp1 When high, reset relative logic
3	RW	0x0	aresetn_hdcp1_biu When high, reset relative logic
2	RW	0x0	presetn_vo1_grf When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	resetn_dp0 When high, reset relative logic

CRU_SOFTRST_CON69

Address: Operational Base(0x27200000) + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_pvtpll_gpu When high, reset relative logic
14	RW	0x0	resetn_gpu_pvtpll When high, reset relative logic
13	RW	0x0	presetn_gpu_grf When high, reset relative logic
12:10	RO	0x0	reserved
9	RW	0x0	presetn_gpu_biu When high, reset relative logic
8	RO	0x0	reserved
7	RW	0x0	aresetn_m0_gpu_biu When high, reset relative logic
6	RW	0x0	aresetn_s_gpu_biu When high, reset relative logic
5:4	RO	0x0	reserved
3	RW	0x0	resetn_gpu When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON72

Address: Operational Base(0x27200000) + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	presetn_center_biu When high, reset relative logic
11	RW	0x0	presetn_sharemem When high, reset relative logic
10	RW	0x0	presetn_dma2ddr When high, reset relative logic
9	RW	0x0	presetn_center_grf When high, reset relative logic

Bit	Attr	Reset Value	Description
8	RW	0x0	hresetn_center_biu When high, reset relative logic
7	RW	0x0	aresetn_ddr_sharemem_biu When high, reset relative logic
6	RW	0x0	aresetn_ddr_sharemem When high, reset relative logic
5	RW	0x0	aresetn_dma2ddr When high, reset relative logic
4	RW	0x0	aresetn_center_biu When high, reset relative logic
3:0	RO	0x0	reserved

CRU_SOFTRST_CON75

Address: Operational Base(0x27200000) + offset (0x0B2C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	resetn_linksym_hdmitxphy0 When high, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST_CON78

Address: Operational Base(0x27200000) + offset (0x0B38)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	resetn_dp2_pixelclk When high, reset relative logic
3	RW	0x0	resetn_dp1_pixelclk When high, reset relative logic
2	RW	0x0	resetn_phy_dp0_tx When high, reset relative logic
1	RW	0x0	resetn_dp0_pixelclk When high, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST_CON79

Address: Operational Base(0x27200000) + offset (0x0B3C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	resetn_vepu1_core When high, reset relative logic
4	RW	0x0	aresetn_vepu1 When high, reset relative logic

Bit	Attr	Reset Value	Description
3	RW	0x0	hresetn_vepu1 When high, reset relative logic
2	RW	0x0	aresetn_vepu1_biu When high, reset relative logic
1	RW	0x0	hresetn_vepu1_biu When high, reset relative logic
0	RO	0x0	reserved

CRU_GLB_CNT_TH

Address: Operational Base(0x27200000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x064	global_reset_counter_threshold global_reset_counter_threshold Global soft reset, wdt reset or tsadc_shut reset asserted time counter threshold. Measured in OSC clock cycles

CRU_GLBRST_ST

Address: Operational Base(0x27200000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	glbrst_wdtpmu_rst glbrst_wdtpmu_rst If High, global reset by PMU_WDT.
14	RW	0x0	glbrst_wdtnpu_rst glbrst_wdtnpu_rst If High, global reset by NPU_WDT.
13	RW	0x0	glbrst_wdts_rst glbrst_wdts_rst If High, global reset by WDT_S.
12	RW	0x0	glbrst_wdtns_rst glbrst_wdtns_rst If High, global reset by WDT_NS.
11	RW	0x0	glbrst_buswdt_rst glbrst_buswdt_rst If High, global reset by BUS_WDT.
10	RW	0x0	glbrst_ddrwdt_rst glbrst_ddrwdt_rst If High, global reset by DDR_WDT.
9	RO	0x0	reserved
8	RW	0x0	glbrst_sgrf_crc_chk_rst glbrst_sgrf_crc_chk_rst If High, global reset by PMUSGRF_CRC check.
7	RW	0x0	glbrst_osc_chk_rst glbrst_osc_chk_rst If High, global reset by OSC check.
6	RW	0x0	glbrst_wdt_rst glbrst_wdt_rst If High, global reset by WDT. Check CRU_GLBRST_ST[15:11] for detail.
5	RW	0x0	second_glbrst_wdt_rst second_glbrst_wdt_rst If High, second global reset by WDT.

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Bit	Attr	Reset Value	Description
4	RW	0x0	first_glbrst_wdt_rst first_glbrst_wdt_rst If High, first global reset by WDT.
3	RW	0x0	second_glbrst_tsadc_rst second_glbrst_tsadc_rst If High, second global reset by TSADC.
2	RW	0x0	first_glbrst_tsadc_rst first_glbrst_tsadc_rst If High, first global reset by TSADC.
1	RW	0x0	second_glbrst_register_rst second_glbrst_register_rst If High, second global reset by register.
0	RW	0x0	first_glbrst_register_rst first_glbrst_register_rst If High, first global reset by register.

CRU_GLB_SRST_FST_VALUE

Address: Operational Base(0x27200000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	glb_srsc_first_value GLB_SRST_FST The first global software reset configuration value. Set 0xfdb9 enable.

CRU_GLB_SRST_SND_VALUE

Address: Operational Base(0x27200000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	glb_srsc_second_value GLB_SRST_SND The second global software reset configuration value. Set 0xeca8 enable.

CRU_GLB_RST_CON

Address: Operational Base(0x27200000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	crc_chk_sgrf_trig_glbrst_sel crc_pmusgrf_chk_trig_glbrst_sel 1'b1: CRC_CHK_SGRF check trigger first global reset. 1'b0: CRC_CHK_SGRF check trigger second global reset.
12	RW	0x0	osc_chk_trig_glbrst_sel osc_chk_trig_glbrst_sel 1'b1: OSC check trigger first global reset. 1'b0: OSC check trigger second global reset.
11	RW	0x0	wdt_trig_glbrst_sel wdt_trig_glbrst_sel 1'b1: WDT trigger first global reset. 1'b0: WDT trigger second global reset.
10:9	RO	0x0	reserved
8	RW	0x0	crc_chk_sgrf_trig_glbrst_en crc_chk_sgrf_trig_glbrst_en 1'b1: Enable CRC_CHK_SGRF check trigger global reset. 1'b0: Disable CRC_CHK_SGRF check trigger global reset.

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Bit	Attr	Reset Value	Description
7	RW	0x0	osc_chk_trig_glbrst_en osc_chk_trig_glbrst_en 1'b1: Enable OSC check trigger global reset. 1'b0: Disable OSC check trigger global reset.
6	RW	0x0	wdt_trig_glbrst_en wdt_trig_glbrst_en 1'b1: Enable WDT trigger global reset. 1'b0: Disable WDT trigger global reset.
5	RO	0x0	reserved
4	RW	0x0	wdt_trig_pmu_en wdt_trig_pmu_en 1'b1: Enable wdt reset trigger pmu reset. 1'b0: Disable wdt reset trigger pmu reset.
3	RW	0x0	glbrst_trig_pmu_en glbrst_trig_pmu_en 1'b1: Enable global reset trigger pmu reset. 1'b0: Disable global reset trigger pmu reset.
2	RW	0x0	glbrst_trig_pmu_sel glbrst_trig_pmu_sel 1'b1: First global reset trigger pmu reset. 1'b0: Second global reset trigger pmu reset.
1	RW	0x0	tsadc_trig_glbrst_en tsadc_trig_glbrst_en 1'b1: Enable tsadc trigger global reset. 1'b0: Disable tsadc trigger global reset.
0	RW	0x0	tsadc_trig_glbrst_sel tsadc_trig_glbrst_sel 1'b1: tsadc trigger first global reset. 1'b0: tsadc trigger second global reset.

CRU_GLBRST_ST_NCLR

Address: Operational Base(0x27200000) + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	glbrst_wdtpmu_rst glbrst_wdtpmu_rst If High, global reset by PMU_WDT. this reg do not have rst value. not clear by rst
14	RW	0x0	glbrst_wdtnpu_rst glbrst_wdtnpu_rst If High, global reset by NPU_WDT. this reg do not have rst value. not clear by rst
13	RW	0x0	glbrst_wdts_rst glbrst_wdts_rst If High, global reset by WDT_S. this reg do not have rst value. not clear by rst
12	RW	0x0	glbrst_wdtns_rst glbrst_wdtns_rst If High, global reset by WDT_NS. this reg do not have rst value. not clear by rst
11	RW	0x0	glbrst_wdtbus_rst glbrst_wdtbus_rst If High, global reset by BUS_WDT. this reg do not have rst value. not clear by rst

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Bit	Attr	Reset Value	Description
10	RW	0x0	glbrst_wdtddr_rst glbrst_wdtddr_rst If High, global reset by DDR_WDT. this reg do not have rst value. not clear by rst
9	RO	0x0	reserved
8	RW	0x0	glbrst_sgrf_crc_chk_rst glbrst_sgrf_crc_chk_rst If High, global reset by PMUSGRF_CRC check. this reg do not have rst value. not clear by rst
7	RW	0x0	glbrst_osc_chk_rst glbrst_osc_chk_rst If High, global reset by OSC check. this reg do not have rst value. not clear by rst
6	RW	0x0	glbrst_wdt_rst glbrst_wdt_rst If High, global reset by WDT. Check CRU_GLBRST_ST[15:11] for detail. this reg do not have rst value. not clear by rst
5	RW	0x0	second_glbrst_wdt_rst second_glbrst_wdt_rst If High, second global reset by WDT. this reg do not have rst value. not clear by rst
4	RW	0x0	first_glbrst_wdt_rst first_glbrst_wdt_rst If High, first global reset by WDT. this reg do not have rst value. not clear by rst
3	RW	0x0	second_glbrst_tsadc_rst second_glbrst_tsadc_rst If High, second global reset by TSADC. this reg do not have rst value. not clear by rst
2	RW	0x0	first_glbrst_tsadc_rst first_glbrst_tsadc_rst If High, first global reset by TSADC. this reg do not have rst value. not clear by rst
1	RW	0x0	second_glbrst_register_rst second_glbrst_register_rst If High, second global reset by register. this reg do not have rst value. not clear by rst
0	RW	0x0	first_glbrst_register_rst first_glbrst_register_rst If High, first global reset by register. this reg do not have rst value. not clear by rst

CRU_CRU_NON_SECURE_GATING_CON00

Address: Operational Base(0x27200000) + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	hclk_trng_s_en_nsctrl clk_pka_crypto_s_en_nsctrl 1'b0: not enable ns gate ctrl; 1'b1: enable ns gate ctrl, use both secure gate_en and non secure gate_en to control clk gating;
2	RW	0x0	aclk_crypto_s_en_nsctrl clk_pka_crypto_s_en_nsctrl 1'b0: not enable ns gate ctrl; 1'b1: enable ns gate ctrl, use both secure gate_en and non secure gate_en to control clk gating;
1	RW	0x0	clk_pka_crypto_s_en_nsctrl clk_pka_crypto_s_en_nsctrl 1'b0: not enable ns gate ctrl; 1'b1: enable ns gate ctrl, use both secure gate_en and non secure gate_en to control clk gating;
0	RO	0x0	reserved

CRU_QCHANNEL_CON01

Address: Operational Base(0x27200000) + offset (0x0CA4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	clk_gpu_qc_gate_en qc_gate_en 1'b1: Enable clk_gpu qchannel gate function. 1'b1: Disable clk_gpu qchannel gate function.
6	RW	0x0	clk_gpu_qc_en qc_en 1'b1: Enable clk_gpu qchannel. 1'b1: Disable clk_gpu qchannel.
5:0	RO	0x00	reserved

CRU_SMOTH_DIVFREE_CON00

Address: Operational Base(0x27200000) + offset (0x0CC0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	clk_rknn_dsu0_freq_keep freq_keep Cycles to keep every step.
15	RW	0x1	clk_rknn_dsu0_bypass bypass Division signal bypass. 1'b1: Bypass. 1'b0: Use Smoothdiv to control clock division.
14	RW	0x1	clk_rknn_dsu0_gate_smth_en gate_smth_en If trigger smoothdiv function when clk been gated. 1'b1: Enable. 1'b0: Disable.

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Bit	Attr	Reset Value	Description
13	RW	0x0	clk_rknn_dsu0_smdiv_clk_off smdiv_clk_off Turn off smoothdiv module clk. 1'b1: Turn off. 1'b0: Turn on.
12:5	RO	0x00	reserved
4:0	RW	0x03	clk_rknn_dsu0_step step Step of div from 0x1f to setting configuration .

CRU_SMOTH_DIVFREE_CON01

Address: Operational Base(0x27200000) + offset (0x0CC4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	aclk_s_gpu_biu_freq_keep freq_keep Cycles to keep every step.
15	RW	0x1	aclk_s_gpu_biu_bypass bypass Division signal bypass. 1'b1: Bypass. 1'b0: Use Smoothdiv to control clock division.
14	RW	0x1	aclk_s_gpu_biu_gate_smth_en gate_smth_en If trigger smoothdiv function when clk been gated. 1'b1: Enable. 1'b0: Disable.
13	RW	0x0	aclk_s_gpu_biu_smdiv_clk_off smdiv_clk_off Turn off smoothdiv module clk. 1'b1: Turn off. 1'b0: Turn on.
12:5	RO	0x00	reserved
4:0	RW	0x03	aclk_s_gpu_biu_step step Step of div from 0x1f to setting configuration .

CRU_SMOTH_DIVFREE_CON02

Address: Operational Base(0x27200000) + offset (0x0CC8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	aclk_m0_gpu_freq_keep freq_keep Cycles to keep every step.
15	RW	0x1	aclk_m0_gpu_bypass bypass Division signal bypass. 1'b1: Bypass. 1'b0: Use Smoothdiv to control clock division.
14	RW	0x1	aclk_m0_gpu_gate_smth_en gate_smth_en If trigger smoothdiv function when clk been gated. 1'b1: Enable. 1'b0: Disable.

Bit	Attr	Reset Value	Description
13	RW	0x0	aclk_m0_gpu_smdiv_clk_off smdiv_clk_off Turn off smoothdiv module clk. 1'b1: Turn off. 1'b0: Turn on.
12:5	RO	0x00	reserved
4:0	RW	0x03	aclk_m0_gpu_step step Step of div from 0x1f to setting configuration .

CRU_HIGH16BIT_AUDIO_FRAC_0

Address: Operational Base(0x27200000) + offset (0x0CD4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	fracdiv_24bit_en if High, enable 24bit frac div. this con is designed for frac divider of clk_matrix_audio_frac_0.
15:8	RW	0x00	numerator_high8bit num_high8bit if enable this fracdiv, numerator = {num_high8bit, num_low16bit}, then numerator is 24bits.
7:0	RW	0x00	denominator_high8bit den_high8bit if enable this fracdiv, denominator = {den_high8bit, den_low16bit}, then denominator is 24bits.

CRU_HIGH16BIT_AUDIO_FRAC_1

Address: Operational Base(0x27200000) + offset (0x0CD8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	fracdiv_24bit_en if High, enable 24bit frac div. this con is designed for frac divider of clk_matrix_audio_frac_1.
15:8	RW	0x00	numerator_high8bit num_high8bit if enable this fracdiv, numerator = {num_high8bit, num_low16bit}, then numerator is 24bits.
7:0	RW	0x00	denominator_high8bit den_high8bit if enable this fracdiv, denominator = {den_high8bit, den_low16bit}, then denominator is 24bits.

CRU_HIGH16BIT_AUDIO_FRAC_2

Address: Operational Base(0x27200000) + offset (0x0CDC)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	fracdiv_24bit_en if High, enable 24bit frac div. this con is designed for frac divider of clk_matrix_audio_frac_2.

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	numerator_high8bit num_high8bit if enable this fracdiv, numerator = {num_high8bit, num_low16bit}, then numerator is 24bits.
7:0	RW	0x00	denominator_high8bit den_high8bit if enable this fracdiv, denominator = {den_high8bit, den_low16bit}, then denominator is 24bits.

CRU_HIGH16BIT_AUDIO_FRAC_3

Address: Operational Base(0x27200000) + offset (0x0CE0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	fracdiv_24bit_en if High, enable 24bit frac div. this con is designed for frac divider of clk_matrix_audio_frac_3.
15:8	RW	0x00	numerator_high8bit num_high8bit if enable this fracdiv, numerator = {num_high8bit, num_low16bit}, then numerator is 24bits.
7:0	RW	0x00	denominator_high8bit den_high8bit if enable this fracdiv, denominator = {den_high8bit, den_low16bit}, then denominator is 24bits.

CRU_AUTOCS_HCLK_TOP_BIU_CON0

Address: Operational Base(0x27200000) + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_TOP_BIU_CON1

Address: Operational Base(0x27200000) + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured

Bit	Attr	Reset Value	Description
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_top control; notes: noc_active_top includes child pd noc active bit1-bit11: reserved;

CRU_AUTOCS_ACLK_BUS_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_BUS_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D24)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_bus control; notes: noc_active_bus includes bus and top noc active bit1: decom_enable control; bit2-bit11: reserved;

CRU_AUTOCS_PCLK_BUS_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D28)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_BUS_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_bus control; notes: noc_active_bus includes bus and top noc active bit1-bit11: reserved;

CRU_AUTOCS_HCLK_RKNN_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D38)

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Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_RKNN_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D3C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg pdpmu auto switch clock selection as source clk 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_npu control; bit1-bit11: reserved;

CRU_AUTOCS_ACLK_NVM_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_NVM_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_nvm control; bit1-bit11: reserved;

CRU_AUTOCS_ACLK_PHP_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D48)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_PHP_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D4C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable

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Bit	Attr	Reset Value	Description
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_php control; bit1-bit11: reserved;

CRU_AUTOCS_ACLK_RKVDEC_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D50)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_RKVDEC_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D54)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_rkvdec control; bit1: rkvdec_acs_idle control; bit2-bit11: reserved;

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CRU_AUTOCS_ACLK_USB_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D68)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_USB_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D6C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_usb control; bit1-bit11: reserved;

CRU_AUTOCS_ACLK_VPU_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D70)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

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CRU_AUTOCS_ACLK_VPU_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D74)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVPUdual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vpu control; bit1: ebc_acs_idle control; bit2: vdpp_acs_idle control; bit3: rga0_acs_idle control; bit4: rga1_acs_idle control; bit5: rkjpeg_acs_idle control; bit6-bit11: reserved;

CRU_AUTOCS_ACLK_VPU_LOW_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D78)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_VPU_LOW_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D7C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVPU_LOWdual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vpu control; bit1: ebc_acs_idle control; bit2: vdpp_acs_idle control; bit3: rga0_acs_idle control; bit4: rga1_acs_idle control; bit5: rkjpeg_acs_idle control; bit6-bit11: reserved;

CRU_AUTOCS_ACLK_JPEG_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D80)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_JPEG_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D84)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiJPEGdual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured

Bit	Attr	Reset Value	Description
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vpu control; bit1: ebc_acs_idle control; bit2: vdpp_acs_idle control; bit3: rga0_acs_idle control; bit4: rga1_acs_idle control; bit5: rkjpeg_acs_idle control; bit6-bit11: reserved;

CRU_AUTOCS_ACLK_VEPU0_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D88)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_VEPU0_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D8C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable

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Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vepu0 control; bit1: vepu0_acs_a_idle control; bit3: vepu0_acs_c_idle control; bit2, bit4-bit11: reserved;

CRU_AUTOCS_ACLK_VI_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0D98)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_VI_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0D9C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vi control; bit1: isp_a_idle control; bit2: isp_c_idle control; bit3: vpss_a_idle control; bit4: vpss_c_idle control; bit5: vicap_isp_c_idle control; bit6: vicap_a_idle control; bit7-bit11: reserved;

CRU_AUTOCS_ACLK_VOP_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0DA0)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_VOP_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0DA4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVOPdual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vop control; bit1: vop_acs_idle control; bit2-bit11: reserved;

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CRU_AUTOCS_ACLK_VPU_MID_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0DB0)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_VPU_MID_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0DB4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVPU_MIDdual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vpu control; bit1: ebc_acs_idle control; bit2: vdpp_acs_idle control; bit3: rga0_acs_idle control; bit4: rga1_acs_idle control; bit5: rkjpeg_acs_idle control; bit6-bit11: reserved;

CRU_AUTOCS_ACLK_TOP_BIU_CON0

Address: Operational Base(0x27200000) + offset (0x0DB8)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16

Bit	Attr	Reset Value	Description
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_TOP_BIU_CON1

Address: Operational Base(0x27200000) + offset (0x0DBC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_top control; notes: noc_active_top includes child pd noc active bit1-bit11: reserved;

CRU_AUTOCS_ACLK_CENTER_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0DE8)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_CENTER_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0DEC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_center control; bit1-bit11: reserved;

CRU_AUTOCS_ACLK_CENTER_LOW_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0DF0)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_CENTER_LOW_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0DF4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable

Bit	Attr	Reset Value	Description
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_center control; bit1-bit11: reserved;

CRU_AUTOCS_HCLK_BUS_CM0_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_BUS_CM0_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E1C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: busmcu_deepsleep control; bit1: busmcu_irq&sgrf_con control; bit2-bit11: reserved;

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CRU_AUTOCS_PCLK_NPUTOP_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_NPUTOP_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_npu control; bit1-bit11: reserved;

CRU_AUTOCS_HCLK_NPU_CM0_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E28)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_NPU_CM0_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E2C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: npumcu_deepsleep control; bit1: npumcu_irq&sgrf_con control; bit2-bit11: reserved;

CRU_AUTOCS_HCLK_NVM_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E30)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_NVM_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E34)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured

Bit	Attr	Reset Value	Description
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_nvm control; bit1-bit11: reserved;

CRU_AUTOCS_PCLK_PHP_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E38)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_PHP_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E3C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_php control; bit1-bit11: reserved;

CRU_AUTOCS_HCLK_RKVDEC_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E48)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_RKVDEC_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E4C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_rkvdec control; bit1: rkvdec_acs_idle control; bit2-bit11: reserved;

CRU_AUTOCS_PCLK_TOP_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E58)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk

Bit	Attr	Reset Value	Description
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_TOP_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E5C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_top control; notes: noc_active_top includes child pd noc active bit1-bit11: reserved;

CRU_AUTOCS_PCLK_USB_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E70)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_USB_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E74)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_usb control; bit1-bit11: reserved;

CRU_AUTOCS_HCLK_VPU_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E78)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_VPU_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E7C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVPUdual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg pdpmu auto switch clock selection as clk_pmu_src 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable

Bit	Attr	Reset Value	Description
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vpu control; bit1: ebc_acs_idle control; bit2: vdpp_acs_idle control; bit3: rga0_acs_idle control; bit4: rga1_acs_idle control; bit5: rkjpeg_acs_idle control; bit6-bit11: reserved;

CRU_AUTOCS_HCLK_VEPU0_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E80)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_VEPU0_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E84)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vepu0 control; bit1: vepu0_acs_a_idle control; bit3: vepu0_acs_c_idle control; bit2, bit4-bit11: reserved;

CRU_AUTOCS_HCLK_VI_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E90)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_VI_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E94)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vi control; bit1: isp_a_idle control; bit2: isp_c_idle control; bit3: vpss_a_idle control; bit4: vpss_c_idle control; bit5: vicap_isp_c_idle control; bit6: vicap_a_idle control; bit7-bit11: reserved;

CRU_AUTOCS_PCLK_VI_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0E98)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_VI_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0E9C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vi control; bit1: isp_a_idle control; bit2: isp_c_idle control; bit3: vpss_a_idle control; bit4: vpss_c_idle control; bit5: vicap_isp_c_idle control; bit6: vicap_a_idle control; bit7-bit11: reserved;

CRU_AUTOCS_HCLK_VOP_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0EA8)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_VOP_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0EAC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVOPdual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vop control; bit1: vop_acs_idle control; bit2-bit11: reserved;

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CRU_AUTOCS_PCLK_VOP_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0EB0)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_VOP_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0EB4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVOPdual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vop control; bit1: vop_acs_idle control; bit2-bit11: reserved;

CRU_AUTOCS_HCLK_VO0_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0EB8)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk

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Bit	Attr	Reset Value	Description
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_VO0_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0EBC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVO0dual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vo0 control; bit1-bit11: reserved;

CRU_AUTOCS_ACLK_TOP_MID_BIU_CON0

Address: Operational Base(0x27200000) + offset (0x0EE0)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_TOP_MID_BIU_CON1

Address: Operational Base(0x27200000) + offset (0x0EE4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_top control; notes: noc_active_top includes child pd noc active bit1-bit11: reserved;

CRU_AUTOCS_PCLK_VO1_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0EE8)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_VO1_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0EEC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVO1dual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable

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Bit	Attr	Reset Value	Description
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vo1 control; bit1-bit11: reserved;

CRU_AUTOCS_HCLK_VO1_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0EF0)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_VO1_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0EF4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVO1dual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vo1 control; bit1-bit11: reserved;

CRU_AUTOCS_HCLK_DDR_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_DDR_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: ddrmcu_deepsleep control; bit1: intmux2ddr&sgrf_con control; bit2-bit11: reserved;

CRU_AUTOCS_PCLK_CENTER_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

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CRU_AUTOCS_PCLK_CENTER_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_center control; bit1-bit11: reserved;

CRU_AUTOCS_ACLK_DDR_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_DDR_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured

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Bit	Attr	Reset Value	Description
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_ddr control; bit1-bit11: reserved;

CRU_AUTOCS_ACLK_VO1_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_VO1_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is indiVO1dual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vo1 control; bit1-bit11: reserved;

CRU_AUTOCS_HCLK_CENTER_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_CENTER_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F24)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_center control; bit1-bit11: reserved;

CRU_AUTOCS_CLK_GPU_INNER_CON0

Address: Operational Base(0x27200000) + offset (0x0F30)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk

Bit	Attr	Reset Value	Description
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_CLK_GPU_INNER_CON1

Address: Operational Base(0x27200000) + offset (0x0F34)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_gpu control; bit1: clk_gpu qchannel active control; bit2-bit11: reserved;

CRU_AUTOCS_HCLK_AUDIO_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F40)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_AUDIO_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F44)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_audio control; bit1-bit11: reserved;

CRU_AUTOCS_PCLK_DDR_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F50)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_PCLK_DDR_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F54)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable

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Bit	Attr	Reset Value	Description
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_ddr control; bit1: ddrmcu_deepsleep control; bit2: intmux2ddr&sgrf_con control; bit3-bit11: reserved;

CRU_AUTOCS_CLK_ISP0_CORE_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F58)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_CLK_ISP0_CORE_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F5C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vi control; bit1: isp_a_idle control; bit2: isp_c_idle control; bit3: vpss_a_idle control; bit4: vpss_c_idle control; bit5: vicap_isp_c_idle control; bit6: vicap_a_idle control; bit7-bit11: reserved;

CRU_AUTOCS_CLK_VEPU0_CORE_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F60)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_CLK_VEPU0_CORE_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F64)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: vepu0_acs_c_idle control; bit2-bit11: reserved;

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CRU_AUTOCS_ACLK_VEPU1_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F68)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_ACLK_VEPU1_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F6C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vepu1 control; bit1: vepu1_acs_a_idle control; bit3: vepu1_acs_c_idle control; bit2, bit4-bit11: reserved;

CRU_AUTOCS_HCLK_VEPU1_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F70)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk

Bit	Attr	Reset Value	Description
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_HCLK_VEPU1_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F74)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vepu1 control; bit1: vepu1_acs_a_idle control; bit3: vepu1_acs_c_idle control; bit2, bit4-bit11: reserved;

CRU_AUTOCS_CLK_VEPU1_CORE_ROOT_CON0

Address: Operational Base(0x27200000) + offset (0x0F78)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CRU_AUTOCS_CLK_VEPU1_CORE_ROOT_CON1

Address: Operational Base(0x27200000) + offset (0x0F7C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: vepu1_acs_c_idle control; bit2-bit11: reserved;

2.5 PPLL_CRU

2.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.5.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PHPTOPCRU_PPLL_CON0	0x0200	W	0x00000145	PPLL configuration register 0
PHPTOPCRU_PPLL_CON1	0x0204	W	0x000000C3	PPLL configuration register 1
PHPTOPCRU_PPLL_CON2	0x0208	W	0x00000000	PPLL configuration register 2
PHPTOPCRU_PPLL_CON3	0x020C	W	0x00000000	PPLL configuration register 3
PHPTOPCRU_PPLL_CON4	0x0210	W	0x00000000	PPLL configuration register 4
PHPTOPCRU_PPLL_CON5	0x0214	W	0x00000000	PPLL configuration register 5
PHPTOPCRU_PPLL_CON6	0x0218	W	0x00000000	PPLL configuration register 6
PHPTOPCRU_CLKSEL_CON00	0x0300	W	0x00000630	Internal clock select and division register 0
PHPTOPCRU_CLKSEL_CON01	0x0304	W	0x00000031	Internal clock select and division register 1
PHPTOPCRU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
PHPTOPCRU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
PHPTOPCRU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
PHPTOPCRU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.5.3 Detail Registers Description

PHPTOPCRU_PPLL_CON0

Address: Operational Base(0x27208000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	ppll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x145	ppll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

PHPTOPCRU_PPLL_CON1

Address: Operational Base(0x27208000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	ppll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x3	ppll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x03	ppll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

PHPTOPCRU_PPLL_CON2

Address: Operational Base(0x27208000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ppll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

PHPTOPCRU_PPLL_CON3

Address: Operational Base(0x27208000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	ppll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.
13:8	RW	0x00	ppll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	ppll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

PHPTOPCRU_PPLL_CON4

Address: Operational Base(0x27208000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	ppll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	ppll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	ppll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	ppll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	ppll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

PHPTOPCRU_PPLL_CON5

Address: Operational Base(0x27208000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	ppll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

PHPTOPCRU_PPLL_CON6

Address: Operational Base(0x27208000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	ppll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	ppll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

PHPTOPCRU_CLKSEL_CON00

Address: Operational Base(0x27208000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_ref_pcie1_inner_phy_sel clk_ref_pcie1_inner_phy clock mux. 2'b00: clk_matrix_pcie_100m_src 2'b01: clk_matrix_pcie_100m_nduty_src 2'b10: xin_osc0_pll
13:12	RW	0x0	clk_ref_pcie0_inner_phy_sel clk_ref_pcie0_inner_phy clock mux. 2'b00: clk_matrix_pcie_100m_src 2'b01: clk_matrix_pcie_100m_nduty_src 2'b10: xin_osc0_pll
11:7	RW	0x0c	clk_matrix_pcie_100m_nduty_src_div Divide clk_matrix_pcie_100m_nduty_src by (div_con + 1).
6:2	RW	0x0c	clk_matrix_pcie_100m_src_div DT50 division register. Divide clk_matrix_pcie_100m_src by (div_con + 1).
1:0	RO	0x0	reserved

PHPTOPCRU_CLKSEL_CON01

Address: Operational Base(0x27208000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:0	RW	0x31	clk_ref_mphy_26m_div Divide clk_ref_mphy_26m by (div_con + 1).

PHPTOPCRU_GATE_CON00

Address: Operational Base(0x27208000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pclk_pcie2_combophy1_grf_en pclk_pcie2_combophy1_grf clock gating control. When high, disable clock
7	RW	0x0	pclk_pcie2_combophy1_en pclk_pcie2_combophy1 clock gating control. When high, disable clock
6	RW	0x0	pclk_pcie2_combophy0_grf_en pclk_pcie2_combophy0_grf clock gating control. When high, disable clock
5	RW	0x0	pclk_pcie2_combophy0_en pclk_pcie2_combophy0 clock gating control. When high, disable clock
4	RO	0x0	reserved
3	RW	0x0	pclk_apb2asb_slv_chip_top_en pclk_apb2asb_slv_chip_top clock gating control. When high, disable clock
2	RW	0x0	pclk_phpphy_root_en pclk_phpphy_root clock gating control. When high, disable clock
1	RW	0x0	pclk_phpphy_cru_en pclk_phpphy_cru clock gating control. When high, disable clock
0	RO	0x0	reserved

PHPTOPCRU_GATE_CON01

Address: Operational Base(0x27208000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	clk_ref_mphy_26m_en clk_ref_mphy_26m clock gating control. When high, disable clock
8	RW	0x0	clk_ref_pcie1_inner_en clk_ref_pcie1_inner_phy clock gating control. When high, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	clk_ref_pcie0_inner_en clk_ref_pcie0_inner_phy clock gating control. When high, disable clock
4:3	RO	0x0	reserved
2	RW	0x0	clk_matrix_pcie_100m_nduty_src_en clk_matrix_pcie_100m_nduty_src clock gating control. When high, disable clock
1	RW	0x0	clk_matrix_pcie_100m_src_en clk_matrix_pcie_100m_src clock gating control. When high, disable clock
0	RO	0x0	reserved

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PHPTOPCRU_SOFTRST_CON00

Address: Operational Base(0x27208000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	presetn_pcie2_combophy1_grf When high, reset relative logic
7	RW	0x0	presetn_pcie2_combophy1 When high, reset relative logic
6	RW	0x0	presetn_pcie2_combophy0_grf When high, reset relative logic
5	RW	0x0	presetn_pcie2_combophy0 When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	presetn_apb2asb_slv_chip_top When high, reset relative logic
2	RO	0x0	reserved
1	RW	0x0	presetn_phpphy_cru When high, reset relative logic
0	RO	0x0	reserved

PHPTOPCRU_SOFTRST_CON01

Address: Operational Base(0x27208000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	resetn_pcie1_pipe_phy When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	resetn_pcie0_pipe_phy When high, reset relative logic
4:0	RO	0x00	reserved

2.6 SECURE_CRU

2.6.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.6.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SECURECRU_CLKSEL_CON00	0x0300	W	0x00000000	Internal clock select and division register 0
SECURECRU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
SECURECRU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0

Name	Offset	Size	Reset Value	Description
SECURECRU_AUTOCS_HCLK_SECURE_NS_ROOT_CON0	0x0D08	W	0x00200047	auto clock switch control 0
SECURECRU_AUTOCS_HCLK_SECURE_NS_ROOT_CON1	0x0D0C	W	0x00000000	auto clock switch control 1
SECURECRU_AUTOCS_PCLK_SECURE_NS_ROOT_CON0	0x0DE0	W	0x00200047	auto clock switch control 0
SECURECRU_AUTOCS_PCLK_SECURE_NS_ROOT_CON1	0x0DE4	W	0x00000000	auto clock switch control 1
SECURECRU_CLKSEL_CON10	0x4000	W	0x00000349	Internal clock select and division register 10
SECURECRU_CLKSEL_CON11	0x4004	W	0x000006C0	Internal clock select and division register 11
SECURECRU_CLKSEL_CON14	0x4010	W	0x00000000	Internal clock select and division register 14
SECURECRU_CLKSEL_CON16	0x4018	W	0x00000000	Internal clock select and division register 16
SECURECRU_GATE_CON10	0x4028	W	0x00000000	Internal clock gate and division register 10
SECURECRU_GATE_CON11	0x402C	W	0x00000000	Internal clock gate and division register 11
SECURECRU_GATE_CON12	0x4030	W	0x00000000	Internal clock gate and division register 12
SECURECRU_GATE_CON13	0x4034	W	0x00000000	Internal clock gate and division register 13
SECURECRU_GATE_CON14	0x4038	W	0x00000000	Internal clock gate and division register 14
SECURECRU_GATE_CON15	0x403C	W	0x00000000	Internal clock gate and division register 15
SECURECRU_SOFTRST_CON10	0x4050	W	0x00000000	Internal clock reset register 10
SECURECRU_SOFTRST_CON11	0x4054	W	0x00000000	Internal clock reset register 11
SECURECRU_SOFTRST_CON12	0x4058	W	0x00000000	Internal clock reset register 12
SECURECRU_SOFTRST_CON13	0x405C	W	0x00000000	Internal clock reset register 13
SECURECRU_SOFTRST_CON14	0x4060	W	0x00000000	Internal clock reset register 14
SECURECRU_SOFTRST_CON15	0x4064	W	0x00000000	Internal clock reset register 15
SECURECRU_SPLL_CON0	0x4220	W	0x0000015F	SPLL configuration register 0
SECURECRU_SPLL_CON1	0x4224	W	0x000000C3	SPLL configuration register 1
SECURECRU_SPLL_CON4	0x4230	W	0x00000002	SPLL configuration register 4
SECURECRU_SPLL_CON5	0x4234	W	0x000007E0	SPLL configuration register 5
SECURECRU_SPLL_CON6	0x4238	W	0x00000000	SPLL configuration register 6
SECURECRU_MODE_CON00	0x4280	W	0x00000000	Internal clock select and division register 0
SECURECRU_AUTOCS_ACLK_SECURE_S_ROOT_CON0	0x4D10	W	0x00200047	auto clock switch control 0

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Name	Offset	Size	Reset Value	Description
SECURECRU_AUTOCS_ACLK_SECURE_S_ROOT_CON1	0x4D14	W	0x00000000	auto clock switch control 1
SECURECRU_AUTOCS_HCLK_SECURE_S_ROOT_CON0	0x4D18	W	0x00200047	auto clock switch control 0
SECURECRU_AUTOCS_HCLK_SECURE_S_ROOT_CON1	0x4D1C	W	0x00000000	auto clock switch control 1
SECURECRU_AUTOCS_PCLK_SECURE_S_ROOT_CON0	0x4D20	W	0x00200047	auto clock switch control 0
SECURECRU_AUTOCS_PCLK_SECURE_S_ROOT_CON1	0x4D24	W	0x00000000	auto clock switch control 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.6.3 Detail Registers Description

SECURECRU_CLKSEL_CON00

Address: Operational Base(0x27210000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	pclk_secure_ns_root_sel pclk_secure_ns_root clock mux. 2'b00: clk_matrix_sec_116m_src 2'b01: clk_matrix_sec_58m_src 2'b10: xin_osc0_func
3:2	RW	0x0	hclk_secure_ns_root_sel hclk_secure_ns_root clock mux. 2'b00: clk_matrix_sec_175m_src 2'b01: clk_matrix_sec_116m_src 2'b10: clk_matrix_sec_58m_src 2'b11: xin_osc0_func
1:0	RW	0x0	aclk_secure_ns_root_sel aclk_secure_ns_root clock mux. 2'b00: clk_matrix_sec_350m_src 2'b01: clk_matrix_sec_175m_src 2'b10: clk_matrix_sec_116m_src 2'b11: xin_osc0_func

SECURECRU_GATE_CON00

Address: Operational Base(0x27210000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_otpc_ns_en clk_otpc_ns clock gating control. When high, disable clock
8	RW	0x0	pclk_otpc_ns_en pclk_otpc_ns clock gating control. When high, disable clock
7	RW	0x0	hclk_secure_ns_biu_en hclk_secure_ns_biu clock gating control. When high, disable clock
6	RW	0x0	aclk_secure_ns_biu_en aclk_secure_ns_biu clock gating control. When high, disable clock
5	RW	0x0	pclk_secure_ns_biu_en pclk_secure_ns_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_trng_ns_en hclk_trng_ns clock gating control. When high, disable clock
3	RW	0x0	hclk_crypto_ns_en hclk_crypto_ns clock gating control. When high, disable clock
2	RW	0x0	pclk_secure_ns_root_en pclk_secure_ns_root clock gating control. When high, disable clock
1	RW	0x0	hclk_secure_ns_root_en hclk_secure_ns_root clock gating control. When high, disable clock
0	RW	0x0	aclk_secure_ns_root_en aclk_secure_ns_root clock gating control. When high, disable clock

SECURECRU_SOFTRST_CON00

Address: Operational Base(0x27210000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	resetn_otpc_ns When high, reset relative logic
8	RW	0x0	presetn_otpc_ns When high, reset relative logic
7	RW	0x0	hresetn_secure_ns_biu When high, reset relative logic
6	RW	0x0	aresetn_secure_ns_biu When high, reset relative logic
5	RW	0x0	presetn_secure_ns_biu When high, reset relative logic
4	RW	0x0	hresetn_trng_ns When high, reset relative logic
3	RW	0x0	hresetn_crypto_ns When high, reset relative logic
2:0	RO	0x0	reserved

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SECURECRU_AUTOCS_HCLK_SECURE_NS_ROOT_CON0

Address: Operational Base(0x27210000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

SECURECRU_AUTOCS_HCLK_SECURE_NS_ROOT_CON1

Address: Operational Base(0x27210000) + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: vepu0_acs_c_idle control; bit2-bit11: reserved;

SECURECRU_AUTOCS_PCLK_SECURE_NS_ROOT_CON0

Address: Operational Base(0x27210000) + offset (0x0DE0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

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SECURECRU_AUTOCS_PCLK_SECURE_NS_ROOT_CON1

Address: Operational Base(0x27210000) + offset (0x0DE4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_vepu1 control; bit1: vepu1_acs_a_idle control; bit3: vepu1_acs_c_idle control; bit2, bit4-bit11: reserved;

SECURECRU_CLKSEL_CON10

Address: Operational Base(0x27210000) + offset (0x4000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:9	RW	0x1	clk_matrix_sec_175m_src_div Divide clk_matrix_sec_175m_src by (div_con + 1).
8:6	RW	0x5	clk_matrix_sec_116m_src_div Divide clk_matrix_sec_116m_src by (div_con + 1).
5:3	RW	0x1	clk_matrix_sec_58m_src_div Divide clk_matrix_sec_58m_src by (div_con + 1).
2:0	RW	0x1	clk_matrix_sec_350m_src_div Divide clk_matrix_sec_350m_src by (div_con + 1).

SECURECRU_CLKSEL_CON11

Address: Operational Base(0x27210000) + offset (0x4004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:11	RW	0x0	clk_pka_crypto_s_sel clk_pka_crypto_s clock mux. 2'b00: clk_matrix_sec_350m_src 2'b01: clk_matrix_sec_175m_src 2'b10: clk_matrix_sec_116m_src 2'b11: xin_osc0_func
10:8	RW	0x6	clk_matrix_sec_100m_src_div Divide clk_matrix_sec_100m_src by (div_con + 1).
7	RW	0x1	clk_stimer1_root_sel clk_stimer1_root clock mux. 1'b0: clk_matrix_sec_100m_src 1'b1: xin_osc0_func
6	RW	0x1	clk_stimer0_root_sel clk_stimer0_root clock mux. 1'b0: clk_matrix_sec_100m_src 1'b1: xin_osc0_func
5:4	RW	0x0	pclk_secure_s_root_sel pclk_secure_s_root clock mux. 2'b00: clk_matrix_sec_116m_src 2'b01: clk_matrix_sec_58m_src 2'b10: xin_osc0_func
3:2	RW	0x0	hclk_secure_s_root_sel hclk_secure_s_root clock mux. 2'b00: clk_matrix_sec_175m_src 2'b01: clk_matrix_sec_116m_src 2'b10: clk_matrix_sec_58m_src 2'b11: xin_osc0_func
1:0	RW	0x0	aclk_secure_s_root_sel aclk_secure_s_root clock mux. 2'b00: clk_matrix_sec_350m_src 2'b01: clk_matrix_sec_175m_src 2'b10: clk_matrix_sec_116m_src 2'b11: xin_osc0_func

SECURECRU_CLKSEL_CON14

Address: Operational Base(0x27210000) + offset (0x4010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	hclk_vo1_s_root_sel hclk_vo1_s_root clock mux. 2'b00: clk_matrix_sec_175m_src 2'b01: clk_matrix_sec_116m_src 2'b10: clk_matrix_sec_58m_src 2'b11: xin_osc0_func

SECURECRU_CLKSEL_CON16

Address: Operational Base(0x27210000) + offset (0x4018)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x0	pclk_vo0_s_root_sel pclk_vo0_s_root clock mux. 2'b00: clk_matrix_sec_116m_src 2'b01: clk_matrix_sec_58m_src 2'b10: xin_osc0_func
1:0	RW	0x0	hclk_vo0_s_root_sel hclk_vo0_s_root clock mux. 2'b00: clk_matrix_sec_175m_src 2'b01: clk_matrix_sec_116m_src 2'b10: clk_matrix_sec_58m_src 2'b11: xin_osc0_func

SECURECRU_GATE_CON10

Address: Operational Base(0x27210000) + offset (0x4028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_stimer4_en clk_stimer4 clock gating control. When high, disable clock
14	RW	0x0	clk_stimer3_en clk_stimer3 clock gating control. When high, disable clock
13	RW	0x0	clk_stimer2_en clk_stimer2 clock gating control. When high, disable clock
12	RW	0x0	clk_stimer1_en clk_stimer1 clock gating control. When high, disable clock
11	RW	0x0	clk_stimer0_en clk_stimer0 clock gating control. When high, disable clock
10	RW	0x0	pclk_stimer0_en pclk_stimer0 clock gating control. When high, disable clock
9	RW	0x0	clk_bus_stimer0_root_en clk_stimer0_root clock gating control. When high, disable clock
8	RW	0x0	pclk_secure_s_root_en pclk_secure_s_root clock gating control. When high, disable clock
7	RW	0x0	hclk_secure_s_root_en hclk_secure_s_root clock gating control. When high, disable clock
6	RW	0x0	aclk_secure_s_root_en aclk_secure_s_root clock gating control. When high, disable clock
5:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	clk_matrix_sec_175m_src_en clk_matrix_sec_175m_src clock gating control. When high, disable clock
2	RW	0x0	clk_matrix_sec_116m_src_en clk_matrix_sec_116m_src clock gating control. When high, disable clock
1	RW	0x0	clk_matrix_sec_58m_src_en clk_matrix_sec_58m_src clock gating control. When high, disable clock
0	RW	0x0	clk_matrix_sec_350m_src_en clk_matrix_sec_350m_src clock gating control. When high, disable clock

SECURECRU_GATE_CON11

Address: Operational Base(0x27210000) + offset (0x402C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pclk_dft2apb_en pclk_dft2apb clock gating control. When high, disable clock
13	RW	0x0	pclk_sys_sgrf_en pclk_sys_sgrf clock gating control. When high, disable clock
12	RW	0x0	clk_stimer11_en clk_stimer11 clock gating control. When high, disable clock
11	RW	0x0	clk_stimer10_en clk_stimer10 clock gating control. When high, disable clock
10	RW	0x0	clk_stimer9_en clk_stimer9 clock gating control. When high, disable clock
9	RW	0x0	clk_stimer8_en clk_stimer8 clock gating control. When high, disable clock
8	RW	0x0	clk_stimer7_en clk_stimer7 clock gating control. When high, disable clock
7	RW	0x0	clk_stimer6_en clk_stimer6 clock gating control. When high, disable clock
6:5	RO	0x0	reserved
4	RW	0x0	pclk_otpmask_en pclk_otpmask clock gating control. When high, disable clock
3	RW	0x0	clk_matrix_sec_100m_src_en clk_matrix_sec_100m_src clock gating control. When high, disable clock
2	RW	0x0	pclk_stimer1_en pclk_stimer1 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	clk_stimer1_root_en clk_stimer1_root clock gating control. When high, disable clock
0	RW	0x0	clk_stimer5_en clk_stimer5 clock gating control. When high, disable clock

SECURECRU_GATE_CON12

Address: Operational Base(0x27210000) + offset (0x4030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	aclk_crypto_s_en aclk_crypto_s clock gating control. When high, disable clock
11	RW	0x0	clk_pka_crypto_s_en clk_pka_crypto_s clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	hclk_klad_en hclk_klad clock gating control. When high, disable clock
8	RW	0x0	hclk_crypto_s_en hclk_crypto_s clock gating control. When high, disable clock
7	RW	0x0	pclk_klad_en pclk_klad clock gating control. When high, disable clock
6	RW	0x0	pclk_secure_s_biu_en pclk_secure_s_biu clock gating control. When high, disable clock
5	RW	0x0	hclk_secure_s_biu_en hclk_secure_s_biu clock gating control. When high, disable clock
4	RW	0x0	aclk_secure_s_biu_en aclk_secure_s_biu clock gating control. When high, disable clock
3:0	RO	0x0	reserved

SECURECRU_GATE_CON13

Address: Operational Base(0x27210000) + offset (0x4034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	tclk_wdt_s_en tclk_wdt_s clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
9	RW	0x0	pclk_wdt_s_en pclk_wdt_s clock gating control. When high, disable clock
8	RW	0x0	pclk_secure_cru_en pclk_secure_cru clock gating control. When high, disable clock
7	RW	0x0	clk_jdbck_dap_en clk_jdbck_dap clock gating control. When high, disable clock
6	RW	0x0	pclk_jdbck_dap_en pclk_jdbck_dap clock gating control. When high, disable clock
5	RW	0x0	hclk_bootrom_en hclk_bootrom clock gating control. When high, disable clock
4	RW	0x0	clk_otpc_s_en clk_otpc_s clock gating control. When high, disable clock
3	RW	0x0	pclk_otpc_s_en pclk_otpc_s clock gating control. When high, disable clock
2:1	RO	0x0	reserved
0	RW	0x0	hclk_trng_s_en hclk_trng_s clock gating control. When high, disable clock

SECURECRU_GATE_CON14

Address: Operational Base(0x27210000) + offset (0x4038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	hclk_hdcp_key1_en hclk_hdcp_key1 clock gating control. When high, disable clock
2	RW	0x0	hclk_vo1_s_biu_en hclk_vo1_s_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_vo1_s_root_en hclk_vo1_s_root clock gating control. When high, disable clock
0	RW	0x0	pclk_hdcp1_trng_en pclk_hdcp1_trng clock gating control. When high, disable clock

SECURECRU_GATE_CON15

Address: Operational Base(0x27210000) + offset (0x403C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	pclk_edp_biu_en pclk_edp_biu clock gating control. When high, disable clock
5	RW	0x0	pclk_edp_s_en pclk_edp_s clock gating control. When high, disable clock
4	RW	0x0	pclk_vo0_s_root_en pclk_vo0_s_root clock gating control. When high, disable clock
3	RW	0x0	hclk_hdcp_key0_en hclk_hdcp_key0 clock gating control. When high, disable clock
2	RW	0x0	hclk_vo0_s_biu_en hclk_vo0_s_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_vo0_s_root_en hclk_vo0_s_root clock gating control. When high, disable clock
0	RW	0x0	pclk_hdcp0_trng_en pclk_hdcp0_trng clock gating control. When high, disable clock

SECURECRU_SOFTRST_CON10

Address: Operational Base(0x27210000) + offset (0x4050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_stimer4 When high, reset relative logic
14	RW	0x0	resetn_stimer3 When high, reset relative logic
13	RW	0x0	resetn_stimer2 When high, reset relative logic
12	RW	0x0	resetn_stimer1 When high, reset relative logic
11	RW	0x0	resetn_stimer0 When high, reset relative logic
10	RW	0x0	presetn_stimer0 When high, reset relative logic
9:0	RO	0x000	reserved

SECURECRU_SOFTRST_CON11

Address: Operational Base(0x27210000) + offset (0x4054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	presetn_dft2apb When high, reset relative logic
13	RW	0x0	presetn_sys_sgrf When high, reset relative logic

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Bit	Attr	Reset Value	Description
12	RW	0x0	resetn_stimer11 When high, reset relative logic
11	RW	0x0	resetn_stimer10 When high, reset relative logic
10	RW	0x0	resetn_stimer9 When high, reset relative logic
9	RW	0x0	resetn_stimer8 When high, reset relative logic
8	RW	0x0	resetn_stimer7 When high, reset relative logic
7	RW	0x0	resetn_stimer6 When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	resetn_otpmask When high, reset relative logic
4	RW	0x0	presetn_otpmask When high, reset relative logic
3	RO	0x0	reserved
2	RW	0x0	presetn_stimer1 When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	resetn_stimer5 When high, reset relative logic

SECURECRU_SOFTRST_CON12

Address: Operational Base(0x27210000) + offset (0x4058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	aresetn_crypto_s When high, reset relative logic
11	RW	0x0	resetn_pka_crypto_s When high, reset relative logic
10	RO	0x0	reserved
9	RW	0x0	hresetn_klad When high, reset relative logic
8	RW	0x0	hresetn_crypto_s When high, reset relative logic
7	RW	0x0	presetn_klad When high, reset relative logic
6	RW	0x0	presetn_secure_s_biu When high, reset relative logic
5	RW	0x0	hresetn_secure_s_biu When high, reset relative logic
4	RW	0x0	aresetn_secure_s_biu When high, reset relative logic
3:2	RO	0x0	reserved
1	RW	0x0	resetn_otpc_arb When high, reset relative logic
0	RO	0x0	reserved

SECURECRU_SOFTRST_CON13

Address: Operational Base(0x27210000) + offset (0x405C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	tresetn_wdt_s When high, reset relative logic
9	RW	0x0	presetn_wdt_s When high, reset relative logic
8	RW	0x0	presetn_secure_cru When high, reset relative logic
7	RW	0x0	resetn_jdbck_dap When high, reset relative logic
6	RW	0x0	presetn_jdbck_dap When high, reset relative logic
5	RW	0x0	hresetn_bootrom When high, reset relative logic
4	RW	0x0	resetn_otpc_s When high, reset relative logic
3	RW	0x0	presetn_otpc_s When high, reset relative logic
2:1	RO	0x0	reserved
0	RW	0x0	hresetn_trng_s When high, reset relative logic

SECURECRU_SOFTRST_CON14

Address: Operational Base(0x27210000) + offset (0x4060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	hresetn_hdcp_key1 When high, reset relative logic
2	RW	0x0	hresetn_vo1_s_biu When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	presetn_hdcp1_trng When high, reset relative logic

SECURECRU_SOFTRST_CON15

Address: Operational Base(0x27210000) + offset (0x4064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	presetn_edp_biu When high, reset relative logic
5	RW	0x0	presetn_edp_s When high, reset relative logic
4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	hresetn_hdcp_key0 When high, reset relative logic
2	RW	0x0	hresetn_vo0_s_biu When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	presetn_hdcp0_trng When high, reset relative logic

SECURECRU_SPLL_CON0

Address: Operational Base(0x27210000) + offset (0x4220)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	spll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x15f	spll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

SECURECRU_SPLL_CON1

Address: Operational Base(0x27210000) + offset (0x4224)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	spll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x3	spll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x03	spll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

SECURECRU_SPLL_CON4

Address: Operational Base(0x27210000) + offset (0x4230)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	spll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	spll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	spll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	spll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RW	0x1	spll_icp Charge-pump current control signal.
0	RO	0x0	reserved

SECURECRU_SPLL_CON5

Address: Operational Base(0x27210000) + offset (0x4234)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:9	RW	0x3	spll_lock_con_dly LOCK_CON_DLY: Lock detector setting of the detection resolution.
8:7	RW	0x3	spll_lock_con_out LOCK_CON_OUT: Lock detector setting of the output margin.
6:5	RW	0x3	spll_lock_con_in LOCK_CON_IN: Lock detector setting of the input margin.
4:1	RO	0x0	reserved
0	RW	0x0	spll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

SECURECRU_SPLL_CON6

Address: Operational Base(0x27210000) + offset (0x4238)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	spll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	spll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

SECURECRU_MODE_CON00

Address: Operational Base(0x27210000) + offset (0x4280)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	clk_spll_mode clk_spll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_spll 2'b10: clk_deepslow

SECURECRU_AUTOCS_ACLK_SECURE_S_ROOT_CON0

Address: Operational Base(0x27210000) + offset (0x4D10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

SECURECRU_AUTOCS_ACLK_SECURE_S_ROOT_CON1

Address: Operational Base(0x27210000) + offset (0x4D14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_secure control; bit1: crypto_idle control; bit2-bit11: reserved;

SECURECRU_AUTOCS_HCLK_SECURE_S_ROOT_CON0

Address: Operational Base(0x27210000) + offset (0x4D18)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

SECURECRU_AUTOCS_HCLK_SECURE_S_ROOT_CON1

Address: Operational Base(0x27210000) + offset (0x4D1C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_secure control; bit1: crypto_idle control; bit2-bit11: reserved;

SECURECRU_AUTOCS_PCLK_SECURE_S_ROOT_CON0

Address: Operational Base(0x27210000) + offset (0x4D20)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

SECURECRU_AUTOCS_PCLK_SECURE_S_ROOT_CON1

Address: Operational Base(0x27210000) + offset (0x4D24)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_secure control; bit1: crypto_idle control; bit2-bit11: reserved;

2.7 PMU1_CRU

2.7.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.7.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU1CRU_CLKSEL_CON00	0x0300	W	0x00000013	Internal clock select and division register 0
PMU1CRU_CLKSEL_CON03	0x030C	W	0x00000000	Internal clock select and division register 3
PMU1CRU_CLKSEL_CON04	0x0310	W	0x00004090	Internal clock select and division register 4

Name	Offset	Size	Reset Value	Description
PMU1CRU_CLKSEL_CON05	0x0314	W	0x00000009	Internal clock select and division register 5
PMU1CRU_CLKSEL_CON06	0x0318	W	0x00000000	Internal clock select and division register 6
PMU1CRU_CLKSEL_CON08	0x0320	W	0x00000001	Internal clock select and division register 8
PMU1CRU_CLKSEL_CON11	0x032C	W	0x00000040	Internal clock select and division register 11
PMU1CRU_CLKSEL_CON20	0x0350	W	0x00000000	Internal clock select and division register 20
PMU1CRU_CLKSEL_CON21	0x0354	W	0x0040B71B	Internal clock select and division register 21
PMU1CRU_GATE_CON00	0x0800	W	0x00002000	Internal clock gate and division register 0
PMU1CRU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
PMU1CRU_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2
PMU1CRU_GATE_CON03	0x080C	W	0x00000000	Internal clock gate and division register 3
PMU1CRU_GATE_CON04	0x0810	W	0x00000000	Internal clock gate and division register 4
PMU1CRU_GATE_CON05	0x0814	W	0x00000000	Internal clock gate and division register 5
PMU1CRU_GATE_CON06	0x0818	W	0x00000000	Internal clock gate and division register 6
PMU1CRU_GATE_CON07	0x081C	W	0x00000000	Internal clock gate and division register 7
PMU1CRU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
PMU1CRU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1
PMU1CRU_SOFTRST_CON02	0x0A08	W	0x00000000	Internal clock reset register 2
PMU1CRU_SOFTRST_CON03	0x0A0C	W	0x00001000	Internal clock reset register 3
PMU1CRU_SOFTRST_CON04	0x0A10	W	0x00000000	Internal clock reset register 4
PMU1CRU_SOFTRST_CON05	0x0A14	W	0x00000000	Internal clock reset register 5
PMU1CRU_SOFTRST_CON06	0x0A18	W	0x00000000	Internal clock reset register 6
PMU1CRU_SOFTRST_CON07	0x0A1C	W	0x00000000	Internal clock reset register 7
PMU1CRU_AUTOCS_PCLK_PMU0_ROOT_SRC_CON0	0x0B00	W	0x00200047	auto clock switch control 0
PMU1CRU_AUTOCS_PCLK_PMU0_ROOT_SRC_CON1	0x0B04	W	0x00000000	auto clock switch control 1
PMU1CRU_AUTOCS_HCLK_PMU1_ROOT_SRC_CON0	0x0B08	W	0x00200047	auto clock switch control 0
PMU1CRU_AUTOCS_HCLK_PMU1_ROOT_SRC_CON1	0x0B0C	W	0x00000000	auto clock switch control 1

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Name	Offset	Size	Reset Value	Description
PMU1CRU_AUTOCS_HCLK_PMU_CM0_ROOT_SRC_CON0	0x0B10	W	0x00200047	auto clock switch control 0
PMU1CRU_AUTOCS_HCLK_PMU_CM0_ROOT_SRC_CON1	0x0B14	W	0x00000000	auto clock switch control 1
PMU1CRU_DEEPSLOW_DETECT_CON	0x0B40	W	0x00000000	Deepslow detect register
PMU1CRU_DEEPSLOW_DETECT_ST	0x0B44	W	0x00000000	Deepslow detect register
PMU1CRU_CLKSEL_CON30	0x4000	W	0x00000000	Internal clock select and division register 30
PMU1CRU_CLKSEL_CON32	0x4008	W	0x00000000	Internal clock select and division register 32
PMU1CRU_GATE_CON10	0x4028	W	0x00000000	Internal clock gate and division register 10
PMU1CRU_GATE_CON12	0x4030	W	0x00000000	Internal clock gate and division register 12
PMU1CRU_SOFTRST_CON10	0x4050	W	0x00000000	Internal clock reset register 10
PMU1CRU_SOFTRST_CON12	0x4058	W	0x00000000	Internal clock reset register 12

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.7.3 Detail Registers Description

PMU1CRU_CLKSEL_CON00

Address: Operational Base(0x27220000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x13	clk_pmuphy_ref_src_div Divide clk_pmuphy_ref_src by (div_con + 1).

PMU1CRU_CLKSEL_CON03

Address: Operational Base(0x27220000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	clk_ref_osc_mphy_sel clk_ref_osc_mphy clock mux. 2'b00: xin_osc0_pll 2'b01: clk_gpio_mphy 2'b10: clk_ref_mphy_26m

PMU1CRU_CLKSEL_CON04

Address: Operational Base(0x27220000) + offset (0x0310)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	tclk_pmu1wdt_sel tclk_pmu1wdt clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
14	RW	0x1	clk_pmu_cm0_rtc_sel clk_pmu_cm0_rtc clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
13:9	RW	0x00	clk_pmu_cm0_rtc_div Divide clk_pmu_cm0_rtc by (div_con + 1).
8:4	RW	0x09	clk_cpll_div10_pmu_src_div Divide clk_cpll_div10_pmu_src by (div_con + 1).
3:2	RW	0x0	hclk_pmu_cm0_root_src_sel hclk_pmu_cm0_root_src clock mux. 2'b00: clk_gpll_div6_pmu_src 2'b01: clk_cpll_div10_pmu_src 2'b10: clk_cpll_div20_pmu_src 2'b11: xin_osc0_func
1:0	RW	0x0	hclk_pmu1_root_src_sel hclk_pmu1_root_src clock mux. 2'b00: clk_gpll_div6_pmu_src 2'b01: clk_cpll_div10_pmu_src 2'b10: clk_cpll_div20_pmu_src 2'b11: xin_osc0_func

PMU1CRU_CLKSEL_CON05

Address: Operational Base(0x27220000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x2	clk_pwm0_sel clk_pwm0 clock mux. 2'b00: clk_cpll_div10_pmu_src 2'b01: clk_cpll_div20_pmu_src 2'b10: xin_osc0_func
1:0	RW	0x1	clk_pmutimer_root_sel clk_pmutimer_root clock mux. 2'b00: clk_cpll_div10_pmu_src 2'b01: xin_osc0_func 2'b10: clk_deepslow

PMU1CRU_CLKSEL_CON06

Address: Operational Base(0x27220000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved
8:7	RW	0x0	clk_i2c0_sel clk_i2c0 clock mux. 2'b00: clk_gpll_div6_pmu_src 2'b01: clk_cpll_div10_pmu_src 2'b10: clk_cpll_div20_pmu_src 2'b11: xin_osc0_func
6:0	RO	0x00	reserved

PMU1CRU_CLKSEL_CON08

Address: Operational Base(0x27220000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	sclk_uart1_sel sclk_uart1 clock mux. 1'b0: clk_uart1_src_top 1'b1: xin_osc0_func

PMU1CRU_CLKSEL_CON11

Address: Operational Base(0x27220000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x1	clk_hptimer_src_sel clk_hptimer_src clock mux. 1'b0: clk_cpll_mux 1'b1: xin_osc0_func
5:1	RW	0x00	clk_hptimer_src_div Divide clk_hptimer_src by (div_con + 1).
0	RO	0x0	reserved

PMU1CRU_CLKSEL_CON20

Address: Operational Base(0x27220000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	dbclk_gpio0_sel not use, controlled by pmu_grf
1:0	RW	0x0	pclk_pmu0_root_src_sel pclk_pmu0_root_src clock mux. 2'b00: clk_cpll_div10_pmu_src 2'b01: clk_cpll_div20_pmu_src 2'b10: xin_osc0_func

PMU1CRU_CLKSEL_CON21

Address: Operational Base(0x27220000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:0	RW	0x0040b71b	xin_osc0_div_div xin_osc0_div fraction division register. High 16-bit for numerator Low 16-bit for denominator

PMU1CRU_GATE_CON00

Address: Operational Base(0x27220000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_usbdp_combo_phy_immortal_en clk_usbdp_combo_phy_immortal clock gating control. When high, disable clock
14	RO	0x0	reserved
13	RW	0x1	clk_pmuphy_ref_src_en clk_pmuphy_ref_src clock gating control. When high, disable clock
12	RW	0x0	pclk_usbdpphy_en pclk_usbdpphy clock gating control. When high, disable clock
11	RW	0x0	pclk_usbdp_grf_en pclk_usbdp_grf clock gating control. When high, disable clock
10	RW	0x0	pclk_usbphy_grf_1_en pclk_usbphy_grf_1 clock gating control. When high, disable clock
9	RW	0x0	pclk_usbphy_grf_0_en pclk_usbphy_grf_0 clock gating control. When high, disable clock
8	RW	0x0	pclk_csidphy_en pclk_csidphy clock gating control. When high, disable clock
7	RW	0x0	pclk_csidphy_grf_en pclk_csidphy_grf clock gating control. When high, disable clock
6	RW	0x0	clk_32k_usb2debug_en clk_32k_usb2debug clock gating control. When high, disable clock
5	RW	0x0	pclk_bot1_apb2asb_en pclk_bot1_apb2asb clock gating control. When high, disable clock
4	RW	0x0	pclk_bot0_apb2asb_en pclk_bot0_apb2asb clock gating control. When high, disable clock
3	RW	0x0	pclk_dcphy_grf_en pclk_dcphy_grf clock gating control. When high, disable clock
2	RW	0x0	pclk_mipi_dcphy_en pclk_mipi_dcphy clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	pclk_hdptx_apb_en pclk_hdptx_apb clock gating control. When high, disable clock
0	RW	0x0	pclk_hdptx_grf_en pclk_hdptx_grf clock gating control. When high, disable clock

PMU1CRU_GATE_CON01

Address: Operational Base(0x27220000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_hdmitxhpd_en clk_hdmitxhpd clock gating control. When high, disable clock
12:7	RO	0x00	reserved
6	RW	0x0	pclk_vccio6_ioc_en pclk_vccio6_ioc clock gating control. When high, disable clock
5:0	RO	0x00	reserved

PMU1CRU_GATE_CON02

Address: Operational Base(0x27220000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_ref_ufs_clkout_en clk_ref_ufs_clkout clock gating control. When high, disable clock
4	RO	0x0	reserved
3	RW	0x0	pclk_vccio7_ioc_en pclk_vccio7_ioc clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	pclk_mphy_grf_en pclk_mphy_grf clock gating control. When high, disable clock
0	RW	0x0	pclk_mphy_en pclk_mphy clock gating control. When high, disable clock

PMU1CRU_GATE_CON03

Address: Operational Base(0x27220000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	pclk_pmu1_en pclk_pmu1 clock gating control. When high, disable clock
14	RW	0x0	clk_pmu_cm0_rtc_en clk_pmu_cm0_rtc clock gating control. When high, disable clock
13	RO	0x0	reserved
12	RW	0x0	fclk_pmu_cm0_core_en fclk_pmu_cm0_core clock gating control. When high, disable clock
11	RW	0x0	hclk_pmu_cm0_biu_en hclk_pmu_cm0_biu clock gating control. When high, disable clock
10	RW	0x0	pclk_pmu1_biu_en pclk_pmu1_biu clock gating control. When high, disable clock
9	RW	0x0	hclk_pmu1_biu_en hclk_pmu1_biu clock gating control. When high, disable clock
8	RW	0x0	hclk_pmu_cm0_root_en hclk_pmu_cm0_root clock gating control. When high, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	hclk_pmu1_root_en hclk_pmu1_root clock gating control. When high, disable clock
4	RW	0x0	clk_cpll_div20_pmu_src_en clk_cpll_div20_pmu_src clock gating control. When high, disable clock
3	RW	0x0	clk_cpll_div10_pmu_src_en clk_cpll_div10_pmu_src clock gating control. When high, disable clock
2	RW	0x0	clk_gpll_div6_pmu_src_en clk_gpll_div6_pmu_src clock gating control. When high, disable clock
1	RW	0x0	hclk_pmu1_cm0_root_src_en hclk_pmu_cm0_root_src clock gating control. When high, disable clock
0	RW	0x0	hclk_pmu1_root_src_en hclk_pmu1_root_src clock gating control. When high, disable clock

PMU1CRU_GATE_CON04

Address: Operational Base(0x27220000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_pwm0_osc_en clk_pwm0_osc clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
12	RW	0x0	clk_pwm0_en clk_pwm0 clock gating control. When high, disable clock
11	RW	0x0	pclk_pwm0_en pclk_pwm0 clock gating control. When high, disable clock
10	RW	0x0	clk_pmutimer1_en clk_pmutimer1 clock gating control. When high, disable clock
9	RW	0x0	clk_pmutimer0_en clk_pmutimer0 clock gating control. When high, disable clock
8	RW	0x0	clk_pmutimer_root_en clk_pmutimer_root clock gating control. When high, disable clock
7	RW	0x0	pclk_pmutimer_en pclk_pmutimer clock gating control. When high, disable clock
6	RW	0x0	tclk_pmu1wdt_en tclk_pmu1wdt clock gating control. When high, disable clock
5	RW	0x0	pclk_pmu1wdt_en pclk_pmu1wdt clock gating control. When high, disable clock
4	RW	0x0	pclk_pmu1_ioc_en pclk_pmu1_ioc clock gating control. When high, disable clock
3	RW	0x0	pclk_pmu1_grf_en pclk_pmu1_grf clock gating control. When high, disable clock
2	RW	0x0	clk_pmu1_en clk_pmu1 clock gating control. When high, disable clock
1	RW	0x0	pclk_pmu1_cru_en pclk_pmu1_cru clock gating control. When high, disable clock
0	RO	0x0	reserved

PMU1CRU_GATE_CON05

Address: Operational Base(0x27220000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hclk_pdm0_en hclk_pdm0 clock gating control. When high, disable clock
14	RO	0x0	reserved
13	RW	0x0	clk_pdm0_en clk_pdm0 clock gating control. When high, disable clock
12:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	clk_pwm0_rc_en clk_pwm0_rc clock gating control. When high, disable clock
6	RW	0x0	pclk_uart1_en pclk_uart1 clock gating control. When high, disable clock
5	RW	0x0	sclk_uart1_en sclk_uart1 clock gating control. When high, disable clock
4:3	RO	0x0	reserved
2	RW	0x0	clk_i2c0_en clk_i2c0 clock gating control. When high, disable clock
1	RW	0x0	pclk_i2c0_en pclk_i2c0 clock gating control. When high, disable clock
0	RW	0x0	pclk_pmuphy_root_en pclk_pmuphy_root clock gating control. When high, disable clock

PMU1CRU_GATE_CON06

Address: Operational Base(0x27220000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	clk_hptimer_src_en clk_hptimer_src clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	clk_pdm0_out_en clk_pdm0_out clock gating control. When high, disable clock
7:5	RO	0x0	reserved
4	RW	0x0	clk_oscchk_pvtm_en clk_oscchk_pvtm clock gating control. When high, disable clock
3:2	RO	0x0	reserved
1	RW	0x0	hclk_vad_en hclk_vad clock gating control. When high, disable clock
0	RW	0x0	mclk_pdm0_en mclk_pdm0 clock gating control. When high, disable clock

PMU1CRU_GATE_CON07

Address: Operational Base(0x27220000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	xin_osc0_div_en xin_osc0_div clock gating control. When high, disable clock
12	RW	0x0	ref_clk2_out_en ref_clk2_out clock gating control. When high, disable clock
11	RW	0x0	ref_clk1_out_en ref_clk1_out clock gating control. When high, disable clock
10	RW	0x0	ref_clk0_out_en ref_clk0_out clock gating control. When high, disable clock
9	RW	0x0	pclk_pmu1_root_en pclk_pmu1_root clock gating control. When high, disable clock
8	RW	0x0	clk_osc0_pmu1_en clk_osc0_pmu1 clock gating control. When high, disable clock
7	RW	0x0	dbclk_gpio0_en dbclk_gpio0 clock gating control. When high, disable clock
6	RW	0x0	pclk_gpio0_en pclk_gpio0 clock gating control. When high, disable clock
5	RW	0x0	pclk_pmu0ioc_en pclk_pmu0ioc clock gating control. When high, disable clock
4	RW	0x0	pclk_pmu0grf_en pclk_pmu0grf clock gating control. When high, disable clock
3	RW	0x0	pclk_pmu0_en pclk_pmu0 clock gating control. When high, disable clock
2	RW	0x0	clk_pmu0_en clk_pmu0 clock gating control. When high, disable clock
1	RW	0x0	pclk_pmu0_root_en pclk_pmu0_root clock gating control. When high, disable clock
0	RW	0x0	pclk_pmu0_root_src_en pclk_pmu0_root_src clock gating control. When high, disable clock

PMU1CRU_SOFTRST_CON00

Address: Operational Base(0x27220000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_usbdp_combo_phy_init When high, reset relative logic
14:13	RO	0x0	reserved
12	RW	0x0	presetn_usbdpphy When high, reset relative logic

Bit	Attr	Reset Value	Description
11	RW	0x0	presetn_usbdp_grf When high, reset relative logic
10	RW	0x0	presetn_usbphy_grf_1 When high, reset relative logic
9	RW	0x0	presetn_usbphy_grf_0 When high, reset relative logic
8	RW	0x0	presetn_csidphy When high, reset relative logic
7	RW	0x0	presetn_csidphy_grf When high, reset relative logic
6	RW	0x0	resetn_usb2debug When high, reset relative logic
5	RW	0x0	presetn_bot1_apb2asb When high, reset relative logic
4	RW	0x0	presetn_bot0_apb2asb When high, reset relative logic
3	RW	0x0	presetn_dcphy_grf When high, reset relative logic
2	RW	0x0	presetn_mipi_dcphy When high, reset relative logic
1	RW	0x0	presetn_hdptx_apb When high, reset relative logic
0	RW	0x0	presetn_hdptx_grf When high, reset relative logic

PMU1CRU_SOFTRST_CON01

Address: Operational Base(0x27220000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_hdmitxhpd When high, reset relative logic
12	RO	0x0	reserved
11	RW	0x0	resetn_hdptx_lane When high, reset relative logic
10	RW	0x0	resetn_hdptx_cmn When high, reset relative logic
9	RW	0x0	resetn_hdptx_init When high, reset relative logic
8	RW	0x0	resetn_otgphy_1 When high, reset relative logic
7	RW	0x0	resetn_otgphy_0 When high, reset relative logic
6	RW	0x0	presetn_vccio6_ioc When high, reset relative logic
5	RW	0x0	scanresetn_csidphy When high, reset relative logic
4	RW	0x0	sresetn_mipi_dcphy When high, reset relative logic
3	RW	0x0	mresetn_mipi_dcphy When high, reset relative logic

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Bit	Attr	Reset Value	Description
2	RW	0x0	resetn_usbdp_combo_phy_pcs When high, reset relative logic
1	RW	0x0	resetn_usbdp_combo_phy_lane When high, reset relative logic
0	RW	0x0	resetn_usbdp_combo_phy_cmn When high, reset relative logic

PMU1CRU_SOFTRST_CON02

Address: Operational Base(0x27220000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	presetn_vccio7_ioc When high, reset relative logic
2	RO	0x0	reserved
1	RW	0x0	presetn_mphy_grf When high, reset relative logic
0	RW	0x0	resetn_mphy_init When high, reset relative logic

PMU1CRU_SOFTRST_CON03

Address: Operational Base(0x27220000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	tresetn_pmu1_cm0_jtag When high, reset relative logic
12	RW	0x1	fresetn_pmu_cm0_core When high, reset relative logic
11	RW	0x0	hresetn_pmu_cm0_biu When high, reset relative logic
10	RW	0x0	presetn_pmu1_biu When high, reset relative logic
9	RW	0x0	hresetn_pmu1_biu When high, reset relative logic
8:0	RO	0x000	reserved

PMU1CRU_SOFTRST_CON04

Address: Operational Base(0x27220000) + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	resetn_pwm0 When high, reset relative logic
11	RW	0x0	presetn_pwm0 When high, reset relative logic

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Bit	Attr	Reset Value	Description
10	RW	0x0	resetn_pmutimer1 When high, reset relative logic
9	RW	0x0	resetn_pmutimer0 When high, reset relative logic
8	RO	0x0	reserved
7	RW	0x0	presetn_pmutimer When high, reset relative logic
6	RW	0x0	tresetn_pmu1wdt When high, reset relative logic
5	RW	0x0	presetn_pmu1wdt When high, reset relative logic
4	RW	0x0	presetn_pmu1_ioc When high, reset relative logic
3	RW	0x0	presetn_pmu1_grf When high, reset relative logic
2	RO	0x0	reserved
1	RW	0x0	presetn_cru_pmu1 When high, reset relative logic
0	RO	0x0	reserved

PMU1CRU_SOFTRST_CON05

Address: Operational Base(0x27220000) + offset (0x0A14)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hresetn_pdm0 When high, reset relative logic
14	RO	0x0	reserved
13	RW	0x0	resetn_pdm0 When high, reset relative logic
12:7	RO	0x00	reserved
6	RW	0x0	presetn_uart1 When high, reset relative logic
5	RW	0x0	sresetn_uart1 When high, reset relative logic
4:3	RO	0x0	reserved
2	RW	0x0	resetn_i2c0 When high, reset relative logic
1	RW	0x0	presetn_i2c0 When high, reset relative logic
0	RO	0x0	reserved

PMU1CRU_SOFTRST_CON06

Address: Operational Base(0x27220000) + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	hresetn_vad When high, reset relative logic

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Bit	Attr	Reset Value	Description
0	RW	0x0	mresetn_pdm0 When high, reset relative logic

PMU1CRU_SOFTRST_CON07

Address: Operational Base(0x27220000) + offset (0x0A1C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	dbresetn_gpio0 When high, reset relative logic
6	RW	0x0	presetn_gpio0 When high, reset relative logic
5	RW	0x0	presetn_pmu0ioc When high, reset relative logic
4	RW	0x0	presetn_pmu0grf When high, reset relative logic
3:0	RO	0x0	reserved

PMU1CRU_AUTOCS_PCLK_PMU0_ROOT_SRC_CON0

Address: Operational Base(0x27220000) + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

PMU1CRU_AUTOCS_PCLK_PMU0_ROOT_SRC_CON1

Address: Operational Base(0x27220000) + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable

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Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_pmu control; bit1-bit11: reserved;

PMU1CRU_AUTOCS_HCLK_PMU1_ROOT_SRC_CON0

Address: Operational Base(0x27220000) + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

PMU1CRU_AUTOCS_HCLK_PMU1_ROOT_SRC_CON1

Address: Operational Base(0x27220000) + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_pmu control; bit1-bit11: reserved;

PMU1CRU_AUTOCS_HCLK_PMU_CM0_ROOT_SRC_CON0

Address: Operational Base(0x27220000) + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk

Bit	Attr	Reset Value	Description
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

PMU1CRU_AUTOCS_HCLK_PMU_CM0_ROOT_SRC_CON1

Address: Operational Base(0x27220000) + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: noc_active_pmu control; bit1: intmux and sgrf_pmu_mcu control; bit2-bit11: reserved;

PMU1CRU_DEEPSLOW_DETECT_CON

Address: Operational Base(0x27220000) + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	detect_32k_en detect_32k_en 1'b0 : not ebable detect. 1'b1 : enable detect 32k io clk.
6:0	RW	0x00	cnt_clk cnt_clk for internal counter counter threhold of using OSC clk to cnt for 32k io clk, counter = cnt_clk * 8

PMU1CRU_DEEPSLOW_DETECT_ST

Address: Operational Base(0x27220000) + offset (0x0B44)

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Bit	Attr	Reset Value	Description
31	RW	0x0	32k_io_exist_st 32k_io_exist_st If High, 32k io input is detected.
30:0	RO	0x00000000	reserved

PMU1CRU_CLKSEL_CON30

Address: Operational Base(0x27220000) + offset (0x4000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	hclk_pmu_s_root_src_sel hclk_pmu_s_root_src clock mux. 2'b00: clk_matrix_sec_175m_src 2'b01: clk_matrix_sec_116m_src 2'b10: xin_osc0_func

PMU1CRU_CLKSEL_CON32

Address: Operational Base(0x27220000) + offset (0x4008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:1	RW	0x000	clk_pvtm_32k_div Divide clk_pvtm_32k by (div_con + 1).
0	RW	0x0	pclk_pmu_s_root_src_sel pclk_pmu_s_root_src clock mux. 1'b0: clk_matrix_sec_116m_src 1'b1: xin_osc0_func

PMU1CRU_GATE_CON10

Address: Operational Base(0x27220000) + offset (0x4028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	pclk_pmu1_s_biu_en pclk_pmu1_s_biu clock gating control. When high, disable clock
5	RW	0x0	pclk_pmu1_sgrf_en pclk_pmu1_sgrf clock gating control. When high, disable clock
4	RW	0x0	hclk_pmu1_mem_en hclk_pmu1_mem clock gating control. When high, disable clock
3	RW	0x0	pclk_pmu1_osc_chk_en pclk_pmu1_osc_chk clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	hclk_pmu1_s_biu_en hclk_pmu1_s_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_pmu_s_root_en hclk_pmu_s_root clock gating control. When high, disable clock
0	RW	0x0	hclk_pmu_s_root_src_en hclk_pmu_s_root_src clock gating control. When high, disable clock

PMU1CRU_GATE_CON12

Address: Operational Base(0x27220000) + offset (0x4030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	pclk_pmu_s_root_en pclk_pmu_s_root clock gating control. When high, disable clock
10	RW	0x0	pclk_pmu1_s_root_en pclk_pmu1_s_root clock gating control. When high, disable clock
9	RW	0x0	pclk_pmu_s_root_src_en pclk_pmu_s_root_src clock gating control. When high, disable clock
8	RW	0x0	clk_pmu0_32k_hp_timer_en clk_pmu0_32k_hp_timer clock gating control. When high, disable clock
7	RW	0x0	clk_pmu0_hp_timer_en clk_pmu0_hp_timer clock gating control. When high, disable clock
6	RW	0x0	pclk_pmu0_hp_timer_en pclk_pmu0_hp_timer clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	pclk_pmu_sgrf_en pclk_pmu_sgrf clock gating control. When high, disable clock
3	RW	0x0	pclk_pmu0pvtm_en pclk_pmu0pvtm clock gating control. When high, disable clock
2	RW	0x0	clk_pmu0pvtm_en clk_pmu0pvtm clock gating control. When high, disable clock
1	RW	0x0	clk_scrkeygen_en clk_scrkeygen clock gating control. When high, disable clock
0	RW	0x0	pclk_pmu0_scrkeygen_en pclk_scrkeygen clock gating control. When high, disable clock

PMU1CRU_SOFTRST_CON10

Address: Operational Base(0x27220000) + offset (0x4050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	presetn_pmu1_s_biu When high, reset relative logic
5	RW	0x0	presetn_pmu1_sgrf When high, reset relative logic
4	RW	0x0	hresetn_pmu1_mem When high, reset relative logic
3	RW	0x0	presetn_pmu1_osc_chk When high, reset relative logic
2	RW	0x0	hresetn_pmu1_s_biu When high, reset relative logic
1:0	RO	0x0	reserved

PMU1CRU_SOFTRST_CON12

Address: Operational Base(0x27220000) + offset (0x4058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	resetn_pmu0_32k_hp_timer When high, reset relative logic
7	RW	0x0	resetn_pmu0_hp_timer When high, reset relative logic
6	RW	0x0	presetn_pmu0_hp_timer When high, reset relative logic
5	RW	0x0	presetn_pmu_sgrf_remap When high, reset relative logic
4	RW	0x0	presetn_pmu_sgrf When high, reset relative logic
3	RW	0x0	presetn_pmu0pvtm When high, reset relative logic
2	RW	0x0	resetn_pmu0pvtm When high, reset relative logic
1:0	RO	0x0	reserved

2.8 DDR0_CRU

2.8.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.8.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DDR0CRU_D0APLL_CON0	0x0000	W	0x00008073	D0APLL configuration register 0
DDR0CRU_D0APLL_CON1	0x0004	W	0x00000001	D0APLL configuration register 1
DDR0CRU_D0APLL_CON2	0x0008	W	0x00009555	D0APLL configuration register 2
DDR0CRU_D0APLL_CON3	0x000C	W	0x00000000	D0APLL configuration register 3
DDR0CRU_D0APLL_CON4	0x0010	W	0x00000000	D0APLL configuration register 4

Name	Offset	Size	Reset Value	Description
DDR0CRU_D0APLL_CON5	0x0014	W	0x00000000	D0APLL configuration register 5
DDR0CRU_D0APLL_CON6	0x0018	W	0x00000000	D0APLL configuration register 6
DDR0CRU_D0BPLL_CON0	0x0020	W	0x00008073	D0BPLL configuration register 0
DDR0CRU_D0BPLL_CON1	0x0024	W	0x00000001	D0BPLL configuration register 1
DDR0CRU_D0BPLL_CON2	0x0028	W	0x00009555	D0BPLL configuration register 2
DDR0CRU_D0BPLL_CON3	0x002C	W	0x00000000	D0BPLL configuration register 3
DDR0CRU_D0BPLL_CON4	0x0030	W	0x00000000	D0BPLL configuration register 4
DDR0CRU_D0BPLL_CON5	0x0034	W	0x00000000	D0BPLL configuration register 5
DDR0CRU_D0BPLL_CON6	0x0038	W	0x00000000	D0BPLL configuration register 6
DDR0CRU_CLKSEL_CON00	0x0300	W	0x00000000	Internal clock select and division register 0
DDR0CRU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
DDR0CRU_SOFTRST_CON00	0x0A00	W	0x00000006	Internal clock reset register 0

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.8.3 Detail Registers Description

DDR0CRU_D0APLL_CON0

Address: Operational Base(0x27228000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	d0apll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x073	d0apll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

DDR0CRU_D0APLL_CON1

Address: Operational Base(0x27228000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	d0apll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x0	d0apll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6

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Bit	Attr	Reset Value	Description
5:0	RW	0x01	d0apll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

DDR0CRU_D0APLL_CON2

Address: Operational Base(0x27228000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x9555	d0apll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

DDR0CRU_D0APLL_CON3

Address: Operational Base(0x27228000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	d0apll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.
13:8	RW	0x00	d0apll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	d0apll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

DDR0CRU_D0APLL_CON4

Address: Operational Base(0x27228000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	d0apll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	d0apll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	d0apll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.

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Bit	Attr	Reset Value	Description
3	RW	0x0	d0apll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	d0apll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

DDR0CRU_D0APLL_CON5

Address: Operational Base(0x27228000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	d0apll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

DDR0CRU_D0APLL_CON6

Address: Operational Base(0x27228000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	d0apll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	d0apll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

DDR0CRU_D0BPLL_CON0

Address: Operational Base(0x27228000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	d0bpll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x073	d0bpll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

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DDR0CRU_D0BPLL_CON1

Address: Operational Base(0x27228000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	d0bpll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x0	d0bpll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x01	d0bpll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

DDR0CRU_D0BPLL_CON2

Address: Operational Base(0x27228000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x9555	d0bpll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

DDR0CRU_D0BPLL_CON3

Address: Operational Base(0x27228000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	d0bpll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.
13:8	RW	0x00	d0bpll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	d0bpll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

DDR0CRU_D0BPLL_CON4

Address: Operational Base(0x27228000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	d0bpll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	d0bpll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	d0bpll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	d0bpll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	d0bpll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

DDR0CRU_D0BPLL_CON5

Address: Operational Base(0x27228000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	d0bpll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

DDR0CRU_D0BPLL_CON6

Address: Operational Base(0x27228000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	d0bpll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	d0bpll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

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DDR0CRU_CLKSEL_CON00

Address: Operational Base(0x27228000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	clk_ddrphy2x_ch0_sel clk_ddrphy2x_ch0 clock mux. 1'b0: clk_d0apll_t 1'b1: clk_d0bpll

DDR0CRU_GATE_CON00

Address: Operational Base(0x27228000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_osc_ddrphy_ch0_en clk_osc_ddrphy_ch0 clock gating control. When high, disable clock
4	RW	0x0	pclk_ddrphy_ch0_en pclk_ddrphy_ch0 clock gating control. When high, disable clock
3	RW	0x0	pclk_ddr_cru_ch0_en pclk_ddr_cru_ch0 clock gating control. When high, disable clock
2:0	RO	0x0	reserved

DDR0CRU_SOFTRST_CON00

Address: Operational Base(0x27228000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	presetn_ddrphy_ch0 When high, reset relative logic
3	RW	0x0	presetn_ddr_cru_ch0 When high, reset relative logic
2	RW	0x1	resetn_ddrphy2x_ch0 When high, reset relative logic
1	RW	0x1	resetn_ddrphy2xdiv_ch0 div_rst_n at ddr ch0 When high, reset relative logic
0	RO	0x0	reserved

2.9 DDR1_CRU

2.9.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.9.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DDR1CRU_D1APLL_CON0	0x0000	W	0x00008073	D1APLL configuration register 0
DDR1CRU_D1APLL_CON1	0x0004	W	0x00000001	D1APLL configuration register 1
DDR1CRU_D1APLL_CON2	0x0008	W	0x00009555	D1APLL configuration register 2
DDR1CRU_D1APLL_CON3	0x000C	W	0x00000000	D1APLL configuration register 3
DDR1CRU_D1APLL_CON4	0x0010	W	0x00000000	D1APLL configuration register 4
DDR1CRU_D1APLL_CON5	0x0014	W	0x00000000	D1APLL configuration register 5
DDR1CRU_D1APLL_CON6	0x0018	W	0x00000000	D1APLL configuration register 6
DDR1CRU_D1BPLL_CON0	0x0020	W	0x00008073	D1BPLL configuration register 0
DDR1CRU_D1BPLL_CON1	0x0024	W	0x00000001	D1BPLL configuration register 1
DDR1CRU_D1BPLL_CON2	0x0028	W	0x00009555	D1BPLL configuration register 2
DDR1CRU_D1BPLL_CON3	0x002C	W	0x00000000	D1BPLL configuration register 3
DDR1CRU_D1BPLL_CON4	0x0030	W	0x00000000	D1BPLL configuration register 4
DDR1CRU_D1BPLL_CON5	0x0034	W	0x00000000	D1BPLL configuration register 5
DDR1CRU_D1BPLL_CON6	0x0038	W	0x00000000	D1BPLL configuration register 6
DDR1CRU_CLKSEL_CON00	0x0300	W	0x00000000	Internal clock select and division register 0
DDR1CRU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
DDR1CRU_SOFTRST_CON00	0x0A00	W	0x00000006	Internal clock reset register 0

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.9.3 Detail Registers Description

DDR1CRU_D1APLL_CON0

Address: Operational Base(0x27230000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	d1apll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x073	d1apll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

DDR1CRU_D1APLL_CON1

Address: Operational Base(0x27230000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	d1apll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x0	d1apll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x01	d1apll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

DDR1CRU_D1APLL_CON2

Address: Operational Base(0x27230000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x9555	d1apll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

DDR1CRU_D1APLL_CON3

Address: Operational Base(0x27230000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	d1apll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.
13:8	RW	0x00	d1apll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	d1apll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

DDR1CRU_D1APLL_CON4

Address: Operational Base(0x27230000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	d1apll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.

Bit	Attr	Reset Value	Description
14	RW	0x0	d1apll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	d1apll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	d1apll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	d1apll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

DDR1CRU_D1APLL_CON5

Address: Operational Base(0x27230000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	d1apll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

DDR1CRU_D1APLL_CON6

Address: Operational Base(0x27230000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	d1apll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	d1apll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

DDR1CRU_D1BPLL_CON0

Address: Operational Base(0x27230000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x1	d1bpll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved
9:0	RW	0x073	d1bpll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

DDR1CRU_D1BPLL_CON1

Address: Operational Base(0x27230000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	d1bpll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x0	d1bpll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x01	d1bpll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

DDR1CRU_D1BPLL_CON2

Address: Operational Base(0x27230000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x9555	d1bpll_k K: Value of 16-bit DSM. pll_k[15:0] is a two's complement integer.

DDR1CRU_D1BPLL_CON3

Address: Operational Base(0x27230000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	d1bpll_sel_pf SEL_PF: Value of 2-bit modulation method control. 2'b00: down spread; 2'b01: up spread; 2'b1x: center spread. PLL has to be reset if pll_sel_pf is changed.

Bit	Attr	Reset Value	Description
13:8	RW	0x00	d1bpll_mrr MRR: Value of 6-bit modulation rate control. PLL has to be reset if pll_mrr is changed.
7:0	RW	0x00	d1bpll_mfr MFR: Value of 8-bit modulation frequency control. PLL has to be reset if pll_mfr is changed.

DDR1CRU_D1BPLL_CON4

Address: Operational Base(0x27230000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	d1bpll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	d1bpll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	d1bpll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	d1bpll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RO	0x0	reserved
0	RW	0x0	d1bpll_sscg_en SSCG_EN: Enable pin for dithered mode. 1'b0: disable dithered mode. 1'b1: enable dithered mode.

DDR1CRU_D1BPLL_CON5

Address: Operational Base(0x27230000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	d1bpll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

DDR1CRU_D1BPLL_CON6

Address: Operational Base(0x27230000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	d1bpll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	d1bpll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

DDR1CRU_CLKSEL_CON00

Address: Operational Base(0x27230000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	clk_ddrphy2x_ch1_sel clk_ddrphy2x_ch1 clock mux. 1'b0: clk_d1apll_t 1'b1: clk_d1bpll

DDR1CRU_GATE_CON00

Address: Operational Base(0x27230000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_osc_ddrphy_ch1_en clk_osc_ddrphy_ch1 clock gating control. When high, disable clock
4	RW	0x0	pclk_ddrphy_ch1_en pclk_ddrphy_ch1 clock gating control. When high, disable clock
3	RW	0x0	pclk_ddr_cru_ch1_en pclk_ddr_cru_ch1 clock gating control. When high, disable clock
2:0	RO	0x0	reserved

DDR1CRU_SOFTRST_CON00

Address: Operational Base(0x27230000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	presetn_ddrphy_ch1 When high, reset relative logic

Bit	Attr	Reset Value	Description
3	RW	0x0	presetn_ddr_cru_ch1 When high, reset relative logic
2	RW	0x1	resetn_ddrphy2x_ch1 When high, reset relative logic
1	RW	0x1	resetn_ddrphy2xdiv_ch1 div_rst_n at ddr ch1 When high, reset relative logic
0	RO	0x0	reserved

2.10 BIGCORE_CRU

2.10.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.10.2 Registers Summary

Name	Offset	Size	Reset Value	Description
BIGCORECRU_MODE_CON00	0x0280	W	0x00000000	Internal clock select and division register 0
BIGCORECRU_CLKSEL_CON00	0x0300	W	0x00000580	Internal clock select and division register 0
BIGCORECRU_CLKSEL_CON01	0x0304	W	0x00000000	Internal clock select and division register 1
BIGCORECRU_CLKSEL_CON02	0x0308	W	0x00000001	Internal clock select and division register 2
BIGCORECRU_CLKSEL_CON03	0x030C	W	0x00000001	Internal clock select and division register 3
BIGCORECRU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
BIGCORECRU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
BIGCORECRU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
BIGCORECRU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1
BIGCORECRU_SOFTRST_CON03	0x0A0C	W	0x00000000	Internal clock reset register 3
BIGCORECRU_SMOTH_DIVFREE_CON00	0x0CC0	W	0x0200C003	Smoothdiv control register
BIGCORECRU_AUTOCS_CLK_BIGCORE_SRC_CON0	0x0F28	W	0x00200047	auto clock switch control 0
BIGCORECRU_AUTOCS_CLK_BIGCORE_SRC_CON1	0x0F2C	W	0x00000000	auto clock switch control 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.10.3 Detail Registers Description

BIGCORECRU_MODE_CON00

Address: Operational Base(0x27238000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	clk_bpll_mode clk_bpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_bpll 2'b10: clk_deepslow

BIGCORECRU_CLKSEL_CON00

Address: Operational Base(0x27238000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	pclk_bigcore_root_sel pclk_bigcore_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_bpll_mux
11:7	RW	0x0b	pclk_bigcore_root_div Divide pclk_bigcore_root by (div_con + 1).
6:0	RO	0x00	reserved

BIGCORECRU_CLKSEL_CON01

Address: Operational Base(0x27238000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_bigcore_sel clk_bigcore clock mux. 2'b00: clk_bigcore_src_out 2'b01: clk_bigcore_pvtpll_src 2'b10: clk_bigcore_clean
13:12	RW	0x0	clk_bigcore_src_sel clk_bigcore_src clock mux. 2'b00: clk_bpll_mux 2'b01: clk_gpll_mux 2'b10: clk_bigcore_pvtpll_src
11:7	RW	0x00	clk_bigcore_src_div Divide clk_bigcore_src by (div_con + 1).
6:3	RO	0x0	reserved
2:0	RW	0x0	mbist_clk_clk_bigcore_src_div Divide mbist_clk_clk_bigcore_src by (div_con + 1).

BIGCORECRU_CLKSEL_CON02

Address: Operational Base(0x27238000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	clk_bigcore_pvtpll_src_sel clk_bigcore_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_bigcore_pvtpll
4:0	RW	0x01	aclk_m_bigcore_div Divide aclk_m_bigcore by (div_con + 1).

BIGCORECRU_CLKSEL_CON03

Address: Operational Base(0x27238000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x01	clk_scanhs_aclk_m_bigcore_div Divide clk_scanhs_aclk_m_bigcore by (div_con + 1).

BIGCORECRU_GATE_CON00

Address: Operational Base(0x27238000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_bigcore_en clk_bigcore clock gating control. When high, disable clock
13	RW	0x0	clk_bigcore_src_en clk_bigcore_src clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x0	clk_bigcore_clean_en clk_bigcore_clean clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	pclk_pvtpll_bigcore_en pclk_pvtpll_bigcore clock gating control. When high, disable clock
8	RW	0x0	pclk_bigcore_cru_en pclk_bigcore_cru clock gating control. When high, disable clock
7	RW	0x0	pclk_bigcore_grf_en pclk_bigcore_grf clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	pclk_bigcore_biu_en pclk_bigcore_biu clock gating control. When high, disable clock
4	RW	0x0	pclk_bigcore_root_en pclk_bigcore_root clock gating control. When high, disable clock
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	clk_ref_pvtpll_bigcore_en clk_ref_pvtpll_bigcore clock gating control. When high, disable clock
0	RO	0x0	reserved

BIGCORECRU_GATE_CON01

Address: Operational Base(0x27238000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	aclk_adb400_a72_cci_en aclk_adb400_a72_cci clock gating control. When high, disable clock
10	RW	0x0	clk_scanhs_bigcore_en clk_scanhs_bigcore clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	pclk_dbg_bigcore_en pclk_dbg_bigcore clock gating control. When high, disable clock
7	RW	0x0	aclk_m_bigcore_en aclk_m_bigcore clock gating control. When high, disable clock
6:0	RO	0x00	reserved

BIGCORECRU_SOFTRST_CON00

Address: Operational Base(0x27238000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	nbigcoreporeset1 When high, reset relative logic
14	RW	0x0	nbigcoreporeset0 When high, reset relative logic
13:10	RO	0x0	reserved
9	RW	0x0	presetn_pvtpll_bigcore When high, reset relative logic
8	RW	0x0	presetn_bigcore_cru When high, reset relative logic
7	RW	0x0	presetn_bigcore_grf When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	presetn_bigcore_biu When high, reset relative logic
4:2	RO	0x0	reserved
1	RW	0x0	resetn_ref_pvtpll_bigcore When high, reset relative logic
0	RO	0x0	reserved

BIGCORECRU_SOFTRST_CON01

Address: Operational Base(0x27238000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	aresetn_adb400_a72_cci When high, reset relative logic
10:9	RO	0x0	reserved
8	RW	0x0	presetn_dbg_bigcore When high, reset relative logic
7	RO	0x0	reserved
6	RW	0x0	nl2reset_bigcore When high, reset relative logic
5	RW	0x0	nbigcoreset3 When high, reset relative logic
4	RW	0x0	nbigcoreset2 When high, reset relative logic
3	RW	0x0	nbigcoreset1 When high, reset relative logic
2	RW	0x0	nbigcoreset0 When high, reset relative logic
1	RW	0x0	nbigcoreporeset3 When high, reset relative logic
0	RW	0x0	nbigcoreporeset2 When high, reset relative logic

BIGCORECRU_SOFTRST_CON03

Address: Operational Base(0x27238000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	nl2reset_bigcore_ac When high, reset relative logic, this rst req will be auto clear
7	RW	0x0	nbigcoreset3_ac When high, reset relative logic, this rst req will be auto clear
6	RW	0x0	nbigcoreset2_ac When high, reset relative logic, this rst req will be auto clear
5	RW	0x0	nbigcoreset1_ac When high, reset relative logic, this rst req will be auto clear
4	RW	0x0	nbigcoreset0_ac When high, reset relative logic, this rst req will be auto clear
3	RW	0x0	nbigcoreporeset3_ac When high, reset relative logic, this rst req will be auto clear
2	RW	0x0	nbigcoreporeset2_ac When high, reset relative logic, this rst req will be auto clear
1	RW	0x0	nbigcoreporeset1_ac When high, reset relative logic, this rst req will be auto clear
0	RW	0x0	nbigcoreporeset0_ac When high, reset relative logic, this rst req will be auto clear

BIGCORECRU_SMOTH_DIVFREE_CON00

Address: Operational Base(0x27238000) + offset (0x0CC0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	clk_bigcore_src_freq_keep freq_keep Cycles to keep every step.
15	RW	0x1	clk_bigcore_src_bypass bypass Division signal bypass. 1'b1: Bypass. 1'b0: Use Smoothdiv to control clock division.
14	RW	0x1	clk_bigcore_src_gate_smth_en gate_smth_en If trigger smoothdiv function when clk been gated. 1'b1: Enable. 1'b0: Disable.
13	RW	0x0	clk_bigcore_src_smdiv_clk_off smdiv_clk_off Turn off smoothdiv module clk. 1'b1: Turn off. 1'b0: Turn on.
12:5	RO	0x00	reserved
4:0	RW	0x03	clk_bigcore_src_step step Step of div from 0x1f to setting configuration .

BIGCORECRU_AUTOCS_CLK_BIGCORE_SRC_CON0

Address: Operational Base(0x27238000) + offset (0x0F28)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

BIGCORECRU_AUTOCS_CLK_BIGCORE_SRC_CON1

Address: Operational Base(0x27238000) + offset (0x0F2C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable

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Bit	Attr	Reset Value	Description
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11:0	RO	0x000	reserved

2.11 LITCORE_CRU

2.11.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.11.2 Registers Summary

Name	Offset	Size	Reset Value	Description
LITCORECRU_MODE_CON00	0x0280	W	0x00000000	Internal clock select and division register 0
LITCORECRU_CLKSEL_CON00	0x0300	W	0x00000000	Internal clock select and division register 0
LITCORECRU_CLKSEL_CON01	0x0304	W	0x0000010B	Internal clock select and division register 1
LITCORECRU_CLKSEL_CON02	0x0308	W	0x00000005	Internal clock select and division register 2
LITCORECRU_CLKSEL_CON03	0x030C	W	0x00000025	Internal clock select and division register 3
LITCORECRU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
LITCORECRU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
LITCORECRU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
LITCORECRU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1
LITCORECRU_SOFTRST_CON03	0x0A0C	W	0x00000000	Internal clock reset register 3
LITCORECRU_SMOTH_DIVFREE_CON00	0x0CC0	W	0x0200C003	Smoothdiv control register
LITCORECRU_AUTOCS_CLK_LITCORE_SRC_CON0	0x0F38	W	0x00200047	auto clock switch control 0
LITCORECRU_AUTOCS_CLK_LITCORE_SRC_CON1	0x0F3C	W	0x00000000	auto clock switch control 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.11.3 Detail Registers Description

LITCORECRU_MODE_CON00

Address: Operational Base(0x27240000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	clk_lpll_mode clk_lpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_lpll 2'b10: clk_deepslow

LITCORECRU_CLKSEL_CON00

Address: Operational Base(0x27240000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	clk_litcore_src_sel clk_litcore_src clock mux. 2'b00: clk_lpll_mux 2'b01: clk_gpll_mux 2'b10: clk_litcore_pvtpll_src
11:7	RW	0x00	clk_litcore_src_div Divide clk_litcore_src by (div_con + 1).
6:4	RW	0x0	mbist_clk_clk_litcore_src_div Divide mbist_clk_clk_litcore_src by (div_con + 1).
3:0	RO	0x0	reserved

LITCORECRU_CLKSEL_CON01

Address: Operational Base(0x27240000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_litcore_pvtpll_src_sel clk_litcore_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_litcore_pvtpll
12:8	RW	0x01	aclk_m_litcore_div Divide aclk_m_litcore by (div_con + 1).
7:6	RW	0x0	clk_litcore_sel clk_litcore clock mux. 2'b00: clk_litcore_src_out 2'b01: clk_litcore_pvtpll_src 2'b10: clk_litcore_clean
5	RW	0x0	pclk_litcore_root_sel pclk_litcore_root clock mux. 1'b0: clk_gpll_mux 1'b1: clk_lpll_mux
4:0	RW	0x0b	pclk_litcore_root_div Divide pclk_litcore_root by (div_con + 1).

LITCORECRU_CLKSEL_CON02

Address: Operational Base(0x27240000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x05	pclk_dbg_litcore_div Divide pclk_dbg_litcore by (div_con + 1).

LITCORECRU_CLKSEL_CON03

Address: Operational Base(0x27240000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:5	RW	0x01	clk_scanhs_aclk_m_litcore_div Divide clk_scanhs_aclk_m_litcore by (div_con + 1).
4:0	RW	0x05	clk_scanhs_pclk_dbg_litcore_div Divide clk_scanhs_pclk_dbg_litcore by (div_con + 1).

LITCORECRU_GATE_CON00

Address: Operational Base(0x27240000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_dbg_litcore_en pclk_dbg_litcore clock gating control. When high, disable clock
14	RW	0x0	aclk_m_litcore_en aclk_m_litcore clock gating control. When high, disable clock
13:6	RO	0x00	reserved
5	RW	0x0	clk_litcore_en clk_litcore clock gating control. When high, disable clock
4	RW	0x0	pclk_litcore_root_en pclk_litcore_root clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	clk_litcore_src_en clk_litcore_src clock gating control. When high, disable clock
1	RW	0x0	clk_litcore_clean_en clk_litcore_clean clock gating control. When high, disable clock
0	RW	0x0	clk_ref_pvtpll_litcore_en clk_ref_pvtpll_litcore clock gating control. When high, disable clock

LITCORECRU_GATE_CON01

Address: Operational Base(0x27240000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_scanhs_litcore_en clk_scanhs_litcore clock gating control. When high, disable clock
4	RW	0x0	pclk_litcore_cru_en pclk_litcore_cru clock gating control. When high, disable clock
3	RW	0x0	pclk_pvtpll_litcore_en pclk_pvtpll_litcore clock gating control. When high, disable clock
2	RW	0x0	aclk_adb400_a53_cci_en aclk_adb400_a53_cci clock gating control. When high, disable clock
1	RW	0x0	pclk_litcore_biu_en pclk_litcore_biu clock gating control. When high, disable clock
0	RW	0x0	pclk_litcore_grf_en pclk_litcore_grf clock gating control. When high, disable clock

LITCORECRU_SOFTRST_CON00

Address: Operational Base(0x27240000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_dbg_litcore When high, reset relative logic
14	RO	0x0	reserved
13	RW	0x0	nl2reset_litcore When high, reset relative logic
12	RW	0x0	nlitcoreset3 When high, reset relative logic
11	RW	0x0	nlitcoreset2 When high, reset relative logic
10	RW	0x0	nlitcoreset1 When high, reset relative logic
9	RW	0x0	nlitcoreset0 When high, reset relative logic
8	RW	0x0	nlitcoreporeset3 When high, reset relative logic
7	RW	0x0	nlitcoreporeset2 When high, reset relative logic
6	RW	0x0	nlitcoreporeset1 When high, reset relative logic
5	RW	0x0	nlitcoreporeset0 When high, reset relative logic
4:1	RO	0x0	reserved
0	RW	0x0	resetn_ref_litcore_pvtpll When high, reset relative logic

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LITCORECRU_SOFTRST_CON01

Address: Operational Base(0x27240000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	presetn_litcore_cru When high, reset relative logic
3	RW	0x0	presetn_pvtpll_litcore When high, reset relative logic
2	RW	0x0	aresetn_adb400_a53_cci When high, reset relative logic
1	RW	0x0	presetn_litcore_biu When high, reset relative logic
0	RW	0x0	presetn_litcore_grf When high, reset relative logic

LITCORECRU_SOFTRST_CON03

Address: Operational Base(0x27240000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	nl2reset_litcore_ac When high, reset relative logic, this rst req will be auto clear
7	RW	0x0	nlitcoreset3_ac When high, reset relative logic, this rst req will be auto clear
6	RW	0x0	nlitcoreset2_ac When high, reset relative logic, this rst req will be auto clear
5	RW	0x0	nlitcoreset1_ac When high, reset relative logic, this rst req will be auto clear
4	RW	0x0	nlitcoreset0_ac When high, reset relative logic, this rst req will be auto clear
3	RW	0x0	nlitcoreporeset3_ac When high, reset relative logic, this rst req will be auto clear
2	RW	0x0	nlitcoreporeset2_ac When high, reset relative logic, this rst req will be auto clear
1	RW	0x0	nlitcoreporeset1_ac When high, reset relative logic, this rst req will be auto clear
0	RW	0x0	nlitcoreporeset0_ac When high, reset relative logic, this rst req will be auto clear

LITCORECRU_SMOTH_DIVFREE_CON00

Address: Operational Base(0x27240000) + offset (0x0CC0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	clk_litcore_src_freq_keep freq_keep Cycles to keep every step.

Bit	Attr	Reset Value	Description
15	RW	0x1	clk_litcore_src_bypass bypass Division signal bypass. 1'b1: Bypass. 1'b0: Use Smoothdiv to control clock division.
14	RW	0x1	clk_litcore_src_gate_smth_en gate_smth_en If trigger smoothdiv function when clk been gated. 1'b1: Enable. 1'b0: Disable.
13	RW	0x0	clk_litcore_src_smdiv_clk_off smdiv_clk_off Turn off smoothdiv module clk. 1'b1: Turn off. 1'b0: Turn on.
12:5	RO	0x00	reserved
4:0	RW	0x03	clk_litcore_src_step step Step of div from 0x1f to setting configuration .

LITCORECRU_AUTOCS_CLK_LITCORE_SRC_CON0

Address: Operational Base(0x27240000) + offset (0x0F38)

Bit	Attr	Reset Value	Description
31:16	RW	0x0020	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

LITCORECRU_AUTOCS_CLK_LITCORE_SRC_CON1

Address: Operational Base(0x27240000) + offset (0x0F3C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	reserved

2.12 CCI_CRU

2.12.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.12.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CCICRU_LPLL_CON0	0x0040	W	0x00000177	LPLL configuration register 0
CCICRU_LPLL_CON1	0x0044	W	0x00000083	LPLL configuration register 1
CCICRU_LPLL_CON4	0x0050	W	0x00000002	LPLL configuration register 4
CCICRU_LPLL_CON5	0x0054	W	0x000007E0	LPLL configuration register 5
CCICRU_LPLL_CON6	0x0058	W	0x00000000	LPLL configuration register 6
CCICRU_CLKSEL_CON04	0x0310	W	0x0000008A	Internal clock select and division register 4
CCICRU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
CCICRU_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2
CCICRU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1
CCICRU_SOFTRST_CON02	0x0A08	W	0x00000000	Internal clock reset register 2
CCICRU_AUTOCS_CTRL_BIGCORE_EXTRA_CCI	0x0C50	W	0x00000000	auto clock switch control in cci
CCICRU_AUTOCS_CTRL_LITCORE_EXTRA_CCI	0x0C54	W	0x00000000	auto clock switch control in cci
CCICRU_AUTOCS_CTRL_CCI2CORE	0x0C58	W	0x00000000	auto clock switch control in cci
CCICRU_AUTOCS_ACLK_CCI_ROOT_CON0	0x0D00	W	0x00A00047	auto clock switch control 0
CCICRU_AUTOCS_ACLK_CCI_ROOT_CON1	0x0D04	W	0x00000000	auto clock switch control 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.12.3 Detail Registers Description

CCICRU_LPLL_CON0

Address: Operational Base(0x27248000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	lpll_bp BYPASS: Bypass mode control signal. 1'b1: bypass mode is enabled. (FOUT = FIN). 1'b0: PLL operates normally.
14:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x177	lpll_m M: Division value of the 10-bit programmable main-divider. PLL has to be reset if M value is changed. 64 <= pll_m <= 1023

CCICRU_LPLL_CON1

Address: Operational Base(0x27248000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	lpll_resetb RESETB: Power down control signal. 1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time. 1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.
12:9	RO	0x0	reserved
8:6	RW	0x2	lpll_s Division value of the 3-bit programmable scaler. 0 <= pll_s <= 6
5:0	RW	0x03	lpll_p P: Division value of the 6-bit programmable pre-divider. PLL has to be reset if P value is changed. 1 <= pll_p <= 63

CCICRU_LPLL_CON4

Address: Operational Base(0x27248000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	lpll_fsel FSEL: Monitoring pin. 1'b0: FEED_OUT = FREF. 1'b1: FEED_OUT = FEED.
14	RW	0x0	lpll_feed_en FEED_EN: Monitoring pin. 1'b0: FEED_OUT is disabled. 1'b1: FEED_OUT is enabled.
13:9	RO	0x00	reserved
8:4	RW	0x00	lpll_extafc EXTAFC: Monitoring pin. If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
3	RW	0x0	lpll_afc_enb AFC_ENB: Monitoring pin. 1'b0: AFC is enabled and VCO is calibrated automatically. 1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range.
2:1	RW	0x1	lpll_icp Charge-pump current control signal.

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Bit	Attr	Reset Value	Description
0	RO	0x0	reserved

CCICRU_LPLL_CON5

Address: Operational Base(0x27248000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:9	RW	0x3	lpll_lock_con_dly LOCK_CON_DLY: Lock detector setting of the detection resolution.
8:7	RW	0x3	lpll_lock_con_out LOCK_CON_OUT: Lock detector setting of the output margin.
6:5	RW	0x3	lpll_lock_con_in LOCK_CON_IN: Lock detector setting of the input margin.
4:1	RO	0x0	reserved
0	RW	0x0	lpll_fout_mask FOUT_MASK: Scaler's re-initialization time control pin.

CCICRU_LPLL_CON6

Address: Operational Base(0x27248000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	lpll_lock LOCK: PLL lock flag. 1'b0: PLL is unlocked. 1'b1: PLL is locked.
14:10	RW	0x00	lpll_afc_code AFC_CODE: Monitoring pin. Output code of AFC(5 bits).
9:0	RO	0x000	reserved

CCICRU_CLKSEL_CON04

Address: Operational Base(0x27248000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_cci_pvtpll_src_sel clk_cci_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_cci_pvtpll
13:12	RW	0x0	aclk_cci_root_sel aclk_cci_root clock mux. 2'b00: xin_osc0_func 2'b01: clk_cci_pvtpll_src 2'b10: clk_gpll_mux 2'b11: clk_lpll

Bit	Attr	Reset Value	Description
11:7	RW	0x01	aclk_cci_root_div Divide aclk_cci_root by (div_con + 1).
6:5	RW	0x0	pclk_cci_root_sel pclk_cci_root clock mux. 2'b00: xin_osc0_func 2'b01: clk_cci_pvtpll_src 2'b10: clk_gpll_mux 2'b11: clk_lpll
4:0	RW	0x0a	pclk_cci_root_div Divide pclk_cci_root by (div_con + 1).

CCICRU_GATE_CON01

Address: Operational Base(0x27248000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_dbg_m_en pclk_dbg_m clock gating control. When high, disable clock
14	RW	0x0	aclk_cci_biu_en aclk_cci_biu clock gating control. When high, disable clock
13	RW	0x0	pclk_cci_biu_en pclk_cci_biu clock gating control. When high, disable clock
12	RW	0x0	aclk_cpe_en aclk_cpe clock gating control. When high, disable clock
11	RW	0x0	aclk_cci_root_en aclk_cci_root clock gating control. When high, disable clock
10	RW	0x0	pclk_cci_root_en pclk_cci_root clock gating control. When high, disable clock
9:0	RO	0x000	reserved

CCICRU_GATE_CON02

Address: Operational Base(0x27248000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_ref_pvtpll_cci_en clk_ref_pvtpll_cci clock gating control. When high, disable clock
11	RW	0x0	pclk_dbg_m_biu_en pclk_dbg_m_biu clock gating control. When high, disable clock
10	RW	0x0	pclk_cci_ddrsch_biu_en pclk_cci_ddrsch_biu clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
9	RO	0x0	reserved
8	RW	0x0	pclk_pvtpll_cci_en pclk_pvtpll_cci clock gating control. When high, disable clock
7	RW	0x0	aclk_adb400_cci_a53_en aclk_adb400_cci_a53 clock gating control. When high, disable clock
6	RW	0x0	aclk_adb400_cci_a72_en aclk_adb400_cci_a72 clock gating control. When high, disable clock
5	RW	0x0	aclk_cci_ddrsch_biu_en aclk_cci_ddrsch_biu clock gating control. When high, disable clock
4	RO	0x0	reserved
3	RW	0x0	aclk_cci_en aclk_cci clock gating control. When high, disable clock
2	RW	0x0	pclk_cci_cru_en pclk_cci_cru clock gating control. When high, disable clock
1	RW	0x0	pclk_cci_grf_en pclk_cci_grf clock gating control. When high, disable clock
0	RW	0x0	pclk_dbg_sys_en pclk_dbg_sys clock gating control. When high, disable clock

CCICRU_SOFTRST_CON01

Address: Operational Base(0x27248000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_dbg_m When high, reset relative logic
14	RW	0x0	aresetn_cci_biu When high, reset relative logic
13	RW	0x0	presetn_cci_biu When high, reset relative logic
12	RW	0x0	aresetn_cpe When high, reset relative logic
11:0	RO	0x000	reserved

CCICRU_SOFTRST_CON02

Address: Operational Base(0x27248000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	resetn_ref_cci_pvtpll When high, reset relative logic

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Bit	Attr	Reset Value	Description
11	RW	0x0	presetn_dbg_m_biu When high, reset relative logic
10	RW	0x0	presetn_cci_ddrsch_biu When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	presetn_pvtpll_cci When high, reset relative logic
7	RW	0x0	aresetn_adb400_cci_a53 When high, reset relative logic
6	RW	0x0	aresetn_adb400_cci_a72 When high, reset relative logic
5	RW	0x0	aresetn_cci_ddrsch_biu When high, reset relative logic
4	RW	0x0	poresetn_jtag When high, reset relative logic
3	RW	0x0	aresetn_cci When high, reset relative logic
2	RW	0x0	presetn_cci_cru When high, reset relative logic
1	RW	0x0	presetn_cci_grf When high, reset relative logic
0	RW	0x0	presetn_dbg_sys When high, reset relative logic

CCICRU_AUTOCS_CTRL_BIGCORE_EXTRA_CCI

Address: Operational Base(0x27248000) + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	autocs_cci2bigcore_ctrl autocs_cci2bigcore_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: bigcore0 standbywfi autocs control; bit1: bigcore0 standbywfe autocs control; bit2: bigcore0 pd_dwn_stat autocs control; bit3: bigcore0 gic_irqfiq_active autocs control; bit4: bigcore1 standbywfi autocs control; bit5: bigcore1 standbywfe autocs control; bit6: bigcore1 pd_dwn_stat autocs control; bit7: bigcore1 gic_irqfiq_active autocs control; bit8: bigcore2 standbywfi autocs control; bit9: bigcore2 standbywfe autocs control; bit10: bigcore2 pd_dwn_stat autocs control; bit11: bigcore2 gic_irqfiq_active autocs control; bit12: bigcore3 standbywfi autocs control; bit13: bigcore3 standbywfe autocs control; bit14: bigcore3 pd_dwn_stat autocs control; bit15: bigcore3 gic_irqfiq_active autocs control;

CCICRU_AUTOCS_CTRL_LITCORE_EXTRA_CCI

Address: Operational Base(0x27248000) + offset (0x0C54)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	autocs_cci2litcore_ctrl autocs_cci2litcore_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: litcore0 standbywfi autocs control; bit1: litcore0 standbywfe autocs control; bit2: litcore0 pd_dwn_stat autocs control; bit3: litcore0 gic_irqfiq_active autocs control; bit4: litcore1 standbywfi autocs control; bit5: litcore1 standbywfe autocs control; bit6: litcore1 pd_dwn_stat autocs control; bit7: litcore1 gic_irqfiq_active autocs control; bit8: litcore2 standbywfi autocs control; bit9: litcore2 standbywfe autocs control; bit10: litcore2 pd_dwn_stat autocs control; bit11: litcore2 gic_irqfiq_active autocs control; bit12: litcore3 standbywfi autocs control; bit13: litcore3 standbywfe autocs control; bit14: litcore3 pd_dwn_stat autocs control; bit15: litcore3 gic_irqfiq_active autocs control;

CCICRU_AUTOCS_CTRL_CCI2CORE

Address: Operational Base(0x27248000) + offset (0x0C58)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	autocs_cci2litcore_ctrl autocs_cci2litcore_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: litcore idle for litcore_autocs control; when enable, only 4*a53 idle to enable litcore autocs bit1: bigcore idle for litcore_autocs control; when enable, only 4*a72 idle to enable litcore autocs bit2: bigcore idle for bigcore_autocs control; when enable, only 4*a72 idle to enable bigcore autocs bit3: litcore idle for bigcore_autocs control; when enable, only 4*a53 idle to enable bigcore autocs bit4: center2cci noc pwractive control for bigcore0 idle; bit5: center2cci noc pwractive control for bigcore1 idle; bit6: center2cci noc pwractive control for bigcore2 idle; bit7: center2cci noc pwractive control for bigcore3 idle; bit8: center2cci noc pwractive control for litcore0 idle; bit9: center2cci noc pwractive control for litcore1 idle; bit10: center2cci noc pwractive control for litcore2 idle; bit11: center2cci noc pwractive control for litcore3 idle;

CCICRU_AUTOCS_ACLK_CCI_ROOT_CON0

Address: Operational Base(0x27248000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original source clk
15:4	RW	0x004	idle_th idle time threshold, measured by original source clk idle_time = idle_th * 16
3	RW	0x0	autocs_gate 1'b1: gate autocs div clk 1'b0: not gate autocs div clk
2:0	RW	0x7	autocs_div source clk is dived by (autocs_div + 1)

CCICRU_AUTOCS_ACLK_CCI_ROOT_CON1

Address: Operational Base(0x27248000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock select 2'b00: original clk 2'b01: xin_osc0_func 2'b10: div clk from original clk, div reg can be configured
13	RW	0x0	switch_en switch en 1'b1: switch clk enable 1'b0: switch clk disable
12	RW	0x0	autocs_en autocs en 1'b1: autocs enable 1'b0: autocs disable
11	RO	0x0	reserved
10:0	RW	0x000	autocs_active autocs_ctrl The autocs ctrl enable for internal hardware signal. all bits: 1'b0, disable ; 1'b1, enable. bit0: autocs_idle_bigcore & autocs_idle_litcore control; bit1: noc active_cci2center control; bit4: noc active_cci2ddrch0 control; bit5: noc active_cci2ddrch1 control; bit6: noc active_center2cci control; bit7: aclk_qactive_cci control; bit2-3,bit8-11: reserved;

2.13 Application Notes

2.13.1 PLL Usage

2.13.1.1 Start-up Operation

Set the registers (such as P[5:0], M[9:0] and so on) at time t3 after setting the power from 0V to VDD at time t2.

Set RESETB=0 before PLL starts to operate. Then set RESETB=1 at t4 to initialize PLL and to start AFC. Note that PLL generates a clock signal with the desired frequency only after lock time has passed.

PLL must be initialized before you change the value of P[5:0] and M[9:0]. However S[2:0] and BYPASS can be changed without the initialization of PLL. The other input pins are not

allowed to be changed after PLL is locked.
To ensure that the register values and operation-mode controls are stable, the time interval of Δt1(t4-t2) should be greater than 1μs and Δt2(t4-t3) should be greater than 1/F_{FREF} respectively.

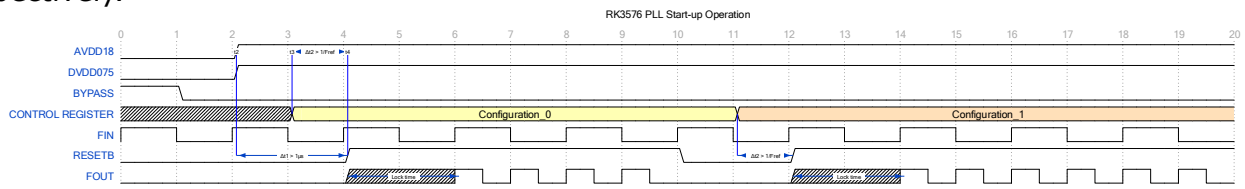

Fig 2-6 PLL Start-up Operation

2.13.1.2 Bypass Operation

Bypass mode works only when PLL is operating (RESETB=1). When ΔT > lock time (as illustrated in Figure below), PLL generates a stable clock signal with desired target frequency.

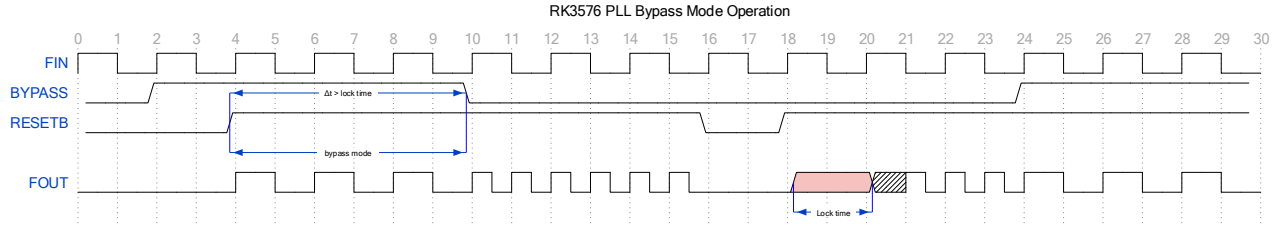

Fig 2-7 PLL Bypass Operation

2.13.1.3 Glitch-free Scaler Operation

S[2:0] can be changed after PLL is locked. The timing diagram of glitch-free scaler is illustrated in the figure below.
When S[2:0] or BYPASS is changed, FOUT first maintains output frequency during max 3 cycles of FIN and then moves to logic low for 2 cycles of FIN. After completing the re-initialization time, FOUT goes to the desired frequency.
To guarantee the glitch-free functionality of scaler in PLL which needs re-initialization time for max 5 cycles of FIN, FIN has to be lower than FOUT. If FIN is higher than FOUT, set FOUT_MASK=1. Note that the maximum re-initialization time for the case of FOUT_MASK=1 takes 8 times longer than that for the case of FOUT_MASK=0.

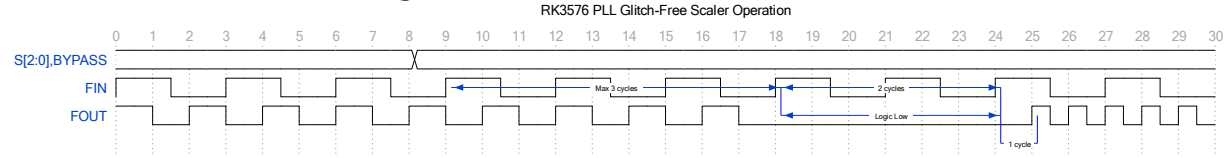

Fig 2-8 PLL Glitch-free Scaler Operation

2.13.1.4 Setting Guide on P, M, S, and K

p, m, s, and k are decimal values of P[5:0], M[9:0], S[2:0], and K[15:0], respectively. (where p = P[5:0], m = M[9:0], s = S[2:0], and k = K[15:0])
F_{VCO} and F_{OUT} are calculated by the following equation.

PLL Type	Equation
FRACPLL	$F_{VCO} = ((m + k / 65536) * F_{IN}) / p$ $F_{OUT} = ((m + k / 65536) * F_{IN}) / (p * 2^s)$
DDRPLL	$F_{VCO} = ((m + k / 65536) * 2 * F_{IN}) / p$ $F_{OUT} = ((m + k / 65536) * 2 * F_{IN}) / (p * 2^s)$
INTPLL	$F_{VCO} = (m * F_{IN}) / p$ $F_{OUT} = (m * F_{IN}) / (p * 2^s)$
Parameter	1 <= p <= 63, 64 <= m <= 1023, 0 <= s <= 6

P[5:0], M[9:0] and S[2:0] are unsigned integers. K[15:0] is a two's complement integer.
6'b00_0001 <= P[5:0] <= 6'b11_1111
10'b00_0100_0000 <= M[9:0] <= 10'b11_1111_1111
3'b000 <= S[2:0] <= 3'b110
16'b1000_0000_0000_0000 <= K[15:0] <= 16'b0111_1111_1111_1111
Setting P[5:0] or M[9:0] to all zero is strictly prohibited while RESETB = 1. (6'b00_0000 /

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10'b00_0000_0000) The division ratio of scaler is controlled by S[2:0] as summarized.

2.13.1.5 Setting Guide on SSCG_EN, SEL_PF, MFR and MRR

When SSCG_EN is set to logic high, the spread spectrum mode is enabled.
Sel_pf, mfr, and mrr are decimal values of SEL_PF[1:0], MFR[7:0] and MRR[5:0], respectively. (where sel_pf = SEL_PF[1:0], mfr = MFR[7:0], mrr = MRR[5:0])
Modulation frequency, MF, is determined by the following equation:

MF = F_{IN} / p / mfr / (2)[Hz].

Modulation rate(pk-pk), MR, is determined by the following equation:

MR = mfr * mrr / m / (2) * 100 [%].

Modulation mode is determined by sel_pf.

00: down spread, 01: up spread, 1x: center spread

Range of registers.

8'b0000_0000 <= MFR[7:0] <= 8'b1111_1111
6'b00_0001 <= MRR[5:0] <= 6'b11_1111
0 <= mrr * mfr <= 512
2'b00 <= SEL_PF[1:0] <= 2'b10

2.13.1.6 Setting Guide on RESETB and BYPASS

RESETB is the reset signal of PLL. PLL enters power down mode when RESETB = 0.
BYPASS enables the bypass mode of PLL. When BYPASS = 1, PLL enters the bypass mode and FOUT is equal to FIN.

2.13.2 Divider Usage

CRU supports multi-dividers for different clock requirement.

- Divider free divider
- Fractional divider
- DivfreeDT50 divider(DT50)
- DivfreeNP5 divider(NP5)

2.13.2.1 DivFree Divider Usage

Frequency of this divider = clk_src / (n+1).

2.13.2.2 Fractional Divider Usage

To get specific frequency, clocks of I2S, audio PWM, UART and SPDIF can be generated by fractional divider. Generally you should set that denominator 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock.

2.13.2.3 DivfreeDT50 Divider Usage

Some modules like EMMC, SDIO, SDMMC need clock of 50% duty cycle, divfreedt50 can generate clock of 50% duty cycle even in odd value divisor.

2.13.2.4 DivFreeNP5 Divider Usage

Some modules which need some special frequency can use this divider. Frequency of this divider=clk_src/(n+1.5).

2.13.3 Global Software Reset

Two global software resets are designed in RK3576. These two software resets are self-de-asserted by hardware. Hold time of global software reset (glb_srstn_1, glb_srstn_2, wdt_rstn, tsadc_rstn) can be programed up to 1ms.

- Set CRU_GLB_SRST_FST_VALUE[15:0] = 0xfdb9 to assert the first global software reset glb_srstn_1.
- Set CRU_GLB_SRST_SND_VALUE[15:0] = 0xeca8 to assert the second global software reset glb_srstn_2.
- glb_srstn_1 resets almost all logic except some registers just supporting hardware reset.

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- glb_srstn_2 resets almost all logic except GRFs and GPIOs.

Reset for IP in PD_PMU can be hold if its reset_hold_enable in PMUGRF_PMU_SOC_CON1 or PMUGRF_PMU_SOC_CON2 is high even if glb_srstn_1 or glb_srstn_2 is active.

2.13.4 BIU Clock gating reliance

In same pd, pclk_biu and hclk_biu are relied, and pclk_biu, hclk_biu are relied to aclk_biu. Also, some BIU clocks are relied to other pd BIU clk, which is shown as following:

Clocks which have dependency	The clock which can not be gated
aclk_ufs_biu	aclk_usb_biu
aclk_usb_biu	aclk_vop_biu
aclk_vo0_biu	aclk_vop_biu、aclk_vo0vop_channel_biu
aclk_vo1_biu	aclk_vop_biu
aclk_vepu0_biu	aclk_vi_biu
aclk_vepu1_biu	aclk_vi_biu
aclk_vi_biu	aclk_top_biu
aclk_top_mid_biu	aclk_top_biu
aclk_php_biu	aclk_top_mid_biu
aclk_bus_biu	aclk_top_mid_biu
aclk_pmu_biu	aclk_top_mid_biu
aclk_gmac_biu	aclk_nvm_biu
aclk_nvm_biu	aclk_secure_biu
aclk_secure_biu	aclk_secure_high_biu
aclk_rga_biu	aclk_secure_high_biu
aclk_vdpp_biu aclk_jpeg_biu aclk_ebc_biu	aclk_rga_biu

Chapter 3 CPU

3.1 Overview

There are two clusters which implement big.LITTLE architecture in RK3576, Big cluster is composed of 4xCortex-A72 cores and 1MB L2 cache, Little cluster is composed of 4xCortex-A53 cores and 512KB L2 cache. The two clusters connects to cache coherent interconnect(CCI-500) through asynchronous domain bridges(ADB-400) which can handle with clock/power/voltage domain crossing issue. The CCI-500 can enable hardware-coherent between clusters to improve system performance. Please refer to Chapter CCI-500 for more details.

3.1.1 Features

3.1.1.1 Cortex-A72 Cluster Feature

- Full implementation of the ARMv8-A architecture instruction set
- Support for both AArch32 and AArch64 Execution status
- Support for all exception levels, EL0, EL1, EL2, and EL3, in each execution states
- Support A32 instruction set, previously called the ARM instruction set
- Support T32 instruction set, previously called the Thumb instruction set
- Support A64 instruction set
- Superscalar, variable-length, out-of-order pipeline
- Dynamic branch prediction with Branch Target Buffer (BTB) and Global History Buffer (GHB) RAMs, a return stack, and an indirect predictor
- 48-entry fully-associative L1 instruction Translation Lookaside Buffer (TLB) with native support for 4KB, 64KB, and 1MB page sizes
- 32-entry fully-associative L1 data TLB with native support for 4KB, 64KB, and 1MB page sizes
- Level 2 (L2) memory system providing cluster memory coherency, with L2 cache
- Support advanced SIMD and Floating-point Extension for integer and floating-point vector operations
- Support ARMv8 Cryptography Extensions
- Support AMBA 4 ACE bus architecture

The configuration details of big cluster are shown in following tables

Table 3-1 Big Cluster Configuration

Number of CPU	4
L1 I cache size	48KB
L1 D cache size	32KB
L2 cache size	1MB
L2 data RAM output latency	3 cycles
L2 data RAM input latency	2 cycles
CPU cache protection	No
SCU L2 cache protection	No
BUS master interface	ACE
NEON and floating point support	Yes
Cryptography extension	Yes

3.1.1.2 Cortex-A53 Cluster Feature

- Full implementation of the ARMv8-A architecture instruction set
- Support for both AArch32 and AArch64 Execution status
- Support for all exception levels, EL0, EL1, EL2, and EL3, in each execution states
- Support A32 instruction set, previously called the ARM instruction set
- Support T32 instruction set, previously called the Thumb instruction set
- Support A64 instruction set

- In-order pipeline with symmetric dual-issue of most instructions
- Harvard Level 1(L1) memory system with a Memory Management Unit (MMU)
- Level 2 (L2) memory system providing cluster memory coherency, with L2 cache
- Support advanced SIMD and Floating-point Extension for integer and floating-point vector operations
- Support ARMv8 Cryptography Extensions
- Support AMBA 4 ACE bus architecture

The configuration details of little cluster are shown in following tables

Table 3-2 Little Core Configuration

Number of CPU	4
L1 I cache size	32K
L1 D cache size	32K
L2 cache size	512K
L2 data RAM output latency	3 cycles
L2 data RAM input latency	2 cycles
CPU cache protection	No
SCU L2 cache protection	No
BUS master interface	ACE
NEON and floating point support	Yes
Cryptography extension	Yes

3.2 Block Diagram

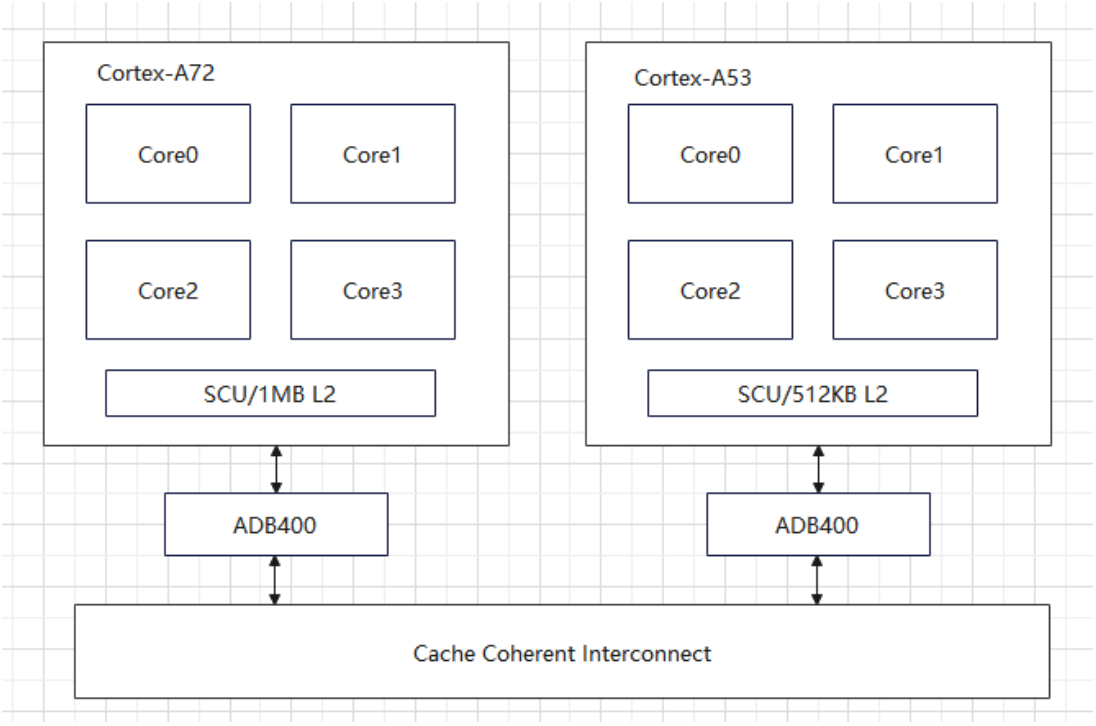

Fig. 3-1 CPU subsystem structure

3.3 Function Description

- Please refer to the document Cortex-A72_MPCore_Technical_Reference_Manual_r1p0-00rel0.pdf for the detail function description

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- Please refer to the document DDI0500J_cortex_a53_r0p4_trm.pdf for the detail function description
- Please refer to the document DUI0615G_adb400_r3p0_ug.pdf for the detail function description

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Chapter 4 GPU (Graphics Process Unit)

4.1 Overview

The Mali-Gondul GPU is a graphics acceleration platform that is based on open standards. It supports 2D graphics, 3D graphics, and General Purpose computing on GPU (GPGPU).
The GPU hardware and software support compute standards and graphics API standards.
The GPU supports these compute API standards:

- OpenCL 2.0 Full Profile.

The GPU supports these graphics API standards:

- OpenGLES 1.1, 2.0, and 3.2.
- Vulkan 1.0 and 1.1.

The Arm Mali-Gondul GPU has significant features and properties.

- Compressed texture formats.
- Arm Frame Buffer Compression (AFBC) 1.2
- 8-bit, 10-bit and 16-bit YUV input and output formats
- L2 cache:256KB
- Support three Shader core and two execution engines

4.2 Block Diagram

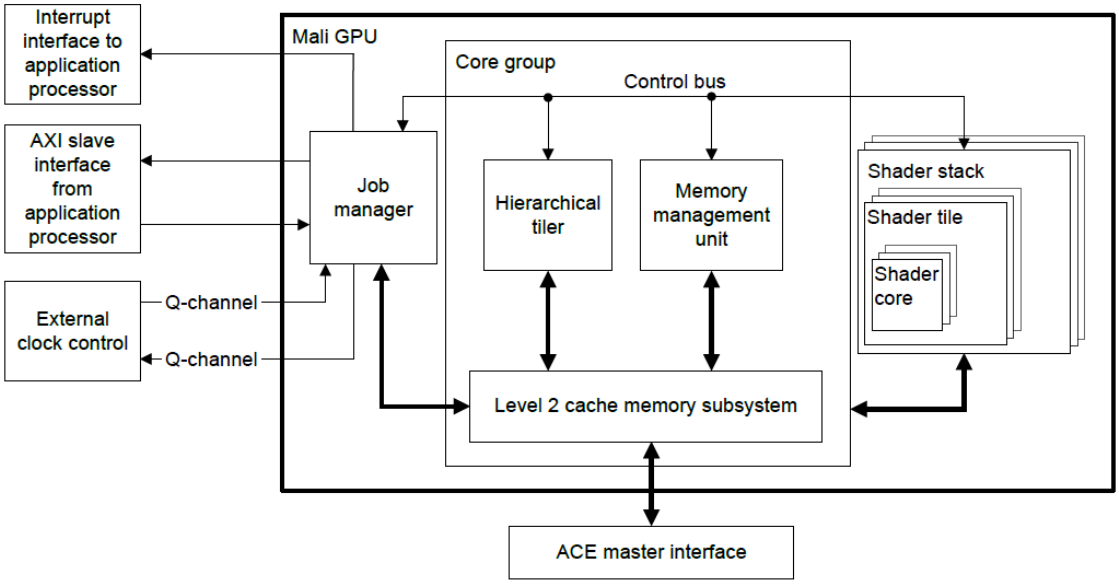

Fig. 4-1 GPU Architecture

4.3 Function Description

Please refer to the document "ARM_Gondul_r1p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

4.4 Register Description

Please refer to the document "ARM_Gondul_r1p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

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Chapter 5 General Register Files (GRF)

5.1 Overview

The general register file will be used to do static setting by software, which is composed of many registers for system control. The GRF is located at several addresses.

5.2 Function Description

The function of general register file is：

- Common system control
- Record the system state
- GPIO MUX control
- GPIO PAD Control

5.3 PMU0_GRF Register Description

5.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU0_GRF_SOC_CON0	0x0000	W	0x00000001	System control register 0
PMU0_GRF_SOC_CON1	0x0004	W	0x00000000	System control register 1
PMU0_GRF_SOC_CON2	0x0008	W	0x00000000	System control register 2
PMU0_GRF_SOC_CON4	0x0010	W	0x000000FF	System control register 4
PMU0_GRF_SOC_CON5	0x0014	W	0x00000000	System control register 5
PMU0_GRF_SOC_CON6	0x0018	W	0x00000000	System control register 6
PMU0_GRF_IO_RET_CON0	0x0020	W	0x00000000	IO retention control register 0
PMU0_GRF_IO_RET_CON1	0x0024	W	0x00000000	IO retention control register 1
PMU0_GRF_MEM_CON	0x0030	W	0x00001410	Memory Configure register
PMU0_GRF_OS_REG16	0x0040	W	0x00000000	Operation system register 16
PMU0_GRF_OS_REG17	0x0044	W	0x00000000	Operation system register 17
PMU0_GRF_OS_REG18	0x0048	W	0x00000000	Operation system register 18
PMU0_GRF_OS_REG19	0x004C	W	0x00000000	Operation system register 19
PMU0_GRF_OS_REG20	0x0050	W	0x00000000	Operation system register 20
PMU0_GRF_OS_REG21	0x0054	W	0x00000000	Operation system register 21
PMU0_GRF_OS_REG22	0x0058	W	0x00000000	Operation system register 22
PMU0_GRF_OS_REG23	0x005C	W	0x00000000	Operation system register 23

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.3.2 Detail Registers Description

PMU0_GRF_SOC_CON0

Address: Operational Base(0x26024000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	ref_clk2_out_sel Clock selection for ref_clk2_out. 2'h0: Select from divider output of PLL 2'h1: Select from oscillator 2'h2: Select from oscillator divided by 2 Others: Reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x0	ref_clk1_out_sel Clock selection for ref_clk1_out. 2'h0: Select from divider output of PLL 2'h1: Select from oscillator 2'h2: Select from oscillator divided by 2 Others: Reserved
11:10	RW	0x0	ref_clk0_out_sel Clock selection for ref_clk0_out. 2'h0: Select from divider output of PLL 2'h1: Select from oscillator 2'h2: Select from oscillator divided by 2 Others: Reserved
9	RW	0x0	pwr_sleep_2_pol Polarity of pwr_sleep_2. 1'b0: High active 1'b1: Low active
8	RW	0x0	pwr_sleep_1_pol Polarity of pwr_sleep_1. 1'b0: High active 1'b1: Low active
7	RW	0x0	pwr_sleep_0_pol Polarity of pwr_sleep_0. 1'b0: High active 1'b1: Low active
6	RW	0x0	pmic_int_pol Polarity of PMIC int. 1'b0: High active 1'b1: Low active
5	RW	0x0	clk_battery_pwrup_gate_en Enable clock gating for battery power up logic. 1'b0: Disable 1'b1: Enable
4	RW	0x0	resetn_battery_pwrup_hold_ena Enable reset hold for battery power up logic. 1'b0: Disable 1'b1: Enable
3	RW	0x0	dbclk_gpio0_sel Clock selection for dbclk_gpio0. 1'b0: Select from oscillator 1'b1: Select from clk_deepslow
2:1	RW	0x0	clk_deepslow_sel Clock selection for clk_deepslow. 2'h0: Select from divider output of oscillator 2'h1: Select from external IO clock 2'h2: Select from divider output of PMU_PVTM Others: Reserved
0	RW	0x1	pd_pmu1_repair_enable Enable memory repair for PD_PMU1. 1'b0: Disable 1'b1: Enable

PMU0_GRF_SOC_CON1

Address: Operational Base(0x26024000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pwr_sleep_2_sftena pwr_sleep_2 generated by software. 1'b0: Inactive 1'b1: Active
13	RW	0x0	pwr_sleep_1_sftena pwr_sleep_1 generated by software. 1'b0: Inactive 1'b1: Active
12	RW	0x0	pwr_sleep_0_sftena pwr_sleep_0 generated by software. 1'b0: Inactive 1'b1: Active
11:8	RW	0x0	pwr_sleep_2_src_sel Source selection for pwr_sleep_2. 4'h1: VD_NPU power off request 4'h2: VD_GPU power off request 4'h3: VD_LITCORE power off request 4'h4: VD_BIGCORE power off request 4'h5: VD_DDR power off request 4'h6: Chip reset output 4'h7: Low power mode or deep low power mode 4'h8: Deep low power mode 4'h9: Low power mode Default: Controlled by software
7:4	RW	0x0	pwr_sleep_1_src_sel Source selection for pwr_sleep_1. 4'h1: VD_NPU power off request 4'h2: VD_GPU power off request 4'h3: VD_LITCORE power off request 4'h4: VD_BIGCORE power off request 4'h5: VD_DDR power off request 4'h6: Chip reset output 4'h7: Low power mode or deep low power mode 4'h8: Deep low power mode 4'h9: Low power mode Default: Controlled by software
3:0	RW	0x0	pwr_sleep_0_src_sel Source selection for pwr_sleep_0. 4'h1: VD_NPU power off request 4'h2: VD_GPU power off request 4'h3: VD_LITCORE power off request 4'h4: VD_BIGCORE power off request 4'h5: VD_DDR power off request 4'h6: Chip reset output 4'h7: Low power mode or deep low power mode 4'h8: Deep low power mode 4'h9: Low power mode Default: Controlled by software

PMU0_GRF_SOC_CON2

Address: Operational Base(0x26024000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x000	pmupvtm_clkout_div Clock divide factor for clock generated by PMU_PVTM. The actual factor equals to {pmupvtm_clkout_div[11:2],2'b0}.

PMU0_GRF_SOC_CON4

Address: Operational Base(0x26024000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x3	ddr_io_rstiov_sel Enable DDR IO rstiov source selection. 1'b0: From hardware 1'b1: From software, ddr_io_rstiov_sftena bit[0]: Used for DDR IO channel 0 bit[1]: Used for DDR IO channel 1
5:4	RW	0x3	ddr_io_reton_sel Enable DDR IO reton source selection. 1'b0: From hardware 1'b1: From software, ddr_io_reton_sftena bit[0]: Used for DDR IO channel 0 bit[1]: Used for DDR IO channel 1
3:2	RW	0x3	ddr_io_rstiov_sftena Enable DDR IO rstiov by software. 1'b0: Exit retention mode 1'b1: Enter retention mode bit[0]: Used for DDR IO channel 0 bit[1]: Used for DDR IO channel 1
1:0	RW	0x3	ddr_io_reton_sftena Enable DDR IO reton by software. 1'b0: Exit retention mode 1'b1: Enter retention mode bit[0]: Used for DDR IO channel 0 bit[1]: Used for DDR IO channel 1

PMU0_GRF_SOC_CON5

Address: Operational Base(0x26024000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	ppll_pll_clamp Enable clamping for PPLL. 1'b0: Disable 1'b1: Enable Detail application guide refers to PMU chapter.

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Bit	Attr	Reset Value	Description
5	RW	0x0	usbphy1_usbphy_clamp_ena Enable clamping for USB2PHY_1 when VD_USBPHY's power supply is neither VDD_PMU nor VDD_LOGIC. 1'b0: Disable 1'b1: Enable. USB2PHY_1's output interface is clamped when VD_USBPHY's power supply is off. Detail application guide refers to PMU chapter.
4	RW	0x0	usbphy1_vddpmu_clamp_ena Enable clamping for USB2PHY_1 when VD_USBPHY's power supply is VDD_PMU. 1'b0: Disable 1'b1: Enable. USB2PHY_1's input interface is clamped when VDD_LOGIC is off. Detail application guide refers to PMU chapter.
3	RW	0x0	usbphy1_vddlogic_clamp_ena Enable clamping for USB2PHY_1 when VD_USBPHY's power supply is VDD_LOGIC. 1'b0: Disable 1'b1: Enable. USB2PHY_1's interface output to VD_PMU is clamped when VDD_LOGIC is off. Detail application guide refers to PMU chapter.
2	RW	0x0	usbphy0_usbphy_clamp_ena Enable clamping for USB2PHY_0 when VD_USBPHY's power supply is neither VDD_PMU nor VDD_LOGIC. 1'b0: Disable 1'b1: Enable. USB2PHY_0's output interface is clamped when VD_USBPHY's power supply is off. Detail application guide refers to PMU chapter.
1	RW	0x0	usbphy0_vddpmu_clamp_ena Enable clamping for USB2PHY_0 when VD_USBPHY's power supply is VDD_PMU. 1'b0: Disable 1'b1: Enable. USB2PHY_0's input interface is clamped when VDD_LOGIC is off. Detail application guide refers to PMU chapter.
0	RW	0x0	usbphy0_vddlogic_clamp_ena Enable clamping for USB2PHY_0 when VD_USBPHY's power supply is VDD_LOGIC. 1'b0: Disable 1'b1: Enable. USB2PHY_0's interface output to VD_PMU is clamped when VDD_LOGIC is off. Detail application guide refers to PMU chapter.

PMU0_GRF_SOC_CON6

Address: Operational Base(0x26024000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	xin_osc0_phy_bd_en Clock gate enable for oscillator output as PHY reference clock with big driver path. 1'b0: Clock enable 1'b1: Clock gate

Bit	Attr	Reset Value	Description
8	RW	0x0	xin_osc0_phy_sd_en Clock gate enable for oscillator output as PHY reference clock with small driver path. 1'b0: Clock enable 1'b1: Clock gate
7	RW	0x0	xin_osc0_pll_bd_en Clock gate enable for oscillator output as PLL reference clock with big driver path. 1'b0: Clock enable 1'b1: Clock gate
6	RW	0x0	xin_osc0_pll_sd_en Clock gate enable for oscillator output as PLL reference clock with small driver path. 1'b0: Clock enable 1'b1: Clock gate
5	RW	0x0	clk_phy_ref_src_sel Clock selection for PHY reference clock. 1'b0: Select from oscillator 1'b1: Select from divider output of CPLL
4	RW	0x0	xin_osc0_phy_sel Path selection for oscillator output as PHY reference clock. 1'b0: Big driver path 1'b1: Small driver path
3	RW	0x0	xin_osc0_pll_sel Path selection for oscillator output as PLL reference clock. 1'b0: Big driver path 1'b1: Small driver path
2	RW	0x0	usbphy_clk24m_sel Clock selection for USBPHY 24MHz clock. 1'b0: Select from USB2PHY_0 1'b1: Select from USB2PHY_1
1	RW	0x0	cpll_refclk_in_sel Clock selection for CPLL reference clock. 1'b0: Select from oscillator 1'b1: Select from USBPHY 24MHz clock
0	RW	0x0	aupll_refclk_in_sel Clock selection for AUPLL reference clock. 1'b0: Select from oscillator 1'b1: Select from external IO

PMU0_GRF_IO_RET_CON0

Address: Operational Base(0x26024000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pmuio1_ret_ena Enable PMUIO1 retention mode by hardware. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
7	RW	0x0	vccio7_ret_ena Enable VCCIO7 retention mode by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	vccio6_ret_ena Enable VCCIO6 retention mode by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	vccio5_ret_ena Enable VCCIO5 retention mode by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	vccio4_ret_ena Enable VCCIO4 retention mode by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	vccio3_ret_ena Enable VCCIO3 retention mode by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	vccio2_ret_ena Enable VCCIO2 retention mode by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	vccio1_ret_ena Enable VCCIO1 retention mode by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	vccio0_ret_ena Enable VCCIO0 retention mode by hardware. 1'b0: Disable 1'b1: Enable

PMU0_GRF_IO_RET_CON1

Address: Operational Base(0x26024000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pmuio1_ret_sftena Enable PMUIO1 retention mode by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	vccio7_ret_sftena Enable VCCIO7 retention mode by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	vccio6_ret_sftena Enable VCCIO6 retention mode by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	vccio5_ret_sftena Enable VCCIO5 retention mode by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	vccio4_ret_sftena Enable VCCIO4 retention mode by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	vccio3_ret_sftena Enable VCCIO3 retention mode by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	vccio2_ret_sftena Enable VCCIO2 retention mode by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	vccio1_ret_sftena Enable VCCIO1 retention mode by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	vccio0_ret_sftena Enable VCCIO0 retention mode by software. 1'b0: Disable 1'b1: Enable

PMU0_GRF_MEM_CON

Address: Operational Base(0x26024000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x1410	pmu0_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_PMU0. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

PMU0_GRF_OS_REG16

Address: Operational Base(0x26024000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, cannot be reset.

PMU0_GRF_OS_REG17

Address: Operational Base(0x26024000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, cannot be reset.

PMU0_GRF_OS_REG18

Address: Operational Base(0x26024000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, cannot be reset.

PMU0_GRF_OS_REG19

Address: Operational Base(0x26024000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, cannot be reset.

PMU0_GRF_OS_REG20

Address: Operational Base(0x26024000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, cannot be reset.

PMU0_GRF_OS_REG21

Address: Operational Base(0x26024000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, cannot be reset.

PMU0_GRF_OS_REG22

Address: Operational Base(0x26024000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, cannot be reset.

PMU0_GRF_OS_REG23

Address: Operational Base(0x26024000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, cannot be reset.

5.4 PMU1_GRF Register Description

5.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU1_GRF_SOC_CON0	0x0000	W	0x00000000	System control register 0
PMU1_GRF_SOC_CON1	0x0004	W	0x0000000C	System control register 1
PMU1_GRF_SOC_CON6	0x0018	W	0x00000000	System control register 6
PMU1_GRF_SOC_CON7	0x001C	W	0xFFFFFFFF	System control register 7
PMU1_GRF_BIU_CON	0x0050	W	0x00000000	BIU interface control register
PMU1_GRF_BIU_STATUS	0x0054	W	0x00000000	BIU interface status register
PMU1_GRF_SOC_STATUS	0x0060	W	0x00000000	System status register
PMU1_GRF_MEM_CON0	0x0080	W	0x00001410	Memory interface control register 0
PMU1_GRF_MEM_CON1	0x0084	W	0x00001410	Memory interface control register 1
PMU1_GRF_FUNC_RST_STATUS	0x0100	W	0x00000000	System function reset status register
PMU1_GRF_FUNC_RST_CLR	0x0104	W	0x00000000	System reset status clear register

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Name	Offset	Size	Reset Value	Description
PMU1_GRF_SD_DETECT_CON	0x0110	W	0x00000000	SDMMC detect control register
PMU1_GRF_SD_DETECT_STS	0x0114	W	0x00000000	SDMMC detect status register
PMU1_GRF_SD_DETECT_CLR	0x0118	W	0x00000000	SDMMC detect clear register
PMU1_GRF_SD_DETECT_CNT	0x011C	W	0x000003E8	SDMMC detect count register
PMU1_GRF_OS_REG0	0x0200	W	0x00000000	Operation system register 0
PMU1_GRF_OS_REG1	0x0204	W	0x00000000	Operation system register 1
PMU1_GRF_OS_REG2	0x0208	W	0x00000000	Operation system register 2
PMU1_GRF_OS_REG3	0x020C	W	0x00000000	Operation system register 3
PMU1_GRF_OS_REG4	0x0210	W	0x00000000	Operation system register 4
PMU1_GRF_OS_REG5	0x0214	W	0x00000000	Operation system register 5
PMU1_GRF_OS_REG6	0x0218	W	0x00000000	Operation system register 6
PMU1_GRF_OS_REG7	0x021C	W	0x00000000	Operation system register 7
PMU1_GRF_OS_REG8	0x0220	W	0x00000000	Operation system register 8
PMU1_GRF_OS_REG9	0x0224	W	0x00000000	Operation system register 9
PMU1_GRF_OS_REG10	0x0228	W	0x00000000	Operation system register 10
PMU1_GRF_OS_REG11	0x022C	W	0x00000000	Operation system register 11
PMU1_GRF_OS_REG12	0x0230	W	0x00000000	Operation system register 12
PMU1_GRF_OS_REG13	0x0234	W	0x00000000	Operation system register 13
PMU1_GRF_OS_REG14	0x0238	W	0x00000000	Operation system register 14
PMU1_GRF_OS_REG15	0x023C	W	0x00000000	Operation system register 15

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.4.2 Detail Registers Description

PMU1_GRF_SOC_CON0

Address: Operational Base(0x26026000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	pmusram_mem_gate_ena PMU_SRAM memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
11	RW	0x0	force_jtag_uart Enable GPIO0d4 and GPIO0d5 switch to JTAG function if uart0_rx_m0_masked_pin low last for a specified period of time defined in uart0rx_low_dly. 1'b0: Disable 1'b1: Enable
10:9	RO	0x0	reserved
8	RW	0x0	sdmmc_det_masked_pin_pol Polarity selection for sdmmc_det_masked_pin. 1'b0: Low active 1'b1: High active

Bit	Attr	Reset Value	Description
7	RW	0x0	pmuwdt_mcu_reset_en Enable PMU_WDT as PMU_MCU reset source. 1'b0: Disable 1'b1: Enable. PMU_MCU is reset when PMU_WDT's reset active.
6	RW	0x0	wakeup_mcu Enable PMU_MCU as PMU wake up source. 1'b0: Disable 1'b1: Enable. When 1, PMU will exit low power mode 1 after PMU enter low power mode 1.
5	RW	0x0	wakeup_timer_sel Select PMU_TIMER interrupt as PMU wake up source. 1'b0: PMU_TIMER channel 0 interrupt selected 1'b1: PMU_TIMER channel 1 interrupt selected
4	RW	0x0	wakeup_pwmir_sel Select PWM_IR interrupt as PMU wake up source. 1'b0: PWM0_2CH channel 0 IR interrupt selected 1'b1: PWM0_2CH channel 1 IR interrupt selected
3	RO	0x0	reserved
2	RW	0x0	pmuwdt_pause PMU_WDT pause enable. It is used to freeze the watchdog counter during pause mode. 1'b0: Disable 1'b1: Enable
1	RW	0x0	uart1_cts_inv Polarity selection for uart1_cts. 1'b0: Low active 1'b1: High active
0	RW	0x0	uart1_rts_inv Polarity selection for uart1_rts. 1'b0: Low active 1'b1: High active

PMU1_GRF_SOC_CON1

Address: Operational Base(0x26026000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	pmumcu_cache_maintain_sram_ena Enable maintain address offset for PMU_MCU cache sram. 1'b0: Disable 1'b1: Enable
2	RW	0x1	pmumcu_cache_maintain_code_ena Enable maintain address offset for PMU_MCU cache code. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pmumcu_cache_mem_gate_ena PMU_MCU cahe memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
0	RO	0x0	reserved

PMU1_GRF_SOC_CON6

Address: Operational Base(0x26026000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reset_width The chip output reset width. Number of xin_osc(24MHz) used by counter logic.

PMU1_GRF_SOC_CON7

Address: Operational Base(0x26026000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	uart0rx_low_dly Count for uart0_rx_m0_masked_pin low time. Number of xin_osc(24MHz) used by counter logic.

PMU1_GRF_BIU_CON

Address: Operational Base(0x26026000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	idle_req_top_sftena Enable sending idle request to BIU_TOP by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_bus_sftena Enable sending idle request to BIU_BUS by software. 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	pmu_pwrstall PwrStall enable for BIU_PMU. 1'b0: Disable 1'b1: Enable

PMU1_GRF_BIU_STATUS

Address: Operational Base(0x26026000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RO	0x0	vdma_nopendingtrans No pending transfer status for VDMA. 1'b0: Inactive 1'b1: Active
9	RO	0x0	pmu_apbs_nopendingtrans No pending transfer status for secure PMU_APB. 1'b0: Inactive 1'b1: Active
8	RO	0x0	pmu_apb_nopendingtrans No pending transfer status for non-secure PMU_APB. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
7	RO	0x0	pmu_ahbs_nopendingtrans No pending transfer status for secure PMU_AHB. 1'b0: Inactive 1'b1: Active
6	RO	0x0	pmu_ahb_nopendingtrans No pending transfer status for non-secure PMU_AHB. 1'b0: Inactive 1'b1: Active
5	RO	0x0	pmu_mcu_nopendingtrans No pending transfer status for PMU_MCU. 1'b0: Inactive 1'b1: Active
4	RO	0x0	pmu_pwractive Power active status for BIU_PMU. 1'b0: Inactive 1'b1: Active
3	RO	0x0	idle_ack_top BIU_TOP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
2	RO	0x0	idle_top BIU_TOP idle state. 1'b0: Not idle 1'b1: Idle
1	RO	0x0	idle_ack_bus BIU_BUS idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
0	RO	0x0	idle_bus BIU_BUS idle state. 1'b0: Not idle 1'b1: Idle

PMU1_GRF_SOC_STATUS

Address: Operational Base(0x26026000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	pmic_int PMIC interrupt status. 1'b0: Inactive 1'b1: Active
12	RO	0x0	pmu1sgrf_crc_chk_rst_req PMU1_SGRF CRC check reset status. It is set to 1 if CRC check for any register in PMU1_SGRF is error. 1'b0: Inactive 1'b1: Active
11	RO	0x0	pmu0sgrf_crc_chk_rst_req PMU0_SGRF CRC check reset status. It is set to 1 if CRC check for any register in PMU0_SGRF is error. 1'b0: Inactive 1'b1: Active
10	RO	0x0	pmu_mcu_deepsleep PMU_MCU deep sleep status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
9	RO	0x0	pmu_mcu_sleeping PMU_MCU sleeping status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	pmu_mcu_lockup PMU_MCU lock up status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	pmu_mcu_halted PMU_MCU halt status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	pmu_mcu_cache_flush_ack PMU_MCU cache flush acknowledge. 1'b0: Not acknowledge 1'b1: Acknowledge
5	RO	0x0	pmu_mcu_txev PMU_MCU TXEV status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	vdma_dig_mic_sts VDMA digital mic status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	pmu_timer1_en_status PMU_TIMER channel 1 enable status. 1'b0: Disable 1'b1: Enable
2	RO	0x0	pmu_timer0_en_status PMU_TIMER channel 0 enable status. 1'b0: Disable 1'b1: Enable
1	RO	0x0	pmu_wdt_sys_rstn PMU_WDT reset request status. 1'b0: Active 1'b1: Inactive
0	RO	0x0	osc_chk_rst_req OSC_CHK reset request status. 1'b0: Inactive 1'b1: Active

PMU1_GRF_MEM_CON0

Address: Operational Base(0x26026000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	pmu1_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_PMU1. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

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PMU1_GRF_MEM_CON1

Address: Operational Base(0x26026000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	pmu1_mem_cfg_hdspra Interface configuration for HDSPRA type memory in PD_PMU1. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

PMU1_GRF_FUNC_RST_STATUS

Address: Operational Base(0x26026000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	tsadc_shut_sts TSADC shut status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	wdt_reset_sts WDT reset status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	first_reset_sts First reset status. 1'b0: Inactive 1'b1: Active

PMU1_GRF_FUNC_RST_CLR

Address: Operational Base(0x26026000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	tsadc_reset_clr Enable clear for TSADC shut status. 1'b0: Disable 1'b1: Enable
1	WO	0x0	wdt_reset_clr Enable clear for WDT reset status. 1'b0: Disable 1'b1: Enable
0	WO	0x0	first_reset_clr Enable clear for first reset status. 1'b0: Disable 1'b1: Enable

PMU1_GRF_SD_DETECT_CON

Address: Operational Base(0x26026000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:2	RO	0x0000	reserved
1	RW	0x0	sd_detect_fall_en Enable SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sd_detect_rise_en Enable SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable

PMU1_GRF_SD_DETECT_STS

Address: Operational Base(0x26026000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	sd_detect_fall_st SDMMC detect pin falling edge status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	sd_detect_rise_st SDMMC detect pin rising edge status. 1'b0: Inactive 1'b1: Active

PMU1_GRF_SD_DETECT_CLR

Address: Operational Base(0x26026000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	WO	0x0	sd_detect_fall_clr Enable clear for SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable
0	WO	0x0	sd_detect_rise_clr Enable clear for SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable

PMU1_GRF_SD_DETECT_CNT

Address: Operational Base(0x26026000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x0003e8	sd_detect_cnt SDMMC detect count. Number of xin_osc(24MHz) used by counter logic.

PMU1_GRF_OS_REG0

Address: Operational Base(0x26026000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG1

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Address: Operational Base(0x26026000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG2

Address: Operational Base(0x26026000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG3

Address: Operational Base(0x26026000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG4

Address: Operational Base(0x26026000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG5

Address: Operational Base(0x26026000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG6

Address: Operational Base(0x26026000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG7

Address: Operational Base(0x26026000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG8

Address: Operational Base(0x26026000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG9

Address: Operational Base(0x26026000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG10

Address: Operational Base(0x26026000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG11

Address: Operational Base(0x26026000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG12

Address: Operational Base(0x26026000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG13

Address: Operational Base(0x26026000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG14

Address: Operational Base(0x26026000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

PMU1_GRF_OS_REG15

Address: Operational Base(0x26026000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Operation system register, with npor reset.

5.5 SYS_GRF Register Description

5.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SYS_GRF_SOC_CON0	0x0000	W	0x00000000	System control register 0
SYS_GRF_SOC_CON1	0x0004	W	0x00000000	System control register 1
SYS_GRF_SOC_CON2	0x0008	W	0x00001000	System control register 2
SYS_GRF_SOC_CON3	0x000C	W	0x00001800	System control register 3
SYS_GRF_SOC_CON4	0x0010	W	0x00000001	System control register 4
SYS_GRF_SOC_CON5	0x0014	W	0x000001D0	System control register 5
SYS_GRF_SOC_CON7	0x001C	W	0x00000001	System control register 7
SYS_GRF_SOC_CON8	0x0020	W	0x00000000	System control register 8
SYS_GRF_SOC_CON9	0x0024	W	0x00000000	System control register 9
SYS_GRF_SOC_CON10	0x0028	W	0x00000000	System control register 10
SYS_GRF_SOC_CON11	0x002C	W	0x00000000	System control register 11
SYS_GRF_SOC_CON12	0x0030	W	0x00000000	System control register 12
SYS_GRF_BIU_CON0	0x0040	W	0x00000000	BIU control register 0
SYS_GRF_BIU_CON1	0x0044	W	0x00000000	BIU control register 1
SYS_GRF_BIU_CON2	0x0048	W	0x00000000	BIU control register 2
SYS_GRF_BIU_CON3	0x004C	W	0x00000000	BIU control register 3

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Name	Offset	Size	Reset Value	Description
SYS_GRF_BIU_CON4	0x0050	W	0x00000000	BIU control register 4
SYS_GRF_BIU_CON5	0x0054	W	0x00000000	BIU control register 5
SYS_GRF_MEM_CON0	0x0080	W	0x00001410	Memory interface configure register 0
SYS_GRF_MEM_CON1	0x0084	W	0x00110010	Memory interface configure register 1
SYS_GRF_MEM_CON2	0x0088	W	0x00008010	Memory interface configure register 2
SYS_GRF_MEM_CON3	0x008C	W	0x00001410	Memory interface configure register 3
SYS_GRF_MEM_CON4	0x0090	W	0x00001410	Memory interface configure register 4
SYS_GRF_MEM_CON5	0x0094	W	0x00001410	Memory interface configure register 5
SYS_GRF_MEM_CON8	0x00A0	W	0x00008010	Memory interface configure register 8
SYS_GRF_MEM_CON9	0x00A4	W	0x00000008	Memory interface configure register 9
SYS_GRF_MEM_CON10	0x00A8	W	0x00000008	Memory interface configure register 10
SYS_GRF_MEM_CON11	0x00AC	W	0x00001410	Memory interface configure register 11
SYS_GRF_MEM_CON12	0x00B0	W	0x00008010	Memory interface configure register 12
SYS_GRF_MEM_CON13	0x00B4	W	0x14101410	Memory interface configure register 13
SYS_GRF_MEM_CON14	0x00B8	W	0x14101410	Memory interface configure register 14
SYS_GRF_MEM_CON15	0x00BC	W	0x00110010	Memory interface configure register 15
SYS_GRF_MEM_CON16	0x00C0	W	0x14101410	Memory interface configure register 16
SYS_GRF_MEM_CON17	0x00C4	W	0x10110010	Memory interface configure register 17
SYS_GRF_MEM_CON18	0x00C8	W	0x00000080	Memory interface configure register 18
SYS_GRF_SOC_STATUS0	0x0140	W	0x00000000	System status register 0
SYS_GRF_SOC_STATUS1	0x0144	W	0x00000000	System status register 1
SYS_GRF_MEMFAULT_STATUS0	0x0148	W	0x00000000	Memory fault status register 0
SYS_GRF_MEMFAULT_STATUS1	0x014C	W	0x00000000	Memory fault status register 1
SYS_GRF_SOC_CODE	0x0180	W	0x4845524F	SOC code register
SYS_GRF_SOC_VERSION	0x0190	W	0x00000000	SOC version register
SYS_GRF_CHIP_ID	0x01A0	W	0x524B3576	Chip id register
SYS_GRF_CHIP_VERSION	0x01B0	W	0x00000000	Chip version register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.5.2 Detail Registers Description

SYS_GRF_SOC_CON0

Address: Operational Base(0x2600A000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	uart8_cts_inv Polarity selection for uart8_cts. 1'b0: Low active 1'b1: High active
14	RW	0x0	uart8_rts_inv Polarity selection for uart8_rts. 1'b0: Low active 1'b1: High active
13	RW	0x0	uart7_cts_inv Polarity selection for uart7_cts. 1'b0: Low active 1'b1: High active
12	RW	0x0	uart7_rts_inv Polarity selection for uart7_rts. 1'b0: Low active 1'b1: High active
11	RW	0x0	uart6_cts_inv Polarity selection for uart6_cts. 1'b0: Low active 1'b1: High active
10	RW	0x0	uart6_rts_inv Polarity selection for uart6_rts. 1'b0: Low active 1'b1: High active
9	RW	0x0	uart5_cts_inv Polarity selection for uart5_cts. 1'b0: Low active 1'b1: High active
8	RW	0x0	uart5_rts_inv Polarity selection for uart5_rts. 1'b0: Low active 1'b1: High active
7	RW	0x0	uart4_cts_inv Polarity selection for uart4_cts. 1'b0: Low active 1'b1: High active
6	RW	0x0	uart4_rts_inv Polarity selection for uart4_rts. 1'b0: Low active 1'b1: High active
5	RW	0x0	uart3_cts_inv Polarity selection for uart3_cts. 1'b0: Low active 1'b1: High active
4	RW	0x0	uart3_rts_inv Polarity selection for uart3_rts. 1'b0: Low active 1'b1: High active
3	RW	0x0	uart2_cts_inv Polarity selection for uart2_cts. 1'b0: Low active 1'b1: High active

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Bit	Attr	Reset Value	Description
2	RW	0x0	uart2_rts_inv Polarity selection for uart2_rts. 1'b0: Low active 1'b1: High active
1	RW	0x0	uart0_cts_inv Polarity selection for uart0_cts. 1'b0: Low active 1'b1: High active
0	RW	0x0	uart0_rts_inv Polarity selection for uart0_rts. 1'b0: Low active 1'b1: High active

SYS_GRF_SOC_CON1

Address: Operational Base(0x2600A000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	i3c1_weakpull I3C1 SDA pull up value configured by software
8	RW	0x0	i3c1_weakpull_sel I3C1 SDA pull up value selection. 1'b0: Controlled by hardware 1'b1: Controlled by software through SYS_GRF_SOC_CON1[9]
7	RW	0x0	i3c0_weakpull I3C0 SDA pull up value configured by software
6	RW	0x0	i3c0_weakpull_sel I3C0 SDA pull up value selection. 1'b0: Controlled by hardware 1'b1: Controlled by software through SYS_GRF_SOC_CON1[7]
5	RW	0x0	uart11_cts_inv Polarity selection for uart11_cts. 1'b0: Low active 1'b1: High active
4	RW	0x0	uart11_rts_inv Polarity selection for uart11_rts. 1'b0: Low active 1'b1: High active
3	RW	0x0	uart10_cts_inv Polarity selection for uart10_cts. 1'b0: Low active 1'b1: High active
2	RW	0x0	uart10_rts_inv Polarity selection for uart10_rts. 1'b0: Low active 1'b1: High active
1	RW	0x0	uart9_cts_inv Polarity selection for uart9_cts. 1'b0: Low active 1'b1: High active

Bit	Attr	Reset Value	Description
0	RW	0x0	uart9_rts_inv Polarity selection for uart9_rts. 1'b0: Low active 1'b1: High active

SYS_GRF_SOC_CON2

Address: Operational Base(0x2600A000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pwm2_ch3_in_phase_a_sel PWM2_CH3 phase A input selection. 1'b0: Select from PWM2_CH3 input 1'b1: Select from UART4_RX input
14	RW	0x0	pwm2_ch2_in_phase_a_sel PWM2_CH2 phase A input selection. 1'b0: Select from PWM2_CH2 input 1'b1: Select from UART3_RX input
13	RW	0x0	pwm2_ch1_in_phase_a_sel PWM2_CH1 phase A input selection. 1'b0: Select from PWM2_CH1 input 1'b1: Select from UART2_RX input
12	RW	0x1	pwm2_ch0_in_phase_a_sel PWM2_CH0 phase A input selection. 1'b0: Select from PWM2_CH0 input 1'b1: Select from UART0_RX input
11:9	RW	0x0	sai4_series_sel SAI4 synchronization selection. 3'h1: SAI4 synchronizes with SAI0 3'h2: SAI4 synchronizes with SAI1 3'h3: SAI4 synchronizes with SAI2 3'h4: SAI4 synchronizes with SAI3 Others: Reserved
8:6	RW	0x0	sai3_series_sel SAI3 synchronization selection. 3'h1: SAI3 synchronizes with SAI0 3'h2: SAI3 synchronizes with SAI1 3'h3: SAI3 synchronizes with SAI2 3'h4: SAI3 synchronizes with SAI4 Others: Reserved
5:4	RW	0x0	sai2_series_sel SAI2 synchronization selection. 2'h1: SAI2 synchronizes with SAI0 2'h2: SAI2 synchronizes with SAI1 2'h3: SAI2 synchronizes with SAI4 Others: Reserved
3:2	RW	0x0	sai1_series_sel SAI1 synchronization selection. 2'h1: SAI1 synchronizes with SAI0 2'h2: SAI1 synchronizes with SAI4 Others: Reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	sai0_series_sel SAI0 synchronization selection. 1'b0: SAI0 doesn't synchronize with SAI4 1'b1: SAI0 synchronizes with SAI4
0	RW	0x0	dsm_sel 1'b0: SAI4 connect to IO 1'b1: SAI4 connect to ACDCDIG_DSM

SYS_GRF_SOC_CON3

Address: Operational Base(0x2600A000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	busmcu_cache_maintain_sram_en Enable maintain address offset for BUS_MCU cache sram. 1'b0: Disable 1'b1: Enable
11	RW	0x1	busmcu_cache_maintain_code_en Enable maintain address offset for BUS_MCU cache code. 1'b0: Disable 1'b1: Enable
10	RW	0x0	busmcu_cache_mem_gate_en BUS_MCU cache memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
9	RW	0x0	busmcu_mem_gate_en BUS_MCU memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
8	RW	0x0	asrc2ch1_mem_gate_en ASRC2CH_1 memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
7	RW	0x0	asrc2ch0_mem_gate_en ASRC2CH_0 memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
6	RW	0x0	asrc4ch1_mem_gate_en ASRC4CH_1 memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
5	RW	0x0	asrc4ch0_mem_gate_en ASRC4CH_0 memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.

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Bit	Attr	Reset Value	Description
4	RW	0x0	can1_mem_gate_en CAN1 memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
3	RW	0x0	can0_mem_gate_en CAN0 memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
2	RW	0x0	crypto_mem_gate_en CRYPTO memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
1	RO	0x0	reserved
0	RW	0x0	decom_mem_gate_en DECOM memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.

SYS_GRF_SOC_CON4

Address: Operational Base(0x2600A000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	ddrwdt_mcu_reset_en Enable DDR_WDT as DDR_MCU reset source. 1'b0: Disable 1'b1: Enable. DDR_MCU is reset when DDR_WDT's reset active.
13	RW	0x0	npuwdt_mcu_reset_en Enable NPU_WDT as NPU_MCU reset source. 1'b0: Disable 1'b1: Enable. NPU_MCU is reset when NPU_WDT's reset active.
12	RW	0x0	buswdt_mcu_reset_en Enable BUS_WDT as BUS_MCU reset source. 1'b0: Disable 1'b1: Enable. BUS_MCU is reset when BUS_WDT's reset active.
11	RW	0x0	buswdt_glb_reset_en BUS_WDT global reset enable. 1'b0: Disable. BUS_WDT reset output cannot reset system. 1'b1: Enable. BUS_WDT reset output can reset system.
10	RW	0x0	npuwdt_glb_reset_en NPU_WDT global reset enable. 1'b0: Disable. NPU_WDT reset output cannot reset system. 1'b1: Enable. NPU_WDT reset output can reset system.
9	RW	0x0	ddrwdt_glb_reset_en DDR_WDT global reset enable. 1'b0: Disable. DDR_WDT reset output cannot reset system. 1'b1: Enable. DDR_WDT reset output can reset system.

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Bit	Attr	Reset Value	Description
8	RW	0x0	wdtns_glb_reset_en WDT_NS global reset enable. 1'b0: Disable. WDT_NS reset output cannot reset system. 1'b1: Enable. WDT_NS reset output can reset system.
7	RW	0x0	pmuwdt_glb_reset_en PMU_WDT global reset enable. 1'b0: Disable. PMU_WDT reset output cannot reset system. 1'b1: Enable. PMU_WDT reset output can reset system.
6	RW	0x0	wdtns_pause_en WDT_NS pause enable. It is used to freeze the watchdog counter during pause mode. 1'b0: Disable 1'b1: Enable
5	RW	0x0	buswdt_pause_en BUS_WDT pause enable. It is used to freeze the watchdog counter during pause mode. 1'b0: Disable 1'b1: Enable
4:0	RO	0x0	reserved

SYS_GRF_SOC_CON5

Address: Operational Base(0x2600A000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8:6	RW	0x7	vicap_access_id 3'h0: VICAP access DDR through port 0 3'h7: VICAP access DDR through port 1 Others: Reserved
5	RO	0x0	reserved
4	RW	0x1	isp_access_arid 1'b0: ISP read access DDR through port 0 1'b1: ISP read access DDR through port 3
3	RO	0x0	reserved
2	RW	0x0	csiphy1_lane_sel 1'b0: CSIDPHY1 works in full mode. 4 lanes are connected to CSIHOST3. 1'b1: CSIDPHY1 works in split mode. Lane 0~1 are connected to CSIHOST3 and Lane 2~3 are connected to CSIHOST4.
1	RW	0x0	csiphy0_lane_sel 1'b0: CSIDPHY0 works in full mode. 4 lanes are connected to CSIHOST1. 1'b1: CSIDPHY0 works in split mode. Lane 0~1 are connected to CSIHOST1 and Lane 2~3 are connected to CSIHOST2.
0	RO	0x0	reserved

SYS_GRF_SOC_CON7

Address: Operational Base(0x2600A000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	npu_debug_sel PD_NPU debug selection. 1'b0: NPU_MCU's jtag interface is connected to PD_NPU debug io 1'b1: RKNN's jtag interface is connected to PD_NPU debug io
4	RW	0x0	jtag_busmcu_sel Select JTAG IO group for BUS_MCU debug. 1'b0: Not select 1'b1: Select
3	RW	0x0	jtag_pmumcu_sel Select JTAG IO group for PMU_MCU debug. 1'b0: Not select 1'b1: Select
2	RW	0x0	jtag_npu_sel Select JTAG IO group for PD_NPU debug. 1'b0: Not select 1'b1: Select
1	RW	0x0	jtag_ddrmcu_sel Select JTAG IO group for DDR_MCU debug. 1'b0: Not select 1'b1: Select
0	RW	0x1	jtag_cpu_sel Select JTAG IO group for CPU debug. 1'b0: Not select 1'b1: Select

SYS_GRF_SOC_CON8

Address: Operational Base(0x2600A000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RO	0x00	mbisr_state MBISR controller state. 5'h0: INIT 5'h1: INIT_BISR 5'h2: READ_0_COUNT 5'h3: READ_OPCODE 5'h4: READ_FUSE 5'h5: SHIFT_BISR_0 5'h6: DONE_SUCCESS 5'h7: DONE_FAILURE 5'h8: SHIFT_BISR_OP_1 5'h9: SHIFT_0_COUNT 5'ha: PROG_OP_1 5'hb: PROG_OP_0 5'hc: COUNT_0 5'hd: FIND_GROUP 5'he: FOUND_GROUP 5'hf: READ_GROUP_PTR 5'h10: ROTATE_GROUP_PTR 5'h11: PROG_GROUP_PTR 5'h12: CAPTURE_BIRA 5'h13: ROTATE_BISR 5'h14: SHIFT_BISR 5'h1e: INIT_FB_READ_BUFFER Others: Reserved

SYS_GRF_SOC_CON9

Address: Operational Base(0x2600A000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	asrc4ch1_src_sel ASRC4CH_1 source LRCK selection. 5'h0: From SAI0 5'h1: From SAI1 5'h2: From SAI2 5'h3: From SAI3 5'h4: From SAI4 5'h5: From SAI5 5'h6: From SAI6 5'h7: From SAI7 5'h8: From SAI8 5'h9: From SAI9 5'ha: From PDM0 5'hb: From PDM1 5'hc: From SPDIF_RX0 5'hd: From SPDIF_RX1 5'he: From SPDIF_RX2 5'hf: lclk_asrc_src_0 from CRU 5'h10: lclk_asrc_src_1 from CRU Others: Reserved

Bit	Attr	Reset Value	Description
9:5	RW	0x00	asrc4ch0_dst_sel ASRC4CH_0 destination LRCK selection. 5'h0: From SAI0 5'h1: From SAI1 5'h2: From SAI2 5'h3: From SAI3 5'h4: From SAI4 5'h5: From SAI5 5'h6: From SAI6 5'h7: From SAI7 5'h8: From SAI8 5'h9: From SAI9 5'ha: From SPDIF_TX0 5'hb: From SPDIF_TX1 5'hc: From SPDIF_TX2 5'hd: From SPDIF_TX3 5'he: From SPDIF_TX4 5'hf: From SPDIF_TX5 5'h10: lclk_asrc_src_0 from CRU 5'h11: lclk_asrc_src_1 from CRU Others: Reserved
4:0	RW	0x00	asrc4ch0_src_sel ASRC4CH_0 source LRCK selection. 5'h0: From SAI0 5'h1: From SAI1 5'h2: From SAI2 5'h3: From SAI3 5'h4: From SAI4 5'h5: From SAI5 5'h6: From SAI6 5'h7: From SAI7 5'h8: From SAI8 5'h9: From SAI9 5'ha: From PDM0 5'hb: From PDM1 5'hc: From SPDIF_RX0 5'hd: From SPDIF_RX1 5'he: From SPDIF_RX2 5'hf: lclk_asrc_src_0 from CRU 5'h10: lclk_asrc_src_1 from CRU Others: Reserved

SYS_GRF_SOC_CON10

Address: Operational Base(0x2600A000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:10	RW	0x00	asrc2ch0_dst_sel ASRC2CH_0 destination LRCK selection. 5'h0: From SAI0 5'h1: From SAI1 5'h2: From SAI2 5'h3: From SAI3 5'h4: From SAI4 5'h5: From SAI5 5'h6: From SAI6 5'h7: From SAI7 5'h8: From SAI8 5'h9: From SAI9 5'ha: From SPDIF_TX0 5'hb: From SPDIF_TX1 5'hc: From SPDIF_TX2 5'hd: From SPDIF_TX3 5'he: From SPDIF_TX4 5'hf: From SPDIF_TX5 5'h10: lclk_asrc_src_0 from CRU 5'h11: lclk_asrc_src_1 from CRU Others: Reserved
9:5	RW	0x00	asrc2ch0_src_sel ASRC2CH_0 source LRCK selection. 5'h0: From SAI0 5'h1: From SAI1 5'h2: From SAI2 5'h3: From SAI3 5'h4: From SAI4 5'h5: From SAI5 5'h6: From SAI6 5'h7: From SAI7 5'h8: From SAI8 5'h9: From SAI9 5'ha: From PDM0 5'hb: From PDM1 5'hc: From SPDIF_RX0 5'hd: From SPDIF_RX1 5'he: From SPDIF_RX2 5'hf: lclk_asrc_src_0 from CRU 5'h10: lclk_asrc_src_1 from CRU Others: Reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	asrc4ch1_dst_sel ASRC4CH_1 destination LRCK selection. 5'h0: From SAI0 5'h1: From SAI1 5'h2: From SAI2 5'h3: From SAI3 5'h4: From SAI4 5'h5: From SAI5 5'h6: From SAI6 5'h7: From SAI7 5'h8: From SAI8 5'h9: From SAI9 5'ha: From SPDIF_TX0 5'hb: From SPDIF_TX1 5'hc: From SPDIF_TX2 5'hd: From SPDIF_TX3 5'he: From SPDIF_TX4 5'hf: From SPDIF_TX5 5'h10: lclk_asrc_src_0 from CRU 5'h11: lclk_asrc_src_1 from CRU Others: Reserved

SYS_GRF_SOC_CON11

Address: Operational Base(0x2600A000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb0_slv_timeout_ena USB0 slave response timeout enable. 1'b0: Disable 1'b1: Enable
14:10	RO	0x00	reserved
9:5	RW	0x00	asrc2ch1_dst_sel ASRC2CH_1 destination LRCK selection. 5'h0: From SAI0 5'h1: From SAI1 5'h2: From SAI2 5'h3: From SAI3 5'h4: From SAI4 5'h5: From SAI5 5'h6: From SAI6 5'h7: From SAI7 5'h8: From SAI8 5'h9: From SAI9 5'ha: From SPDIF_TX0 5'hb: From SPDIF_TX1 5'hc: From SPDIF_TX2 5'hd: From SPDIF_TX3 5'he: From SPDIF_TX4 5'hf: From SPDIF_TX5 5'h10: lclk_asrc_src_0 from CRU 5'h11: lclk_asrc_src_1 from CRU Others: Reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	asrc2ch1_src_sel ASRC2CH_1 source LRCK selection. 5'h0: From SAI0 5'h1: From SAI1 5'h2: From SAI2 5'h3: From SAI3 5'h4: From SAI4 5'h5: From SAI5 5'h6: From SAI6 5'h7: From SAI7 5'h8: From SAI8 5'h9: From SAI9 5'ha: From PDM0 5'hb: From PDM1 5'hc: From SPDIF_RX0 5'hd: From SPDIF_RX1 5'he: From SPDIF_RX2 5'hf: lclk_asrc_src_0 from CRU 5'h10: lclk_asrc_src_1 from CRU Others: Reserved

SYS_GRF_SOC_CON12

Address: Operational Base(0x2600A000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bus_apb_slv_timeout_ena PD_BUS apb slave response timeout enable. 1'b0: Disable 1'b1: Enable
14	RW	0x0	bus_ahb_slv_timeout_ena PD_BUS ahb slave response timeout enable. 1'b0: Disable 1'b1: Enable
13	RW	0x0	vo0_apb_slv_timeout_ena PD_VO0 apb slave response timeout enable. 1'b0: Disable 1'b1: Enable
12	RW	0x0	ufs_apb_slv_timeout_ena UFSHC apb slave response timeout enable. 1'b0: Disable 1'b1: Enable
11	RW	0x0	ufs_axi_slv_timeout_ena UFSHC axi slave response timeout enable. 1'b0: Disable 1'b1: Enable
10	RW	0x0	gmac_ahb_slv_timeout_ena PD_GMAC ahb slave response timeout enable. 1'b0: Disable 1'b1: Enable
9	RW	0x0	gmac_apb_slv_timeout_ena PD_GMAC apb slave response timeout enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	dsmc_slv_timeout_ena DSMC slave response timeout enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	usb1_slv_timeout_ena USB1 slave response timeout enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	sata1_slv_timeout_ena SATA1 slave response timeout enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	sata0_slv_timeout_ena SATA0 slave response timeout enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pcie1_slv_timeout_ena PCIE1 slave response timeout enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pcie1_dbi_timeout_ena PCIE1 DBI response timeout enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pcie0_slv_timeout_ena PCIE0 slave response timeout enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pcie0_dbi_timeout_ena PCIE0 DBI response timeout enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	nvm_slv_timeout_ena PD_NVM slave response timeout enable. 1'b0: Disable 1'b1: Enable

SYS_GRF_BIU_CON0

Address: Operational Base(0x2600A000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	biu_pwrstall_con Each bit controls the behavior of corresponding path if the target power domain is in idle status. 1'b0: Access to the idle power domain will be response error. 1'b1: Access to the idle power domain will be stalled. bit[0]: From BIU_CCI to BIU_DDRSCH0 port4 bit[1]: From BIU_CCI to BIU_DDRSCH1 port4 bit[2]: From BIU_CENTER to BIU_DDRSCH0 port0 bit[3]: From BIU_CENTER to BIU_DDRSCH0 port1 bit[4]: From BIU_CENTER to BIU_DDRSCH0 port2 bit[5]: From BIU_CENTER to BIU_DDRSCH0 port3 bit[6]: From BIU_CENTER to BIU_DDRSCH1 port0 bit[7]: From BIU_CENTER to BIU_DDRSCH1 port1 bit[8]: From BIU_CENTER to BIU_DDRSCH1 port2 bit[9]: From BIU_CENTER to BIU_DDRSCH1 port3 bit[10]: From BIU_CENTER to BIU_CCI bit[11]: From BIU_VOP to BIU_DDRSCH0 port0 bit[12]: From BIU_VOP to BIU_DDRSCH0 port1 bit[13]: From BIU_VOP to BIU_DDRSCH1 port0 bit[14]: From BIU_VOP to BIU_DDRSCH1 port1 bit[15]: From BIU_BUS to BIU_TOP

SYS_GRF_BIU_CON1

Address: Operational Base(0x2600A000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	biu_pwrstall_con Each bit controls the behavior of corresponding path if the target power domain is in idle status. 1'b0: Access to the idle power domain will be response Error. 1'b1: Access to the idle power domain will be stalled. bit0: From BIU_CCI to BIU_CENTER bit1: From BIU_CCI to BIU_BIGCORE bit2: From BIU_CCI to BIU_LITCORE bit3: From BIU_CENTER to BIU_GPU bit4: From BIU_CENTER to BIU_TOP bit5: From BIU_CENTER to BIU_CCI bit6: From BIU_CENTER to BIU_DDR config bus bit7: From BIU_CENTER to BIU_VDEC bit8: From BIU_CENTER to BIU_CCI service bus bit9: From BIU_CENTER to DDR port0 bus0 bit10: From BIU_CENTER to DDR port0 bus1 bit11: From BIU_CENTER to DDR port2 bus0 bit12: From BIU_CENTER to DDR port2 bus1 bit13: From BIU_CENTER to DDR port3 bus0 bit14: From BIU_CENTER to DDR port3 bus1 bit15: From BIU_CENTER to BIU_VOP

SYS_GRF_BIU_CON2

Address: Operational Base(0x2600A000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	biu_pwrstall_con Each bit controls the behavior of corresponding path if the target power domain is in idle status. 1'b0: Access to the idle power domain will be response error. 1'b1: Access to the idle power domain will be stalled. bit0: From BIU_DDR to BIU_CENTER bit1: From BIU_GMAC to BIU_NVM bit2: From BIU_GPU to BIU_CENTER bit3: From BIU_NPU to BIU_TOP bus0 bit4: From BIU_NPU to BIU_TOP bus1 bit5: Not used bit6: Not used bit7: Not used bit8: Not used bit9: From BIU_NVM to BIU_SECURE bit10: From BIU_NVM to BIU_GMAC bit11: From BIU_PHP to BIU_TOP bus0 bit12: From BIU_PHP to BIU_TOP bus1 bit13: From BIU_SECURE to BIU_TOP bus0 bit14: From BIU_SECURE to BIU_TOP bus1 bit15: From BIU_SECURE to BIU_NVM

SYS_GRF_BIU_CON3

Address: Operational Base(0x2600A000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	biu_pwrstall_con Each bit controls the behavior of corresponding path if the target power domain is in idle status. 1'b0: Access to the idle power domain will be response error. 1'b1: Access to the idle power domain will be stalled. bit0: From BIU_SECURE to BIU_VPU bit1: From BIU_TOP to BIU_CENTER bit2: From BIU_TOP to BIU_BUS bit3: From BIU_TOP to BIU_NPU bit4: From BIU_TOP to BIU_CENTER port0 bus0 bit5: From BIU_TOP to BIU_CENTER port1 bus0 bit6: From BIU_TOP to BIU_CENTER port2 bus0 bit7: From BIU_TOP to BIU_CENTER port2 bus1 bit8: From BIU_TOP to BIU_CENTER port3 bus0 bit9: From BIU_TOP to BIU_CENTER port3 bus1 bit10: From BIU_TOP to BIU_PHP bit11: From BIU_TOP to BIU_AUDIO bit12: From BIU_TOP to BIU_PMU1 bit13: From BIU_TOP to BIU_SECURE bit14: From BIU_TOP to BIU_VI bit15: From BIU_TOP to BIU_VOP

SYS_GRF_BIU_CON4

Address: Operational Base(0x2600A000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	biu_pwrstall_con Each bit controls the behavior of corresponding path if the target power domain is in idle status. 1'b0: Access to the idle power domain will be response error. 1'b1: Access to the idle power domain will be stalled. bit0: From BIU_VDEC to BIU_CENTER bit1: From BIU_VENC to BIU_VI bit2: From BIU_VI to BIU_TOP bus0 bit3: From BIU_VI to BIU_TOP bus1 bit4: From BIU_VI to BIU_TOP bus2 bit5: From BIU_VI to BIU_TOP bus3 bit6: From BIU_VI to BIU_TOP bus4 bit7: From BIU_VI to BIU_TOP bus5 bit8: From BIU_VI to BIU_VENC bit9: From BIU_VO0 to BIU_VO0VOP_CHANNEL bus0 bit10: From BIU_VO0VOP_CHANNEL to BIU_VOP bus0 bit11: From BIU_VO0VOP_CHANNEL to BIU_VOP bus1 bit12: From BIU_VO1 to BIU_VOP bit13: From BIU_VOP to BIU_DDR bit14: From BIU_VOP to BIU_VO0VOPCHN bit15: From BIU_VOP to BIU_USB

SYS_GRF_BIU_CON5

Address: Operational Base(0x2600A000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	biu_pwrstall_con Each bit controls the behavior of corresponding path if the target power domain is in idle status. 1'b0: Access to the idle power domain will be response error. 1'b1: Access to the idle power domain will be stalled. bit0: From BIU_VOP to BIU_VO1 bit1: From BIU_VOP to DDR port0 bus1 bit2: From BIU_VOP to DDR port1 bus1 bit3: From BIU_VPU to BIU_SECURE bus0 bit4: From BIU_VPU to BIU_SECURE bus1 bit5: From BIU_CENTER to BIU_CCI bit6: Not used bit7: Not used bit8: Not used bit9: From BIU_VEPU1 to BIU_TOP bit10: From BIU_TOP to BIU_VEPU1 bit11: From BIU_SECURE to BIU_TOP bit12: Not used bit13: Not used bit14: Not used bit15: Not used

SYS_GRF_MEM_CON0

Address: Operational Base(0x2600A000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	bus_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_BUS. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SYS_GRF_MEM_CON1

Address: Operational Base(0x2600A000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x110010	bus_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_BUS. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

SYS_GRF_MEM_CON2

Address: Operational Base(0x2600A000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x08010	bus_mem_cfg_uhdpdprf Interface configuration for UHDPDPPRF type memory in PD_BUS. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

SYS_GRF_MEM_CON3

Address: Operational Base(0x2600A000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x1410	audio_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_AUDIO. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SYS_GRF_MEM_CON4

Address: Operational Base(0x2600A000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	nvm_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_NVM. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SYS_GRF_MEM_CON5

Address: Operational Base(0x2600A000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	secure_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_SECURE. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SYS_GRF_MEM_CON8

Address: Operational Base(0x2600A000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x08010	secure_mem_cfg_uhdpdprf Interface configuration for UHDPDPPRF type memory in PD_SECURE. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

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SYS_GRF_MEM_CON9

Address: Operational Base(0x2600A000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x08	secure_mem_cfg_rom Interface configuration for ROM type memory in PD_SECURE. Bit[0]: TEST1 Bit[4:1]: RM Bit[5]: LS Other bits: Reserved

SYS_GRF_MEM_CON10

Address: Operational Base(0x2600A000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x08	audio_mem_cfg_lpprom Interface configuration for ROM type memory in PD_AUDIO. Bit[0]: TEST1 Bit[4:1]: RM Bit[5]: LS Other bits: Reserved

SYS_GRF_MEM_CON11

Address: Operational Base(0x2600A000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	vdec_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_VDEC. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SYS_GRF_MEM_CON12

Address: Operational Base(0x2600A000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x08010	vpu_mem_cfg_uhdpdprf Interface configuration for UHDPDPPRF type memory in PD_VPU. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

SYS_GRF_MEM_CON13

Address: Operational Base(0x2600A000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1410	venc_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_VEPU0 and PD_VEPU1. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved
15:0	RW	0x1410	venc_mem_cfg_hdspra Interface configuration for HDSPRA type memory in PD_VEPU0 and PD_VEPU1. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SYS_GRF_MEM_CON14

Address: Operational Base(0x2600A000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x1410	vi_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_VI. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved
15:0	RW	0x1410	vi_mem_cfg_hdspra Interface configuration for HDSPRA type memory in PD_VI. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SYS_GRF_MEM_CON15

Address: Operational Base(0x2600A000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x110010	vi_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_VI. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

SYS_GRF_MEM_CON16

Address: Operational Base(0x2600A000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x1410	vpu_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_VPU. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved
15:0	RW	0x1410	vpu_mem_cfg_hdspra Interface configuration for HDSPRA type memory in PD_VPU. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SYS_GRF_MEM_CON17

Address: Operational Base(0x2600A000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	vdec_mem_cfg_uhdpdprf_l Interface configuration for UHDPDPPRF type memory in PD_VDEC, lower 8 bits. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

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Bit	Attr	Reset Value	Description
23:0	RW	0x110010	vdec_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_VDEC. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

SYS_GRF_MEM_CON18

Address: Operational Base(0x2600A000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x080	vdec_mem_cfg_uhdpdprf_h Interface configuration for UHDPDPPRF type memory in PD_VDEC, higher 10 bits. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

SYS_GRF_SOC_STATUS0

Address: Operational Base(0x2600A000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	ddr_mcu_deepsleep DDR_MCU deep sleep status. 1'b0: Inactive 1'b1: Active
24	RO	0x0	ddr_mcu_sleeping DDR_MCU sleeping status. 1'b0: Inactive 1'b1: Active
23	RO	0x0	ddr_mcu_lockup DDR_MCU lock up status. 1'b0: Inactive 1'b1: Active
22	RO	0x0	ddr_mcu_halted DDR_MCU halt status. 1'b0: Inactive 1'b1: Active
21	RO	0x0	ddr_mcu_txev DDR_MCU TXEV status. 1'b0: Inactive 1'b1: Active
20	RO	0x0	crc_chk_rst_req_sgrf CRC check reset status. It is set to 1 if CRC check for any register in secure GRF is error. 1'b0: Inactive 1'b1: Active

Bit	Attr	Reset Value	Description
19	RO	0x0	cpu7_standbywfe CPU7 STANDBYWFE state. 1'b0: Normal 1'b1: STANDBYWFE
18	RO	0x0	cpu6_standbywfe CPU6 STANDBYWFE state. 1'b0: Normal 1'b1: STANDBYWFE
17	RO	0x0	cpu5_standbywfe CPU5 STANDBYWFE state. 1'b0: Normal 1'b1: STANDBYWFE
16	RO	0x0	cpu4_standbywfe CPU4 STANDBYWFE state. 1'b0: Normal 1'b1: STANDBYWFE
15	RO	0x0	cpu3_standbywfe CPU3 STANDBYWFE state. 1'b0: Normal 1'b1: STANDBYWFE
14	RO	0x0	cpu2_standbywfe CPU2 STANDBYWFE state. 1'b0: Normal 1'b1: STANDBYWFE
13	RO	0x0	cpu1_standbywfe CPU1 STANDBYWFE state. 1'b0: Normal 1'b1: STANDBYWFE
12	RO	0x0	cpu0_standbywfe CPU0 STANDBYWFE state. 1'b0: Normal 1'b1: STANDBYWFE
11	RO	0x0	timer11_en_status TIMER_NS1 channel 5 enable status. 1'b0: Inactive 1'b1: Active
10	RO	0x0	timer10_en_status TIMER_NS1 channel 4 enable status. 1'b0: Inactive 1'b1: Active
9	RO	0x0	timer9_en_status TIMER_NS1 channel 3 enable status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	timer8_en_status TIMER_NS1 channel 2 enable status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	timer7_en_status TIMER_NS1 channel 1 enable status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	timer6_en_status TIMER_NS1 channel 0 enable status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
5	RO	0x0	timer5_en_status TIMER_NS0 channel 5 enable status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	timer4_en_status TIMER_NS0 channel 4 enable status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	timer3_en_status TIMER_NS0 channel 3 enable status. 1'b0: Inactive 1'b1: Active
2	RO	0x0	timer2_en_status TIMER_NS0 channel 2 enable status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	timer1_en_status TIMER_NS0 channel 1 enable status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	timer0_en_status TIMER_NS0 channel 0 enable status. 1'b0: Inactive 1'b1: Active

SYS_GRF_SOC_STATUS1

Address: Operational Base(0x2600A000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	bus_apb_slv_timeout PD_BUS apb slave response timeout indication. 1'b0: Normal 1'b1: Timeout
23	RO	0x0	bus_ahb_slv_timeout PD_BUS ahb slave response timeout indication. 1'b0: Normal 1'b1: Timeout
22	RO	0x0	vo0_apb_slv_timeout PD_VO0 apb slave response timeout indication. 1'b0: Normal 1'b1: Timeout
21	RO	0x0	ufs_apb_slv_timeout UFSHC apb slave response timeout indication. 1'b0: Normal 1'b1: Timeout
20	RO	0x0	ufs_axi_slv_timeout UFSHC axi slave response timeout indication. 1'b0: Normal 1'b1: Timeout
19	RO	0x0	gmac_apb_slv_timeout PD_GMAC apb slave response timeout indication. 1'b0: Normal 1'b1: Timeout

Bit	Attr	Reset Value	Description
18	RO	0x0	gmac_ahb_slv_timeout PD_GMAC ahb slave response timeout indication. 1'b0: Normal 1'b1: Timeout
17	RO	0x0	dsmc_slv_timeout DSMC slave response timeout indication. 1'b0: Normal 1'b1: Timeout
16	RO	0x0	usb1_slv_timeout USB1 slave response timeout indication. 1'b0: Normal 1'b1: Timeout
15	RO	0x0	usb0_slv_timeout USB0 slave response timeout indication. 1'b0: Normal 1'b1: Timeout
14	RO	0x0	sata1_slv_timeout SATA1 slave response timeout indication. 1'b0: Normal 1'b1: Timeout
13	RO	0x0	sata0_slv_timeout SATA0 slave response timeout indication. 1'b0: Normal 1'b1: Timeout
12	RO	0x0	pcie1_slv_timeout PCIE1 slave response timeout indication. 1'b0: Normal 1'b1: Timeout
11	RO	0x0	pcie1_dbi_timeout PCIE1 DBI response timeout indication. 1'b0: Normal 1'b1: Timeout
10	RO	0x0	pcie0_slv_timeout PCIE0 slave response timeout indication. 1'b0: Normal 1'b1: Timeout
9	RO	0x0	pcie0_dbi_timeout PCIE0 DBI response timeout indication. 1'b0: Normal 1'b1: Timeout
8	RO	0x0	nvm_slv_timeout PD_NVM slave response timeout indication. 1'b0: Normal 1'b1: Timeout
7:0	RO	0x00	reserved

SYS_GRF_MEMFAULT_STATUS0

Address: Operational Base(0x2600A000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31	RO	0x0	pd_litcore_mem_fault Memory fault status for PD_LITCORE. 1'b0: Memory has no fault 1'b1: Memory has fault

Bit	Attr	Reset Value	Description
30	RO	0x0	pd_cpu4_mem_fault Memory fault status for PD_CPU4. 1'b0: Memory has no fault 1'b1: Memory has fault
29	RO	0x0	pd_cpu5_mem_fault Memory fault status for PD_CPU5. 1'b0: Memory has no fault 1'b1: Memory has fault
28	RO	0x0	pd_cpu6_mem_fault Memory fault status for PD_CPU6. 1'b0: Memory has no fault 1'b1: Memory has fault
27	RO	0x0	pd_cpu7_mem_fault Memory fault status for PD_CPU7. 1'b0: Memory has no fault 1'b1: Memory has fault
26	RO	0x0	pd_bigcore_mem_fault Memory fault status for PD_BIGCORE. 1'b0: Memory has no fault 1'b1: Memory has fault
25	RO	0x0	pd_gpu_mem_fault Memory fault status for VD_GPU. 1'b0: Memory has no fault 1'b1: Memory has fault
24	RO	0x0	pd_npu1_mem_fault Memory fault status for PD_NPU1. 1'b0: Memory has no fault 1'b1: Memory has fault
23	RO	0x0	pd_npu0_mem_fault Memory fault status for PD_NPU0. 1'b0: Memory has no fault 1'b1: Memory has fault
22	RO	0x0	pd_nputop_mem_fault Memory fault status for PD_NPUTOP. 1'b0: Memory has no fault 1'b1: Memory has fault
21	RO	0x0	pd_vpu_mem_fault Memory fault status for PD_VPU. 1'b0: Memory has no fault 1'b1: Memory has fault
20	RO	0x0	pd_vdec_mem_fault Memory fault status for PD_VDEC. 1'b0: Memory has no fault 1'b1: Memory has fault
19	RO	0x0	pd_vepu1_mem_fault Memory fault status for PD_VEPU1. 1'b0: Memory has no fault 1'b1: Memory has fault
18	RO	0x0	pd_vepu0_mem_fault Memory fault status for PD_VEPU0. 1'b0: Memory has no fault 1'b1: Memory has fault
17	RO	0x0	pd_vi_mem_fault Memory fault status for PD_VI. 1'b0: Memory has no fault 1'b1: Memory has fault

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Bit	Attr	Reset Value	Description
16	RO	0x0	pd_usb_mem_fault Memory fault status for PD_USB. 1'b0: Memory has no fault 1'b1: Memory has fault
15	RO	0x0	pd_vo0_mem_fault Memory fault status for PD_VO0. 1'b0: Memory has no fault 1'b1: Memory has fault
14	RO	0x0	pd_vo1_mem_fault Memory fault status for PD_VO1. 1'b0: Memory has no fault 1'b1: Memory has fault
13	RO	0x0	pd_vop_cluster_mem_fault Memory fault status for PD_VOP_CLUSTER. 1'b0: Memory has no fault 1'b1: Memory has fault
12	RO	0x0	pd_vop_esmart_mem_fault Memory fault status for PD_VOP_ESMART. 1'b0: Memory has no fault 1'b1: Memory has fault
11	RO	0x0	pd_vop_mem_fault Memory fault status for PD_VOP. 1'b0: Memory has no fault 1'b1: Memory has fault
10	RO	0x0	pd_subphp_mem_fault Memory fault status for PD_SUBPHP. 1'b0: Memory has no fault 1'b1: Memory has fault
9	RO	0x0	pd_php_mem_fault Memory fault status for PD_PHP. 1'b0: Memory has no fault 1'b1: Memory has fault
8	RO	0x0	pd_audio_mem_fault Memory fault status for PD_AUDIO. 1'b0: Memory has no fault 1'b1: Memory has fault
7	RO	0x0	pd_sdgmac_mem_fault Memory fault status for PD_SDGMAC. 1'b0: Memory has no fault 1'b1: Memory has fault
6	RO	0x0	pd_nvm_mem_fault Memory fault status for PD_NVM. 1'b0: Memory has no fault 1'b1: Memory has fault
5	RO	0x0	pd_cci_mem_fault Memory fault status for PD_CCI. 1'b0: Memory has no fault 1'b1: Memory has fault
4	RO	0x0	pd_ddr_mem_fault Memory fault status for VD_DDR. 1'b0: Memory has no fault 1'b1: Memory has fault
3	RO	0x0	pd_center_mem_fault Memory fault status for PD_CENTER. 1'b0: Memory has no fault 1'b1: Memory has fault

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Bit	Attr	Reset Value	Description
2	RO	0x0	pd_secure_mem_fault Memory fault status for PD_SECURE. 1'b0: Memory has no fault 1'b1: Memory has fault
1	RO	0x0	pd_bus_mem_fault Memory fault status for PD_BUS. 1'b0: Memory has no fault 1'b1: Memory has fault
0	RO	0x0	pd_pmu1_mem_fault Memory fault status for PD_PMU1. 1'b0: Memory has no fault 1'b1: Memory has fault

SYS_GRF_MEMFAULT_STATUS1

Address: Operational Base(0x2600A000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	pd_cpu0_mem_fault Memory fault status for PD_CPU0. 1'b0: Memory has no fault 1'b1: Memory has fault
2	RO	0x0	pd_cpu1_mem_fault Memory fault status for PD_CPU1. 1'b0: Memory has no fault 1'b1: Memory has fault
1	RO	0x0	pd_cpu2_mem_fault Memory fault status for PD_CPU2. 1'b0: Memory has no fault 1'b1: Memory has fault
0	RO	0x0	pd_cpu3_mem_fault Memory fault status for PD_CPU3. 1'b0: Memory has no fault 1'b1: Memory has fault

SYS_GRF_SOC_CODE

Address: Operational Base(0x2600A000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RO	0x4845524f	soc_code SOC code

SYS_GRF_SOC_VERSION

Address: Operational Base(0x2600A000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	soc_version SOC version

SYS_GRF_CHIP_ID

Address: Operational Base(0x2600A000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x524b3576	chip_id Chip ID

SYS_GRF_CHIP_VERSION

Address: Operational Base(0x2600A000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chip_version Chip version

5.6 LITCORE_GRF Register Description

5.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
LITCORE_GRF_CPU_STATUS0	0x002C	W	0x00003C20	CPU status register
LITCORE_GRF_CPU_CON0	0x0034	W	0x000000B4	CPU control register 0
LITCORE_GRF_CPU_CON1	0x0038	W	0x00000000	CPU control register 1
LITCORE_GRF_CPU_MEM_CFG_HDSPRF	0x003C	W	0x00001410	CPU HDSPRF memory configuration register
LITCORE_GRF_CPU_MEM_CFG_HSSPRF	0x0044	W	0x00000010	CPU HSSPRF memory configuration register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.6.2 Detail Registers Description

LITCORE_GRF_CPU_STATUS0

Address: Operational Base(0x2600E000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:10	RW	0xf	standbywfi Indicates whether a processer is in WFI low-power state,high active. The bit[0] is for A53_0, and so on.
9:6	RO	0x0	standbywfe Indicates whether a processer is in WFE low-power state,high active. The bit[0] is for A53_0, and so on.
5	RO	0x1	standbywfil2 Indicates whether the L2 is in WFI low-power state,high active.
4	RO	0x0	clrexmonack Clearing of the external global exclusive monitor acknowledge.
3:0	RO	0x0	smpen CPUECTLR.SMPEN output. This signal indicates: 1'b0: The CPUECTLR.SMPEN bit is not set. 1'b1: The CPUECTLR.SMPEN bit is set. The bit[0] is for A53_0, and so on.

LITCORE_GRF_CPU_CON0

Address: Operational Base(0x2600E000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:12	RW	0x0	cfgte Individual core control of the default exception handling state. It sets the initial value of the TE bit in the CP15 System Control Register (SCTLR when the highest Exception level is AArch32): 1'b0: TE bit is 0. 1'b1: TE bit is 1. This signal is only sampled during powerup reset of the processor.

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	cfgend Individual core control of the endianness configuration at reset. It sets the initial value of the EE bit in the System Control Register (SCTLR or SCTLR_EL3): 1'b0: EE bit is 0. 1'b1: EE bit is 1. This signal is only sampled during powerup reset of the processor.
7	RW	0x1	abd400s_ace_pwrq_permit_deny This signal determines whether the ADB-400 can enter the Q_DENIED state instead of the Q_STOPPED state. This signal is sampled as the slave interface half of the bridge exits reset.
6	RW	0x0	broadcastcachemaint Enable broadcasting of cache maintenance operations to downstream caches: 1'b0: Cache maintenance operations are not broadcasted to downstream caches. 1'b1: Cache maintenance operations are broadcasted to downstream caches. This signal is only sampled during powerup reset of the processor.
5	RW	0x1	broadcastouter Enable broadcasting of Outer Shareable transactions: 1'b0: Outer Shareable transactions are not broadcasted externally. 1'b1: Outer Shareable transactions are broadcasted externally. This signal is only sampled during powerup reset of the processor.
4	RW	0x1	broadcastinner Enable broadcasting of Inner Shareable transactions: 1'b0: Inner Shareable transactions are not broadcasted externally. 1'b1: Inner Shareable transactions are broadcasted externally. If BROADCASTINNER is tied HIGH, BROADCASTOUTER must also be tied HIGH. This signal is only sampled during powerup reset of the processor.
3	RW	0x0	clrexmonreq Clearing of the external global exclusive monitor request. When this signal is asserted, it acts as a WFE wake-up event to all the processors in the MPCore device.
2	RW	0x1	clk_enable Global clock enable. This signal can only be deasserted when all the cores in the processor device and the L2 are in WFI low-power state, and the ACE/CHI and ACP interfaces are idle.
1	RW	0x0	dbgl1rstdisable Disable L1 data cache and L2 snoop tag RAM automatic invalidate on reset functionality. 1'b0: Enable automatic invalidation of L1 data cache and L2 snoop tag RAMs on reset. 1'b1: Disable automatic invalidation of L1 data cache and L2 snoop tag RAMs on reset This signal is sampled only during reset of the processor.
0	RW	0x0	l2rstdisable Disable automatic L2 cache invalidate at reset: 1'b0: L2 cache is reset by hardware. 1'b1: L2 cache is not reset by hardware.

LITCORE_GRF_CPU_CON1

Address: Operational Base(0x2600E000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:11	RO	0x00	reserved
10:8	RW	0x0	corereset_hold Core reset hold for a53_1/2/3,low active.
7	RO	0x0	reserved
6:4	RW	0x0	poreset_hold Power on reset hold for a53_1/2/3,low active.
3:2	RO	0x0	reserved
1	RW	0x0	cpu_mem_cfg_idle_trig Triggle cpu_idle for updating memory configuration,high active.
0	RW	0x0	cpu_mem_cfg_idle_en This signal is used to select where cpu_idle is from: 1'b0: cpu_idle is from cpu_mem_cfg_idle_trig 1'b1: cpu_idle is from standbywfil2 & standbywfi And the memory configuration will update when cpu_idle is 1'b1.

LITCORE_GRF_CPU_MEM_CFG_HDSPRF

Address: Operational Base(0x2600E000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:0	RW	0x1410	mem_cfg_hdsprf HDSPRF memory configuration. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

LITCORE_GRF_CPU_MEM_CFG_HSSPRF

Address: Operational Base(0x2600E000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:0	RW	0x0010	mem_cfg_hssprf HSSPRF memory configuration Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

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5.7 BIGCORE_GRF Register Description

5.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
BIGCORE_GRF_CPU_STATUS0	0x002C	W	0x00003C20	CPU status register
BIGCORE_GRF_CPU_CON0	0x0034	W	0x000000B4	CPU control register 0
BIGCORE_GRF_CPU_CON1	0x0038	W	0x00000000	CPU control register 1
BIGCORE_GRF_CPU_MEM_CFG_HDSPRF	0x003C	W	0x00001410	CPU HDSPRF memory configuration register
BIGCORE_GRF_CPU_MEM_CFG_HSSPRF	0x0044	W	0x00000010	CPU HSSPRF memory configuration register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.7.2 Detail Registers Description

BIGCORE_GRF_CPU_STATUS0

Address: Operational Base(0x2600C000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:10	RO	0xf	standbywfi Indicates whether a processer is in WFI low-power state,high active.The bit[0] is for A53_0, and so on.
9:6	RO	0x0	standbywfe Indicates whether a processer is in WFE low-power state,high active.The bit[0] is for A53_0, and so on.
5	RO	0x1	standbywfil2 Indicates whether the L2 is in WFI low-power state,high active.
4	RO	0x0	clrexmonack Clearing of the external global exclusive monitor acknowledge.
3:0	RO	0x0	smpen CPUECTLR.SMPEN output. This signal indicates: 1'b0: The CPUECTLR.SMPEN bit is not set. 1'b1: The CPUECTLR.SMPEN bit is set. The bit[0] is for A72_0, and so on.

BIGCORE_GRF_CPU_CON0

Address: Operational Base(0x2600C000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:12	RW	0x0	cfgte Individual core control of the default exception handling state. It sets the initial value of the TE bit in the CP15 System Control Register (SCTLR when the highest Exception level is AArch32): 1'b0: TE bit is 0. 1'b1: TE bit is 1. This signal is only sampled during powerup reset of the processor.

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	cfgend Individual core control of the endianness configuration at reset. It sets the initial value of the EE bit in the System Control Register (SCTLR or SCTLR_EL3): 1'b0: EE bit is 0. 1'b1: EE bit is 1. This signal is only sampled during powerup reset of the processor.
7	RW	0x1	abd400s_ace_pwrq_permit_deny This signal determines whether the ADB-400 can enter the Q_DENIED state instead of the Q_STOPPED state. This signal is sampled as the slave interface half of the bridge exits reset.
6	RW	0x0	broadcastcachemaint Enable broadcasting of cache maintenance operations to downstream caches: 1'b0: Cache maintenance operations are not broadcasted to downstream caches. 1'b1: Cache maintenance operations are broadcasted to downstream caches. This signal is only sampled during powerup reset of the processor.
5	RW	0x1	broadcastouter Enable broadcasting of Outer Shareable transactions: 1'b0: Outer Shareable transactions are not broadcasted externally. 1'b1: Outer Shareable transactions are broadcasted externally. This signal is only sampled during powerup reset of the processor.
4	RW	0x1	broadcastinner Enable broadcasting of Inner Shareable transactions: 1'b0: Inner Shareable transactions are not broadcasted externally. 1'b1: Inner Shareable transactions are broadcasted externally. If BROADCASTINNER is tied HIGH, BROADCASTOUTER must also be tied HIGH. This signal is only sampled during powerup reset of the processor.
3	RW	0x0	clrexmonreq Clearing of the external global exclusive monitor request. When this signal is asserted, it acts as a WFE wake-up event to all the processors in the MPCore device.
2	RW	0x1	clk_enable Global clock enable. This signal can only be deasserted when all the cores in the processor device and the L2 are in WFI low-power state, and the ACE/CHI and ACP interfaces are idle.
1	RW	0x0	dbgl1rstdisable Disable L1 data cache and L2 snoop tag RAM automatic invalidate on reset functionality. 1'b0: Enable automatic invalidation of L1 data cache and L2 snoop tag RAMs on reset. 1'b1: Disable automatic invalidation of L1 data cache and L2 snoop tag RAMs on reset This signal is sampled only during reset of the processor.
0	RW	0x0	l2rstdisable Disable automatic L2 cache invalidate at reset: 1'b0: L2 cache is reset by hardware. 1'b1: L2 cache is not reset by hardware.

BIGCORE_GRF_CPU_CON1

Address: Operational Base(0x2600C000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:2	RO	0x0000	reserved
1	RW	0x0	cpu_mem_cfg_idle_trig Triggle cpu_idle for updating memory configuration,high active.
0	RW	0x0	cpu_mem_cfg_idle_en This signal is used to select where cpu_idle is from: 1'b0: cpu_idle is from cpu_mem_cfg_idle_trig 1'b1: cpu_idle is from standbywfil2 & standbywfi And the memory configuration will update when cpu_idle is 1'b1.

BIGCORE_GRF_CPU_MEM_CFG_HDSPRF

Address: Operational Base(0x2600C000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:0	RW	0x1410	mem_cfg_hdsprf HDSPRF memory configuration. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

BIGCORE_GRF_CPU_MEM_CFG_HSSPRF

Address: Operational Base(0x2600C000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:0	RW	0x0010	mem_cfg_hssprf HSSPRF memory configuration. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

5.8 CCI_GRF Register Description

5.8.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CCI_GRF_CCI_CON0	0x0000	W	0x0000023C	CCI control register 0

Name	Offset	Size	Reset Value	Description
CCI_GRF_CCI_CON1	0x0004	W	0x00000000	CCI control register 1
CCI_GRF_CCI_CON2	0x0008	W	0x00000000	CCI control register 2
CCI_GRF_CCI_CON3	0x000C	W	0x00000000	CCI control register 3
CCI_GRF_CCI_CON4	0x0010	W	0x00000000	A72 cluster all reset hold control register
CCI_GRF_CCI_STATUS0	0x0034	W	0x00000000	CCI status register 0
CCI_GRF_CCI_STATUS1	0x0038	W	0x00000000	CCI status register 1
CCI_GRF_CCI_STATUS2	0x003C	W	0x00000000	CCI status register 2
CCI_GRF_CCI_STATUS3	0x0040	W	0x00000000	CCI status register 3
CCI_GRF_CCI_STATUS4	0x0044	W	0x00000000	CCI status register 4
CCI_GRF_CCI_MEM_CFG_HDSPRF	0x0054	W	0x00001410	CCI HDSPRF memory configuration register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.8.2 Detail Registers Description

CCI_GRF_CCI_CON0

Address: Operational Base(0x26010000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:11	RO	0x00	reserved
10	RW	0x0	mem_clk_gating_en Memory clock gating enable,high active.
9	RW	0x1	cci_burst_split_all If HIGH, all incoming requests are split into 64-byte transfers, rather than shareable requests only. One bit exists for each ACE-Lite slave interface.
8:6	RW	0x0	cci_qosoverride If HIGH, the internally generated values override the ARQOS and AWQOS input signals. One bit exists for each slave interface.
5:4	RW	0x3	cci_acchanelens2 AC channel enables, one input per slave interface. These inputs override any software enables. Bit[0], DVM message enable This bit is encoded as follows: 1'b0: DVM messages disabled. 1'b1: DVM messages enabled. Bit[1], Snoop enable This bit applies to ACE interfaces only, and is encoded as follows: 1'b0: Snoop requests disabled. 1'b1: Snoop requests enabled.
3:2	RW	0x3	cci_acchannelens1 AC channel enables, one input per slave interface. These inputs override any software enables. Bit[0], DVM message enable This bit is encoded as follows: 1'b0: DVM messages disabled. 1'b1: DVM messages enabled. Bit[1], Snoop enable This bit applies to ACE interfaces only, and is encoded as follows: 1'b0: Snoop requests disabled. 1'b1: Snoop requests enabled.

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Bit	Attr	Reset Value	Description
1:0	RO	0x0	reserved

CCI_GRF_CCI_CON1

Address: Operational Base(0x26010000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15	RO	0x0	reserved
14:12	RW	0x0	awqos_a53_2 A53_2 AWQOS configuration.
11:9	RW	0x0	arqos_a53_1 A53_1 ARQOS configuration.
8:6	RW	0x0	awqos_a53_1 A53_1 AWQOS configuration.
5:3	RW	0x0	arqos_a53_0 A53_0 AWQOS configuration.
2:0	RW	0x0	awqos_a53_0 A53_0 AWQOS configuration.

CCI_GRF_CCI_CON2

Address: Operational Base(0x26010000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15	RO	0x0	reserved
14:12	RW	0x0	arqos_a72_cluster A72 cluster ARQOS configuration.
11:9	RW	0x0	awqos_a72_cluster A72 cluster AWQOS configuration.
8:6	RW	0x0	arqos_a53_3 A53_3 ARQOS configuration.
5:3	RW	0x0	awqos_a53_3 A53_3 AWQOS configuration.
2:0	RW	0x0	arqos_a53_2 A53_2 ARQOS configuration.

CCI_GRF_CCI_CON3

Address: Operational Base(0x26010000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15	RO	0x0	reserved
14	RW	0x0	awcache_buf_m2 CCI AXI master2 AWCACHE bufferable bit. 1'b1: AWCACHE bufferable. 1'b0: AWCACHE non-bufferable.

Bit	Attr	Reset Value	Description
13	RW	0x0	awcache_buf_m1 CCI AXI master1 AWCACHE bufferable bit. 1'b1: AWCACHE bufferable. 1'b0: AWCACHE non-bufferable.
12	RW	0x0	awcache_buf_m0 CCI AXI master0 AWCACHE bufferable bit. 1'b1: AWCACHE bufferable. 1'b0: AWCACHE non-bufferable.
11	RO	0x0	reserved
10	RW	0x0	awcache_buf_sel_m2 CCI AXI master2 AWCACHE bufferable bit select. 1'b1: AWCACHE bufferable bit is from awcache_buf_m2. 1'b0: AWCACHE bufferable bit is from original transaction.
9	RW	0x0	awcache_buf_sel_m1 CCI AXI master1 AWCACHE bufferable bit select. 1'b1: AWCACHE bufferable bit is from awcache_buf_m1. 1'b0: AWCACHE bufferable bit is from original transaction.
8	RW	0x0	awcache_buf_sel_m0 CCI AXI master0 AWCACHE bufferable bit select. 1'b1: AWCACHE bufferable bit is from awcahe_buf_m0. 1'b0: AWCACHE bufferable bit is from original transaction.
7:6	RO	0x0	reserved
5:3	RW	0x0	awqos_hs_ctrl High speed controller AWQOS configuration, like PCIE/SATA/GMAC/USB.
2:0	RW	0x0	arqos_hs_ctrl High speed controller ARQOS configuration, like PCIE/SATA/GMAC/USB.

CCI_GRF_CCI_CON4

Address: Operational Base(0x26010000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:0	RW	0x0000	rst_hold A72 cluster all reset hold control,low active. Bit[0]: areset_adb400_a72_cci Bit[1]: reset hold for nbigcoreporest0 Bit[2]: reset hold for nbigcoreporest1 Bit[3]: reset hold for nbigcoreporest2 Bit[4]: reset hold for nbigcoreporest3 Bit[5]: reset hold for nbigcoreset0 Bit[6]: reset hold for nbigcoreset1 Bit[7]: reset hold for nbigcoreset2 Bit[8]: reset hold for nbigcoreset3 Bit[9]: reset hold for nl2reset_bigcore Bit[10]: reset hold for presetn_bigcore_biu Bit[11]: reset hold for presetn_bigcore_cru Bit[12]: reset hold for presetn_bigcore_grf Bit[13]: reset hold for presetn_dbg_bigcore Bit[14]: reset hold for presetn_pvtpll_bigcore Bit[15]: reset hold for resetn_refpvtpll_bigcore

CCI_GRF_CCI_STATUS0

Address: Operational Base(0x26010000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cci_eventbus_s2 The CCI-500 events exported if enabled in the PMCR. This status indicates 32 slave2 events.

CCI_GRF_CCI_STATUS1

Address: Operational Base(0x26010000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cci_eventbus_s1 The CCI-500 events exported if enabled in the PMCR. This status indicates 32 slave1 events.

CCI_GRF_CCI_STATUS2

Address: Operational Base(0x26010000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cci_eventbus_s0 The CCI-500 events exported if enabled in the PMCR. This status indicates 32 slave0 events.

CCI_GRF_CCI_STATUS3

Address: Operational Base(0x26010000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cci_eventbus_misc The CCI-500 events exported if enabled in the PMCR. This status indicates 21 master events and 11 global events.

CCI_GRF_CCI_STATUS4

Address: Operational Base(0x26010000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	dap_swactive This signal indicates the daplite is active by serial wire.
4:0	RO	0x00	cci_eventbus_glob The CCI-500 events exported if enabled in the PMCR. This status indicates 5 global events.

CCI_GRF_CCI_MEM_CFG_HDSPRF

Address: Operational Base(0x26010000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:0	RW	0x1410	mem_cfg_hdsprf HDSPRF memory configuration. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

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5.9 DDR_GRF Register Description

5.9.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DDR_GRF_CHA_CON0	0x0000	W	0x00000000	DDR CHA Control Register 0
DDR_GRF_CHA_CON1	0x0004	W	0x00000600	DDR CHA Control Register 1
DDR_GRF_CHA_CON2	0x0008	W	0x00000000	DDR CHA Control Register 2
DDR_GRF_CHA_CON4	0x0010	W	0x00000000	DDR CHA Control Register 4
DDR_GRF_CHA_CON6	0x0018	W	0x00000000	DDR CHA Control Register 6
DDR_GRF_CHA_CON7	0x001C	W	0x00000000	DDR CHA Control Register 7
DDR_GRF_CHA_CON8	0x0020	W	0x00000000	DDR CHA Control Register 8
DDR_GRF_CHA_CON12	0x0030	W	0x00000000	DDR CHA Control Register 12
DDR_GRF_CHA_CON13	0x0034	W	0x00000000	DDR CHA Control Register 13
DDR_GRF_CHA_CON14	0x0038	W	0x00000000	DDR CHA Control Register 14
DDR_GRF_CHA_CON15	0x003C	W	0x00000000	DDR CHA Control Register 15
DDR_GRF_CHA_CON16	0x0040	W	0x00000000	DDR CHA Control Register 16
DDR_GRF_CHA_CON17	0x0044	W	0x00000000	DDR CHA Control Register 17
DDR_GRF_CHA_CON18	0x0048	W	0x00000000	DDR CHA Control Register 18
DDR_GRF_CHA_CON19	0x004C	W	0x00000000	DDR CHA Control Register 19
DDR_GRF_CHB_CON0	0x0100	W	0x00000000	DDR CHB Control Register 0
DDR_GRF_CHB_CON1	0x0104	W	0x00000600	DDR CHB Control Register 1
DDR_GRF_CHB_CON2	0x0108	W	0x00000000	DDR CHB Control Register 2
DDR_GRF_CHB_CON4	0x0110	W	0x00000000	DDR CHB Control Register 4
DDR_GRF_CHB_CON6	0x0118	W	0x00000000	DDR CHB Control Register 6
DDR_GRF_CHB_CON7	0x011C	W	0x00000000	DDR CHB Control Register 7
DDR_GRF_CHB_CON8	0x0120	W	0x00000000	DDR CHB Control Register 8
DDR_GRF_CHB_CON12	0x0130	W	0x00000000	DDR CHB Control Register 12
DDR_GRF_CHB_CON13	0x0134	W	0x00000000	DDR CHB Control Register 13
DDR_GRF_CHB_CON14	0x0138	W	0x00000000	DDR CHB Control Register 14
DDR_GRF_CHB_CON15	0x013C	W	0x00000000	DDR CHB Control Register 15
DDR_GRF_CHB_CON16	0x0140	W	0x00000000	DDR CHB Control Register 16
DDR_GRF_CHB_CON17	0x0144	W	0x00000000	DDR CHB Control Register 17
DDR_GRF_CHB_CON18	0x0148	W	0x00000000	DDR CHB Control Register 18
DDR_GRF_CHB_CON19	0x014C	W	0x00000000	DDR CHB Control Register 19
DDR_GRF_CHA_STATUS0	0x0200	W	0x00000000	DDR CHA Status Register 0
DDR_GRF_CHA_STATUS16	0x0220	W	0x7FE01FFB	DDR CHA Status Register 16
DDR_GRF_CHA_STATUS17	0x0224	W	0x00401F21	DDR CHA Status Register 17
DDR_GRF_CHA_STATUS19	0x022C	W	0x00000000	DDR CHA Status Register 19
DDR_GRF_CHB_STATUS0	0x0300	W	0x00000000	DDR CHB Status Register 0
DDR_GRF_CHB_STATUS16	0x0320	W	0x7FE01FFB	DDR CHB Status Register 16
DDR_GRF_CHB_STATUS17	0x0324	W	0x00401F21	DDR CHB Status Register 17
DDR_GRF_CHB_STATUS19	0x032C	W	0x00000000	DDR CHB Status Register 19
DDR_GRF_CHA_PHY_CON0	0x0530	W	0x00000400	DDRPHY CHA Control Register 0
DDR_GRF_CHB_PHY_CON0	0x0534	W	0x00000400	DDRPHY CHB Control Register 0

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Name	Offset	Size	Reset Value	Description
DDR_GRF_CHA_PHY_STATUS0	0x0538	W	0x00000000	DDRPHY CHA Status Register 0
DDR_GRF_CHB_PHY_STATUS0	0x053C	W	0x00000000	DDRPHY CHB Status Register 1
DDR_GRF_COMMON_CON0	0x0540	W	0x00110010	DDR Common Control Register 0
DDR_GRF_COMMON_CON1	0x0544	W	0x14101410	DDR Common Control Register 1
DDR_GRF_COMMON_CON2	0x0548	W	0x00000000	DDR Common Control Register 2
DDR_GRF_COMMON_CON3	0x054C	W	0x00000000	DDR Common Control Register 3
DDR_GRF_COMMON_CON4	0x0550	W	0x00000000	DDR Common Control Register 4
DDR_GRF_COMMON_CON5	0x0554	W	0x00000000	DDR Common Control Register 5
DDR_GRF_STATUS0	0x0580	W	0x00000000	DDR Status Register 0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

The CHA registers is used to configure DDR channel 0 while CHB registers is used to config ure DDR channel 1.

5.9.2 Detail Registers Description

DDR_GRF_CHA_CON0

Address: Operational Base(0x26012000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ddrctl_axi_cg_en DDRCTL AXI port 0~4 aclk gate enable. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable DDRCTL AXI auto gate
7:5	RO	0x0	reserved
4	RW	0x0	ddrctl_slverr_enable DDRCTL slave APB error response enable 1'b0: Disable DDRCTL from responding error 1'b1: Enable DDRCTL from responding error
3:0	RO	0x0	reserved

DDR_GRF_CHA_CON1

Address: Operational Base(0x26012000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	ddrctl_apb_pclk_cg_en DDRCTL APB interface pclk clock gate enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
14:13	RW	0x0	dfi_phyupd_type This signal is the DFI PHY-initiated update. This signal indicates which one of the four types of PHY update times is being requested by the dfi_phyupd_req signal. The valid values are as follows: 2'b00: Tphyupd_type0 2'b01: Tphyupd_type1 2'b10: Tphyupd_type2 2'b11: Tphyupd_type3
12	RW	0x0	ddrmon_pclk_cg_en DDRMON pclk clock gate enable 1'b0: Disable 1'b1: Enable
11:8	RW	0x6	auto_sr_dly When SDRAM is in self-refresh state indicated by selfref_type2_en, the core clk of DDRCTL will be gated after auto_sr_dly clocks.
7	RW	0x0	dfi_scramble_cg_en DFI scramble module clock gate enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	ddrctl_mem_cg_en DDRCTL memory clock gate enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	bsm_clk_cg_en DDRCTL internal bsm module operation clock gate enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	ddrctl_syscreq_cg_en DDRCTL core clock gate enable during SR-PD 1'b0: Disable 1'b1: Enable
3	RW	0x0	selfref_type2_en DDRCTL self-refresh type for auto gate 1'b0: SDRAM is in SR-Powerdown (LPDDR4/5), which was caused by automatic self refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. 1'b1: SDRAM is in SR-Powerdown (LPDDR4/5), which was not caused solely under automatic self refresh control. It could have been caused by hardware low power interface and/or software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error.
2	RW	0x0	ddrctl_core_cg_en DDRCTL core clock gate enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddrctl_apb_cg_en DDRCTL AXI port 0~4 aclk gate enable mode. This register is valid only when ddrctl_axi_cg_en is none zero. 1'b0: The DDRCTL AXI port aclk will be gated and ignores the status of DDRCTL APB slave interface. 1'b1: The DDRCTL AXI port aclk will be ungated when the APB slave interface of DDRCTL is active.
0	RO	0x0	reserved

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DDR_GRF_CHA_CON2

Address: Operational Base(0x26012000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	pre_dfi0_reset_n_sel Select the driver of DDRPHY's dfi0_reset_n signal. 1'b0: Select DDRCTL dfi0_reset_n signal connect to DDRPHY. 1'b1: Select pre_dfi0_reset_n signal connect to DDRPHY.
12	RW	0x0	pre_dfi0_reset_n Control the status of DFI dfi0_reset_n signal when pre_dfi0_reset_n_sel is set to 1'b1.
11	RW	0x0	csysreq_axi_pmu DDRCTL AXI low power request by PMU. 1'b0: DDRCTL AXI low power request is not driven by PMU. 1'b1: DDRCTL AXI low power request is driven by PMU.
10	RW	0x0	csysreq_axi_hwlp DDRCTL AXI low power request by hw_lp_controller(HWLP). 1'b0: DDRCTL AXI low power request is not driven by HWLP. 1'b1: DDRCTL AXI low power request is driven by HWLP.
9	RW	0x0	csysreq_ddrc_pmu DDRCTL ddrc hardware low power request by PMU. 1'b0: DDRCTL ddrc hardware low power request is not driven by PMU. 1'b1: DDRCTL ddrc hardware low power request is driven by PMU.
8	RW	0x0	csysreq_ddrc_hwlp DDRCTL ddrc hardware low power request by hw_lp_controller(HWLP). 1'b0: DDRCTL ddrc hardware low power request is not driven by HWLP. 1'b1: DDRCTL ddrc hardware low power request is driven by HWLP.
7:6	RW	0x0	pre_dfi0_cs_combo_P3 These grf bits drive dfi_cs_P3
5:4	RW	0x0	pre_dfi0_cs_combo_P2 These grf bits drive dfi_cs_P2
3:2	RW	0x0	pre_dfi0_cs_combo_P1 These grf bits drive dfi_cs_P1
1:0	RW	0x0	pre_dfi0_cs_combo_P0 These grf bits drive dfi_cs_P0

DDR_GRF_CHA_CON4

Address: Operational Base(0x26012000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	awpoison DDRCTL AXI port 0~4 write address poison. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable poison on write command
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x00	arpoison DDRCTL AXI port 0~4 read address poison. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable poison on read command
15:13	RO	0x0	reserved
12:8	RW	0x00	awautopre DDRCTL AXI port 0~4 auto-precharge signal for write command. This register should be keep 1'b0 for each AXI port. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on.
7:5	RO	0x0	reserved
4:0	RW	0x00	arautopre DDRCTL AXI port 0~4 auto-precharge signal for read command. This register should be keep 1'b0 for each AXI port. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on.

DDR_GRF_CHA_CON6

Address: Operational Base(0x26012000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	cmd_dly_eq0_en Control the assertion of dfi_lp_data_req. 1'b0: Don't assert the dfi_lp_data_req again during DDRCTL auto SR-PD when dfi_lp_data_req desserts because of DDRPHY dfi_phyupd_req assertion. 1'b1: Assert the dfi_lp_data_req again during DDRCTL auto SR-PD when dfi_lp_data_req desserts because of DDRPHY dfi_phyupd_req assertion.
14:8	RW	0x00	wr_lat_delay Control dfi_lp_data_req high level time during write.
7	RO	0x0	reserved
6:0	RW	0x00	rd_lat_delay Control dfi_lp_data_req high level time during read.

DDR_GRF_CHA_CON7

Address: Operational Base(0x26012000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	scramble_lp5_8bank_mode 1'b0: LPDDR5 8 bank mode is disabled. 1'b1: LPDDR5 8 bank mode is enabled.
13	RW	0x0	scramble_rdbi_en 1'b0: Read DBI is disabled. 1'b1: Read DBI is enabled.
12	RW	0x0	scramble_wdbi_en 1'b0: Write DBI is disabled. 1'b1: Write DBI is enabled.
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	scramble_dq_bus_width 2'b00: 8 bits 2'b01: 16 bits 2'b10: 32 bits Others: Reserved
7:6	RW	0x0	scramble_rank_num 2'b00: 1 rank 2'b01: 2 rank 2'b11: 4 rank 2'b10: Invalid
5:4	RW	0x0	scramble_ddr_bl 2'b00: BL4 2'b01: BL8 2'b10: BL16 2'b11: Invalid
3	RW	0x0	scramble_freq_ratio DDR frequency ratio for DFI Scramble 1'b0: 1:2 1'b1: 1:4
2:0	RW	0x0	scramble_ddr_type DDR type for DFI Scramble 3'b101: LPDDR4/4X 3'b110: LPDDR5 Others: Reserved

DDR_GRF_CHA_CON8

Address: Operational Base(0x26012000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	scramble_dfi_phyupd_ack_noff 1'b0: dfi_phyupd_ack is output from DFI scramble after 3 pipelines. 1'b1: dfi_phyupd_ack is output from DFI scramble without any pipelines.
14	RW	0x0	scramble_dfi_ctrlupd_req_noff 1'b0: dfi_ctrlupd_req is output from DFI scramble after 3 pipelines. 1'b1: dfi_ctrlupd_req is output from DFI scramble without any pipelines.
13	RW	0x0	scramble_dfi_phymstr_ack_noff 1'b0: dfi_phymstr_ack is output from DFI scramble after 3 pipelines. 1'b1: dfi_phymstr_ack is output from DFI scramble without any pipelines.
12	RO	0x0	reserved
11	RW	0x0	scramble_dfi_lp_data_req_noff 1'b0: dfi_lp_data_req is output from DFI scramble after 3 pipelines. 1'b1: dfi_lp_data_req is output from DFI scramble without any pipelines.

Bit	Attr	Reset Value	Description
10	RW	0x0	scramble_dfi_lp_ctrl_req_noff 1'b0: dfi_lp_ctrl_req is output from DFI scramble after 3 pipelines. 1'b1: dfi_lp_ctrl_req is output from DFI scramble without any pipelines.
9	RW	0x0	scramble_wdbi_pattern_opt 1'b0: DFI write data will be fixed to 8'hff when write DBI is enabled. 1'b1: DFI write data will be fixed to 8'hf8 when write DBI is enabled.
8	RW	0x0	scramble_ddr_2t_en 2T timing mode enable. Not support, please keep default value.
7	RO	0x0	reserved
6:4	RW	0x0	scramble_tphy_wrdata For wck:ck=2:1, set this register same to DDRCTL register (DFITMG0.dfi_tphy_wrdata)/2. For wck:ck=4:1, set this register same to DDRCTL register (DFITMG0.dfi_tphy_wrdata)/4.
3:2	RO	0x0	reserved
1:0	RW	0x0	scramble_tphy_wrlat Set this register according to DDRCTL register DFITMG0.dfi_tphy_wrlat[1:0] and DDR type. For LPDDR4, please set this register to ~dfi_tphy_wrlat[0], allowed value is 0/1. For LPDDR5, if wck:ck = 2:1, set this register to dfi_tphy_wrlat[0]. For LPDDR5, if wck:ck = 4:1, set this register to dfi_tphy_wrlat[1:0].

DDR_GRF_CHA_CON12

Address: Operational Base(0x26012000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x00	hpr_entry_num The HPR entry numbers that used to make write command go to critical when wr_mask_by_hpr is set to 1'b1. If wr_mask_by_hpr is set to 1'b0, hpr_entry_num is not used.
7:5	RO	0x0	reserved
4	RW	0x0	wr_mask_by_hpr If set to 1, when the HPR is not empty, it will prevents awurgent from triggering go2critical_wr. Thus the HPR requests are less likely to be blocked by write requests.
3	RW	0x0	rrbtoken_empty2critical 1'b0: The DDRCTL read CAM will not go to critical state when rrb token is empty. When the RRB token is empty, the PA cannot arbitrate to the read request, and the priority mechanism of the read request may be invalidated. 1'b1: The DDRCTL read CAM will go to critical state when rrb read token is empty. So that the read CAM is prioritized for scheduling, and the PA recovers the arbitration ability of read requests as soon as possible.

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Bit	Attr	Reset Value	Description
2	RW	0x0	wr_full2critical 1'b0: The DDRCTL WR CAM will go to critical state when awurgent assert. 1'b1: The DDRCTL WR CAM will go to critical state when awurgent assert and WR credits are empty simultaneously.
1	RW	0x0	hpr_full2critical 1'b0: The DDRCTL HPR will go to critical state when arurgent assert. 1'b1: The DDRCTL HPR will go to critical state when arurgent assert and HPR credits are empty simultaneously. It is strongly recommended to set hpr_full2critical=0, otherwise unexpected situations may occur.
0	RW	0x0	lpr_full2critical 1'b0: The DDRCTL LPR will go to critical state when arurgent assert. 1'b1: The DDRCTL LPR will go to critical state when arurgent assert and LPR credits are empty simultaneously.

DDR_GRF_CHA_CON13

Address: Operational Base(0x26012000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	awqos_urgent_en Enable the urgent mechanism of DDRCTL's AXI write port 0~4 according to the Awqos. Each bit is corresponding to DDRCTL's AXI write port 0~4 respectively. For example, awqos_urgent_en[0] is used to enable AXI write port 0, awqos_urgent_en[1] is used to enable AXI write port 1 and so on. 1'b0: Disable 1'b1: Enable
7:5	RO	0x0	reserved
4:0	RW	0x00	arqos_urgent_en Enable the urgent mechanism of DDRCTL's AXI read port 0~4 according to the Arqos. Each bit is corresponding to DDRCTL's AXI read port 0~4 respectively. For example, arqos_urgent_en[0] is used to enable AXI read port 0, arqos_urgent_en[1] is used to enable AXI read port 1 and so on. 1'b0: Disable 1'b1: Enable

DDR_GRF_CHA_CON14

Address: Operational Base(0x26012000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	press_aw_th Qos/Press threshold for wite requests. The awugent may assert only when press (qos) > grf_press_aw_th. The press_aw_th[2:0] set the threshold for AXI write port 0. The press_aw_th[5:3] set the threshold for AXI write port 1, and so on.
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:0	RW	0x0000	press_ar_th Qos/Press threshold for read requests. The arugent may assert only when press (qos) > grf_press_ar_th. The press_ar_th[2:0] set the threshold for AXI read port 0. The press_ar_th[5:3] set the threshold for AXI read port 1, and so on.

DDR_GRF_CHA_CON15

Address: Operational Base(0x26012000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	press_cg_en Clock gate enable of DDRCTL's urgent control module. Each bit is corresponding to DDRCTL's AXI port 0~4 respectively. 1'b0: Disable 1'b1: Enable If the DDRCTL's urgent control module is not used, please set press_cg_en[4:0] to 5'h1f to save power.
7:5	RO	0x0	reserved
4:0	RW	0x00	press_en Urgent control function enable for DDRCTL's AXI port 0~4. Each bit is corresponding to DDRCTL's AXI port 0~4 respectively. For example, press_en[0] is used to control AXI port 0, press_en[1] is used to control AXI port 1 and so on. 1'b0: Disable 1'b1: Enable

DDR_GRF_CHA_CON16

Address: Operational Base(0x26012000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	press_rdwr_order Read/write order enable of DDRCTL's urgent control module. Each bit is corresponding to DDRCTL's AXI port 0~4 respectively. For example, press_rdwr_order[0] is used to control AXI port 0, press_rdwr_order[1] is used to control AXI port 1 and so on.
7	RO	0x0	reserved
6:2	RW	0x00	press_queue_wait_limit The QOS may trigger urgent only when the request with high QOS in the queue is not poped for press_queue_wait_limit*4 cycles.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	press_policy Bit[0]: 1'b0: The arurgent and awurgent will not assert simultaneously. 1'b1: The arurgent and awurgent may assert simultaneously. Bit[1]: 1'b0: The QOS queue pops once when the queue in DDRCTL pops. 1'b1: The QOS queue pops once when the queue in DDRCTL pops and is arbitrated by the PA.

DDR_GRF_CHA_CON17

Address: Operational Base(0x26012000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	pa_rmask_en The DDRCTL's PA(Port Arbitar) read mask enable. Only even bits are used, odd bits are ignored. For example, pa_rmask_en[0]/[2]/[4]/[6]/[8] is used to control DDRCTL AXI read port 0/1/2/3/4. If enabled, read commands from that AXI read port are not arbitared and are blocked in read address FIFO. 1'b0: Disable 1'b1: Enable

DDR_GRF_CHA_CON18

Address: Operational Base(0x26012000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x00	pa_wmask_en The DDRCTL's PA(Port Arbitar) write mask enable. Each bit is corresponding to DDRCTL's AXI write port 0~4. For example, pa_wmask_en[0] is used to enable the write port mask function for DDRCTL's AXI write port 0. 1'b0: Disable 1'b1: Enable

DDR_GRF_CHA_CON19

Address: Operational Base(0x26012000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	pa_mask_urgent_en Bit0: If set to 1'b1, the DDRCTL's PA mask control module will generate read urgent signal(vop_axi0_rd_urgency_out) driven by VOP AXI0 urgency signal(vop_axi0_rd_urgency). The vop_axi0_rd_urgency_out will ored together with urgency signal from AXI press control module, and the output from the OR-gate finally connected to the DDRCTL AXI read port 0. Bit1: If set to 1'b1, the DDRCTL's PA mask control module will generate read urgent signal(vop_axi1_rd_urgency_out) driven by VOP AXI1 urgency signal(vop_axi1_rd_urgency). The vop_axi1_rd_urgency_out will ored together with urgency signal from AXI press control module, and the output from the OR-gate finally connected to the DDRCTL AXI read port 1. Bit2: If set to 1'b1, the DDRCTL's PA mask control module will generate read urgent signal(ebc_axi_rd_urgency_out) driven by EBC AXI urgency signal(ebc_axi_rd_urgency). The ebc_axi_rd_urgency_out will ored together with urgency signal from AXI press control module, and the output from the OR-gate finally connected to the DDRCTL AXI read port 2.
11:9	RO	0x0	reserved
8	RW	0x0	pa_mask_cg_en Clock gate enable of DDRCTL's PA mask control module. 1'b0: Disable 1'b1: Enable If the DDRCTL's PA mask control module is not used, please set pa_mask_cg_en to 1'b1 to save power.
7:5	RO	0x0	reserved
4:0	RW	0x00	pa_mask_rdwr_order Read/write order enable. Each bit is corresponding to DDRCTL's read PA. If the corresponding bit is set, the DDRCTL's AXI write port can't be masked when the read port is urgent.

DDR_GRF_CHB_CON0

Address: Operational Base(0x26012000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ddrctl_axi_cg_en DDRCTL AXI port 0~4 aclk gate enable. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable DDRCTL AXI auto gate
7:5	RO	0x0	reserved
4	RW	0x0	ddrctl_slverr_enable DDRCTL slave APB error response enable 1'b0: Disable DDRCTL from responding error 1'b1: Enable DDRCTL from responding error
3:0	RO	0x0	reserved

DDR_GRF_CHB_CON1

Address: Operational Base(0x26012000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	ddrctl_apb_pclk_cg_en DDRCTL APB interface pclk clock gate enable 1'b0: Disable 1'b1: Enable
14:13	RW	0x0	dfi_phyupd_type This signal is the DFI PHY-initiated update. This signal indicates which one of the four types of PHY update times is being requested by the dfi_phyupd_req signal. The valid values are as follows: 2'b00: Tphyupd_type0 2'b01: Tphyupd_type1 2'b10: Tphyupd_type2 2'b11: Tphyupd_type3
12	RW	0x0	ddrmon_pclk_cg_en DDRMON pclk clock gate enable 1'b0: Disable 1'b1: Enable
11:8	RW	0x6	auto_sr_dly When SDRAM is in self-refresh state indicated by selfref_type2_en, the core clk of DDRCTL will be gated after auto_sr_dly clocks.
7	RW	0x0	dfi_scramble_cg_en DFI scramble module clock gate enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	ddrctl_mem_cg_en DDRCTL memory clock gate enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	bsm_clk_cg_en DDRCTL internal bsm module operation clock gate enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	ddrctl_syscreq_cg_en DDRCTL core clk gate enable during SR-PD 1'b0: Disable 1'b1: Enable
3	RW	0x0	selfref_type2_en DDRCTL self-refresh type for auto gate 1'b0: SDRAM is in SR-Powerdown (LPDDR4/5), which was caused by automatic self refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. 1'b1: SDRAM is in SR-Powerdown (LPDDR4/5), which was not caused solely under automatic self refresh control. It could have been caused by hardware low power interface and/or software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error.
2	RW	0x0	ddrctl_core_cg_en DDRCTL core clk gate enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	ddrctl_apb_cg_en_mode DDRCTL AXI port 0~4 aclk gate enable mode. This register is valid only when ddrctl_axi_cg_en is none zero. 1'b0: The DDRCTL AXI port aclk will be gated and ignores the status of DDRCTL APB slave interface. 1'b1: The DDRCTL AXI port aclk will be ungated when the APB slave interface of DDRCTL is active.
0	RO	0x0	reserved

DDR_GRF_CHB_CON2

Address: Operational Base(0x26012000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	pre_dfi0_reset_n_sel Select the driver of DDRPHY's dfi0_reset_n signal. 1'b0: Select DDRCTL dfi0_reset_n signal connect to DDRPHY. 1'b1: Select pre_dfi0_reset_n signal connect to DDRPHY.
12	RW	0x0	pre_dfi0_reset_n Control the status of DFI dfi0_reset_n signal when pre_dfi0_reset_n_sel is set to 1'b1.
11	RW	0x0	csysreq_axi_pmu DDRCTL AXI low power request by PMU. 1'b0: DDRCTL AXI low power request is not driven by PMU. 1'b1: DDRCTL AXI low power request is driven by PMU.
10	RW	0x0	csysreq_axi_hwlp DDRCTL AXI low power request by hw_lp_controller(HWLP). 1'b0: DDRCTL AXI low power request is not driven by HWLP. 1'b1: DDRCTL AXI low power request is driven by HWLP.
9	RW	0x0	csysreq_ddrc_pmu DDRCTL ddrc hardware low power request by PMU. 1'b0: DDRCTL ddrc hardware low power request is not driven by PMU. 1'b1: DDRCTL ddrc hardware low power request is driven by PMU.
8	RW	0x0	csysreq_ddrc_hwlp DDRCTL ddrc hardware low power request by hw_lp_controller(HWLP). 1'b0: DDRCTL ddrc hardware low power request is not driven by HWLP. 1'b1: DDRCTL ddrc hardware low power request is driven by HWLP.
7:6	RW	0x0	pre_dfi0_cs_combo_P3 These grf bits drive dfi_cs_P3
5:4	RW	0x0	pre_dfi0_cs_combo_P2 These grf bits drive dfi_cs_P2
3:2	RW	0x0	pre_dfi0_cs_combo_P1 These grf bits drive dfi_cs_P1
1:0	RW	0x0	pre_dfi0_cs_combo_P0 These grf bits drive dfi_cs_P0

DDR_GRF_CHB_CON4

Address: Operational Base(0x26012000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	awpoison DDRCTL AXI port 0~4 write address poison. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable poison on write command
23:21	RO	0x0	reserved
20:16	RW	0x00	arpoison DDRCTL AXI port 0~4 read address poison. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable poison on read command
15:13	RO	0x0	reserved
12:8	RW	0x00	awautopre DDRCTL AXI port 0~4 auto-precharge signal for write command. This register should be keep 1'b0 for each AXI port. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on.
7:5	RO	0x0	reserved
4:0	RW	0x00	arautopre DDRCTL AXI port 0~4 auto-precharge signal for read command. This register should be keep 1'b0 for each AXI port. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on.

DDR_GRF_CHB_CON6

Address: Operational Base(0x26012000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	cmd_dly_eq0_en Control the assertion of dfi_lp_data_req. 1'b0: Don't assert the dfi_lp_data_req again during DDRCTL auto SR-PD when dfi_lp_data_req desserts because of DDRPHY dfi_phyupd_req assertion. 1'b1: Assert the dfi_lp_data_req again during DDRCTL auto SR-PD when dfi_lp_data_req desserts because of DDRPHY dfi_phyupd_req assertion.
14:8	RW	0x00	wr_lat_delay Control dfi_lp_data_req high level time during write
7	RO	0x0	reserved
6:0	RW	0x00	rd_lat_delay Control dfi_lp_data_req high level time during read

DDR_GRF_CHB_CON7

Address: Operational Base(0x26012000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14	RW	0x0	scramble_lp5_8bank_mode 1'b0: LPDDR5 8 bank mode is disabled. 1'b1: LPDDR5 8 bank mode is enabled.
13	RW	0x0	scramble_rdbi_en 1'b0: Read DBI is disabled. 1'b1: Read DBI is enabled.
12	RW	0x0	scramble_wdbi_en 1'b0: Write DBI is disabled. 1'b1: Write DBI is enabled.
11:10	RO	0x0	reserved
9:8	RW	0x0	scramble_dq_bus_width 2'b00: 8 bits 2'b01: 16 bits 2'b10: 32 bits Others: Reserved
7:6	RW	0x0	scramble_rank_num 2'b00: 1 rank 2'b01: 2 rank 2'b11: 4 rank 2'b10: Invalid
5:4	RW	0x0	scramble_ddr_bl 2'b00: BL4 2'b01: BL8 2'b10: BL16 2'b11: Invalid
3	RW	0x0	scramble_freq_ratio DDR frequency ratio for DFI Scramble 1'b0: 1:2 1'b1: 1:4
2:0	RW	0x0	scramble_ddr_type DDR type for DFI Scramble 3'b101: LPDDR4/4X 3'b110: LPDDR5 Others: Reserved

DDR_GRF_CHB_CON8

Address: Operational Base(0x26012000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	scramble_dfi_phyupd_ack_noff 1'b0: dfi_phyupd_ack is output from DFI scramble after 3 pipelines. 1'b1: dfi_phyupd_ack is output from DFI scramble without any pipelines.
14	RW	0x0	scramble_dfi_ctrlupd_req_noff 1'b0: dfi_ctrlupd_req is output from DFI scramble after 3 pipelines. 1'b1: dfi_ctrlupd_req is output from DFI scramble without any pipelines.

Bit	Attr	Reset Value	Description
13	RW	0x0	scramble_dfi_phymstr_ack_noff 1'b0: dfi_phymstr_ack is output from DFI scramble after 3 pipelines. 1'b1: dfi_phymstr_ack is output from DFI scramble without any pipelines.
12	RO	0x0	reserved
11	RW	0x0	scramble_dfi_lp_data_req_noff 1'b0: dfi_lp_data_req is output from DFI scramble after 3 pipelines. 1'b1: dfi_lp_data_req is output from DFI scramble without any pipelines.
10	RW	0x0	scramble_dfi_lp_ctrl_req_noff 1'b0: dfi_lp_ctrl_req is output from DFI scramble after 3 pipelines. 1'b1: dfi_lp_ctrl_req is output from DFI scramble without any pipelines.
9	RW	0x0	scramble_wdbi_pattern_opt 1'b0: DFI write data will be fixed to 8'hff when write DBI is enabled. 1'b1: DFI write data will be fixed to 8'hf8 when write DBI is enabled.
8	RW	0x0	scramble_ddr_2t_en 2T timing mode enable. Not support, please keep default value.
7	RO	0x0	reserved
6:4	RW	0x0	scramble_tphy_wrdata For wck:ck=2:1, set this register same to DDRCTL register (DFITMG0.dfi_tphy_wrdata)/2. For wck:ck=4:1, set this register same to DDRCTL register (DFITMG0.dfi_tphy_wrdata)/4.
3:2	RO	0x0	reserved
1:0	RW	0x0	scramble_tphy_wrlat Set this register according to DDRCTL register DFITMG0.dfi_tphy_wrlat[1:0] and DDR type. For LPDDR4, please set this register to ~dfi_tphy_wrlat[0], allowed value is 0/1. For LPDDR5, if wck:ck = 2:1, set this register to dfi_tphy_wrlat[0]. For LPDDR5, if wck:ck = 4:1, set this register to dfi_tphy_wrlat[1:0].

DDR_GRF_CHB_CON12

Address: Operational Base(0x26012000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x00	hpr_entry_num The HPR entry numbers that used to make write command go to critical when wr_mask_by_hpr is set to 1'b1. If wr_mask_by_hpr is set to 1'b0, hpr_entry_num is not used.
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	wr_mask_by_hpr If set to 1, when the HPR is not empty, it will prevents awurgent from triggering go2critical_wr. Thus the HPR requests are less likely to be blocked by write requests.
3	RW	0x0	rrbtoken_empty2critical 1'b0: The DDRCTL read CAM will not go to critical state when rrb token is empty. When the RRB token is empty, the PA cannot arbitrate to the read request, and the priority mechanism of the read request may be invalidated. 1'b1: The DDRCTL read CAM will go to critical state when rrb read token is empty. So that the read CAM is prioritized for scheduling, and the PA recovers the arbitration ability of read requests as soon as possible.
2	RW	0x0	wr_full2critical 1'b0: The DDRCTL WR CAM will go to critical state when awurgent assert. 1'b1: The DDRCTL WR CAM will go to critical state when awurgent assert and WR credits are empty simultaneously.
1	RW	0x0	hpr_full2critical 1'b0: The DDRCTL HPR will go to critical state when arurgent assert. 1'b1: The DDRCTL HPR will go to critical state when arurgent assert and HPR credits are empty simultaneously. It is strongly recommended to set hpr_full2critical=0, otherwise unexpected situations may occur.
0	RW	0x0	lpr_full2critical 1'b0: The DDRCTL LPR will go to critical state when arurgent assert. 1'b1: The DDRCTL LPR will go to critical state when arurgent assert and LPR credits are empty simultaneously.

DDR_GRF_CHB_CON13

Address: Operational Base(0x26012000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	awqos_urgent_en Enable the urgent mechanism of DDRCTL's AXI write port 0~4 according to the Awqos. Each bit is corresponding to DDRCTL's AXI write port 0~4 respectively. For example, awqos_urgent_en[0] is used to enable AXI write port 0, awqos_urgent_en[1] is used to enable AXI write port 1 and so on. 1'b0: Disable 1'b1: Enable
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	arqos_urgent_en Enable the urgent mechanism of DDRCTL's AXI read port 0~4 according to the Arqos. Each bit is corresponding to DDRCTL's AXI read port 0~4 respectively. For example, arqos_urgent_en[0] is used to enable AXI read port 0, arqos_urgent_en[1] is used to enable AXI read port 1 and so on. 1'b0: Disable 1'b1: Enable

DDR_GRF_CHB_CON14

Address: Operational Base(0x26012000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	press_aw_th Qos/Press threshold for wite requests. The awugent may assert only when press (qos) > grf_press_aw_th. The press_aw_th[2:0] set the threshold for axi write port 0. The press_aw_th[5:3] set the threshold for axi write port 1, and so on.
15	RO	0x0	reserved
14:0	RW	0x0000	press_ar_th Qos/Press threshold for read requests. The arugent may assert only when press (qos) > grf_press_ar_th. The press_ar_th[2:0] set the threshold for AXI read port 0. The press_ar_th[5:3] set the threshold for AXI read port 1, and so on.

DDR_GRF_CHB_CON15

Address: Operational Base(0x26012000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	press_cg_en Clock gate enable of DDRCTL's urgent control module. Each bit is corresponding to DDRCTL's AXI port 0~4 respectively. 1'b0: Disable 1'b1: Enable If the DDRCTL's urgent control module is not used, please set press_cg_en[4:0] to 5'h1f to save power.
7:5	RO	0x0	reserved
4:0	RW	0x00	press_en Urgent control function enable for DDRCTL's AXI port 0~4. Each bit is corresponding to DDRCTL's AXI port 0~4 respectively. For example, press_en[0] is used to control AXI port 0, press_en[1] is used to control AXI port 1 and so on. 1'b0: Disable 1'b1: Enable

DDR_GRF_CHB_CON16

Address: Operational Base(0x26012000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	press_rdwr_order Read/write order enable of DDRCTL's urgent control module. Each bit is corresponding to DDRCTL's AXI port 0~4 respectively. For example, press_rdwr_order[0] is used to control AXI port 0, press_rdwr_order[1] is used to control AXI port 1 and so on.
7	RO	0x0	reserved
6:2	RW	0x00	press_queue_wait_limit The QOS may trigger urgent only when the request with high QOS in the queue is not poped for press_queue_wait_limit*4 cycles.
1:0	RW	0x0	press_policy Bit[0]: 1'b0: The arurgent and awurgent will not assert simultaneously. 1'b1: The arurgent and awurgent may assert simultaneously. Bit[1]: 1'b0: The QOS queue pops once when the queue in DDRCTL pops. 1'b1: The QOS queue pops once when the queue in DDRCTL pops and is arbitrated by the PA.

DDR_GRF_CHB_CON17

Address: Operational Base(0x26012000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	pa_rmask_en The DDRCTL's PA(Port Arbitar) read mask enable. Only even bits are used, odd bits are ignored. For example, pa_rmask_en[0]/[2]/[4]/[6]/[8] is used to control DDRCTL AXI read port 0/1/2/3/4. If enabled, read commands from that AXI read port are not arbitared and are blocked in read address FIFO. 1'b0: Disable 1'b1: Enable

DDR_GRF_CHB_CON18

Address: Operational Base(0x26012000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	pa_wmask_en The DDRCTL's PA(Port Arbitar) write mask enable. Each bit is corresponding to DDRCTL's AXI write port 0~4. For example, pa_wmask_en[0] is used to enable the write port mask function for DDRCTL's AXI write port 0. 1'b0: Disable 1'b1: Enable

DDR_GRF_CHB_CON19

Address: Operational Base(0x26012000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	pa_mask_urgent_en Bit0: If set to 1'b1, the DDRCTL's PA mask control module will generate read urgent signal(vop_axi0_rd_urgency_out) driven by VOP AXI0 urgency signal(vop_axi0_rd_urgency). The vop_axi0_rd_urgency_out will ored together with urgency signal from AXI press control module, and the output from the OR-gate finally connected to the DDRCTL AXI read port 0. Bit1: If set to 1'b1, the DDRCTL's PA mask control module will generate read urgent signal(vop_axi1_rd_urgency_out) driven by VOP AXI1 urgency signal(vop_axi1_rd_urgency). The vop_axi1_rd_urgency_out will ored together with urgency signal from AXI press control module, and the output from the OR-gate finally connected to the DDRCTL AXI read port 1. Bit2: If set to 1'b1, the DDRCTL's PA mask control module will generate read urgent signal(ebc_axi_rd_urgency_out) driven by EBC AXI urgency signal(ebc_axi_rd_urgency). The ebc_axi_rd_urgency_out will ored together with urgency signal from AXI press control module, and the output from the OR-gate finally connected to the DDRCTL AXI read port 2.
11:9	RO	0x0	reserved
8	RW	0x0	pa_mask_cg_en Clock gate enable of DDRCTL's PA mask control module. 1'b0: Disable 1'b1: Enable If the DDRCTL's PA mask control module is not used, please set pa_mask_cg_en to 1'b1 to save power.
7:5	RO	0x0	reserved
4:0	RW	0x00	pa_mask_rdwr_order Read/write order enable. Each bit is corresponding to DDRCTL's read PA. If the corresponding bit is set, the DDRCTL's AXI write port can't be masked when the read port is urgent.

DDR_GRF_CHA_STATUS0

Address: Operational Base(0x26012000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data0 MRR data from DDRCTL

DDR_GRF_CHA_STATUS16

Address: Operational Base(0x26012000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x1	bready_4 bready_4 signal status of DDRCTL AXI write port 4.
29	RO	0x1	bready_3 bready_3 signal status of DDRCTL AXI write port 3.
28	RO	0x1	bready_2 bready_2 signal status of DDRCTL AXI write port 2.
27	RO	0x1	bready_1 bready_1 signal status of DDRCTL AXI write port 1.
26	RO	0x1	bready_0 bready_0 signal status of DDRCTL AXI write port 0.
25	RO	0x1	rready_4 rready_4 signal status of DDRCTL AXI read port 4.
24	RO	0x1	rready_3 rready_3 signal status of DDRCTL AXI read port 3.
23	RO	0x1	rready_2 rready_2 signal status of DDRCTL AXI read port 2.
22	RO	0x1	rready_1 rready_1 signal status of DDRCTL AXI read port 1.
21	RO	0x1	rready_0 rready_0 signal status of DDRCTL AXI read port 0.
20	RO	0x0	scramble_shift_ready Scramble shift ready status 1'b0: Not ready 1'b1: Ready
19:18	RO	0x0	st_stat_ddrc_reg_selfref_type DDRCTL selfrefresh type status Flags if SR-Powerdown is entered and if it was under automatic self refresh control only or not. 2'b00: SDRAM is not in SR-Powerdown. 2'b01: SDRAM is in self refresh, which was caused by PHY master request. 2'b10: SDRAM is in SR-Powerdown, which was not caused solely under automatic self refresh control. 2'b11: SDRAM is in SR-Powerdown, which was caused by automatic self refresh only.
17:13	RO	0x00	st_cactive_aclk DDRCTL aclk cactive status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Not active 1'b1: Active
12:8	RO	0x1f	st_csysack_aclk DDRCTL aclk csysack status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Low power request is acknowledged. 1'b1: Low power request is not acknowledged.
7:3	RO	0x1f	st_csysreq_aclk DDRCTL aclk csysreq status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Low power request 1'b1: No low power request

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Bit	Attr	Reset Value	Description
2	RO	0x0	st_cactive_ddrc DDRCTL core cactive status 1'b0: Not active 1'b1: Active
1	RO	0x1	st_csysack_ddrc DDRCTL core low power ack status 1'b0: Low power request is acknowledged. 1'b1: Low power request is not acknowledged.
0	RO	0x1	st_csysreq_ddrc DDRCTL core low power request status 1'b0: Low power request. 1'b1: No low power request.

DDR_GRF_CHA_STATUS17

Address: Operational Base(0x26012000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RO	0x40	st_wr_credit_cnt DDRCTL wr credit count
15	RO	0x0	reserved
14:8	RO	0x1f	st_hpr_credit_cnt DDRCTL hpr credit count
7	RO	0x0	reserved
6:0	RO	0x21	st_lpr_credit_cnt DDRCTL lpr credit count

DDR_GRF_CHA_STATUS19

Address: Operational Base(0x26012000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RO	0x0	st_derate_temp_limit_intr_fault This signal is the derate temperature limit fault. This is a version of derate_temp_limit_intr, which can not be disabled or forced via a register. It is a 2-bit antivalent signal with encoding as follows: 2'b01: No Fault 2'b10: Fault Detected
7:6	RO	0x0	reserved
5:0	RO	0x00	st_hif_refresh_req_bank This signal indicates the next bank that is refreshed; for multi-rank configurations, the bank number is reported independently for each rank, and the information for all ranks is concatenated to form this signal.

DDR_GRF_CHB_STATUS0

Address: Operational Base(0x26012000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data0 MRR data from DDRCTL

DDR_GRF_CHB_STATUS16

Address: Operational Base(0x26012000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x1	bready_4 bready_4 signal status of DDRCTL AXI write port 4.

Bit	Attr	Reset Value	Description
29	RO	0x1	bready_3 bready_3 signal status of DDRCTL AXI write port 3.
28	RO	0x1	bready_2 bready_2 signal status of DDRCTL AXI write port 2.
27	RO	0x1	bready_1 bready_1 signal status of DDRCTL AXI write port 1.
26	RO	0x1	bready_0 bready_0 signal status of DDRCTL AXI write port 0.
25	RO	0x1	rready_4 rready_4 signal status of DDRCTL AXI read port 4.
24	RO	0x1	rready_3 rready_3 signal status of DDRCTL AXI read port 3.
23	RO	0x1	rready_2 rready_2 signal status of DDRCTL AXI read port 2.
22	RO	0x1	rready_1 rready_1 signal status of DDRCTL AXI read port 1.
21	RO	0x1	rready_0 rready_0 signal status of DDRCTL AXI read port 0.
20	RO	0x0	scramble_shift_ready Scramble shift ready status 1'b0: Not ready 1'b1: Ready
19:18	RO	0x0	st_stat_ddrc_reg_selfref_type DDRCTL selfrefresh type status Flags if SR-Powerdown is entered and if it was under automatic self refresh control only or not. 2'b00: SDRAM is not in SR-Powerdown. 2'b01: SDRAM is in self refresh, which was caused by PHY master request. 2'b10: SDRAM is in SR-Powerdown, which was not caused solely under automatic self refresh control. 2'b11: SDRAM is in SR-Powerdown, which was caused by automatic self refresh only.
17:13	RO	0x00	st_cactive_aclk DDRCTL aclk cactive status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Not active 1'b1: Active
12:8	RO	0x1f	st_csysack_aclk DDRCTL aclk csysack status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Low power request is acknowledged. 1'b1: Low power request is not acknowledged.
7:3	RO	0x1f	st_csysreq_aclk DDRCTL aclk csysreq status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Low power request 1'b1: No low power request
2	RO	0x0	st_cactive_ddrc DDRCTL core cactive status 1'b0: Not active 1'b1: Active

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Bit	Attr	Reset Value	Description
1	RO	0x1	st_csysack_ddrc DDRCTL core low power ack status 1'b0: Low power request is acknowledged. 1'b1: Low power request is not acknowledged.
0	RO	0x1	st_csysreq_ddrc DDRCTL core low power request status 1'b0: Low power request. 1'b1: No low power request.

DDR_GRF_CHB_STATUS17

Address: Operational Base(0x26012000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RO	0x40	st_wr_credit_cnt DDRCTL wr credit count
15	RO	0x0	reserved
14:8	RO	0x1f	st_hpr_credit_cnt DDRCTL hpr credit count
7	RO	0x0	reserved
6:0	RO	0x21	st_lpr_credit_cnt DDRCTL lpr credit count

DDR_GRF_CHB_STATUS19

Address: Operational Base(0x26012000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RO	0x0	st_derate_temp_limit_intr_fault This signal is the derate temperature limit fault. This is a version of derate_temp_limit_intr, which can not be disabled or forced via a register. It is a 2-bit antivalent signal with encoding as follows: 2'b01: No Fault 2'b10: Fault Detected
7:6	RO	0x0	reserved
5:0	RO	0x00	st_hif_refresh_req_bank This signal indicates the next bank that is refreshed; for multi-rank configurations, the bank number is reported independently for each rank, and the information for all ranks is concatenated to form this signal.

DDR_GRF_CHA_PHY_CON0

Address: Operational Base(0x26012000) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	ddrphy_pclk_cg_en DDRPHY APB pclk clock gate enable 1'b0: Disable 1'b1: Enable
13	RW	0x0	ctrl_clkm_cg_en DDRPHY master DLL clock gating enable. 1'b0: DDRPHY master DLL clock gating is disabled. 1'b1: DDRPHY master DLL clock gating is enabled.

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Bit	Attr	Reset Value	Description
12:11	RW	0x0	dfi_phymstr_type Value of dfi_phymstr_type This signal is the DFI PHY master type for the DFIn channel. This signal indicates which of the four types of PHY master interface times the dfi_phymstr_req signal is requesting. 2'b00: tphymstr_type0 2'b01: tphymstr_type1 2'b10: tphymstr_type2 2'b11: tphymstr_type3
10	RW	0x1	dfi_phymstr_state_sel Value of dfi_phymastr_state_sel This signal is the DFI PHY master state select for the DFI interface. This signal indicates the state requested by the DDRPHY. 1'b0: IDLE 1'b1: Self-Refresh Note: This input port is not used internally as the DDRCTL puts all ranks of SDRAM into Self Refresh in response to dfi_phymstr_req.
9:8	RW	0x0	dfi_phymstr_cs_state Value of dfi_phymstr_cs_state This signal is the DFI PHY master CS state for the DFI interface. This signal indicates the state of the DRAM when the DDRPHY becomes the master. 1'b0: The DDRPHY specifies the required state, using the dfi_phymstr_state_sel signal. 1'b1: The DDRPHY does not specify the state. This signal is valid only when dfi_phymstr_req is asserted. Each memory rank uses one bit. Note: This input port is not used internally as the DDRCTL puts all ranks of SDRAM into Self Refresh in response to dfi_phymstr_req.
7	RW	0x0	dfi_init_start Value of dfi_init_start
6	RW	0x0	dfi_init_start_sel DDRPHY dfi_init_start select 1'b0: DDRPHY dfi_init_start is driven by DDRCTL 1'b1: DDRPHY dfi_init_start is driven by DDR_GRF
5	RW	0x0	dfi_init_complete Value of dfi_init_complete
4	RW	0x0	dfi_init_complete_sel DDRCTL dfi_init_complete select 1'b0: DDRCTL dfi_init_complete is driven by DDRPHY 1'b1: DDRCTL dfi_init_complete is driven by DDR_GRF
3	RW	0x0	ddrphy2xclkgate_enable Root clock gating control of DDRPHY. It controls clock gating of clk_phy2x. Set this pin to low to enable clock gating for clk_phy2x. For normal operation and DDRPHY test mode, this pin should be high. Root clock gating should be enabled while dfi_dram_clk_disable=1'b1.

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Bit	Attr	Reset Value	Description
2	RW	0x0	i_g_drcg_en Dynamic regional clock gating control for DDRPHY. DRCG refers to clock gating controlled by pcl_pd field in DDRPHY_LP_CON0 register. 1'b0: DRCG will be controlled by pcl_pd field in DDRPHY_LP_CON0 1'b1: DRCG is enabled regardless of pcl_pd field
1:0	RW	0x0	dvfs_clk_mode DVFS mode select for clock mode between DFI clock and DFI PHY clock. This signal controls which DVFS register sets will be used after frequency change. 2'b00: Normal mode 2'b01: DVFS0 mode 2'b10: DVFS1 mode

DDR_GRF_CHB_PHY_CON0

Address: Operational Base(0x26012000) + offset (0x0534)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	ddrphy_pclk_cg_en DDRPHY APB pclk clock gate enable 1'b0: Disable 1'b1: Enable
13	RW	0x0	ctrl_clkm_cg_en DDRPHY master DLL clock gating enable. 1'b0: DDRPHY master DLL clock gating is disabled. 1'b1: DDRPHY master DLL clock gating is enabled.
12:11	RW	0x0	dfi_phymstr_type Value of dfi_phymstr_type This signal is the DFI PHY master type for the DFIn channel. This signal indicates which of the four types of PHY master interface times the dfi_phymstr_req signal is requesting. 2'b00: tphymstr_type0 2'b01: tphymstr_type1 2'b10: tphymstr_type2 2'b11: tphymstr_type3
10	RW	0x1	dfi_phymstr_state_sel Value of dfi_phymastr_state_sel This signal is the DFI PHY master state select for the DFI interface. This signal indicates the state requested by the DDRPHY. 1'b0: IDLE 1'b1: Self-Refresh Note: This input port is not used internally as the DDRCTL puts all ranks of SDRAM into Self Refresh in response to dfi_phymstr_req.

Bit	Attr	Reset Value	Description
9:8	RW	0x0	dfi_phymstr_cs_state Value of dfi_phymstr_cs_state This signal is the DFI PHY master CS state for the DFI interface. This signal indicates the state of the DRAM when the DDRPHY becomes the master. 1'b0: The DDRPHY specifies the required state, using the dfi_phymstr_state_sel signal. 1'b1: The DDRPHY does not specify the state. This signal is valid only when dfi_phymstr_req is asserted. Each memory rank uses one bit. Note: This input port is not used internally as the DDRCTL puts all ranks of SDRAM into Self Refresh in response to dfi_phymstr_req.
7	RW	0x0	dfi_init_start Value of dfi_init_start
6	RW	0x0	dfi_init_start_sel DDRPHY dfi_init_start select 1'b0: DDRPHY dfi_init_start is driven by DDRCTL 1'b1: DDRPHY dfi_init_start is driven by DDR_GRF
5	RW	0x0	dfi_init_complete Value of dfi_init_complete
4	RW	0x0	dfi_init_complete_sel DDRCTL dfi_init_complete select 1'b0: DDRCTL dfi_init_complete is driven by DDRPHY 1'b1: DDRCTL dfi_init_complete is driven by DDR_GRF
3	RW	0x0	ddrphy2xclkgate_enable Root clock gating control of DDRPHY. It controls clock gating of clk_phy2x. Set this pin to low to enable clock gating for clk_phy2x. For normal operation and DDRPHY test mode, this pin should be high. Root clock gating should be enabled while dfi_dram_clk_disable=1'b1.
2	RW	0x0	i_g_drcg_en Dynamic regional clock gating control for DDRPHY. DRCG refers to clock gating controlled by pcl_pd field in DDRPHY_LP_CON0 register. 1'b0: DRCG will be controlled by pcl_pd field in DDRPHY_LP_CON0 1'b1: DRCG is enabled regardless of pcl_pd field
1:0	RW	0x0	dvfs_clk_mode DVFS mode select for clock mode between DFI clock and DFI PHY clock. This signal controls which DVFS register sets will be used after frequency change. 2'b00: Normal mode 2'b01: DVFS0 mode 2'b10: DVFS1 mode

DDR_GRF_CHA_PHY_STATUS0

Address: Operational Base(0x26012000) + offset (0x0538)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	st_dfi_init_complete dfi_init_complete status 1'b0: DFI init not complete 1'b1: DFI init complete

Bit	Attr	Reset Value	Description
3	RO	0x0	st_dfi_init_start dfi_init_start status 1'b0: DFI init not start 1'b1: DFI init start
2	RO	0x0	st_ddrphy2xclkgate_enout Status of ddrphy2xclkgate_enout signal. This is a feed-through signal of ddrphy2xclkgate_enable. This signal can be monitored to get the status of ddrphy2xclkgate_enable signal.
1	RO	0x0	st_dfi_phymstr_active DDRPHY phymstr_active status
0	RO	0x0	st_dfi_error DDRPHY dfi error status Indicates that the DDRPHY has detected an error condition such as read FIFO pointer error, conflict DLL update and wrdata and conflict DLL update and rddata.

DDR_GRF_CHB_PHY_STATUS0

Address: Operational Base(0x26012000) + offset (0x053C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	st_dfi_init_complete dfi_init_complete status 1'b0: DFI init not complete 1'b1: DFI init complete
3	RO	0x0	st_dfi_init_start dfi_init_start status 1'b0: DFI init not start 1'b1: DFI init start
2	RO	0x0	st_ddrphy2xclkgate_enout Status of ddrphy2xclkgate_enout signal. This is a feed-through signal of ddrphy2xclkgate_enable. This signal can be monitored to get the status of ddrphy2xclkgate_enable signal.
1	RO	0x0	st_dfi_phymstr_active DDRPHY phymstr_active status
0	RO	0x0	st_dfi_error DDRPHY dfi error status Indicates that the DDRPHY has detected an error condition such as read FIFO pointer error, conflict DLL update and wrdata and conflict DLL update and rddata.

DDR_GRF_COMMON_CON0

Address: Operational Base(0x26012000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x110010	mem_cfg_hsdprf_ddrctl HSDPRF type memory configuration of DDRCTL Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB

DDR_GRF_COMMON_CON1

Address: Operational Base(0x26012000) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:0	RW	0x14101410	mem_cfg_hsdprf_ddrmcu Memory configuration of DDR_MCU. There are 2 kinds of memories inside DDR_MCU. The following is for HDSPRA memory type. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA The following is for HDSPRF memory type. Bit[16]: TEST1 Bit[17]: TEST_RNM Bit[20:18]: RM Bit[21]: WMD Bit[23]: LS Bit[27:26]: WPULSE Bit[29:28]: RA

DDR_GRF_COMMON_CON2

Address: Operational Base(0x26012000) + offset (0x0548)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	grf_con_ddr_mcu_stcalib Bit 0-23 provides an integer value to compute a 10ms delay from the reference clock is not implemented. Bit 24 1'b0: If the system timer clock or SCLK, can guarantee an exact multiple of 10ms. 1'b1: System timer clock of SCLK can not guarantee an exact multiple of 10ms. Bit 25 indicate no alternative reference clock source has been integrated. 1 means STCLKEN has been tie off.

DDR_GRF_COMMON_CON3

Address: Operational Base(0x26012000) + offset (0x054C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_int_trigger Write 1'b1 will trigger an interrupt
14:11	RO	0x0	reserved
10	RW	0x0	grf_mcu_ddrcfg_mode_sel 1'b0: Parallel mode. DDR_MCU write the slave APB interface of two DDR channels at the same time by sending only one APB write operation to the same location. It's only effective for DDRCTL and DDRPHY. 1'b1: Normal mode.
9	RW	0x0	grf_con_wdt_pause_en DDR_WDT pause enable. Used to freeze the watchdog counter during pause mode. High active.

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Bit	Attr	Reset Value	Description
8	RW	0x0	grf_con_ddrmcu_tcm_mem_cg_en DDR_MCU TCM clock gate enable 1'b0: Disable 1'b1: Enable
7:0	RW	0x00	grf_con_ddr_mcu_irqlatency Irqlatency specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface.

DDR_GRF_COMMON_CON4

Address: Operational Base(0x26012000) + offset (0x0550)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	grf_external_trigger_en 1'b0: Two DDRMON channels will start work controlled by their own registers. 1'b1: Two DDRMON channels will start work at the same time controlled by grf_external_trigger_en. Before setting grf_external_trigger_en to 1'b1, the two DDRMON channels should be fully configured and waitting for grf_external_trigger_en to trigger to start work.
7:3	RO	0x00	reserved
2	RW	0x0	grf_con_probe_2vop_suspend_en If enabled, the main suspend state of vop interconnect probe will be controlled by DDRMON module.
1	RW	0x0	grf_con_probe_2core_suspend_en If enabled, the main suspend state of core interconnect probe will be controlled by DDRMON module.
0	RW	0x0	grf_con_probe_2center_suspend_en If enabled, the main suspend state of center interconnect probe will be controlled by DDRMON module.

DDR_GRF_COMMON_CON5

Address: Operational Base(0x26012000) + offset (0x0554)

Bit	Attr	Reset Value	Description
31	RW	0x0	wr_credit_en Enable the write credits function to generate a control signal to control shapping function of RKNN interconnect. 1'b0: Disable 1'b1: Enable
30:24	RW	0x00	wr_credit_high_thd If the WR credits of DDRCTL is lower than wr_credit_low_thd, a control signal will be generated and set high to control shapping function of RKNN interconnect. If the WR credits is higher than wr_credit_high_thd, this generated signal will be set low.There are 2 control signals generated, one for each DDR channel. The two generated signals will be ORed together and connected to RKNN interconnect.
23	RW	0x0	vop_axi1_wr_credit_en If enabled, the vop_axi1_rd_urgency signal comming from VOP will be Ored together with signal generated by WR credits.

Bit	Attr	Reset Value	Description
22:16	RW	0x00	wr_credit_low_thd If the WR credits of DDRCTL is lower than wr_credit_low_thd, a control signal will be generated and set high to control shapping function of RKNN interconnect. If the WR credits is higher than wr_credit_high_thd, this generated signal will be set low.There are 2 control signals generated, one for each DDR channel. The two generated signals will be ORed together and connected to RKNN interconnect.
15	RW	0x0	lpr_credit_en Enable the LPR credits function to generate a control signal to control shapping function of RKNN interconnect. 1'b0: Disable 1'b1: Enable
14:8	RW	0x00	lpr_credit_high_thd If the LPR credits of DDRCTL is lower than lpr_credit_low_thd, a control signal will be generated and set high to control shapping function of RKNN interconnect. If the LPR credits is higher than lpr_credit_high_thd, this generated signal will be set low.There are 2 control signals generated, one for each DDR channel. The two generated signals will be ORed together and connected to RKNN interconnect.
7	RW	0x0	vop_axi1_lpr_credit_en If enabled, the vop_axi1_rd_urgency signal comming from VOP will be Ored together with signal generated by LPR credits.
6:0	RW	0x00	lpr_credit_low_thd If the LPR credits of DDRCTL is lower than lpr_credit_low_thd, a control signal will be generated and set high to control shapping function of RKNN interconnect. If the LPR credits is higher than lpr_credit_high_thd, this generated signal will be set low.There are 2 control signals generated, one for each DDR channel. The two generated signals will be ORed together and connected to RKNN interconnect.

DDR_GRF_STATUS0

Address: Operational Base(0x26012000) + offset (0x0580)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	st_ddr_timer1_en DDR_TIMER channel 1 enable status.
0	RO	0x0	st_ddr_timer0_en DDR_TIMER channel 0 enable status.

5.10 CENTER_GRF Register Description

5.10.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CENTER_GRF_SOC_CON0	0x0000	W	0x00008010	Center Control Register 0
CENTER_GRF_SOC_CON1	0x0004	W	0x00001410	Center Control Register 1
CENTER_GRF_SOC_CON2	0x0008	W	0x00008010	Center Control Register 2
CENTER_GRF_SOC_CON4	0x0010	W	0x00000000	Center Control Register 4
CENTER_GRF_SOC_CON5	0x0014	W	0x00000000	Center Control Register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.10.2 Detail Registers Description

CENTER_GRF_SOC_CON0

Address: Operational Base(0x26014000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x08010	mem_cfg_uhdpdprf_dma2ddr UHDPDPRF type memory configuration of DMA2DDR module. bit[0]: TEST1 bit[1]: TEST_RNM bit[4:2]: RM bit[5]: WMDA bit[7]: LS bit[16]: TESTRWM

CENTER_GRF_SOC_CON1

Address: Operational Base(0x26014000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	mem_cfg_hdspra_shrm HDSPRA type memory configuration of system sram. bit[0]: TEST1 bit[1]: TEST_RNM bit[4:2]: RM bit[5]: WMD bit[7]: LS bit[11:10]: WPULSE bit[13:12]: RA

CENTER_GRF_SOC_CON2

Address: Operational Base(0x26014000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x08010	mem_cfg_uhdpdprf_interconnect UHDPDPRF type memory configuration of center interconnect. bit[0]: TEST1 bit[1]: TEST_RNM bit[4:2]: RM bit[5]: WMDA bit[7]: LS bit[16]: TESTRWM

CENTER_GRF_SOC_CON4

Address: Operational Base(0x26014000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	grf_interconnect_mem_cg_en Memory clock gate enable of center interconnect. 1'b0: Disable 1'b1: Enable
0	RW	0x0	grf_dma2ddr_mem_cg_en Memory clock gate enable of DMA2DDR. 1'b0: Disable 1'b1: Enable

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CENTER_GRF_SOC_CON5

Address: Operational Base(0x26014000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x00	grf_con_size DDR size configuration of interconnect. Please keep default value and not modify it.

5.11 GPU_GRF Register Description

5.11.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPU_GRF_GPU_CON0	0x0020	W	0x00000000	GPU various memory configuration high part register
GPU_GRF_GPU_MEM_CFG_HDSPRF	0x003C	W	0x00001410	GPU HDSPRF memory configuration register
GPU_GRF_GPU_MEM_CFG_HSSPRA	0x0040	W	0x00000010	GPU HSSPRA memory configuration register
GPU_GRF_GPU_MEM_CFG_UHDPDPRF_LOW	0x0048	W	0x00008010	GPU UHDPDPRF memory configuration low part register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.11.2 Detail Registers Description

GPU_GRF_GPU_CON0

Address: Operational Base(0x26016000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:13	RW	0x0	gpu_striping_granule Memory striping control. This signal must be set during the GPU reset and remain static during operation. see "Chapter GPU" for details.
12:10	RW	0x0	mem_cfg_uhdpdprf_high UHDPDPRF memory configuration high bit[18:16]. Bit[0]: TESTRWM Other bits: Reserved
9:0	RO	0x000	reserved

GPU_GRF_GPU_MEM_CFG_HDSPRF

Address: Operational Base(0x26016000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.

Bit	Attr	Reset Value	Description
15:0	RW	0x1410	mem_cfg_hdsprf HDSPRF memory configuration. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

GPU_GRF_GPU_MEM_CFG_HSSPRA

Address: Operational Base(0x26016000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:0	RW	0x0010	mem_cfg_hsspra HSSPRA memory configuration. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

GPU_GRF_GPU_MEM_CFG_UHDPDPRF_LOW

Address: Operational Base(0x26016000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:0	RW	0x8010	mem_cfg_uhdpdprf_low UHDPDPRF memory configuration high bit[15:0]. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Other bits: Reserved

5.12 NPU_GRF Register Description

5.12.1 Registers Summary

Name	Offset	Size	Reset Value	Description
NPU_GRF_MEM_CON0	0x0008	W	0x00001410	NPU memory configuration for HDSPRF
NPU_GRF_MEM_CON1	0x000C	W	0x00110010	NPU memory configuration for HSDPRF

Name	Offset	Size	Reset Value	Description
NPU_GRF_MEM_CON2	0x0010	W	0x00008010	NPU memory configuration for UHDDPRF
NPU_GRF_MEMGATE_CON0	0x0014	W	0x00000000	RKNN memory gate control register
NPU_GRF_MEMGATE_CON1	0x0018	W	0x00000000	PD_NPU memory gate control register
NPU_GRF_RKNNST	0x001C	W	0x00000000	Active state for RKNN
NPU_GRF_NSP_SLV_ADDR	0x0020	W	0x00000000	NSP slave address register
NPU_GRF_NPUTOP_CON	0x0028	W	0x00000000	PD NPU control register
NPU_GRF_STCALIB	0x002C	W	0x00000000	NPU_MCU Systick timer counter register
NPU_GRF_START_ADDR	0x0030	W	0x20000000000	NPU_MCU cache start address register
NPU_GRF_END_ADDR	0x0034	W	0x2FFFF000000	NPU_MCU cache end address register
NPU_GRF_NPUTOP_ST	0x0038	W	0x00000000	PD_NPU status register
NPU_GRF_CACHE_MAINTAIN	0x0058	W	0x00000003	NPU_MCU cache maintain register
NPU_GRF_RV_BASE_ADDR	0x005C	W	0x00000000	RKNN RV core base address register
NPU_GRF_URGENT_CON0	0x006C	W	0x000000FF	BIU urgent control register 0
NPU_GRF_URGENT_CON1	0x0070	W	0x000000FF	BIU urgent control register 1
NPU_GRF_URGENT_CON2	0x0074	W	0x000000FF	BIU urgent control register 2
NPU_GRF_URGENT_CON3	0x0078	W	0x000000FF	BIU urgent control register 3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.12.2 Detail Registers Description

NPU_GRF_MEM_CON0

Address: Operational Base(0x26018000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	npu_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_NPU. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

NPU_GRF_MEM_CON1

Address: Operational Base(0x26018000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:0	RW	0x110010	npu_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_NPU. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

NPU_GRF_MEM_CON2

Address: Operational Base(0x26018000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x08010	npu_mem_cfg_uhddprf Interface configuration for UHDPDPPRF type memory in PD_NPU. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

NPU_GRF_MEMGATE_CON0

Address: Operational Base(0x26018000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_mem_gate Clock gate control for RKNN cbuf memory. Bit[15:0]: Clock gate enable for cbuf bank 0-15. Bit[31]: Clock gate enable for RV core. Other: reserved. 1'b0: Disable memory auto gating. 1'b1: Enable memory auto gating.

NPU_GRF_MEMGATE_CON1

Address: Operational Base(0x26018000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	cache_mem_gate Clock gate control for NPU_MCU cache memory. 1'b0: Disable memory auto gating. 1'b1: Enable memory auto gating.
1	RW	0x0	npu_mcu_mem_gate Clock gate control for NPU_MCU memory. 1'b0: Disable memory auto gating. 1'b1: Enable memory auto gating.

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Bit	Attr	Reset Value	Description
0	RW	0x0	nsp_mem_gate Clock gate control for RKNN nsp memory. 1'b0: Disable memory auto gating. 1'b1: Enable memory auto gating.

NPU_GRF_RKNNST

Address: Operational Base(0x26018000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	dap_swactive DAPLITE swactive for RKNN state, Active high.
1	RO	0x0	core1_work_on RKNN core1 work state, Active high.
0	RO	0x0	core0_work_on RKNN core0 work state, Active high.

NPU_GRF_NSP_SLV_ADDR

Address: Operational Base(0x26018000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nsp_slv_addr Slave address for nsp.

NPU_GRF_NPUTOP_CON

Address: Operational Base(0x26018000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	npum0_dclk_cm0s_en Enable dclk for NPU_MCU, active high.
13	RW	0x0	npum0_hclk_cm0s_en Enable hclk for NPU_MCU, active high.
12	RW	0x0	npum0_sclk_cm0s_en Enable sclk for NPU_MCU, active high.
11:10	RW	0x0	cache_slv_memattr Transaction memory attribute When support mpu mode, the cache controller will cache the request if both the hprot[3] and memattr[0] is high on AHB slave bus, or will bypass the request.
9	RW	0x0	mcu_cache_fluse_req NPU_MCU cache memory flush request.
8:1	RW	0x00	mcu_irqlatency NPU_MCU supports zero jitter interrupt latency for zero wait-state memory. IRQLATENCY specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface.
0	RW	0x0	npu_wdt_pause NPU_WDT pause control. When this signal is high, WDT will stop the counter.

NPU_GRF_STCALIB

Address: Operational Base(0x26018000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	mcu_stcalib Systick timer counter. Stcalib[25]: Indicates that no alternative reference clock source has been integrated. Stcalib[24]: Tie this LOW if the system timer clock, the external reference clock, or SCLK as indicated by STCALIB[25], can guarantee an exact multiple of 10ms. Stcalib[23:0]: Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV.

NPU_GRF_START_ADDR

Address: Operational Base(0x26018000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:12	RW	0x20000000	cache_peri_addr_start NPU_MCU cache peripheral start address. Higher [31:12] bits.
11:0	RO	0x000	reserved

NPU_GRF_END_ADDR

Address: Operational Base(0x26018000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RW	0x2ffff000	cache_peri_addr_start NPU_MCU cache peripheral end address. Higher [31:12] bits.
11:0	RO	0x000	reserved

NPU_GRF_NPUTOP_ST

Address: Operational Base(0x26018000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	mcu_deepsleep Active only when SLEEPING is HIGH. Indicates that the SLEEPDEEP bit in the NVIC is set to 1.
6	RO	0x0	mcu_sleep Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV.
5	RO	0x0	mcu_lockup Indicates that the processor is in the architect lock-up state, as the result of an unrecoverable exception. See the ARMv6-M Architecture Reference Manual for more information.
4	RO	0x0	mcu_halted Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state.
3	RO	0x0	mcu_cache_flush_ack NPU_MCU cache memory flush acknowledge.
2	RO	0x0	mcu_txev A single SCLK cycle HIGH level is generated on this output every time an SEV instruction is executed on the MCU processor.
1	RO	0x0	npu_timer1_en NPU_TIMER channel 1 clock enable state. If this signal is high, timer clock is enable.
0	RO	0x0	npu_timer0_en NPU_TIMER channel 0 clock enable state. If this signal is high, timer clock is enable.

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NPU_GRF_CACHE_MAINTAIN

Address: Operational Base(0x26018000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	cache_maintain_sram_en Maintain address offset of sram space enable. 1'b1: Enable. 1'b0: Disable.
0	RW	0x1	cache_maintain_code_en Maintain address offset of code space enable. 1'b1: Enable. 1'b0: Disable.

NPU_GRF_RV_BASE_ADDR

Address: Operational Base(0x26018000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rvcore_base_addr RKNN RV core base address.

NPU_GRF_URGENT_CON0

Address: Operational Base(0x26018000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x0000	reserved
8	RW	0x0	npu_m0_ro_urgent_sel Select the urgent function, active high. When this bit set to 1'b1 and ddr can almost full, npu_m0_ro_urgent will be used. Otherwise, use internal shaping.
7:0	RW	0xff	npu_m0_ro_urgent Maximum number of packets sent by BIU.

NPU_GRF_URGENT_CON1

Address: Operational Base(0x26018000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x0000	reserved
8	RW	0x0	npu_m1_ro_urgent_sel Select the urgent function, active high. When this bit set to 1'b1 and ddr can almost full, npu_m0_ro_urgent will be used. Otherwise, use internal shaping.
7:0	RW	0xff	npu_m1_ro_urgent Maximum number of packets sent by BIU.

NPU_GRF_URGENT_CON2

Address: Operational Base(0x26018000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x0000	reserved
8	RW	0x0	npu_m0_urgent_sel Select the urgent function, active high. When this bit set to 1'b1 and ddr can almost full, npu_m0_ro_urgent will be used. Otherwise, use internal shaping.
7:0	RW	0xff	npu_m0_urgent Maximum number of packets sent by BIU.

NPU_GRF_URGENT_CON3

Address: Operational Base(0x26018000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x0000	reserved
8	RW	0x0	npu_m1_urgent_sel Select the urgent function, active high. When this bit set to 1'b1 and ddr can almost full, npu_m0_ro_urgent will be used. Otherwise, use internal shaping.
7:0	RW	0xff	npu_m1_urgent Maximum number of packets sent by BIU.

5.13 PHP_GRF Register Description

5.13.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PHP_GRF_MMUBP_ST	0x0000	W	0x00000000	MMU bypass status register
PHP_GRF_MMUBP_CON0	0x0004	W	0x00000000	MMU bypass address control register
PHP_GRF_MMU0_CON	0x0008	W	0x00000001	MMU0 control register
PHP_GRF_MMU1_CON	0x000C	W	0x00000001	MMU1 control register
PHP_GRF_MEM_CON0	0x0010	W	0x00001410	PD_PHP memory configuration for HDSPRF
PHP_GRF_MEM_CON1	0x0014	W	0x00110010	PD_PHP memory configuration for HSDPRF
PHP_GRF_MEM_CON2	0x0018	W	0x00008010	PD_PHP memory configuration for UHDDPRF
PHP_GRF_SATA0_CON	0x001C	W	0x00000000	SATA0 control register
PHP_GRF_SATA1_CON	0x0020	W	0x00000000	SATA1 control register
PHP_GRF_USB3OTG1_STATUS_LAT0	0x0024	W	0x00000000	USB3OTG1 status register 0
PHP_GRF_USB3OTG1_STATUS_LAT1	0x0028	W	0x00000000	USB3OTG1 status register 1
PHP_GRF_USB3OTG1_STATUS_CB	0x002C	W	0x000007E8	USB3OTG1 status register 2
PHP_GRF_USB3OTG1_STATUS	0x0030	W	0x00000000	USB3OTG1 status register 3

Name	Offset	Size	Reset Value	Description
PHP_GRF_USB3OTG1_CON0	0x0034	W	0x00002000	USB3OTG1 control register 0
PHP_GRF_USB3OTG1_CON1	0x0038	W	0x00001100	USB3OTG1 control register 1
PHP_GRF_PCIEPIPE_CON0	0x0048	W	0x00000000	PCIe pipe control register 0
PHP_GRF_PCIE_CLKREQ_ST	0x0054	W	0x00000000	PCIe clkreq status register
PHP_GRF_MMU0_ST0	0x005C	W	0x00000700	MMU0 status register 0
PHP_GRF_MMU0_ST1	0x0060	W	0x00000000	MMU0 status register 1
PHP_GRF_MMU0_ST2	0x0064	W	0x00000000	MMU0 status register 2
PHP_GRF_MMU0_ST3	0x0068	W	0x00000000	MMU0 status register 3
PHP_GRF_MMU0_ST4	0x006C	W	0x00000000	MMU0 status register 4
PHP_GRF_MMU1_ST0	0x0070	W	0x00000700	MMU1 status register 0
PHP_GRF_MMU1_ST1	0x0074	W	0x00000000	MMU1 status register 1
PHP_GRF_MMU1_ST2	0x0078	W	0x00000000	MMU1 status register 2
PHP_GRF_MMU1_ST3	0x007C	W	0x00000000	MMU1 status register 3
PHP_GRF_MMU1_ST4	0x0080	W	0x00000000	MMU1 status register 4

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.13.2 Detail Registers Description

PHP_GRF_MMUBP_ST

Address: Operational Base(0x26020000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	mmu1_idle MMU1 idle state. 1'b0: Not idle state 1'b1: Idle state
4	RO	0x0	mmu0_idle MMU0 idle state. 1'b0: Not idle state 1'b1: Idle state
3:0	RO	0x0	reserved

PHP_GRF_MMUBP_CON0

Address: Operational Base(0x26020000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	usb3otg1_araddr_h Software control usb3otg1 araddr[39:32].
7:0	RW	0x00	usb3otg1_awaddr_h Software control usb3otg1 awaddr[39:32].

PHP_GRF_MMU0_CON

Address: Operational Base(0x26020000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved
4	RW	0x0	dbg_err_clr 1'b1: Enable to Clear the MMU debug counters 0,1,2,3 1'b0: Disable it
3	RW	0x0	mem_gate_en 1'b1: Enable to auto gating the MMU TLB memory 1'b0: Disable it
2	RW	0x0	mon_clr 1'b1: Enable to clear the axi monitor counter 1'b0: Disable it
1	RW	0x0	bypass_grf 1'b1: Enable to bypass it when the MMU is idle state 1'b0: Disable
0	RW	0x1	bypass_force 1'b1: Enable to force MMU bypass 1'b0: Disable

PHP_GRF_MMU1_CON

Address: Operational Base(0x26020000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	dbg_err_clr 1'b1: Enable to Clear the MMU debug counters 0,1,2,3 1'b0: Disable it
3	RW	0x0	mem_gate_en 1'b1: Enable to auto gating the MMU TLB memory 1'b0: Disable it
2	RW	0x0	mon_clr 1'b1: Enable to clear the axi monitor counter 1'b0: Disable it
1	RW	0x0	bypass_grf 1'b1: Enable to bypass it when the MMU is idle state 1'b0: Disable
0	RW	0x1	bypass_force 1'b1: Enable to force MMU bypass 1'b0: Disable

PHP_GRF_MEM_CON0

Address: Operational Base(0x26020000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	php_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_PHP. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

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PHP_GRF_MEM_CON1

Address: Operational Base(0x26020000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x110010	php_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_PHP. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

PHP_GRF_MEM_CON2

Address: Operational Base(0x26020000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x08010	php_mem_cfg_uhdpdprf Interface configuration for UHDPDPPRF type memory in PD_PHP. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

PHP_GRF_SATA0_CON

Address: Operational Base(0x26020000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	sata0_pd_sel1 If this bit set to 1'b0, remap powerdown form 4'd2 to 4'd7. If this bit set to 1'b1, remap powerdown form 4'd2 to 4'd5.
3	RW	0x0	sata0_pd_sel0 If this bit set to 1'b0, remap powerdown form 4'd1 to 4'd3. If this bit set to 1'b1, not remap powerdown form 4'd1.
2	RW	0x0	sata0_phy_rxerr SATA0 phy_rx_err input control, before using set this bit to 1'b0.
1:0	RW	0x0	sata0_phy_spdmode SATA0 phy_spdmode input control. 2'b00: 1.5Gb/s 2'b01: 3.0Gb/s 2'b10: 6.0Gb/s 2'b11: Reserved This should be set before using SATA.

PHP_GRF_SATA1_CON

Address: Operational Base(0x26020000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	sata1_pd_sel1 If this bit set to 1'b0, remap powerdown form 4'd2 to 4'd7. If this bit set to 1'b1, remap powerdown form 4'd2 to 4'd5.
3	RW	0x0	sata1_pd_sel0 If this bit set to 1'b0, remap powerdown form 4'd1 to 4'd3. If this bit set to 1'b1, not remap powerdown form 4'd1.
2	RW	0x0	sata1_phy_rxerr SATA1 phy_rx_err input control, before using set this bit to 1'b0.
1:0	RW	0x0	sata1_phy_spdmode SATA1 phy_spdmode input control. 2'b00: 1.5Gb/s 2'b01: 3.0Gb/s 2'b10: 6.0Gb/s 2'b11: Reserved This should be set before using SATA.

PHP_GRF_USB3OTG1_STATUS_LAT0

Address: Operational Base(0x26020000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	usb3otg_logic_analyzer_trace0 Usb3otg_logic_analyzer_trace[31:0] bit status. Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility.

PHP_GRF_USB3OTG1_STATUS_LAT1

Address: Operational Base(0x26020000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	usb3otg_logic_analyzer_trace1 Usb3otg_logic_analyzer_trace[63:32] bit status. Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility.

PHP_GRF_USB3OTG1_STATUS_CB

Address: Operational Base(0x26020000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x7e8	usb3otg_host_current_belt[11:0] Usb3otg_host_current_belt[11:0] bit status. Current BELT Value. This signal indicates the minimum value of all received BELT values and the BELT that is set by the Set LTV command. This signal is valid only in Host mode.

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PHP_GRF_USB3OTG1_STATUS

Address: Operational Base(0x26020000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	usb3otg1_pme_generation PME Generation. This signal is used to generate a PME# (Power Management Event). When the Run/Stop bit of the USB Command Register is cleared during USB suspend mode, the core cannot generate an event and cannot assert a regular interrupt. In this case, the core asserts a pme_generation signal to report any wakeup condition if pme_en is high. If the system does not support PCI-like PME interface, then it must not clear the Run/Stop bit during USB suspend mode. In this case, the core generates an event and asserts an interrupt when there is any wakeup event.
0	RO	0x0	usb3otg1_host_sys_err Host System Error. This signal indicates that a Host System Error has occurred as reflected in the USBSTS.HSE field. This signal is asserted only if the USBCMD.HSEE field is set to '1'. It can occur when the host controller encounters an 'Error' response in the AHB, the AXI, or the Native Master Bus. When the USBSTS.HSE field is cleared by software, this signal is deasserted unless the master continues to assert its bus error output. The typical software response to an HSE is to reset the core. For more details, refer to section 4.10.2.6 of the xHCI 1.0 specification.

PHP_GRF_USB3OTG1_CON0

Address: Operational Base(0x26020000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb3otg1_host_u2_port_disable USB2.0 Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state.
14	RW	0x0	usb3otg1_host_port_power_control_present This indicates whether the host controller implementation includes port power control. 1'b0: Indicates that the port does not have port power switches 1'b1: Indicates that the port has port power switches

Bit	Attr	Reset Value	Description
13:8	RW	0x20	usb3otg1_fladj_30mhz_reg HS Jitter Adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 's duration. With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933ns. You must program the value in terms of high speed bit times in a 30 MHz cycle. The default value that must be driven is 32 (assuming 30 MHz perfect clock). Fladj_30mhz_reg connects to the FLADJ register defined in the xHCI spec in the PCI configuration space. Each count is equal to 16 high speed bit times. By default, when this register is set to 32, it gives a 125us interval. Now, based the clock accuracy you can decrement the count or increment the count to get the 125 us uSOF window. For non-PCI systems, it is recommended that this strap is connected to a register that can be controlled by software. This strap is used in device mode also. If device only mode is implemented, it is recommended to tie this input to 'd32.
7:6	RW	0x0	usb3otg1_hub_port_perm_attach Indicates if the device attached to a downstream port is permanently attached or not. 1'b0: Not permanently attached 1'b1: Permanently attached Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port
5:4	RW	0x0	usb3otg1_hub_port_overcurrent This is the per port Overcurrent indication of the root-hub ports: 1'b0: No Overcurrent 1'b1: Overcurrent Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port
3:0	RW	0x0	usb3otg1_bus_filter_bypass It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core. The function of each bit is: bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports In non-OTG Host-only mode, internal bus filters are not needed. Values: 1'b0: Bus filter(s) enabled 1'b1: Bus filter(s) disabled (bypassed)

PHP_GRF_USB3OTG1_CON1

Address: Operational Base(0x26020000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x1	usb3otg1_host_num_u3_port xHCI usb3 port number, default as 1.
11:8	RW	0x1	usb3otg1_host_num_u2_port xHCI host USB2 Port number, default as 1.

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Bit	Attr	Reset Value	Description
7	RW	0x0	usb3otg1_pipe_clk_sel usb3otg1_pipe3_rx_pclk/tx_pclk input source clk select. 1'b0: Select clk_usb3otg1_pipe for source clock 1'b1: Select clk_usb3otg1_utmi for source clock
6	RW	0x0	usb3otg1_mem_gate_en 1'b1: Enable memory auto clock gating 1'b0: Disable memory auto clock gating
5	RW	0x0	usb3otg1_host_legacy_smi_bar Use this register to support SMI on BAR defined in xHCI spec. Software must set this register, then clear this register to indicate Base Address Register written.
4	RW	0x0	usb3otg1_host_legacy_smi_pci_cmd Use this register to support SMI on PCI Command defined in xHCI spec. Software must set this register, then clear this register to indicate PCI command register written.
3:2	RW	0x0	usb3otg1_phystatus_con Grf controll usb pipe phystatus. 2'b00: Select phystatus form phy 2'b10: Set phystatus to 0 Others: Reserved
1	RW	0x0	usb3otg1_pme_en Enable signal for the pme_generation. Enable the core to assert pme_generation. If not use set this bit to 1'b1.
0	RW	0x0	usb3otg1_host_u3_port_disable USB 3.0 SS Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled

PHP_GRF_PCIEPIPE_CON0

Address: Operational Base(0x26020000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	pcie1_pipe_gate Gate PCIE1 pipe clock, set 1'b1 to gate the pipe clock.
2	RW	0x0	pcie0_pipe_gate Gate PCIE0 pipe clock, set 1'b1 to gate the pipe clock.
1:0	RO	0x0	reserved

PHP_GRF_PCIE_CLKREQ_ST

Address: Operational Base(0x26020000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	pcie1_clkreq_in PCIE1 clkreq.
0	RO	0x0	pcie0_clkreq_in PCIE0 clkreq.

PHP_GRF_MMU0_ST0

Address: Operational Base(0x26020000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000700	mmu0_st0 Bit[0]: Error Type is page write. Bit[1]: Error Type is die tag hits. Bit[2]: Error Type is pte tag hits. Bit[8]: AXI bus is idle. Bit[9]: AXI bus is idle in slave side. Bit[10]: AXI bus is idle in master side. Bit[11]: AXI bus counter is overflow in slave side. Bit[12]: AXI bus counter is overflow in master side. Bit[18]: PTE_LRU_ORG is 0, these means PTE LRU ERR. Bit[19]: DTE_LRU_ORG is 0, these means DTE LRU ERR. Bit[20]: PTE_LRU_ORG is not one hot, these means PTE LRU ERR. Bit[21]: DTE_LRU_ORG is not one hot, these means DTE LRU ERR.

PHP_GRF_MMU0_ST1

Address: Operational Base(0x26020000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu0_st1 Bit[7:0]: Return the External Rx AXI Command Counter Value. Bit[15:8]: Return the External Tx AXI Command Counter Value. Bit[23:16]: Return the AXI Page Read Data Channel Counter Value. Bit[31:24]: Return the AXI Page Address Read Channel Counter Value.

PHP_GRF_MMU0_ST2

Address: Operational Base(0x26020000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu0_st2 Bit[7:0]: Return the AXI B channel Counter in Slave Side. Bit[15:8]: Return the AXI Wdata channel Counter in Slave Side. Bit[23:16]: Return the AXI WAddress channel Counter in Slave Side.

PHP_GRF_MMU0_ST3

Address: Operational Base(0x26020000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu0_st3 Bit[7:0]: Return the AXI B channel Counter in Master Side. Bit[15:8]: Return the AXI Wdata channel Counter in Master Side. Bit[23:16]: Return the AXI WAddress channel Counter in Master Side.

PHP_GRF_MMU0_ST4

Address: Operational Base(0x26020000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu0_st4 Bit[7:0]: Return the AXI Rdata Channel Counter value in Master Side. It includes the AXI PAGE Read Counter. Bit[15:8]: Return the AXI RAddress Channel Counter value in Master Side. It includes the AXI PAGE Raddr Counter.

PHP_GRF_MMU1_ST0

Address: Operational Base(0x26020000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000700	mmu1_st0 Bit[0]: Error Type is page write. Bit[1]: Error Type is die tag hits. Bit[2]: Error Type is pte tag hits. Bit[8]: AXI bus is idle. Bit[9]: AXI bus is idle in slave side. Bit[10]: AXI bus is idle in master side. Bit[11]: AXI bus counter is overflow in slave side. Bit[12]: AXI bus counter is overflow in master side. Bit[18]: PTE_LRU_ORG is 0, these means PTE LRU ERR. Bit[19]: DTE_LRU_ORG is 0, these means DTE LRU ERR. Bit[20]: PTE_LRU_ORG is not one hot, these means PTE LRU ERR. Bit[21]: DTE_LRU_ORG is not one hot, these means DTE LRU ERR.

PHP_GRF_MMU1_ST1

Address: Operational Base(0x26020000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu1_st1 Bit[7:0]: Return the External Rx AXI Command Counter Value. Bit[15:8]: Return the External Tx AXI Command Counter Value. Bit[23:16]: Return the AXI Page Read Data Channel Counter Value. Bit[31:24]: Return the AXI Page Address Read Channel Counter Value.

PHP_GRF_MMU1_ST2

Address: Operational Base(0x26020000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu1_st2 Bit[7:0]: Return the AXI B channel Counter in Slave Side. Bit[15:8]: Return the AXI Wdata channel Counter in Slave Side. Bit[23:16]: Return the AXI WAddress channel Counter in Slave Side.

PHP_GRF_MMU1_ST3

Address: Operational Base(0x26020000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu1_st3 Bit[7:0]: Return the AXI B channel Counter in Master Side. Bit[15:8]: Return the AXI Wdata channel Counter in Master Side. Bit[23:16]: Return the AXI WAddress channel Counter in Master Side.

PHP_GRF_MMU1_ST4

Address: Operational Base(0x26020000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu1_st4 Bit[7:0]: Return the AXI Rdata Channel Counter value in Master Side. It includes the AXI PAGE Read Counter. Bit[15:8]: Return the AXI RAddress Channel Counter value in Master Side. It includes the AXI PAGE Raddr Counter.

5.14 USB_GRF Register Description

5.14.1 Registers Summary

Name	Offset	Size	Reset Value	Description
USB_GRF_MMUBP_ST	0x0000	W	0x00000000	MMU2 bypass status register
USB_GRF_MMUBP_CON	0x0004	W	0x00000000	MMU2 bypass address control register
USB_GRF_MMU2_CON	0x0008	W	0x00000000	MMU2 control register
USB_GRF_MEM_CON0	0x000C	W	0x00001410	PD_USB memory configuration for HDSPPRF
USB_GRF_MEM_CON1	0x0010	W	0x00008010	PD_USB memory configuration for UHDDPRF
USB_GRF_USB3OTG0_STATUS_LAT0	0x001C	W	0x00000000	USB3OTG0 status register 0
USB_GRF_USB3OTG0_STATUS_LAT1	0x0020	W	0x00000000	USB3OTG0 status register 1
USB_GRF_USB3OTG0_STATUS_CB	0x0024	W	0x00000000	USB3OTG0 status register 2
USB_GRF_USB3OTG0_STATUS	0x0028	W	0x00000000	USB3OTG0 status register 3
USB_GRF_USB3OTG0_CON0	0x002C	W	0x00002000	USB3OTG0 control register 0
USB_GRF_USB3OTG0_CON1	0x0030	W	0x00000000	USB3OTG0 control register 1
USB_GRF_MMU2_ST0	0x0044	W	0x00000700	MMU2 status register 0
USB_GRF_MMU2_ST1	0x0048	W	0x00000000	MMU2 status register 1
USB_GRF_MMU2_ST2	0x004C	W	0x00000000	MMU2 status register 2
USB_GRF_MMU2_ST3	0x0050	W	0x00000000	MMU2 status register 3
USB_GRF_MMU2_ST4	0x0054	W	0x00000000	MMU2 status register 4
USB_GRF_MEM_CON2	0x0058	W	0x00110010	PD_USB memory configuration for HDSPRF

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access*

5.14.2 Detail Registers Description

USB_GRF_MMUBP_ST

Address: Operational Base(0x2601E000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	mmu2_idle MMU2 idle state. 1'b0: Not idle state 1'b1: Idle state
3:0	RO	0x0	reserved

USB_GRF_MMUBP_CON

Address: Operational Base(0x2601E000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	usb3otg0_araddr_h Software control usb3otg0 araddr[39:32].

Bit	Attr	Reset Value	Description
7:0	RW	0x00	usb3otg0_awaddr_h Software control usb3otg0 awaddr[39:32].

USB_GRF_MMU2_CON

Address: Operational Base(0x2601E000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	dbg_err_clr 1'b1: Enable to Clear the MMU debug counters0,1,2,3 1'b0: Disable it
3	RW	0x0	mem_gate_en 1'b1: Enable to auto gating the MMU TLB Memory 1'b0: Disable it.
2	RW	0x0	mon_clr 1'b1: Enable to clear the AXI monitor counter 1'b0: Disable it
1	RW	0x0	bypass_grf 1'b1: Enable to bypass it when the MMU is idle state 1'b0: Disable
0	RW	0x0	bypass_force 1'b1: Enable to force MMU bypass 1'b0: Disable

USB_GRF_MEM_CON0

Address: Operational Base(0x2601E000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x1410	usb_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_USB. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

USB_GRF_MEM_CON1

Address: Operational Base(0x2601E000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
18:0	RW	0x08010	usb_mem_cfg_uhdpdprf Interface configuration for UHDPDPPRF type memory in PD_USB. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

USB_GRF_USB3OTG0_STATUS_LAT0

Address: Operational Base(0x2601E000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	usb3otg_logic_analyzer_trace0 Usb3otg_logic_analyzer_trace[31:0] bit status. Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility.

USB_GRF_USB3OTG0_STATUS_LAT1

Address: Operational Base(0x2601E000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	usb3otg_logic_analyzer_trace1 Usb3otg_logic_analyzer_trace[63:32] bit status. Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility.

USB_GRF_USB3OTG0_STATUS_CB

Address: Operational Base(0x2601E000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	usb3otg_host_current_belt[11:0] Usb3otg_host_current_belt[11:0] bit status. Current BELT Value. This signal indicates the minimum value of all received BELT values and the BELT that is set by the Set LTV command. This signal is valid only in Host mode.

USB_GRF_USB3OTG0_STATUS

Address: Operational Base(0x2601E000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x0	usb3otg0_pme_generation PME Generation. This signal is used to generate a PME# (Power Management Event). When the Run/Stop bit of the USB Command Register is cleared during USB suspend mode, the core cannot generate an event and cannot assert a regular interrupt. In this case, the core asserts a pme_generation signal to report any wakeup condition if pme_en is high. If the system does not support PCI-like PME interface, then it must not clear the Run/Stop bit during USB suspend mode. In this case, the core generates an event and asserts an interrupt when there is any wakeup event.
0	RO	0x0	usb3otg0_host_sys_err Host System Error. This signal indicates that a Host System Error has occurred as reflected in the USBSTS.HSE field. This signal is asserted only if the USBCMD.HSEE field is set to '1'. It can occur when the host controller encounters an 'Error' response in the AHB, the AXI, or the Native Master Bus. When the USBSTS.HSE field is cleared by software, this signal is deasserted unless the master continues to assert its bus error output. The typical software response to an HSE is to reset the core. For more details, refer to section 4.10.2.6 of the xHCI 1.0 specification.

USB_GRF_USB3OTG0_CON0

Address: Operational Base(0x2601E000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb3otg0_host_u2_port_disable USB2.0 Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state.
14	RW	0x0	usb3otg0_host_port_power_control_present This indicates whether the host controller implementation includes port power control. 1'b0: Indicates that the port does not have port power switches 1'b1: Indicates that the port has port power switches

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Bit	Attr	Reset Value	Description
13:8	RW	0x20	usb3otg0_fladj_30mhz_reg HS Jitter Adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 's duration. With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933ns. You must program the value in terms of high speed bit times in a 30 MHz cycle. The default value that must be driven is 32 (assuming 30 MHz perfect clock). Fladj_30mhz_reg connects to the FLADJ register defined in the xHCI spec in the PCI configuration space. Each count is equal to 16 high speed bit times. By default, when this register is set to 32, it gives a 125us interval. Now, based the clock accuracy you can decrement the count or increment the count to get the 125 us uSOF window. For non-PCI systems, it is recommended that this strap is connected to a register that can be controlled by software. This strap is used in device mode also. If device only mode is implemented, it is recommended to tie this input to 'd32.
7:6	RW	0x0	usb3otg0_hub_port_perm_attach Indicates if the device attached to a downstream port is permanently attached or not. 1'b0: Not permanently attached 1'b1: Permanently attached Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port
5:4	RW	0x0	usb3otg0_hub_port_overcurrent This is the per port Overcurrent indication of the root-hub ports: 1'b0: No Overcurrent 1'b1: Overcurrent Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port
3:0	RW	0x0	usb3otg0_bus_filter_bypass It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core. The function of each bit is: bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports In non-OTG Host-only mode, internal bus filters are not needed. Values: 1'b0: Bus filter(s) enabled 1'b1: Bus filter(s) disabled (bypassed)

USB_GRF_USB3OTG0_CON1

Address: Operational Base(0x2601E000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x1	usb3otg0_host_num_u3_port xHCI usb3 port number, default as 1.
11:8	RW	0x1	usb3otg0_host_num_u2_port xHCI host USB2 Port number, default as 1.

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Bit	Attr	Reset Value	Description
7	RW	0x0	usb3otg0_pipe_clk_sel usb3otg1_pipe3_rx_pclk/tx_pclk input source clk select. 1'b0: Select clk_usb3otg0_pipe for source clock 1'b1: Select clk_usb3otg0_utmi for source clock
6	RW	0x0	usb3otg0_mem_gate_en 1'b1: Enanle memory auto clock gating 1'b0: Disable memory auto clock gating
5	RW	0x0	usb3otg0_host_legacy_smi_bar Use this register to support SMI on BAR defined in xHCI spec. Software must set this register, then clear this register to indicate Base Address Register written.
4	RW	0x0	usb3otg0_host_legacy_smi_pci_cmd Use this register to support SMI on PCI Command defined in xHCI spec. Software must set this register, then clear this register to indicate PCI command register written.
3:2	RW	0x0	usb3otg0_phystatus_con Grf controll usb pipe phystatus. 2'b00: Select phystatus form phy. 2'b10: Set phystatus to 0. Others: Reserved
1	RW	0x0	usb3otg0_pme_en Enable signal for the pme_generation. Enable the core to assert pme_generation. If not use set this bit to 1'b1.
0	RW	0x0	usb3otg0_host_u3_port_disable USB 3.0 SS Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled

USB_GRF_MMU2_ST0

Address: Operational Base(0x2601E000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000700	mmu2_st0 Bit[0]: Error Type is page write. Bit[1]: Error Type is die tag hits. Bit[2]: Error Type is pte tag hits. Bit[8]: AXI bus is idle. Bit[9]: AXI bus is idle in slave side. Bit[10]: AXI bus is idle in master side. Bit[11]: AXI bus counter is overflow in slave side. Bit[12]: AXI bus counter is overflow in master side. Bit[18]: PTE_LRU_ORG is 0, these means PTE LRU ERR. Bit[19]: DTE_LRU_ORG is 0, these means DTE LRU ERR. Bit[20]: PTE_LRU_ORG is not one hot, these means PTE LRU ERR. Bit[21]: DTE_LRU_ORG is not one hot, these means DTE LRU ERR.

USB_GRF_MMU2_ST1

Address: Operational Base(0x2601E000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu2_st1 Bit[7:0]: Return the External Rx AXI Command Counter Value. Bit[15:8]: Return the External Tx AXI Command Counter Value. Bit[23:16]: Return the AXI Page Read Data Channel Counter Value. Bit[31:24]: Return the AXI Page Address Read Channel Counter Value.

USB_GRF_MMU2_ST2

Address: Operational Base(0x2601E000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu2_st2 Bit[7:0]: Return the AXI B channel Counter in Slave Side. Bit[15:8]: Return the AXI Wdata channel Counter in Slave Side. Bit[23:16]: Return the AXI WAddress channel Counter in Slave Side.

USB_GRF_MMU2_ST3

Address: Operational Base(0x2601E000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu2_st3 Bit[7:0]: Return the AXI B channel Counter in Master Side. Bit[15:8]: Return the AXI Wdata channel Counter in Master Side. Bit[23:16]: Return the AXI WAddress channel Counter in Master Side.

USB_GRF_MMU2_ST4

Address: Operational Base(0x2601E000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RC	0x00000000	mmu2_st4 Bit[7:0]: Return the AXI Rdata Channel Counter value in Master Side. It includes the AXI PAGE Read Counter. Bit[15:8]: Return the AXI RAddress Channel Counter value in Master Side. It includes the AXI PAGE Raddr Counter.

USB_GRF_MEM_CON2

Address: Operational Base(0x2601E000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x110010	usb_mem_cfg_hdsprf Interface configuration for HSDPRF type memory in PD_USB. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

5.15 SDGMAC_GRF Register Description

5.15.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SDGMAC_GRF_MEM_CON0	0x0000	W	0x00001410	PD_SDGMAC memory configuration for HDSPRF
SDGMAC_GRF_MEM_CON1	0x0004	W	0x00008010	PD_SDGMAC memory configuration for UHDDPRF
SDGMAC_GRF_MEM_CON2	0x0010	W	0x00110010	PD_SDGMAC memory configuration for HSDPRF
SDGMAC_GRF_GMAC_ST0	0x001C	W	0x00000000	GMAC status register
SDGMAC_GRF_GMAC0_CON	0x0020	W	0x00000000	GMAC0 control register
SDGMAC_GRF_GMAC1_CON	0x0024	W	0x00000000	GMAC1 control register
SDGMAC_GRF_GMAC0_TP0	0x0028	W	0x00000000	GMAC0 timestamp status 0 register
SDGMAC_GRF_GMAC0_TP1	0x002C	W	0x00000000	GMAC0 timestamp status 1 register
SDGMAC_GRF_GMAC1_TP0	0x0030	W	0x00000000	GMAC1 timestamp status 0 register
SDGMAC_GRF_GMAC1_TP1	0x0034	W	0x00000000	GMAC1 timestamp status 1 register
SDGMAC_GRF_GMAC0_CMD	0x0038	W	0x00000000	GAMC0 command register
SDGMAC_GRF_GMAC1_CMD	0x003C	W	0x00000000	GAMC1 command register
SDGMAC_GRF_MEM_GATE_CON	0x0048	W	0x00000000	Memory gate control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.15.2 Detail Registers Description

SDGMAC_GRF_MEM_CON0

Address: Operational Base(0x26038000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x1410	sdgmac_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_SDGMAC. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

SDGMAC_GRF_MEM_CON1

Address: Operational Base(0x26038000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
18:0	RW	0x08010	sdgmac_mem_cfg_uhddprf Interface configuration for UHDPDPPRF type memory in PD_SDGMAC. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Bit[16]: TESTRWM Other bits: Reserved

SDGMAC_GRF_MEM_CON2

Address: Operational Base(0x26038000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x110010	sdgmac_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_SDGMAC. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

SDGMAC_GRF_GMAC_ST0

Address: Operational Base(0x26038000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	gmac1_mac_speed GMAC1 Speed indication/status. 2'b00:1000Mbps(GMII) 2'b01: 2500Mbps(GMII) 2'b10: 10Mbps(MII) 2'b11: 100Mbps(MII)
4	RO	0x0	gmac1_sbd_tx_clk_gating GMAC1 LPI Tx Clock Gating Control. This signal is high after the MAC enters the Tx LPI (low power idle) mode. You can use this signal to control the Tx clock gating.
3	RO	0x0	gmac0_mac_speed GMAC0 Speed indication/status. 2'b00:1000Mbps(GMII) 2'b01: 2500Mbps(GMII) 2'b10: 10Mbps(MII) 2'b11: 100Mbps(MII)
2	RO	0x0	gmac0_sbd_tx_clk_gating GMAC0 LPI Tx Clock Gating Control. This signal is high after the MAC enters the Tx LPI (low power idle) mode. You can use this signal to control the Tx clock gating.
1	RO	0x0	gmac1_ptp_pps GMAC1 Pulse Per Second. This signal is high based on the PPS mode selected in the GMAC_MAC_PPS_CONTROL register. When PPS is programmed in Media Clock recovery Mode, this port indicates the recovered clock.

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Bit	Attr	Reset Value	Description
0	RO	0x0	gmac0_ptp_pps GMAC0 Pulse Per Second. This signal is high based on the PPS mode selected in the GMAC_MAC_PPS_CONTROL register. When PPS is programmed in Media Clock recovery Mode, this port indicates the recovered clock.

SDGMAC_GRF_GMAC0_CON

Address: Operational Base(0x26038000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	gmac0_ptp_aux_ts_trig Auxiliary Time Stamp Trigger. This signal is asserted to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO. A rising edge on this port is used to trigger the auxiliary snapshot.
10	RO	0x0	reserved
9	RW	0x0	gmac0_mcg_pst_trig Trigger Input to the DUT to capture presentation time.
8	RW	0x0	gmac0_mcg_pst_trig_sel Trigger Input to the DUT to capture presentation time. From IO or software. 1'b1: From IO 1'b0: From gmac0_mcg_pst_trig.
7:3	RW	0x00	gmac0_clk_con GMAC0 cru configuration. Bit[3]: RMII mode. Bit[4]: Gate RMII 50MHz clock, active high. Bit[6:5]: GMAC0 controller txclk divider sel. In RMII mode : 2'b0: 25Mhz 2'b1: 2.5Mhz In RGMII mode : 2'b10: 2.5Mhz 2'b11: 25Mhz other: 125Mhz Bit[7]: GMAC0 txclk select control. 1'b0: Select clock form CRU 1'b1: Select clock form IO
2:1	RW	0x0	gnac0_sbd_flowctrl Sideband Flow Control. When set high, instructs the MAC to transmit Pause frames in Full-duplex mode. In half-duplex mode, the MAC enables the Back-pressure function until this signal is made low again.
0	RW	0x0	gmac0_clk_gating_en GMAC0 memory clock gate enable, active high.

SDGMAC_GRF_GMAC1_CON

Address: Operational Base(0x26038000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	gmac1_ptp_aux_ts_trig Auxiliary Time Stamp Trigger. This signal is asserted to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO. A rising edge on this port is used to trigger the auxiliary snapshot.
10	RO	0x0	reserved
9	RW	0x0	gmac1_mcg_pst_trig Trigger Input to the DUT to capture presentation time.
8	RW	0x0	gmac1_mcg_pst_trig_sel Trigger Input to the DUT to capture presentation time. From IO or software. 1'b1: From IO 1'b0: From gmac0_mcg_pst_trig.
7:3	RW	0x00	gmac1_clk_con GMAC1 cru configuration. Bit[3]: RMII mode. Bit[4]: Gate RMII 50MHz clock, active high. Bit[6:5]: GMAC1 controller txclk divider sel. In RMII mode : 2'b0: 25Mhz 2'b1: 2.5Mhz In RGMII mode : 2'b10: 2.5Mhz 2'b11: 25Mhz other: 125Mhz Bit[7]: GMAC1 txclk select control. 1'b0: Select clock form CRU 1'b1: Select clock form IO
2:1	RW	0x0	gnac1_sbd_flowctrl Sideband Flow Control. When set high, instructs the MAC to transmit Pause frames in Full-duplex mode. In half-duplex mode, the MAC enables the Back-pressure function until this signal is made low again.
0	RW	0x0	gmac1_clk_gating_en GMAC1 memory clock gate enable, active high.

SDGMAC_GRF_GMAC0_TP0

Address: Operational Base(0x26038000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gmac0_timestamp_0 GMAC0 ptp timestamp[31:0] Reference Time Output. This bus provides the System Time output when it is generated internally.

SDGMAC_GRF_GMAC0_TP1

Address: Operational Base(0x26038000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gmac0_timestamp_1 GMAC0 ptp timestamp[63:32] Reference Time Output. This bus provides the System Time output when it is generated internally.

SDGMAC_GRF_GMAC1_TP0

Address: Operational Base(0x26038000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gmac1_timestamp_0 GMAC1 ptp timestamp[31:0] Reference Time Output. This bus provides the System Time output when it is generated internally.

SDGMAC_GRF_GMAC1_TP1

Address: Operational Base(0x26038000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gmac1_timestamp_1 GMAC1 ptp timestamp[63:32] Reference Time Output. This bus provides the System Time output when it is generated internally.

SDGMAC_GRF_GMAC0_CMD

Address: Operational Base(0x26038000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	gmac0_mcgr_dma_ack_cmd If write this be written to 1, a pulse will be set to GMAC0.

SDGMAC_GRF_GMAC1_CMD

Address: Operational Base(0x26038000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	gmac1_mcgr_dma_ack_cmd If write this be written to 1, a pulse will be set to GMAC1.

SDGMAC_GRF_MEM_GATE_CON

Address: Operational Base(0x26038000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	flexbus_rx_mem_gat_en FLEXBUS memory clock gate enable for RX, active high.
1	RW	0x0	flexbus_tx_mem_gat_en FLEXBUS memory clock gate enable for TX, active high.
0	RO	0x0	reserved

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5.16 VO0_GRF Register Description

5.16.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VO0_GRF_SOC_CON0	0x0000	W	0x00000000	Video output group 0 system control register 0
VO0_GRF_SOC_CON1	0x0004	W	0x00000000	Video output group 0 HDMITX control register 0
VO0_GRF_SOC_CON5	0x0014	W	0x00000000	Video output group 0 HDMITX control register 4
VO0_GRF_SOC_CON6	0x0018	W	0x00000000	Video output group 0 HDMITX control register 5
VO0_GRF_SOC_CON7	0x001C	W	0x00000000	Video output group 0 HDMITX control register 6
VO0_GRF_SOC_CON8	0x0020	W	0x00000000	Video output group 0 HDMITX control register 8
VO0_GRF_SOC_CON9	0x0024	W	0x00000000	Video output group 0 system control register 9
VO0_GRF_SOC_CON10	0x0028	W	0x00000000	Video output group 0 system control register 10
VO0_GRF_SOC_CON11	0x002C	W	0x00000000	Video output group 0 HDMITX control register 7
VO0_GRF_SOC_CON12	0x0030	W	0x00000000	Video output group 0 HDMITX control register 8
VO0_GRF_SOC_CON13	0x0034	W	0x00000000	Video output group 0 system control register 13
VO0_GRF_SOC_CON14	0x0038	W	0x00000000	Video output group 0 system control register 14
VO0_GRF_SOC_CON32	0x0080	W	0x00001410	Video output group 0 system control register 32
VO0_GRF_SOC_CON33	0x0084	W	0x00110010	Video output group 0 system control register 33
VO0_GRF_SOC_ST0	0x00C0	W	0x00000000	Video output group 0 system status register 0
VO0_GRF_SOC_ST2	0x00C8	W	0x00000000	Video output group 0 system status register 2
VO0_GRF_SOC_ST3	0x00CC	W	0x00000000	Video output group 0 system status register 3
VO0_GRF_SOC_ST4	0x00D0	W	0x00000000	Video output group 0 system status register 4
VO0_GRF_SOC_ST5	0x00D4	W	0x00000000	Video output group 0 system status register 5
VO0_GRF_HDCP0_RNG_CON0	0x00F0	W	0x00000000	Video output group 0 HDCP0_RNG control register 0
VO0_GRF_HDCP0_RNG_ST0	0x00F8	W	0x00000000	Video output group 0 HDCP0_RNG status register 0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.16.2 Detail Registers Description

VO0_GRF_SOC_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:6	RO	0x000	reserved
5	RW	0x0	grf_con_edp0_spdif_sel Enable connect SPDIF_TX2 interface to EDP0 SPDIF port. 1'b0: Disable 1'b1: Enable
4	RW	0x0	grf_con_edp0_i2s_sel Enable connect SAI6 interface to EDP0 I2S port. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

VO0_GRF_SOC_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15	RW	0x0	grf_con_hdmtx_revapb_sel 1'b1: The rev ram can be accessed by the cpu with the apb bus. Attention: In the func mode, this must be 0. 1'b0: Disable it.
14	RW	0x0	grf_con_hdmtx_emp_mem_len_en 1'b1: Choose the 1 value for enable the emp_mem_len sync From the VOP to HDMITX. This means, if the emp_mem_len changed From the VOP side, it also auto changed at the HDMITX side. 1'b0: Disable it.
13	RW	0x0	grf_con_hdmtx_emp_mem_len_bypass 1'b0: Choose the 0 value for keep the emp mem function as the original version. 1'b1: Choose the 1 value for bypass the VOP emp_mem_len to the hdmi emp_mem_len.
12	RW	0x0	grf_con_hdmtx_hdcp14_cntclr_hw_force 1'b0: Choose the 0 value for keep the hdcp1.4 function as the old version. 1'b1: Choose the 1 value for force clear the hdcp1.4 inter rvalid_cnt to 0.
11	RW	0x0	grf_con_hdmtx_hdcp14_cntclr_hw_org 1'b0: Choose the 0 value for keep the hdcp1.4 function as the old version. 1'b1: Choose the 1 value for solve the hdcp1.4 inter rvalid_cnt auto clear func.
10	RW	0x0	grf_con_hdmtx_force_rpt_bit_org 1'b0: Choose the 0 value for not force rpt bit. 1'b1: Choose the 1 value for force rpt bit.
9	RW	0x0	grf_con_hdmtx_revoc_mbist_force_open 1'b0: Choose the 0 value for not force clk revoc in the mbist mode SP RAM. 1'b1: Choose the 1 value for force clk revoc in the mbist mode SP RAM.

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Bit	Attr	Reset Value	Description
8	RW	0x0	grf_con_hdmtx_pktzb_mbist_force_open 1'b0: Choose the 0 value for not force clk pktzb in the mbist mode DP RAM. 1'b1: Choose the 1 value for force clk pktzb in the mbist mode DP RAM.
7	RW	0x0	grf_con_hdmtx_revoc_fifo_force_open 1'b0: Choose the 0 value for auto clocking revoc fifo. 1'b1: Choose the 1 value for always on clock revoc fifo.
6	RW	0x0	grf_con_hdmtx_pktzb_fifo_force_open 1'b0: Choose the 0 value for auto clocking pktzb in the frl mode DP RAM. 1'b1: Choose the 1 value for always on clock pktzb in the frl mode DP RAM.
5	RW	0x0	grf_con_hdmtx_pktza_fifo_force_open 1'b0: Choose the 0 value for auto clocking pktza in the frl mode DP RAM. 1'b1: Choose the 1 value for always on clock pktza in the frl mode DP RAM.
4	RW	0x0	grf_con_hdmtx_ophyclk_phase 1'b0: Choose the 0 value ophyclk_phase link2phy in frl mode. 1'b1: Choose the 1 value ophyclk_phase link2phy in frl mode. Attention: Software Engineer should not change the value if the frl mode is ok.
3	RW	0x0	grf_con_hdmtx_set_clr 1'b0: Not clear counter link2phy in frl mode. 1'b1: Clear counter link2phy in frl mode. Attention: Software Engineer should not change the value if the frl mode is ok.
2	RW	0x0	grf_con_hdmtx_samplevalue 1'b0: Choose the 0 value link2phy in frl mode. 1'b1: Choose the 1 value link2phy in frl mode. Attention: Software Engineer should not change the value if the frl mode is ok.
1	RW	0x0	grf_con_hdmtx_tob18en 1'b0: Choose the 36bit link2phy in frl mode. 1'b1: Choose the 18bit link2phy in frl mode. Attention: Software Engineer should not change the value if the frl mode is ok.
0	RW	0x0	grf_con_hdmitx_frlmod 1'b1: Choose the hdmi2.1 frl mode, can support up to4k120p. 1'b0: Choose the hdmi2.0 tmds mode. can support up to 4k60p.

VO0_GRF_SOC_CON5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15	RW	0x0	grf_i2c_rst 1'b1: Means i2c delayline module reset. 1'b0: Normal mode.
14:0	RO	0x0000	reserved

VO0_GRF_SOC_CON6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:12	RW	0x0	grf_iscl_dlyn The negedge delay for signal "iscl" From 1 to 0. The value range is {0, 1, 2, 3, ...15}. For example, if 1 delay scale = 40ns, the value is 3. So the posedge delay is 3 * 40ns = 120ns.
11:8	RW	0x0	grf_iscl_dlyp The posedge delay for signal "iscl" From 0 to 1. The value range is {0, 1, 2, 3, ...15}. For example, if 1 delay scale = 40ns, the value is 3. So the posedge delay is 3 * 40ns = 120ns.
7:1	RW	0x00	grf_iscl_div The delayline delay scale. 1 delay scale = (1 + n) * 40ns. n is {0, 1, 2, 3, ...127}. For example: n = 0, means 1 delay scale is 40ns. n = 1, means 1 delay scale is 80ns. n = 2, means 1 delay scale is 120ns. n = 127, means 1 delay scale is (127 + 1) * 40ns = 5.12us.
0	RW	0x0	grf_iscl_dly_en 1'b1: Enable the delay line for "iscl" signal. 1'b0: Disable it.

VO0_GRF_SOC_CON7

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	grf_isda_dlyn The negedge delay for signal "isda" From 1 to 0. The value range is {0, 1, 2, 3, ...15}. For example, if 1 delay scale = 40ns, the value is 3. So the posedge delay is 3 * 40ns = 120ns.
11:8	RW	0x0	grf_isda_dlyp The posedge delay for signal "isda" From 0 to 1. The value range is {0, 1, 2, 3, ...15}. For example, if 1 delay scale = 40ns, the value is 3. So the posedge delay is 3 * 40ns=120ns.
7:1	RW	0x00	grf_isda_div The delayline delay scale. 1 delay scale = (1 + n) * 40ns. n is {0, 1, 2, 3, ...127}. For example: n = 0, means 1 delay scale is 40ns. n = 1, means 1 delay scale is 80ns. n = 2, means 1 delay scale is 120ns. n = 127, means 1 delay scale is (127 + 1) * 40ns = 5.12us.
0	RW	0x0	grf_isda_dly_en 1'b1: Enable the delay line for "isda" signal. 1'b0: Disable it.

VO0_GRF_SOC_CON8

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b9: Write access enable.
15	RW	0x0	grf_vo0_edp_div2_gate Enable EDP clk_div2 gating. 1'b0: Disable 1'b1: Enable
14	RW	0x0	grf_vo0_edp_chtxd_gate Enable EDP clk_chtxd gating. 1'b0: Disable 1'b1: Enable
13	RW	0x0	grf_edp_i_hdcp_protect Enable EDP hdcp protect function. 1'b0: Disable 1'b1: Enable
12	RW	0x0	hdcp_gating_en HDCP0 memory clock gating enable. 1'b0: always on 1'b1: auto gating
11:8	RW	0x0	grf_hdmitx_iipi_color_depth HDMITX image pixel interace video color depth. 4'h5: 0 bits per component 4'h6: 10 bits per component Others: Reserved.
7:4	RW	0x0	grf_hdmitx_iipi_format HDMITX image pixel interface video format. 4'h0: RGB 4'h1: YCbCr 4:2:2 4'h2: YCbCr 4:4:4 4'h3: YCbCr 4:2:0 4'hb: Compressed Data Others: Reserved.
3	RW	0x0	grf_hdmitx_cec_in_disable 1'b1: Disable cec function. 1'b0: Enable cec function.
2	RW	0x0	grf_vo0_hdmi_gate Disable clk_linksym_hdmitxphy0. 1'b0: Clock on 1'b1: Clock off
1	RW	0x0	edp_mem_gat_en Enable EDP memory clock auto gating. 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

VO0_GRF_SOC_CON9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b9: Write access enable.

Bit	Attr	Reset Value	Description
15:12	RW	0x0	grf_hdcp_i_global_gpio_in HDCP0 global GPIO input.
11	RO	0x0	reserved
10	RW	0x0	grf_edp_ch_sel Select path between VOP and EBC. 1'b0: Choose VOP path. 1'b1: Choose EBC path.
9	RW	0x0	grf_hdmi_ch_sel Select path between VOP and EDP. 1'b0: Choose EDP path. 1'b1: Choose VOP path.
8	RW	0x0	grf_mipi_ch_sel Select path between MIPI ipi and EBC ipi. 1'b0: Choose MIPI ipi. 1'b1: Choose EBC ipi.
7:4	RW	0x0	grf_hdcp_i_tmds1_color_depth HDCP0 color depth in.align with HDMITX ipi color depth. 4'h5: 8 bits per component 4'h6: 10 bits per component Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	edp_I_BIST_EN Enable EDP video bist function. 1'b0: Disable 1'b1: Enable

VO0_GRF_SOC_CON10

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b9: Write access enable.
15:12	RO	0x0	reserved
11:8	RW	0x0	dsihost_ipi_color_depth Configures the IPI color depth. 4'b0010: 5-6-5 bits 4'b0011: 6 bits 4'b0101: 8 bits 4'b0110: 10 bits Others: Reserved
7:4	RW	0x0	dsihost_ipi_format Configures the IPI pixel format. 4'b0000: RGB Others: Reserved
3	RW	0x0	dsihost_ipi_shutdn DSIHOST shutdown command. 1: Enable 0: Disable
2	RW	0x0	dsihost_ipi_colorm DSIHOST color mode command. 1: Enable 0: Disable

Bit	Attr	Reset Value	Description
1	RW	0x0	dsihost_txreqclkhs_mask DSIHOST De-skew request debug enable 1: Enable 0: Disable
0	RW	0x0	dsihost_dsi_host_gating_en DSIHOST memory clock gating enable 1: Enable 0: Disable

VO0_GRF_SOC_CON11

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:12	RW	0x0	grf_oscl_dlyn The negedge delay for signal "oscl" From 1 to 0. The value range is {0, 1, 2, 3, ...15}. For example, if 1 delay scale = 40ns, the value is 3. So the posedge delay is 3 * 40ns = 120ns.
11:8	RW	0x0	grf_oscl_dlyp The posedge delay for signal "oscl" From 0 to 1. The value range is {0, 1, 2, 3, ...15}. For example, if 1 delay scale = 40ns, the value is 3. So the posedge delay is 3 * 40ns = 120ns.
7:1	RW	0x00	grf_oscl_div The delayline delay scale. 1 delay scale = (1 + n) * 40ns. n is {0, 1, 2, 3, ...127}. For example: n = 0, means 1 delay scale is 40ns. n = 1, means 1 delay scale is 80ns. n = 2, means 1 delay scale is 120ns. n = 127, means 1 delay scale is (127 + 1) * 40ns = 5.12us.
0	RW	0x0	grf_oscl_dly_en 1'b1: Enable the delay line for "oscl" signal. 1'b0: Disable it.

VO0_GRF_SOC_CON12

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:12	RW	0x0	grf_osda_dlyn The negedge delay for signal "osda" From 1 to 0. The value range is {0, 1, 2, 3, ...15}. For example, if 1 delay scale = 40ns, the value is 3. So the posedge delay is 3 * 40ns = 120ns.
11:8	RW	0x0	grf_osda_dlyp The posedge delay for signal "osda" From 0 to 1. The value range is {0, 1, 2, 3, ...15}. For example, if 1 delay scale = 40ns, the value is 3. So the posedge delay is 3 * 40ns = 120ns.

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Bit	Attr	Reset Value	Description
7:1	RW	0x00	grf_osda_div The delayline delay scale. It is also named delay time unit. 1 delay scale = (1 + n) * 40ns. n is {0, 1, 2, 3, ...127}. For example: n = 0, means 1 delay scale is 40ns. n = 1, means 1 delay scale is 80ns. n = 2, means 1 delay scale is 120ns. n = 127, means 1 delay scale is (127 + 1) * 40ns = 5.12us.
0	RW	0x0	grf_osda_dly_en 1'b1: Enable the delay line for "osda" signal. 1'b0: Disable it.

VO0_GRF_SOC_CON13

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b9: Write access enable.
15:11	RO	0x00	reserved
10	RW	0x0	grf_hdcp_ipiclk_disable HDCP0 ipiclk gating. When high, disable clock.
9	RW	0x0	grf_ebc_dclk2dsihost_disable Disable EBC dclk for DSIHOST. 1'b0: Clock On 1'b1: Clock Off
8	RW	0x0	grf_ebc_dclk2hdmitx_disable Disable EBC dclk for HDMITX. 1'b0: Clock On 1'b1: Clock Off
7	RW	0x0	grf_ebc_dclk2edp_disable Disable EBC dclk for EDP. 1'b0: Clock On 1'b1: Clock Off
6	RW	0x0	grf_sw_hdmi_hsync_pol Hsync polarity. 1'b0:Positive 1'b1:Negative
5	RW	0x0	grf_sw_hdmi_vsync_pol Vsync polarity. 1'b0:Positive 1'b1:Negative
4	RW	0x0	grf_sw_hdmi_1to4_en HDMI 1to4 enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	grf_sw_mipi_mode EBC to DSIHOST mode control, it should be 0 (video mode).
2	RW	0x0	grf_sw_mipi_hsync_pol EBC to DSIHOST polar control, it should be 1.
1	RW	0x0	grf_sw_mipi_vsync_pol EBC to DSIHOST polar control, it should be 1.

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Bit	Attr	Reset Value	Description
0	RW	0x0	grf_sw_mipi_1to4_en EBC to DSIHOST interface enable 1: Enable 0: Disable

VO0_GRF_SOC_CON14

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:12	RO	0x0	reserved
11:8	RW	0x0	grf_hdmitx_ih2out_esm_global_gpio_out The set value of the hdmitx_ih2out_esm_golbal_gpio_out when the "grf_con_hdmitx_esm_global_gpio_sel is 0".
7	RW	0x0	grf_con_hdmitx_hdcp_i2c_grant_sw The value of the hdmi_hdcp_i2c_grant_i when grf_con_hdmitx_hdcp_i2c_grant_sel is 1.
6	RW	0x0	grf_con_hdmitx_hdcp_i2c_grant_sel HDMITX hdcp i2c grant select. 1'b1: Choose software control HDCP0 i2c path. 1'b0: Choose hardware.
5	RW	0x0	grf_con_hdmitx_sdain_msk 1'b1: Choose hdmitx_sda, so means enable HDMITX iic. 1'b0: Choose 1'b1, so means disable it.
4	RW	0x0	grf_con_hdmitx_sclin_msk 1'b1: Choose hdmitx_scl, so means enable HDMITX iic. 1'b0: Choose 1'b1, so means disable it.
3	RW	0x0	grf_con_hdmitx_esm_global_gpio_sel 1'b1: Choose hdcp_0_global_gpio_out. 1'b0: Choose grf_hdmitx_ih2out_esm_global_gpio_out.
2	RW	0x0	grf_con_hdcp_p1_gpio_in_sel HDCP0 p1 gpio in select(HDMITX port). 1'b1: HDMITX oh2in_esm_gpio in 1'b0: {2'b0, hdmitx_i2c grant, 1'b1}
1	RW	0x0	grf_con_hdmitx_spdif_sel 1'b1: Choose SPDIF_TX2 enable for HDMITX. 1'b0: Not choose SPDIF_TX2 enable for HDMITX.
0	RW	0x0	grf_con_hdmitx_i2s_sel 1'b1: Choose SAI6 enable for HDMITX. 1'b0: Not choose SAI6 enable for HDMITX.

VO0_GRF_SOC_CON32

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x1410	grf_con_vo0_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_VO0. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

VO0_GRF_SOC_CON33

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x110010	grf_con_vo0_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_VO0. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

VO0_GRF_SOC_ST0

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	grf_hdmitx_status0 The bit [3: 0] store the value for int_ophy_txffe0. The bit [7: 4] store the value for int_ophy_txffe1. The bit [11: 8] store the value for int_ophy_txffe2. The bit [15:12] store the value for int_ophy_txffe3. The bit [23:16] store the value for link2phy_status. The bit [24] store the value for ii2cm_scl. The bit [25] store the value for ii2cm_sda. The bit [26] store the value for oi2cm_scl. The bit [27] store the value for oi2cm_sda. The bit [30:28] store the value for grf_st_hdcp14_rmemaccess_ff2. Attention, it can not solve the meta state, so software should read 3 times is same state to use it. The bit [31] store the value for 1'b0.

VO0_GRF_SOC_ST2

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RO	0x0	dsihost_phy_l0_txdatawidthhs DSIHOST Reserved.
7	RO	0x0	dsihost_phy_l0_txdatatransferenhs DSIHOST Reserved.
6	RO	0x0	dsihost_phy_forcerxmode DSIHOST Reserved.

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Bit	Attr	Reset Value	Description
5	RO	0x0	dsihost_phy_forcetxstopmode DSIHOST Reserved.
4	RO	0x0	dsihost_phy_clk_enable DSIHOST debug status.
3	RO	0x0	dsihost_phy_l0_enable DSIHOST debug status.
2	RO	0x0	dsihost_phy_l1_enable DSIHOST debug status.
1	RO	0x0	dsihost_phy_l2_enable DSIHOST debug status.
0	RO	0x0	dsihost_phy_l3_enable DSIHOST debug status.

VO0_GRF_SOC_ST3

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	hdptx_o_pll_lock_done 1'b1: Means HDPTXPHY pll locked. 1'b0: Means HDPTXPHY pll not locked.
2	RO	0x0	hdptx_o_phy_rdy 1'b1: Means HDPTXPHY ready. 1'b0: Means HDPTXPHY not ready.
1	RO	0x0	hdptx_o_phy_clk_rdy 1'b1: Means HDPTXPHY phy_clk ready. 1'b0: Means HDPTXPHY phy_clk not ready.
0	RO	0x0	hdptx_dtb 1'b1: Means HDPTXPHY monitoring digital signal is high level. 1'b0: Means HDPTXPHY monitoring digital signal is low level.

VO0_GRF_SOC_ST4

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	grf_st_hdcp_O_diag_out HDCP0 diag_out data.

VO0_GRF_SOC_ST5

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RO	0x0	hdcp_O_global_gpio_out HDCP0 global GPIO output data.
19:16	RO	0x0	hdmitx_oh2in_esm_global_gpio_in HDMITX oh2in esm global gpio in data.
15:0	RO	0x0000	hdcp_O_p1_gpio_out HDCP0 gpio out status.

VO0_GRF_HDCP0_RNG_CON0

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b9: Write access enable.
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	trng_I_ctrl_reseed Enable HDCP0_RNG reseed operation. 1'b0: Disable 1'b1: Enable When it is asserted, the HDCP0_RNG responds by stopping any reseed operation that is currently underway and initiating a new reseed operation.
0	RW	0x0	trng_I_ctrl_zeroize Enable HDCP0_RNG zeroize operation. 1'b0: Disable 1'b1: Enable

VO0_GRF_HDCP0_RNG_ST0

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	trng_O_ctrl_secure HDCP0_RNG secure mode output. 1'b0: Inactive 1'b1: Active
4	RO	0x0	trng_O_ctrl_reminder HDCP0_RNG reseed reminder output. 1'b0: Inactive 1'b1: Active
3	RO	0x0	trng_O_ctrl_reseeding HDCP0_RNG reseeding activity output. 1'b0: Inactive 1'b1: Active
2	RO	0x0	trng_O_ctrl_seeded HDCP0_RNG reseeding/seeding completion output. 1'b0: Inactive 1'b1: Active
1	RO	0x0	trng_O_ctrl_rand_bit HDCP0_RNG serial random bit output 1'b0: Inactive 1'b1: Active
0	RO	0x0	trng_O_ctrl_rand_vld HDCP0_RNG serial random bit valid output. 1'b0: Inactive 1'b1: Active

5.17 VO1_GRF Register Description

5.17.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VO1_GRF_SOC_CON0	0x0000	W	0x000000E4	Video output group 1 system control register 0
VO1_GRF_SOC_CON1	0x0004	W	0x00000000	Video output group 1 system control register 1
VO1_GRF_SOC_CON8	0x0020	W	0x00000000	Video output group 1 system control register 8
VO1_GRF_SOC_CON9	0x0024	W	0x00000000	Video output group 1 system control register 9

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Name	Offset	Size	Reset Value	Description
VO1_GRF_SOC_CON32	0x0080	W	0x14101410	Video output group 1 system control register 32
VO1_GRF_SOC_CON33	0x0084	W	0x00110010	Video output group 1 system control register 33
VO1_GRF_SOC_CON34	0x0088	W	0x00000000	Video output group 1 system control register 34
VO1_GRF_SOC_ST0	0x00C0	W	0x00000000	Video output group 1 system status register 0
VO1_GRF_SOC_ST1	0x00C4	W	0x00000000	Video output group 1 system status register 0
VO1_GRF_SOC_ST2	0x00C8	W	0x00000000	Video output group 1 system status register 0
VO1_GRF_HDCP1_RNG_CON0	0x00F0	W	0x00000000	Video output group 1 HDCP1_RNG control register 0
VO1_GRF_HDCP1_RNG_ST0	0x00F8	W	0x00000000	Video output group 1 HDCP1_RNG status register 0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.17.2 Detail Registers Description

VO1_GRF_SOC_CON0

Address: Operational Base(0x26036000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15:12	RO	0x0	reserved
11	RW	0x0	grf_con_dp0_sink_hpd_cfg Software configuration for DP0 hot plug detect input.
10	RW	0x0	grf_con_dp0_sink_hpd_sel Source selection for DP hot plug detect input. 1'b0: DP hot plug detect input controlled by hardware. 1'b1: DP hot plug detect input controlled by software.
9	RW	0x0	grf_con_dp0_aux_din_sel Polarity of DP aux data input. 1'b0: Normal 1'b1: Inverted
8	RW	0x0	grf_con_dp0_aux_dout_sel Polarity of DP aux data output. 1'b0: Normal 1'b1: Inverted
7:6	RW	0x3	grf_con_dp0_lane3_sel Data source selection for USBDPPHY lane 3. 2'h0: Select DP host lane 0 transmit parallel data output as USBDPPHY lane 3 data source. 2'h1: Select DP host lane 1 transmit parallel data output as USBDPPHY lane 3 data source. 2'h2: Select DP host lane 2 transmit parallel data output as USBDPPHY lane 3 data source. 2'h3: Select DP host lane 3 transmit parallel data output as USBDPPHY lane 3 data source.

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Bit	Attr	Reset Value	Description
5:4	RW	0x2	grf_con_dp0_lane2_sel Data source selection for USBDPPHY lane 2. 2'h0: Select DP host lane 0 transmit parallel data output as USBDPPHY lane 2 data source. 2'h1: Select DP host lane 1 transmit parallel data output as USBDPPHY lane 2 data source. 2'h2: Select DP host lane 2 transmit parallel data output as USBDPPHY lane 2 data source. 2'h3: Select DP host lane 3 transmit parallel data output as USBDPPHY lane 2 data source.
3:2	RW	0x1	grf_con_dp0_lane1_sel Data source selection for USBDPPHY lane 1. 2'h0: Select DP host lane 0 transmit parallel data output as USBDPPHY lane 1 data source. 2'h1: Select DP host lane 1 transmit parallel data output as USBDPPHY lane 1 data source. 2'h2: Select DP host lane 2 transmit parallel data output as USBDPPHY lane 1 data source. 2'h3: Select DP host lane 3 transmit parallel data output as USBDPPHY lane 1 data source.
1:0	RW	0x0	grf_con_dp0_lane0_sel Data source selection for USBDPPHY lane 0. 2'h0: Select DP host lane 0 transmit parallel data output as USBDPPHY lane 0 data source. 2'h1: Select DP host lane 1 transmit parallel data output as USBDPPHY lane 0 data source. 2'h2: Select DP host lane 2 transmit parallel data output as USBDPPHY lane 0 data source. 2'h3: Select DP host lane 3 transmit parallel data output as USBDPPHY lane 0 data source.

VO1_GRF_SOC_CON1

Address: Operational Base(0x26036000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x0	grf_con_dp0_phystatus_cfg Software configuration for USBDPPHY lane 0/1/2/3 PHY status. bit0: lane0 status bit1: lane1 status bit2: lane2 status bit3: lane3 status

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	grf_con_dp0_phystatus_sel Bit0: USBDPPHY lane 0 PHY status selection. 1'b0: USBDPPHY lane 0 PHY status controlled by hardware. 1'b1: USBDPPHY lane 0 PHY status controlled by software. Bit1: USBDPPHY lane 1 PHY status selection. 1'b0: USBDPPHY lane 1 PHY status controlled by hardware. 1'b1: USBDPPHY lane 1 PHY status controlled by software. Bit2: USBDPPHY lane 2 PHY status selection. 1'b0: USBDPPHY lane 2 PHY status controlled by hardware. 1'b1: USBDPPHY lane 2 PHY status controlled by software. Bit3: USBDPPHY lane 3 PHY status selection. 1'b0: USBDPPHY lane 3 PHY status controlled by hardware. 1'b1: USBDPPHY lane 3 PHY status controlled by software.
3:0	RO	0x0	reserved

VO1_GRF_SOC_CON8

Address: Operational Base(0x26036000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	grf_dp_tca_disable_i Disable DP input from the type-C assit block. 1'b0: Enable 1'b1: Disable
13:6	RO	0x00	reserved
5:2	RW	0x0	grf_hdcp1_I_global_gpio_in HDCP1 global gpio in grf source. Active when VO1_GRF_SOC_CON8[1] == 1'b0.
1	RW	0x0	grf_hdcp1_I_global_gpio_in_sel HDCP1 global gpio in source select. 1'b1: From IO 1'b0: From VO1_GRF_SOC_CON8[5:2]
0	RW	0x0	dp_mem_gat_en Enable DP memory clock gating. 1'b0: Disable 1'b1: Enable

VO1_GRF_SOC_CON9

Address: Operational Base(0x26036000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15	RW	0x0	grf_dp_spdif_sel2 Select DP SPDIF stream2. 1'b0: SPDIF_TX3 1'b1: SPDIF_TX5
14	RW	0x0	grf_dp_spdif_sel1 Select DP SPDIF stream1. 1'b0: SPDIF_TX3 1'b1: SPDIF_TX4

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Bit	Attr	Reset Value	Description
13	RW	0x0	grf_dp_spdif_sel0 Select DP SPDIF stream0. 1'b0: SPDIF_TX3 1'b1: SPDIF_TX4
12	RW	0x0	grf_dp_sai_sel2 Select DP I2S stream2. 1'b0: SAI7 1'b1: SAI9
11	RW	0x0	grf_dp_sai_sel1 Select DP I2S stream1. 1'b0: SAI7 1'b1: SAI8
10	RW	0x0	grf_dp_sai_sel0 Select DP I2S stream0. 1'b0: SAI7 1'b1: SAI8
9	RW	0x0	hdcp1_I_aes0_debug_trigger HDCP1 DP AES port 0 debug trigger configuration. When asserted, the hdcp_aes0_debug_data is captured internally by HDCP1.
8	RW	0x0	hdcp1_gating_en HDCP1 memory clock gate enable. 1'b0: Always on 1'b1: Auto gating
7:0	RO	0x00	reserved

VO1_GRF_SOC_CON32

Address: Operational Base(0x26036000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x1410	grf_con_vo1_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_VO1. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved
15:0	RW	0x1410	grf_con_vo1_mem_cfg_hdspra Interface configuration for HDSPRA type memory in PD_VO1. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

VO1_GRF_SOC_CON33

Address: Operational Base(0x26036000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x110010	grf_con_vo1_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_VO1. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

VO1_GRF_SOC_CON34

Address: Operational Base(0x26036000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hdcp1_I_aes0_debug_data HDCP1 DP AES port 0 debug data configuration.

VO1_GRF_SOC_ST0

Address: Operational Base(0x26036000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:14	RO	0x0	hdcp1_I_global_gpio_in HDCP1 global GPIO input.
13	RO	0x0	grf_dp_tca_disable_ack_o Acknowledge from DP to the Type-C assit block.
12	RO	0x0	grf_dp_hdcp22_rst_o DP HDCP22 reset output.
11	RO	0x0	grf_dp_aux_timeout_o DP aux transfer timeout indication.
10:7	RO	0x0	hdcp1_I_p0_gpio_in HDCP1 port0 GPIO input.
6:0	RO	0x00	reserved

VO1_GRF_SOC_ST1

Address: Operational Base(0x26036000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	grf_vo1_status1 Reflect the status of controller for the debug purpose. More details is in the DPTX chapter.

VO1_GRF_SOC_ST2

Address: Operational Base(0x26036000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RO	0x0	hdcp1_glb_gpio_out HDCP1 global GPIO output.
25:0	RO	0x0000000	dptx_dbg_o DPTX_debug_o[57:32]

VO1_GRF_HDCP1_RNG_CON0

Address: Operational Base(0x26036000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable. 1'b9: Write access enable.
15:2	RO	0x0000	reserved
1	RW	0x0	trng_I_ctrl_reseed Enable HDCP1_RNG reseed operation. 1'b0: Disable 1'b1: Enable When it is asserted, the HDCP1_RNG responds by stopping any reseed operation that is currently underway and initiating a new reseed operation.
0	RW	0x0	trng_I_ctrl_zeroize Enable HDCP1_RNG zeroize operation. 1'b0: Disable 1'b1: Enable

VO1_GRF_HDCP1_RNG_ST0

Address: Operational Base(0x26036000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	trng_O_ctrl_secure HDCP1_RNG secure mode output. 1'b0: Inactive 1'b1: Active
4	RO	0x0	trng_O_ctrl_reminder HDCP1_RNG reseed reminder output. 1'b0: Inactive 1'b1: Active
3	RO	0x0	trng_O_ctrl_reseeding HDCP1_RNG reseeding activity output. 1'b0: Inactive 1'b1: Active
2	RO	0x0	trng_O_ctrl_seeded HDCP1_RNG reseeding/seeding completion output. 1'b0: Inactive 1'b1: Active
1	RO	0x0	trng_O_ctrl_rand_bit HDCP1_RNG serial random bit output. 1'b0: Inactive 1'b1: Active
0	RO	0x0	trng_O_ctrl_rand_vld HDCP1_RNG serial random bit valid output. 1'b0: Inactive 1'b1: Active

5.18 VOP_GRF Register Description

5.18.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VOP_GRF_SOC_CON1	0x0004	W	0x00001410	Video output control register 1
VOP_GRF_SOC_CON2	0x0008	W	0x10110010	Video output control register 2
VOP_GRF_SOC_CON3	0x000C	W	0x00000080	Video output control register 3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

Double WORD (64 bits) access

5.18.2 Detail Registers Description

VOP_GRF_SOC_CON1

Address: Operational Base(0x26022000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x1410	grf_con_vop_mem_cfg_hdsprf Interface configuration for HDSPRF type memory in PD_VOP. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMD Bit[7]: LS Bit[11:10]: WPULSE Bit[13:12]: RA Other bits: Reserved

VOP_GRF_SOC_CON2

Address: Operational Base(0x26022000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	grf_con_vop_mem_cfg0_uhdpdpprf Interface configuration for UHDPDPPRF type memory in PD_VOP. Bit[0]: TEST1 Bit[1]: TEST_RNM Bit[4:2]: RM Bit[5]: WMDA Bit[7]: LS Other bits: Reserved
23:0	RW	0x110010	grf_con_vop_mem_cfg_hsdprf Interface configuration for HSDPRF type memory in PD_VOP. Bit[0]: TEST1A Bit[1]: TEST_RNMA Bit[5:2]: RMA Bit[6]: WMDA Bit[8]: LS Bit[17]: TEST1B Bit[21:18]: RMB Other bits: Reserved

VOP_GRF_SOC_CON3

Address: Operational Base(0x26022000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x080	grf_con_vop_mem_cfg1_uhdpdpprf Interface configuration for UHDPDPPRF type memory in PD_VOP. Bit[8]: TESTRWM Other bits: Reserved

5.19 COMBO_PIPE_PHY_GRF Register Description

5.19.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
COMBO_PIPE_PHY0_GRF	0x26028000

Name	Base Address
COMBO_PIPE_PHY1_GRF	0x2602A000

5.19.2 Registers Summary

Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_GRF_PIPE_CON0	0x0000	W	0x00000110	PIPE Combo PHY Configuration Register 0
COMBO_PIPE_PHY_GRF_PIPE_CON1	0x0004	W	0x00000000	PIPE Combo PHY Configuration Register 1
COMBO_PIPE_PHY_GRF_PIPE_CON2	0x0008	W	0x00009401	PIPE Combo PHY Configuration Register 2
COMBO_PIPE_PHY_GRF_PIPE_CON3	0x000C	W	0x00000000	PIPE Combo PHY Configuration Register 3
COMBO_PIPE_PHY_GRF_PIPE_CON4	0x0010	W	0x00000000	PIPE Combo PHY Configuration Register 4
COMBO_PIPE_PHY_GRF_PIPE_STATUS1	0x0034	W	0x000000C0	PIPE Combo PHY Status Register1
COMBO_PIPE_PHY_GRF_LFPS_DET_CON	0x0080	W	0x00000009	PIPE Combo PHY LFPS Detect Control Register
COMBO_PIPE_PHY_GRF_PHY_INT_EN	0x00A0	W	0x00000000	PIPE Combo PHY Interrupt Signal Enable
COMBO_PIPE_PHY_GRF_PHY_INT_STATUS	0x00A4	W	0x00000000	PIPE Combo PHY Interrupt Status

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.19.3 Detail Registers Description

COMBO_PIPE_PHY_GRF_PIPE_CON0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pipe_rxstandby SATA mode Controls whether the PHY RX is active when the PHY is in any power state with PCLK on. RX_STANDBY is ignored when the PHY is in any power state where the high-speed receiver is always off. 1'b0: Active 1'b1: Standby PCIe mode Controls whether the PHY RX is active when the PHY is in P0 or P0s. RX_STANDBY is ignored when the PHY is in P1 or P2 1'b0: Active 1'b1: Standby Only used in SATA and PCIe mode. USB3.0 mode should be tied to 1'b0. The value when override enable is selected.
13	RW	0x0	pipe_rxelecidle_disable RX electrical idle detect disable. The value when override enable is selected. 1'b0: Idle detect enable 1'b1: Idle detect disable

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Bit	Attr	Reset Value	Description
12	RW	0x0	pipe_rxterm Control presence of receiver terminations. The value when override enable is selected. 1'b0: Termination removed 1'b1: Termination present Only used in USB3.0 mode, PCIe and SATA mode should be tied to 1'b1.
11	RW	0x0	pipe_bypass_codec PCIe mode, USB mode, and SATA mode. The value when override enable is selected. Controls whether the PHY performs 8b/10b encode and decode. 1'b0: 8b/10b encode/decode performed normally by the PHY 1'b1: 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2'b01 It should be tie to 1'b1 in SATA low latency and SERDES mode.
10	RW	0x0	pipe_ebuffmode RX Elasticity Buffer operating mode selection. The value when override enable is selected. 1'b0: Nominal half-full buffer mode 1'b1: Nominal empty buffer mode In SATA and USB3.0 mode, when RX elastic buffer is operating at nominal empty buffer mode, RX_DATA_VALID is de-asserted which means elastic buffer is empty and no data is available. In PCIe mode, only nominal half-full Elasticity Buffer mode is supported.
9	RW	0x0	pipe_l1sub_entreq In PCIe mode L1 sub-state entry request signal in PCIe mode. When set to high, it instructs PHY to do power transition to L1 sub-state. In SATA Mode When set to high, it will be power down PLL. This signal could be connected to the L1 sub-state enable/request signal from controller Only used in PCIe and SATA mode, USB mode should be tied to 1'b0. The value when override enable is selected. Reserved for current chip.
8	RW	0x1	pipe_mac_pclkreq_n PCIe common clock request signal in PCIe mode. The signal shall be low and CKREF_SRC[1:0] is set to 2'b10 when CKREFP/N and PCI_100M_CLK output from PHY is used for PCIe system with common clock Note: Details refer to CKREFP/N and PCI_100M_CLK. Only used in PCIe mode, USB and SATA mode should be tied to 1'b1. This bit is a override bit for input CLKREQ for PHY when override selection enable.

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	pipe_powerdown Power up or power down status control of Transceiver. If PIPE PHY support PIPE4.3, the powerdown is 4-bit, PIPE4.2 or below 2-bit. This filed is powerdown [1:0], powerdown[3:2] is controlled by pipe_powerdown_4p3. The value when override enable is selected. In PCIe mode 4'h0: P0, normal mode 4'h1: P0s, low recovery time latency, power saving state 4'h2: P1, longer recovery time latency, lower power saving 4'h3: P2, lowest power state 4'h4: P1.CPM 4'h5: P1.1 4'hc: P1.2 Others: Reserved In USB3.0 mode 4'h0: P0, normal mode 4'h1: P1, low recovery time latency, power saving state 4'h2: P2, longer recovery time latency, lower power saving 4'h3: P3, lowest power state Others: Reserved In SATA and Serdes mode 4'h0: POWER_STATE_0 operational state, PHY normal operation 4'h1: PCLK on, TX common mode on 4'h3: PCLK on, TX common mode off 4'h5: PCLK off, TX common mode on 4'h7: PCLK off, TX common mode off Others: Reserved
5:4	RW	0x1	pipe_rate Combo PHY link signaling rate. The value when override enable is selected. In PCIe mode 2'b00: 2.5GT/s 2'b01: 5.0GT/s Others: Reserved In USB3.0 mode 2'b00: 5GT/s Others: Reserved In SATA mode 2'b00: 1.5GT/s 2'b01: 3.0GT/s 2'b10: 6.0GT/s 2'b11: Reserved In SERDES(QSGMII/SGMII) mode 2'b00: 1.25Gbps 2'b01: Reserved 2'b10: 5.0Gbps 2'b11: Reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	pipe_phymode Combo PHY mode. 2'b00: PCIe 2'b01: USB3 2'b10: SATA 2'b11: Serdes
1:0	RW	0x0	pipe_databuswidth Combo PHY PIPE data bus width. The value when override enable is selected. 2'b00: 32-bit, PCIe and USB3 only support 32-bit 2'b01: Reserved 2'b10: Reserved 2'b11: Reserved

COMBO_PIPE_PHY_GRF_PIPE_CON1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x0	phy_clk_sel Combo Phy PIPE reference clock frequency selection. 2'b00: 24M 2'b01: 25M 2'b10: 100M 2'b11: Reserved
12:11	RW	0x0	pipe_txpattern_sata Controls which pattern the PHY sends at the Gen 1 rate when sending OOB or initialization signaling. The PHY transmits this pattern at the Gen 1 rate regardless of what rate the PHY is configured at. Used in SATA mode only. The value when override enable is selected. 2'b00: C ALIGN 2'b01: C D24.3 2'b10: C D10.2 2'b11: C Reserved
10:8	RW	0x0	pipe_txmargin Transmit margin control, combined with txswing to control TX output amplitude. The value when override enable is selected.
7:6	RW	0x0	pipe_txdeemph Transmitter de-emphasis level configuration. The value when override enable is selected. 2'b00: -6dB 2'b01: -3.5dB 2'b10: No de-emphasis 2'b11: Reserved
5	RW	0x0	pipe_txswing Control transmitter voltage swing level. The value when override enable is selected. 1'b0: Full swing 1'b1: Low swing

Bit	Attr	Reset Value	Description
4	RW	0x0	pipe_txcompliance Set the running disparity to negative. Only used in PCIe mode, USB and SATA mode should be tied to 1'b0. The value when override enable is selected.
3	RW	0x0	pipe_txcommonmode_disable TX Common mode Control. 1'b0: Enable 1'b1: Disable The value when override enable is selected.
2	RW	0x0	pipe_txoneszeros This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8. When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA. Only used in USB mode, PCIE and SATA mode should be tied to 1'b0. The value when override enable is selected.
1	RW	0x0	pipe_txelecidle Forces TX output to electrical idle when asserted except in loopback, refer to PIPE spec for details on control signal usage. When asserted with TX_COMPLIANCE high, the PHY is fully powered off. Shall be kept high when SATA mode that is not in P0. The value when override enable is selected.
0	RW	0x0	pipe_txdectrx_loopback Used to tell the PHY to begin a receiver detection operation or to begin loopback. Refer to s PIPE spec for detail description. This signal shall be set to low when SATA mode that is not in P0. The value when override enable is selected.

COMBO_PIPE_PHY_GRF_PIPE_CON2

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	sel_pipe_txcompliance pipe_txcompliance selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
14	RW	0x0	sel_pipe_txcommonmode_disable pipe_txcommonmode_disable selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
13	RW	0x0	sel_pipe_txoneszeros pipe_txoneszeros selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

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Bit	Attr	Reset Value	Description
12	RW	0x1	sel_pipe_txelecidle pipe_txelecidle selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
11	RW	0x0	sel_pipe_txdectrx_loopback pipe_txdectrx_loopback selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
10	RW	0x1	sel_pipe_rxstandby sel_pipe_rxstandby selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
9	RW	0x0	sel_pipe_rxelecidle_disable pipe_rxelecidle_disable selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
8	RW	0x0	sel_pipe_rxterm pipe_rxterm selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
7	RW	0x0	sel_pipe_bypass_codec pipe_bypass_codec selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
6	RW	0x0	sel_pipe_ebuffmode pipe_ebuffmode selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
5	RW	0x0	sel_pipe_l1sub_entreq pipe_l1sub_entreq selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF Reserved
4	RW	0x0	sel_pipe_powerdown pipe_powerdown selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
3	RW	0x0	sel_pipe_mac_pclkreq_n pipe_mac_pclkreq_n selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
2	RW	0x0	sel_pipe_rate pipe_rate selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

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Bit	Attr	Reset Value	Description
1	RW	0x0	sel_pipe_phymode pipe_phymode selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF Reserved
0	RW	0x1	sel_pipe_databuswidth pipe_databuswidth selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

COMBO_PIPE_PHY_GRF_PIPE_CON3

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	qsgm_mode QSGMII mode enable. 1'b0: Other mode 1'b1: QSGMII/SGMII mode Reserved in this chip
14:13	RW	0x0	pipe_sel Reserved
12	RO	0x0	reserved
11	RW	0x0	sel_clkreq CLKREQ for PIPE PHY source selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side(Controller/Constant/PD GRF/PHY GRF) 1'b1: From GPIO mux for CLKREQ_N Because the CLKREQ is valid when high, so the pipe_mac_pclkreq_n should set to "0" when sel_pipe_mac_pclkreq_n is set to "1".
10	RW	0x0	sel_rxelecidle Rxelecidle to controller source selection. Override value is selected for PIPE PHY interface. 1'b0: From PIPE PHY 1'b1: When rxelecidle_disable is high, rxelecidle return "1" to controller
9:8	RW	0x0	phy_clk_ref_src Combo PHY PIPE reference clock source selection. 2'b00: Use PLL_CKREF_INNER as reference clock source, CKREFP/N is not active, the PAD can be floating 2'b01: Use CKREFP/N as input reference clock source 2'b10: Use PLL_CKREF_INNER (From SoC CRU) as reference clock source, Use CKREFP/N as output clock to provide a differential 100M reference clock in PCIe mode while PIPE PHY CLKREQ is high. 2'b11: Not allowed
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	sel_pipe_txpattern_sata pipe_txpattern_sata selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
2	RW	0x0	sel_pipe_txmargin pipe_txmargin selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
1	RW	0x0	sel_pipe_txdeemph pipe_txdeemph selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
0	RW	0x0	sel_pipe_txswing pipe_txswing selection. Override value is selected select for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

COMBO_PIPE_PHY_GRF_PIPE_CON4

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pipe_txdeemph_ext Extra direct control the txdeemph bit3.
7:4	RW	0x0	bist_mode BIST mode test in normal operation. 4'h0: PHY Normal operation, default value of BIST_MODE 4'h8: PHY external BIST from TXP/TXN to RXP/RXN 4'h9: PHY internal BIST 4'ha: PHY send 1'b0 on TXP and 1'b1 on TXN (only for VOL test) 4'hc: PHY send 1'b1 on TXP and 1'b0 on TXN (only for VOH test) 4'he: PHY send D10.2 (only for Eye-Diagram test) Others: Reserved
3:2	RW	0x0	serdes_arch This signal indicates whether Serdes architecture and SATA low latency is enabled. 2'b00: PCIe/USB/SATA normal working 2'b01: Used for SATA SAPIS compliant controller, that bypass PHY elastic buffer to reduce latency, RX_DATA is the result of comma align. 2'b10: General serdes mode and RX_DATA is the result of CDR in PMA 2'b11: General serdes mode and RX_DATA is the result of comma align
1:0	RW	0x0	pipe_powerdown_4p3 For PIPE4.3 interface, the powerdown are 4 bit, the field is for powerdown[3:2]. Override value when override enable is selected.

COMBO_PIPE_PHY_GRF_PIPE_STATUS1

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	pipe_clkreq_n Indicates that the PHY is in corresponding state to L1-sub-state in PCIE mode, during which PHY reference clock could be turned off. This signal could connect to corresponding signal in controller IP, if applicable.
8	RO	0x0	pipe_power_presetn Reserved
7	RO	0x1	pipe_rxelecidle_o Indicates receiver detection of an electrical idle. When de-asserted with the PHY in P2 (PCIE Mode), indicates a detection of beacon, while indicate exit from electrical idle in other power states in PCIe mode. In USB3.0 mode, it indicates the detection of LFPS. In SATA mode, it indicates if there is no data/OOB received.
6	RO	0x1	pipe_phystatus_o Used to communicate completion of several PHY functions including power management state transitions, rate change and receiver detection.
5:3	RO	0x0	pipe_rxstatus_o PIPE PHY receiver status. Encode receiver status and error codes for the received data stream when receiving data. 3'b000: Received data OK 3'b001: PCIe mode, 1 SKP added; USB mode: 1 SKP added; SATA mode: 1 ALIGN added Asseted width first byte of Align that was added 3'b010: PCIe mode: 1 SKP Ordered set removed; 1 SKP Ordered Set removed; SATA mode: 1 or more ALIGNs 3'b011: PCIe and USB mode: Receiver detected 3'b100: 8B/10B decode error 3'b101: Elastic buffer overflow 3'b110: Elastic buffer under flow, this error code is not used if the elastic buffer is operating in the nominal buffer empty mode 3'b111: Receive disparity error, overwritten by decode error
2:0	RO	0x0	reserved

COMBO_PIPE_PHY_GRF_LFPS_DET_CON

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x09	lfps_detect_con LFPS Detect Count Filter Control. This counter determines whether a rxelecidle (high pulse) is valid or not. The counter is based on Combo PIPE PHY APB PCLK.

COMBO_PIPE_PHY_GRF_PHY_INT_EN

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	rxelecidle_l0_fall_irq_en rxelecidle_l0_fall irq enable. 1'b0: IRQ disable 1'b1: IRQ enable

COMBO_PIPE_PHY_GRF_PHY_INT_STATUS

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	rxelecidle_l0_fall_irq_st rxelecidle_l0_fall irq status. 1'b0: Interrupt inactive 1'b1: Interrupt active

5.20 USBDPPHY_GRF Register Description

5.20.1 Registers Summary

Name	Offset	Size	Reset Value	Description
USBDPPHY_GRF_CON1	0x0004	W	0x00000000	USBDPPHY Control Register 1
USBDPPHY_GRF_CON2	0x0008	W	0x00000000	USBDPPHY Control Register 2
USBDPPHY_GRF_CON3	0x000C	W	0x00000000	USBDPPHY Control Register 3
USBDPPHY_GRF_STATUS1	0x0084	W	0x00000000	USBDPPHY Status Register
USBDPPHY_GRF_LFPS_DET_CON	0x00C0	W	0x00000009	LFPS Detect Control
USBDPPHY_GRF_INT_EN	0x00C4	W	0x00000000	Interrupt Enable Register
USBDPPHY_GRF_INT_STATUS	0x00C8	W	0x00000000	Interrupt Status Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.20.2 Detail Registers Description

USBDPPHY_GRF_CON1

Address: Operational Base(0x2602C000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	rx_lfps_en Enable RX LFPS Detector Block. 1'b1: RX SQ enable 1'b0: RX SQ disable
13	RW	0x0	usbdp_low_pwrn Used for the PMA power off function. 1'b0: PMA block power off 1'b1: PMA block power on
12:0	RO	0x0000	reserved

USBDPPHY_GRF_CON2

Address: Operational Base(0x2602C000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	phy_clamp 1'b0: Normal mode 1'b1: Clamp PHY output before PHY power off

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	debug_clock_sel Select phy debug clock output. 2'b00: o_vcoclk_div40_mon 2'b01: o_dbg_clk 2'b10: o_dp_txclk 2'b11: o_vcoclk_div40_mon
12	RW	0x0	debug_clk_gate_disable 1'b0: Gate phy debug clock output 1'b1: Do not gate phy debug clock output
11:0	RO	0x000	reserved

USBDPPHY_GRF_CON3

Address: Operational Base(0x2602C000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	soft_pipe3_txdetectrxloopbk When USBDPPHY_GRF_CON3[0] is 1'b1, tx_detectrx_loopback is controlled by this bit.
4:3	RW	0x0	soft_pipe3_powerdown When USBDPPHY_GRF_CON3[0] is 1'b1, powerdown is controlled by this bit.
2	RW	0x0	soft_pipe3_txelecidle When USBDPPHY_GRF_CON3[0] is 1'b1, tx_elecidle is controlled by this bit.
1	RW	0x0	soft_pipe3_rxtermination When USBDPPHY_GRF_CON3[0] is 1'b1, rx_termination is controlled by this bit.
0	RW	0x0	grf_control_sel 1'b0: Normal mode 1'b1: rx_termination , tx_elecidle, powerdown, tx_detectrx_loopback are controlled by software through GRF

USBDPPHY_GRF_STATUS1

Address: Operational Base(0x2602C000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:22	RO	0x0	pipe_rxstatus Encodes receiver status and error codes for the received data stream when receiving data.
21	RO	0x0	pipe_rxelecidle Indicates receiver detection of an electrical idle. While deasserted with the PHY in P2, indicates detection of a beacon.
20	RO	0x0	pipe_phy_status Used to communicate completion of several PHY functions including power management state transitions, rate change, and receiver detection.
19	RO	0x0	pll_lock_done PLL Lock Indication. This bit is high when PLL Locking is complete.
18:0	RO	0x00000	reserved

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USBDPPHY_GRF_LFPS_DET_CON

Address: Operational Base(0x2602C000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x09	lfps_detect_con LFPS filter counter control

USBDPPHY_GRF_INT_EN

Address: Operational Base(0x2602C000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	lfps_l0_beacon_int_en Beacon interrupt enable. 1'b0: Interrupt disable 1'b1: Interrupt enable

USBDPPHY_GRF_INT_STATUS

Address: Operational Base(0x2602C000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	lfps_l0_beacon_int_status Beacon interrupt status. Write 1 to this bit will clear the interrupt

5.21 USB2PHY_GRF Register Description

5.21.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
USB2PHY0_GRF	0x2602E000
USB2PHY1_GRF	0x26030000

5.21.2 Registers Summary

Name	Offset	Size	Reset Value	Description
USB2PHY_GRF_CON0	0x0000	W	0x00008C52	USB2PHY Control Register 0
USB2PHY_GRF_CON1	0x0004	W	0x00000002	USB2PHY Control Register 1
USB2PHY_GRF_CON2	0x0008	W	0x00007066	USB2PHY Control Register 2
USB2PHY_GRF_CON3	0x000C	W	0x00007633	USB2PHY Control Register 3
USB2PHY_GRF_CON4	0x0010	W	0x00000D00	USB2PHY Control Register 4
USB2PHY_GRF_CON5	0x0014	W	0x00002200	USB2PHY Control Register 5
USB2PHY_GRF_LS_CON	0x0020	W	0x00030100	USB2PHY linestate filter control register
USB2PHY_GRF_DIS_CON	0x0024	W	0x00030100	USB2PHY Disconnect Filter Control Register
USB2PHY_GRF_BVALID_CON	0x0028	W	0x00030100	USB2PHY BValid Filter Control Register
USB2PHY_GRF_ID_CON	0x002C	W	0x00030100	USB2PHY ID Filter Control Register
USB2PHY_GRF_VBUSVALID_CON	0x0030	W	0x00030100	USB2PHY VbusValid Filter Control Register
USB2PHY_GRF_DBG_CON0	0x0040	W	0x00000000	USB Debug Mode Contol Register

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Name	Offset	Size	Reset Value	Description
USB2PHY_GRF_LINEST_TIMEOUT	0x0044	W	0x00000000	USB Debug Mode Timeout Register
USB2PHY_GRF_LINEST_DEB	0x0048	W	0x00000000	USB Debug Mode Debounce Register
USB2PHY_GRF_RX_TIMEOUT	0x004C	W	0x00000000	UART RX Down Counter Register
USB2PHY_GRF_SEQ_LIMT	0x0050	W	0x00000000	Handshake Sequence Counter Control Register
USB2PHY_GRF_LINEST_CNT_ST	0x0054	W	0x00000000	Linestate Conter For Debug Register
USB2PHY_GRF_DBG_ST	0x0058	W	0x00000000	Debug State Register
USB2PHY_GRF_RX_CNT_ST	0x005C	W	0x00000000	RX Counter Register
USB2PHY_GRF_ST0	0x0080	W	0x00000000	Status Register 0
USB2PHY_GRF_INT_EN	0x00C0	W	0x00000000	Interrupt Enable Register
USB2PHY_GRF_INT_ST	0x00C4	W	0x00000000	Interrupt Status Register
USB2PHY_GRF_INT_ST_CLR	0x00C8	W	0x00000000	Interrupt Clear Register
USB2PHY_GRF_DETCLK_SEL	0x00D0	W	0x00000000	Detect Clock Select Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.21.3 Detail Registers Description

USB2PHY_GRF_CON0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	soft_vbusvalid_bvalid When soft_vbusvalid_sel is 1'b1, vbusvalid and bvalid is controlled by soft_vbus.
14	RW	0x0	soft_vbusvalid_bvalid_sel VBUS/Bvalid valid software control select.
13:12	RO	0x0	reserved
11	RW	0x1	soft_utmi_idpullup Pull-up enable control for IDDIG pin. High valid.
10	RW	0x1	soft_utmi_iddig When soft_iddig_sel is 1'b1, IDDIG is controlled by soft_utmi_iddig.
9	RW	0x0	soft_iddig_sel IDDIG select 1'b0: Select iddig output from PHY. 1'b1: Select soft_utmi_iddig.
8	RW	0x0	soft_utmi_dmpulldown When soft_con_sel is 1'b1, dmpulldown is controlled by soft_utmi_dmpulldown.
7	RW	0x0	soft_utmi_dppulldown When soft_con_sel is 1'b1, dppulldown is controlled by soft_utmi_dppulldown.

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Bit	Attr	Reset Value	Description
6	RW	0x1	soft_utmi_termselect When soft_con_sel is 1'b1, termselect is controlled by soft_utmi_termselect.
5:4	RW	0x1	soft_utmi_xcvrselect When soft_con_sel is 1'b1, xcvrselect is controlled by soft_utmi_xcvrselect.
3:2	RW	0x0	soft_utmi_opmode When soft_con_sel is 1'b1, opmode is controlled by soft_utmi_opmode.
1	RW	0x1	soft_utmi_suspendn When soft_con_sel is 1'b1, suspendn is controlled by soft_utmi_suspendn.
0	RW	0x0	soft_con_sel Soft control select Bit.

USB2PHY_GRF_CON1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	drvvbus This bit only be used when field drvvbus_sel high
8	RW	0x0	drvvbus_sel When this bit set to 1'b1, use field drvvbus to control.
7:3	RO	0x00	reserved
2:0	RW	0x2	fsel Reference Clock Frequency Select Selects the USB 2.0 femtoPHY reference clock frequency. For information on supported reference clock frequencies and the required FSEL[2:0] settings. 3’b010: 24Mhz 3’b110: 26Mhz

USB2PHY_GRF_CON2

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	port_reset Per-Port Reset When asserted, this signal resets the corresponding port's transmit and receive logic without disabling the clocks within the USB 2.0 PHY. 1'b1: The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. 1'b0: The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK0 cycles.

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Bit	Attr	Reset Value	Description
14	RW	0x1	pllbtune PLL Bandwidth adjustment This adjustment doubles the bandwidth of the PLL as needed for some input reference clock frequencies. Set this to 1'b1 for all 24Mhz and 26Mhz reference clock.
13:10	RW	0xc	pllptune PLL Proportional Path Tune This signal should be set to the Design default. 4'b1111: 4.75x 4'b1110: 4.50x 4'b1101: 4.25x 4'b1100: 4.00x, Design default 4'b1011: 3.75x 4'b1010: 3.50x 4'b1001: 3.25x 4'b1000: 3.00x 4'b0111: 2.75x 4'b0110: 2.50x 4'b0101: 2.25x 4'b0100: 2.00x 4'b0011: 1.75x 4'b0010: 1.50x 4'b0001: 1.25x 4'b0000: 1.00x
9:8	RW	0x0	pllitune PLL Integral Path Tune This signal should be set to the Design default. 2'b11: 2.0x 2'b10: 1.5x 2'b01: 1.0x 2'b00: 0.5x, Design
7:5	RW	0x3	tune VBUS Valid Threshold Adjustment This bus adjusts the voltage level for the VBUS Valid threshold. 3'b111: +12.59% 3'b110: +9.63% 3'b101: +6.42% 3'b100: +3.21% 3'b011: 0, Design default 3'b010: -2.96% 3'b001: -6.17% 3'b000: -9.38%
4	RW	0x0	disable OTG Block Disable This signal powers down the VBUS Valid comparator, but not the Session Valid comparator, nor the ID detection circuitry. To save power, if the application does not use the OTG function, this input can be set high. 1'b1: The OTG block is powered down. 1'b0: The OTG block is powered up.

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Bit	Attr	Reset Value	Description
3:1	RW	0x3	compdistune Disconnect Threshold Adjustment This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 3'b111: +15.20% 3'b110: +11.15% 3'b101: +7.05% 3'b100: +3.59% 3'b011: 0 3'b010: -2.94% 3'b001: -5.96% 3'b000: -8.58%
0	RW	0x0	common_on_n Common Block Power-Down Control This signal controls the power-down signals in the REFCLK_LOGIC, Bias, and PLL blocks when the USB 2.0 PHY is in Suspend, or Sleep mode. 1'b1: In Suspend mode, the REFCLK_LOGIC, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. 1'b0: In Suspend or Sleep modes, the REFCLK_LOGIC, Bias, and PLL blocks remain powered. With this setting, the input reference clock must remain on and valid during suspend or sleep.

USB2PHY_GRF_CON3

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	txrisetune HS Transmitter Rise/Fall Time Adjustment This bus adjusts the rise/fall times of the high-speed waveform. 2'b11: -3.24% 2'b10: -1.33% 2'b01: 0, Design default 2'b00: +2.19%
13:12	RW	0x3	txhsxvtune Transmitter High-Speed Crossover Adjustment This bus adjusts the voltage at which the DP0 and DM0 signals cross while transmitting in HS mode. 2'b11: 0, Default setting 2'b10: +11.05 mV 2'b01: -9.2 mV 2'b00: +0.67 mV

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Bit	Attr	Reset Value	Description
11:8	RW	0x6	txvreftune HS DC Voltage Level Adjustment This bus adjusts the high-speed DC level voltage. 4'b1111: +21.58% 4'b1110: +17.66% 4'b1101: +13.74% 4'b1100: +11.78% 4'b1011: +9.81% 4'b1010: +7.85% 4'b1001: +5.89% 4'b1000: +3.92% 4'b0111: +1.96% 4'b0110: 0, Design default 4'b0101: -1.96% 4'b0100: -3.92% 4'b0011: -5.89% 4'b0010: -7.85% 4'b0001: -9.81% 4'b0000: -13.73%
7:4	RW	0x3	txfslstune This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 4'b1111: -10.33% 4'b0111: -5.49% 4'b0011: 0, Design default 4'b0001: +6.34% 4'b0000: +13.63% All other bit settings are reserved.
3	RW	0x0	txpreemppulsetune This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. The HS Transmitter pre_emphasis duration is defined in terms of unit amounts. One unit of pre- emphasis duration is approximately 580 ps and is defined as 1X pre- emphasis duration. 1'b1: 1x, short pre-emphasis current duration 1'b0 (design default): 2x, long pre-emphasis current duration
2:0	RW	0x3	sqrxtune Squelch Threshold Adjustment This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 3'b111: -21.12% 3'b110: -15.93% 3'b101: -10.53% 3'b100: -5.41% 3'b011: 0, Design default 3'b010: +5.14% 3'b001: +10.51% 3'b000: +15.68%

USB2PHY_GRF_CON4

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	dcdenb Enhanced Data Contact Detection Enable Enables current sourcing on the D+ line. For special applications, the IDP_SRC control and the RDM_DWN control are separated. For standard DCD operation in accordance with the Battery Charger v1.2 specification, simultaneously set DCDENB0=1'b1 (to enable IDP_SRC) and set DMPULLDOWN0=1'b1 (to enable RDM_DWN). Set both signals to 1'b0 when DCD is completed. 1'b1: IDP_SRC current is sourced onto DP0 1'b0: IDP_SRC current is disabled
13	RW	0x0	siddq IDDQ Test Enable This test signal enables you to perform IDDQ testing by powering down all analog blocks. Before asserting SIDDQ, ensure that TESTBURNIN is set to 1'b0, and RETENABLEN is set to 1'b1. 1'b1: The analog blocks are powered down. 1'b0: The analog blocks are powered up.
12:11	RW	0x1	txrestune USB Source Impedance Adjustment In some applications, there can be significant series resistance on the D+ and D- paths between the transceiver and cable. This bus adjusts the driver source impedance to compensate for added series resistance on the USB. Note: Any setting other than the default can result in source impedance variation across process, voltage, and temperature conditions that does not meet USB 2.0 specification limits. 2'b11: Source impedance is decreased by approximately 4.74 ohm 2'b10: Source impedance is decreased by approximately 2.5 ohm 2'b01: 0, Design default 2'b00: Source impedance is increased by approximately 3.23 ohm If this bus is not used, leave it at the default setting.
10	RW	0x1	sleempm Sleep Assertion Asserting this signal places the USB 2.0 PHY in Sleep mode according to the USB 2.0 Link Power Management (LPM) addendum to the USB 2.0 specification. In Sleep mode, the transmitter is tri_stated and the USB 2.0 PHY circuits are powered down except for the REFCLK_LOGIC block. The REFCLK_LOGIC block remains powered when the USB 2.0 PHY is placed in Sleep mode. 1'b1: Normal operating mode 1'b0: Sleep mode
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x1	retenable_n Retention Mode Enable Retention mode allows the USB 2.0 PHY to retain internal digital core signal states when the PHY DVDD supply is lowered to a process specific retention voltage level. Retention mode also forces all internal DVDD-to-VDD18 level translators into a pre_defined state based on the PHY operating mode.
7	RW	0x0	vdatsrcenb Battery Charging Sourcing Select Enables or disables sourcing for battery charging. 1'b1: Data source voltage (VDAT_SRC) is enabled. 1'b0: Data source voltage (VDAT_SRC) is disabled.
6	RW	0x0	vdatdetenb Battery Charging Attach/Connect Detection Enable Enables or disables attach/connect detection. 1'b1: Data detect voltage (CHG_DET) is enabled. 1'b0: Data detect voltage (CHG_DET) is disabled.
5	RW	0x0	chrgsel Determines whether current is sourced onto or sunk from DP0 or DM0. The definitions shown below apply when CHRGSRCPUENB0[1:0]=2'b00. See CHRGSRCPUENB0[1:0] for other modes. 1'b1: Data source voltage (VDAT_SRC) is sourced onto DM0 and sunk from DP0. 1'b0: Data source voltage (VDAT_SRC) is sourced onto DP0 and sunk from DM0.
4:3	RW	0x0	txpreempamptune HS Transmitter Pre-Emphasis Current Control This signal controls the amount of current sourced to DP0 and DM0 after a J-to-K or K-to-J transition. The HS Transmitter pre-emphasis current is defined in terms of unit amounts. One unit amount is approximately 2 mA and is defined as 1X pre-emphasis current. 2'b11: HS Transmitter pre-emphasis circuit sources 3x pre-emphasis current. 2'b10: HS Transmitter pre-emphasis circuit sources 2x pre-emphasis current. 2'b01: HS Transmitter pre-emphasis circuit sources 1x pre-emphasis current. 2'b00 (design default): HS Transmitter pre-emphasis is disabled.
2	RO	0x0	reserved
1	RW	0x0	vbusvldextsel External VBUS Valid Select This signal selects either the VBUSVLDEXT0 input or the internal Session Valid comparator to detect whether the VBUS signal on the USB cable is valid and to assert the DP0 pull-up resistor. The activation of the DP0 pull-up resistor also depends on the state of XCVRSEL0[1:0], OPMODE0[1:0], TERMSEL0, DPPULLDOWN0, and DMPULLDOWN0. 1'b1: The VBUSVLDEXT0 input is used to assert the DP0 pull-up resistor. 1'b0: The internal Session Valid comparator is used to assert the DP0 pull-up resistor.

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Bit	Attr	Reset Value	Description
0	RW	0x0	vbusvldext External VBUS Valid Indicator This signal is valid in Device mode and only when the VBUSVLDEXTSEL0 signal is set to 1'b1. VBUSVLDEXT0 indicates whether the VBUS signal on the USB cable is valid. In addition, VBUSVLDEXT0 enables the pull-up resistor on the D+ line. VBUSVLDEXT0 does not change the OTGSESSVLD0 output. 1'b1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled. 1'b0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled. In Host mode, this input is not used and can be tied to 1'b0.

USB2PHY_GRF_CON5

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	fsxcvrowner UTMI+/Serial Interface Select This controller signal enables the UTMI+ or serial interface. 1'b1: The TXENABLEN0, FSDATAEXT0, and FSSE0EXT0 inputs drive USB 2.0 femtoPHY data output onto the D+ and D- lines. Data that the USB 2.0 femtoPHY receives from the D+ and Dlines appears on the FSVMINUS0 and FSVPLUS0 outputs. 1'b0: Data on the D+ and D- lines is transmitted and received through the UTMI+. If FSXCVROWNER0 is not used, set it to 1'b0.
13	RW	0x1	txenablen USB 1.1 Data Enable This controller signal enables the FSDATAEXT0 and FSSE0EXT0 inputs. TXENABLEN0 is valid only when the FSXCVROWNER0 signal is set to 1'b1. 1'b1: FSDATAEXT0 and FSSE0EXT0 are disabled. 1'b0: FSDATAEXT0 and FSSE0EXT0 are enabled. If TXENABLEN0 is not used, set it to 1'b1.
12	RW	0x0	fsse0ext USB 1.1 SE0 Generation This controller signal sets the USB to an SE0 state. This signal is valid only if FSXCVROWNER0 is set to 1'b1 and TXENABLEN0 is set to 1'b0. 1'b1: The D+ and D- lines are driven to an SE0 state. 1'b0: The D+ and D- line states are determined by FSDATAEXT0. If FSSE0EXT0 is not used, set it to 1'b0.
11	RW	0x0	fsdataext USB 1.1 Transmit Data This controller signal sets the USB to either a J or K state. This signal is valid only if FSXCVROWNER0 is set to 1'b1, TXENABLEN0 is set to 1'b0, and FSSE0EXT0 is set to 1'b0. 1'b1: The D+ and D- lines are driven to a Differential 1. 1'b0: The D+ and D- lines are driven to a Differential 0. If FSDATAEXT0 is not used, set it to 1'b0

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Bit	Attr	Reset Value	Description
10:9	RW	0x1	vdatreftune0 Data Detect Voltage Adjustment This bus adjusts the threshold voltage level (Vdat_ref) used to detect data during charger type detection. 2'b11: -19.8% 2'b10: -9.84% 2'b01: 0, Design default 2'b00: +9.93%
8	RW	0x0	hsxcvrextctl0 HS Transceiver Asynchronous Control This signal asynchronously selects the HS transceiver Tx/Rx path. This signal can be used with the bypass signals in "UART/Autoresume Signals" on page 50 to perform proprietary tests on the HS Tx / Rx paths. The PHY must be in an HS state with XCVRSEL0[1:0] = 2'b00 and TERMSEL0 = 1'b0. 1'b1: HS Tx/Rx path is selected 1'b0: FS Tx/Rx path is selected
7	RW	0x0	autorsmenb0 Autoresume Mode Enable Autoresume mode can be used when the USB 2.0 PHY is operating in a host role. This mode enables the autoresume logic in the PHY, so that the PHY will automatically respond to a remote wake-up resume-k from a peripheral, without initial involvement from the host controller. The PHY will respond to a remote wake-up resume-k by driving out its own resume-k. The PHY resume-k will be held until the host controller takes over and configures the PHY to continue driving the resume-k.
6	RW	0x0	bypasssel Transmitter Digital Bypass Select Enables/disables Transmitter Digital Bypass mode. The standard FS UART mode is selected by setting HSXCVREXTCTL0 = 1'b0, and a proprietary HS test mode is selected by setting HSXCVREXTCTL0 = 1'b1. 1'b1: Transmitter Digital Bypass mode is enabled. 1'b0: Transmitter Digital Bypass mode is disabled
5	RW	0x0	bypassdmen DM0 Transmitter Digital Bypass Enable Enables/disables the DM0 FS/LS driver (if HSXCVREXTCTL0 = 1'b0) in Transmitter Digital Bypass mode. FS mode is the standard UART mode. To use this mode,BYPASSSEL0 must be 1'b1. 1'b1: DM0 FS/LS driver (if HSXCVREXTCTL0 = 1'b0) is enabled and driven with the BYPASSDPDATA0 signal. 1'b0: DM0 FS/LS driver (if HSXCVREXTCTL0 = 1'b0) is disabled in Transmitter Digital Bypass mode.
4:0	RO	0x00	reserved

USB2PHY_GRF_LS_CON

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	linestate_filter_con Host/Otg port linestate filter time control register. Unit: PCLK or xin_osc(24MHz) selected by USB2PHY_GRF_DETCLK_SEL.

USB2PHY_GRF_DIS_CON

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	disconnect_filter_con Host/Otg port hostdisconnect filter time control register. Unit: PCLK or xin_osc(24MHz) selected by USB2PHY_GRF_DETCLK_SEL.

USB2PHY_GRF_BVALID_CON

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	bvalid_filter_con Otg port bvalid filter time control register. Unit: PCLK or xin_osc(24MHz) selected by USB2PHY_GRF_DETCLK_SEL.

USB2PHY_GRF_ID_CON

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0030100	id_filter_con Otg ID port filter time control register. Unit: PCLK or xin_osc(24MHz) selected by USB2PHY_GRF_DETCLK_SEL.

USB2PHY_GRF_VBUSVALID_CON

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x00000000	reserved
27:0	RW	0x00030100	vbusvalid_filter_con Otg port bvalid filter time control register. Unit: PCLK or xin_osc(24MHz) selected by USB2PHY_GRF_DETCLK_SEL.

USB2PHY_GRF_DBG_CON0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	exit_jtag If this bit set to 1'b1, USB debug for JTAG will exit. After exit please set this bit to 1'b0.
0	RW	0x0	usbdebug_en This bit will enable USB bypass mode for JTAG or UART. 1'b1: Enable 1'b0: Disable

USB2PHY_GRF_LINEST_TIMEOUT

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	linestate_timeout Timeout counter for linestate when use debug mode for JTAG or UART. Unit:32KHz

USB2PHY_GRF_LINEST_DEB

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	linestate_deb Linestate filter time control register when use debug mode for JTAG or UART. Unit:32KHz

USB2PHY_GRF_RX_TIMEOUT

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	rx_timeout UART debug timeout counter for RX pulldown. Unit:32KHz

USB2PHY_GRF_SEQ_LIMT

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	seq_limt Handshake counter number for SE0, SE1 sequence. Unit:32KHz

USB2PHY_GRF_LINEST_CNT_ST

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	linestate_counter The state of USB debug linestate counter.

USB2PHY_GRF_DBG_ST

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	fs_set When this bit is 1'b1, USB2PHY utmi is set to FS.
11	RO	0x0	bypass_set When this bit is 1'b1, USB2PHY is in bypass mode.
10	RO	0x0	jtag_mode Current mode is JTAG mode. 1'b0: Inactive 1'b1: Active
9	RO	0x0	uart_mode Current mode is UART mode. 1'b0: Inactive 1'b1: Active
8:6	RO	0x0	fsm_state The FSM state for debug.

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Bit	Attr	Reset Value	Description
5:2	RO	0x0	seq_cnt The SE0, SE1 sequence number.
1	RO	0x0	rx_down If this bit set to 1'b1, this mean UART RX is pulldown and will exit UART mode.
0	RO	0x0	st_timeout Timeout state. 1'b0: Inactive 1'b1: Active

USB2PHY_GRF_RX_CNT_ST

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rx_counter The state of UART debug timeout counter for RX pulldown.

USB2PHY_GRF_ST0

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	fslsrcv Differential Data Receive Indicator This controller signal indicates the state of differential data on the USB during normal operation.
12	RO	0x0	hsrxdat0 This signal asynchronously outputs the state of the HS receiver. This signal can be used with the bypass signals in "UART/Autoresume Signals" on page 50 to perform proprietary tests on the HS Rx block. The PHY must be in an HS state with XCVRSEL0[1:0] = 2'b00 and TERMSEL0 = 1'b0. HSXCVREXTCTL0 must be set to 1'b1 to use this mode. HSRXDAT0 is gated to 1'b0 if HSXCVREXTCTL0 = 1'b0. 1'b1: If HSXCVREXTCTL0 = 1'b1 and HSSQUELCH0 = 1'b0, the HS differential receiver has detected an HS J. 1'b0: If HSXCVREXTCTL0 = 1'b1 and HSSQUELCH0 = 1'b0, the HS differential receiver has detected an HS K.
11	RO	0x0	hssquelch0 HS Squelch Detector Asynchronous Output This signal asynchronously outputs the state of the HS squelch detector. This signal can be used with the bypass signals in "UART/ Autoresume Signals" on page 50 to perform proprietary tests on the HS Rx block. The PHY must be in an HS state with XCVRSEL[1:0] = 2'b00 and TERMSEL = 1'b0. HSXCVREXTCTL must be set to 1'b1 to use this mode. HSSQUELCH is gated to 1'b0 if HSXCVREXTCTL = 1'b0. 1'b1: If HSXCVREXTCTL = 1'b1, the HS squelch detector has not detected a valid HS VIL level. The line is squelched. 1'b0: If HSXCVREXTCTL = 1'b1, the HS squelch detector has detected a valid HS VIL level. The line is not squelched. The HSRXDAT signal indicates whether the detected signal is a J or a K.

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Bit	Attr	Reset Value	Description
10	RO	0x0	fsvminus Single-Ended D- Indicator This controller signal indicates the state of the D- line in normal operation. 1'b1: The voltage on D- is high. 1'b0: The voltage on D- is low
9	RO	0x0	fsvplus Single-Ended D+ Indicator This controller signal indicates the state of the D+ line during normal operation or UART data reception. 1'b1: The voltage on D+ is high. 1'b0: The voltage on D+ is low.
8	RO	0x0	chgdet Battery Charger Detection Output Indicates whether the voltage level on DP0 or DM0 is greater than VDAT_REF as defined in the Battery Charger specification. 1'b1: VDP > VDAT_REF (for CHRGSEL0 = 1'b1) or VDM > VDAT_REF (for CHRGSEL0 = 1'b0) 1'b0: VDP < VDAT_REF (for CHRGSEL0 = 1'b1) or VDM < VDAT_REF (for CHRGSEL0 = 1'b0)
7	RO	0x0	hostdisconnect Host Disconnect status 1'b0: connect 1'b1: disconnect
6	RO	0x0	utmi_iddig IDDIG status. 1'b0: Host 1'b1: Device
5:4	RO	0x0	utmi_linestate Line State Indicator This controller bus reflects the state of the single-ended receivers. In Suspend or Sleep mode, this bus is a combinatorial output (directly reflecting the current state of D- and D+, respectively). 11: SE1 (D+ high, D- high) 10: K state for high-speed and full-speed USB traffic; J state for low-speed USB traffic (D+ low, D- high) 01: J state for high-speed and full-speed USB traffic; K state for low-speed USB traffic (D+ high, D- low) 00: SE0 (D+ low, D- low)
3	RO	0x0	otgsessvld OTG Device Session Valid Indicator (Low Voltage) This controller signal is output from the USB 2.0 PHY's Session Valid comparator and indicates whether the voltage on VBUS is below the OTG Device Session Valid threshold. 1'b1: The voltage on VBUS is above the OTG Device Session Valid threshold. 1'b0: The voltage on VBUS is below the OTG Device Session Valid threshold.
2	RO	0x0	utmi_vbusvalid VBUS valid status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
1	RO	0x0	utmi_avalid VBUS avalid status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	utmi_bvalid VBUS bvalid status. 1'b0: Inactive 1'b1: Active

USB2PHY_GRF_INT_EN

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8:7	RW	0x0	vbusvalid_irq_en vbusvalid edge status irq enable 2'bx1: Vbusvalid rising edge interrupt request status enable 2'b1x: Vbusvalid falling edge interrupt request status enable
6:5	RW	0x0	disconnect_irq_en disconnect_irq edge status enable 2'bx1: Disconnect rising edge interrupt request status enable 2'b1x: Disconnect falling edge interrupt request status enable
4:3	RW	0x0	id_irq_en id edge status enable 2'bx1: ID rising edge interrupt request status enable 2'b1x: ID falling edge interrupt request status enable
2:1	RW	0x0	bvalid_irq_en bvalid edge status irq enable 2'bx1: Bvalid rising edge interrupt request status enable 2'b1x: Bvalid falling edge interrupt request status enable
0	RW	0x0	linestate_irq_en linestate change status interrupt request enable High valid.

USB2PHY_GRF_INT_ST

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:7	RW	0x0	vbusvalid_irq vbusvalid edge status 2'bx1: Vbusvalid rising edge interrupt request status 2'b1x: Vbusvalid falling edge interrupt request status
6:5	RO	0x0	disconnect_irq disconnect edge status 2'bx1: Disconnect rising edge interrupt request status 2'b1x: Disconnect falling edge interrupt request status
4:3	RO	0x0	id_irq id edge status 2'bx1: ID rising edge interrupt request status 2'b1x: ID falling edge interrupt request status

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Bit	Attr	Reset Value	Description
2:1	RO	0x0	bvalid_irq bvalid edge status status 2'bx1: Bvalid rising edge interrupt request status 2'b1x: Bvalid falling edge interrupt request status
0	RO	0x0	linestate_irq linestate change status interrupt request status

USB2PHY_GRF_INT_ST_CLR

Address: **Operational Base** + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
8:7	RW	0x0	vbusvalid_irq_clr vbusvalid edge status interrupt request status clear, write 1 to clear interrupt request status 2'bx1: Vbusvalid rising edge interrupt request status clear, write 1 to clear interrupt request status 2'b1x: Vbusvalid falling edge interrupt request status clear, write 1 to clear interrupt request status
6:5	WO	0x0	disconnect_irq_clr disconnect edge status clear, write 1 to clear interrupt request status 2'bx1: Disconnect rising edge interrupt request status clear, write 1 to clear interrupt request status 2'b1x: Disconnect falling edge interrupt request status clear, write 1 to clear interrupt request status
4:3	WO	0x0	id_irq_clr id edge status clear, write 1 to clear interrupt request status 2'bx1: ID rising edge interrupt request status clear, write 1 to clear interrupt request status 2'b1x: ID falling edge interrupt request status clear, write 1 to clear interrupt request status
2:1	WO	0x0	bvalid_irq_clr bvalid edge status interrupt request status clear, write 1 to clear interrupt request status 2'bx1: Bvalid rising edge interrupt request status clear, write 1 to clear interrupt request status 2'b1x: Bvalid falling edge interrupt request status clear, write 1 to clear interrupt request status
0	WO	0x0	linestate_irq_clr linestate change status interrupt request status clear, write 1 to clear interrupt request status

USB2PHY_GRF_DETCLK_SEL

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	detclk_sel When VD_LOGIC is powerdown and USB2PHY changed to PMU power, set this bit to 1'b1 can change the interrupt logic clock to OSC clock.

5.22 HDPTXPHY_GRF Register Description

5.22.1 Registers Summary

Name	Offset	Size	Reset Value	Description
HDPTXPHY_GRF_CON0	0x0000	W	0x00000000	HDPTXPHY Control Register 0
HDPTXPHY_GRF_CON1	0x0004	W	0x00000000	HDPTXPHY Control Register 1
HDPTXPHY_GRF_STATUS0	0x0080	W	0x00000000	HDPTXPHY Status Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.22.2 Detail Registers Description

HDPTXPHY_GRF_CON0

Address: Operational Base(0x26032000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	hdptxphy_clamp_en HDPTXPHY output clamp enable. 1'b0: Normal mode 1'b1: Clamp phy output before PHY power off
11:10	RW	0x0	ro_ref_clk_sel Input Reference Clock source selector. This pin controls reference clock source. 2'b00: Input reference clock from refclk_xtal 2'b01: Input reference clock from sideband IO. 2'b10: Input reference clock from LC PLL (cascade mode). 2'b11: Input reference clock from refclk_soc_pll (System PLL).
9:8	RW	0x0	lc_ref_clk_sel Input Reference Clock source selector. This pin controls reference clock source. 2'b00: Input reference clock from refclk_xtal 2'b01: Input reference clock from sideband IO. 2'b10: Input reference clock from RO PLL. 2'b11: Input reference clock from refclk_soc_pll (System PLL).
7	RW	0x0	pll_en PLL Block Enable Signal. 1'b0: Disable 1'b1: Enable
6	RW	0x0	bias_en Bias Block Enable Signal. 1'b0: Disable 1'b1: Enable
5	RW	0x0	bgr_en Band Gap Reference Block Enable Signal. 1'b0: Disable 1'b1: Enable
4	RW	0x0	tx_aux_tx_mode When hdptx_mode_sel is 1'b0, this bit controls the i_aux_tx_mode of PHY. Enables transmission in AUX mode. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	earc_rx_mode When hdptx_mode_sel is 1'b1, this bit controls the i_earc_rx_mode of PHY. Enables CMDC receiver in eARC mode. 1'b0: Disable 1'b1: Enable
2	RW	0x0	earc_tx_mode When hdptx_mode_sel is 1'b1, this bit controls the i_earc_tx_mode of PHY. Enables CMDC transmission in eARC mode. 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	hdptx_mode_sel 1'b0: earc_tx_mode/earc_rx_mode/aux_tx_mode is controlled by HDMITX controller 1'b1: earc_tx_mode/earc_rx_mode/aux_tx_mode is controlled by EDP controller or software.

HDPTXPHY_GRF_CON1

Address: Operational Base(0x26032000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	dbgclk_gate 1'b0: Gate debug clock. 1'b1: Do not gate debug clock.
6:4	RO	0x0	reserved
3:0	RW	0x0	dbgclk_sel Debug clock selection. 4'h0: hdptx_o_dig_refclk 4'h1: hdptx_o_mon_clk 4'h2: hdptx_o_earc_dmac_rxclk 4'h3: hdptx_o_tx_link_sym_clk 4'h4: hdptx_o_tx_hs_clk 4'h5: hdptx_i_tx_data_clk 4'h6: hdptx_o_hdmi_pixel_clk 4'h7: hdptx_o_aux_arc_rxdata 4'h8: hdptx_i_aux_earc_txdata_i 4'h9: hdptx_i_aux_tx_mode Others: hdptx_o_dig_refclk

HDPTXPHY_GRF_STATUS0

Address: Operational Base(0x26032000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	o_pll_lock_done PLL Lock Indication. The pin is high when PLL locking is completed. This means that all the output clocks are at the correct frequency.

Bit	Attr	Reset Value	Description
2	RO	0x0	o_phy_clk_rdy Indicates PHY data path clock outputs are stable. 1'b1: Clocks are ready 1'b0: Clocks are not ready
1	RO	0x0	o_phy_rdy Indicates PHY lanes are ready for data transmission. 1'b1: PHY lanes are ready 1'b0: PHY lanes are not ready
0	RO	0x0	o_sb_rdy Indicates sideband calibrations are complete and ready for sideband transceiver operations. 1'b1: Sideband block ready 1'b0: Sideband block not ready

5.23 DCPHY_GRF Register Description

5.23.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DCPHY_GRF_CON0	0x0000	W	0x00000000	MIPI DCPHY Control Register 0
DCPHY_GRF_CON1	0x0004	W	0x00000000	MIPI DCPHY Control Register 1
DCPHY_GRF_STATUS0	0x0080	W	0x00000000	MIPI DCPHY Status Register 0
DCPHY_GRF_STATUS1	0x0084	W	0x00000000	MIPI DCPHY Status Register 1
DCPHY_GRF_STATUS2	0x0088	W	0x00000000	MIPI DCPHY Status Register 2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.23.2 Detail Registers Description

DCPHY_GRF_CON0

Address: Operational Base(0x26034000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dcphy_clamp_en DCPHY output clamp enable. 1'b0: Normal mode 1'b1: Clamp DCPHY output to special value
14:4	RO	0x000	reserved
3	RW	0x0	s_cphy_mode C-PHY mode select signal of slave data lane. Active high.
2:1	RO	0x0	reserved
0	RW	0x0	m_cphy_mode C-PHY mode select signal of master data lane. Active high.

DCPHY_GRF_CON1

Address: Operational Base(0x26034000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	dcphy_hsclk_inv_sel 1'b0: Normal mode 1'b1: Invert M_TXWORDCLKHSCLK to controller.
14	RW	0x0	ppi_if_man_en If ppi_if_man_en is 1, M_TXREQUESTESC0, M_TXTRIGGERESC0, M_TXCLKESCCLK and M_TXCLKESC0 are controlled by software.
13:10	RW	0x0	m_txtriggeresc Escape mode transmit trigger 0. If ppi_if_man_en is 1, M_TXTRIGGERESC0 is controlled by this bit.
9	RW	0x0	m_txrequestesc Escape mode transmit request, high active. If ppi_if_man_en is 1, M_TXREQUESTESC0 is controlled by this bit.
8	RW	0x0	txclkesc Escape mode clock. If ppi_if_man_en is 1, M_TXCLKESCCLK and M_TXCLKESC0 is controlled by this bit.
7:4	RW	0x0	s_forcerxmode Force lane into receive mode/wait for stop state. Active high.
3:0	RW	0x0	m_forcetxstopmode Force lane into transmit mode generate stop state. Active high.

DCPHY_GRF_STATUS0

Address: Operational Base(0x26034000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	pll_cnt_done When PLL_EN is set to high , PLL lock counter is started to generate a delay to get a stabilized clock. The lock counter expires when the count value reaches the value set as PLL_LOCK_CNT(DCPHY_M0_PLL_CON7[15:0]). Then, the interface signal PLL_CNT_DONE is asserted.
8	RO	0x0	m_stopstateclk Master clock lane is in stop state. Active high.
7:4	RO	0x0	s_stopstate Slave lane is in stop state. Active high.
3:0	RO	0x0	m_stopstate Master data lane is in stop state. Active high.

DCPHY_GRF_STATUS1

Address: Operational Base(0x26034000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RO	0x00	m_phyerr0lane Master lane error status. Active high.

DCPHY_GRF_STATUS2

Address: Operational Base(0x26034000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	s_phyerr3 Slave lane error status. Active high.
11:8	RO	0x0	s_phyerr2 Slave lane error status. Active high.

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	s_phyerr1 Slave lane error status. Active high.
3:0	RO	0x0	s_phyerr0 Slave lane error status. Active high.

5.24 CSIDPHY_GRF Register Description

5.24.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
CSIDPHY0_GRF	0x2603A000
CSIDPHY1_GRF	0x2604C000

5.24.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CSIDPHY_GRF_CON0	0x0000	W	0x00000000	CSIDPHY Control Register
CSIDPHY_GRF_STATUS0	0x0080	W	0x00000000	CSIDPHY Status Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.24.3 Detail Registers Description

CSIDPHY_GRF_CON0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	csidphy_clk_1_inv Invert CSIDPHY clock lane1 rxbyte clock. 1'b0: Do not invert CSIDPHY clock lane 1 rxbyte_clk_hs 1'b1: Invert CSIDPHY clock lane 1 rxbyte_clk_hs
10	RW	0x0	csidphy_enable_ck_1 CSIDPHY Clock Lane 1 enable signal. Active State: High
9	RW	0x0	csidphy_clk_0_inv Invert CSIDPHY rxbyte clock. 1'b0: Do not invert CSIDPHY rxbyte_clk_hs 1'b1: Invert CSIDPHY rxbyte_clk_hs
8	RW	0x0	csidphy_enable_ck_0 CSIDPHY Clock Lane enable signal. Active State: High
7:4	RW	0x0	csidphy_enable_dat CSIDPHY enable lane module. This active high signal forces the Lane Module out of "shutdown". All line drivers, receivers, terminators, and connection detectors are turned off when Enable is low. Enable is a level sensitive signal and does not depend on any clock.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	csidphy_forcerxmode CSIDPHY force receive mode. Force Lane Module Into Receive mode / Wait for Stop state.This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode.

CSIDPHY_GRF_STATUS0

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	s_ulpsactivenotclk_1_raw ULP State (not) Active 1 status This active low signal is asserted to indicate that the Lane is in ULP state.
17	RO	0x0	s_ulpsactivenotclk_raw ULP State (not) Active status This active low signal is asserted to indicate that the Lane is in ULP state.
16:9	RO	0x00	errcontentionlp LP Contention Error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low.
8:5	RO	0x0	rxskewcalhs High-Speed Receive Skew Calibration This optional active high signal indicates that the high speed deskew burst is being received. RxSkewCalHS is set to the active state when the all-ones sync pattern is received, and is cleared to the inactive state when Dp and Dn transition back to the LP-11 Stop State.
4	RO	0x0	direction This signal is used to indicate the current direction of the Lane interconnects. When pin_direction =0, the Lane is in transmit mode. When pin_direction =1, the Lane is in receive mode.
3:0	RO	0x0	ulpsactivenot ULP State (not) Active. This active low signal is asserted to indicate that the Lane is in ULP state.

5.25 MPHY_GRF Register Description

5.25.1 Registers Summary

Name	Offset	Size	Reset Value	Description
MPHY_GRF_CON0	0x0000	W	0x00000003	MPHY Control Register 0
MPHY_GRF_CON1	0x0004	W	0x00000000	MPHY Control Register 1
MPHY_GRF_STATUS0	0x0008	W	0x00000000	MPHY Status Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.25.2 Detail Registers Description

MPHY_GRF_CON0

Address: Operational Base(0x2603C000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	MPHY_CLAMP_N MPHY output clamp enable. 1'b0: Normal mode 1'b1: Clamp MPHY output to special value
14:2	RO	0x0000	reserved
1:0	RW	0x3	REFCLK_SEL PMA REFCLK Select. 2'b00: From xin_osc_26Mhz 2'b11: From PLL

MPHY_GRF_CON1

Address: Operational Base(0x2603C000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	RX_TEST_RTC Internal multiplexers with signals on this bus are selected by programming
7:0	RW	0x00	TX_TEST_RTC Internal multiplexers with signals on this bus are selected by programming

MPHY_GRF_STATUS0

Address: Operational Base(0x2603C000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	PLL_LCK_DONE The Value of PMA.pll_lock_done
25	RO	0x0	CDR_LCK_DONE_CH0 The Value of PMA.cdr_lock_done_ch0
24	RO	0x0	CDR_LCK_DONE_CH1 The Value of PMA.cdr_lock_done_ch1
23:16	RO	0x00	RX_TEST_RTO The Value of PCS.rx_test_rto
15:8	RO	0x00	TX_TEST_RTO The Value of PCS.tx_test_rto
7:2	RO	0x00	reserved
1	RO	0x0	DBT_PMA The Value of PMA.o_dtb
0	RO	0x0	PCS_INTR The Interrupt state of PCS

5.26 PMU0_IOC (GPIO0 MUX/Attribute) Register Description

5.26.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU0_IOC_GPIO0A_IOMUX_SEL_L	0x0000	W	0x00000090	GPIO0A IOMUX selection register, lower bits
PMU0_IOC_GPIO0A_IOMUX_SEL_H	0x0004	W	0x00000000	GPIO0A IOMUX selection register, higher bits
PMU0_IOC_GPIO0B_IOMUX_SEL_L	0x0008	W	0x00000000	GPIO0B IOMUX selection register, lower bits
PMU0_IOC_GPIO0A_DS_L	0x0010	W	0x00002222	GPIO0A driver strength register, lower bits
PMU0_IOC_GPIO0A_DS_H	0x0014	W	0x00002222	GPIO0A driver strength register, higher bits
PMU0_IOC_GPIO0B_DS_L	0x0018	W	0x00002222	GPIO0B driver strength register, lower bits
PMU0_IOC_GPIO0A_PULL	0x0020	W	0x0000F551	GPIO0A pull up/down register
PMU0_IOC_GPIO0B_PULL_L	0x0024	W	0x00000000	GPIO0B pull up/down register, lower bits
PMU0_IOC_GPIO0A_IE	0x0028	W	0x000000FD	GPIO0A input enable register
PMU0_IOC_GPIO0B_IE_L	0x002C	W	0x00000000	GPIO0B input enable register, lower bits
PMU0_IOC_GPIO0A_SMT	0x0030	W	0x000000FF	GPIO0A schmitt register
PMU0_IOC_GPIO0B_SMT_L	0x0034	W	0x0000000F	GPIO0B schmitt register, lower bits
PMU0_IOC_GPIO0A_PDIS	0x0038	W	0x000000FF	GPIO0A auto pull-up/down disable register
PMU0_IOC_GPIO0B_PDIS_L	0x003C	W	0x0000000F	GPIO0A auto pull-up/down disable register
PMU0_IOC_OSC_CON	0x0040	W	0x00000008	Oscillator control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.26.2 Detail Registers Description

PMU0_IOC_GPIO0A_IOMUX_SEL_L

Address: Operational Base(0x26040000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0a3_sel 4'h0: GPIO0_A3 4'h9: PWR_CTRL1 4’ha: TSADC_CTRL_M1
11:8	RW	0x0	gpio0a2_sel 4'h0: GPIO0_A2 4'h9: CLK_32K_IN 4’ha: CLK0_32K_OUT 4’hb: I2C6_SCL_M0
7:4	RW	0x9	gpio0a1_sel 4'h0: GPIO0_A1 4'h9: TSADC_CTRL_M0 4’ha: TSADC_CTRL_ORG
3:0	RW	0x0	gpio0a0_sel 4'h0: GPIO0_A0 4'h1: REF_CLK0_OUT 4'h3: AUPLL_CLK_IN_M0

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PMU0_IOC_GPIO0A_IOMUX_SEL_H

Address: Operational Base(0x26040000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0a7_sel 4'h0: GPIO0_A7 4'h1: SDMMC0_DETN 4'h9: SPI2_CSN1_M0
11:8	RW	0x0	gpio0a6_sel 4'h0: GPIO0_A6 4'h9: PMIC_INT
7:4	RW	0x0	gpio0a5_sel 4'h0: GPIO0_A5 4'h9: PWR_CTRL3 4'hb: I2C6_SDA_M0
3:0	RW	0x0	gpio0a4_sel 4'h0: GPIO0_A4 4'h9: PWR_CTRL2

PMU0_IOC_GPIO0B_IOMUX_SEL_L

Address: Operational Base(0x26040000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0b3_sel 4'h0: GPIO0_B3 4'h9: SPI2_MOSI_M0 4'hb: I2C1_SDA_M0
11:8	RW	0x0	gpio0b2_sel 4'h0: GPIO0_B2 4'h9: SPI2_CLK_M0 4'hb: I2C1_SCL_M0
7:4	RW	0x0	gpio0b1_sel 4'h0: GPIO0_B1 4'h9: SPI2_MISO_M0 4'hb: I2C0_SDA_M0
3:0	RW	0x0	gpio0b0_sel 4'h0: GPIO0_B0 4'h3: AUPLL_CLK_IN_M1 4'h9: SPI2_CSN0_M0 4'hb: I2C0_SCL_M0

PMU0_IOC_GPIO0A_DS_L

Address: Operational Base(0x26040000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x2	gpio0a3_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
11:10	RO	0x0	reserved
9:8	RW	0x2	gpio0a2_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
7:6	RO	0x0	reserved
5:4	RW	0x2	gpio0a1_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
3:2	RO	0x0	reserved
1:0	RW	0x2	gpio0a0_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)

PMU0_IOC_GPIO0A_DS_H

Address: Operational Base(0x26040000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	gpio0a7_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
11:10	RO	0x0	reserved
9:8	RW	0x2	gpio0a6_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x2	gpio0a5_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
3:2	RO	0x0	reserved
1:0	RW	0x2	gpio0a4_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)

PMU0_IOC_GPIO0B_DS_L

Address: Operational Base(0x26040000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	gpio0b3_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
11:10	RO	0x0	reserved
9:8	RW	0x2	gpio0b2_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
7:6	RO	0x0	reserved
5:4	RW	0x2	gpio0b1_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
3:2	RO	0x0	reserved
1:0	RW	0x2	gpio0b0_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)

PMU0_IOC_GPIO0A_PULL

Address: Operational Base(0x26040000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0a7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
13:12	RW	0x3	gpio0a6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio0a5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio0a4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio0a3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio0a2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x0	gpio0a1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio0a0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

PMU0_IOC_GPIO0B_PULL_L

Address: Operational Base(0x26040000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	gpio0b3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x0	gpio0b2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x0	gpio0b1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x0	gpio0b0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

PMU0_IOC_GPIO0A_IE

Address: Operational Base(0x26040000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0a7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio0a6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio0a5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio0a4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x1	gpio0a3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio0a2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0a1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio0a0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

PMU0_IOC_GPIO0B_IE_L

Address: Operational Base(0x26040000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	gpio0b3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0b2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0b1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0b0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

PMU0_IOC_GPIO0A_SMT

Address: Operational Base(0x26040000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0a7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x1	gpio0a6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio0a5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio0a4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio0a3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio0a2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio0a1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio0a0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

PMU0_IOC_GPIO0B_SMT_L

Address: Operational Base(0x26040000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	gpio0b3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio0b2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio0b1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio0b0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

PMU0_IOC_GPIO0A_PDIS

Address: Operational Base(0x26040000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0a7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio0a6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio0a5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio0a4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio0a3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio0a2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio0a1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio0a0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

PMU0_IOC_GPIO0B_PDIS_L

Address: Operational Base(0x26040000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	gpio0b3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio0b2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio0b1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio0b0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

PMU0_IOC_OSC_CON

Address: Operational Base(0x26040000) + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x2	osc_sf Frequency selection. 2'b00: 1~12 MHz 2'b10: 12~26 MHz 2'b01: 26~36 MHz 2'b11: 36~52 MHz
1	RO	0x0	reserved
0	RW	0x0	osc_te External clock receive mode enable. 1'b0: Disable 1'b1: Enable

5.27 PMU1_IOC (GPIO0 MUX/Attribute) Register Description

5.27.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU1_IOC_GPIO0B_IOMUX_SEL_H	0x0000	W	0x00000000	GPIO0B IOMUX selection register, higher bits
PMU1_IOC_GPIO0C_IOMUX_SEL_L	0x0004	W	0x00000000	GPIO0C IOMUX selection register, lower bits
PMU1_IOC_GPIO0C_IOMUX_SEL_H	0x0008	W	0x00000000	GPIO0C IOMUX selection register, higher bits
PMU1_IOC_GPIO0D_IOMUX_SEL_L	0x000C	W	0x00000000	GPIO0D IOMUX selection register, lower bits
PMU1_IOC_GPIO0D_IOMUX_SEL_H	0x0010	W	0x00000000	GPIO0D IOMUX selection register, higher bits
PMU1_IOC_GPIO0B_DS_H	0x0014	W	0x00006666	GPIO0B driver strength register, higher bits
PMU1_IOC_GPIO0C_DS_L	0x0018	W	0x00006666	GPIO0C driver strength register, lower bits
PMU1_IOC_GPIO0C_DS_H	0x001C	W	0x00006666	GPIO0C driver strength register, higher bits
PMU1_IOC_GPIO0D_DS_L	0x0020	W	0x00006666	GPIO0D driver strength register, lower bits
PMU1_IOC_GPIO0D_DS_H	0x0024	W	0x00000066	GPIO0D driver strength register, higher bits
PMU1_IOC_GPIO0B_PULL_H	0x0028	W	0x00005500	GPIO0B pull up/down register, higher bits
PMU1_IOC_GPIO0C_PULL	0x002C	W	0x00005555	GPIO0C pull up/down register
PMU1_IOC_GPIO0D_PULL	0x0030	W	0x00000F55	GPIO0D pull up/down register
PMU1_IOC_GPIO0B_IE_H	0x0034	W	0x000000F0	GPIO0B input enable register, higher bits
PMU1_IOC_GPIO0C_IE	0x0038	W	0x000000FF	GPIO0C input enable register
PMU1_IOC_GPIO0D_IE	0x003C	W	0x0000003F	GPIO0D input enable register
PMU1_IOC_GPIO0B_SMT_H	0x0040	W	0x000000F0	GPIO0B schmitt register, higher bits
PMU1_IOC_GPIO0C_SMT	0x0044	W	0x000000FF	GPIO0C schmitt register
PMU1_IOC_GPIO0D_SMT	0x0048	W	0x0000003F	GPIO0D schmitt register

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Name	Offset	Size	Reset Value	Description
PMU1_IOC_GPIO0B_PDIS_H	0x004C	W	0x000000FF	GPIO0B auto pull-up/down disable register, higher bits
PMU1_IOC_GPIO0C_PDIS	0x0050	W	0x000000FF	GPIO0C auto pull-up/down disable register
PMU1_IOC_GPIO0D_PDIS	0x0054	W	0x000000FF	GPIO0D auto pull-up/down disable register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.27.2 Detail Registers Description

PMU1_IOC_GPIO0B_IOMUX_SEL_H

Address: Operational Base(0x26042000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0b7_sel 4'h0: GPIO0_B7 4'h9: I2C2_SCL_M0 4'ha: UART1_TX_M0 4'hb: NPU_AVS 4'hc: PWM1_CH4_M0
11:8	RW	0x0	gpio0b6_sel 4'h0: GPIO0_B6 4'h1: SDMMC0_PWREN 4'h2: SDMMC1_DETN_M2 4'h9: HDMI_TX_HPDIN_M1 4'ha: EDP_TX_HPDIN_M1 4'hc: PWM1_CH2_M0
7:4	RW	0x0	gpio0b5_sel 4'h0: GPIO0_B5 4'h1: REF_CLK2_OUT 4'h9: I2C1_SDA_M1 4'ha: UART4_RX_M2 4'hc: PWM1_CH1_M0
3:0	RW	0x0	gpio0b4_sel 4'h0: GPIO0_B4 4'h1: REF_CLK1_OUT 4'h9: I2C1_SCL_M1 4'ha: UART4_TX_M2 4'hc: PWM1_CH0_M0

PMU1_IOC_GPIO0C_IOMUX_SEL_L

Address: Operational Base(0x26042000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0c3_sel 4'h0: GPIO0_C3 4'h3: PDM0_CLK1_M0 4'h9: HDMI_TX_CEC_M1 4'hb: SPI0_CSN1_M0 4'hc: PWM0_CH1_M0

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio0c2_sel 4'h0: GPIO0_C2 4'h9: I2C0_SDA_M1 4'ha: UART8_RX_M2 4'hb: I3C0_SDA_M0
7:4	RW	0x0	gpio0c1_sel 4'h0: GPIO0_C1 4'h9: I2C0_SCL_M1 4'ha: UART8_TX_M2 4'hb: I3C0_SCL_M0
3:0	RW	0x0	gpio0c0_sel 4'h0: GPIO0_C0 4'h9: I2C2_SDA_M0 4'ha: UART1_RX_M0 4'hb: CPULIT_AVS 4'hc: PWM1_CH3_M0

PMU1_IOC_GPIO0C_IOMUX_SEL_H

Address: Operational Base(0x26042000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0c7_sel 4'h0: GPIO0_C7 4'h1: SAI0_LRCK_M1 4'h9: I2C3_SDA_M1 4'hb: SPI0_CLK_M0
11:8	RW	0x0	gpio0c6_sel 4'h0: GPIO0_C6 4'h1: SAI0_SCLK_M1 4'h9: I2C3_SCL_M1 4'hb: SPI0_CSN0_M0
7:4	RW	0x0	gpio0c5_sel 4'h0: GPIO0_C5 4'h1: SAI0_SDO0_M1 4'h9: DP_HPDIN_M1 4'ha: UART10_RX_M2 4'hb: I3C0_SDA_PU_M0
3:0	RW	0x0	gpio0c4_sel 4'h0: GPIO0_C4 4'h1: SAI0_MCLK_M1 4'h3: PDM0_CLK0_M0 4'ha: UART10_TX_M2 4'hc: PWM0_CH0_M0

PMU1_IOC_GPIO0D_IOMUX_SEL_L

Address: Operational Base(0x26042000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio0d3_sel 4'h0: GPIO0_D3 4'h1: SAI0_SDI3_M1 4'h2: SAI0_SDO1_M1 4'h3: PDM0_SDI3_M0 4'h9: I2C4_SDA_M0 4'hb: GPU_AVS 4'hc: PWM2_CH0_M0 4'hd: UART1_RTSN_M0
11:8	RW	0x0	gpio0d2_sel 4'h0: GPIO0_D2 4'h1: SAI0_SDI2_M1 4'h2: SAI0_SDO2_M1 4'h3: PDM0_SDI2_M0 4'h9: I2C4_SCL_M0 4'hb: CPUBIG_AVS 4'hc: PWM1_CH5_M0 4'hd: UART1_CTSN_M0
7:4	RW	0x0	gpio0d1_sel 4'h0: GPIO0_D1 4'h1: SAI0_SDI1_M1 4'h2: SAI0_SDO3_M1 4'h3: PDM0_SDI1_M0 4'hb: SPI0_MISO_M0
3:0	RW	0x0	gpio0d0_sel 4'h0: GPIO0_D0 4'h1: SAI0_SDI0_M1 4'h3: PDM0_SDI0_M0 4'hb: SPI0_MOSI_M0

PMU1_IOC_GPIO0D_IOMUX_SEL_H

Address: Operational Base(0x26042000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio0d5_sel 4'h0: GPIO0_D5 4'h9: UART0_RX_M0 4'ha: JTAG_TMS_M1
3:0	RW	0x0	gpio0d4_sel 4'h0: GPIO0_D4 4'h9: UART0_TX_M0 4'ha: JTAG_TCK_M1

PMU1_IOC_GPIO0B_DS_H

Address: Operational Base(0x26042000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x6	gpio0b7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio0b6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio0b5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio0b4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

PMU1_IOC_GPIO0C_DS_L

Address: Operational Base(0x26042000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio0c3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x6	gpio0c2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio0c1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio0c0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

PMU1_IOC_GPIO0C_DS_H

Address: Operational Base(0x26042000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio0c7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio0c6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x6	gpio0c5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio0c4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

PMU1_IOC_GPIO0D_DS_L

Address: Operational Base(0x26042000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio0d3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio0d2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio0d1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x6	gpio0d0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

PMU1_IOC_GPIO0D_DS_H

Address: Operational Base(0x26042000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:4	RW	0x6	gpio0d5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio0d4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

PMU1_IOC_GPIO0B_PULL_H

Address: Operational Base(0x26042000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio0b7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
13:12	RW	0x1	gpio0b6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x1	gpio0b5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio0b4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:0	RO	0x00	reserved

PMU1_IOC_GPIO0C_PULL

Address: Operational Base(0x26042000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio0c7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
13:12	RW	0x1	gpio0c6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio0c5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio0c4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio0c3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x1	gpio0c2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio0c1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio0c0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

PMU1_IOC_GPIO0D_PULL

Address: Operational Base(0x26042000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x3	gpio0d5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x3	gpio0d4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio0d3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio0d2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	gpio0d1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio0d0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

PMU1_IOC_GPIO0B_IE_H

Address: Operational Base(0x26042000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0b7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio0b6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio0b5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio0b4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

PMU1_IOC_GPIO0C_IE

Address: Operational Base(0x26042000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0c7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio0c6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x1	gpio0c5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio0c4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio0c3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio0c2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio0c1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio0c0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

PMU1_IOC_GPIO0D_IE

Address: Operational Base(0x26042000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio0d5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio0d4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio0d3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio0d2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio0d1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x1	gpio0d0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

PMU1_IOC_GPIO0B_SMT_H

Address: Operational Base(0x26042000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0b7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio0b6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio0b5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio0b4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

PMU1_IOC_GPIO0C_SMT

Address: Operational Base(0x26042000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0c7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio0c6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio0c5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio0c4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x1	gpio0c3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio0c2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio0c1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio0c0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

PMU1_IOC_GPIO0D_SMT

Address: Operational Base(0x26042000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio0d5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio0d4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio0d3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio0d2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio0d1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio0d0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

PMU1_IOC_GPIO0B_PDIS_H

Address: Operational Base(0x26042000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0b7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio0b6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio0b5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio0b4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3:0	RO	0xF	reserved

PMU1_IOC_GPIO0C_PDIS

Address: Operational Base(0x26042000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0c7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio0c6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio0c5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio0c4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio0c3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio0c2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio0c1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio0c0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

PMU1_IOC_GPIO0D_PDIS

Address: Operational Base(0x26042000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x003	reserved
5	RW	0x1	gpio0d5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio0d4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio0d3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio0d2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio0d1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio0d0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

5.28 TOP_IOC (GPIO1/2/3/4 MUX) Register Description

5.28.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TOP_IOC_GPIO1A_IOMUX_SEL_L	0x0020	W	0x00000000	GPIO1A IOMUX selection register, lower bits
TOP_IOC_GPIO1A_IOMUX_SEL_H	0x0024	W	0x00000000	GPIO1A IOMUX selection register, higher bits
TOP_IOC_GPIO1B_IOMUX_SEL_L	0x0028	W	0x00000000	GPIO1B IOMUX selection register, lower bits
TOP_IOC_GPIO1B_IOMUX_SEL_H	0x002C	W	0x00000000	GPIO1B IOMUX selection register, higher bits
TOP_IOC_GPIO1C_IOMUX_SEL_L	0x0030	W	0x00000000	GPIO1C IOMUX selection register, lower bits
TOP_IOC_GPIO1C_IOMUX_SEL_H	0x0034	W	0x00000000	GPIO1C IOMUX selection register, higher bits
TOP_IOC_GPIO1D_IOMUX_SEL_L	0x0038	W	0x00000000	GPIO1D IOMUX selection register, lower bits
TOP_IOC_GPIO1D_IOMUX_SEL_H	0x003C	W	0x00000000	GPIO1D IOMUX selection register, higher bits
TOP_IOC_GPIO2A_IOMUX_SEL_L	0x0040	W	0x00009900	GPIO2A IOMUX selection register, lower bits
TOP_IOC_GPIO2A_IOMUX_SEL_H	0x0044	W	0x00000000	GPIO2A IOMUX selection register, higher bits
TOP_IOC_GPIO2B_IOMUX_SEL_L	0x0048	W	0x00000000	GPIO2B IOMUX selection register, lower bits
TOP_IOC_GPIO2B_IOMUX_SEL_H	0x004C	W	0x00000000	GPIO2B IOMUX selection register, higher bits

Name	Offset	Size	Reset Value	Description
TOP_IOC_GPIO2C_IOMUX_SEL_L	0x0050	W	0x00000000	GPIO2C IOMUX selection register, lower bits
TOP_IOC_GPIO2C_IOMUX_SEL_H	0x0054	W	0x00000000	GPIO2C IOMUX selection register, higher bits
TOP_IOC_GPIO2D_IOMUX_SEL_L	0x0058	W	0x00000000	GPIO2D IOMUX selection register, lower bits
TOP_IOC_GPIO2D_IOMUX_SEL_H	0x005C	W	0x00000000	GPIO2D IOMUX selection register, higher bits
TOP_IOC_GPIO3A_IOMUX_SEL_L	0x0060	W	0x00000000	GPIO3A IOMUX selection register, lower bits
TOP_IOC_GPIO3A_IOMUX_SEL_H	0x0064	W	0x00000000	GPIO3A IOMUX selection register, higher bits
TOP_IOC_GPIO3B_IOMUX_SEL_L	0x0068	W	0x00000000	GPIO3B IOMUX selection register, lower bits
TOP_IOC_GPIO3B_IOMUX_SEL_H	0x006C	W	0x00000000	GPIO3B IOMUX selection register, higher bits
TOP_IOC_GPIO3C_IOMUX_SEL_L	0x0070	W	0x00000000	GPIO3C IOMUX selection register, lower bits
TOP_IOC_GPIO3C_IOMUX_SEL_H	0x0074	W	0x00000000	GPIO3C IOMUX selection register, higher bits
TOP_IOC_GPIO3D_IOMUX_SEL_L	0x0078	W	0x00000000	GPIO3D IOMUX selection register, lower bits
TOP_IOC_GPIO3D_IOMUX_SEL_H	0x007C	W	0x00000000	GPIO3D IOMUX selection register, higher bits
TOP_IOC_GPIO4A_IOMUX_SEL_L	0x0080	W	0x00000000	GPIO4A IOMUX selection register, lower bits
TOP_IOC_GPIO4A_IOMUX_SEL_H	0x0084	W	0x00000000	GPIO4A IOMUX selection register, higher bits
TOP_IOC_GPIO4B_IOMUX_SEL_L	0x0088	W	0x00000000	GPIO4B IOMUX selection register, lower bits
TOP_IOC_GPIO4B_IOMUX_SEL_H	0x008C	W	0x00000000	GPIO4B IOMUX selection register, higher bits
TOP_IOC_IOC_MISC_CON	0x00F0	W	0x00000002	Miscellaneous control register
TOP_IOC_SDMMC_DETN_FLT	0x00F4	W	0x00000000	SDMMC detectn filter count register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.28.2 Detail Registers Description

TOP_IOC_GPIO1A_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1a3_sel 4'h0: GPIO1_A3 4'h1: EMMC_D3 4'h2: FSPI0_D3 4'h3: SAI0_SDO2_M2 4'h4: SAI0_SDI2_M2 4'h5: PDM0_SDI1_M1 4'h9: UART7_RX_M1 4'ha: UART6_CTSN_M2

Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio1a2_sel 4'h0: GPIO1_A2 4'h1: EMMC_D2 4'h2: FSPI0_D2 4'h3: SAI0_SDO1_M2 4'h4: SAI0_SDI3_M2 4'h5: PDM0_SDI3_M1 4'h9: UART7_TX_M1 4'ha: UART6_RTSN_M2
7:4	RW	0x0	gpio1a1_sel 4'h0: GPIO1_A1 4'h1: EMMC_D1 4'h2: FSPI0_D1 4'h3: SAI0_LRCK_M2 4'h9: UART7_CTSN_M1 4'ha: I2C2_SDA_M1
3:0	RW	0x0	gpio1a0_sel 4'h0: GPIO1_A0 4'h1: EMMC_D0 4'h2: FSPI0_D0 4'h3: SAI0_SCLK_M2 4'h9: UART7_RTSN_M1 4'ha: I2C2_SCL_M1

TOP_IOC_GPIO1A_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1a7_sel 4'h0: GPIO1_A7 4'h1: EMMC_D7 4'h3: SAI0_SDO0_M2 4'h4: SAI3_SDI_M0 4'h9: SPI0_CLK_M2
11:8	RW	0x0	gpio1a6_sel 4'h0: GPIO1_A6 4'h1: EMMC_D6 4'h4: SAI3_LRCK_M0 4'h5: PDM0_CLK1_M1 4'h9: SPI0_MISO_M2 4'ha: I2C9_SDA_M0
7:4	RW	0x0	gpio1a5_sel 4'h0: GPIO1_A5 4'h1: EMMC_D5 4'h4: SAI3_SCLK_M0 4'h5: PDM0_SDI2_M1 4'h9: SPI0_MOSI_M2 4'ha: I2C9_SCL_M0

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio1a4_sel 4'h0: GPIO1_A4 4'h1: EMMC_D4 4'h3: SAI0_MCLK_M2 4'h4: SAI3_MCLK_M0 4'h9: SPI0_CSN0_M2

TOP_IOC_GPIO1B_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1b3_sel 4'h0: GPIO1_B3 4'h1: EMMC_RSTN 4'h2: FSPI0_CSN0 4'h9: UART6_RX_M2 4'ha: I2C7_SDA_M0 4'hb: MIPI_TE_M3 4'hc: PWM2_CH1_M0
11:8	RW	0x0	gpio1b2_sel 4'h0: GPIO1_B2 4'h1: EMMC_STRB 4'h3: SAI0_SDI0_M2 4'h4: SAI3_SDO_M0 4'h5: PDM0_SDI0_M1 4'h9: SPI0_CSN1_M2
7:4	RW	0x0	gpio1b1_sel 4'h0: GPIO1_B1 4'h1: EMMC_CLK 4'h2: FSPI0_CLK 4'h3: SAI0_SDO3_M2 4'h4: SAI0_SDI1_M2 4'h5: PDM0_CLK0_M1 4'hc: PWM2_CH7_M1
3:0	RW	0x0	gpio1b0_sel 4'h0: GPIO1_B0 4'h1: EMMC_CMD 4'h2: FSPI0_CSN1 4'h9: UART6_TX_M2 4'ha: I2C7_SCL_M0

TOP_IOC_GPIO1B_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio1b7_sel 4'h0: GPIO1_B7 4'h1: ETH1_TXD2_M1 4'h2: SDMMC1_D3_M0 4'h4: SAI3_SDI_M1 4'h9: UART3_RTSN_M2 4'hb: SPI1_CSN0_M0
11:8	RW	0x0	gpio1b6_sel 4'h0: GPIO1_B6 4'h1: ETH1_RXCLK_M1 4'h2: SDMMC1_D2_M0 4'h4: SAI3_SDO_M1 4'h9: UART3_CTSN_M2 4'hb: SPI1_MISO_M0 4'hc: PCIE0_CLKREQ_M1
7:4	RW	0x0	gpio1b5_sel 4'h0: GPIO1_B5 4'h1: ETH1_RXD3_M1 4'h2: SDMMC1_D1_M0 4'h4: SAI3_LRCK_M1 4'ha: I2C9_SCL_M1 4'hb: SPI1_MOSI_M0 4'hd: PWM1_CH1_M1
3:0	RW	0x0	gpio1b4_sel 4'h0: GPIO1_B4 4'h1: ETH1_RXD2_M1 4'h2: SDMMC1_D0_M0 4'h4: SAI3_SCLK_M1 4'ha: I2C9_SDA_M1 4'hb: SPI1_CLK_M0 4'hc: PCIE1_CLKREQ_M1 4'hd: PWM1_CH0_M1

TOP_IOC_GPIO1C_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1c3_sel 4'h0: GPIO1_C3 4'h1: ETH1_PPSTRIG_M1 4'h2: SDMMC1_DETN_M0 4'h3: FSPI1_CSN0_M1 4'h9: UART4_CTSN_M1 4'ha: I2C6_SDA_M1 4'hb: SPI2_CSN0_M1

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio1c2_sel 4'h0: GPIO1_C2 4'h1: ETH1_PPSCLK_M1 4'h2: SDMMC1_PWREN_M0 4'h3: FSPI1_CSN1_M1 4'h9: UART4_RTSN_M1 4'ha: I2C6_SCL_M1 4'hb: SPI2_CSN1_M1 4'hd: PWM1_CH2_M1
7:4	RW	0x0	gpio1c1_sel 4'h0: GPIO1_C1 4'h1: ETH1_TXCLK_M1 4'h2: SDMMC1_CLK_M0 4'h4: SAI3_MCLK_M1 4'h5: PDM0_CLK0_M2 4'h9: UART3_RX_M2
3:0	RW	0x0	gpio1c0_sel 4'h0: GPIO1_C0 4'h1: ETH1_TXD3_M1 4'h2: SDMMC1_CMD_M0 4'h5: PDM0_SDI2_M2 4'h9: UART3_TX_M2 4'hb: SPI1_CSN1_M0 4'hd: PWM0_CH0_M1

TOP_IOC_GPIO1C_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1c7_sel 4'h0: GPIO1_C7 4'h1: ETH1_RXD0_M1 4'h3: FSPI1_D3_M1 4'h5: PDM0_SDI1_M2 4'h9: UART2_RX_M0 4'ha: I2C8_SDA_M1 4'hc: SATA_CPDET
11:8	RW	0x0	gpio1c6_sel 4'h0: GPIO1_C6 4'h1: ETH1_TXCTL_M1 4'h3: FSPI1_D2_M1 4'h5: PDM0_SDI0_M2 4'h9: UART2_TX_M0 4'ha: I2C8_SCL_M1 4'hc: SATA_CPPOD
7:4	RW	0x0	gpio1c5_sel 4'h0: GPIO1_C5 4'h1: ETH1_TXD1_M1 4'h3: FSPI1_D1_M1 4'h9: UART4_RX_M1 4'ha: UART2_CTSN_M0 4'hb: SPI2_MISO_M1 4'hc: PCIE1_BUTTONRST

Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio1c4_sel 4'h0: GPIO1_C4 4'h1: ETH1_TXD0_M1 4'h3: FSPI1_D0_M1 4'h9: UART4_TX_M1 4'ha: UART2_RTSN_M0 4'hb: SPI2_MOSI_M1 4'hc: PCIE0_BUTTONRST

TOP_IOC_GPIO1D_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1d3_sel 4'h0: GPIO1_D3 4'h1: ETH1_MDIO_M1 4'h4: SAI2_SDI_M0 4'ha: I3C0_SDA_M1 4'hd: PWM1_CH4_M1
11:8	RW	0x0	gpio1d2_sel 4'h0: GPIO1_D2 4'h1: ETH1_MDC_M1 4'h4: SAI2_LRCK_M0 4'ha: I3C0_SCL_M1 4'hd: PWM1_CH3_M1
7:4	RW	0x0	gpio1d1_sel 4'h0: GPIO1_D1 4'h1: ETH1_RXCTL_M1 4'h4: SAI2_SCLK_M0 4'h9: UART10_RX_M1 4'ha: I3C0_SDA_PU_M1
3:0	RW	0x0	gpio1d0_sel 4'h0: GPIO1_D0 4'h1: ETH1_RXD1_M1 4'h4: SAI2_SDO_M0 4'h9: UART10_TX_M1

TOP_IOC_GPIO1D_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio1d5_sel 4'h0: GPIO1_D5 4'h1: ETH_CLK1_25M_OUT_M1 4'h3: FSPI1_CLK_M1 4'h5: PDM0_CLK1_M2 4'h6: SPDIF_TX1_M2 4'h9: UART10_CTSN_M1 4'ha: I2C5_SDA_M1 4'hb: SPI2_CLK_M1 4'hc: SATA_MPSWIT 4'hd: CLK1_32K_OUT
3:0	RW	0x0	gpio1d4_sel 4'h0: GPIO1_D4 4'h1: ETH1_MCLK_M1 4'h4: SAI2_MCLK_M0 4'h5: PDM0_SDI3_M2 4'h6: SPDIF_RX1_M2 4'h9: UART10_RTSN_M1 4'ha: I2C5_SCL_M1

TOP_IOC_GPIO2A_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x9	gpio2a3_sel 4'h0: GPIO2_A3 4'h1: SDMMC0_D3 4'h2: FSPI1_D3_M0 4'h3: DSM_AUD_RN_M0 4'h4: SAI3_SDI_M3 4'h9: JTAG_TMS_M0 4'ha: UART5_CTSN_M2 4'hd: CAN1_TX_M0 4'he: I3C1_SDA_M1
11:8	RW	0x9	gpio2a2_sel 4'h0: GPIO2_A2 4'h1: SDMMC0_D2 4'h2: FSPI1_D2_M0 4'h3: DSM_AUD_RP_M0 4'h4: SAI3_LRCK_M3 4'h9: JTAG_TCK_M0 4'ha: UART5_RTSN_M2 4'hc: SPI0_CSN1_M1 4'hd: CAN1_RX_M0 4'he: I3C1_SCL_M1

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio2a1_sel 4'h0: GPIO2_A1 4'h1: SDMMC0_D1 4'h2: FSPI1_D1_M0 4'h3: DSM_AUD_LN_M0 4'h4: SAI3_MCLK_M3 4'h9: UART0_TX_M1 4'ha: UART7_TX_M2 4'hb: I2C8_SDA_M0 4'hc: SPI0_MISO_M1 4'hd: CAN0_TX_M0 4'he: PWM2_CH3_M0
3:0	RW	0x0	gpio2a0_sel 4'h0: GPIO2_A0 4'h1: SDMMC0_D0 4'h2: FSPI1_D0_M0 4'h3: DSM_AUD_LP_M0 4'h9: UART0_RX_M1 4'ha: UART7_RX_M2 4'hb: I2C8_SCL_M0 4'hc: SPI0_MOSI_M1 4'hd: CAN0_RX_M0 4'he: PWM2_CH2_M0

TOP_IOC_GPIO2A_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2a7_sel 4'h0: GPIO2_A7 4'h1: VI_CIF_D14 4'h2: SDMMC1_D1_M1 4'h3: ETH0_TXCTL_M1 4'h4: SAI0_SDO1_M0 4'h9: UART8_RX_M1 4'hb: I2C4_SDA_M2
11:8	RW	0x0	gpio2a6_sel 4'h0: GPIO2_A6 4'h1: VI_CIF_D15 4'h2: SDMMC1_D0_M1 4'h3: ETH0_RXD0_M1 4'h4: SAI0_SDO0_M0 4'h9: UART8_TX_M1 4'ha: SPI4_CSN1_M3 4'hb: I2C4_SCL_M2

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio2a5_sel 4'h0: GPIO2_A5 4'h1: SDMMC0_CLK 4'h2: FSPI1_CLK_M0 4'h4: SAI3_SCLK_M3 4'h5: TEST_CLK_OUT 4'h9: UART5_TX_M2 4'hb: I2C5_SCL_M0 4'hc: SPI0_CLK_M1 4'he: I3C1_SDA_PU_M1
3:0	RW	0x0	gpio2a4_sel 4'h0: GPIO2_A4 4'h1: SDMMC0_CMD 4'h2: FSPI1_CSN0_M0 4'h4: SAI3_SDO_M3 4'h9: UART5_RX_M2 4'hb: I2C5_SDA_M0 4'hc: SPI0_CSN0_M1 4'he: PWM2_CH4_M0

TOP_IOC_GPIO2B_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2b3_sel 4'h0: GPIO2_B3 4'h1: VI_CIF_D10 4'h2: SDMMC1_CLK_M1 4'h3: ETH0_TXCLK_M1 4'h4: SAI0_SDO2_M0 4'h5: PDM0_CLK1_M3 4'h9: UART1_RTSN_M1 4'ha: SPI4_CLK_M3 4'hb: PCIE1_CLKREQ_M0
11:8	RW	0x0	gpio2b2_sel 4'h0: GPIO2_B2 4'h1: VI_CIF_D11 4'h2: SDMMC1_CMD_M1 4'h3: ETH0_TXD3_M1 4'h4: SAI0_SDI2_M0 4'h5: PDM0_SDI1_M3 4'h9: UART1_CTSN_M1 4'ha: SPI4_CSN0_M3 4'hb: PCIE0_CLKREQ_M0
7:4	RW	0x0	gpio2b1_sel 4'h0: GPIO2_B1 4'h1: VI_CIF_D12 4'h2: SDMMC1_D3_M1 4'h3: ETH0_TXD0_M1 4'h4: SAI0_SDI1_M0 4'h5: PDM0_SDI2_M3 4'h9: UART1_RX_M1

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio2b0_sel 4'h0: GPIO2_B0 4'h1: VI_CIF_D13 4'h2: SDMMC1_D2_M1 4'h3: ETH0_TXD1_M1 4'h4: SAI0_SDI0_M0 4'h5: PDM0_SDI3_M3 4'h9: UART1_TX_M1

TOP_IOC_GPIO2B_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2b7_sel 4'h0: GPIO2_B7 4'h1: VI_CIF_D6 4'h3: ETH0_RXD2_M1 4'h4: SAI0_LRCK_M0 4'h9: UART7_RX_M0 4'ha: UART8_CTSN_M1 4'hb: I2C8_SDA_M2
11:8	RW	0x0	gpio2b6_sel 4'h0: GPIO2_B6 4'h1: VI_CIF_D7 4'h2: ETH1_PTP_REFCLK_M1 4'h3: ETH0_RXD3_M1 4'h4: SAI0_SCLK_M0 4'h9: UART7_TX_M0 4'ha: UART8_RTSN_M1 4'hb: I2C8_SCL_M2
7:4	RW	0x0	gpio2b5_sel 4'h0: GPIO2_B5 4'h1: VI_CIF_D8 4'h2: SDMMC1_DETN_M1 4'h3: ETH0_RXCLK_M1 4'h4: SAI0_MCLK_M0 4'h5: PDM0_CLK0_M3 4'h9: UART7_RTSN_M0 4'ha: SPI4_MISO_M3 4'hc: SATA1_ACTLED_M0
3:0	RW	0x0	gpio2b4_sel 4'h0: GPIO2_B4 4'h1: VI_CIF_D9 4'h2: SDMMC1_PWREN_M1 4'h3: ETH0_TXD2_M1 4'h4: SAI0_SDI3_M0 4'h5: PDM0_SDI0_M3 4'h9: UART7_CTSN_M0 4'ha: SPI4_MOSI_M3 4'hc: SATA0_ACTLED_M0

TOP_IOC_GPIO2C_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2c3_sel 4'h0: GPIO2_C3 4'h1: VI_CIF_D2 4'h2: ETH1_TXD2_M0 4'h4: SAI2_LRCK_M1 4'h5: PDM1_SDI3_M0 4'h9: UART11_RTSN_M1 4'ha: SPI1_MISO_M1 4'hd: PWM0_CH0_M2
11:8	RW	0x0	gpio2c2_sel 4'h0: GPIO2_C2 4'h1: VI_CIF_D3 4'h2: ETH1_RXCLK_M0 4'h3: ETH0_PPSTRIG_M1 4'h4: SAI2_SCLK_M1 4'h5: PDM1_SDI2_M0 4'h9: UART11_CTSN_M1 4'ha: SPI1_MOSI_M1 4'hd: PWM1_CH2_M2
7:4	RW	0x0	gpio2c1_sel 4'h0: GPIO2_C1 4'h1: VI_CIF_D4 4'h2: ETH1_RXD3_M0 4'h3: ETH0_PPSCLK_M1 4'h4: SAI2_MCLK_M1 4'h5: PDM1_CLK1_M0 4'h9: UART9_TX_M0 4'ha: SPI1_CSN1_M1 4'hd: PWM1_CH1_M2
3:0	RW	0x0	gpio2c0_sel 4'h0: GPIO2_C0 4'h1: VI_CIF_D5 4'h2: ETH1_RXD2_M0 4'h3: ETH0_PTP_REFCLK_M1 4'h5: PDM1_SDI1_M0 4'h9: UART9_RX_M0 4'hd: PWM1_CH0_M2

TOP_IOC_GPIO2C_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2c7_sel 4'h0: GPIO2_C7 4'h2: ETH1_TXD1_M0 4'h4: SAI4_LRCK_M3 4'h9: UART4_RTSN_M0 4'hb: I2C5_SDA_M2 4'hd: PWM0_CH1_M2

Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio2c6_sel 4'h0: GPIO2_C6 4'h2: ETH1_TXD0_M0 4'h4: SAI4_SCLK_M3 4'h9: UART4_CTSN_M0 4'hb: I2C5_SCL_M2 4'hd: PWM1_CH5_M2
7:4	RW	0x0	gpio2c5_sel 4'h0: GPIO2_C5 4'h1: VI_CIF_D0 4'h2: ETH1_TXCLK_M0 4'h4: SAI2_SDI_M1 4'h5: PDM1_CLK0_M0 4'h9: UART11_RX_M1 4'ha: SPI1_CLK_M1 4'hd: PWM1_CH4_M2
3:0	RW	0x0	gpio2c4_sel 4'h0: GPIO2_C4 4'h1: VI_CIF_D1 4'h2: ETH1_TXD3_M0 4'h4: SAI2_SDO_M1 4'h5: PDM1_SDI0_M0 4'h9: UART11_TX_M1 4'ha: SPI1_CSN0_M1 4'hd: PWM1_CH3_M2

TOP_IOC_GPIO2D_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2d3_sel 4'h0: GPIO2_D3 4'h2: ETH1_RXCTL_M0 4'h9: UART6_RX_M1 4'hc: I3C1_SDA_M0 4'hd: PWM2_CH3_M2
11:8	RW	0x0	gpio2d2_sel 4'h0: GPIO2_D2 4'h1: CAM_CLK0_OUT_M1 4'h2: ETH1_RXD1_M0 4'h4: SAI4_MCLK_M3 4'h9: UART6_TX_M1 4'hc: I3C1_SCL_M0 4'hd: PWM2_CH2_M2
7:4	RW	0x0	gpio2d1_sel 4'h0: GPIO2_D1 4'h2: ETH1_RXD0_M0 4'h4: SAI4_SDO_M3 4'h9: UART4_RX_M0 4'hb: I2C6_SDA_M2 4'hd: PWM2_CH1_M2

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio2d0_sel 4'h0: GPIO2_D0 4'h2: ETH1_TXCTL_M0 4'h4: SAI4_SDI_M3 4'h9: UART4_TX_M0 4'hb: I2C6_SCL_M2 4'hd: PWM2_CH0_M2

TOP_IOC_GPIO2D_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2d7_sel 4'h0: GPIO2_D7 4'h1: CAM_CLK2_OUT_M1 4'h2: ETH1_MCLK_M0 4'h3: ETH_CLK0_25M_OUT_M1 4'h4: SAI0_SDO3_M0 4'h5: SPDIF_TX0_M2 4'h9: UART9_CTSN_M0 4'ha: SPI3_CSN1_M0 4'hd: PWM2_CH7_M2
11:8	RW	0x0	gpio2d6_sel 4'h0: GPIO2_D6 4'h1: CAM_CLK1_OUT_M1 4'h2: ETH_CLK1_25M_OUT_M0 4'h3: ETH0_MCLK_M1 4'h4: SAI3_MCLK_M2 4'h5: SPDIF_RX0_M2 4'h9: UART9_RTSN_M0 4'hc: I3C1_SDA_PU_M0 4'hd: PWM2_CH6_M2
7:4	RW	0x0	gpio2d5_sel 4'h0: GPIO2_D5 4'h1: ISP_FLASH_TRIGOUT_M0 4'h2: ETH1_MDIO_M0 4'h9: UART6_CTSN_M1 4'hb: I2C9_SCL_M2 4'hd: PWM2_CH5_M2
3:0	RW	0x0	gpio2d4_sel 4'h0: GPIO2_D4 4'h1: ISP_PRELIGHT_TRIG_M0 4'h2: ETH1_MDC_M0 4'h9: UART6_RTSN_M1 4'hb: I2C9_SDA_M2 4'hd: PWM2_CH4_M2

TOP_IOC_GPIO3A_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3a3_sel 4'h0: GPIO3_A3 4'h1: VI_CIF_CLKI 4'h2: ETH1_PTP_REFCLK_M0 4'h3: ETH0_RXD1_M1 4'h4: SAI3_SDI_M2 4'h5: SPDIF_TX1_M1 4'h9: UART3_RTSN_M0 4'ha: SPI3_CSN0_M0 4'hb: CAN1_RX_M3
11:8	RW	0x0	gpio3a2_sel 4'h0: GPIO3_A2 4'h1: VI_CIF_CLKO 4'h2: ETH1_PPSCLK_M0 4'h3: ETH0_RXCTL_M1 4'h4: SAI3_SDO_M2 4'h5: SPDIF_RX1_M1 4'h9: UART3_CTSN_M0 4'ha: SPI3_MISO_M0 4'hb: CAN1_TX_M3 4'hc: MIPI_TE_M1
7:4	RW	0x0	gpio3a1_sel 4'h0: GPIO3_A1 4'h1: VI_CIF_VSYNC 4'h2: ETH1_PPSTRIG_M0 4'h3: ETH0_MDC_M1 4'h4: SAI3_LRCK_M2 4'h9: UART3_RX_M0 4'ha: SPI3_MOSI_M0 4'hb: I2C7_SDA_M1
3:0	RW	0x0	gpio3a0_sel 4'h0: GPIO3_A0 4'h1: VI_CIF_HREF 4'h3: ETH0_MDIO_M1 4'h4: SAI3_SCLK_M2 4'h9: UART3_TX_M0 4'ha: SPI3_CLK_M0 4'hb: I2C7_SCL_M1

TOP_IOC_GPIO3A_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3a7_sel 4'h0: GPIO3_A7 4'h1: VO_LCDC_D20 4'h2: VO_EBC_VCOM 4'h3: ETH0_RXCTL_M0 4'h4: PDM1_CLK1_M2 4'h5: DSMC_DATA13 4'h6: FLEXBUS0_D5 4'h9: UART1_TX_M2 4'ha: UART10_RTSN_M0
11:8	RW	0x0	gpio3a6_sel 4'h0: GPIO3_A6 4'h1: VO_LCDC_D21 4'h2: VO_EBC_GDOE 4'h3: ETH0_MDC_M0 4'h4: PDM1_SDI2_M2 4'h5: DSMC_DATA14 4'h6: FLEXBUS0_D6 4'h9: UART1_RX_M2 4'ha: UART10_CTSN_M0 4'hc: PWM1_CH2_M3
7:4	RW	0x0	gpio3a5_sel 4'h0: GPIO3_A5 4'h1: VO_LCDC_D22 4'h2: VO_EBC_GDSP 4'h3: ETH0_MDIO_M0 4'h4: PDM1_SDI3_M2 4'h5: DSMC_DATA15 4'h6: FLEXBUS0_D7 4'h9: UART1_RTSN_M2 4'ha: SPI2_CSN1_M2 4'hc: PWM1_CH1_M3
3:0	RW	0x0	gpio3a4_sel 4'h0: GPIO3_A4 4'h1: VO_LCDC_D23 4'h2: VO_EBC_SDSHR 4'h3: ETH_CLK0_25M_OUT_M0 4'h4: SAI4_SDI_M1 4'h5: DSMC_RDYN 4'h6: FLEXBUS1_D11 4'h8: FLEXBUS0_CSN_M0 4'h9: UART1_CTSN_M2 4'ha: SPI2_CLK_M2 4'hc: PWM1_CH0_M3

TOP_IOC_GPIO3B_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3b3_sel 4'h0: GPIO3_B3 4'h1: VO_LCDC_D16 4'h2: VO_EBC_SDCE0 4'h3: ETH0_TXCTL_M0 4'h4: PDM1_SDI0_M2 4'h5: DSMC_DATA10 4'h6: FLEXBUS0_D2 4'h9: UART9_TX_M1 4'hb: I2C8_SCL_M3
11:8	RW	0x0	gpio3b2_sel 4'h0: GPIO3_B2 4'h1: VO_LCDC_D17 4'h2: VO_EBC_SDCE1 4'h3: ETH0_RXD0_M0 4'h4: PDM1_SDI1_M2 4'h5: DSMC_DATA11 4'h6: FLEXBUS0_D3 4'h9: UART9_RX_M1 4'hb: I2C8_SDA_M3
7:4	RW	0x0	gpio3b1_sel 4'h0: GPIO3_B1 4'h1: VO_LCDC_D18 4'h2: VO_EBC_SDCE2 4'h3: ETH0_RXD1_M0 4'h4: PDM1_CLK0_M2 4'h5: DSMC_DATA12 4'h6: FLEXBUS0_D4 4'h9: UART10_TX_M0 4'ha: SPI4_CSN0_M1 4'hc: PWM1_CH3_M3
3:0	RW	0x0	gpio3b0_sel 4'h0: GPIO3_B0 4'h1: VO_LCDC_D19 4'h2: VO_EBC_SDCE3 4'h3: ETH0_MCLK_M0 4'h4: SAI4_MCLK_M1 4'h5: DSMC_CSN1 4'h6: FLEXBUS0_D8 4'h9: UART10_RX_M0 4'ha: SPI2_MOSI_M2 4'hc: PWM0_CH0_M3

TOP_IOC_GPIO3B_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3b7_sel 4'h0: GPIO3_B7 4'h1: VO_LCDC_D12 4'h2: VO_EBC_SDDO12 4'h3: ETH0_PPSTRIG_M0 4'h4: SAI1_SDI0_M1 4'h5: DSMC_DQS0 4'h6: FLEXBUS1_D10 4'h8: FLEXBUS1_CSN_M0 4'h9: UART2_RX_M2 4'ha: UART3_CTSN_M1 4'hb: I2C4_SDA_M3
11:8	RW	0x0	gpio3b6_sel 4'h0: GPIO3_B6 4'h1: VO_LCDC_D13 4'h2: VO_EBC_SDDO13 4'h3: ETH0_TXCLK_M0 4'h5: DSMC_DQS1 4'h6: FLEXBUS0_CLK 4'ha: SPI3_CSN0_M1 4'hc: PWM0_CH1_M3
7:4	RW	0x0	gpio3b5_sel 4'h0: GPIO3_B5 4'h1: VO_LCDC_D14 4'h2: VO_EBC_SDDO14 4'h3: ETH0_TXD0_M0 4'h4: SPDIF_TX1_M0 4'h5: DSMC_DATA8 4'h6: FLEXBUS0_D0 4'h9: UART9_CTSN_M1 4'hc: PWM1_CH5_M3
3:0	RW	0x0	gpio3b4_sel 4'h0: GPIO3_B4 4'h1: VO_LCDC_D15 4'h2: VO_EBC_SDDO15 4'h3: ETH0_TXD1_M0 4'h4: SPDIF_RX1_M0 4'h5: DSMC_DATA9 4'h6: FLEXBUS0_D1 4'h9: UART9_RTSN_M1 4'hc: PWM1_CH4_M3

TOP_IOC_GPIO3C_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3c3_sel 4'h0: GPIO3_C3 4'h1: VO_LCDC_D8 4'h2: VO_EBC_SDDO8 4'h3: ETH0_TXD2_M0 4'h4: SAI2_LRCK_M2 4'h5: DSMC_INT3 4'h6: FLEXBUS0_D10 4'h8: FLEXBUS0_CSN_M2 4'h9: UART11_CTSN_M0 4'ha: SPI4_MOSI_M1 4'hb: I2C9_SDA_M3 4'hc: PWM2_CH1_M3
11:8	RW	0x0	gpio3c2_sel 4'h0: GPIO3_C2 4'h1: VO_LCDC_D9 4'h2: VO_EBC_SDDO9 4'h3: ETH0_TXD3_M0 4'h4: SAI2_SCLK_M2 4'h5: DSMC_INT1 4'h6: FLEXBUS0_D9 4'h9: UART11_RTSN_M0 4'ha: SPI4_MISO_M1 4'hb: I2C9_SCL_M3 4'hc: PWM2_CH0_M3
7:4	RW	0x0	gpio3c1_sel 4'h0: GPIO3_C1 4'h1: VO_LCDC_D10 4'h2: VO_EBC_SDDO10 4'h3: ETH0_PTP_REFCLK_M0 4'h4: SAI1_SDO2_M1 4'h5: DSMC_DATA6 4'h6: FLEXBUS1_D8 4'h9: UART11_RX_M0 4'ha: SPI2_MISO_M2 4'hb: I2C5_SDA_M3 4'hc: CAN0_RX_M3
3:0	RW	0x0	gpio3c0_sel 4'h0: GPIO3_C0 4'h1: VO_LCDC_D11 4'h2: VO_EBC_SDDO11 4'h3: ETH0_PPSCLK_M0 4'h4: SAI1_SDO3_M1 4'h5: DSMC_DATA7 4'h6: FLEXBUS1_D9 4'h9: UART2_TX_M2 4'ha: UART3_RTSN_M1 4'hb: I2C4_SCL_M3

TOP_IOC_GPIO3C_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3c7_sel 4'h0: GPIO3_C7 4'h1: VO_LCDC_D4 4'h2: VO_EBC_SDDO4 4'h4: SAI1_SCLK_M1 4'h5: DSMC_DATA2 4'h6: FLEXBUS1_D4 4'h9: UART8_RTSN_M0 4'ha: SPI1_CLK_M2
11:8	RW	0x0	gpio3c6_sel 4'h0: GPIO3_C6 4'h1: VO_LCDC_D5 4'h2: VO_EBC_SDDO5 4'h4: SAI1_LRCK_M1 4'h5: DSMC_DATA3 4'h6: FLEXBUS1_D5 4'h9: UART8_TX_M0 4'ha: SPI1_MOSI_M2
7:4	RW	0x0	gpio3c5_sel 4'h0: GPIO3_C5 4'h1: VO_LCDC_D6 4'h2: VO_EBC_SDDO6 4'h4: SAI1_SDO0_M1 4'h5: DSMC_DATA4 4'h6: FLEXBUS1_D6 4'h9: UART8_RX_M0 4'ha: SPI1_MISO_M2 4'hc: PWM2_CH2_M3
3:0	RW	0x0	gpio3c4_sel 4'h0: GPIO3_C4 4'h1: VO_LCDC_D7 4'h2: VO_EBC_SDDO7 4'h4: SAI1_SDO1_M1 4'h5: DSMC_DATA5 4'h6: FLEXBUS1_D7 4'h9: UART11_TX_M0 4'ha: SPI2_CSN0_M2 4'hb: I2C5_SCL_M3 4'hc: CAN0_TX_M3

TOP_IOC_GPIO3D_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3d3_sel 4'h0: GPIO3_D3 4'h1: VO_LCDC_D0 4'h2: VO_EBC_SDDO0 4'h3: ETH0_RXD2_M0 4'h4: SAI2_SDO_M2 4'h5: DSMC_CSN0 4'h6: FLEXBUS1_D2 4'h9: UART2_CTSN_M2 4'hb: I3C1_SCL_M2 4'hc: PWM2_CH5_M3
11:8	RW	0x0	gpio3d2_sel 4'h0: GPIO3_D2 4'h1: VO_LCDC_D1 4'h2: VO_EBC_SDDO1 4'h3: ETH0_RXD3_M0 4'h4: SAI2_SDI_M2 4'h5: DSMC_CSN3 4'h6: FLEXBUS0_D12 4'h7: FLEXBUS1_D15_M0 4'h8: FLEXBUS0_CSN_M3 4'h9: UART2_RTSN_M2 4'ha: SPI4_CSN1_M1 4'hb: I3C1_SDA_M2 4'hc: PWM2_CH4_M3
7:4	RW	0x0	gpio3d1_sel 4'h0: GPIO3_D1 4'h1: VO_LCDC_D2 4'h2: VO_EBC_SDDO2 4'h3: ETH0_RXCLK_M0 4'h4: SAI2_MCLK_M2 4'h5: DSMC_CSN2 4'h6: FLEXBUS0_D11 4'h8: FLEXBUS1_CSN_M2 4'ha: SPI4_CLK_M1 4'hb: I3C1_SDA_PU_M2
3:0	RW	0x0	gpio3d0_sel 4'h0: GPIO3_D0 4'h1: VO_LCDC_D3 4'h2: VO_EBC_SDDO3 4'h4: SAI1_MCLK_M1 4'h5: DSMC_DATA1 4'h6: FLEXBUS1_D3 4'h9: UART8_CTSN_M0 4'ha: SPI1_CSN0_M2 4'hc: PWM2_CH3_M3

TOP_IOC_GPIO3D_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3d7_sel 4'h0: GPIO3_D7 4'h1: VO_LCDC_CLK 4'h2: VO_EBC_SDOE 4'h3: CAM_CLK0_OUT_M0 4'h4: SAI4_SCLK_M1 4'h5: DSMC_RESETN 4'h6: FLEXBUS0_D15_M0 4'h7: FLEXBUS1_D12_M0 4'h8: FLEXBUS1_CSN_M1 4'h9: UART5_RTSN_M0 4'ha: SPI3_CSN1_M1 4'hc: PWM2_CH7_M3
11:8	RW	0x0	gpio3d6_sel 4'h0: GPIO3_D6 4'h1: VO_LCDC_VSYNC 4'h2: VO_EBC_SDCLK 4'h4: SAI1_SDI3_M1 4'h5: DSMC_CLKN 4'h6: FLEXBUS1_CLK 4'h9: UART5_CTSN_M0 4'ha: SPI3_MOSI_M1 4'hc: PWM2_CH6_M3
7:4	RW	0x0	gpio3d5_sel 4'h0: GPIO3_D5 4'h1: VO_LCDC_HSYNC 4'h2: VO_EBC_GDCLK 4'h4: SAI1_SDI2_M1 4'h5: DSMC_CLKP 4'h6: FLEXBUS1_D0 4'h9: UART5_TX_M0 4'ha: SPI3_MISO_M1 4'hb: I2C3_SDA_M2
3:0	RW	0x0	gpio3d4_sel 4'h0: GPIO3_D4 4'h1: VO_LCDC_DEN 4'h2: VO_EBC_SDLE 4'h4: SAI1_SDI1_M1 4'h5: DSMC_DATA0 4'h6: FLEXBUS1_D1 4'h9: UART5_RX_M0 4'ha: SPI3_CLK_M1 4'hb: I2C3_SCL_M2

TOP_IOC_GPIO4A_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio4a3_sel 4'h0: GPIO4_A3 4'h1: SAI1_SCLK_M0 4'h4: FLEXBUS1_CSN_M4 4'h9: SPI3_CSN0_M2 4'ha: UART5_RTSN_M1 4'hb: I2C2_SCL_M2 4'hd: PWM2_CH4_M1
11:8	RW	0x0	gpio4a2_sel 4'h0: GPIO4_A2 4'h1: SAI1_MCLK_M0 4'h2: SAI4_MCLK_M0 4'h3: AUPLL_CLK_IN_M2 4'hd: PWM2_CH5_M0
7:4	RW	0x0	gpio4a1_sel 4'h0: GPIO4_A1 4'h1: VO_POST_EMPTY 4'h2: SPDIF_TX0_M1 4'h3: CAM_CLK2_OUT_M0 4'h4: SAI4_SDO_M1 4'h5: DSMC_INT2 4'h6: FLEXBUS0_D14_M0 4'h7: FLEXBUS1_D13_M0 4'h8: FLEXBUS0_CSN_M1 4'h9: UART3_RX_M1 4'hb: I2C7_SDA_M2
3:0	RW	0x0	gpio4a0_sel 4'h0: GPIO4_A0 4'h2: SPDIF_RX0_M1 4'h3: CAM_CLK1_OUT_M0 4'h4: SAI4_LRCK_M1 4'h5: DSMC_INT0 4'h6: FLEXBUS0_D13_M0 4'h7: FLEXBUS1_D14_M0 4'h8: FLEXBUS1_CSN_M3 4'h9: UART3_TX_M1 4'ha: SPI1_CSN1_M2 4'hb: I2C7_SCL_M2 4'hc: MIPI_TE_M2

TOP_IOC_GPIO4A_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4a7_sel 4'h0: GPIO4_A7 4'h1: SAI1_SDO0_M0 4'h2: SAI4_SDI_M0 4'h9: SPI3_CLK_M2 4'hd: PWM2_CH6_M0

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio4a6_sel 4'h0: GPIO4_A6 4'h2: SAI4_LRCK_M0 4'h3: PDM1_CLK0_M1 4'h4: FLEXBUS0_D14_M1 4'h9: SPI3_MISO_M2 4'ha: UART6_RX_M0 4'hb: I2C4_SDA_M1 4'hd: CAN0_RX_M2
7:4	RW	0x0	gpio4a5_sel 4'h0: GPIO4_A5 4'h1: SAI1_LRCK_M0 4'h4: FLEXBUS1_D12_M1 4'h9: SPI4_CSN1_M2 4'ha: UART5_CTSN_M1 4'hb: I2C2_SDA_M2 4'hc: PCIE1_CLKREQ_M2
3:0	RW	0x0	gpio4a4_sel 4'h0: GPIO4_A4 4'h2: SAI4_SCLK_M0 4'h3: PDM1_SDI3_M1 4'h4: FLEXBUS0_D13_M1 4'h9: SPI3_MOSI_M2 4'ha: UART6_TX_M0 4'hb: I2C4_SCL_M1 4'hd: CAN0_TX_M2

TOP_IOC_GPIO4B_IOMUX_SEL_L

Address: Operational Base(0x26044000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4b3_sel 4'h0: GPIO4_B3 4'h1: SAI1_SDI0_M0 4'h2: SAI4_SDO_M0 4'h3: PDM1_SDI0_M1 4'h9: SPI4_CSN0_M2 4'ha: SPI3_CSN1_M2 4'hd: PWM2_CH7_M0
11:8	RW	0x0	gpio4b2_sel 4'h0: GPIO4_B2 4'h1: SAI1_SDO3_M0 4'h2: SAI1_SDI1_M0 4'h3: PDM1_SDI1_M1 4'h4: FLEXBUS1_D15_M1 4'h9: SPI4_MISO_M2 4'hb: MIPI_TE_M0 4'hc: PCIE0_PERST_M2 4'hd: PCIE1_PERST_M2

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio4b1_sel 4'h0: GPIO4_B1 4'h1: SAI1_SDO2_M0 4'h2: SAI1_SDI2_M0 4'h3: PDM1_SDI2_M1 4'h4: FLEXBUS1_D14_M1 4'h9: SPI4_MOSI_M2 4’ha: UART5_RX_M1 4’hb: UART6_CTSN_M0 4’hc: UART2_CTSN_M1
3:0	RW	0x0	gpio4b0_sel 4'h0: GPIO4_B0 4'h1: SAI1_SDO1_M0 4'h2: SAI1_SDI3_M0 4'h3: PDM1_CLK1_M1 4'h4: FLEXBUS1_D13_M1 4'h9: SPI4_CLK_M2 4’ha: UART5_TX_M1 4’hb: UART6_RTSN_M0 4’hc: UART2_RTSN_M1

TOP_IOC_GPIO4B_IOMUX_SEL_H

Address: Operational Base(0x26044000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio4b5_sel 4'h0: GPIO4_B5 4'h1: SPDIF_TX0_M0 4'h4: FLEXBUS0_D15_M1 4’ha: UART2_TX_M1 4’hb: I2C3_SCL_M0 4’hc: PCIE0_CLKREQ_M2 4’hd: CAN1_TX_M2
3:0	RW	0x0	gpio4b4_sel 4'h0: GPIO4_B4 4'h1: SPDIF_RX0_M0 4'h4: FLEXBUS0_CSN_M4 4’ha: UART2_RX_M1 4’hb: I2C3_SDA_M0 4’hd: CAN1_RX_M2

TOP_IOC_IOC_MISC_CON

Address: Operational Base(0x26044000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x1	sdmmc_force_jtag Force IO from SDMMC mode to JTAG mode. When sdmmc_force_jtag is 1, GPIO2A2 and GPIO2A3 are used for SDMMC mode, and SDMMC detectn signal is inactice, then GPIO2A2 and GPIO2A3 will swith to JTAG mode.
0	RW	0x0	sata_io_sel SATA io selection. 1'b0: SATA0 1'b1: SATA1

TOP_IOC_SDMMC_DETN_FLT

Address: Operational Base(0x26044000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sdmmc_detn_flt SDMMC detect IO delay count. Number of xin_osc(24MHz) used by counter logic.

5.29 VCCIO_IOC (GPIO1/2/3/4 Attribute) Register

Description

5.29.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VCCIO_IOC_GPIO1A_DSL	0x0020	W	0x00006666	GPIO1A driver strength register, lower bits
VCCIO_IOC_GPIO1A_DSH	0x0024	W	0x00006666	GPIO1A driver strength register, higher bits
VCCIO_IOC_GPIO1B_DSL	0x0028	W	0x00006666	GPIO1B driver strength register, lower bits
VCCIO_IOC_GPIO1B_DSH	0x002C	W	0x00006666	GPIO1B driver strength register, higher bits
VCCIO_IOC_GPIO1C_DSL	0x0030	W	0x00006666	GPIO1C driver strength register, lower bits
VCCIO_IOC_GPIO1C_DSH	0x0034	W	0x00006666	GPIO1C driver strength register, higher bits
VCCIO_IOC_GPIO1D_DSL	0x0038	W	0x00006666	GPIO1D driver strength register, lower bits
VCCIO_IOC_GPIO1D_DSH	0x003C	W	0x00000066	GPIO1D driver strength register, higher bits
VCCIO_IOC_GPIO2A_DSL	0x0040	W	0x00006666	GPIO2A driver strength register, lower bits
VCCIO_IOC_GPIO2A_DSH	0x0044	W	0x00006666	GPIO2A driver strength register, higher bits
VCCIO_IOC_GPIO2B_DSL	0x0048	W	0x00006666	GPIO2B driver strength register, lower bits
VCCIO_IOC_GPIO2B_DSH	0x004C	W	0x00006666	GPIO2B driver strength register, higher bits
VCCIO_IOC_GPIO2C_DSL	0x0050	W	0x00006666	GPIO2C driver strength register, lower bits
VCCIO_IOC_GPIO2C_DSH	0x0054	W	0x00006666	GPIO2C driver strength register, higher bits
VCCIO_IOC_GPIO2D_DSL	0x0058	W	0x00006666	GPIO2D driver strength register, lower bits

Name	Offset	Size	Reset Value	Description
VCCIO_IOC_GPIO2D_DS_H	0x005C	W	0x00006666	GPIO2D driver strength register, higher bits
VCCIO_IOC_GPIO3A_DS_L	0x0060	W	0x00006666	GPIO3A driver strength register, lower bits
VCCIO_IOC_GPIO3A_DS_H	0x0064	W	0x00006666	GPIO3A driver strength register, higher bits
VCCIO_IOC_GPIO3B_DS_L	0x0068	W	0x00006666	GPIO3B driver strength register, lower bits
VCCIO_IOC_GPIO3B_DS_H	0x006C	W	0x00006666	GPIO3B driver strength register, higher bits
VCCIO_IOC_GPIO3C_DS_L	0x0070	W	0x00006666	GPIO3C driver strength register, lower bits
VCCIO_IOC_GPIO3C_DS_H	0x0074	W	0x00006666	GPIO3C driver strength register, higher bits
VCCIO_IOC_GPIO3D_DS_L	0x0078	W	0x00006666	GPIO3D driver strength register, lower bits
VCCIO_IOC_GPIO3D_DS_H	0x007C	W	0x00006666	GPIO3D driver strength register, higher bits
VCCIO_IOC_GPIO4A_DS_L	0x0080	W	0x00006666	GPIO4A driver strength register, lower bits
VCCIO_IOC_GPIO4A_DS_H	0x0084	W	0x00006666	GPIO4A driver strength register, higher bits
VCCIO_IOC_GPIO4B_DS_L	0x0088	W	0x00006666	GPIO4B driver strength register, lower bits
VCCIO_IOC_GPIO4B_DS_H	0x008C	W	0x00000066	GPIO4B driver strength register, higher bits
VCCIO_IOC_GPIO1A_PULL	0x0110	W	0x0000FFFF	GPIO1A pull up/down register
VCCIO_IOC_GPIO1B_PULL	0x0114	W	0x000055D7	GPIO1B pull up/down register
VCCIO_IOC_GPIO1C_PULL	0x0118	W	0x000055F5	GPIO1C pull up/down register
VCCIO_IOC_GPIO1D_PULL	0x011C	W	0x00000555	GPIO1D pull up/down register
VCCIO_IOC_GPIO2A_PULL	0x0120	W	0x00005555	GPIO2A pull up/down register
VCCIO_IOC_GPIO2B_PULL	0x0124	W	0x00005555	GPIO2B pull up/down register
VCCIO_IOC_GPIO2C_PULL	0x0128	W	0x00005555	GPIO2C pull up/down register
VCCIO_IOC_GPIO2D_PULL	0x012C	W	0x00005555	GPIO2D pull up/down register
VCCIO_IOC_GPIO3A_PULL	0x0130	W	0x00005555	GPIO3A pull up/down register
VCCIO_IOC_GPIO3B_PULL	0x0134	W	0x00005555	GPIO3B pull up/down register
VCCIO_IOC_GPIO3C_PULL	0x0138	W	0x00005555	GPIO3C pull up/down register
VCCIO_IOC_GPIO3D_PULL	0x013C	W	0x00005555	GPIO3D pull up/down register
VCCIO_IOC_GPIO4A_PULL	0x0140	W	0x00005555	GPIO4A pull up/down register
VCCIO_IOC_GPIO4B_PULL	0x0144	W	0x00000555	GPIO4B pull up/down register

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Name	Offset	Size	Reset Value	Description
VCCIO_IOC_GPIO1A_IE	0x0180	W	0x000000FF	GPIO1A input enable register
VCCIO_IOC_GPIO1B_IE	0x0184	W	0x000000FF	GPIO1B input enable register
VCCIO_IOC_GPIO1C_IE	0x0188	W	0x000000FF	GPIO1C input enable register
VCCIO_IOC_GPIO1D_IE	0x018C	W	0x0000003F	GPIO1D input enable register
VCCIO_IOC_GPIO2A_IE	0x0190	W	0x000000FF	GPIO2A input enable register
VCCIO_IOC_GPIO2B_IE	0x0194	W	0x000000FF	GPIO2B input enable register
VCCIO_IOC_GPIO2C_IE	0x0198	W	0x000000FF	GPIO2C input enable register
VCCIO_IOC_GPIO2D_IE	0x019C	W	0x000000FF	GPIO2D input enable register
VCCIO_IOC_GPIO3A_IE	0x01A0	W	0x000000FF	GPIO3A input enable register
VCCIO_IOC_GPIO3B_IE	0x01A4	W	0x000000FF	GPIO3B input enable register
VCCIO_IOC_GPIO3C_IE	0x01A8	W	0x000000FF	GPIO3C input enable register
VCCIO_IOC_GPIO3D_IE	0x01AC	W	0x000000FF	GPIO3D input enable register
VCCIO_IOC_GPIO4A_IE	0x01B0	W	0x000000FF	GPIO4A input enable register
VCCIO_IOC_GPIO4B_IE	0x01B4	W	0x0000003F	GPIO4B input enable register
VCCIO_IOC_GPIO1A_SMT	0x0210	W	0x000000FF	GPIO1A schmitt register
VCCIO_IOC_GPIO1B_SMT	0x0214	W	0x000000FF	GPIO1B schmitt register
VCCIO_IOC_GPIO1C_SMT	0x0218	W	0x000000FF	GPIO1C schmitt register
VCCIO_IOC_GPIO1D_SMT	0x021C	W	0x0000003F	GPIO1D schmitt register
VCCIO_IOC_GPIO2A_SMT	0x0220	W	0x000000FF	GPIO2A schmitt register
VCCIO_IOC_GPIO2B_SMT	0x0224	W	0x000000FF	GPIO2B schmitt register
VCCIO_IOC_GPIO2C_SMT	0x0228	W	0x000000FF	GPIO2C schmitt register
VCCIO_IOC_GPIO2D_SMT	0x022C	W	0x000000FF	GPIO2D schmitt register
VCCIO_IOC_GPIO3A_SMT	0x0230	W	0x000000FF	GPIO3A schmitt register
VCCIO_IOC_GPIO3B_SMT	0x0234	W	0x000000FF	GPIO3B schmitt register
VCCIO_IOC_GPIO3C_SMT	0x0238	W	0x000000FF	GPIO3C schmitt register
VCCIO_IOC_GPIO3D_SMT	0x023C	W	0x000000FF	GPIO3D schmitt register
VCCIO_IOC_GPIO4A_SMT	0x0240	W	0x000000FF	GPIO4A schmitt register
VCCIO_IOC_GPIO4B_SMT	0x0244	W	0x0000003F	GPIO4B schmitt register
VCCIO_IOC_GPIO1A_PDIS	0x0280	W	0x000000FF	GPIO1A auto pull-up/down disable register
VCCIO_IOC_GPIO1B_PDIS	0x0284	W	0x000000FF	GPIO1B auto pull-up/down disable register
VCCIO_IOC_GPIO1C_PDIS	0x0288	W	0x000000FF	GPIO1C auto pull-up/down disable register
VCCIO_IOC_GPIO1D_PDIS	0x028C	W	0x000000FF	GPIO1D auto pull-up/down disable register
VCCIO_IOC_GPIO2A_PDIS	0x0290	W	0x000000FF	GPIO2A auto pull-up/down disable register
VCCIO_IOC_GPIO2B_PDIS	0x0294	W	0x000000FF	GPIO2B auto pull-up/down disable register
VCCIO_IOC_GPIO2C_PDIS	0x0298	W	0x000000FF	GPIO2C auto pull-up/down disable register
VCCIO_IOC_GPIO2D_PDIS	0x029C	W	0x000000FF	GPIO2D auto pull-up/down disable register
VCCIO_IOC_GPIO3A_PDIS	0x02A0	W	0x000000FF	GPIO3A auto pull-up/down disable register
VCCIO_IOC_GPIO3B_PDIS	0x02A4	W	0x000000FF	GPIO3B auto pull-up/down disable register
VCCIO_IOC_GPIO3C_PDIS	0x02A8	W	0x000000FF	GPIO3C auto pull-up/down disable register
VCCIO_IOC_GPIO3D_PDIS	0x02AC	W	0x000000FF	GPIO3D auto pull-up/down disable register

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Name	Offset	Size	Reset Value	Description
VCCIO_IOC_GPIO4A_PDIS	0x02B0	W	0x000000FF	GPIO4A auto pull-up/down disable register
VCCIO_IOC_GPIO4B_PDIS	0x02B4	W	0x000000FF	GPIO4B auto pull-up/down disable register
VCCIO_IOC_MISC_CON0	0x0400	W	0x0000001F	Miscellaneous control register 0
VCCIO_IOC_MISC_CON1	0x0404	W	0x00000000	Miscellaneous control register 1
VCCIO_IOC_MISC_CON2	0x0408	W	0x00000000	Miscellaneous control register 2
VCCIO_IOC_MISC_CON3	0x040C	W	0x00000000	Miscellaneous control register 3
VCCIO_IOC_MISC_CON4	0x0410	W	0x00000000	Miscellaneous control register 4
VCCIO_IOC_MISC_CON5	0x0414	W	0x00000000	Miscellaneous control register 5
VCCIO_IOC_MISC_CON8	0x0420	W	0x00000000	Miscellaneous control register 8

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.29.2 Detail Registers Description

VCCIO_IOC_GPIO1A_DS_L

Address: Operational Base(0x26046000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio1a3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio1a2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio1a1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x6	gpio1a0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO1A_DS_H

Address: Operational Base(0x26046000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio1a7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio1a6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio1a5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio1a4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO1B_DS_L

Address: Operational Base(0x26046000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio1b3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio1b2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio1b1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio1b0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO1B_DS_H

Address: Operational Base(0x26046000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x6	gpio1b7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio1b6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio1b5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio1b4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO1C_DS_L

Address: Operational Base(0x26046000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio1c3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x6	gpio1c2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio1c1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio1c0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO1C_DS_H

Address: Operational Base(0x26046000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio1c7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio1c6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x6	gpio1c5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio1c4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO1D_DS_L

Address: Operational Base(0x26046000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio1d3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio1d2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio1d1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x6	gpio1d0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO1D_DS_H

Address: Operational Base(0x26046000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:4	RW	0x6	gpio1d5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio1d4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO2A_DS_L

Address: Operational Base(0x26046000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio2a3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x6	gpio2a2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio2a1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio2a0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO2A_DS_H

Address: Operational Base(0x26046000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio2a7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio2a6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x6	gpio2a5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio2a4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO2B_DS_L

Address: Operational Base(0x26046000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio2b3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio2b2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio2b1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x6	gpio2b0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO2B_DS_H

Address: Operational Base(0x26046000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio2b7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio2b6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio2b5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio2b4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO2C_DS_L

Address: Operational Base(0x26046000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio2c3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio2c2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio2c1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio2c0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO2C_DS_H

Address: Operational Base(0x26046000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x6	gpio2c7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio2c6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio2c5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio2c4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO2D_DS_L

Address: Operational Base(0x26046000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio2d3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x6	gpio2d2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio2d1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio2d0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO2D_DS_H

Address: Operational Base(0x26046000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio2d7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio2d6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x6	gpio2d5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio2d4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO3A_DS_L

Address: Operational Base(0x26046000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio3a3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio3a2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio3a1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x6	gpio3a0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO3A_DS_H

Address: Operational Base(0x26046000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio3a7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio3a6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio3a5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio3a4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO3B_DS_L

Address: Operational Base(0x26046000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio3b3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio3b2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio3b1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio3b0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO3B_DS_H

Address: Operational Base(0x26046000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x6	gpio3b7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio3b6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio3b5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio3b4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO3C_DS_L

Address: Operational Base(0x26046000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio3c3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x6	gpio3c2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio3c1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio3c0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO3C_DS_H

Address: Operational Base(0x26046000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio3c7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio3c6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x6	gpio3c5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio3c4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO3D_DS_L

Address: Operational Base(0x26046000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio3d3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio3d2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio3d1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x6	gpio3d0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO3D_DS_H

Address: Operational Base(0x26046000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio3d7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio3d6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio3d5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio3d4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO4A_DS_L

Address: Operational Base(0x26046000) + offset (0x0080)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio4a3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio4a2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio4a1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio4a0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO4A_DS_H

Address: Operational Base(0x26046000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x6	gpio4a7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio4a6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio4a5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio4a4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO4B_DS_L

Address: Operational Base(0x26046000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio4b3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x6	gpio4b2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio4b1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio4b0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO4B_DS_H

Address: Operational Base(0x26046000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:4	RW	0x6	gpio4b5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio4b4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO_IOC_GPIO1A_PULL

Address: Operational Base(0x26046000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio1a7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
13:12	RW	0x3	gpio1a6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x3	gpio1a5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x3	gpio1a4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x3	gpio1a3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x3	gpio1a2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x3	gpio1a1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x3	gpio1a0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO1B_PULL

Address: Operational Base(0x26046000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1b7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
13:12	RW	0x1	gpio1b6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio1b5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio1b4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x3	gpio1b3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio1b2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio1b1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x3	gpio1b0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO1C_PULL

Address: Operational Base(0x26046000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1c7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
13:12	RW	0x1	gpio1c6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio1c5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio1c4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x3	gpio1c3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x3	gpio1c2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio1c1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio1c0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO1D_PULL

Address: Operational Base(0x26046000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x1	gpio1d5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio1d4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio1d3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio1d2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio1d1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio1d0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO2A_PULL

Address: Operational Base(0x26046000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio2a7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio2a6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio2a5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio2a4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio2a3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio2a2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio2a1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio2a0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO2B_PULL

Address: Operational Base(0x26046000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio2b7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio2b6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio2b5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio2b4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio2b3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio2b2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio2b1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio2b0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO2C_PULL

Address: Operational Base(0x26046000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio2c7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio2c6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio2c5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio2c4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio2c3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio2c2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio2c1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio2c0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO2D_PULL

Address: Operational Base(0x26046000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio2d7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio2d6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio2d5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio2d4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio2d3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio2d2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio2d1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio2d0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO3A_PULL

Address: Operational Base(0x26046000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio3a7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio3a6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio3a5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio3a4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio3a3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio3a2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio3a1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio3a0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO3B_PULL

Address: Operational Base(0x26046000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio3b7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio3b6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio3b5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio3b4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio3b3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio3b2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio3b1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio3b0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO3C_PULL

Address: Operational Base(0x26046000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio3c7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio3c6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio3c5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio3c4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio3c3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio3c2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio3c1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio3c0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO3D_PULL

Address: Operational Base(0x26046000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio3d7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio3d6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio3d5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio3d4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio3d3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio3d2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio3d1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio3d0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO4A_PULL

Address: Operational Base(0x26046000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio4a7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio4a6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio4a5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio4a4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio4a3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio4a2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio4a1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio4a0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO4B_PULL

Address: Operational Base(0x26046000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:10	RW	0x1	gpio4b5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio4b4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio4b3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
5:4	RW	0x1	gpio4b2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio4b1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio4b0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO_IOC_GPIO1A_IE

Address: Operational Base(0x26046000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1a7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio1a6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x1	gpio1a5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio1a4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio1a3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio1a2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio1a1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio1a0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO1B_IE

Address: Operational Base(0x26046000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1b7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio1b6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio1b5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio1b4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio1b3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x1	gpio1b2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio1b1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio1b0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO1C_IE

Address: Operational Base(0x26046000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1c7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio1c6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio1c5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio1c4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio1c3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio1c2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio1c1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio1c0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO1D_IE

Address: Operational Base(0x26046000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio1d5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio1d4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio1d3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio1d2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio1d1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio1d0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO2A_IE

Address: Operational Base(0x26046000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2a7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio2a6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio2a5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio2a4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x1	gpio2a3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio2a2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio2a1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio2a0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO2B_IE

Address: Operational Base(0x26046000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2b7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio2b6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio2b5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio2b4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio2b3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio2b2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio2b1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x1	gpio2b0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO2C_IE

Address: Operational Base(0x26046000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2c7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio2c6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio2c5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio2c4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio2c3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio2c2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio2c1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio2c0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO2D_IE

Address: Operational Base(0x26046000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7	RW	0x1	gpio2d7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio2d6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio2d5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio2d4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio2d3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio2d2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio2d1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio2d0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO3A_IE

Address: Operational Base(0x26046000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3a7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio3a6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio3a5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x1	gpio3a4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio3a3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio3a2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio3a1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio3a0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO3B_IE

Address: Operational Base(0x26046000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3b7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio3b6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio3b5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio3b4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio3b3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio3b2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x1	gpio3b1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio3b0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO3C_IE

Address: Operational Base(0x26046000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3c7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio3c6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio3c5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio3c4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio3c3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio3c2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio3c1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio3c0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO3D_IE

Address: Operational Base(0x26046000) + offset (0x01AC)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3d7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio3d6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio3d5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio3d4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio3d3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio3d2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio3d1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio3d0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO4A_IE

Address: Operational Base(0x26046000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio4a7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio4a6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x1	gpio4a5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio4a4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio4a3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio4a2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio4a1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio4a0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO4B_IE

Address: Operational Base(0x26046000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio4b5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio4b4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio4b3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio4b2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio4b1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x1	gpio4b0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO1A_SMT

Address: Operational Base(0x26046000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1a7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio1a6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio1a5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio1a4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio1a3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio1a2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio1a1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio1a0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO1B_SMT

Address: Operational Base(0x26046000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7	RW	0x1	gpio1b7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio1b6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio1b5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio1b4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio1b3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio1b2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio1b1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio1b0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO1C_SMT

Address: Operational Base(0x26046000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1c7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio1c6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio1c5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x1	gpio1c4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio1c3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio1c2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio1c1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio1c0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO1D_SMT

Address: Operational Base(0x26046000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio1d5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio1d4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio1d3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio1d2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio1d1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio1d0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO2A_SMT

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Address: Operational Base(0x26046000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2a7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio2a6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio2a5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio2a4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio2a3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio2a2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio2a1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio2a0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO2B_SMT

Address: Operational Base(0x26046000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2b7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio2b6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x1	gpio2b5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio2b4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio2b3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio2b2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio2b1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio2b0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO2C_SMT

Address: Operational Base(0x26046000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2c7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio2c6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio2c5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio2c4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio2c3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x1	gpio2c2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio2c1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio2c0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO2D_SMT

Address: Operational Base(0x26046000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2d7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio2d6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio2d5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio2d4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio2d3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio2d2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio2d1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio2d0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO3A_SMT

Address: Operational Base(0x26046000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3a7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio3a6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio3a5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio3a4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio3a3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio3a2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio3a1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio3a0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO3B_SMT

Address: Operational Base(0x26046000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3b7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio3b6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x1	gpio3b5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio3b4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio3b3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio3b2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio3b1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio3b0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO3C_SMT

Address: Operational Base(0x26046000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3c7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio3c6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio3c5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio3c4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio3c3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x1	gpio3c2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio3c1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio3c0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO3D_SMT

Address: Operational Base(0x26046000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3d7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio3d6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio3d5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio3d4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio3d3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio3d2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio3d1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio3d0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO4A_SMT

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Address: Operational Base(0x26046000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio4a7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio4a6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio4a5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio4a4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio4a3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio4a2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio4a1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio4a0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO4B_SMT

Address: Operational Base(0x26046000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio4b5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio4b4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x1	gpio4b3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio4b2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio4b1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio4b0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_GPIO1A_PDIS

Address: Operational Base(0x26046000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1a7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio1a6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio1a5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio1a4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio1a3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio1a2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio1a1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio1a0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO1B_PDIS

Address: Operational Base(0x26046000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1b7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio1b6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio1b5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio1b4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio1b3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio1b2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio1b1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio1b0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO1C_PDIS

Address: Operational Base(0x26046000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1c7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio1c6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio1c5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio1c4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio1c3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

Bit	Attr	Reset Value	Description
2	RW	0x1	gpio1c2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio1c1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio1c0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO1D_PDIS

Address: Operational Base(0x26046000) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x003	reserved
5	RW	0x1	gpio1d5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio1d4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio1d3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio1d2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio1d1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio1d0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO2A_PDIS

Address: Operational Base(0x26046000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2a7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio2a6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio2a5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

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Bit	Attr	Reset Value	Description
4	RW	0x1	gpio2a4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio2a3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio2a2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio2a1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio2a0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO2B_PDIS

Address: Operational Base(0x26046000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2b7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio2b6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio2b5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio2b4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio2b3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio2b2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio2b1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio2b0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO2C_PDIS

Address: Operational Base(0x26046000) + offset (0x0298)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2c7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio2c6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio2c5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio2c4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio2c3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio2c2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio2c1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio2c0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO2D_PDIS

Address: Operational Base(0x26046000) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2d7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio2d6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio2d5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio2d4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio2d3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

Bit	Attr	Reset Value	Description
2	RW	0x1	gpio2d2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio2d1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio2d0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO3A_PDIS

Address: Operational Base(0x26046000) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3a7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio3a6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio3a5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio3a4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio3a3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio3a2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio3a1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio3a0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO3B_PDIS

Address: Operational Base(0x26046000) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3b7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

Bit	Attr	Reset Value	Description
6	RW	0x1	gpio3b6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio3b5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio3b4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio3b3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio3b2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio3b1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio3b0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO3C_PDIS

Address: Operational Base(0x26046000) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3c7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio3c6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio3c5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio3c4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio3c3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio3c2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio3c1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio3c0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

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VCCIO_IOC_GPIO3D_PDIS

Address: Operational Base(0x26046000) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3d7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio3d6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio3d5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio3d4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio3d3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio3d2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio3d1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio3d0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO4A_PDIS

Address: Operational Base(0x26046000) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio4a7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio4a6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio4a5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio4a4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio4a3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

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Bit	Attr	Reset Value	Description
2	RW	0x1	gpio4a2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio4a1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio4a0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO_IOC_GPIO4B_PDIS

Address: Operational Base(0x26046000) + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x003	reserved
5	RW	0x1	gpio4b5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio4b4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio4b3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio4b2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio4b1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio4b0_pdis PDIS enable. 1'b0: Disable 1'b1: Enable

VCCIO_IOC_MISC_CON0

Address: Operational Base(0x26046000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	flexbus_data_pipe_sel FLEXBUS data pipe selection. 1'b0: Normal 1'b1: Pipe
7	RW	0x0	flexbus_clk_inv_sel FLEXBUS clock invert selection. 1'b0: Normal 1'b1: Inverted

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Bit	Attr	Reset Value	Description
6	RW	0x0	fspi1_clk_ioe_n FSPI1 clk output enable. 1'b0: Output enable 1'b1: Output disable
5	RW	0x0	fspi0_clk_ioe_n FSPI0 clk output enable. 1'b0: Output enable 1'b1: Output disable
4	RW	0x1	sai4_mclk_ioe_n SAI4 mclk output enable. 1'b0: Output enable 1'b1: Output disable
3	RW	0x1	sai3_mclk_ioe_n SAI3 mclk output enable. 1'b0: Output enable 1'b1: Output disable
2	RW	0x1	sai2_mclk_ioe_n SAI2 mclk output enable. 1'b0: Output enable 1'b1: Output disable
1	RW	0x1	sai1_mclk_ioe_n SAI1 mclk output enable. 1'b0: Output enable 1'b1: Output disable
0	RW	0x1	sai0_mclk_ioe_n SAI0 mclk output enable. 1'b0: Output enable 1'b1: Output disable

VCCIO_IOC_MISC_CON1

Address: Operational Base(0x26046000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	cif_datapath CIF data path selection. 1'b0: Select single edge mode 1'b1: Select dual edge mode
8	RW	0x0	cif_clk_inv_sel CIF clock invert selection. 1'b0: Normal 1'b1: Inverted
7	RO	0x0	reserved
6:0	RW	0x00	cif_clk_delayline_num The number of delay elements used for CIF clock delayline

VCCIO_IOC_MISC_CON2

Address: Operational Base(0x26046000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gmac0_m0_rxclk_delay_ena Enable GMAC0-IOMUX0 RXCLK delayed by delayline. 1'b0: Disable 1'b1: Enable
14:8	RW	0x00	gmac0_m0_rxclk_delayline_num The number of delay elements used for GMAC0-IOMUX0 RXCLK delayline
7	RW	0x0	gmac0_m0_txclk_delay_ena Enable GMAC0-IOMUX0 TXCLK delayed by delayline. 1'b0: Disable 1'b1: Enable
6:0	RW	0x00	gmac0_m0_txclk_delayline_num The number of delay elements used for GMAC0-IOMUX0 TXCLK delayline

VCCIO_IOC_MISC_CON3

Address: Operational Base(0x26046000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gmac0_m1_rxclk_delay_ena Enable GMAC0-IOMUX1 RXCLK delayed by delayline. 1'b0: Disable 1'b1: Enable
14:8	RW	0x00	gmac0_m1_rxclk_delayline_num The number of delay elements used for GMAC0-IOMUX1 RXCLK delayline
7	RW	0x0	gmac0_m1_txclk_delay_ena Enable GMAC0-IOMUX1 TXCLK delayed by delayline. 1'b0: Disable 1'b1: Enable
6:0	RW	0x00	gmac0_m1_txclk_delayline_num The number of delay elements used for GMAC0-IOMUX1 TXCLK delayline

VCCIO_IOC_MISC_CON4

Address: Operational Base(0x26046000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gmac1_m0_rxclk_delay_ena Enable GMAC1-IOMUX0 RXCLK delayed by delayline. 1'b0: Disable 1'b1: Enable
14:8	RW	0x00	gmac1_m0_rxclk_delayline_num The number of delay elements used for GMAC1-IOMUX0 RXCLK delayline

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Bit	Attr	Reset Value	Description
7	RW	0x0	gmac1_m0_txclk_delay_ena Enable GMAC1-IOMUX0 TXCLK delayed by delayline. 1'b0: Disable 1'b1: Enable
6:0	RW	0x00	gmac1_m0_txclk_delayline_num The number of delay elements used for GMAC1-IOMUX0 TXCLK delayline

VCCIO_IOC_MISC_CON5

Address: Operational Base(0x26046000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gmac1_m1_rxclk_delay_ena Enable GMAC1-IOMUX1 RXCLK delayed by delayline. 1'b0: Disable 1'b1: Enable
14:8	RW	0x00	gmac1_m1_rxclk_delayline_num The number of delay elements used for GMAC1-IOMUX1 RXCLK delayline
7	RW	0x0	gmac1_m1_txclk_delay_ena Enable GMAC1-IOMUX1 TXCLK delayed by delayline. 1'b0: Disable 1'b1: Enable
6:0	RW	0x00	gmac1_m1_txclk_delayline_num The number of delay elements used for GMAC1-IOMUX1 TXCLK delayline

VCCIO_IOC_MISC_CON8

Address: Operational Base(0x26046000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	vop_rgb_output_sel VOP selection for BT1120/BT656/MCU/RGB interface output. 1'b0: VOP 1'b1: VOP_LITE
10	RW	0x0	vop_mcu_sel VOP MCU interface selection. 1'b0: Other interface 1'b1: MCU interface
9	RW	0x0	vop_dclk_inv_sel VOP dclk invert selection. 1'b0: Normal 1'b1: Inverted
8	RW	0x0	vop_dclk_dll_sel Enable VOP dclk delayed by delayline. 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	vop_dclk_delayline_num The number of delay elements used for VOP dclk delayline

5.30 VCCIO6_IOC (GPIO4 MUX/Attribute) Register

Description

5.30.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VCCIO6_IOC_GPIO4C_DS_L	0x0090	W	0x00006666	GPIO4C driver strength register, lower bits
VCCIO6_IOC_GPIO4C_DS_H	0x0094	W	0x00006666	GPIO4C driver strength register, higher bits
VCCIO6_IOC_GPIO4C_PULL	0x0148	W	0x00005555	GPIO4C pull up/down register
VCCIO6_IOC_GPIO4C_IE	0x01B8	W	0x000000FF	GPIO4C input enable register
VCCIO6_IOC_GPIO4C_SMT	0x0248	W	0x000000FF	GPIO4C schmitt register
VCCIO6_IOC_GPIO4C_PDIS	0x02B8	W	0x000000FF	GPIO4C auto pull-up/down disable register
VCCIO6_IOC_GPIO4C_IOMUX_SEL_L	0x0390	W	0x00000000	GPIO4C IOMUX selection register, lower bits
VCCIO6_IOC_GPIO4C_IOMUX_SEL_H	0x0394	W	0x00000000	GPIO4C IOMUX selection register, higher bits
VCCIO6_IOC_MISC_CON0	0x0400	W	0x00000001	Miscellaneous control register 0
VCCIO6_IOC_MISC_CON1	0x0404	W	0x00000000	Miscellaneous control register 1
VCCIO6_IOC_HDMITX_HPD_STATUS	0x0440	W	0x00000000	HDMITX HDP status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.30.2 Detail Registers Description

VCCIO6_IOC_GPIO4C_DS_L

Address: Operational Base(0x2604A000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio4c3_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x6	gpio4c2_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved
6:4	RW	0x6	gpio4c1_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio4c0_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO6_IOC_GPIO4C_DS_H

Address: Operational Base(0x2604A000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x6	gpio4c7_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
11	RO	0x0	reserved
10:8	RW	0x6	gpio4c6_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x6	gpio4c5_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)
3	RO	0x0	reserved
2:0	RW	0x6	gpio4c4_ds Driver strength selection(ohm). 3'b000: Level0 (100 ohm) 3'b100: Level1 (66 ohm) 3'b010: Level2 (50 ohm) 3'b110: Level3 (40 ohm) 3'b001: Level4 (33 ohm) 3'b101: Level5 (25 ohm)

VCCIO6_IOC_GPIO4C_PULL

Address: Operational Base(0x2604A000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio4c7_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
13:12	RW	0x1	gpio4c6_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
11:10	RW	0x1	gpio4c5_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
9:8	RW	0x1	gpio4c4_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
7:6	RW	0x1	gpio4c3_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x1	gpio4c2_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
3:2	RW	0x1	gpio4c1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved
1:0	RW	0x1	gpio4c0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO6_IOC_GPIO4C_IE

Address: Operational Base(0x2604A000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio4c7_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio4c6_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio4c5_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio4c4_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio4c3_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio4c2_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio4c1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x1	gpio4c0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO6_IOC_GPIO4C_SMT

Address: Operational Base(0x2604A000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio4c7_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
6	RW	0x1	gpio4c6_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
5	RW	0x1	gpio4c5_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
4	RW	0x1	gpio4c4_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
3	RW	0x1	gpio4c3_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio4c2_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio4c1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio4c0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO6_IOC_GPIO4C_PDIS

Address: Operational Base(0x2604A000) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7	RW	0x1	gpio4c7_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
6	RW	0x1	gpio4c6_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
5	RW	0x1	gpio4c5_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
4	RW	0x1	gpio4c4_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
3	RW	0x1	gpio4c3_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
2	RW	0x1	gpio4c2_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
1	RW	0x1	gpio4c1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio4c0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

VCCIO6_IOC_GPIO4C_IOMUX_SEL_L

Address: Operational Base(0x2604A000) + offset (0x0390)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4c3_sel 4'h0: GPIO4_C3 4'h1: DSM_AUD_RN_M1 4'h9: HDMI_TX_SDA 4’hb: I2C2_SDA_M3 4’hc: CAN0_RX_M1 4’hd: UART9_RX_M2 4’he: PWM2_CH1_M1
11:8	RW	0x0	gpio4c2_sel 4'h0: GPIO4_C2 4'h1: DSM_AUD_RP_M1 4'h9: HDMI_TX_SCL 4’hb: I2C2_SCL_M3 4’hc: CAN0_TX_M1 4’hd: UART9_TX_M2 4’he: PWM2_CH0_M1

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio4c1_sel 4'h0: GPIO4_C1 4'h1: DSM_AUD_LN_M1 4'h9: HDMI_TX_HPDIN_M0 4'ha: PCIE1_CLKREQ_M3 4'hb: I2C7_SDA_M3 4'hc: EDP_TX_HPDIN_M0 4'hd: UART11_RX_M2 4'he: PWM0_CH1_M1
3:0	RW	0x0	gpio4c0_sel 4'h0: GPIO4_C0 4'h1: DSM_AUD_LP_M1 4'h2: SAI4_MCLK_M2 4'h9: HDMI_TX_CEC_M0 4'hb: I2C7_SCL_M3 4'hc: SPI4_CSN1_M0 4'hd: UART11_TX_M2 4'he: PWM1_CH5_M1

VCCIO6_IOC_GPIO4C_IOMUX_SEL_H

Address: Operational Base(0x2604A000) + offset (0x0394)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4c7_sel 4'h0: GPIO4_C7 4'h2: SAI4_SCLK_M2 4'h3: VP2_SYNC_OUT 4'hb: I2C6_SDA_M3 4'hc: SPI4_CLK_M0 4'hd: CAN1_RX_M1 4'he: PWM2_CH3_M1
11:8	RW	0x0	gpio4c6_sel 4'h0: GPIO4_C6 4'h2: SAI4_SDI_M2 4'h3: VP1_SYNC_OUT 4'h9: PCIE0_CLKREQ_M3 4'ha: SATA0_ACTLED_M1 4'hb: I2C6_SCL_M3 4'hc: SPI4_MISO_M0 4'hd: CAN1_TX_M1 4'he: PWM2_CH2_M1
7:4	RW	0x0	gpio4c5_sel 4'h0: GPIO4_C5 4'h1: ISP_FLASH_TRIGOUT_M1 4'h2: SAI4_SDO_M2 4'h3: VP0_SYNC_OUT 4'ha: SATA1_ACTLED_M1 4'hb: I2C3_SDA_M3 4'hc: SPI4_MOSI_M0 4'hd: UART6_RX_M3 4'he: PWM2_CH5_M1

Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio4c4_sel 4'h0: GPIO4_C4 4'h1: ISP_PRELIGHT_TRIG_M1 4'h2: SAI4_LRCK_M2 4’ha: DP_HPDIN_M0 4’hb: I2C3_SCL_M3 4’hc: SPI4_CSN0_M0 4’hd: UART6_TX_M3 4’he: PWM2_CH6_M1

VCCIO6_IOC_MISC_CON0

Address: Operational Base(0x2604A000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	hdmitx_hpd_int_mask HDMITX HPD interrupt mask. 1'b0: Interrupt enable 1'b1: Interrupt disable
1	RW	0x0	hdmitx_hpd_int_clr HDMITX HPD interrupt clear. A rising edge of hdmitx_hpd_int_clr will clear the HDMITX HPD interrupt.
0	RW	0x1	sai4_mclk_ioe_n SAI4 mclk output enable for VCCIO6. 1'b0: Output enable 1'b1: Output disable

VCCIO6_IOC_MISC_CON1

Address: Operational Base(0x2604A000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	hdmitx_hpd_con HDMITX HDP control bits

VCCIO6_IOC_HDMITX_HPD_STATUS

Address: Operational Base(0x2604A000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hdmitx_hpd_status HDMITX HDP status

5.31 VCCIO7_IOC (GPIO4 MUX/Attribute) Register

Description

5.31.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VCCIO7_IOC_GPIO4D_DS_L	0x0098	W	0x00000012	GPIO4D driver strength register, lower bits
VCCIO7_IOC_GPIO4D_PULL	0x014C	W	0x00000005	GPIO4D pull up/down register
VCCIO7_IOC_GPIO4D_IE	0x01BC	W	0x00000003	GPIO4D input enable register
VCCIO7_IOC_GPIO4D_SMT	0x024C	W	0x00000003	GPIO4D schmitt register
VCCIO7_IOC_GPIO4D_PDIS	0x02BC	W	0x00000003	GPIO4D auto pull-up/down disable register
VCCIO7_IOC_GPIO4D_IOMUX_SEL_L	0x0398	W	0x00000000	GPIO4D IOMUX selection register, lower bits
VCCIO7_IOC_XIN_UFS_CON	0x0400	W	0x0000000A	Oscillator control register for UFS

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.31.2 Detail Registers Description

VCCIO7_IOC_GPIO4D_DS_L

Address: Operational Base(0x2604B000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x1	gpio4d1_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)
3:2	RO	0x0	reserved
1:0	RW	0x2	gpio4d0_ds Driver strength selection(ohm). 2'b00: Level0 (100 ohm) 2'b10: Level1 (50 ohm) 2'b01: Level2 (33 ohm) 2'b11: Level3 (25 ohm)

VCCIO7_IOC_GPIO4D_PULL

Address: Operational Base(0x2604B000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x1	gpio4d1_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x1	gpio4d0_pull Weak PU/PD resistor selection. 2'b00: Z 2'b01: Pull down 2'b11: Pull up 2'b10: Reserved

VCCIO7_IOC_GPIO4D_IE

Address: Operational Base(0x2604B000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio4d1_ie Input buffer enable. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio4d0_ie Input buffer enable. 1'b0: Disable 1'b1: Enable

VCCIO7_IOC_GPIO4D_SMT

Address: Operational Base(0x2604B000) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio4d1_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable
0	RW	0x1	gpio4d0_smt CMOS/Schmitt trigger selection. 1'b0: Disable 1'b1: Enable

VCCIO7_IOC_GPIO4D_PDIS

Address: Operational Base(0x2604B000) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio4d1_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.
0	RW	0x1	gpio4d0_pdis PDIS enable. When 1'b1, disable GPIO pull up/down when output enable.

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VCCIO7_IOC_GPIO4D_IOMUX_SEL_L

Address: Operational Base(0x2604B000) + offset (0x0398)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio4d1_sel 4'h0: GPIO4_D1 4'h1: UFS_REFCLK
3:0	RW	0x0	gpio4d0_sel 4'h0: GPIO4_D0 4'h1: UFS_RSTN

VCCIO7_IOC_XIN_UFS_CON

Address: Operational Base(0x2604B000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	ufs_rstn_out UFS reset io configuration
3:2	RW	0x2	xin_ufs_sf Frequency selection. 2'b00: 1~12 MHz 2'b10: 12~26 MHz 2'b01: 26~36 MHz 2'b11: 36~52 MHz
1	RW	0x1	xin_ufs_e0 Crystal oscillation mode enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	xin_ufs_te External clock receive mode enable. 1'b0: Disable 1'b1: Enable

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Chapter 6 PMU

6.1 Overview

In order to meet low power requirements, a power management unit (PMU) is designed for controlling power resources in SoC. The PMU is dedicated for managing the power of the whole chip.

PMU supports the following features:

- Support multi voltage domains: VD_LITCORE, VD_BIGCORE, VD_GPU, VD_NPU, VD_DDR, VD_LOGIC, VD_PMU
- Support 4 power domains in VD_LITCORE: PD_CPU0, PD_CPU1, PD_CPU2, PD_CPU3
- Support 5 power domains in VD_BIGCORE: PD_CPU4, PD_CPU5, PD_CPU6, PD_CPU7, PD_BIGCORE
- Support 3 power domains in VD_NPU: PD_NPUTOP, PD_NPU0, PD_NPU1
- Support 17 power domains in VD_LOGIC: PD_CENTER, PD_NVM, PD_SDGMAC, PD_USB, PD_AUDIO, PD_VEPU0, PD_VEPU1, PD_VPU, PD_VDEC, PD_VI, PD_VO0, PD_VO1, PD_VOP, PD_VOP_ESMART, PD_VOP_CLUSTER, PD_PHP, PD_SUBPHP
- Support 1 power domain in VD_PMU: PD_PMU1
- Support BIU idle operation by software or hardware
- Support CPU0~CPU7 auto power down
- Support power down/up all power domains by software or hardware
- Support power down/up all voltage domains by software or hardware
- Support global interrupt disable in low power mode
- Support low frequency clock source from PMU PVTM, OSC DIV or external IO
- Support PMU clock switch to low frequency clock in low power mode automatically
- Support PLLs power down/up by hardware in low power mode
- Support OSC enable/disable request in low power mode
- Support DDR self-refresh and retention in low power mode
- Support IO retention in low power mode
- Support varies configurable wakeup source for low power mode
- Support repair for fault memory by software or hardware
- Support power down PPLL/MPHY/DCPHY/HDPTXPHY/USBDPPHY by software

6.2 Block Diagram

The following figure is the PMU block diagram. The PMU includes 3 following sections:

- APB Interface and Register: Provide AMBA APB interface for register read and write
- System Power State Control: Provide power management for various low power modes
- Power Gating Control: Provide power gating control for power domains

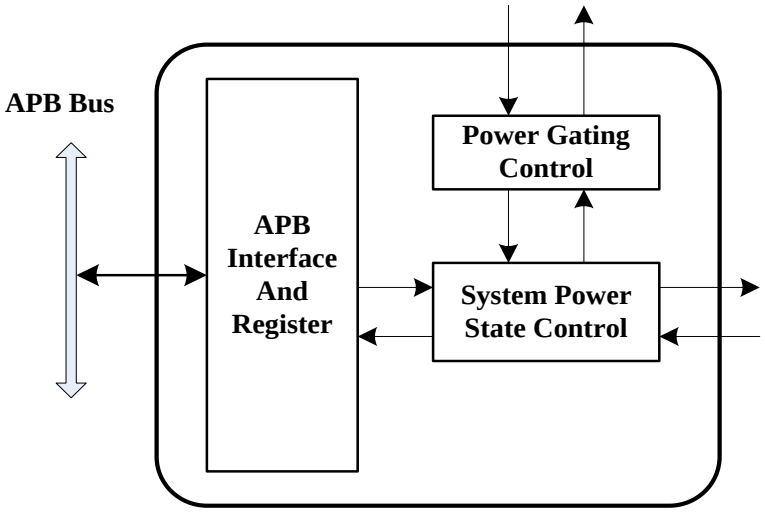

Fig. 6-1 PMU Block Diagram

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6.3 Function Description

6.3.1 Domain Partition

The SoC is divided into different power domains or voltage domains for power management.

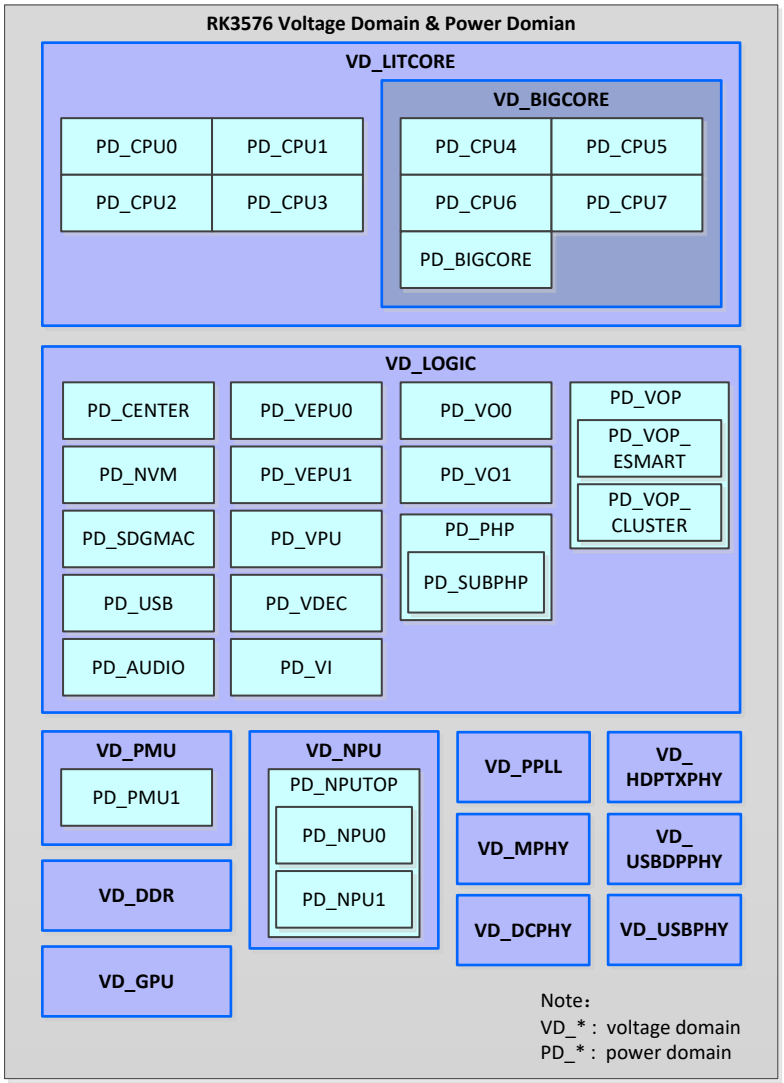

Fig. 6-2 RK3576 Voltage Domain and Power Domain Partition

6.3.2 Domain Description

The following table lists IPs in every domain.

Table 6-1 Domain Description Summary

Voltage Domain	Power Domain	Description
VD_LITCORE	PD_CPU0	CPU0(A53_0)
	PD_CPU1	CPU1(A53_1)
	PD_CPU2	CPU2(A53_2)
	PD_CPU3	CPU3(A53_3)
	PD_LITCORE *(Virtual Power Domain, ALIVE)*	BIU_LITCORE LITCORE_CRU LITCORE_PVTPLL LITCORE_GRF ADB0 SCU0
	PD_CCI *(Virtual Power Domain, ALIVE)*	BIU_CCI BIU_CCI_DDRSCH CCI_CRU CCI_PVTPLL

Voltage Domain	Power Domain	Description
		CCI_GRF CCI CPE DAP_LITE
VD_BIGCORE	PD_CPU4	CPU4(A72_0)
	PD_CPU5	CPU5(A72_1)
	PD_CPU6	CPU6(A72_2)
	PD_CPU7	CPU7(A72_3)
	PD_BIGCORE	BIU_BIGCORE BIGCORE_CRU BIGCORE_PVTPLL BIGCORE_GRF ADB1 SCU1
VD_NPU	PD_NPUTOP	BIU_NPUTOP BIU_NPUSYS NPU_PVTPLL NPU_MCU NPU_WDT NPU_TIMER RKNN_TOP
	PD_NPU0	BIU_NPU0 RKNN_CORE0
	PD_NPU1	BIU_NPU1 RKNN_CORE1
VD_GPU		BIU_GPU GPU GPU_PVTPLL GPU_GRF
VD_DDR		BIU_DDRSCH0 BIU_DDRSCH1 BIU_DDR DDRCTL0~1 DDRPHY0~1 DFI_SCRAMBLE0~1 DDRMON0~1 HWLP0~1 DDR_GRF DDR_MCU DDR_WDT DDR_TIMER DDR0_CRU DDR1_CRU D0APLL D0BPLL D1APLL D1BPLL
VD_PMU	PD_PMU1	BIU_PMU1 PMU1_CRU PMU1_GRF PMU1_SGRF PMU1_IOC PMU1 PMU_MCU PMU_WDT PMU_TIMER

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Voltage Domain	Power Domain	Description
		PMU_SRAM I2C0 PWM0_2CH UART1 OSC_CHK VDMA PDM0 PMUIO1_PMUX
	PD_PMU0 *(ALIVE)*	PMU0_CRU PMU0_GRF PMU0_SGRF PMU0 PMU_PVTM HPTIMER SCRAMBLE_KEY GPIO0 PMU0_IOC PMU0_PMUX PMUIO0_PADRING PMUIO1_PADRING VCCIO7_PMUX VCCIO7_PADRING PPLL_CRU
VD_LOGIC	PD_CENTER	BIU_CENTER_DDRSCH BIU_CENTER_MIAN CENTER_GRF DMA2DDR SYSTEM_SRAM
	PD_NVM	BIU_NVM EMMC FSPI0
	PD_SDGMAC	BIU_SDGMAC SDGMAC_GRF SDMMC SDIO FLEXBUS DSMC GMAC0 GMAC1 FSPI1
	PD_USB	BIU_USB USB_GRF USB0 UFSHC MMU2
	PD_PHP	BIU_PHP PHP_GRF USB1 PCIE0 MMU0 MMU1
	PD_SUBPHP	SATA0 SATA1 PCIE1
	PD_AUDIO	BIU_AUDIO SAI0

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Voltage Domain	Power Domain	Description
		SAI1 SAI2 SAI3 SAI4 ASRC4CH_0 ASRC4CH_1 ASRC2CH_0 ASRC2CH_1 SPDIF_TX0 SPDIF_TX1 SPDIF_RX0 SPDIF_RX1 ACDCDIG_DSM PDM1
	PD_VEPU0	BIU_VEPU0 VEPU0
	PD_VEPU1	BIU_VEPU1 VEPU1
	PD_VPU	BIU_VPU JPEG EBC VDPP RGA0 RGA1
	PD_VDEC	BIU_VDEC VDPU
	PD_VI	BIU_VI VICAP VPSS ISP CSIHOST0 CSIHOST1 CSIHOST2 CSIHOST3 CSIHOST4
	PD_VO0	BIU_VO0 VO0_GRF HDMITX HDCP0 HDCP0_KEY HDCP0_RNG EDP DSIHOST SAI5 SAI6 SPDIF_TX2 SPDIF_RX2
	PD_VO1	BIU_VO1 VO1_GRF HDCP1 HDCP1_KEY HDCP1_RNG DP SAI7 SAI8 SAI9

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Voltage Domain	Power Domain	Description
		SPDIF_TX3 SPDIF_TX4 SPDIF_TX5
	PD_VOP	BIU_VOP BIU_VOP_DDRSCH BIU_VO0VOP_CHANNEL VOP_GRF VOP
	PD_VOP_ESMART	VOP_ESMART0 VOP_ESMART1 VOP_ESMART2 VOP_ESMART3
	PD_VOP_CLUSTER	VOP_CLUSTER0 VOP_CLUSTER1
	PD_BUS *(Virtual Power Domain, ALIVE)*	BIU_TOP BIU_BUS SYS_GRF INTMUX_2PMU INTMUX_2DDR INTMUX_2BUS MAILBOX BUS_WDT BUS_MCU SPINLOCK GIC400 DMAC0~2 DECOM UART0,2~11 SPI0~4 I2C1~9 I3C0~1 CAN0~1 GPIO1~4 PWM1_6CH PWM2_8CH WDT_NS TIMER_NS_0~1 SARADC TSADC CRU PMU2 B/L/S/G/C/AU/VPLL VCCIO0~7_IOC VCCIO0~6_PMUX VCCIO0~6_PAD COMBO_PIPE_PHY0~1 CSIDPHY0~1 DCPHY digital logic USBDPPHY digital logic HDPTXPHY digital logic M-PHY digital logic
	PD_SECURE *(Virtual Power Domain, ALIVE)*	BIU_SECURE SYS_SGRF SECURE_CRU SPLL BOOTROM

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Voltage Domain	Power Domain	Description
		WDT_S TIMER_S_0~1 OTPC_BISR OTPC_NS OTPC_S RKRNG_NS RKRNG_S CRYPTO JTAG_LOCK
VD_PPLL		PPLL
VD_MPHY		M-PHY
VD_DCPHY		DCPHY
VD_HDPTXPHY		HDPTXPHY
VD_USBDPPHY		USBDPPHY
VD_USBPHY		USB2PHY_0 USB2PHY_1

6.3.3 Operation Mode

We define two operation modes of PMU, software power mode and hardware power mode. When operating at software power mode, that means software can manage power sources directly by accessing PMU registers. For example, CPU or MCU can write PMU_PWR_GATE_SFTCON0/1 registers to determine that power off/on which power domain independently.

When operating at hardware power mode, software manages power sources indirectly through FSM (Finite States Machine) in PMU and those settings always not take effect immediately. That means software also can configure PMU registers to power down/up some power resources, but these setting will not be executed immediately after configured. They will be delayed to execute after FSM running in particular phase. And the specific power sources will be controlled during specific status in FSM. So the low power mode is a "delay affect" way to handle power sources inside the chip.

6.3.4 Low Power Mode

There are 2 low power modes defined for RK3576: power mode 0, power mode 1.

Power mode 0: Ultra low power mode. In this power mode, all logic except PMU0_ALIVE in VD_PMU can be power off or power down. Chip can be waked up by GPIO interrupt triggered by PMUIO.

Power mode 1: Normal low power mode. In this power mode, all logic except BUS_ALIVE, SECURE_ALIVE and VD_PMU can be power off or power down. Chip can be waked up by GPIO interrupt triggered by PMUIO or other wakeup sources such as PMU_MCU and PMU_TIMER, etc.

6.4 Register Description

RK3576 PMU registers are divided into 3 parts for flexible applications:

- Offset = 0x00000~0x0FFFF: registers defined in PMU0, in PD_PMU0;
- Offset = 0x10000~0x1FFFF: registers defined in PMU1, in PD_PMU1;
- Offset = 0x20000~0x2FFFF: registers defined in PMU2, in PD_BUS.

6.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU_PWR_CON_P0	0x0000	W	0x00000000	PMU power control mode 0 register
PMU_WAKEUP_INT_CON_P0	0x0008	W	0x00000000	PMU wake up interrupt control register for power mode 0
PMU_WAKEUP_INT_STS_P0	0x000C	W	0x00000000	PMU wake up interrupt status register for power mode 0

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Name	Offset	Size	Reset Value	Description
PMU_PMIC_STABLE_CNT_P0	0x0010	W	0x000FFFFF	PMIC stable count register for power mode 0
PMU_WAKEUP_RST_CLR_CNT_P0	0x0014	W	0x000FFFFF	Wake up reset clear count register for power mode 0
PMU_OSC_STABLE_CNT_P0	0x0018	W	0x000FFFFF	Oscillator stable count register for power mode 0
PMU_PMU1_PWR_CHAIN_STABLE_CON	0x001C	W	0x00003E3F	PD_PMU1 power chain stable control register
PMU_DDR_RET_CON0_P0	0x0020	W	0x00000000	DDR retention control register 0 for power mode 0
PMU_DDR_RET_CON1_P0	0x0024	W	0x00000000	DDR retention control register 1 for power mode 0
PMU_INFO_TX_CON	0x0030	W	0x00000000	PMU information transmit control register
PMU_VERSION	0x10000	W	0x01010002	PMU version register
PMU_PWR_CON_P1	0x10004	W	0x00000000	PMU power control mode 1 register
PMU_GLB_POWER_STS	0x10008	W	0x00000000	PMU global power status register
PMU_INT_MASK_CON	0x1000C	W	0x00000000	PMU interrupt mask control register
PMU_WAKEUP_INT_CON	0x10010	W	0x00000000	PMU wake up interrupt control register
PMU_WAKEUP_INT_STS	0x10014	W	0x00000000	PMU wake up interrupt status register
PMU_DDR_PWR_CON0	0x10100	W	0x00000000	DDR hardware power control register for DDR controller channel 0
PMU_DDR_PWR_CON1	0x10104	W	0x00000000	DDR hardware power control register for DDR controller channel 1
PMU_DDR_PWR_SFTCON0	0x10110	W	0x00000000	DDR software power control register for DDR controller channel 0
PMU_DDR_PWR_SFTCON1	0x10114	W	0x00000000	DDR software power control register for DDR controller channel 1
PMU_DDR_AXIPWR_CON0	0x10120	W	0x00000000	DDR axi-clock domain hardware power control register 0
PMU_DDR_AXIPWR_CON1	0x10124	W	0x00000000	DDR axi-clock domain hardware power control register 1
PMU_DDR_AXIPWR_SFTCON0	0x10130	W	0x00000000	DDR axi-clock domain software power control register 0
PMU_DDR_AXIPWR_SFTCON1	0x10134	W	0x00000000	DDR axi-clock domain software power control register 1
PMU_DDR_AXIPWR_SFTCON2	0x10138	W	0x00000000	DDR axi-clock domain software power control register 2
PMU_DDR_POWER_STS	0x10140	W	0x00000000	DDR power state register
PMU_DDR_STS	0x10144	W	0x00000000	DDR state register
PMU_DDR_AXI_STS	0x10148	W	0x00000000	DDR axi-clock domain state register
PMU_CRU_PWR_CON0	0x10200	W	0x00000000	Clock and reset hardware power control register 0
PMU_CRU_PWR_CON1	0x10204	W	0x00000000	Clock and reset hardware power control register 1

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Name	Offset	Size	Reset Value	Description
PMU_CRU_PWR_SFTCON0	0x10208	W	0x00000000	Clock and reset software power control register 0
PMU_CRU_PWR_SFTCON1	0x1020C	W	0x00000000	Clock and reset hardware power control register 1
PMU_CRU_POWER_STS	0x10210	W	0x00000000	Clock and reset power state register
PMU_PLLPD_CON	0x10220	W	0x00000000	PLL hardware power control register
PMU_PLLPD_SFTCON	0x10228	W	0x00000000	PLL software power control register
PMU_PMIC_STABLE_CNT	0x10300	W	0x000FFFFF	PMIC stable count register
PMU_OSC_STABLE_CNT	0x10304	W	0x000FFFFF	Oscillator stable count register
PMU_WAKEUP_RST_CLR_CNT	0x10308	W	0x000FFFFF	Wake up reset clear count register
PMU_PLL_LOCK_CNT	0x1030C	W	0x000FFFFF	PLL lock count register
PMU_WAKEUP_TIMEOUT_CNT	0x10310	W	0x00005DC0	PMU wake up timeout count register
PMU_WAKEUP_SRC_STABLE_CNT	0x10318	W	0x00005DC0	PMU wakeup source stable count register
PMU_SCU0_PWR_CON	0x20000	W	0x00000200	SCU0 power hardware control register
PMU_SCU1_PWR_CON	0x20004	W	0x00000200	SCU1 power hardware control register
PMU_SCU0_PWR_SFTCON	0x20008	W	0x00000000	SCU0 power software control register
PMU_SCU1_PWR_SFTCON	0x2000C	W	0x00000000	SCU1 power software control register
PMU_SCU0_AUTO_CON	0x20010	W	0x00000000	SCU0 power auto control register
PMU_SCU1_AUTO_CON	0x20014	W	0x00000000	SCU1 power auto control register
PMU_SCU_POWER_STS	0x20018	W	0x00000000	SCU power state register
PMU_CLUSTER_PWR_ST	0x20024	W	0x00000000	Cluster power state register
PMU_CLUSTER0_IDLE_CON	0x20028	W	0x00000000	Cluster0 idle control register
PMU_CLUSTER1_IDLE_CON	0x2002C	W	0x00000000	Cluster1 idle control register
PMU_CLUSTER0_IDLE_SFTCON	0x20030	W	0x00000000	Cluster0 idle software control register
PMU_CLUSTER1_IDLE_SFTCON	0x20034	W	0x00000000	Cluster1 idle software control register
PMU_CLUSTER_IDLE_ACK	0x20038	W	0x00000000	Cluster idle acknowledge register
PMU_CLUSTER_IDLE_ST	0x2003C	W	0x00000000	Cluster idle state register
PMU_CORE0_STABLE_CNT	0x20048	W	0x000FFFFF	VD_LITCORE power stable counter register
PMU_CORE1_STABLE_CNT	0x20054	W	0x000FFFFF	VD_BIGCORE power stable counter register
PMU_CPU0_AUTO_PWR_CON	0x20080	W	0x00000000	CPU0 power automatic control register
PMU_CPU1_AUTO_PWR_CON	0x20084	W	0x00000000	CPU1 power automatic control register
PMU_CPU2_AUTO_PWR_CON	0x20088	W	0x00000000	CPU2 power automatic control register
PMU_CPU3_AUTO_PWR_CON	0x2008C	W	0x00000000	CPU3 power automatic control register

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Name	Offset	Size	Reset Value	Description
PMU_CPU4_AUTO_PWR_CON	0x20090	W	0x00000000	CPU4 power automatic control register
PMU_CPU5_AUTO_PWR_CON	0x20094	W	0x00000000	CPU5 power automatic control register
PMU_CPU6_AUTO_PWR_CON	0x20098	W	0x00000000	CPU6 power automatic control register
PMU_CPU7_AUTO_PWR_CON	0x2009C	W	0x00000000	CPU7 power automatic control register
PMU_CPU0_PWR_SFTCON	0x200A0	W	0x00000000	CPU0 power software control register
PMU_CPU1_PWR_SFTCON	0x200A4	W	0x00000000	CPU1 power software control register
PMU_CPU2_PWR_SFTCON	0x200A8	W	0x00000000	CPU2 power software control register
PMU_CPU3_PWR_SFTCON	0x200AC	W	0x00000000	CPU3 power software control register
PMU_CPU4_PWR_SFTCON	0x200B0	W	0x00000000	CPU4 power software control register
PMU_CPU5_PWR_SFTCON	0x200B4	W	0x00000000	CPU5 power software control register
PMU_CPU6_PWR_SFTCON	0x200B8	W	0x00000000	CPU6 power software control register
PMU_CPU7_PWR_SFTCON	0x200BC	W	0x00000000	CPU7 power software control register
PMU_CCI_PWR_CON	0x200E0	W	0x00000008	CCI power hardware control register
PMU_CCI_PWR_SFTCON	0x200E4	W	0x00000000	CCI power software control register
PMU_CCI_PWR_ST	0x200E8	W	0x00000000	CCI power state
PMU_CCI_POWER_STS	0x200EC	W	0x00000000	CCI power state register
PMU_BIU_IDLE_CON0	0x20100	W	0x00000000	BIU idle request hardware control register 0
PMU_BIU_IDLE_CON1	0x20104	W	0x00000000	BIU idle request hardware control register 1
PMU_BIU_IDLE_SFTCON0	0x20110	W	0x00000000	BIU idle request software control register 0
PMU_BIU_IDLE_SFTCON1	0x20114	W	0x00000000	BIU idle request software control register 1
PMU_BIU_IDLE_ACK_STS	0x20120	W	0x00000000	BIU idle acknowledge status register
PMU_BIU_IDLE_STS	0x20128	W	0x00000000	BIU idle status register
PMU_BIU_GATMASK_CON0	0x20130	W	0x00000000	BIU clock gate mask hardware control register 0
PMU_BIU_GATMASK_CON1	0x20134	W	0x00000000	BIU clock gate mask hardware control register 1
PMU_BIU_GATMASK_SFTCON0	0x20140	W	0x00000000	BIU clock gate mask software control register 0
PMU_BIU_GATMASK_SFTCON1	0x20144	W	0x00000000	BIU clock gate mask software control register 1
PMU_BIU_IDLEACK_BYPASS_CON	0x20150	W	0x00000000	BIU idle acknowledge bypass control register
PMU_PWR_GATE_CON0	0x20200	W	0x00000000	Power domain hardware power control register 0

Name	Offset	Size	Reset Value	Description
PMU_PWR_GATE_CON1	0x20204	W	0x00000000	Power domain hardware power control register 1
PMU_PWR_GATE_SFTCON0	0x20210	W	0x00000000	Power domain software power control register 0
PMU_PWR_GATE_SFTCON1	0x20214	W	0x00000200	Power domain software power control register 1
PMU_VOL_GATE_CON0	0x20220	W	0x00000000	Voltage domain hardware power control register 0
PMU_VOL_GATE_CON1	0x20224	W	0x00000000	Voltage domain hardware power control register 1
PMU_PWR_GATE_STS	0x20230	W	0x02000000	Power domain power status register
PMU_PWR_GATE_POWER_STS	0x20238	W	0x00000000	Power gating status register
PMU_PWR_CHAIN0_STS0	0x20240	W	0xBDFFFFC8	Power chain 0 power status register 0
PMU_PWR_CHAIN0_STS1	0x20244	W	0x0000000F	Power chain 0 power status register 1
PMU_PWR_CHAIN1_STS0	0x20248	W	0xBDFFFFC8	Power chain 1 power status register 0
PMU_PWR_CHAIN1_STS1	0x2024C	W	0x0000000F	Power chain 1 power status register 1
PMU_PWR_MEM_STS0	0x20250	W	0x00000000	Memory power status register 0
PMU_PWR_MEM_STS1	0x20254	W	0x00000000	Memory power status register 1
PMU_PWR_CHAIN_PWRUP_CON0	0x20260	W	0x0000FFC8	Power chain stable control register 0 for power up
PMU_PWR_CHAIN_PWRUP_CON1	0x20264	W	0x0000BDFF	Power chain stable control register 1 for power up
PMU_PWR_CHAIN_PWRUP_CON2	0x20268	W	0x0000000F	Power chain stable control register 2 for power up
PMU_PWR_CHAIN_PWRDN_CON0	0x20270	W	0x00000000	Power chain stable control register 0 for power down
PMU_PWR_CHAIN_PWRDN_CON1	0x20274	W	0x00000000	Power chain stable control register 1 for power down
PMU_PWR_CHAIN_PWRDN_CON2	0x20278	W	0x00000000	Power chain stable control register 2 for power down
PMU_PWR_STABLE_CNT_THRES	0x2027C	W	0x001F001F	Power chain stable count register
PMU_VOL_GATE_FAST_CON	0x20284	W	0x00000000	Voltage domain fast power control register
PMU_NPU_PWRUP_CNT	0x20288	W	0x000FFFFF	VD_NPU power up count register
PMU_NPU_PWRDN_CNT	0x2028C	W	0x000FFFFF	VD_NPU power down count register
PMU_LITCORE_PWRUP_CNT	0x20290	W	0x000FFFFF	VD_LITCORE power up count register
PMU_LITCORE_PWRDN_CNT	0x20294	W	0x000FFFFF	VD_LITCORE power down count register
PMU_GPU_PWRUP_CNT	0x20298	W	0x000FFFFF	VD_GPU power up count register
PMU_GPU_PWRDN_CNT	0x2029C	W	0x000FFFFF	VD_GPU power down count register
PMU_MEM_PWR_GATE_SFTCON0	0x20300	W	0x00000000	Memory software power control register 0
PMU_MEM_PWR_GATE_SFTCON1	0x20304	W	0x00000000	Memory software power control register 1

Name	Offset	Size	Reset Value	Description
PMU_PWR_C0_ACK_SEL_CON0	0x20380	W	0x00000000	Power chain 0 acknowledge selection control register 0
PMU_PWR_C0_ACK_SEL_CON1	0x20384	W	0x00000000	Power chain 0 acknowledge selection control register 1
PMU_PWR_C0_ACK_SEL_CON2	0x20388	W	0x00000000	Power chain 0 acknowledge selection control register 2
PMU_PWR_C1_ACK_SEL_CON0	0x20390	W	0x00000000	Power chain 1 acknowledge selection control register 0
PMU_PWR_C1_ACK_SEL_CON1	0x20394	W	0x00000000	Power chain 1 acknowledge selection control register 1
PMU_PWR_C1_ACK_SEL_CON2	0x20398	W	0x00000000	Power chain 1 acknowledge selection control register 2
PMU_PWR_MEM_ACK_SEL_CON0	0x203A0	W	0x00000000	Memory power acknowledge selection control register 0
PMU_PWR_MEM_ACK_SEL_CON1	0x203A4	W	0x00000000	Memory power acknowledge selection control register 1
PMU_PWR_MEM_ACK_SEL_CON2	0x203A8	W	0x00000000	Memory power acknowledge selection control register 2
PMU_DEBUG_INFO_CON	0x203F0	W	0x00000000	PMU debug information control register
PMU_BISR_GLB_CON	0x20500	W	0x00000203	Memory repair global control register
PMU_BISR_TIMEOUT_THRES	0x20504	W	0xFFFFFFFF	Memory repair threshold timeout register
PMU_BISR_PDGEN_CON0	0x20510	W	0x0000FFFF	Memory repair hardware control register 0
PMU_BISR_PDGEN_CON1	0x20514	W	0x0000FDFF	Memory repair hardware control register 1
PMU_BISR_PDGEN_CON2	0x20518	W	0x0000000F	Memory repair hardware control register 2
PMU_BISR_PDGEN_SFTCON0	0x20520	W	0x00000000	Memory repair software control register 0
PMU_BISR_PDGEN_SFTCON1	0x20524	W	0x00000000	Memory repair software control register 1
PMU_BISR_PDGEN_SFTCON2	0x20528	W	0x00000000	Memory repair software control register 2
PMU_BISR_PDGDONE_SFTCON0	0x20530	W	0x00000000	Memory repair PDGDone software control register 0
PMU_BISR_PDGDONE_SFTCON1	0x20534	W	0x00000000	Memory repair PDGDone software control register 1
PMU_BISR_PDGDONE_SFTCON2	0x20538	W	0x00000000	Memory repair PDGDone software control register 2
PMU_BISR_INITRST_SFTCON0	0x20540	W	0x00000000	Memory repair initial reset software control register 0
PMU_BISR_INITRST_SFTCON1	0x20544	W	0x00000000	Memory repair initial reset software control register 1
PMU_BISR_INITRST_SFTCON2	0x20548	W	0x00000000	Memory repair initial reset software control register 2
PMU_BISR_PDGDONE_STATUS0	0x20550	W	0x00000000	Memory repair PDGDone status register 0
PMU_BISR_PDGDONE_STATUS1	0x20554	W	0x00000000	Memory repair PDGDone status register 1
PMU_BISR_PDGCEDIS_STATUS0	0x20560	W	0x00000000	Memory repair PDGCedis status register 0

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Name	Offset	Size	Reset Value	Description
PMU_BISR_PDGCEDIS_STATUS1	0x20564	W	0x00000000	Memory repair PDGCedis status register 1
PMU_BISR_PWR_REPAIR_STATUS0	0x20570	W	0x00000000	Memory power and repair status register 0
PMU_BISR_PWR_REPAIR_STATUS1	0x20574	W	0x00000000	Memory power and repair status register 1
PMU_BISR_GLB_STATUS	0x20580	W	0x00000000	Memory repair global status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

6.4.2 Detail Registers Description

PMU_PWR_CON_P0

Address: Operational Base(0x27360000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	io_sleep_ena Enable IO enter low power mode(retention mode) by hardware. 1'b0: Disable 1'b1: Enable
13	RW	0x0	gate_mask_pmu1_ena If enable, BIU_PMU1 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pmu1_bus_idle_sftena Enable sending idle request to BIU_PMU1 by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pmu1_bus_idle_ena Enable sending idle request to BIU_PMU1 by hardware. 1'b0: Disable 1'b1: Enable
10	RO	0x0	reserved
9	RW	0x0	pmu1_pwr_gate_sftena Enable power down PD_PMU1 by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pmu1_pwr_gate_ena Enable power down PD_PMU1 by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	osc_dis_bypass Bypass disable oscillator in power mode 0 procedure. If asserted, the oscillator cannot be disabled by FSM during power mode 0 procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x0	freq_switch_bypass Bypass frequency switch stability in power mode 0 procedure. If asserted, clk_pmu cannot be switched to 32KHz clock source during power mode 0 procedure. 1'b0: Disable 1'b1: Enable
5	RW	0x0	reset_bypass Bypass wake up reset clear stability in power mode 0 procedure. If asserted, the FSM will enter next state not wait for reset counter, and chip will not be reset. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pmic_bypass Bypass waiting for PMIC stability in power mode 0 procedure. If asserted, the FSM will enter next state without waiting until PMIC is stable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	wakeup_bypass Bypass waiting for wakeup source in power mode 0 procedure. If asserted, the FSM will exit sleep state without waiting for wakeup source. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pmu1_bus_bypass Bypass BIU_PMU1 idle flow in power mode 0 procedure. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pmu1_pwr_bypass Bypass PD_PMU1 power gating flow in power mode 0 procedure. If asserted, PD_PMU1 is not power down or power up during power mode 0 procedure. 1'b0: Disable 1'b1: Enable
0	R/WSC	0x0	powermode0_en Power mode 0 enable. When controller enters power mode 0 procedure, this bit is automatically cleared. 1'b0: Disable 1'b1: Enable

PMU_WAKEUP_INT_CON_P0

Address: Operational Base(0x27360000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	hptimer_wakeup_int_en Enable HPTIMER timeout interrupt as wakeup source to exit power mode 0 procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpio_wakeup_int_en Enable GPIO interrupt as wakeup source to exit power mode 0 procedure. 1'b0: Disable 1'b1: Enable

PMU_WAKEUP_INT_STS_P0

Address: Operational Base(0x27360000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	hptimer_wakeup_int_st Power mode 0 HPTIMER wakeup source status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	gpio_wakeup_int_st Power mode 0 GPIO wakeup source status. 1'b0: Inactive 1'b1: Active

PMU_PMIC_STABLE_CNT_P0

Address: Operational Base(0x27360000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pmic_stable_cnt PMIC stable count for power mode 0 procedure. Number of clk_pmu used by counter logic.

PMU_WAKEUP_RST_CLR_CNT_P0

Address: Operational Base(0x27360000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	wakeup_rst_clr_cnt Wake up reset clear count for power mode 0 procedure. Number of clk_pmu used by counter logic.

PMU_OSC_STABLE_CNT_P0

Address: Operational Base(0x27360000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	osc_stable_cnt Oscillator stable count for power mode 0 procedure. Number of clk_pmu used by counter logic.

PMU_PMU1_PWR_CHAIN_STABLE_CON

Address: Operational Base(0x27360000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:9	RW	0x1f	pmu1_pwr_dwn_stable_cnt Stable count for PD_PMU1 power down flow. Number of clk_pmu used by counter logic.

Bit	Attr	Reset Value	Description
8	RW	0x0	pmu1_pwr_dwn_stable_en Enable stable counter between power chains for PD_PMU1 power down flow. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:1	RW	0x1f	pmu1_pwr_up_stable_cnt Stable count for PD_PMU1 power up flow. Number of clk_pmu used by counter logic.
0	RW	0x1	pmu1_pwr_up_stable_en Enable stable counter between power chains for PD_PMU1 power up flow. 1'b0: Disable 1'b1: Enable

PMU_DDR_RET_CON0_P0

Address: Operational Base(0x27360000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	ddrio_rstiov_exit_ena Enable DDR exits retention mode through RST_IOV by hardware in power mode 0 procedure. Bit[12] used for DDR channel 0. Bit[13] used for DDR channel 1. 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9:8	RW	0x0	ddrio_reton_exit_ena Enable DDR exits retention mode through RETON/RETOFF by hardware in power mode 0 procedure. Bit[8] used for DDR channel 0. Bit[9] used for DDR channel 1. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:4	RW	0x0	ddrio_rstiov_enter_ena Enable DDR enters retention mode through RST_IOV by hardware in power mode 0 procedure. Bit[4] used for DDR channel 0. Bit[5] used for DDR channel 1. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	ddrio_reton_enter_ena Enable DDR enters retention mode through RETON/RETOFF by hardware in power mode 0 procedure. Bit[0] used for DDR channel 0. Bit[1] used for DDR channel 1. 1'b0: Disable 1'b1: Enable

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PMU_DDR_RET_CON1_P0

Address: Operational Base(0x27360000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	ddrio_rstiov_exit_sftena Enable DDR exits retention mode through RST_IOV by software. Bit[12] used for DDR channel 0. Bit[13] used for DDR channel 1. 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9:8	RW	0x0	ddrio_reton_exit_sftena Enable DDR exits retention mode through RETON/RETOFF by software. Bit[8] used for DDR channel 0. Bit[9] used for DDR channel 1. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:4	RW	0x0	ddrio_rstiov_enter_sftena Enable DDR enters retention mode through RST_IOV by software. Bit[4] used for DDR channel 0. Bit[5] used for DDR channel 1. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	ddrio_reton_enter_sftena Enable DDR enters retention mode through RETON/RETOFF by software. Bit[0] used for DDR channel 0. Bit[1] used for DDR channel 1. 1'b0: Disable 1'b1: Enable

PMU_INFO_TX_CON

Address: Operational Base(0x27360000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	info_tx_en Enable PMU information transition. 1'b0: Disable 1'b1: Enable
7:0	RW	0x00	info_tx_intv_time The interval time between the bytes of PMU information.

PMU_VERSION

Address: Operational Base(0x27360000) + offset (0x10000)

Bit	Attr	Reset Value	Description
31:0	RO	0x01010002	version PMU version

PMU_PWR_CON_P1

Address: Operational Base(0x27360000) + offset (0x10004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	wakeup_src_stable_cnt_en PMU wakeup source stable count enable. 1'b0: PMU FSM will exit sleep mode as soon as the wakeup source is valid 1'b1: PMU FSM will not exit sleep mode unitl wakeup source is valid and wakeup source stable counter is count to 0
12	RW	0x0	wfi_bypass Bypass WFI in power mode 1 procedure. If asserted, PMU FSM does not need to wait for CPU standbywfi state before executing low power flow. 1'b0: Disable 1'b1: Enable
11:8	RO	0x0	reserved
7	RW	0x0	cru_bypass Bypass clock and reset low power flow in power mode 1 procedure. If asserted, PMU_CRU_PWR_CON* cannot take effect for clock and reset low power flow. If you want to execute clock and reset low power flow, you can program PMU_CRU_PWR_SFTCON* through software flow. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pwrgate_bypass Bypass power gating flow in power mode 1 procedure. If asserted, PMU_PWR_GATE_CON* cannot take effect for power gating flow. If you want to execute power gating flow, you can program PMU_PWR_GATE_SFTCON* through software flow. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddr_bypass Bypass DDR low power flow in power mode 1 procedure. If asserted, PMU_DDR_PWR_CON* cannot take effect for DDR low power flow. If you want to execute DDR low power flow, you can program PMU_DDR_PWR_SFTCON* through software flow. 1'b0: Disable 1'b1: Enable
4	RW	0x0	bus_bypass Bypass BIU idle request in power mode 1 procedure. If asserted, PMU_BIU_IDLE_CON* cannot take effect for BIU idle request. If you want to execute BIU idle request, you can program PMU_BIU_IDLE_SFTCON* through software flow. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	cci_bypass Bypass CCI low power flow in power mode 1 procedure. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu1_bypass Bypass SCU1 low power flow in power mode 1 procedure. 1'b0: Disable 1'b1: Enable
1	RW	0x0	scu0_bypass Bypass SCU0 low power flow in power mode 1 procedure. 1'b0: Disable 1'b1: Enable
0	R/WSC	0x0	powermode1_en Power mode 1 enable. When controller enters power mode 1 procedure, this bit is automatically cleared. 1'b0: Disable 1'b1: Enable

PMU_GLB_POWER_STS

Address: Operational Base(0x27360000) + offset (0x10008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	power_state PMU1 global power state. 4'h0: Normal state 4'h1: SCU low power state 4'h2: CCI low power state 4'h4: Bus low power state 4'h5: DDR low power state 4'h6: Power gating low power state 4'h7: Clock and reset low power state 4'h8: Sleep state 4'h9: Clock and reset active state 4'ha: Power gating active state 4'hb: DDR active state 4'hc: Bus active state 4'hd: CCI active state 4'hf: SCU active state

PMU_INT_MASK_CON

Address: Operational Base(0x27360000) + offset (0x1000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	R/WSC	0x0	glb_int_mask_ena Global interrupt mask enable. 1'b0: Interrupt is not masked, SCU0/1 will be wakeup if wakeup source is valid. 1'b1: Interrupt is masked, SCU0/1 will not be wakeup if wakeup source is valid.

PMU_WAKEUP_INT_CON

Address: Operational Base(0x27360000) + offset (0x10010)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	wakeup_timeout_en Enable PMU timeout as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
19	RW	0x0	wakeup_saradc_int_en Enable SARADC interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
18	RW	0x0	wakeup_hptimer_int_en Enable HPTIMER timeout interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
17	RW	0x0	wakeup_tsadc_int_en Enable TSADC interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
16	RW	0x0	wakeup_pwmir_int_en Enable PWMIR interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
15	RW	0x0	wakeup_sys_int_en Enable system interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
14	RW	0x0	wakeup_timer_int_en Enable PMU_TIMER interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
13	RW	0x0	wakeup_mcu_int_en Enable MCU interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
12	RW	0x0	wakeup_uart1_int_en Enable UART1 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
11	RW	0x0	wakeup_usb_int_en Enable USB detect interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
10	RW	0x0	wakeup_sdio_int_en Enable SDIO interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
9	RW	0x0	wakeup_sdmmc_int_en Enable SDMMC detect interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
8	RW	0x0	wakeup_gpio0_int_en Enable GPIO0 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
7	RW	0x0	wakeup_cpu7_int_en Enable CPU7 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
6	RW	0x0	wakeup_cpu6_int_en Enable CPU6 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
5	RW	0x0	wakeup_cpu5_int_en Enable CPU5 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
4	RW	0x0	wakeup_cpu4_int_en Enable CPU4 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
3	RW	0x0	wakeup_cpu3_int_en Enable CPU3 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_cpu2_int_en Enable CPU2 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
1	RW	0x0	wakeup_cpu1_int_en Enable CPU1 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
0	RW	0x0	wakeup_cpu0_int_en Enable CPU0 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable

PMU_WAKEUP_INT_STS

Address: Operational Base(0x27360000) + offset (0x10014)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20	RO	0x0	wakeup_timeout_st PMU timeout as wakeup source status. 1'b0: Inactive 1'b1: Active
19	RO	0x0	wakeup_saradc_int_st SARADC interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
18	RO	0x0	wakeup_hptimer_int_st HPTIMER interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
17	RO	0x0	wakeup_tsadc_int_st TSADC interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
16	RO	0x0	wakeup_pwmir_int_st PWMIR interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
15	RO	0x0	wakeup_sys_int_st System interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
14	RO	0x0	wakeup_timer_int_st PMU_TIMER interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
13	RO	0x0	wakeup_mcu_int_st MCU interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
12	RO	0x0	wakeup_uart1_int_st UART1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
11	RO	0x0	wakeup_usb_int_st USB detect interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
10	RO	0x0	wakeup_sdio_int_st SDIO interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
9	RO	0x0	wakeup_sdmmc_int_st SDMMC detect interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	wakeup_gpio0_int_st GPIO0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	wakeup_cpu7_int_st CPU7 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
6	RO	0x0	wakeup_cpu6_int_st CPU6 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	wakeup_cpu5_int_st CPU5 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	wakeup_cpu4_int_st CPU4 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	wakeup_cpu3_int_st CPU3 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
2	RO	0x0	wakeup_cpu2_int_st CPU2 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	wakeup_cpu1_int_st CPU1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	wakeup_cpu0_int_st CPU0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active

PMU_DDR_PWR_CON0

Address: Operational Base(0x27360000) + offset (0x10100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	ddrphy_auto_gating_ena Enable DDRPHY auto clock gating. DDRPHY's clock can be gated when in low power mode. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddrctl_c_auto_gating_ena Enable DDRCTRL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode. 1'b0: Disable 1'b1: Enable
4	RW	0x0	ddrio_rstiov_exit_ena Enable DDR exits retention mode through RST_IOV by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	ddrio_rstiov_enter_ena Enable DDR enters retention mode through RST_IOV by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	ddrio_reton_exit_ena Enable DDR exits retention mode through RETON/RETOFF by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddrio_reton_enter_ena Enable DDR enters retention mode through RETON/RETOFF by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_c_ena Enable DDR self-refresh mode for core-clock domain by hardware. 1'b0: Disable 1'b1: Enable

PMU_DDR_PWR_CON1

Address: Operational Base(0x27360000) + offset (0x10104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	ddrphy_auto_gating_ena Enable DDRPHY auto clock gating. DDRPHY's clock can be gated when in low power mode. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddrctl_c_auto_gating_ena Enable DDRCTRL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode. 1'b0: Disable 1'b1: Enable
4	RW	0x0	ddrio_rstiov_exit_ena Enable DDR exits retention mode through RST_IOV by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	ddrio_rstiov_enter_ena Enable DDR enters retention mode through RST_IOV by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	ddrio_reton_exit_ena Enable DDR exits retention mode through RETON/RETOFF by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	ddrio_reton_enter_ena Enable DDR enters retention mode through RETON/RETOFF by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_c_ena Enable DDR self-refresh mode for core-clock domain by hardware. 1'b0: Disable 1'b1: Enable

PMU_DDR_PWR_SFTCON0

Address: Operational Base(0x27360000) + offset (0x10110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	ddrctl_c_active_wait_enter 1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state
5	RW	0x0	ddrctl_c_active_wait_exit 1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state
4	R/WSC	0x0	ddrio_rstiov_exit_sftena Enable DDR exits retention mode through RST_IOV by software. It is auto cleared after DDR exits retention mode. 1'b0: Disable 1'b1: Enable
3	RW	0x0	ddrio_rstiov_enter_sftena Enable DDR enters retention mode through RST_IOV by software. 1'b0: Disable 1'b1: Enable
2	R/WSC	0x0	ddrio_reton_exit_sftena Enable DDR exits retention mode through RETON/RETOFF by software. It is auto cleared after DDR exits retention mode. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddrio_reton_enter_sftena Enable DDR enters retention mode through RETON/RETOFF by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_c_sftena Enable DDR self-refresh mode for core-clock domain by software. 1'b0: Disable 1'b1: Enable

PMU_DDR_PWR_SFTCON1

Address: Operational Base(0x27360000) + offset (0x10114)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	ddrctl_c_active_wait_enter 1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state
5	RW	0x0	ddrctl_c_active_wait_exit 1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state
4	R/WSC	0x0	ddrio_rstiov_exit_sftena Enable DDR exits retention mode through RST_IOV by software. It is auto cleared after DDR exits retention mode. 1'b0: Disable 1'b1: Enable
3	RW	0x0	ddrio_rstiov_enter_sftena Enable DDR enters retention mode through RST_IOV by software. 1'b0: Disable 1'b1: Enable
2	R/WSC	0x0	ddrio_reton_exit_sftena Enable DDR exits retention mode through RETON/RETOFF by software. It is auto cleared after DDR exits retention mode. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddrio_reton_enter_sftena Enable DDR enters retention mode through RETON/RETOFF by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_c_sftena Enable DDR self-refresh mode for core-clock domain by software. 1'b0: Disable 1'b1: Enable

PMU_DDR_AXIPWR_CON0

Address: Operational Base(0x27360000) + offset (0x10120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	ddr_sref_a_ena Enable DDR self-refresh mode for AXI-clock domain by hardware. Bit[i] used for AXI-clock channel i, i=0~9. 1'b0: Disable 1'b1: Enable

PMU_DDR_AXIPWR_CON1

Address: Operational Base(0x27360000) + offset (0x10124)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	ddrctl_a_auto_gating_ena Enable DDRCTRL's AXI-clock auto clock gating. AXI-clock can be gated when in self-refresh mode. Bit[i] used for AXI-clock channel i, i=0~9. 1'b0: Disable 1'b1: Enable

PMU_DDR_AXIPWR_SFTCON0

Address: Operational Base(0x27360000) + offset (0x10130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	ddr_sref_a_sftena Enable DDR self-refresh mode for AXI-clock domain by software. Bit[i] used for AXI-clock channel i, i=0~9. 1'b0: Disable 1'b1: Enable

PMU_DDR_AXIPWR_SFTCON1

Address: Operational Base(0x27360000) + offset (0x10134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	ddrctl_a_active_wait_enter Bit[i] used for AXI-clock channel i, i=0~9. 1'b0: Not need to wait for ddrctl_a_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_a_active low before FSM enter self-refresh state

PMU_DDR_AXIPWR_SFTCON2

Address: Operational Base(0x27360000) + offset (0x10138)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	ddrctl_a_active_wait_exit Bit[i] used for AXI-clock channel i, i=0~9. 1'b0: Not need to wait for ddrctl_a_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_a_active high before FSM exit self-refresh state

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PMU_DDR_POWER_STS

Address: Operational Base(0x27360000) + offset (0x10140)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	ddr_power_state DDR power state. 4'h0: Normal state 4'h1: Enter self-refresh mode for AXI-clock state 4'h2: Enter self-refresh mode core-clock state 4'h3: Enter retention mode through RETON/RETOFF state 4'h4: Enter retention mode through RST_IOV state 4'h5: Sleep state 4'h6: Exit retention mode through RST_IOV state 4'h7: Exit retention mode through RETON/RETOFF state 4'h8: Exit self-refresh mode for core-clock state 4'h9: Exit self-refresh mode for AXI-clock state Others: Reserved

PMU_DDR_STS

Address: Operational Base(0x27360000) + offset (0x10144)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	ddrctrl_c_sysactive_ch1 DDRC hardware low-power clock active for channel 1. 1'b0: Inactive 1'b1: Active
6	RO	0x0	ddrctrl_c_sysack_ch1 DDRC hardware low-power request acknowledge for channel 1. 1'b0: Inactive 1'b1: Active
5	RO	0x0	ddr_io_rstiov_ch1 DDR RST_IOV state for channel 1. 1'b0: Inactive 1'b1: Active
4	RO	0x0	ddr_io_reton_ch1 DDR RETON/RETOFF state for channel 1. 1'b0: Inactive 1'b1: Active
3	RO	0x0	ddrctrl_c_sysactive_ch0 DDRC hardware low-power clock active for channel 0. 1'b0: Inactive 1'b1: Active
2	RO	0x0	ddrctrl_c_sysack_ch0 DDRC hardware low-power request acknowledge for channel 0. 1'b0: Inactive 1'b1: Active
1	RO	0x0	ddr_io_rstiov_ch0 DDR RST_IOV state for channel 0. 1'b0: Inactive 1'b1: Active
0	RO	0x0	ddr_io_reton_ch0 DDR RETON/RETOFF state for channel 0. 1'b0: Inactive 1'b1: Active

PMU_DDR_AXI_STS

Address: Operational Base(0x27360000) + offset (0x10148)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RO	0x0	ddrctrl_a_sysactive_ch9 DDRC AXI clock active for channel 9. 1'b0: Inactive 1'b1: Active
18	RO	0x0	ddrctrl_a_sysack_ch9 DDRC AXI hardware low-power request acknowledge for channel 9. 1'b0: Inactive 1'b1: Active
17	RO	0x0	ddrctrl_a_sysactive_ch8 DDRC AXI clock active for channel 8. 1'b0: Inactive 1'b1: Active
16	RO	0x0	ddrctrl_a_sysack_ch8 DDRC AXI hardware low-power request acknowledge for channel 8. 1'b0: Inactive 1'b1: Active
15	RO	0x0	ddrctrl_a_sysactive_ch7 DDRC AXI clock active for channel 7. 1'b0: Inactive 1'b1: Active
14	RO	0x0	ddrctrl_a_sysack_ch7 DDRC AXI hardware low-power request acknowledge for channel 7. 1'b0: Inactive 1'b1: Active
13	RO	0x0	ddrctrl_a_sysactive_ch6 DDRC AXI clock active for channel 6. 1'b0: Inactive 1'b1: Active
12	RO	0x0	ddrctrl_a_sysack_ch6 DDRC AXI hardware low-power request acknowledge for channel 6. 1'b0: Inactive 1'b1: Active
11	RO	0x0	ddrctrl_a_sysactive_ch5 DDRC AXI clock active for channel 5. 1'b0: Inactive 1'b1: Active
10	RO	0x0	ddrctrl_a_sysack_ch5 DDRC AXI hardware low-power request acknowledge for channel 5. 1'b0: Inactive 1'b1: Active
9	RO	0x0	ddrctrl_a_sysactive_ch4 DDRC AXI clock active for channel 4. 1'b0: Inactive 1'b1: Active
8	RO	0x0	ddrctrl_a_sysack_ch4 DDRC AXI hardware low-power request acknowledge for channel 4. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
7	RO	0x0	ddrctrl_a_sysactive_ch3 DDRC AXI clock active for channel 3. 1'b0: Inactive 1'b1: Active
6	RO	0x0	ddrctrl_a_sysack_ch3 DDRC AXI hardware low-power request acknowledge for channel 3. 1'b0: Inactive 1'b1: Active
5	RO	0x0	ddrctrl_a_sysactive_ch2 DDRC AXI clock active for channel 2. 1'b0: Inactive 1'b1: Active
4	RO	0x0	ddrctrl_a_sysack_ch2 DDRC AXI hardware low-power request acknowledge for channel 2. 1'b0: Inactive 1'b1: Active
3	RO	0x0	ddrctrl_a_sysactive_ch1 DDRC AXI clock active for channel 1. 1'b0: Inactive 1'b1: Active
2	RO	0x0	ddrctrl_a_sysack_ch1 DDRC AXI hardware low-power request acknowledge for channel 1. 1'b0: Inactive 1'b1: Active
1	RO	0x0	ddrctrl_a_sysactive_ch0 DDRC AXI clock active for channel 0. 1'b0: Inactive 1'b1: Active
0	RO	0x0	ddrctrl_a_sysack_ch0 DDRC AXI hardware low-power request acknowledge for channel 0. 1'b0: Inactive 1'b1: Active

PMU_CRU_PWR_CON0

Address: Operational Base(0x27360000) + offset (0x10200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	io_sleep_ena Enable IO enter low power mode(retention mode) by hardware. 1'b0: Disable 1'b1: Enable
8:6	RO	0x0	reserved
5	RW	0x0	power_off_ena Enable chip power off by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	alive_osc_ena Enable clk_pmu/hclk_pmu/pclk_pmu switch to oscillator by hardware. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_ena Enable VD_PMU input clamped by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_ena Enable wake up reset by hardware. If asserted, all registers without reset hold will be reset after chip wake up. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_ena Disable oscillator by hardware. 1'b0: Enable 1'b1: Disable
0	RW	0x0	alive_32k_ena Enable pclk_pmu and clk_pmu switch to 32KHz clock by hardware. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_CON1

Address: Operational Base(0x27360000) + offset (0x10204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	cci_clk_gate_ena Enable PD_CCI clock gate by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	secure_clk_gate_ena Enable PD_SECURE clock gate by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	bus_clk_gate_ena Enable PD_BUS clock gate by hardware. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_SFTCON0

Address: Operational Base(0x27360000) + offset (0x10208)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	io_sleep_sftena Enable IO enter low power mode(retention mode) by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	power_off_sftena Enable chip power off by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	alive_osc_sftena Enable clk_pmu/hclk_pmu/pclk_pmu switch to oscillator by software. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_sftena Enable VD_PMU input clamp by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_sftena Enable wake up reset by software. If asserted, all digital except IP with reset hold will be reset. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_sftena Disable oscillator by software. 1'b0: Enable 1'b1: Disable
0	RW	0x0	alive_32k_sftena Enable pclk_pmu and clk_pmu switch to 32KHz clock by software. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_SFTCON1

Address: Operational Base(0x27360000) + offset (0x1020C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	cci_clk_gate_sftena Enable PD_CCI clock gate by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	secure_clk_gate_sftena Enable PD_SECURE clock gate by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	bus_clk_gate_sftena Enable PD_BUS clock gate by software. 1'b0: Disable 1'b1: Enable

PMU_CRU_POWER_STS

Address: Operational Base(0x27360000) + offset (0x10210)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	cru_power_state Clock and reset power state. 4'h0: Normal state 4'h1: Clock low frequency state 4'h2: PLL power down state 4'h3: IO sleep state 4'h4: Input clamp state 4'h5: Oscillator disable state 4'h6: Sleep state 4'h7: Wake up state 4'h8: IO wake up state 4'h9: Oscillator enable state 4'ha: Input clamp release state 4'hb: Clock high frequency state 4'hc: Wake up reset clear state 4'he: PLL power up state Others: Reserved

PMU_PLLPD_CON

Address: Operational Base(0x27360000) + offset (0x10220)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	vpll_pd_ena Enable power down VPLL by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x0	aupll_pd_ena Enable power down AUPLL by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x0	ppll_pd_ena Enable power down PPLL by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cpll_pd_ena Enable power down CPLL by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	gpll_pd_ena Enable power down GPLL by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	spll_pd_ena Enable power down SPLL by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	lpll_pd_ena Enable power down LPLL by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	bpll_pd_ena Enable power down BPLL by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	d1bpll_pd_ena Enable power down D1BPLL by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	d1apll_pd_ena Enable power down D1APLL by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	d0bpll_pd_ena Enable power down D0BPLL by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	d0apll_pd_ena Enable power down D0APLL by hardware. 1'b0: Disable 1'b1: Enable

PMU_PLLPD_SFTCON

Address: Operational Base(0x27360000) + offset (0x10228)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	vpll_pd_sftena Enable power down VPLL by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	aupll_pd_sftena Enable power down AUPLL by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	ppll_pd_sftena Enable power down PPLL by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cpll_pd_sftena Enable power down CPLL by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	gpll_pd_sftena Enable power down GPLL by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	spll_pd_sftena Enable power down SPLL by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	lpll_pd_sftena Enable power down LPLL by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	bpll_pd_sftena Enable power down BPLL by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	d1bpll_pd_sftena Enable power down D1BPLL by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	d1apll_pd_sftena Enable power down D1APLL by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	d0bpll_pd_sftena Enable power down D0BPLL by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	d0apll_pd_sftena Enable power down D0APLL by software. 1'b0: Disable 1'b1: Enable

PMU_PMIC_STABLE_CNT

Address: Operational Base(0x27360000) + offset (0x10300)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pmic_stable_cnt PMIC stable count for mode 1 procedure. Number of clk_pmu used by counter logic.

PMU_OSC_STABLE_CNT

Address: Operational Base(0x27360000) + offset (0x10304)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	osc_stable_cnt Oscillator stable count for mode 1 procedure. Number of clk_pmu used by counter logic.

PMU_WAKEUP_RST_CLR_CNT

Address: Operational Base(0x27360000) + offset (0x10308)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	wakeup_rst_clr_cnt Wake up reset clear count for mode 1 procedure. Number of clk_pmu used by counter logic.

PMU_PLL_LOCK_CNT

Address: Operational Base(0x27360000) + offset (0x1030C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0xfffff	pll_lock_cnt Count for PLL from power up to lock. Number of clk_pmu used by counter logic.

PMU_WAKEUP_TIMEOUT_CNT

Address: Operational Base(0x27360000) + offset (0x10310)

Bit	Attr	Reset Value	Description
31:0	RW	0x00005dc0	wakeup_timeout_cnt Wake up timeout count. Number of clk_pmu used by counter logic.

PMU_WAKEUP_SRC_STABLE_CNT

Address: Operational Base(0x27360000) + offset (0x10318)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	wakeup_src_stable_cnt PMU wakeup source stable count. Number of clk_pmu used by counter logic.

PMU_SCU0_PWR_CON

Address: Operational Base(0x27360000) + offset (0x20000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	scu_vol_gate_ena SCU voltage gate enable. 1'b0: Disable 1'b1: Enable
9	RW	0x1	standbywfil2_bypass_ena L2 standbywfi bypass enable for SCU enter low power mode. 1'b0: Disable 1'b1: Enable. SCU not needs wait for L2 standbywfi state before execute low power procedure.
8	RW	0x0	standbywfi_bypass_ena CPU standbywfi bypass enable for SCU enter low power mode. 1'b0: Disable 1'b1: Enable. SCU not needs wait for CPU standbywfi state before execute low power procedure.
7:6	RO	0x0	reserved
5	RW	0x0	cluster_cpu_pwrdn_ena CPU hardware power down enable. 1'b0: Disable. 1'b1: Enable. CPU will power down before SCU power down.
4	RO	0x0	reserved
3	RW	0x0	scu_pwroff_ena SCU hardware power off enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_ena SCU hardware power down enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
1	RW	0x0	l2_idle_ena L2 idle enable. 1'b0: Disable 1'b1: Enable. Snoop interface is inactive automatically before SCU power down.
0	RW	0x0	l2_flush_ena L2 flush enable. 1'b0: Disable 1'b1: Enable. L2 will be flushed automatically before SCU power down.

PMU_SCU1_PWR_CON

Address: Operational Base(0x27360000) + offset (0x20004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	scu_vol_gate_ena SCU voltage gate enable. 1'b0: Disable 1'b1: Enable
9	RW	0x1	standbywfil2_bypass_ena L2 standbywfi bypass enable for SCU enter low power mode. 1'b0: Disable 1'b1: Enable. SCU not needs wait for L2 standbywfi state before execute low power procedure.
8	RW	0x0	standbywfi_bypass_ena CPU standbywfi bypass enable for SCU enter low power mode. 1'b0: Disable 1'b1: Enable. SCU not needs wait for CPU standbywfi state before execute low power procedure.
7:6	RO	0x0	reserved
5	RW	0x0	cluster_cpu_pwrdn_ena CPU hardware power down enable. 1'b0: Disable. 1'b1: Enable. CPU will power down before SCU power down.
4	RO	0x0	reserved
3	RW	0x0	scu_pwroff_ena SCU hardware power off enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_ena SCU hardware power down enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	l2_idle_ena L2 idle enable. 1'b0: Disable 1'b1: Enable. Snoop interface is inactive automatically before SCU power down.

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Bit	Attr	Reset Value	Description
0	RW	0x0	l2_flush_ena L2 flush enable. 1'b0: Disable 1'b1: Enable. L2 will be flushed automatically before SCU power down.

PMU_SCU0_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x20008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scu_pwroff_sftena SCU software power off enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_sftena SCU software power down enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	l2_idle_sftena L2 software idle enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	l2_flush_sftena L2 software flash enable. 1'b0: Disable 1'b1: Enable

PMU_SCU1_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x2000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scu_pwroff_sftena SCU software power off enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_sftena SCU software power down enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	l2_idle_sftena L2 software idle enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	l2_flush_sftena L2 software flash enable. 1'b0: Disable 1'b1: Enable

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PMU_SCU0_AUTO_CON

Address: Operational Base(0x27360000) + offset (0x20010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scu_sft_wakeup_cluster_ena SCU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_int_mask_ena SCU interrupt mask enable. 1'b0: Interrupt source is not masked. Interrupt Controller will generate interrupt if interrupt source is valid. 1'b1: Interrupt source is masked. Interrupt Controller will not generate interrupt if interrupt source is valid, until SCU exit low power state.
1	RW	0x0	scu_int_wakeup_cluster_ena SCU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	scu_lp_ena SCU low power enable. It is automatically cleared after SCU wakeup. 1'b0: Disable 1'b1: Enable

PMU_SCU1_AUTO_CON

Address: Operational Base(0x27360000) + offset (0x20014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scu_sft_wakeup_cluster_ena SCU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_int_mask_ena SCU interrupt mask enable. 1'b0: Interrupt source is not masked. Interrupt Controller will generate interrupt if interrupt source is valid. 1'b1: Interrupt source is masked. Interrupt Controller will not generate interrupt if interrupt source is valid, until SCU exit low power state.
1	RW	0x0	scu_int_wakeup_cluster_ena SCU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	scu_lp_ena SCU low power enable. It is automatically cleared after SCU wakeup. 1'b0: Disable 1'b1: Enable

PMU_SCU_POWER_STS

Address: Operational Base(0x27360000) + offset (0x20018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RO	0x0	scu1_power_state SCU1 power state. 4'h0: SCU normal state 4'h1: CPU power down state 4'h2: L2 flush state 4'h3: L2 idle state 4'h4: Cluster transfer idle state 4'h5: SCU power down state 4'h6: SCU sleep state 4'h7: SCU wakeup state 4'h8: SCU power up state 4'h9: Cluster transfer resume state 4'ha: CPU power up state Others: Reserved
3:0	RO	0x0	scu0_power_state SCU0 power state. 4'h0: SCU normal state 4'h1: CPU power down state 4'h2: L2 flush state 4'h3: L2 idle state 4'h4: Cluster transfer idle state 4'h5: SCU power down state 4'h6: SCU sleep state 4'h7: SCU wakeup state 4'h8: SCU power up state 4'h9: Cluster transfer resume state 4'ha: CPU power up state Others: Reserved

PMU_CLUSTER_PWR_ST

Address: Operational Base(0x27360000) + offset (0x20024)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	scu1_dwn_state SCU1 power down state. 1'b0: Inactive 1'b1: Active
24	RO	0x0	scu0_dwn_state SCU0 power down state. 1'b0: Inactive 1'b1: Active
23	RO	0x0	cpu7_dwn_state CPU7 power down state. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
22	RO	0x0	cpu6_dwn_state CPU6 power down state. 1'b0: Inactive 1'b1: Active
21	RO	0x0	cpu5_dwn_state CPU5 power down state. 1'b0: Inactive 1'b1: Active
20	RO	0x0	cpu4_dwn_state CPU4 power down state. 1'b0: Inactive 1'b1: Active
19	RO	0x0	cpu3_dwn_state CPU3 power down state. 1'b0: Inactive 1'b1: Active
18	RO	0x0	cpu2_dwn_state CPU2 power down state. 1'b0: Inactive 1'b1: Active
17	RO	0x0	cpu1_dwn_state CPU1 power down state. 1'b0: Inactive 1'b1: Active
16	RO	0x0	cpu0_dwn_state CPU0 power down state. 1'b0: Inactive 1'b1: Active
15:12	RO	0x0	reserved
11	RO	0x0	scu1_l2flushdone SCU1 L2 flush done state. 1'b0: Inactive 1'b1: Active
10	RO	0x0	scu0_l2flushdone SCU0 L2 flush done state. 1'b0: Inactive 1'b1: Active
9	RO	0x0	scu1_standbywfil2 SCU1 L2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
8	RO	0x0	scu0_standbywfil2 SCU0 L2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
7	RO	0x0	cpu7_standbywfi CPU7 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
6	RO	0x0	cpu6_standbywfi CPU6 STANDBYWFI state. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
5	RO	0x0	cpu5_standbywfi CPU5 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
4	RO	0x0	cpu4_standbywfi CPU4 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
3	RO	0x0	cpu3_standbywfi CPU3 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
2	RO	0x0	cpu2_standbywfi CPU2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
1	RO	0x0	cpu1_standbywfi CPU1 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
0	RO	0x0	cpu0_standbywfi CPU0 STANDBYWFI state. 1'b0: Inactive 1'b1: Active

PMU_CLUSTER0_IDLE_CON

Address: Operational Base(0x27360000) + offset (0x20028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	cluster_clk_gate_mask_ena If enable, BIU_LITCORE corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cluster_biu_idle_req_ena Enable sending idle request to BIU_LITCORE by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	adb_idle_req_ena Enable sending idle request to ADB. 1'b0: Disable 1'b1: Enable

PMU_CLUSTER1_IDLE_CON

Address: Operational Base(0x27360000) + offset (0x2002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	cluster_clk_gate_mask_ena If enable, BIU_BIGCORE corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cluster_biu_idle_req_ena Enable sending idle request to BIU_BIGCORE by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	adb_idle_req_ena Enable sending idle request to ADB. 1'b0: Disable 1'b1: Enable

PMU_CLUSTER0_IDLE_SFTCON

Address: Operational Base(0x27360000) + offset (0x20030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	cluster_clk_gate_mask_sftena If enable, BIU_LITCORE corresponding clock can be opened or gated by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cluster_biu_idle_req_sftena Enable sending bus idle request to BIU_LITCORE by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	adb_idle_req_sftena Enable sending idle request to ADB by software. 1'b0: Disable 1'b1: Enable

PMU_CLUSTER1_IDLE_SFTCON

Address: Operational Base(0x27360000) + offset (0x20034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	cluster_clk_gate_mask_sftena If enable, BIU_BIGCORE corresponding clock can be opened or gated by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cluster_biu_idle_req_sftena Enable sending bus idle request to BIU_BIGCORE by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	adb_idle_req_sftena Enable sending idle request to ADB by software. 1'b0: Disable 1'b1: Enable

PMU_CLUSTER_IDLE_ACK

Address: Operational Base(0x27360000) + offset (0x20038)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	cluster1_adb_pwrqdeny ADB1 low power deny state. 1'b0: Inactive 1'b1: Active
4	RO	0x0	cluster1_adb_pwrqaccept ADB1 low power accept state. 1'b0: Inactive 1'b1: Active
3	RO	0x0	cluster0_adb_pwrqdeny ADB0 low power deny state. 1'b0: Inactive 1'b1: Active
2	RO	0x0	cluster0_adb_pwrqaccept ADB0 low power accept state. 1'b0: Inactive 1'b1: Active
1	RO	0x0	cluster1_biu_idle_ack BIU_BIGCORE biu idle acknowledge state. 1'b0: Inactive 1'b1: Active
0	RO	0x0	cluster0_biu_idle_ack BIU_LITCORE idle acknowledge state. 1'b0: Inactive 1'b1: Active

PMU_CLUSTER_IDLE_ST

Address: Operational Base(0x27360000) + offset (0x2003C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	cluster1_adb_pwrqactive ADB1 low power active state. 1'b0: Inactive 1'b1: Active
2	RO	0x0	cluster0_adb_pwrqactive ADB0 low power active state. 1'b0: Inactive 1'b1: Active
1	RO	0x0	cluster1_biu_idle BIU_BIGCORE idle state. 1'b0: Inactive 1'b1: Active
0	RO	0x0	cluster0_biu_idle BIU_LITCORE idle state. 1'b0: Inactive 1'b1: Active

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PMU_CORE0_STABLE_CNT

Address: Operational Base(0x27360000) + offset (0x20048)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	core_stable_cnt VD_LITCORE power stable count. Number of clk_pmu used by counter logic.

PMU_CORE1_STABLE_CNT

Address: Operational Base(0x27360000) + offset (0x20054)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	core_stable_cnt VD_BIGCORE power stable count. Number of clk_pmu used by counter logic.

PMU_CPU0_AUTO_PWR_CON

Address: Operational Base(0x27360000) + offset (0x20080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_sft_wakeup_ena CPU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu_int_mask_ena CPU interrupt mask enable. 1'b0: Interrupt is not masked, CPU will execute interrupt routine if interrupt is valid. 1'b1: Interrupt is masked, CPU will not execute interrupt routine if interrupt is valid, until CPU exit low power state.
1	RW	0x0	cpu_int_wakeup_ena CPU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu_auto_pwrdn_ena CPU auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU1_AUTO_PWR_CON

Address: Operational Base(0x27360000) + offset (0x20084)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_sft_wakeup_ena CPU software wakeup enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	cpu_int_mask_ena CPU interrupt mask enable. 1'b0: Interrupt is not masked, CPU will execute interrupt routine if interrupt is valid. 1'b1: Interrupt is masked, CPU will not execute interrupt routine if interrupt is valid, until CPU exit low power state.
1	RW	0x0	cpu_int_wakeup_ena CPU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu_auto_pwrdn_ena CPU auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU2_AUTO_PWR_CON

Address: Operational Base(0x27360000) + offset (0x20088)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_sft_wakeup_ena CPU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu_int_mask_ena CPU interrupt mask enable. 1'b0: Interrupt is not masked, CPU will execute interrupt routine if interrupt is valid. 1'b1: Interrupt is masked, CPU will not execute interrupt routine if interrupt is valid, until CPU exit low power state.
1	RW	0x0	cpu_int_wakeup_ena CPU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu_auto_pwrdn_ena CPU auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU3_AUTO_PWR_CON

Address: Operational Base(0x27360000) + offset (0x2008C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_sft_wakeup_ena CPU software wakeup enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	cpu_int_mask_ena CPU interrupt mask enable. 1'b0: Interrupt is not masked, CPU will execute interrupt routine if interrupt is valid. 1'b1: Interrupt is masked, CPU will not execute interrupt routine if interrupt is valid, until CPU exit low power state.
1	RW	0x0	cpu_int_wakeup_ena CPU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu_auto_pwrdn_ena CPU auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU4_AUTO_PWR_CON

Address: Operational Base(0x27360000) + offset (0x20090)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_sft_wakeup_ena CPU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu_int_mask_ena CPU interrupt mask enable. 1'b0: Interrupt is not masked, CPU will execute interrupt routine if interrupt is valid. 1'b1: Interrupt is masked, CPU will not execute interrupt routine if interrupt is valid, until CPU exit low power state.
1	RW	0x0	cpu_int_wakeup_ena CPU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu_auto_pwrdn_ena CPU auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU5_AUTO_PWR_CON

Address: Operational Base(0x27360000) + offset (0x20094)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_sft_wakeup_ena CPU software wakeup enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	cpu_int_mask_ena CPU interrupt mask enable. 1'b0: Interrupt is not masked, CPU will execute interrupt routine if interrupt is valid. 1'b1: Interrupt is masked, CPU will not execute interrupt routine if interrupt is valid, until CPU exit low power state.
1	RW	0x0	cpu_int_wakeup_ena CPU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu_auto_pwrdn_ena CPU auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU6_AUTO_PWR_CON

Address: Operational Base(0x27360000) + offset (0x20098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_sft_wakeup_ena CPU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu_int_mask_ena CPU interrupt mask enable. 1'b0: Interrupt is not masked, CPU will execute interrupt routine if interrupt is valid. 1'b1: Interrupt is masked, CPU will not execute interrupt routine if interrupt is valid, until CPU exit low power state.
1	RW	0x0	cpu_int_wakeup_ena CPU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu_auto_pwrdn_ena CPU auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU7_AUTO_PWR_CON

Address: Operational Base(0x27360000) + offset (0x2009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_sft_wakeup_ena CPU software wakeup enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	cpu_int_mask_ena CPU interrupt mask enable. 1'b0: Interrupt is not masked, CPU will execute interrupt routine if interrupt is valid. 1'b1: Interrupt is masked, CPU will not execute interrupt routine if interrupt is valid, until CPU exit low power state.
1	RW	0x0	cpu_int_wakeup_ena CPU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu_auto_pwrdn_ena CPU auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU0_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu_pwrdn_sftena CPU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU1_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu_pwrdn_sftena CPU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU2_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu_pwrdn_sftena CPU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU3_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu_pwrdn_sftena CPU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU4_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu_pwrdn_sftena CPU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU5_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200B4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu_pwrdn_sftena CPU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU6_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu_pwrdn_sftena CPU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU7_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu_pwrdn_sftena CPU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CCI_PWR_CON

Address: Operational Base(0x27360000) + offset (0x200E0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:1	RW	0x4	cci_pstate_cfg CCI power state configured by software. 3'b100: ON 3'b000: OFF Others: Reserved
0	RW	0x0	cci_pidle_ena CCI low power enable by hardware. 1'b0: Disable 1'b1: Enable

PMU_CCI_PWR_SFTCON

Address: Operational Base(0x27360000) + offset (0x200E4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	cci_pidle_sftena CCI low power enable by software. 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

PMU_CCI_PWR_ST

Address: Operational Base(0x27360000) + offset (0x200E8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:2	RO	0x00	cci_pactive CCI low power pactive state.
1	RO	0x0	cci_pdeny CCI low power deny state. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
0	RO	0x0	cci_paccept CCI low power accept state. 1'b0: Inactive 1'b1: Active

PMU_CCI_POWER_STS

Address: Operational Base(0x27360000) + offset (0x200EC)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	cci_power_state CCI power state. 3'h0: CCI normal state 3'h1: CCI low power state 3'h3: CCI sleep state 3'h5: CCI power active state Others: Reserved

PMU_BIU_IDLE_CON0

Address: Operational Base(0x27360000) + offset (0x20100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	idle_req_php_ena Enable sending idle request to BIU_PHP by hardware. 1'b0: Disable 1'b1: Enable
14	RW	0x0	idle_req_vop_ddrsch_ena Enable sending idle request to BIU_VOP_DDRSCH by hardware. 1'b0: Disable 1'b1: Enable
13	RW	0x0	idle_req_vop_ena Enable sending idle request to BIU_VOP by hardware. 1'b0: Disable 1'b1: Enable
12	RW	0x0	idle_req_vo1_ena Enable sending idle request to BIU_VO1 by hardware. 1'b0: Disable 1'b1: Enable
11	RW	0x0	idle_req_vo0_ena Enable sending idle request to BIU_VO0 by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_usb_ena Enable sending idle request to BIU_USB by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_vi_ena Enable sending idle request to BIU_VI by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	idle_req_vepu1_ena Enable sending idle request to BIU_VEPU1 by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_vepu0_ena Enable sending idle request to BIU_VEPU0 by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_vdec_ena Enable sending idle request to BIU_VDEC by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	idle_req_vpu_ena Enable sending idle request to BIU_VPU by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_npusys_ena Enable sending idle request to BIU_NPUSYS by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_nputop_ena Enable sending idle request to BIU_NPUTOP by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_npu1_ena Enable sending idle request to BIU_NPU1 by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_npu0_ena Enable sending idle request to BIU_NPU0 by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_gpu_ena Enable sending idle request to BIU_GPU by hardware. 1'b0: Disable 1'b1: Enable

PMU_BIU_IDLE_CON1

Address: Operational Base(0x27360000) + offset (0x20104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	idle_req_cci_ddrsch_ena Enable sending idle request to BIU_CCI_DDRSCH by hardware. 1'b0: Disable 1'b1: Enable
12	RW	0x0	idle_req_cci_ena Enable sending idle request to BIU_CCI by hardware. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
11	RW	0x0	idle_req_vo0vop_channel_ena Enable sending idle request to BIU_VO0VOP_CHANNEL by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_top_ena Enable sending idle request to BIU_TOP by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_secure_ena Enable sending idle request to BIU_SECURE by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x0	idle_req_bus_ena Enable sending idle request to BIU_BUS by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_ddrsch1_ena Enable sending idle request to BIU_DDRSCH1 by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_ddrsch0_ena Enable sending idle request to BIU_DDRSCH0 by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	idle_req_ddr_ena Enable sending idle request to BIU_DDR by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_center_main_ena Enable sending idle request to BIU_CENTER_MAIN by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_center_ddrsch_ena Enable sending idle request to BIU_CENTER_DDRSCH by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_nvm_ena Enable sending idle request to BIU_NVM by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_gmac_ena Enable sending idle request to BIU_GMAC by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_audio_ena Enable sending idle request to BIU_AUDIO by hardware. 1'b0: Disable 1'b1: Enable

PMU_BIU_IDLE_SFTCON0

Address: Operational Base(0x27360000) + offset (0x20110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	idle_req_php_sftena Enable sending idle request to BIU_PHP by software. 1'b0: Disable 1'b1: Enable
14	RW	0x0	idle_req_vop_ddrsch_sftena Enable sending idle request to BIU_VOP_DDRSCH by software. 1'b0: Disable 1'b1: Enable
13	RW	0x0	idle_req_vop_sftena Enable sending idle request to BIU_VOP by software. 1'b0: Disable 1'b1: Enable
12	RW	0x0	idle_req_vo1_sftena Enable sending idle request to BIU_VO1 by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	idle_req_vo0_sftena Enable sending idle request to BIU_VO0 by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_usb_sftena Enable sending idle request to BIU_USB by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_vi_sftena Enable sending idle request to BIU_VI by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	idle_req_vepu1_sftena Enable sending idle request to BIU_VEPU1 by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_vepu0_sftena Enable sending idle request to BIU_VEPU0 by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_vdec_sftena Enable sending idle request to BIU_VDEC by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	idle_req_vpu_sftena Enable sending idle request to BIU_VPU by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_npusys_sftena Enable sending idle request to BIU_NPUSYS by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_nputop_sftena Enable sending idle request to BIU_NPUTOP by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	idle_req_npu1_sftena Enable sending idle request to BIU_NPU1 by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_npu0_sftena Enable sending idle request to BIU_NPU0 by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_gpu_sftena Enable sending idle request to BIU_GPU by software. 1'b0: Disable 1'b1: Enable

PMU_BIU_IDLE_SFTCON1

Address: Operational Base(0x27360000) + offset (0x20114)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	idle_req_cci_ddrsch_sftena Enable sending idle request to BIU_CCI_DDRSCH by software. 1'b0: Disable 1'b1: Enable
12	RW	0x0	idle_req_cci_sftena Enable sending idle request to BIU_CCI by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	idle_req_vo0vop_channel_sftena Enable sending idle request to BIU_VO0VOP_CHANNEL by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_top_sftena Enable sending idle request to BIU_TOP by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_secure_sftena Enable sending idle request to BIU_SECURE by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	idle_req_bus_sftena Enable sending idle request to BIU_BUS by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_ddrsch1_sftena Enable sending idle request to BIU_DDRSCH1 by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_ddrsch0_sftena Enable sending idle request to BIU_DDRSCH0 by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	idle_req_ddr_sftena Enable sending idle request to BIU_DDR by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_center_main_sftena Enable sending idle request to BIU_CENTER_MAIN by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_center_ddrsch_sftena Enable sending idle request to BIU_CENTER_DDRSCH by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_nvm_sftena Enable sending idle request to BIU_NVM by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_gmac_sftena Enable sending idle request to BIU_GMAC by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_audio_sftena Enable sending idle request to BIU_AUDIO by software. 1'b0: Disable 1'b1: Enable

PMU_BIU_IDLE_ACK_STS

Address: Operational Base(0x27360000) + offset (0x20120)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	idle_ack_cci_ddrsch BIU_CCI_DDRSCH idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
28	RO	0x0	idle_ack_cci BIU_CCI idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
27	RO	0x0	idle_ack_vo0vop_channel BIU_VO0VOP_CHANNEL idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
26	RO	0x0	idle_ack_top BIU_TOP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
25	RO	0x0	idle_ack_secure BIU_SECURE idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
24	RO	0x0	idle_ack_bus BIU_BUS idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

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Bit	Attr	Reset Value	Description
23	RO	0x0	idle_ack_ddrsch1 BIU_DDRSCH1 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
22	RO	0x0	idle_ack_ddrsch0 BIU_DDRSCH0 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
21	RO	0x0	idle_ack_ddr BIU_DDR idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
20	RO	0x0	idle_ack_center_main BIU_CENTER_MAIN idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
19	RO	0x0	idle_ack_center_ddrsch BIU_CENTER_DDRSCH idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
18	RO	0x0	idle_ack_nvm BIU_NVM idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
17	RO	0x0	idle_ack_gmac BIU_GMAC idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
16	RO	0x0	idle_ack_audio BIU_AUDIO idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
15	RO	0x0	idle_ack_php BIU_PHP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
14	RO	0x0	idle_ack_vop_ddrsch BIU_VOP_DDRSCH idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
13	RO	0x0	idle_ack_vop BIU_VOP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
12	RO	0x0	idle_ack_vo1 BIU_VO1 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
11	RO	0x0	idle_ack_vo0 BIU_VO0 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
10	RO	0x0	idle_ack_usb BIU_USB idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

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Bit	Attr	Reset Value	Description
9	RO	0x0	idle_ack_vi BIU_VI idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
8	RO	0x0	idle_ack_vepu1 BIU_VEPU1 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
7	RO	0x0	idle_ack_vepu0 BIU_VEPU0 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
6	RO	0x0	idle_ack_vdec BIU_VDEC idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
5	RO	0x0	idle_ack_vpu BIU_VPU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
4	RO	0x0	idle_ack_npusys BIU_NPUSYS idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
3	RO	0x0	idle_ack_nputop BIU_NPUTOP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
2	RO	0x0	idle_ack_npu1 BIU_NPU1 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
1	RO	0x0	idle_ack_npu0 BIU_NPU0 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
0	RO	0x0	idle_ack_gpu BIU_GPU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

PMU_BIU_IDLE_STS

Address: Operational Base(0x27360000) + offset (0x20128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	idle_cci_ddrsch BIU_CCI_DDRSCH idle state. 1'b0: Not idle 1'b1: Idle
28	RO	0x0	idle_cci BIU_CCI idle state. 1'b0: Not idle 1'b1: Idle

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Bit	Attr	Reset Value	Description
27	RO	0x0	idle_vo0vop_channel BIU_VO0VOP_CHANNEL idle state. 1'b0: Not idle 1'b1: Idle
26	RO	0x0	idle_top BIU_TOP idle state. 1'b0: Not idle 1'b1: Idle
25	RO	0x0	idle_secure BIU_SECURE idle state. 1'b0: Not idle 1'b1: Idle
24	RO	0x0	idle_bus BIU_BUS idle state. 1'b0: Not idle 1'b1: Idle
23	RO	0x0	idle_ddrsch1 BIU_DDRSCH1 idle state. 1'b0: Not idle 1'b1: Idle
22	RO	0x0	idle_ddrsch0 BIU_DDRSCH0 idle state. 1'b0: Not idle 1'b1: Idle
21	RO	0x0	idle_ddr BIU_DDR idle state. 1'b0: Not idle 1'b1: Idle
20	RO	0x0	idle_center_main BIU_CENTER_MAIN idle state. 1'b0: Not idle 1'b1: Idle
19	RO	0x0	idle_center_ddrsch BIU_CENTER_DDRSCH idle state. 1'b0: Not idle 1'b1: Idle
18	RO	0x0	idle_nvm BIU_NVM idle state. 1'b0: Not idle 1'b1: Idle
17	RO	0x0	idle_gmac BIU_GMAC idle state. 1'b0: Not idle 1'b1: Idle
16	RO	0x0	idle_audio BIU_AUDIO idle state. 1'b0: Not idle 1'b1: Idle
15	RO	0x0	idle_php BIU_PHP idle state. 1'b0: Not idle 1'b1: Idle
14	RO	0x0	idle_vop_ddrsch BIU_VOP_DDRSCH idle state. 1'b0: Not idle 1'b1: Idle

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Bit	Attr	Reset Value	Description
13	RO	0x0	idle_vop BIU_VOP idle state. 1'b0: Not idle 1'b1: Idle
12	RO	0x0	idle_vo1 BIU_VO1 idle state. 1'b0: Not idle 1'b1: Idle
11	RO	0x0	idle_vo0 BIU_VO0 idle state. 1'b0: Not idle 1'b1: Idle
10	RO	0x0	idle_usb BIU_USB idle state. 1'b0: Not idle 1'b1: Idle
9	RO	0x0	idle_vi BIU_VI idle state. 1'b0: Not idle 1'b1: Idle
8	RO	0x0	idle_vepu1 BIU_VEPU1 idle state. 1'b0: Not idle 1'b1: Idle
7	RO	0x0	idle_vepu0 BIU_VEPU0 idle state. 1'b0: Not idle 1'b1: Idle
6	RO	0x0	idle_vdec BIU_VDEC idle state. 1'b0: Not idle 1'b1: Idle
5	RO	0x0	idle_vpu BIU_VPU idle state. 1'b0: Not idle 1'b1: Idle
4	RO	0x0	idle_npusys BIU_NPUSYS idle state. 1'b0: Not idle 1'b1: Idle
3	RO	0x0	idle_nputop BIU_NPUTOP idle state. 1'b0: Not idle 1'b1: Idle
2	RO	0x0	idle_npu1 BIU_NPU1 idle state. 1'b0: Not idle 1'b1: Idle
1	RO	0x0	idle_npu0 BIU_NPU0 idle state. 1'b0: Not idle 1'b1: Idle
0	RO	0x0	idle_gpu BIU_GPU idle state. 1'b0: Not idle 1'b1: Idle

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PMU_BIU_GATMASK_CON0

Address: Operational Base(0x27360000) + offset (0x20130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gate_mask_php_ena If enable, BIU_PHP corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
14	RW	0x0	gate_mask_vop_ddrsch_ena If enable, BIU_VOP_DDRSCH corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
13	RW	0x0	gate_mask_vop_ena If enable, BIU_VOP corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
12	RW	0x0	gate_mask_vo1_ena If enable, BIU_VO1 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
11	RW	0x0	gate_mask_vo0_ena If enable, BIU_VO0 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
10	RW	0x0	gate_mask_usb_ena If enable, BIU_USB corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
9	RW	0x0	gate_mask_vi_ena If enable, BIU_VI corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
8	RW	0x0	gate_mask_vepu1_ena If enable, BIU_VEPU1 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
7	RW	0x0	gate_mask_vepu0_ena If enable, BIU_VEPU0 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x0	gate_mask_vdec_ena If enable, BIU_VDEC corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
5	RW	0x0	gate_mask_vpu_ena If enable, BIU_VPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
4	RW	0x0	gate_mask_npusys_ena If enable, BIU_NPUSYS corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
3	RW	0x0	gate_mask_nputop_ena If enable, BIU_NPUTOP corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
2	RW	0x0	gate_mask_npu1_ena If enable, BIU_NPU1 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	gate_mask_npu0_ena If enable, BIU_NPU0 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
0	RW	0x0	gate_mask_gpu_ena If enable, BIU_GPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

PMU_BIU_GATMASK_CON1

Address: Operational Base(0x27360000) + offset (0x20134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	gate_mask_cci_ddrsch_ena If enable, BIU_CCI_DDRSCH corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
12	RW	0x0	gate_mask_cci_ena If enable, BIU_CCI corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11	RW	0x0	gate_mask_vo0vop_channel_ena If enable, BIU_VO0VOP_CHANNEL corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
10	RW	0x0	gate_mask_top_ena If enable, BIU_TOP corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
9	RW	0x0	gate_mask_secure_ena If enable, BIU_SECURE corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
8	RW	0x0	gate_mask_bus_ena If enable, BIU_BUS corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
7	RW	0x0	gate_mask_ddrsch1_ena If enable, BIU_DDRSCH1 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
6	RW	0x0	gate_mask_ddrsch0_ena If enable, BIU_DDRSCH0 corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
5	RW	0x0	gate_mask_ddr_ena If enable, BIU_DDR corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
4	RW	0x0	gate_mask_center_main_ena If enable, BIU_CENTER_MAIN corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
3	RW	0x0	gate_mask_center_ddrsch_ena If enable, BIU_CENTER_DDRSCH corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
2	RW	0x0	gate_mask_nvm_ena If enable, BIU_NVM corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	gate_mask_gmac_ena If enable, BIU_GMAC corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	gate_mask_audio_ena If enable, BIU_AUDIO corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

PMU_BIU_GATMASK_SFTCON0

Address: Operational Base(0x27360000) + offset (0x20140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gate_mask_php_sftena If enable, BIU_PHP corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
14	RW	0x0	gate_mask_vop_ddrsch_sftena If enable, BIU_VOP_DDRSCH corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
13	RW	0x0	gate_mask_vop_sftena If enable, BIU_VOP corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
12	RW	0x0	gate_mask_vo1_sftena If enable, BIU_VO1 corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
11	RW	0x0	gate_mask_vo0_sftena If enable, BIU_VO0 corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
10	RW	0x0	gate_mask_usb_sftena If enable, BIU_USB corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
9	RW	0x0	gate_mask_vi_sftena If enable, BIU_VI corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
8	RW	0x0	gate_mask_vepu1_sftena If enable, BIU_VEPU1 corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
7	RW	0x0	gate_mask_vepu0_sftena If enable, BIU_VEPU0 corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
6	RW	0x0	gate_mask_vdec_sftena If enable, BIU_VDEC corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
5	RW	0x0	gate_mask_vpu_sftena If enable, BIU_VPU corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
4	RW	0x0	gate_mask_npusys_sftena If enable, BIU_NPUSYS corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
3	RW	0x0	gate_mask_nputop_sftena If enable, BIU_NPUTOP corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
2	RW	0x0	gate_mask_npu1_sftena If enable, BIU_NPU1 corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	gate_mask_npu0_sftena If enable, BIU_NPU0 corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
0	RW	0x0	gate_mask_gpu_sftena If enable, BIU_GPU corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable

PMU_BIU_GATMASK_SFTCON1

Address: Operational Base(0x27360000) + offset (0x20144)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	gate_mask_cci_ddrsch_sftena If enable, BIU_CCI_DDRSCH corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
12	RW	0x0	gate_mask_cci_sftena If enable, BIU_CCI corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
11	RW	0x0	gate_mask_vo0vop_channel_sftena If enable, BIU_VO0VOP_CHANNEL corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
10	RW	0x0	gate_mask_top_sftena If enable, BIU_TOP corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
9	RW	0x0	gate_mask_secure_sftena If enable, BIU_SECURE corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
8	RW	0x0	gate_mask_bus_sftena If enable, BIU_BUS corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
7	RW	0x0	gate_mask_ddrsch1_sftena If enable, BIU_DDRSCH1 corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
6	RW	0x0	gate_mask_ddrsch0_sftena If enable, BIU_DDRSCH0 corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
5	RW	0x0	gate_mask_ddr_sftena If enable, BIU_DDR corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
4	RW	0x0	gate_mask_center_main_sftena If enable, BIU_CENTER_MAIN corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
3	RW	0x0	gate_mask_center_ddrsch_sftena If enable, BIU_CENTER_DDRSCH corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
2	RW	0x0	gate_mask_nvm_sftena If enable, BIU_NVM corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	gate_mask_gmac_sftena If enable, BIU_GMAC corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable
0	RW	0x0	gate_mask_audio_sftena If enable, BIU_AUDIO corresponding clock can be opened or gated by software when idle operation. 1'b0: Disable 1'b1: Enable

PMU_BIU_IDLEACK_BYPASS_CON

Address: Operational Base(0x27360000) + offset (0x20150)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	ddrsch1_idleack_bypass_ena Bypass BIU_DDRSCH1 idle acknowledge signal. 1'b0: Not bypass, BIU_DDRSCH1 idle acknowledge signal is used to check acknowledge state. 1'b1: Bypass, BIU_DDRSCH1 idle acknowledge signal is ignored, and BIU_DDRSCH1 idle request signal is used as acknowledge signal.
0	RW	0x0	ddrsch0_idleack_bypass_ena Bypass BIU_DDRSCH0 idle acknowledge signal. 1'b0: Not bypass, BIU_DDRSCH0 idle acknowledge signal is used to check acknowledge state. 1'b1: Bypass, BIU_DDRSCH0 idle acknowledge signal is ignored, and BIU_DDRSCH0 idle request signal is used as acknowledge signal.

PMU_PWR_GATE_CON0

Address: Operational Base(0x27360000) + offset (0x20200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_dwn_ena Enable power down PD_VO0 by hardware. 1'b0: Disable 1'b1: Enable
14	RW	0x0	pd_vo1_dwn_ena Enable power down PD_VO1 by hardware. 1'b0: Disable 1'b1: Enable
13	RW	0x0	pd_vop_cluster_dwn_ena Enable power down PD_VOP_CLUSTER by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
12	RW	0x0	pd_vop_esmart_dwn_ena Enable power down PD_VOP_ESMART by hardware. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pd_vop_dwn_ena Enable power down PD_VOP by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x0	pd_subphp_dwn_ena Enable power down PD_SUBPHP by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pd_php_dwn_ena Enable power down PD_PHP by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_audio_dwn_ena Enable power down PD_AUDIO by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_sdgmac_dwn_ena Enable power down PD_SDGMAC by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nvm_dwn_ena Enable power down PD_NVM by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_cci_dwn_ena Enable power down PD_CCI by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_ddr_dwn_ena Enable power down VD_DDR by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_center_dwn_ena Enable power down PD_CENTER by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_secure_dwn_ena Enable power down PD_SECURE by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_bus_dwn_ena Enable power down PD_BUS by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_npu_dwn_ena Enable power down VD_NPU by hardware. 1'b0: Disable 1'b1: Enable

PMU_PWR_GATE_CON1

Address: Operational Base(0x27360000) + offset (0x20204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pd_gpu_dwn_ena Enable power down VD_GPU by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_npu1_dwn_ena Enable power down PD_NPU1 by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_npu0_dwn_ena Enable power down PD_NPU0 by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nputop_dwn_ena Enable power down PD_NPUTOP by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_vpu_dwn_ena Enable power down PD_VPU by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_vdec_dwn_ena Enable power down PD_VDEC by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_vepu1_dwn_ena Enable power down PD_VEPU1 by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vepu0_dwn_ena Enable power down PD_VEPU0 by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vi_dwn_ena Enable power down PD_VI by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_usb_dwn_ena Enable power down PD_USB by hardware. 1'b0: Disable 1'b1: Enable

PMU_PWR_GATE_SFTCON0

Address: Operational Base(0x27360000) + offset (0x20210)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	pd_vo0_dwn_sftena Enable power down PD_VO0 by software. 1'b0: Disable 1'b1: Enable
14	RW	0x0	pd_vo1_dwn_sftena Enable power down PD_VO1 by software. 1'b0: Disable 1'b1: Enable
13	RW	0x0	pd_vop_cluster_dwn_sftena Enable power down PD_VOP_CLUSTER by software. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pd_vop_esmart_dwn_sftena Enable power down PD_VOP_ESMART by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pd_vop_dwn_sftena Enable power down PD_VOP by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	pd_subphp_dwn_sftena Enable power down PD_SUBPHP by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pd_php_dwn_sftena Enable power down PD_PHP by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_audio_dwn_sftena Enable power down PD_AUDIO by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_sdgmac_dwn_sftena Enable power down PD_SDGMAC by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nvm_dwn_sftena Enable power down PD_NVM by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_cci_dwn_sftena Enable power down PD_CCI by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_ddr_dwn_sftena Enable power down VD_DDR by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_center_dwn_sftena Enable power down PD_CENTER by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_secure_dwn_sftena Enable power down PD_SECURE by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	pd_bus_dwn_sftena Enable power down PD_BUS by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_npu_dwn_sftena Enable power down VD_NPU by software. 1'b0: Disable 1'b1: Enable

PMU_PWR_GATE_SFTCON1

Address: Operational Base(0x27360000) + offset (0x20214)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x1	pd_gpu_dwn_sftena Enable power down VD_GPU by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_npu1_dwn_sftena Enable power down PD_NPU1 by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_npu0_dwn_sftena Enable power down PD_NPU0 by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nputop_dwn_sftena Enable power down PD_NPUTOP by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_vpu_dwn_sftena Enable power down PD_VPU by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_vdec_dwn_sftena Enable power down PD_VDEC by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_vepu1_dwn_sftena Enable power down PD_VEPU1 by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vepu0_dwn_sftena Enable power down PD_VEPU0 by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vi_dwn_sftena Enable power down PD_VI by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	pd_usb_dwn_sftena Enable power down PD_USB by software. 1'b0: Disable 1'b1: Enable

PMU_VOL_GATE_CON0

Address: Operational Base(0x27360000) + offset (0x20220)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Enable power down VD_NPU by hardware. 1'b0: Disable 1'b1: Enable
15:6	RO	0x000	reserved
5	RW	0x0	vd_cci_dwn_ena Enable power off VD_LITCORE by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	vd_ddr_dwn_ena Enable power off VD_DDR by hardware. 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	vd_npu_dwn_ena Enable power off VD_NPU by hardware. 1'b0: Disable 1'b1: Enable

PMU_VOL_GATE_CON1

Address: Operational Base(0x27360000) + offset (0x20224)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	vd_gpu_dwn_ena Enable power off VD_GPU by hardware. 1'b0: Disable 1'b1: Enable
8:0	RO	0x000	reserved

PMU_PWR_GATE_STS

Address: Operational Base(0x27360000) + offset (0x20230)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x1	pd_gpu_dwn_stat The power state of VD_GPU. 1'b0: Power up 1'b1: Power down
24	RO	0x0	pd_npu1_dwn_stat The power state of PD_NPU1. 1'b0: Power up 1'b1: Power down

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Bit	Attr	Reset Value	Description
23	RO	0x0	pd_npu0_dwn_stat The power state of PD_NPU0. 1'b0: Power up 1'b1: Power down
22	RO	0x0	pd_nputop_dwn_stat The power state of PD_NPUTOP. 1'b0: Power up 1'b1: Power down
21	RO	0x0	pd_vpu_dwn_stat The power state of PD_VPU. 1'b0: Power up 1'b1: Power down
20	RO	0x0	pd_vdec_dwn_stat The power state of PD_VDEC. 1'b0: Power up 1'b1: Power down
19	RO	0x0	pd_vepu1_dwn_stat The power state of PD_VEPU1. 1'b0: Power up 1'b1: Power down
18	RO	0x0	pd_vepu0_dwn_stat The power state of PD_VEPU0. 1'b0: Power up 1'b1: Power down
17	RO	0x0	pd_vi_dwn_stat The power state of PD_VI. 1'b0: Power up 1'b1: Power down
16	RO	0x0	pd_usb_dwn_stat The power state of PD_USB. 1'b0: Power up 1'b1: Power down
15	RO	0x0	pd_vo0_dwn_stat The power state of PD_VO0. 1'b0: Power up 1'b1: Power down
14	RO	0x0	pd_vo1_dwn_stat The power state of PD_VO1. 1'b0: Power up 1'b1: Power down
13	RO	0x0	pd_vop_cluster_dwn_stat The power state of PD_VOP_CLUSTER. 1'b0: Power up 1'b1: Power down
12	RO	0x0	pd_vop_esmart_dwn_stat The power state of PD_VOP_ESMART. 1'b0: Power up 1'b1: Power down
11	RO	0x0	pd_vop_dwn_stat The power state of PD_VOP. 1'b0: Power up 1'b1: Power down
10	RO	0x0	pd_subphp_dwn_stat The power state of PD_SUBPHP. 1'b0: Power up 1'b1: Power down

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Bit	Attr	Reset Value	Description
9	RO	0x0	pd_php_dwn_stat The power state of PD_PHP. 1'b0: Power up 1'b1: Power down
8	RO	0x0	pd_audio_dwn_stat The power state of PD_AUDIO. 1'b0: Power up 1'b1: Power down
7	RO	0x0	pd_sdgmac_dwn_stat The power state of PD_SDGMAC. 1'b0: Power up 1'b1: Power down
6	RO	0x0	pd_nvm_dwn_stat The power state of PD_NVM. 1'b0: Power up 1'b1: Power down
5	RO	0x0	pd_cci_dwn_stat The power state of PD_CCI. 1'b0: Power up 1'b1: Power down
4	RO	0x0	pd_ddr_dwn_stat The power state of VD_DDR. 1'b0: Power up 1'b1: Power down
3	RO	0x0	pd_center_dwn_stat The power state of PD_CENTER. 1'b0: Power up 1'b1: Power down
2	RO	0x0	pd_secure_dwn_stat The power state of PD_SECURE. 1'b0: Power up 1'b1: Power down
1	RO	0x0	pd_bus_dwn_stat The power state of PD_BUS. 1'b0: Power up 1'b1: Power down
0	RO	0x0	pd_npu_dwn_stat The power state of VD_NPU. 1'b0: Power up 1'b1: Power down

PMU_PWR_GATE_POWER_STS

Address: Operational Base(0x27360000) + offset (0x20238)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	power_gate_state Power gating state. 3'h0: Normal state 3'h1: Power down start state 3'h2: Power down running state 3'h3: Wait for power up state 3'h4: Power up start state 3'h5: Power up running state Others: Reserved

PMU_PWR_CHAIN0_STS0

Address: Operational Base(0x27360000) + offset (0x20240)

Bit	Attr	Reset Value	Description
31	RO	0x1	pd_cpu4_c0_pwr_stat The power state of PD_CPU4 power chain 0. 1'b0: Power down 1'b1: Power up
30	RO	0x0	reserved
29	RO	0x1	pd_cpu3_c0_pwr_stat The power state of PD_CPU3 power chain 0. 1'b0: Power down 1'b1: Power up
28	RO	0x1	pd_cpu2_c0_pwr_stat The power state of PD_CPU2 power chain 0. 1'b0: Power down 1'b1: Power up
27	RO	0x1	pd_cpu1_c0_pwr_stat The power state of PD_CPU1 power chain 0. 1'b0: Power down 1'b1: Power up
26	RO	0x1	pd_cpu0_c0_pwr_stat The power state of PD_CPU0 power chain 0. 1'b0: Power down 1'b1: Power up
25	RO	0x0	reserved
24	RO	0x1	pd_npu1_c0_pwr_stat The power state of PD_NPU1 power chain 0. 1'b0: Power down 1'b1: Power up
23	RO	0x1	pd_npu0_c0_pwr_stat The power state of PD_NPU0 power chain 0. 1'b0: Power down 1'b1: Power up
22	RO	0x1	pd_nputop_c0_pwr_stat The power state of PD_NPUTOP power chain 0. 1'b0: Power down 1'b1: Power up
21	RO	0x1	pd_vpu_c0_pwr_stat The power state of PD_VPU power chain 0. 1'b0: Power down 1'b1: Power up
20	RO	0x1	pd_vdec_c0_pwr_stat The power state of PD_VDEC power chain 0. 1'b0: Power down 1'b1: Power up
19	RO	0x1	pd_vepu1_c0_pwr_stat The power state of PD_VEPU1 power chain 0. 1'b0: Power down 1'b1: Power up
18	RO	0x1	pd_vepu0_c0_pwr_stat The power state of PD_VEPU0 power chain 0. 1'b0: Power down 1'b1: Power up
17	RO	0x1	pd_vi_c0_pwr_stat The power state of PD_VI power chain 0. 1'b0: Power down 1'b1: Power up

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Bit	Attr	Reset Value	Description
16	RO	0x1	pd_usb_c0_pwr_stat The power state of PD_USB power chain 0. 1'b0: Power down 1'b1: Power up
15	RO	0x1	pd_vo0_c0_pwr_stat The power state of PD_VO0 power chain 0. 1'b0: Power down 1'b1: Power up
14	RO	0x1	pd_vo1_c0_pwr_stat The power state of PD_VO1 power chain 0. 1'b0: Power down 1'b1: Power up
13	RO	0x1	pd_vop_cluster_c0_pwr_stat The power state of PD_VOP_CLUSTER power chain 0. 1'b0: Power down 1'b1: Power up
12	RO	0x1	pd_vop_esmart_c0_pwr_stat The power state of PD_VOP_ESMART power chain 0. 1'b0: Power down 1'b1: Power up
11	RO	0x1	pd_vop_c0_pwr_stat The power state of PD_VOP power chain 0. 1'b0: Power down 1'b1: Power up
10	RO	0x1	pd_subphp_c0_pwr_stat The power state of PD_SUBPHP power chain 0. 1'b0: Power down 1'b1: Power up
9	RO	0x1	pd_php_c0_pwr_stat The power state of PD_PHP power chain 0. 1'b0: Power down 1'b1: Power up
8	RO	0x1	pd_audio_c0_pwr_stat The power state of PD_AUDIO power chain 0. 1'b0: Power down 1'b1: Power up
7	RO	0x1	pd_sdgmac_c0_pwr_stat The power state of PD_SDGMAC power chain 0. 1'b0: Power down 1'b1: Power up
6	RO	0x1	pd_nvm_c0_pwr_stat The power state of PD_NVM power chain 0. 1'b0: Power down 1'b1: Power up
5:4	RO	0x0	reserved
3	RO	0x1	pd_center_c0_pwr_stat The power state of PD_CENTER power chain 0. 1'b0: Power down 1'b1: Power up
2:0	RO	0x0	reserved

PMU_PWR_CHAIN0_STS1

Address: Operational Base(0x27360000) + offset (0x20244)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3	RO	0x1	pd_bigcore_c0_pwr_stat The power state of PD_BIGCORE power chain 0. 1'b0: Power down 1'b1: Power up
2	RO	0x1	pd_cpu7_c0_pwr_stat The power state of PD_CPU7 power chain 0. 1'b0: Power down 1'b1: Power up
1	RO	0x1	pd_cpu6_c0_pwr_stat The power state of PD_CPU6 power chain 0. 1'b0: Power down 1'b1: Power up
0	RO	0x1	pd_cpu5_c0_pwr_stat The power state of PD_CPU5 power chain 0. 1'b0: Power down 1'b1: Power up

PMU_PWR_CHAIN1_STS0

Address: Operational Base(0x27360000) + offset (0x20248)

Bit	Attr	Reset Value	Description
31	RO	0x1	pd_cpu4_c1_pwr_stat The power state of PD_CPU4 power chain 1. 1'b0: Power down 1'b1: Power up
30	RO	0x0	reserved
29	RO	0x1	pd_cpu3_c1_pwr_stat The power state of PD_CPU3 power chain 1. 1'b0: Power down 1'b1: Power up
28	RO	0x1	pd_cpu2_c1_pwr_stat The power state of PD_CPU2 power chain 1. 1'b0: Power down 1'b1: Power up
27	RO	0x1	pd_cpu1_c1_pwr_stat The power state of PD_CPU1 power chain 1. 1'b0: Power down 1'b1: Power up
26	RO	0x1	pd_cpu0_c1_pwr_stat The power state of PD_CPU0 power chain 1. 1'b0: Power down 1'b1: Power up
25	RO	0x0	reserved
24	RO	0x1	pd_npu1_c1_pwr_stat The power state of PD_NPU1 power chain 1. 1'b0: Power down 1'b1: Power up
23	RO	0x1	pd_npu0_c1_pwr_stat The power state of PD_NPU0 power chain 1. 1'b0: Power down 1'b1: Power up
22	RO	0x1	pd_nputop_c1_pwr_stat The power state of PD_NPUTOP power chain 1. 1'b0: Power down 1'b1: Power up

Bit	Attr	Reset Value	Description
21	RO	0x1	pd_vpu_c1_pwr_stat The power state of PD_VPU power chain 1. 1'b0: Power down 1'b1: Power up
20	RO	0x1	pd_vdec_c1_pwr_stat The power state of PD_VDEC power chain 1. 1'b0: Power down 1'b1: Power up
19	RO	0x1	pd_vepu1_c1_pwr_stat The power state of PD_VEPU1 power chain 1. 1'b0: Power down 1'b1: Power up
18	RO	0x1	pd_vepu0_c1_pwr_stat The power state of PD_VEPU0 power chain 1. 1'b0: Power down 1'b1: Power up
17	RO	0x1	pd_vi_c1_pwr_stat The power state of PD_VI power chain 1. 1'b0: Power down 1'b1: Power up
16	RO	0x1	pd_usb_c1_pwr_stat The power state of PD_USB power chain 1. 1'b0: Power down 1'b1: Power up
15	RO	0x1	pd_vo0_c1_pwr_stat The power state of PD_VO0 power chain 1. 1'b0: Power down 1'b1: Power up
14	RO	0x1	pd_vo1_c1_pwr_stat The power state of PD_VO1 power chain 1. 1'b0: Power down 1'b1: Power up
13	RO	0x1	pd_vop_cluster_c1_pwr_stat The power state of PD_VOP_CLUSTER power chain 1. 1'b0: Power down 1'b1: Power up
12	RO	0x1	pd_vop_esmart_c1_pwr_stat The power state of PD_VOP_ESMART power chain 1. 1'b0: Power down 1'b1: Power up
11	RO	0x1	pd_vop_c1_pwr_stat The power state of PD_VOP power chain 1. 1'b0: Power down 1'b1: Power up
10	RO	0x1	pd_subphp_c1_pwr_stat The power state of PD_SUBPHP power chain 1. 1'b0: Power down 1'b1: Power up
9	RO	0x1	pd_php_c1_pwr_stat The power state of PD_PHP power chain 1. 1'b0: Power down 1'b1: Power up
8	RO	0x1	pd_audio_c1_pwr_stat The power state of PD_AUDIO power chain 1. 1'b0: Power down 1'b1: Power up

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Bit	Attr	Reset Value	Description
7	RO	0x1	pd_sdgmac_c1_pwr_stat The power state of PD_SDGMAC power chain 1. 1'b0: Power down 1'b1: Power up
6	RO	0x1	pd_nvm_c1_pwr_stat The power state of PD_NVM power chain 1. 1'b0: Power down 1'b1: Power up
5:4	RO	0x0	reserved
3	RO	0x1	pd_center_c1_pwr_stat The power state of PD_CENTER power chain 1. 1'b0: Power down 1'b1: Power up
2:0	RO	0x0	reserved

PMU_PWR_CHAIN1_STS1

Address: Operational Base(0x27360000) + offset (0x2024C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x1	pd_bigcore_c1_pwr_stat The power state of PD_BIGCORE power chain 1. 1'b0: Power down 1'b1: Power up
2	RO	0x1	pd_cpu7_c1_pwr_stat The power state of PD_CPU7 power chain 1. 1'b0: Power down 1'b1: Power up
1	RO	0x1	pd_cpu6_c1_pwr_stat The power state of PD_CPU6 power chain 1. 1'b0: Power down 1'b1: Power up
0	RO	0x1	pd_cpu5_c1_pwr_stat The power state of PD_CPU5 power chain 1. 1'b0: Power down 1'b1: Power up

PMU_PWR_MEM_STS0

Address: Operational Base(0x27360000) + offset (0x20250)

Bit	Attr	Reset Value	Description
31	RO	0x0	pd_cpu4_mem_pwr_stat The power state of PD_CPU4 memory. 1'b0: Power up 1'b1: Power down
30	RO	0x0	reserved
29	RO	0x0	pd_cpu3_mem_pwr_stat The power state of PD_CPU3 memory. 1'b0: Power up 1'b1: Power down
28	RO	0x0	pd_cpu2_mem_pwr_stat The power state of PD_CPU2 memory. 1'b0: Power up 1'b1: Power down

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Bit	Attr	Reset Value	Description
27	RO	0x0	pd_cpu1_mem_pwr_stat The power state of PD_CPU1 memory. 1'b0: Power up 1'b1: Power down
26	RO	0x0	pd_cpu0_mem_pwr_stat The power state of PD_CPU0 memory. 1'b0: Power up 1'b1: Power down
25	RO	0x0	reserved
24	RO	0x0	pd_npu1_mem_pwr_stat The power state of PD_NPU1 memory. 1'b0: Power up 1'b1: Power down
23	RO	0x0	pd_npu0_mem_pwr_stat The power state of PD_NPU0 memory. 1'b0: Power up 1'b1: Power down
22	RO	0x0	pd_nputop_mem_pwr_stat The power state of PD_NPUTOP memory. 1'b0: Power up 1'b1: Power down
21	RO	0x0	pd_vpu_mem_pwr_stat The power state of PD_VPU memory. 1'b0: Power up 1'b1: Power down
20	RO	0x0	pd_vdec_mem_pwr_stat The power state of PD_VDEC memory. 1'b0: Power up 1'b1: Power down
19	RO	0x0	pd_vepu1_mem_pwr_stat The power state of PD_VEPU1 memory. 1'b0: Power up 1'b1: Power down
18	RO	0x0	pd_vepu0_mem_pwr_stat The power state of PD_VEPU0 memory. 1'b0: Power up 1'b1: Power down
17	RO	0x0	pd_vi_mem_pwr_stat The power state of PD_VI memory. 1'b0: Power up 1'b1: Power down
16	RO	0x0	pd_usb_mem_pwr_stat The power state of PD_USB memory. 1'b0: Power up 1'b1: Power down
15	RO	0x0	pd_vo0_mem_pwr_stat The power state of PD_VO0 memory. 1'b0: Power up 1'b1: Power down
14	RO	0x0	pd_vo1_mem_pwr_stat The power state of PD_VO1 memory. 1'b0: Power up 1'b1: Power down

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Bit	Attr	Reset Value	Description
13	RO	0x0	pd_vop_cluster_mem_pwr_stat The power state of PD_VOP_CLUSTER memory. 1'b0: Power up 1'b1: Power down
12	RO	0x0	pd_vop_esmart_mem_pwr_stat The power state of PD_VOP_ESMART memory. 1'b0: Power up 1'b1: Power down
11	RO	0x0	pd_vop_mem_pwr_stat The power state of PD_VOP memory. 1'b0: Power up 1'b1: Power down
10	RO	0x0	pd_subphp_mem_pwr_stat The power state of PD_SUBPHP memory. 1'b0: Power up 1'b1: Power down
9	RO	0x0	pd_php_mem_pwr_stat The power state of PD_PHP memory. 1'b0: Power up 1'b1: Power down
8	RO	0x0	pd_audio_mem_pwr_stat The power state of PD_AUDIO memory. 1'b0: Power up 1'b1: Power down
7	RO	0x0	pd_sdgmac_mem_pwr_stat The power state of PD_SDGMAC memory. 1'b0: Power up 1'b1: Power down
6	RO	0x0	pd_nvm_mem_pwr_stat The power state of PD_NVM memory. 1'b0: Power up 1'b1: Power down
5:4	RO	0x0	reserved
3	RO	0x0	pd_center_mem_pwr_stat The power state of PD_CENTER memory. 1'b0: Power up 1'b1: Power down
2:0	RO	0x0	reserved

PMU_PWR_MEM_STS1

Address: Operational Base(0x27360000) + offset (0x20254)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	pd_bigcore_mem_pwr_stat The power state of PD_BIGCORE memory. 1'b0: Power up 1'b1: Power down
2	RO	0x0	pd_cpu7_mem_pwr_stat The power state of PD_CPU7 memory. 1'b0: Power up 1'b1: Power down
1	RO	0x0	pd_cpu6_mem_pwr_stat The power state of PD_CPU6 memory. 1'b0: Power up 1'b1: Power down

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Bit	Attr	Reset Value	Description
0	RO	0x0	pd_cpu5_mem_pwr_stat The power state of PD_CPU5 memory. 1'b0: Power up 1'b1: Power down

PMU_PWR_CHAIN_PWRUP_CON0

Address: Operational Base(0x27360000) + offset (0x20260)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	pd_vo0_pwrup_stable_ena Enable stable counter between power chains for PD_VO0 power up flow. 1'b0: Disable 1'b1: Enable
14	RW	0x1	pd_vo1_pwrup_stable_ena Enable stable counter between power chains for PD_VO1 power up flow. 1'b0: Disable 1'b1: Enable
13	RW	0x1	pd_vop_cluster_pwrup_stable_ena Enable stable counter between power chains for PD_VOP_CLUSTER power up flow. 1'b0: Disable 1'b1: Enable
12	RW	0x1	pd_vop_esmart_pwrup_stable_ena Enable stable counter between power chains for PD_VOP_ESMART power up flow. 1'b0: Disable 1'b1: Enable
11	RW	0x1	pd_vop_pwrup_stable_ena Enable stable counter between power chains for PD_VOP power up flow. 1'b0: Disable 1'b1: Enable
10	RW	0x1	pd_subphp_pwrup_stable_ena Enable stable counter between power chains for PD_SUBPHP power up flow. 1'b0: Disable 1'b1: Enable
9	RW	0x1	pd_php_pwrup_stable_ena Enable stable counter between power chains for PD_PHP power up flow. 1'b0: Disable 1'b1: Enable
8	RW	0x1	pd_audio_pwrup_stable_ena Enable stable counter between power chains for PD_AUDIO power up flow. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
7	RW	0x1	pd_sdgmac_pwrup_stable_ena Enable stable counter between power chains for PD_SDGMAC power up flow. 1'b0: Disable 1'b1: Enable
6	RW	0x1	pd_nvm_pwrup_stable_ena Enable stable counter between power chains for PD_NVM power up flow. 1'b0: Disable 1'b1: Enable
5:4	RO	0x0	reserved
3	RW	0x1	pd_center_pwrup_stable_ena Enable stable counter between power chains for PD_CENTER power up flow. 1'b0: Disable 1'b1: Enable
2:0	RO	0x0	reserved

PMU_PWR_CHAIN_PWRUP_CON1

Address: Operational Base(0x27360000) + offset (0x20264)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	pd_cpu4_pwrup_stable_ena Enable stable counter between power chains for PD_CPU4 power up flow. 1'b0: Disable 1'b1: Enable
14	RO	0x0	reserved
13	RW	0x1	pd_cpu3_pwrup_stable_ena Enable stable counter between power chains for PD_CPU3 power up flow. 1'b0: Disable 1'b1: Enable
12	RW	0x1	pd_cpu2_pwrup_stable_ena Enable stable counter between power chains for PD_CPU2 power up flow. 1'b0: Disable 1'b1: Enable
11	RW	0x1	pd_cpu1_pwrup_stable_ena Enable stable counter between power chains for PD_CPU1 power up flow. 1'b0: Disable 1'b1: Enable
10	RW	0x1	pd_cpu0_pwrup_stable_ena Enable stable counter between power chains for PD_CPU0 power up flow. 1'b0: Disable 1'b1: Enable
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x1	pd_npu1_pwrup_stable_ena Enable stable counter between power chains for PD_NPU1 power up flow. 1'b0: Disable 1'b1: Enable
7	RW	0x1	pd_npu0_pwrup_stable_ena Enable stable counter between power chains for PD_NPU0 power up flow. 1'b0: Disable 1'b1: Enable
6	RW	0x1	pd_nputop_pwrup_stable_ena Enable stable counter between power chains for PD_NPUTOP power up flow. 1'b0: Disable 1'b1: Enable
5	RW	0x1	pd_vpu_pwrup_stable_ena Enable stable counter between power chains for PD_VPU power up flow. 1'b0: Disable 1'b1: Enable
4	RW	0x1	pd_vdec_pwrup_stable_ena Enable stable counter between power chains for PD_VDEC power up flow. 1'b0: Disable 1'b1: Enable
3	RW	0x1	pd_vepu1_pwrup_stable_ena Enable stable counter between power chains for PD_VEPU1 power up flow. 1'b0: Disable 1'b1: Enable
2	RW	0x1	pd_vepu0_pwrup_stable_ena Enable stable counter between power chains for PD_VEPU0 power up flow. 1'b0: Disable 1'b1: Enable
1	RW	0x1	pd_vi_pwrup_stable_ena Enable stable counter between power chains for PD_VI power up flow. 1'b0: Disable 1'b1: Enable
0	RW	0x1	pd_usb_pwrup_stable_ena Enable stable counter between power chains for PD_USB power up flow. 1'b0: Disable 1'b1: Enable

PMU_PWR_CHAIN_PWRUP_CON2

Address: Operational Base(0x27360000) + offset (0x20268)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x1	pd_bigcore_pwrup_stable_ena Enable stable counter between power chains for PD_BIGCORE power up flow. 1'b0: Disable 1'b1: Enable
2	RW	0x1	pd_cpu7_pwrup_stable_ena Enable stable counter between power chains for PD_CPU7 power up flow. 1'b0: Disable 1'b1: Enable
1	RW	0x1	pd_cpu6_pwrup_stable_ena Enable stable counter between power chains for PD_CPU6 power up flow. 1'b0: Disable 1'b1: Enable
0	RW	0x1	pd_cpu5_pwrup_stable_ena Enable stable counter between power chains for PD_CPU5 power up flow. 1'b0: Disable 1'b1: Enable

PMU_PWR_CHAIN_PWRDN_CON0

Address: Operational Base(0x27360000) + offset (0x20270)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_pwrdn_stable_ena Enable stable counter between power chains for PD_VO0 power down flow. 1'b0: Disable 1'b1: Enable
14	RW	0x0	pd_vo1_pwrdn_stable_ena Enable stable counter between power chains for PD_VO1 power down flow. 1'b0: Disable 1'b1: Enable
13	RW	0x0	pd_vop_cluster_pwrdn_stable_ena Enable stable counter between power chains for PD_VOP_CLUSTER power down flow. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pd_vop_esmart_pwrdn_stable_ena Enable stable counter between power chains for PD_VOP_ESMART power down flow. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pd_vop_pwrdn_stable_ena Enable stable counter between power chains for PD_VOP power down flow. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
10	RW	0x0	pd_subphp_pwrdn_stable_ena Enable stable counter between power chains for PD_SUBPHP power down flow. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pd_php_pwrdn_stable_ena Enable stable counter between power chains for PD_PHP power down flow. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_audio_pwrdn_stable_ena Enable stable counter between power chains for PD_AUDIO power down flow. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_sdgmac_pwrdn_stable_ena Enable stable counter between power chains for PD_SDGMAC power down flow. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nvm_pwrdn_stable_ena Enable stable counter between power chains for PD_NVM power down flow. 1'b0: Disable 1'b1: Enable
5:4	RO	0x0	reserved
3	RW	0x0	pd_center_pwrdn_stable_ena Enable stable counter between power chains for PD_CENTER power down flow. 1'b0: Disable 1'b1: Enable
2:0	RO	0x0	reserved

PMU_PWR_CHAIN_PWRDN_CON1

Address: Operational Base(0x27360000) + offset (0x20274)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_cpu4_pwrdn_stable_ena Enable stable counter between power chains for PD_CPU4 power down flow. 1'b0: Disable 1'b1: Enable
14	RO	0x0	reserved
13	RW	0x0	pd_cpu3_pwrdn_stable_ena Enable stable counter between power chains for PD_CPU3 power down flow. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
12	RW	0x0	pd_cpu2_pwrdn_stable_ena Enable stable counter between power chains for PD_CPU2 power down flow. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pd_cpu1_pwrdn_stable_ena Enable stable counter between power chains for PD_CPU1 power down flow. 1'b0: Disable 1'b1: Enable
10	RW	0x0	pd_cpu0_pwrdn_stable_ena Enable stable counter between power chains for PD_CPU0 power down flow. 1'b0: Disable 1'b1: Enable
9	RO	0x0	reserved
8	RW	0x0	pd_npu1_pwrdn_stable_ena Enable stable counter between power chains for PD_NPU1 power down flow. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_npu0_pwrdn_stable_ena Enable stable counter between power chains for PD_NPU0 power down flow. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nputop_pwrdn_stable_ena Enable stable counter between power chains for PD_NPUTOP power down flow. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_vpu_pwrdn_stable_ena Enable stable counter between power chains for PD_VPU power down flow. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_vdec_pwrdn_stable_ena Enable stable counter between power chains for PD_VDEC power down flow. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_vepu1_pwrdn_stable_ena Enable stable counter between power chains for PD_VEPU1 power down flow. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vepu0_pwrdn_stable_ena Enable stable counter between power chains for PD_VEPU0 power down flow. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vi_pwrdn_stable_ena Enable stable counter between power chains for PD_VI power down flow. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	pd_usb_pwrdn_stable_ena Enable stable counter between power chains for PD_USB power down flow. 1'b0: Disable 1'b1: Enable

PMU_PWR_CHAIN_PWRDN_CON2

Address: Operational Base(0x27360000) + offset (0x20278)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	pd_bigcore_pwrdn_stable_ena Enable stable counter between power chains for PD_BIGCORE power down flow. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_cpu7_pwrdn_stable_ena Enable stable counter between power chains for PD_CPU7 power down flow. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_cpu6_pwrdn_stable_ena Enable stable counter between power chains for PD_CPU6 power down flow. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_cpu5_pwrdn_stable_ena Enable stable counter between power chains for PD_CPU5 power down flow. 1'b0: Disable 1'b1: Enable

PMU_PWR_STABLE_CNT_THRES

Address: Operational Base(0x27360000) + offset (0x2027C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x1f	pwrdn_stable_cnt Count for power chain power down stability. Number of clk_pmu used by counter logic.
15:5	RO	0x000	reserved
4:0	RW	0x1f	pwrup_stable_cnt Count for power chain power up stability. Number of clk_pmu used by counter logic.

PMU_VOL_GATE_FAST_CON

Address: Operational Base(0x27360000) + offset (0x20284)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	vd_gpu_fast_ena Enable VD_GPU fast power control. When asserted, it means that VD_GPU will power up completely if VD_GPU power up count from PMU_GPU_PWRUP_CNT to zero when VD_GPU power up request active, or VD_GPU will power down completely if VD_GPU power down count from PMU_GPU_PWRDN_CNT to zero when VD_GPU power down request active. Otherwise, it means that VD_GPU will power up completely as soon as VD_GPU power up request active, or power down completely as soon as VD_GPU power down request active. 1'b0: Disable 1'b1: Enable
1	RW	0x0	vd_litcore_fast_ena Enable VD_LITCORE fast power control. When asserted, it means that VD_LITCORE will power up completely if VD_LITCORE power up count from PMU_LITCORE_PWRUP_CNT to zero when VD_LITCORE power up request active, or VD_LITCORE will power down completely if VD_LITCORE power down count from PMU_LITCORE_PWRDN_CNT to zero when VD_LITCORE power down request active. Otherwise, it means that VD_LITCORE will power up completely as soon as VD_LITCORE power up request active, or power down completely as soon as VD_LITCORE power down request active. 1'b0: Disable 1'b1: Enable
0	RW	0x0	vd_npu_fast_ena Enable VD_NPU fast power control. When asserted, it means that VD_NPU will power up completely if VD_NPU power up count from PMU_NPU_PWRUP_CNT to zero when VD_NPU power up request active, or VD_NPU will power down completely if VD_NPU power down count from PMU_NPU_PWRDN_CNT to zero when VD_NPU power down request active. Otherwise, it means that VD_NPU will power up completely as soon as VD_NPU power up request active, or power down completely as soon as VD_NPU power down request active. 1'b0: Disable 1'b1: Enable

PMU_NPU_PWRUP_CNT

Address: Operational Base(0x27360000) + offset (0x20288)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	npu_pwrup_cnt VD_NPU power up count. Number of clk_pmu used by counter logic.

PMU_NPU_PWRDN_CNT

Address: Operational Base(0x27360000) + offset (0x2028C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	npu_pwrdn_cnt VD_NPU power down count. Number of clk_pmu used by counter logic.

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PMU_LITCORE_PWRUP_CNT

Address: Operational Base(0x27360000) + offset (0x20290)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	litcore_pwrup_cnt VD_LITCORE power up count. Number of clk_pmu used by counter logic.

PMU_LITCORE_PWRDN_CNT

Address: Operational Base(0x27360000) + offset (0x20294)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	litcore_pwrdn_cnt VD_LITCORE power down count. Number of clk_pmu used by counter logic.

PMU_GPU_PWRUP_CNT

Address: Operational Base(0x27360000) + offset (0x20298)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	gpu_pwrup_cnt VD_GPU power up count. Number of clk_pmu used by counter logic.

PMU_GPU_PWRDN_CNT

Address: Operational Base(0x27360000) + offset (0x2029C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	gpu_pwrdn_cnt VD_GPU power down count. Number of clk_pmu used by counter logic.

PMU_MEM_PWR_GATE_SFTCON0

Address: Operational Base(0x27360000) + offset (0x20300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_mem_dwn_sftena Enable power down PD_VO0 memory by software. 1'b0: Disable 1'b1: Enable
14	RW	0x0	pd_vo1_mem_dwn_sftena Enable power down PD_VO1 memory by software. 1'b0: Disable 1'b1: Enable
13	RW	0x0	pd_vop_cluster_mem_dwn_sftena Enable power down PD_VOP_CLUSTER memory by software. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pd_vop_esmart_mem_dwn_sftena Enable power down PD_VOP_ESMART memory by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11	RW	0x0	pd_vop_mem_dwn_sftena Enable power down PD_VOP memory by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	pd_subphp_mem_dwn_sftena Enable power down PD_SUBPHP memory by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pd_php_mem_dwn_sftena Enable power down PD_PHP memory by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_audio_mem_dwn_sftena Enable power down PD_AUDIO memory by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_sdgmac_mem_dwn_sftena Enable power down PD_SDGMAC memory by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nvm_mem_dwn_sftena Enable power down PD_NVM memory by software. 1'b0: Disable 1'b1: Enable
5:4	RO	0x0	reserved
3	RW	0x0	pd_center_mem_dwn_sftena Enable power down PD_CENTER memory by software. 1'b0: Disable 1'b1: Enable
2:0	RO	0x0	reserved

PMU_MEM_PWR_GATE_SFTCON1

Address: Operational Base(0x27360000) + offset (0x20304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pd_npu1_mem_dwn_sftena Enable power down PD_NPU1 memory by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_npu0_mem_dwn_sftena Enable power down PD_NPU0 memory by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nputop_mem_dwn_sftena Enable power down PD_NPUTOP memory by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_vpu_mem_dwn_sftena Enable power down PD_VPU memory by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	pd_vdec_mem_dwn_sftena Enable power down PD_VDEC memory by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_vepu1_mem_dwn_sftena Enable power down PD_VEPU1 memory by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vepu0_mem_dwn_sftena Enable power down PD_VEPU0 memory by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vi_mem_dwn_sftena Enable power down PD_VI memory by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_usb_mem_dwn_sftena Enable power down PD_USB memory by software. 1'b0: Disable 1'b1: Enable

PMU_PWR_C0_ACK_SEL_CON0

Address: Operational Base(0x27360000) + offset (0x20380)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pd_bigcore_dwn_c0_ack_sel PD_BIGCORE power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
7	RW	0x0	pd_cpu7_dwn_c0_ack_sel PD_CPU7 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
6	RW	0x0	pd_cpu6_dwn_c0_ack_sel PD_CPU6 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
5	RW	0x0	pd_cpu5_dwn_c0_ack_sel PD_CPU5 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
4	RW	0x0	pd_cpu4_dwn_c0_ack_sel PD_CPU4 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
3	RW	0x0	pd_cpu3_dwn_c0_ack_sel PD_CPU3 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal

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Bit	Attr	Reset Value	Description
2	RW	0x0	pd_cpu2_dwn_c0_ack_sel PD_CPU2 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
1	RW	0x0	pd_cpu1_dwn_c0_ack_sel PD_CPU1 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
0	RW	0x0	pd_cpu0_dwn_c0_ack_sel PD_CPU0 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal

PMU_PWR_C0_ACK_SEL_CON1

Address: Operational Base(0x27360000) + offset (0x20384)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_dwn_c0_ack_sel PD_VO0 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
14	RW	0x0	pd_vo1_dwn_c0_ack_sel PD_VO1 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
13	RW	0x0	pd_vop_cluster_dwn_c0_ack_sel PD_VOP_CLUSTER power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
12	RW	0x0	pd_vop_esmart_dwn_c0_ack_sel PD_VOP_ESMART power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
11	RW	0x0	pd_vop_dwn_c0_ack_sel PD_VOP power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
10	RW	0x0	pd_subphp_dwn_c0_ack_sel PD_SUBPHP power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
9	RW	0x0	pd_php_dwn_c0_ack_sel PD_PHP power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
8	RW	0x0	pd_audio_dwn_c0_ack_sel PD_AUDIO power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal

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Bit	Attr	Reset Value	Description
7	RW	0x0	pd_sdgmac_dwn_c0_ack_sel PD_SDGMAC power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
6	RW	0x0	pd_nvm_dwn_c0_ack_sel PD_NVM power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
5:4	RO	0x0	reserved
3	RW	0x0	pd_center_dwn_c0_ack_sel PD_CENTER power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
2:0	RO	0x0	reserved

PMU_PWR_C0_ACK_SEL_CON2

Address: Operational Base(0x27360000) + offset (0x20388)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pd_npu1_dwn_c0_ack_sel PD_NPU1 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
7	RW	0x0	pd_npu0_dwn_c0_ack_sel PD_NPU0 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
6	RW	0x0	pd_nputop_dwn_c0_ack_sel PD_NPUTOP power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
5	RW	0x0	pd_vpu_dwn_c0_ack_sel PD_VPU power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
4	RW	0x0	pd_vdec_dwn_c0_ack_sel PD_VDEC power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
3	RW	0x0	pd_vepu1_dwn_c0_ack_sel PD_VEPU1 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
2	RW	0x0	pd_vepu0_dwn_c0_ack_sel PD_VEPU0 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal
1	RW	0x0	pd_vi_dwn_c0_ack_sel PD_VI power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1’b1: From power chain 0 request signal

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Bit	Attr	Reset Value	Description
0	RW	0x0	pd_usb_dwn_c0_ack_sel PD_USB power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal

PMU_PWR_C1_ACK_SEL_CON0

Address: Operational Base(0x27360000) + offset (0x20390)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pd_bigcore_dwn_c1_ack_sel PD_BIGCORE power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
7	RW	0x0	pd_cpu7_dwn_c1_ack_sel PD_CPU7 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
6	RW	0x0	pd_cpu6_dwn_c1_ack_sel PD_CPU6 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
5	RW	0x0	pd_cpu5_dwn_c1_ack_sel PD_CPU5 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
4	RW	0x0	pd_cpu4_dwn_c1_ack_sel PD_CPU4 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
3	RW	0x0	pd_cpu3_dwn_c1_ack_sel PD_CPU3 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
2	RW	0x0	pd_cpu2_dwn_c1_ack_sel PD_CPU2 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
1	RW	0x0	pd_cpu1_dwn_c1_ack_sel PD_CPU1 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
0	RW	0x0	pd_cpu0_dwn_c1_ack_sel PD_CPU0 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal

PMU_PWR_C1_ACK_SEL_CON1

Address: Operational Base(0x27360000) + offset (0x20394)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_dwn_c1_ack_sel PD_VO0 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
14	RW	0x0	pd_vo1_dwn_c1_ack_sel PD_VO1 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
13	RW	0x0	pd_vop_cluster_dwn_c1_ack_sel PD_VOP_CLUSTER power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
12	RW	0x0	pd_vop_esmart_dwn_c1_ack_sel PD_VOP_ESMART power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
11	RW	0x0	pd_vop_dwn_c1_ack_sel PD_VOP power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
10	RW	0x0	pd_subphp_dwn_c1_ack_sel PD_SUBPHP power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
9	RW	0x0	pd_php_dwn_c1_ack_sel PD_PHP power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
8	RW	0x0	pd_audio_dwn_c1_ack_sel PD_AUDIO power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
7	RW	0x0	pd_sdgmac_dwn_c1_ack_sel PD_SDGMAC power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
6	RW	0x0	pd_nvm_dwn_c1_ack_sel PD_NVM power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
5:4	RO	0x0	reserved
3	RW	0x0	pd_center_dwn_c1_ack_sel PD_CENTER power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
2:0	RO	0x0	reserved

PMU_PWR_C1_ACK_SEL_CON2

Address: Operational Base(0x27360000) + offset (0x20398)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pd_npu1_dwn_c1_ack_sel PD_NPU1 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
7	RW	0x0	pd_npu0_dwn_c1_ack_sel PD_NPU0 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
6	RW	0x0	pd_nputop_dwn_c1_ack_sel PD_NPUTOP power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
5	RW	0x0	pd_vpu_dwn_c1_ack_sel PD_VPU power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
4	RW	0x0	pd_vdec_dwn_c1_ack_sel PD_VDEC power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
3	RW	0x0	pd_vepu1_dwn_c1_ack_sel PD_VEPU1 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
2	RW	0x0	pd_vepu0_dwn_c1_ack_sel PD_VEPU0 power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
1	RW	0x0	pd_vi_dwn_c1_ack_sel PD_VI power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal
0	RW	0x0	pd_usb_dwn_c1_ack_sel PD_USB power chain 1 acknowledge signal selection. 1'b0: From power chain 1 output 1'b1: From power chain 1 request signal

PMU_PWR_MEM_ACK_SEL_CON0

Address: Operational Base(0x27360000) + offset (0x203A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pd_bigcore_dwn_mem_ack_sel PD_BIGCORE memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal

Bit	Attr	Reset Value	Description
7	RW	0x0	pd_cpu7_dwn_mem_ack_sel PD_CPU7 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
6	RW	0x0	pd_cpu6_dwn_mem_ack_sel PD_CPU6 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
5	RW	0x0	pd_cpu5_dwn_mem_ack_sel PD_CPU5 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
4	RW	0x0	pd_cpu4_dwn_mem_ack_sel PD_CPU4 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
3	RW	0x0	pd_cpu3_dwn_mem_ack_sel PD_CPU3 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
2	RW	0x0	pd_cpu2_dwn_mem_ack_sel PD_CPU2 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
1	RW	0x0	pd_cpu1_dwn_mem_ack_sel PD_CPU1 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
0	RW	0x0	pd_cpu0_dwn_mem_ack_sel PD_CPU0 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal

PMU_PWR_MEM_ACK_SEL_CON1

Address: Operational Base(0x27360000) + offset (0x203A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_dwn_mem_ack_sel PD_VO0 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
14	RW	0x0	pd_vo1_dwn_mem_ack_sel PD_VO1 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
13	RW	0x0	pd_vop_cluster_dwn_mem_ack_sel PD_VOP_CLUSTER memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal

Bit	Attr	Reset Value	Description
12	RW	0x0	pd_vop_esmart_dwn_mem_ack_sel PD_VOP_ESMART memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
11	RW	0x0	pd_vop_dwn_mem_ack_sel PD_VOP memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
10	RW	0x0	pd_subphp_dwn_mem_ack_sel PD_SUBPHP memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
9	RW	0x0	pd_php_dwn_mem_ack_sel PD_PHP memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
8	RW	0x0	pd_audio_dwn_mem_ack_sel PD_AUDIO memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
7	RW	0x0	pd_sdgmac_dwn_mem_ack_sel PD_SDGMAC memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
6	RW	0x0	pd_nvm_dwn_mem_ack_sel PD_NVM memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
5:4	RO	0x0	reserved
3	RW	0x0	pd_center_dwn_mem_ack_sel PD_CENTER memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
2:0	RO	0x0	reserved

PMU_PWR_MEM_ACK_SEL_CON2

Address: Operational Base(0x27360000) + offset (0x203A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pd_npu1_dwn_mem_ack_sel PD_NPU1 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal
7	RW	0x0	pd_npu0_dwn_mem_ack_sel PD_NPU0 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1'b1: From memory power chain request signal

Bit	Attr	Reset Value	Description
6	RW	0x0	pd_nputop_dwn_mem_ack_sel PD_NPUTOP memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
5	RW	0x0	pd_vpu_dwn_mem_ack_sel PD_VPU memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
4	RW	0x0	pd_vdec_dwn_mem_ack_sel PD_VDEC memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
3	RW	0x0	pd_vepu1_dwn_mem_ack_sel PD_VEPU1 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
2	RW	0x0	pd_vepu0_dwn_mem_ack_sel PD_VEPU0 memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
1	RW	0x0	pd_vi_dwn_mem_ack_sel PD_VI memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal
0	RW	0x0	pd_usb_dwn_mem_ack_sel PD_USB memory power chain acknowledge signal selection. 1'b0: From memory power chain output 1’b1: From memory power chain request signal

PMU_DEBUG_INFO_CON

Address: Operational Base(0x27360000) + offset (0x203F0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	core1_power_state_sel Select PD_BIGCORE power state as debug information output to IO. 1'b0: Not select 1'b1: Select
8	RW	0x0	core0_power_state_sel Select PD_LITCORE power state as debug information output to IO. 1'b0: Not select 1'b1: Select
7:0	RO	0x00	reserved

PMU_BISR_GLB_CON

Address: Operational Base(0x27360000) + offset (0x20500)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	bisr_initrstn_dis Disable initial reset for memory repair logic. 1'b0: Enable 1'b1: Disable
10	RW	0x0	bisr_ctrl_sel Memory repair controller selection. 1'b0: Controlled by hardware 1'b1: Controlled by software
9	RW	0x1	bisr_resetn_sft Generate bisr_resetN by software. 1'b0: Assert reset 1'b1: Dis-assert reset
8	RW	0x0	bisr_repair_mode Memory repair mode. 1'b0: Serial repair mode. In this mode, memory repair will start after power domain is power up, not need to wait for other domain power up. If multi domains are power up at the same time, the repair is executed according to the repair group order. 1'b1: Parallel repair mode. In this mode, memory repair will not start until all specified power domains are power up.
7	RW	0x0	bisr_timeout_ena Enable memory repair timeout counter. 1'b0: Disable 1'b1: Enable. When asserted, counter begins count after repair start. It the counter reachs to BISR_TIMEOUT_THRES hasn't waiting for PDGDone or Done, repair is timeout, and bisr_timeout is high. bisr_timeout is valid only for current repair operation, and will be cleared when new repair start.
6	RW	0x0	bisr_clkgate_sftena Enable memory repair clock gate by software. If asserted, memory repair clock is gated. 1'b0: Disable 1'b1: Enable
5	RW	0x0	bisr_clkgate_ena Enable memory repair clock gate by hardware. If asserted, memory repair clock is auto gated when memory repair is idle. 1'b0: Disable 1'b1: Enable
4:1	RW	0x1	bisr_pdgdone_sel PDGDone source selection. If bit[1]=1, PDGDone come from bisr_PDGDone, controlled by hardware. If bit[2]=1, PDGDone come from BISR_PDGDONE_SFTCON0/1/2, controlled by software. If bit[3]=1, PDGDone come from bisr_Done, controlled by hardware. If bit[4]=1, PDGDone come from bisr_timeout, controlled by hardware. Only one bit can be set to 1 at a time.

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Bit	Attr	Reset Value	Description
0	RW	0x1	bisr_init Enable memory repair initialization. When asserted, the chip will start memory repair flow automatically after chip power up. It should be set to 0 if chip is reset by software. 1'b0: Disable 1'b1: Enable

PMU_BISR_TIMEOUT_THRES

Address: Operational Base(0x27360000) + offset (0x20504)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	bisr_timeout_cnt Timeout count for PDGDone or Done. Number of repair clock used by counter logic.

PMU_BISR_PDGEN_CON0

Address: Operational Base(0x27360000) + offset (0x20510)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	pd_vo0_repair_ena Enable memory repair for PD_VO0 by hardware. 1'b0: Disable 1'b1: Enable
14	RW	0x1	pd_vo1_repair_ena Enable memory repair for PD_VO1 by hardware. 1'b0: Disable 1'b1: Enable
13	RW	0x1	pd_vop_cluster_repair_ena Enable memory repair for PD_VOP_CLUSTER by hardware. 1'b0: Disable 1'b1: Enable
12	RW	0x1	pd_vop_esmart_repair_ena Enable memory repair for PD_VOP_ESMART by hardware. 1'b0: Disable 1'b1: Enable
11	RW	0x1	pd_vop_repair_ena Enable memory repair for PD_VOP by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x1	pd_subphp_repair_ena Enable memory repair for PD_SUBPHP by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x1	pd_php_repair_ena Enable memory repair for PD_PHP by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x1	pd_audio_repair_ena Enable memory repair for PD_AUDIO by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
7	RW	0x1	pd_sdgmac_repair_ena Enable memory repair for PD_SDGMAC by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x1	pd_nvm_repair_ena Enable memory repair for PD_NVM by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x1	pd_cci_repair_ena Enable memory repair for PD_CCI by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x1	pd_ddr_repair_ena Enable memory repair for VD_DDR by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x1	pd_center_repair_ena Enable memory repair for PD_CENTER by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x1	pd_secure_repair_ena Enable memory repair for PD_SECURE by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x1	pd_bus_repair_ena Enable memory repair for PD_BUS by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x1	pd_pmu1_repair_ena Enable memory repair for PD_PMU1 by hardware. 1'b0: Disable 1'b1: Enable

PMU_BISR_PDGEN_CON1

Address: Operational Base(0x27360000) + offset (0x20514)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	pd_litcore_repair_ena Enable memory repair for PD_LITCORE by hardware. 1'b0: Disable 1'b1: Enable
14	RW	0x1	pd_cpu4_repair_ena Enable memory repair for PD_CPU4 by hardware. 1'b0: Disable 1'b1: Enable
13	RW	0x1	pd_cpu5_repair_ena Enable memory repair for PD_CPU5 by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
12	RW	0x1	pd_cpu6_repair_ena Enable memory repair for PD_CPU6 by hardware. 1'b0: Disable 1'b1: Enable
11	RW	0x1	pd_cpu7_repair_ena Enable memory repair for PD_CPU7 by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x1	pd_bigcore_repair_ena Enable memory repair for PD_BIGCORE by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pd_gpu_repair_ena Enable memory repair for VD_GPU by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x1	pd_npu1_repair_ena Enable memory repair for PD_NPU1 by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x1	pd_npu0_repair_ena Enable memory repair for PD_NPU0 by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x1	pd_nputop_repair_ena Enable memory repair for PD_NPUTOP by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x1	pd_vpu_repair_ena Enable memory repair for PD_VPU by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x1	pd_vdec_repair_ena Enable memory repair for PD_VDEC by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x1	pd_vepu1_repair_ena Enable memory repair for PD_VEPU1 by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x1	pd_vepu0_repair_ena Enable memory repair for PD_VEPU0 by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x1	pd_vi_repair_ena Enable memory repair for PD_VI by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x1	pd_usb_repair_ena Enable memory repair for PD_USB by hardware. 1'b0: Disable 1'b1: Enable

PMU_BISR_PDGEN_CON2

Address: Operational Base(0x27360000) + offset (0x20518)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	pd_cpu0_repair_ena Enable memory repair for PD_CPU0 by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x1	pd_cpu1_repair_ena Enable memory repair for PD_CPU1 by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x1	pd_cpu2_repair_ena Enable memory repair for PD_CPU2 by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x1	pd_cpu3_repair_ena Enable memory repair for PD_CPU3 by hardware. 1'b0: Disable 1'b1: Enable

PMU_BISR_PDGEN_SFTCON0

Address: Operational Base(0x27360000) + offset (0x20520)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_repair_sftena Enable memory repair for PD_VO0 by software. 1'b0: Disable 1'b1: Enable
14	RW	0x0	pd_vo1_repair_sftena Enable memory repair for PD_VO1 by software. 1'b0: Disable 1'b1: Enable
13	RW	0x0	pd_vop_cluster_repair_sftena Enable memory repair for PD_VOP_CLUSTER by software. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pd_vop_esmart_repair_sftena Enable memory repair for PD_VOP_ESMART by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pd_vop_repair_sftena Enable memory repair for PD_VOP by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	pd_subphp_repair_sftena Enable memory repair for PD_SUBPHP by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
9	RW	0x0	pd_php_repair_sftena Enable memory repair for PD_PHP by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_audio_repair_sftena Enable memory repair for PD_AUDIO by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_sdgmac_repair_sftena Enable memory repair for PD_SDGMAC by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nvm_repair_sftena Enable memory repair for PD_NVM by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_cci_repair_sftena Enable memory repair for PD_CCI by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_ddr_repair_sftena Enable memory repair for VD_DDR by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_center_repair_sftena Enable memory repair for PD_CENTER by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_secure_repair_sftena Enable memory repair for PD_SECURE by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_bus_repair_sftena Enable memory repair for PD_BUS by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_pmu1_repair_sftena Enable memory repair for PD_PMU1 by software. 1'b0: Disable 1'b1: Enable

PMU_BISR_PDGEN_SFTCON1

Address: Operational Base(0x27360000) + offset (0x20524)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_litcore_repair_sftena Enable memory repair for PD_LITCORE by software. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
14	RW	0x0	pd_cpu4_repair_sftena Enable memory repair for PD_CPU4 by software. 1'b0: Disable 1'b1: Enable
13	RW	0x0	pd_cpu5_repair_sftena Enable memory repair for PD_CPU5 by software. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pd_cpu6_repair_sftena Enable memory repair for PD_CPU6 by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pd_cpu7_repair_sftena Enable memory repair for PD_CPU7 by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	pd_bigcore_repair_sftena Enable memory repair for PD_BIGCORE by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pd_gpu_repair_sftena Enable memory repair for VD_GPU by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_npu1_repair_sftena Enable memory repair for PD_NPU1 by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_npu0_repair_sftena Enable memory repair for PD_NPU0 by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_nputop_repair_sftena Enable memory repair for PD_NPUTOP by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_vpu_repair_sftena Enable memory repair for PD_VPU by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_vdec_repair_sftena Enable memory repair for PD_VDEC by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_vepu1_repair_sftena Enable memory repair for PD_VEPU1 by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vepu0_repair_sftena Enable memory repair for PD_VEPU0 by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vi_repair_sftena Enable memory repair for PD_VI by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	pd_usb_repair_sftena Enable memory repair for PD_USB by software. 1'b0: Disable 1'b1: Enable

PMU_BISR_PDGEN_SFTCON2

Address: Operational Base(0x27360000) + offset (0x20528)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	pd_cpu0_repair_sftena Enable memory repair for PD_CPU0 by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_cpu1_repair_sftena Enable memory repair for PD_CPU1 by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_cpu2_repair_sftena Enable memory repair for PD_CPU2 by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_cpu3_repair_sftena Enable memory repair for PD_CPU3 by software. 1'b0: Disable 1'b1: Enable

PMU_BISR_PDGDONE_SFTCON0

Address: Operational Base(0x27360000) + offset (0x20530)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_pdgdone_sftena Configure PDGDone for PD_VO0 by software. 1'b0: Inactive 1'b1: Active
14	RW	0x0	pd_vo1_pdgdone_sftena Configure PDGDone for PD_VO1 by software. 1'b0: Inactive 1'b1: Active
13	RW	0x0	pd_vop_cluster_pdgdone_sftena Configure PDGDone for PD_VOP_CLUSTER by software. 1'b0: Inactive 1'b1: Active
12	RW	0x0	pd_vop_esmart_pdgdone_sftena Configure PDGDone for PD_VOP_ESMART by software. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
11	RW	0x0	pd_vop_pdgdone_sftena Configure PDGDone for PD_VOP by software. 1'b0: Inactive 1'b1: Active
10	RW	0x0	pd_subphp_pdgdone_sftena Configure PDGDone for PD_SUBPHP by software. 1'b0: Inactive 1'b1: Active
9	RW	0x0	pd_php_pdgdone_sftena Configure PDGDone for PD_PHP by software. 1'b0: Inactive 1'b1: Active
8	RW	0x0	pd_audio_pdgdone_sftena Configure PDGDone for PD_AUDIO by software. 1'b0: Inactive 1'b1: Active
7	RW	0x0	pd_sdgmac_pdgdone_sftena Configure PDGDone for PD_SDGMAC by software. 1'b0: Inactive 1'b1: Active
6	RW	0x0	pd_nvm_pdgdone_sftena Configure PDGDone for PD_NVM by software. 1'b0: Inactive 1'b1: Active
5	RW	0x0	pd_cci_pdgdone_sftena Configure PDGDone for PD_CCI by software. 1'b0: Inactive 1'b1: Active
4	RW	0x0	pd_ddr_pdgdone_sftena Configure PDGDone for VD_DDR by software. 1'b0: Inactive 1'b1: Active
3	RW	0x0	pd_center_pdgdone_sftena Configure PDGDone for PD_CENTER by software. 1'b0: Inactive 1'b1: Active
2	RW	0x0	pd_secure_pdgdone_sftena Configure PDGDone for PD_SECURE by software. 1'b0: Inactive 1'b1: Active
1	RW	0x0	pd_bus_pdgdone_sftena Configure PDGDone for PD_BUS by software. 1'b0: Inactive 1'b1: Active
0	RW	0x0	pd_pmu1_pdgdone_sftena Configure PDGDone for PD_PMU1 by software. 1'b0: Inactive 1'b1: Active

PMU_BISR_PDGDONE_SFTCON1

Address: Operational Base(0x27360000) + offset (0x20534)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_litcore_pdgdone_sftena Configure PDGDone for PD_LITCORE by software. 1'b0: Inactive 1'b1: Active
14	RW	0x0	pd_cpu4_pdgdone_sftena Configure PDGDone for PD_CPU4 by software. 1'b0: Inactive 1'b1: Active
13	RW	0x0	pd_cpu5_pdgdone_sftena Configure PDGDone for PD_CPU5 by software. 1'b0: Inactive 1'b1: Active
12	RW	0x0	pd_cpu6_pdgdone_sftena Configure PDGDone for PD_CPU6 by software. 1'b0: Inactive 1'b1: Active
11	RW	0x0	pd_cpu7_pdgdone_sftena Configure PDGDone for PD_CPU7 by software. 1'b0: Inactive 1'b1: Active
10	RW	0x0	pd_bigcore_pdgdone_sftena Configure PDGDone for PD_BIGCORE by software. 1'b0: Inactive 1'b1: Active
9	RW	0x0	pd_gpu_pdgdone_sftena Configure PDGDone for VD_GPU by software. 1'b0: Inactive 1'b1: Active
8	RW	0x0	pd_npu1_pdgdone_sftena Configure PDGDone for PD_NPU1 by software. 1'b0: Inactive 1'b1: Active
7	RW	0x0	pd_npu0_pdgdone_sftena Configure PDGDone for PD_NPU0 by software. 1'b0: Inactive 1'b1: Active
6	RW	0x0	pd_nputop_pdgdone_sftena Configure PDGDone for PD_NPUTOP by software. 1'b0: Inactive 1'b1: Active
5	RW	0x0	pd_vpu_pdgdone_sftena Configure PDGDone for PD_VPU by software. 1'b0: Inactive 1'b1: Active
4	RW	0x0	pd_vdec_pdgdone_sftena Configure PDGDone for PD_VDEC by software. 1'b0: Inactive 1'b1: Active
3	RW	0x0	pd_vepu1_pdgdone_sftena Configure PDGDone for PD_VEPU1 by software. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
2	RW	0x0	pd_vepu0_pdgdone_sftena Configure PDGDone for PD_VEPU0 by software. 1'b0: Inactive 1'b1: Active
1	RW	0x0	pd_vi_pdgdone_sftena Configure PDGDone for PD_VI by software. 1'b0: Inactive 1'b1: Active
0	RW	0x0	pd_usb_pdgdone_sftena Configure PDGDone for PD_USB by software. 1'b0: Inactive 1'b1: Active

PMU_BISR_PDGDONE_SFTCON2

Address: Operational Base(0x27360000) + offset (0x20538)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	pd_cpu0_pdgdone_sftena Configure PDGDone for PD_CPU0 by software. 1'b0: Inactive 1'b1: Active
2	RW	0x0	pd_cpu1_pdgdone_sftena Configure PDGDone for PD_CPU1 by software. 1'b0: Inactive 1'b1: Active
1	RW	0x0	pd_cpu2_pdgdone_sftena Configure PDGDone for PD_CPU2 by software. 1'b0: Inactive 1'b1: Active
0	RW	0x0	pd_cpu3_pdgdone_sftena Configure PDGDone for PD_CPU3 by software. 1'b0: Inactive 1'b1: Active

PMU_BISR_INITRST_SFTCON0

Address: Operational Base(0x27360000) + offset (0x20540)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_vo0_initrst_sftena Configure memory repair initial reset for PD_VO0 by software. 1'b0: Reset 1'b1: Normal
14	RW	0x0	pd_vo1_initrst_sftena Configure memory repair initial reset for PD_VO1 by software. 1'b0: Reset 1'b1: Normal

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Bit	Attr	Reset Value	Description
13	RW	0x0	pd_vop_cluster_initrst_sftena Configure memory repair initial reset for PD_VOP_CLUSTER by software. 1'b0: Reset 1'b1: Normal
12	RW	0x0	pd_vop_esmart_initrst_sftena Configure memory repair initial reset for PD_VOP_ESMART by software. 1'b0: Reset 1'b1: Normal
11	RW	0x0	pd_vop_initrst_sftena Configure memory repair initial reset for PD_VOP by software. 1'b0: Reset 1'b1: Normal
10	RW	0x0	pd_subphp_initrst_sftena Configure memory repair initial reset for PD_SUBPHP by software. 1'b0: Reset 1'b1: Normal
9	RW	0x0	pd_php_initrst_sftena Configure memory repair initial reset for PD_PHP by software. 1'b0: Reset 1'b1: Normal
8	RW	0x0	pd_audio_initrst_sftena Configure memory repair initial reset for PD_AUDIO by software. 1'b0: Reset 1'b1: Normal
7	RW	0x0	pd_sdgmac_initrst_sftena Configure memory repair initial reset for PD_SDGMAC by software. 1'b0: Reset 1'b1: Normal
6	RW	0x0	pd_nvm_initrst_sftena Configure memory repair initial reset for PD_NVM by software. 1'b0: Reset 1'b1: Normal
5	RW	0x0	pd_cci_initrst_sftena Configure memory repair initial reset for PD_CCI by software. 1'b0: Reset 1'b1: Normal
4	RW	0x0	pd_ddr_initrst_sftena Configure memory repair initial reset for VD_DDR by software. 1'b0: Reset 1'b1: Normal
3	RW	0x0	pd_center_initrst_sftena Configure memory repair initial reset for PD_CENTER by software. 1'b0: Reset 1'b1: Normal
2	RW	0x0	pd_secure_initrst_sftena Configure memory repair initial reset for PD_SECURE by software. 1'b0: Reset 1'b1: Normal
1	RW	0x0	pd_bus_initrst_sftena Configure memory repair initial reset for PD_BUS by software. 1'b0: Reset 1'b1: Normal

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Bit	Attr	Reset Value	Description
0	RW	0x0	pd_pmu1_initrst_sftena Configure memory repair initial reset for PD_PMU1 by software. 1'b0: Reset 1'b1: Normal

PMU_BISR_INITRST_SFTCON1

Address: Operational Base(0x27360000) + offset (0x20544)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_litcore_initrst_sftena Configure memory repair initial reset for PD_CPU4 by software. 1'b0: Reset 1'b1: Normal
14	RW	0x0	pd_cpu4_initrst_sftena Configure memory repair initial reset for PD_CPU3 by software. 1'b0: Reset 1'b1: Normal
13	RW	0x0	pd_cpu5_initrst_sftena Configure memory repair initial reset for PD_CPU2 by software. 1'b0: Reset 1'b1: Normal
12	RW	0x0	pd_cpu6_initrst_sftena Configure memory repair initial reset for PD_CPU1 by software. 1'b0: Reset 1'b1: Normal
11	RW	0x0	pd_cpu7_initrst_sftena Configure memory repair initial reset for PD_CPU0 by software. 1'b0: Reset 1'b1: Normal
10	RW	0x0	pd_bigcore_initrst_sftena Configure memory repair initial reset for PD_BIGCORE by software. 1'b0: Reset 1'b1: Normal
9	RW	0x0	pd_gpu_initrst_sftena Configure memory repair initial reset for VD_GPU by software. 1'b0: Reset 1'b1: Normal
8	RW	0x0	pd_npu1_initrst_sftena Configure memory repair initial reset for PD_NPU1 by software. 1'b0: Reset 1'b1: Normal
7	RW	0x0	pd_npu0_initrst_sftena Configure memory repair initial reset for PD_NPU0 by software. 1'b0: Reset 1'b1: Normal
6	RW	0x0	pd_nputop_initrst_sftena Configure memory repair initial reset for PD_NPUTOP by software. 1'b0: Reset 1'b1: Normal

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Bit	Attr	Reset Value	Description
5	RW	0x0	pd_vpu_initrst_sftena Configure memory repair initial reset for PD_VPU by software. 1'b0: Reset 1'b1: Normal
4	RW	0x0	pd_vdec_initrst_sftena Configure memory repair initial reset for PD_VDEC by software. 1'b0: Reset 1'b1: Normal
3	RW	0x0	pd_vepu1_initrst_sftena Configure memory repair initial reset for PD_VEPU1 by software. 1'b0: Reset 1'b1: Normal
2	RW	0x0	pd_vepu0_initrst_sftena Configure memory repair initial reset for PD_VEPU0 by software. 1'b0: Reset 1'b1: Normal
1	RW	0x0	pd_vi_initrst_sftena Configure memory repair initial reset for PD_VI by software. 1'b0: Reset 1'b1: Normal
0	RW	0x0	pd_usb_initrst_sftena Configure memory repair initial reset for PD_USB by software. 1'b0: Reset 1'b1: Normal

PMU_BISR_INITRST_SFTCON2

Address: Operational Base(0x27360000) + offset (0x20548)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	pd_cpu0_initrst_sftena Configure memory repair initial reset for PD_BIGCORE by software. 1'b0: Reset 1'b1: Normal
2	RW	0x0	pd_cpu1_initrst_sftena Configure memory repair initial reset for PD_CPU7 by software. 1'b0: Reset 1'b1: Normal
1	RW	0x0	pd_cpu2_initrst_sftena Configure memory repair initial reset for PD_CPU6 by software. 1'b0: Reset 1'b1: Normal
0	RW	0x0	pd_cpu3_initrst_sftena Configure memory repair initial reset for PD_CPU5 by software. 1'b0: Reset 1'b1: Normal

PMU_BISR_PDGDONE_STATUS0

Address: Operational Base(0x27360000) + offset (0x20550)

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Bit	Attr	Reset Value	Description
31	RO	0x0	pd_litcore_repair_pdgdone PDGDone status for PD_LITCORE repair. 1'b0: Repair not complete 1'b1: Repair complete
30	RO	0x0	pd_cpu4_repair_pdgdone PDGDone status for PD_CPU4 repair. 1'b0: Repair not complete 1'b1: Repair complete
29	RO	0x0	pd_cpu5_repair_pdgdone PDGDone status for PD_CPU5 repair. 1'b0: Repair not complete 1'b1: Repair complete
28	RO	0x0	pd_cpu6_repair_pdgdone PDGDone status for PD_CPU6 repair. 1'b0: Repair not complete 1'b1: Repair complete
27	RO	0x0	pd_cpu7_repair_pdgdone PDGDone status for PD_CPU7 repair. 1'b0: Repair not complete 1'b1: Repair complete
26	RO	0x0	pd_bigcore_repair_pdgdone PDGDone status for PD_BIGCORE repair. 1'b0: Repair not complete 1'b1: Repair complete
25	RO	0x0	pd_gpu_repair_pdgdone PDGDone status for VD_GPU repair. 1'b0: Repair not complete 1'b1: Repair complete
24	RO	0x0	pd_npu1_repair_pdgdone PDGDone status for PD_NPU1 repair. 1'b0: Repair not complete 1'b1: Repair complete
23	RO	0x0	pd_npu0_repair_pdgdone PDGDone status for PD_NPU0 repair. 1'b0: Repair not complete 1'b1: Repair complete
22	RO	0x0	pd_nputop_repair_pdgdone PDGDone status for PD_NPUTOP repair. 1'b0: Repair not complete 1'b1: Repair complete
21	RO	0x0	pd_vpu_repair_pdgdone PDGDone status for PD_VPU repair. 1'b0: Repair not complete 1'b1: Repair complete
20	RO	0x0	pd_vdec_repair_pdgdone PDGDone status for PD_VDEC repair. 1'b0: Repair not complete 1'b1: Repair complete
19	RO	0x0	pd_vepu1_repair_pdgdone PDGDone status for PD_VEPU1 repair. 1'b0: Repair not complete 1'b1: Repair complete
18	RO	0x0	pd_vepu0_repair_pdgdone PDGDone status for PD_VEPU0 repair. 1'b0: Repair not complete 1'b1: Repair complete

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Bit	Attr	Reset Value	Description
17	RO	0x0	pd_vi_repair_pdgdone PDGDone status for PD_VI repair. 1'b0: Repair not complete 1'b1: Repair complete
16	RO	0x0	pd_usb_repair_pdgdone PDGDone status for PD_USB repair. 1'b0: Repair not complete 1'b1: Repair complete
15	RO	0x0	pd_vo0_repair_pdgdone PDGDone status for PD_VO0 repair. 1'b0: Repair not complete 1'b1: Repair complete
14	RO	0x0	pd_vo1_repair_pdgdone PDGDone status for PD_VO1 repair. 1'b0: Repair not complete 1'b1: Repair complete
13	RO	0x0	pd_vop_cluster_repair_pdgdone PDGDone status for PD_VOP_CLUSTER repair. 1'b0: Repair not complete 1'b1: Repair complete
12	RO	0x0	pd_vop_esmart_repair_pdgdone PDGDone status for PD_VOP_ESMART repair. 1'b0: Repair not complete 1'b1: Repair complete
11	RO	0x0	pd_vop_repair_pdgdone PDGDone status for PD_VOP repair. 1'b0: Repair not complete 1'b1: Repair complete
10	RO	0x0	pd_subphp_repair_pdgdone PDGDone status for PD_SUBPHP repair. 1'b0: Repair not complete 1'b1: Repair complete
9	RO	0x0	pd_php_repair_pdgdone PDGDone status for PD_PHP repair. 1'b0: Repair not complete 1'b1: Repair complete
8	RO	0x0	pd_audio_repair_pdgdone PDGDone status for PD_AUDIO repair. 1'b0: Repair not complete 1'b1: Repair complete
7	RO	0x0	pd_sdgmac_repair_pdgdone PDGDone status for PD_SDGMAC repair. 1'b0: Repair not complete 1'b1: Repair complete
6	RO	0x0	pd_nvm_repair_pdgdone PDGDone status for PD_NVM repair. 1'b0: Repair not complete 1'b1: Repair complete
5	RO	0x0	pd_cci_repair_pdgdone PDGDone status for PD_CCI repair. 1'b0: Repair not complete 1'b1: Repair complete
4	RO	0x0	pd_ddr_repair_pdgdone PDGDone status for VD_DDR repair. 1'b0: Repair not complete 1'b1: Repair complete

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Bit	Attr	Reset Value	Description
3	RO	0x0	pd_center_repair_pdgdone PDGDone status for PD_CENTER repair. 1'b0: Repair not complete 1'b1: Repair complete
2	RO	0x0	pd_secure_repair_pdgdone PDGDone status for PD_SECURE repair. 1'b0: Repair not complete 1'b1: Repair complete
1	RO	0x0	pd_bus_repair_pdgdone PDGDone status for PD_BUS repair. 1'b0: Repair not complete 1'b1: Repair complete
0	RO	0x0	pd_pmu1_repair_pdgdone PDGDone status for PD_PMU1 repair. 1'b0: Repair not complete 1'b1: Repair complete

PMU_BISR_PDGDONE_STATUS1

Address: Operational Base(0x27360000) + offset (0x20554)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	pd_cpu0_repair_pdgdone PDGDone status for PD_CPU0 repair. 1'b0: Repair not complete 1'b1: Repair complete
2	RO	0x0	pd_cpu1_repair_pdgdone PDGDone status for PD_CPU1 repair. 1'b0: Repair not complete 1'b1: Repair complete
1	RO	0x0	pd_cpu2_repair_pdgdone PDGDone status for PD_CPU2 repair. 1'b0: Repair not complete 1'b1: Repair complete
0	RO	0x0	pd_cpu3_repair_pdgdone PDGDone status for PD_CPU3 repair. 1'b0: Repair not complete 1'b1: Repair complete

PMU_BISR_PDGCEDIS_STATUS0

Address: Operational Base(0x27360000) + offset (0x20560)

Bit	Attr	Reset Value	Description
31	RO	0x0	pd_litcore_repair_pdgcedis PDGCedis status for PD_LITCORE repair. 1'b0: Repair ready 1'b1: Repair busy
30	RO	0x0	pd_cpu4_repair_pdgcedis PDGCedis status for PD_CPU4 repair. 1'b0: Repair ready 1'b1: Repair busy
29	RO	0x0	pd_cpu5_repair_pdgcedis PDGCedis status for PD_CPU5 repair. 1'b0: Repair ready 1'b1: Repair busy

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Bit	Attr	Reset Value	Description
28	RO	0x0	pd_cpu6_repair_pdgcedis PDGCedis status for PD_CPU6 repair. 1'b0: Repair ready 1'b1: Repair busy
27	RO	0x0	pd_cpu7_repair_pdgcedis PDGCedis status for PD_CPU7 repair. 1'b0: Repair ready 1'b1: Repair busy
26	RO	0x0	pd_bigcore_repair_pdgcedis PDGCedis status for PD_BIGCORE repair. 1'b0: Repair ready 1'b1: Repair busy
25	RO	0x0	pd_gpu_repair_pdgcedis PDGCedis status for VD_GPU repair. 1'b0: Repair ready 1'b1: Repair busy
24	RO	0x0	pd_npu1_repair_pdgcedis PDGCedis status for PD_NPU1 repair. 1'b0: Repair ready 1'b1: Repair busy
23	RO	0x0	pd_npu0_repair_pdgcedis PDGCedis status for PD_NPU0 repair. 1'b0: Repair ready 1'b1: Repair busy
22	RO	0x0	pd_nputop_repair_pdgcedis PDGCedis status for PD_NPUTOP repair. 1'b0: Repair ready 1'b1: Repair busy
21	RO	0x0	pd_vpu_repair_pdgcedis PDGCedis status for PD_VPU repair. 1'b0: Repair ready 1'b1: Repair busy
20	RO	0x0	pd_vdec_repair_pdgcedis PDGCedis status for PD_VDEC repair. 1'b0: Repair ready 1'b1: Repair busy
19	RO	0x0	pd_vepu1_repair_pdgcedis PDGCedis status for PD_VEPU1 repair. 1'b0: Repair ready 1'b1: Repair busy
18	RO	0x0	pd_vepu0_repair_pdgcedis PDGCedis status for PD_VEPU0 repair. 1'b0: Repair ready 1'b1: Repair busy
17	RO	0x0	pd_vi_repair_pdgcedis PDGCedis status for PD_VI repair. 1'b0: Repair ready 1'b1: Repair busy
16	RO	0x0	pd_usb_repair_pdgcedis PDGCedis status for PD_USB repair. 1'b0: Repair ready 1'b1: Repair busy
15	RO	0x0	pd_vo0_repair_pdgcedis PDGCedis status for PD_VO0 repair. 1'b0: Repair ready 1'b1: Repair busy

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Bit	Attr	Reset Value	Description
14	RO	0x0	pd_vo1_repair_pdgcedis PDGCedis status for PD_VO1 repair. 1'b0: Repair ready 1'b1: Repair busy
13	RO	0x0	pd_vop_cluster_repair_pdgcedis PDGCedis status for PD_VOP_CLUSTER repair. 1'b0: Repair ready 1'b1: Repair busy
12	RO	0x0	pd_vop_esmart_repair_pdgcedis PDGCedis status for PD_VOP_ESMART repair. 1'b0: Repair ready 1'b1: Repair busy
11	RO	0x0	pd_vop_repair_pdgcedis PDGCedis status for PD_VOP repair. 1'b0: Repair ready 1'b1: Repair busy
10	RO	0x0	pd_subphp_repair_pdgcedis PDGCedis status for PD_SUBPHP repair. 1'b0: Repair ready 1'b1: Repair busy
9	RO	0x0	pd_php_repair_pdgcedis PDGCedis status for PD_PHP repair. 1'b0: Repair ready 1'b1: Repair busy
8	RO	0x0	pd_audio_repair_pdgcedis PDGCedis status for PD_AUDIO repair. 1'b0: Repair ready 1'b1: Repair busy
7	RO	0x0	pd_sdgmac_repair_pdgcedis PDGCedis status for PD_SDGMAC repair. 1'b0: Repair ready 1'b1: Repair busy
6	RO	0x0	pd_nvm_repair_pdgcedis PDGCedis status for PD_NVM repair. 1'b0: Repair ready 1'b1: Repair busy
5	RO	0x0	pd_cci_repair_pdgcedis PDGCedis status for PD_CCI repair. 1'b0: Repair ready 1'b1: Repair busy
4	RO	0x0	pd_ddr_repair_pdgcedis PDGCedis status for VD_DDR repair. 1'b0: Repair ready 1'b1: Repair busy
3	RO	0x0	pd_center_repair_pdgcedis PDGCedis status for PD_CENTER repair. 1'b0: Repair ready 1'b1: Repair busy
2	RO	0x0	pd_secure_repair_pdgcedis PDGCedis status for PD_SECURE repair. 1'b0: Repair ready 1'b1: Repair busy
1	RO	0x0	pd_bus_repair_pdgcedis PDGCedis status for PD_BUS repair. 1'b0: Repair ready 1'b1: Repair busy

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Bit	Attr	Reset Value	Description
0	RO	0x0	pd_pmu1_repair_pdgcedis PDGCedis status for PD_PMU1 repair. 1'b0: Repair ready 1'b1: Repair busy

PMU_BISR_PDGCEDIS_STATUS1

Address: Operational Base(0x27360000) + offset (0x20564)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	pd_cpu0_repair_pdgcedis PDGCedis status for PD_CPU0 repair. 1'b0: Repair ready 1'b1: Repair busy
2	RO	0x0	pd_cpu1_repair_pdgcedis PDGCedis status for PD_CPU1 repair. 1'b0: Repair ready 1'b1: Repair busy
1	RO	0x0	pd_cpu2_repair_pdgcedis PDGCedis status for PD_CPU2 repair. 1'b0: Repair ready 1'b1: Repair busy
0	RO	0x0	pd_cpu3_repair_pdgcedis PDGCedis status for PD_CPU3 repair. 1'b0: Repair ready 1'b1: Repair busy

PMU_BISR_PWR_REPAIR_STATUS0

Address: Operational Base(0x27360000) + offset (0x20570)

Bit	Attr	Reset Value	Description
31	RO	0x0	pd_litcore_pwr_repair_stat Power and repair status for PD_LITCORE. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
30	RO	0x0	pd_cpu4_pwr_repair_stat Power and repair status for PD_CPU4. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
29	RO	0x0	pd_cpu5_pwr_repair_stat Power and repair status for PD_CPU5. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
28	RO	0x0	pd_cpu6_pwr_repair_stat Power and repair status for PD_CPU6. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
27	RO	0x0	pd_cpu7_pwr_repair_stat Power and repair status for PD_CPU7. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
26	RO	0x0	pd_bigcore_pwr_repair_stat Power and repair status for PD_BIGCORE. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete

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Bit	Attr	Reset Value	Description
25	RO	0x0	pd_gpu_pwr_repair_stat Power and repair status for VD_GPU. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
24	RO	0x0	pd_npu1_pwr_repair_stat Power and repair status for PD_NPU1. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
23	RO	0x0	pd_npu0_pwr_repair_stat Power and repair status for PD_NPU0. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
22	RO	0x0	pd_nputop_pwr_repair_stat Power and repair status for PD_NPUTOP. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
21	RO	0x0	pd_vpu_pwr_repair_stat Power and repair status for PD_VPU. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
20	RO	0x0	pd_vdec_pwr_repair_stat Power and repair status for PD_VDEC. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
19	RO	0x0	pd_vepu1_pwr_repair_stat Power and repair status for PD_VEPU1. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
18	RO	0x0	pd_vepu0_pwr_repair_stat Power and repair status for PD_VEPU0. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
17	RO	0x0	pd_vi_pwr_repair_stat Power and repair status for PD_VI. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
16	RO	0x0	pd_usb_pwr_repair_stat Power and repair status for PD_USB. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
15	RO	0x0	pd_vo0_pwr_repair_stat Power and repair status for PD_VO0. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
14	RO	0x0	pd_vo1_pwr_repair_stat Power and repair status for PD_VO1. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
13	RO	0x0	pd_vop_cluster_pwr_repair_stat Power and repair status for PD_VOP_CLUSTER. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
12	RO	0x0	pd_vop_esmart_pwr_repair_stat Power and repair status for PD_VOP_ESMART. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete

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Bit	Attr	Reset Value	Description
11	RO	0x0	pd_vop_pwr_repair_stat Power and repair status for PD_VOP. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
10	RO	0x0	pd_subphp_pwr_repair_stat Power and repair status for PD_SUBPHP. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
9	RO	0x0	pd_php_pwr_repair_stat Power and repair status for PD_PHP. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
8	RO	0x0	pd_audio_pwr_repair_stat Power and repair status for PD_AUDIO. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
7	RO	0x0	pd_sdgmac_pwr_repair_stat Power and repair status for PD_SDGMAC. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
6	RO	0x0	pd_nvm_pwr_repair_stat Power and repair status for PD_NVM. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
5	RO	0x0	pd_cci_pwr_repair_stat Power and repair status for PD_CCI. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
4	RO	0x0	pd_ddr_pwr_repair_stat Power and repair status for VD_DDR. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
3	RO	0x0	pd_center_pwr_repair_stat Power and repair status for PD_CENTER. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
2	RO	0x0	pd_secure_pwr_repair_stat Power and repair status for PD_SECURE. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
1	RO	0x0	pd_bus_pwr_repair_stat Power and repair status for PD_BUS. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
0	RO	0x0	pd_pmu1_pwr_repair_stat Power and repair status for PD_PMU1. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete

PMU_BISR_PWR_REPAIR_STATUS1

Address: Operational Base(0x27360000) + offset (0x20574)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3	RO	0x0	pd_cpu0_pwr_repair_stat Power and repair status for PD_CPU0. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
2	RO	0x0	pd_cpu1_pwr_repair_stat Power and repair status for PD_CPU1. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
1	RO	0x0	pd_cpu2_pwr_repair_stat Power and repair status for PD_CPU2. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete
0	RO	0x0	pd_cpu3_pwr_repair_stat Power and repair status for PD_CPU3. 1'b0: Power down or repair not complete 1'b1: Power up and repair complete

PMU_BISR_GLB_STATUS

Address: Operational Base(0x27360000) + offset (0x20580)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	bisr_done_timeout Memory repair group done or global done timeout state. 1'b0: Repair group done and global done are normal 1'b1: Repair group done or global done is timeout
6	RO	0x0	bisr_go Memory repair success state. 1'b0: Repair is not successful 1'b1: Repair is successful
5	RO	0x0	bisr_done Memory repair global done state. 1'b0: One or more groups' repair not complete 1'b1: All groups' repair complete
4	RO	0x0	reserved
3:0	RO	0x0	bisr_intf_state BISR interface state. 4'h0: Idle state 4'h1: Begin state 4'h2: Send repair group enable state 4'h3: Send repair start signal state 4'h4: Wait repair group done state 4'h5: Wait repair global done state 4'h6: Clear repair group enable state 4'h7: Start next new repair state 4'h7: End state Others: Reserved

6.5 Application Notes

6.5.1 Hardware Low Power Mode

PMU can work in power mode 1 by setting bit[0] in PMU_PWR_CON1 register. After setting this bit and all CPUs enter STANDBYWFI state, PMU power mode 1 FSM will start to run. In this low power mode, PMU will manage power resources by hardware or software, such as send idle request or resume transfer to specified BIU interface, power down or power up the specified power domain, DDR enters or exits retention mode, shut down or power up

PLL, disable or enable oscillator, and so on. All of above are configurable by setting corresponding registers.
PMU can work in power mode 0 by setting bit[0] in PMU_PWR_CON0 register. After setting this bit and PMU enters power mode 1, PMU power mode 0 FSM will start to run. In this low power mode, PMU will manage PD_PMU1 power resource and idle request, manage DDR retention mode, VCCIO retention mode, disable oscillator, etc. All of above are configurable by setting corresponding registers.
There are similar control bits for bit[0]/[1]/[2]/[3]/[9] in PMU_CRU_PWR_CON0 and bit[5]/[6]/[7]/[14] in PMU_PWR_CON0. If chip is planned to enter power mode 0, these bits in PMU_CRU_PWR_CON are not need to configure since those low power flow are controlled by PMU_PWR_CON0.

6.5.2 Software Low Power Mode

PMU can work in the low power mode by software. In this application, you can use MCU such as PMU_MCU to set PMU software power control registers to execute low power procedure.

6.5.3 Power Domain Dependence Relationship

There exists power dependence between some power domains. Level 0 Power Domain has higher power prior than Level 1 Power Domain. Level 0 Power Domain should be power up before Level 1 Power Domain; and Level 1 Power Domain should be power down before Level 0 Power Domain. Incorrect operation may cause power leakage.
There exists bus dependence between some power domains, include virtual power domain. The bus of Level 0 Power Domain should be active when Level 1 Power Domain accesses external slave or Level 1 Power Domain is accessed. Incorrect operation may cause system access error.
If any master access PD_DDR or CPU access any slave outside of VD_LITCORE, PD_CENTER should power on and its bus should be active.
The relationship is shown in follow table.

Table 6-2 Relationship Between Power Domains

Level 1 Power Domain	Level 0 Power Domain	Power Dependence	Bus Dependence
PD_SDGMAC	PD_NVM	×	√
PD_NVM	PD_SECURE(Virtual)	×	√
PD_VPU	PD_SECURE(Virtual)	×	√
PD_SUBPHP	PD_PHP	√	√
PD_VEPU0	PD_VI	√	√
VD_GPU	PD_CENTER	√	√
PD_VOP	PD_CENTER	√	√
PD_USB	PD_VOP	√	√
PD_VO0	PD_VOP	×	√
PD_VO1	PD_VOP	√	√
PD_VOP_ESMART	PD_VOP	√	√
PD_VOP_CLUSTER	PD_VOP	√	√
PD_NPU0	PD_NPUTOP	√	√
PD_NPU1	PD_NPUTOP	√	√

There also have nested voltage domains in RK3576: VD_BIGCORE and VD_LITCORE. VD_LITCORE should power on before VD_BIGCORE power on. VD_BIGCORE should power off before VD_LITCORE power off.

6.5.4 Virtual Power Domain

There are some virtual power domains in RK3576: PD_CCI, PD_BUS, PD_SECURE. These virtual power domains have similar operation with real power domains, except they don’t care the power status.

6.5.5 Bus Interface Unit(BIU) Idle/Active Operation

BIU is used as the bridge between masters and slaves. There may be one or more BIUs in every power domain. If you want to gate bus clock or power down the power domain, the domain’s BIU should be idle firstly. After the block power up, the BIU should be active before access.

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The corresponding relationship between BIU and power domain is described in "3.3.2 Domain Description" section.
The BIU idle/active operation can be done by hardware automatically or by software flexibly.

6.5.5.1 BIU idle/active operation by hardware

(1) Send BIU idle request by setting the corresponding bit to 1 in PMU_IDLE_CON0/1 register;
(2) Set PMU_PWR_CON_P1[4] to 1; set PMU_PWR_CON_P1[0] to 1;
(3) Query PMU_GLB_POWER_STS register to wait for the system enters sleep state. BIU is idle now;
(4) If wakeup source is valid, the system is wakeup;
(5) Query PMU_GLB_POWER_STS register to wait for the system enters normal state; BIU is active now.

6.5.5.2 BIU idle/active operation by software

BIU idle operation by software:

(1) Send BIU idle request by setting the corresponding bit to 1 in PMU_IDLE_SFTCON0/1 register;
(2) Query PMU_IDLE_ACK_STS register to wait for the corresponding BIU idle acknowledge state; Query PMU_IDLE_STS register to wait for the corresponding BIU in idle state.

BIU active operation by software:

(1) Send BIU active request by setting the corresponding bit to 0 in PMU_IDLE_SFTCON0/1 register;
(2) Query PMU_IDLE_ACK_STS register to wait for the corresponding BIU active acknowledge state; Query PMU_IDLE_STS register to wait for the corresponding BIU in active state.

6.5.6 Power Domain(PD) Power Up/Down Operation

There are multi power domains in RK3576. Each power domain can be power down to reduce chip power when it is idle, and re-power up if needed.
The power up/down operation sequence can be executed by hardware automatically or by software flexibly.

6.5.6.1 PD power down/up operation by hardware

(1) Send BIU idle request if BIU interface exists in specific power domain that you want to power down by setting the corresponding bit to 1 in PMU_IDLE_CON0/1 register. If BIU interface does not exist, skip this step;
(2) Enable power gate to the specific power domain by setting corresponding bit to 1 in PMU_PWR_GATE_CON0/1 register;
(3) Set PMU_PWR_CON_P1[4] to 1if BIU idle operation needed; set PMU_PWR_CON_P1[6] to 1; set PMU_PWR_CON_P1[0] to 1;
(4) Query PMU_GLB_POWER_STS register to wait for the system enters sleep state. Now BIU is idle and PD is power down.
(5) If wakeup source is valid, the system is wakeup;
(6) Query PMU_GLB_POWER_STS register to wait for the system enters normal state; PD is power up and BIU is active now.

6.5.6.2 PD power down/up operation by software

1. PD power down operation by software

(1) Do BIU idle operation by software if BIU interface exists in specific power domain that you want to power down; If BIU interface does not exist, skip this step;
(2) Enable power down to the specific power domain by setting corresponding bit to 1 in PMU_PWR_GATE_SFTCON0/1 register;
(3) Query PMU_PWR_GATE_STS register to wait for the specific power domain power down;

2. PD power up operation by software

(1) Enable power up to the specific power domain by setting corresponding bit to 0 in PMU_PWR_GATE_SFTCON0/1 register;
(2) Query PMU_PWR_GATE_STS register to wait for the specific power domain power up;
(3) Do BIU active operation by software if BIU interface exists in specific power domain that you want to power down; If BIU interface does not exist, skip this step.

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6.5.7 Voltage Domain(VD) Power On/Off Operation Sequence

There are multi voltage domains in RK3576. Each voltage domain can power off to reduce chip power when it is idle, and re-power on if needed.

Power off request is generated independently during power off/on operation for VD_DDR/VD_GPU/VD_NPU/VD_BIGCORE/VD_LITCORE, etc. The power off request can be selected as the power sleep source by configuring PMU0_GRF_SOC_CON1, and output to IO to control the external power manage unit.

6.5.7.1 VD_DDR power off/on operation

1. VD_DDR power off operation

Set PMU_VOL_GATE_CON0[4] to 1; Set PMU_PWR_GATE_CON0[4] to 1 and execute hardware power down operation, or set PMU_PWR_GATE_SFTCON0[4] to 1 and execute software power down operation. After operation, VD_DDR power off request is high and it can power off.

2. VD_DDR power on operation

Set PMU_PWR_GATE_SFTCON0[4] to 0, execute software power up operation; or execute hardware power up operation. After operation, VD_DDR power on request is high and it should power on. The hardware should make sure the VD_DDR's power is stable before VD_DDR power on.

6.5.7.2 VD_GPU power off/on operation

1. VD_GPU power off operation

Set PMU_VOL_GATE_CON1[9] to 1; Set PMU_PWR_GATE_CON1[9] to 1 and execute hardware power down operation, or set PMU_PWR_GATE_SFTCON1[9] to 1 and execute software power down operation. After operation, VD_GPU power off request is high and it can power off. If PMU_VOL_GATE_FAST_CON[2]=1, VD_GPU will power off completely after PMU_GPU_PWRDN_CNT time.

2. VD_GPU power on operation

Set PMU_PWR_GATE_SFTCON1[9] to 0 and execute software power up operation, or execute hardware power up operation. After operation, VD_GPU power on request is high and it should power on. If PMU_VOL_GATE_FAST_CON[2]=1, VD_GPU will power on completely after PMU_GPU_PWRUP_CNT time; otherwise, hardware should make sure the VD_GPU's power is stable before VD_GPU power on.

6.5.7.3 VD_NPU power off/on operation

6.5.7.3.1 VD_NPU power off/on operation by hardware

Set PMU_VOL_GATE_CON0[0] to 1; Set PMU_PWR_GATE_CON0[0] and PMU_PWR_GATE_CON1[6/7/8] to 1, and execute hardware power down operation. After system enter sleep state, PD_NPU0/PD_NPU1/PD_NPUTOP power down, VD_NPU power off request is high and it can power off. If PMU_VOL_GATE_FAST_CON[0]=1, VD_NPU will power off completely after PMU_NPU_PWRDN_CNT time.

If wakeup source is valid, the system is wakeup. Query PMU_GLB_POWER_STS register to wait for the system enters normal state. Then PD_NPU0/PD_NPU1/PD_NPUTOP can power up automatically if needed.

6.5.7.3.2 VD_NPU power off/on operation by software

1. VD_NPU power off operation by software

Firstly, power down PD_NPU0/PD_NPU1/PD_NPUTOP in turn. Then set PMU_VOL_GATE_CON0[0] to 1; Set PMU_PWR_GATE_CON0[0] to 1 and execute hardware power down operation, or set PMU_PWR_GATE_SFTCON0[0] to 1 and execute software power down operation. After operation, VD_NPU power off request is high and it can power off. If PMU_VOL_GATE_FAST_CON[0]=1, VD_NPU will power off completely after PMU_NPU_PWRDN_CNT time.

2. VD_NPU power on operation by software

Set PMU_VOL_GATE_CON0[0] to 0; Set PMU_PWR_GATE_CON0[0] to 0 and execute hardware power up operation, or set PMU_PWR_GATE_SFTCON0[0] to 0 and execute software power up operation. After operation, VD_NPU power on request is high and it should power on. If PMU_VOL_GATE_FAST_CON[0]=1, VD_NPU will power on completely after PMU_NPU_PWRUP_CNT time; otherwise, hardware should make sure the VD_NPU's power is stable before VD_NPU power on. Then you can power up PD_NPU0/PD_NPU1/PD_NPUTOP in proper order.

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6.5.7.4 VD_BIGCORE power off/on operation

6.5.7.4.1 VD_BIGCORE power off/on operation by hardware

(1) Set PMU_PWR_C0_ACK_SEL_CON0/ PMU_PWR_C1_ACK_SEL_CON0/ PMU_PWR_MEM_ACK_SEL_CON0 bit 8 to 1;
(2) Set PMU_CLUSTER1_IDLE_CON bit 0/1 to 1;
(3) Set PMU_CORE1_PWR_CON bit 0/1/2/3/5/10 to 1;
(4) Set PMU_CORE1_AUTO_PWR_CON[0] to 1. The system will power down PD_CPU/4/5/6/7 and PD_BIGCORE automatically, and generate VD_BIGCORE power off request;
(5) Set PMU_CORE1_AUTO_PWR_CON[2] to 1. If wakeup source is valid, the system will re-power on VD_BIGCORE and power up PD_CPU/4/5/6/7 and PD_BIGCORE automatically.

6.5.7.4.2 VD_BIGCORE power off/on operation by software

1. VD_BIGCORE power off operation by software

(1) Set PMU_CPU4/5/6/7_PWR_SFTCON[0] to 1, power down PD_CPU4~7;
(2) Set PMU_SCU1_PWR_SFTCON[0] to 1, flush L2, and wait for L2 enter STANDBYWFI state;
(3) Set PMU_CLUSTER1_IDLE_SFTCON[1] to 1, idle BIU_BIGCORE;
(4) Set PMU_CLUSTER1_IDLE_SFTCON[0] to 1, idle ADB1;
(5) Set PMU_SCU1_PWR_SFTCON[2] to 1, power down PD_BIGCORE;
(6) Set PMU_CORE1_PWR_CON[10] to 1, clamp VD_BIGCORE output;
(7) Set PMU_SCU1_PWR_SFTCON[3] to 1. VD_BIGCORE power off request is high and it can power off.

2. VD_BIGCORE power on operation by software

(1) Set PMU_SCU1_PWR_SFTCON[3] to 0. VD_BIGCORE power on request is high and it can power on.
(2) Set PMU_CORE1_PWR_CON[10] to 0, release VD_BIGCORE output;
(3) Set PMU_SCU1_PWR_SFTCON[2] to 0, power up PD_BIGCORE;
(4) Set PMU_CLUSTER1_IDLE_SDTCON[0] to 0, active ADB1
(5) Set PMU_CLUSTER1_IDLE_SDTCON[1] to 0, active BIU_BIGCORE
(6) Set PMU_SCU1_PWR_SFTCON[0] to 0;
(7) Set PMU_CPU4/5/6/7_PWR_SFTCON[0] to 0, power up PD_CPU4~7.

6.5.7.5 VD_LITCORE power off/on operation

1. VD_LITCORE power off operation

(1) Power down PD_LITCORE, similar to VD_BIGCORE power off operation;
(2) Set PMU_VOL_GATE_CON0[5] to 1; Set PMU_PWR_GATE_CON0[5] to 1 and execute hardware power down operation, or set PMU_PWR_GATE_SFTCON0[] to 1 and execute software power down operation. After operation, VD_LITCORE power off request is high and it can power off. If PMU_VOL_GATE_FAST_CON[1]=1, VD_LITCORE will power off completely after PMU_LITCORE_PWRDN_CNT time.

2. VD_LITCORE power on operation

Set PMU_PWR_GATE_SFTCON0[5] to 0 and execute software power up operation, or execute hardware power up operation. After operation, VD_LITCORE power on request is high and it should power on. If PMU_VOL_GATE_FAST_CON[1]=1, VD_LITCORE will power on completely after PMU_LITCORE_PWRUP_CNT time; otherwise, hardware should make sure the VD_LITCORE's power is stable before VD_LITCORE power on.
After VD_LITCORE power on, PD_LITCORE, PD_CPU0/1/2/3 can power up, similar to VD_BIGCORE power on operation.

6.5.7.6 VD_PPLL power off/on operation

The VD_PPLL can power off by software if it is not used.

1. VD_PPLL power off operation

(1) Set PMU0_GRF_SOC_CON5[6] to 1;
(2) Power off VD_PPLL.

2. VD_PPLL power on operation

(1) Power on VD_PPLL;
(2) Set PMU0_GRF_SOC_CON5[6] to 0.

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6.5.7.7 VD_MPHY power off/on operation

The VD_MPHY can power off by software if it is not used.

1. VD_MPHY power off operation

(1) Set MPHY_GRF_CON0[15] to 1;

(2) Power off VD_MPHY.

2. VD_MPHY power on operation

(1) Power on VD_MPHY;

(2) Set MPHY_GRF_CON0[15] to 0.

6.5.7.8 VD_DCPHY power off/on operation

The VD_DCPHY can power off by software if it is not used.

1. VD_DCPHY power off operation

(1) Set DCPHY_GRF_CON0[15] to 1;

(2) Power off VD_DCPHY.

2. VD_DCPHY power on operation

(1) Power on VD_DCPHY;

(2) Set DCPHY_GRF_CON0[15] to 0.

6.5.7.9 VD_HDPTXPHY power off/on operation

The VD_HDPTXPHY can power off by software if it is not used.

1. VD_HDPTXPHY power off operation

(1) Set HDPTXPHY_GRF_CON0[12] to 1;

(2) Power off VD_HDPTXPHY.

2. VD_HDPTXPHY power on operation

(1) Power on VD_HDPTXPHY;

(2) Set HDPTXPHY_GRF_CON0[12] to 0.

6.5.7.10 VD_USBDPHY power off/on operation

The VD_USBDPPHY can power off by software if it is not used.

1. VD_USBDPPHY power off operation

(1) Set USBDPPHY_GRF_CON2[15] to 1;

(2) Power off VD_USBDPPHY.

2. VD_USBDPPHY power on operation

(1) Power on VD_USBDPPHY;

(2) Set USBDPPHY_GRF_CON2[15] to 0.

6.5.7.11 VD_USBPHY power off/on operation

VD_USBPHY may have various power supply scheme for various application.

6.5.7.11.1 VD_USBPHY power supplied with VDD_LOGIC

VD_USBPHY's power supply is VDD_LOGIC. VD_USBPHY is always on if VDD_LOGIC is on. System can be wakeup by USB2PHY_0 or USB2PHY_1 if VDD_LOGIC is on.

If you prepare to power off VDD_LOGIC, PMU0_GRF_SOC_CON5[0] and PMU0_GRF_SOC_CON5[3] need set to 1, USB2PHY_0 and USB2PHY_1's interfaces output to VD_PMU are clamped automatically when VDD_LOGIC is off. Otherwise, it may cause power leakage.

6.5.7.11.2 VD_USBPHY power supplied with VDD_PMU

VD_USBPHY's power supply is VDD_PMU. VD_USBPHY is always on if VDD_PMU is on. System can be wakeup by USB2PHY_0 or USB2PHY_1 if VDD_LOGIC is off.

If you prepare to power off VDD_LOGIC, PMU0_GRF_SOC_CON5[1] and PMU0_GRF_SOC_CON5[4] need set to 1, the input interfaces of USB2PHY_0 and USB2PHY_1 are clamped automatically when VDD_LOGIC is off. Otherwise, it may lead to fail for USB wakeup flow; also, it may cause power leakage.

6.5.7.11.3 VD_USBPHY power supplied with individual power

VD_USBPHY's power supply is neither VDD_PMU nor VDD_LOGIC, but a individual power. VD_USBPHY can power off by software if it is not used. System can be wakeup by USB2PHY_0 or USB2PHY_1 if VD_USBPHY power on.

If you prepare to power off VD_USBPHY, PMU0_GRF_SOC_CON5[2] and PMU0_GRF_SOC_CON5[5] need set to 1, and USB2PHY_0 and USB2PHY_1's output interfaces are clamped immediately. Otherwise, it may cause system exception and power leakage.

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6.5.8 Memory Repair Operation

6.5.8.1 Memory Repair State

RK3576 supports memory repair for fault memory. SYS_GRF_MEMFAULT_STATUS0/1 stores the fault flags. If power domain (include virtual domain) has fault memory, the corresponding fault flag is 1. It means this power domain should be repaired after power up and before used.

During repair, you can query SYS_GRF_SOC_CON8[4:0] to get the detail repair information. Also, you can query PMU_BISR_GLB_STATUS[3:0] to get the global repair information.

K3576 support hardware repair and software repair.

6.5.8.2 Hardware Repair Operation

If the power domain's memory fault flag is 1, you can set hardware repair enable bit is 1. In this case, the power domain will automatically execute memory repair after power up. The flow is described as bellow.

(1) Set corresponding repair enable bit to 1 in PMU_BISR_PDGEN_CON0/1/2;
(2) Execute power up operation;
(3) Query PMU_BISR_PWR_REPAIR_STATUS0/1 register to wait for the specific power domain power up and repair done; also, if there are multi memory groups need repair, you can queue PMU_BISR_GLB_STATUS[4] to wait for all groups' repair done, and then queue PMU_BISR_GLB_STATUS[5] to check whether repair is successful or not.
(4) After repair operation, the power domain can start work normally.

6.5.8.3 Software Repair Operation

If the power domain's memory fault flag is 1, you also can set software repair enable bit is 1, in this case, the power domain can execute memory repair at any time you want. The flow is described as bellow.

(1) Set PMU_BISR_PDGEN_SFTCON0 /1/2 all bits to 0, set BISR_INITRST_SFTCON0/1/2 all bits to 1. Disable repair clock by set PMU_BISR_GLB_CON[6] to 1, and make sure no any block is repairing.
(2) Set PMU_BISR_GLB_CON [10] to 1, select software repair mode;
(3) Execute power up operation;
(4) Enable software repair clock by set PMU_BISR_GLB_CON[6] to 0;
(5) Enable software repair to the specific power domain by setting corresponding bit to 1 in PMU_BISR_PDGEN_SFTCON0 /1/2 register;
(6) Set PMU_BISR_GLB_CON[9] to 1 to initial repair global reset signal high; then set PMU_BISR_GLB_CON[9] to 0 to set repair global reset signal low; then set PMU_BISR_GLB_CON[9] to 1 to set repair global reset signal high;
(7) Query BISR_PDGDONE_STATUS0/1 register to wait for the specific power domain repair done. Also, you can queue PMU_BISR_GLB_STATUS[4] to wait for all groups' repair done, then queue PMU_BISR_GLB_STATUS[5] to check whether repair is successful or not.

6.5.9 Power Management IO Usage

There are independent power supplies for different voltage domain. You can communicate with external PMIC (Power Management Integrated Circuits) through I2C interface, or through IO interface.

There are multi IOs designed for purpose, corresponding Module Pin names are pwr0_sleep~pwr2_sleep. Each pwr_sleep has multi power off request source and you can only choose one source at a time. Detail refers to PMU0_GRF_SOC_CON1.

Each pwr_sleep has two polarities: high active or low active. You can choose the polarity through PMU0_GRF_SOC_CON0[9:7].

The IO interface configuration is as below.

Table 6-3 Power Management IO Interface

Module Pin	Direction	Pin Name	IOMUX Setting
pwr_sleep_0	O	PWR_CTRL1/TSADC_CTRL_M1/GPIO0_A3_d	PMUIO0_IOC_GPIO0A_IOMUX_SEL_L[15:12]=4'h9
pwr_sleep_1	O	PWR_CTRL2/GPIO0_A4_d	PMUIO0_IOC_GPIO0A_IOMUX_SEL_H[3:0]

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Module Pin	Direction	Pin Name	IOMUX Setting
			=4'h9
pwr_sleep_2	O	PWR_CTRL3/I2C6_SDA_M0/ GPIO0_A5_d	PMUIO0_IOC_ GPIO0A_IOMUX_SEL_H[7:4] =4'h9

Notes: I=input, O=output, I/O=input/output, bidirectional

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Chapter 7 MMU

7.1 Overview

The MMU controller is nested in front of the IP AXI master to convert the AXI virtual address access from the IP into physical address access. It supports the follow features

- Support a two-level page table method for address mapping, the physical address is 40bits, the virtual address is 32bits.
- Support One Read One Write AXI Channel.
- Support LRUK(K=1) Page Table replacement algorithm.

7.2 Block Diagram

MMU comprises with:

- AXI_INTF: It can convert the virtual address from AXI Slave Interface to the physical address by the AXI Master Interface
- SIF : AHB Slave Interface. It is the slave configuration interface. It can be read or write registers by the interface.
- SRAM : The MMU Page Table information is stored in the SRAM.
- Cache: Cache Controller. It implement the address translation for MMU.

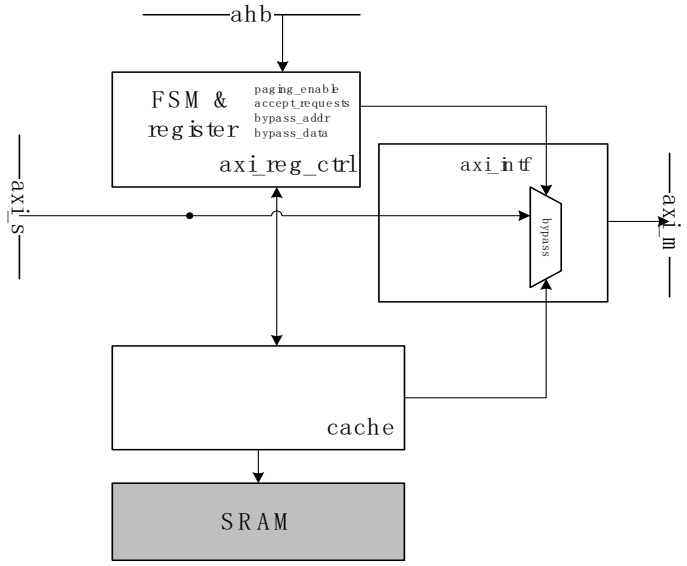

Fig. 7-1 MMU Structure

7.3 Function Description

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:

1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

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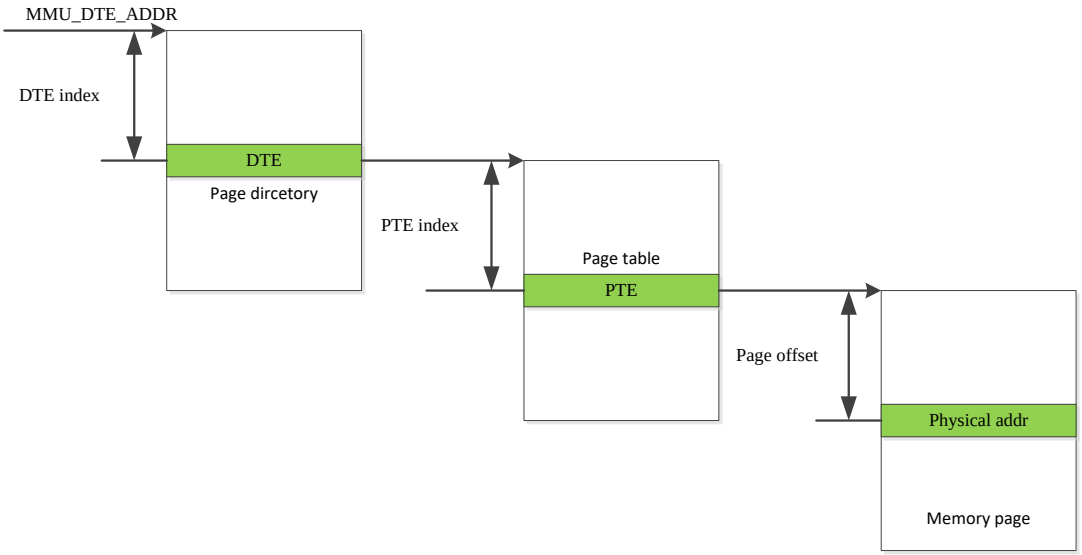
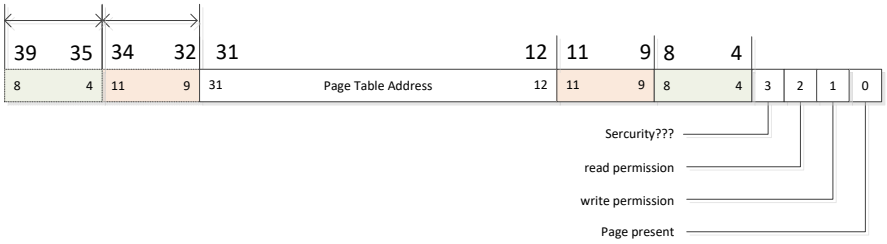


32BIT DTE mapping to 40bit Addr



32BIT PTE mapping to 40bit Addr

Fig. 7-2 Structure of two-level page table

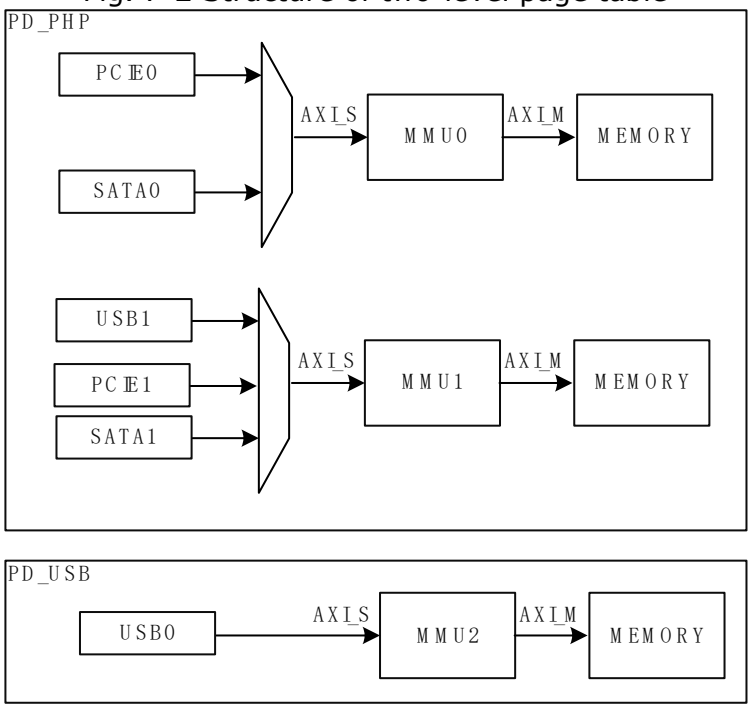


Fig. 7-3 MMU Position in the system

There are three MMU in the chip.

MMU0 is in the PD_PHP domain. Both PCIE0 and SATA0 use the same MMU which named MMU0.

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MMU1 is in the PD_PHP domain. USB1 , PCIE1 and SATA1 use the same MMU which named MMU1.

MMU2 is in the PD_USB domain. It is exclusively for USB0 Master.

7.4 Register Description

7.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
MMU0	0x2A260000
MMU1	0x2A270000
MMU2	0x2A2C0000

7.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address. It is only can be written when MMU state is disable or page fault or MMU enable stall state
MMU_STATUS	0x0004	W	0x00000018	MMU status register
MMU_COMMAND	0x0008	W	0x00000000	MMU command register
MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault
MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
MMU_INT_MASK	0x001C	W	0x00000000	MMU raw interrupt status register
MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
MMU_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3 Detail Registers Description

MMU_DTE_ADDR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	MMU_DTE_ADDR mmu dte base addr[31:12] , the address must be 4kb aligned
11:8	RW	0x0	MMU_DTE_ADDR_35_32 mmu dte base addr[35:32] , the address must be 4kb aligned
7:4	RW	0x0	MMU_DTE_ADDR_39_36 mmu dte base addr[39:36] , the address must be 4kb aligned
3:0	RO	0x0	reserved

MMU_STATUS

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master responsible for last page fault

Bit	Attr	Reset Value	Description
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty.
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STALL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled. The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

MMU_COMMAND

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_ALL_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

MMU_PAGE_FAULT_ADDR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

MMU_ZAP_ONE_LINE

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

MMU_INT_RAWSTAT

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

MMU_INT_CLEAR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	READ_BUS_ERROR write 1 to clear read bus error Write 0 not to clear read bus error
0	WO	0x0	PAGE_FAULT write 1 to clear page fault Write 0 not to clear page fault

MMU_INT_MASK

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT page fault enable an interrupt source if the corresponding mask bit is set to 1

MMU_INT_STATUS

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

MMU_AUTO_GATING

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_auto_gating when it is 1'b1, the MMU will auto gating it self

7.5 Interface Description

None.

7.6 Application Notes

7.6.1 Normal Process

After the power on reset is completed, the MMU is in a disabled state, which can be achieved it through the following steps

Step1: Prepare a space to save MMU page table information

Step2: Write the address of Page Directory into the MMU_DTE_ADDR register

Step3: Write MMU_ENABLE_PAGING into MMU_COMMAND register

7.6.2 Page Fault Process

When the MMU caused by page not present

Step1: Update page tables

Step2: Clear the page fault interrupt

Step3: Read the MMU_STATUS register to get information

Step4: Zap all

Step5: Writing MMU_PAGE_FAULT_DONE to the MMU_COMMAND register to leave the page

fault state

When the MMU caused by unpermitted
Reset the MMU and the processor connected to it. Or Redirect all memory accesses to a temporary memory area until the processor can safely stopped.

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Chapter 8 MCU Subsystem

8.1 Overview

The MCU Subsystem embedded one MCU processor (Cortex-M0 r0p0-03rel0), a 16KB unified I/D cache, a tightly-coupled memory(TCM) and interrupt multiplexer(INTMUX). It allowed fast & efficient data exchange. And the Level 1 Instruction/Data Cache designed for MCU can improve the memory access performance significantly.
The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.
The MCU features and benefits are:

- One MCU processor
- Tightly-coupled memory(TCM)
- Optional debug support
  - Two hardware breakpoints
  - One watch points
  - Support Serial Wire debug connection
- Interrupt multiplexer(INTMUX)
  - Mux 12 interrupts from 357 interrupt sources using round-robin algorithm
  - Each 32 adjacent interrupts are seen as a group which share same INTMUX_INT_ENABLE_GROUPx and INTMUX_INT_FLAG_GROUPx register
- 16KB unified I/D Cache
  - Support 2-way set-associative with 32Byte cache line size
  - Support one 64bit AHB-Lite bus master interface to SOC interconnect
  - Support memory cacheable access and peripheral bypass access
  - Support Write-Through with No-Write-Allocate and Read-Allocate
  - Support Write-Back with Write-Allocate and Read-Allocate
  - Support cache maintenance operations (clean/invalidate/clean & invalidate) by address
  - Support cache invalidate/clean & invalidate operations for all cache lines
  - Support cache initialization by software configuration
  - Support RAM debug mode for tag RAM and data RAM
  - Support one interrupt source

There are four MCU subsystem in RK3576, PMU_MCU, NPU_MCU, DDR_MCU and BUS_MCU respectively. But only BUS_MCU is available for the third-party, the other three MCU are reserved for Rockchip. Their main configurations are different, As shown below.

Table 8-1 MCU Subsystem Configurations

	PMU_MCU	NPU_MCU	DDR_MCU	BUS_MCU
TCM	NA	NA	20KB	NA
CACHE	16KB	16KB	NA	16KB
IRQ_NUM	32	32	32	32
INTMUX	YES	NA	YES	YES

8.2 Block Diagram

The Int_in[356:0] will connect with all interrupt source of RK3576 except that only for CPU, and please refer to "Chapter System Overview" for the detail interrupt number. MCU Subsystem are shown below.

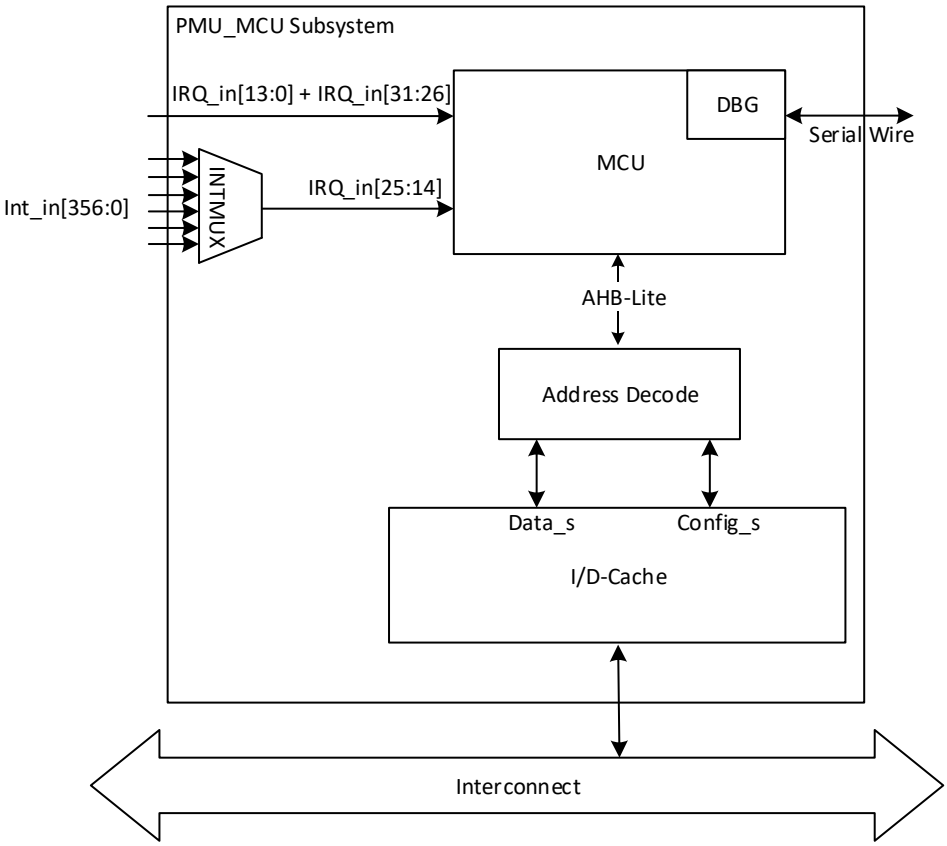

Fig. 8-1 Block Diagram of PMU_MCU Subsystem

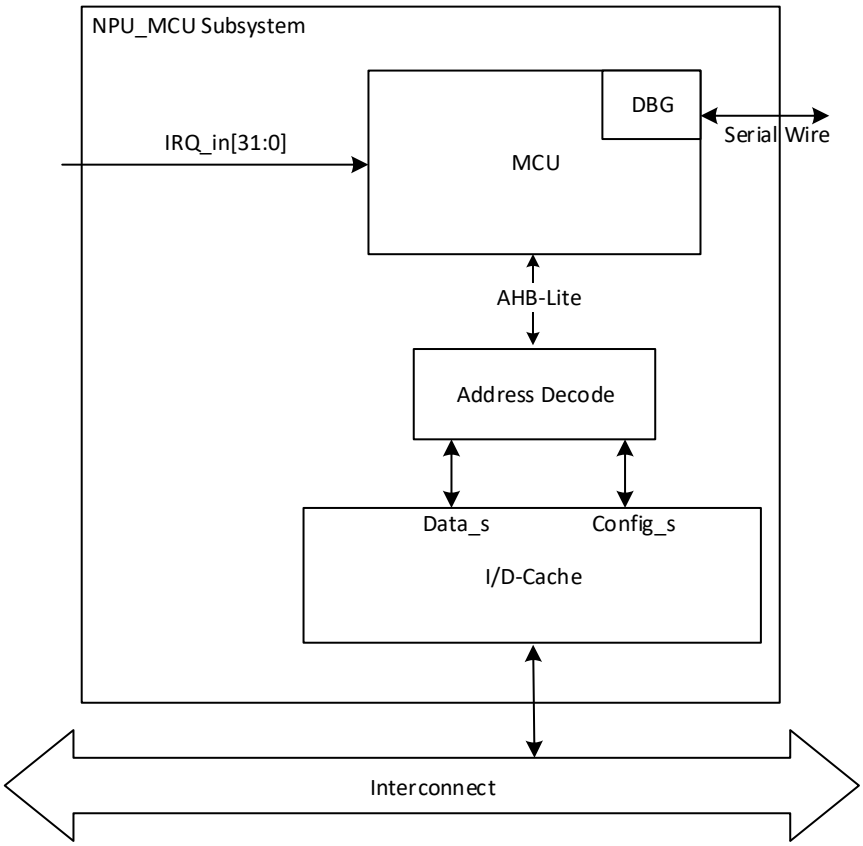

Fig. 8-2 Block Diagram of NPU_MCU Subsystem

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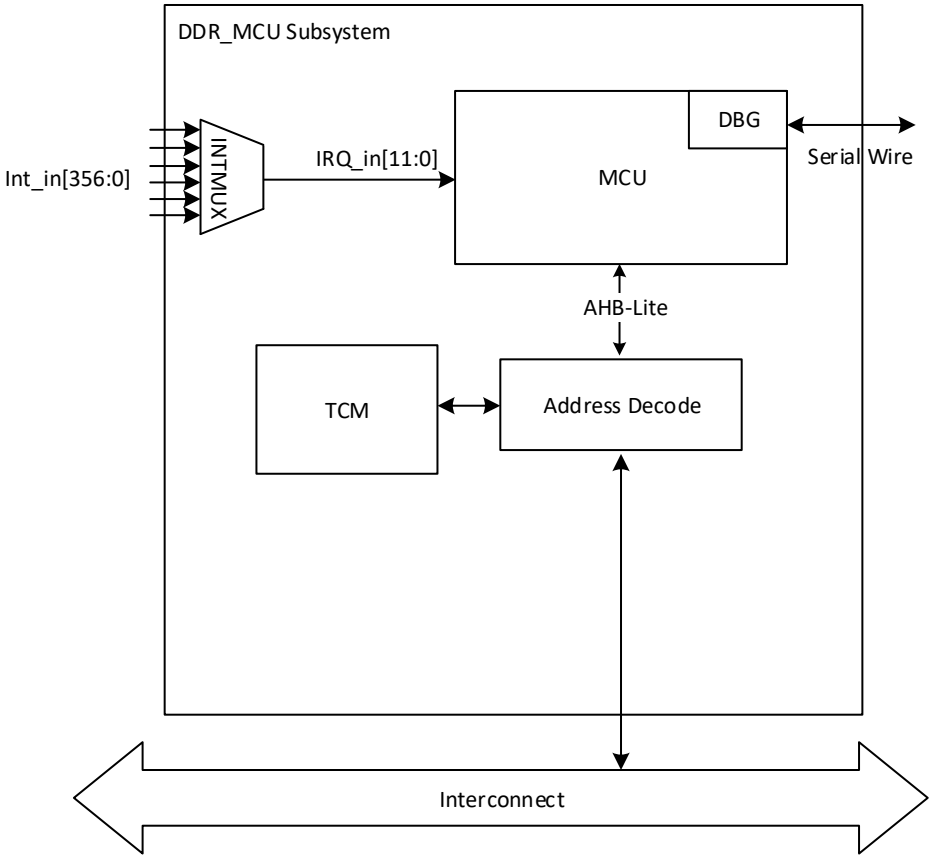

Fig. 8-3 Block Diagram of DDR_MCU Subsystem

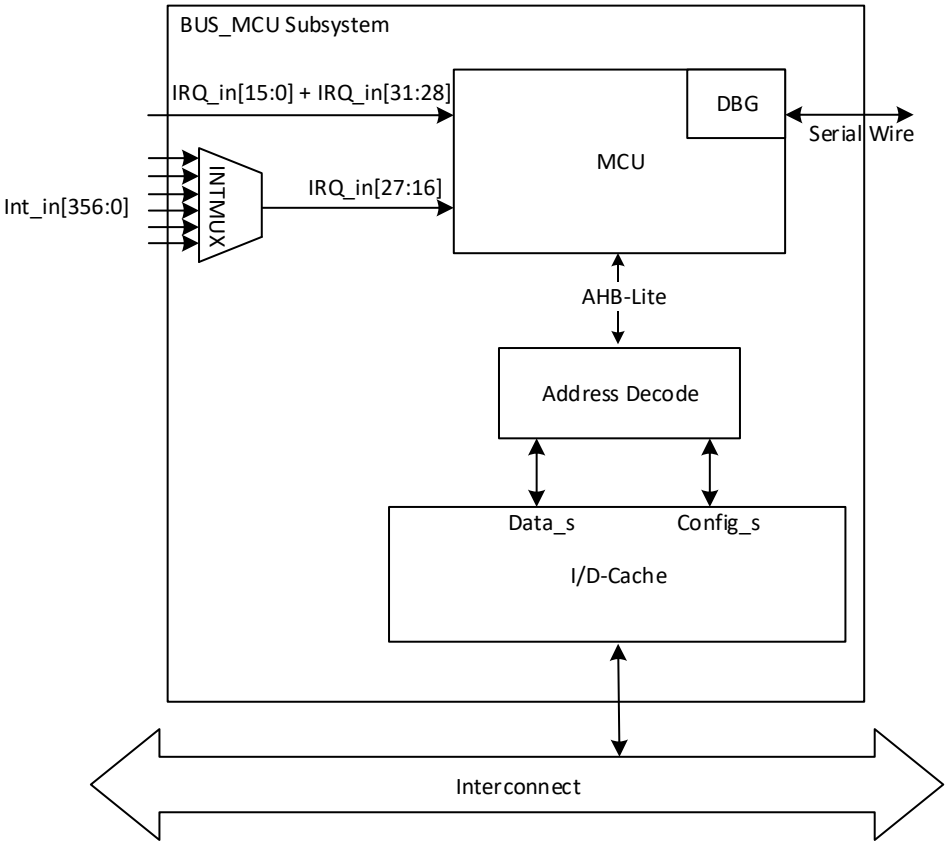

Fig. 8-4 Block Diagram of BUS_MCU Subsystem

8.3 CACHE Register Description

8.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

8.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CACHE_CACHE_CTRL	0x0000	W	0x0000002D	Cache Control Register
CACHE_CACHE_MAINTAIN0	0x0004	W	0x00000000	Cache Maintain Register0
CACHE_CACHE_MAINTAIN1	0x0008	W	0x00000000	Cache Maintain Register1
CACHE_STB_TIMEOUT_CTRL	0x000C	W	0x00000000	Store Buffer Timeout Control Register
CACHE_CACHE_INT_EN	0x0020	W	0x00000000	Cache Interrupt Enable Register
CACHE_CACHE_INT_ST	0x0024	W	0x00000000	Interrupt Status Register
CACHE_CACHE_ERR_HADDR	0x0028	W	0x00000000	Address record when AHB error response on AHB master interface
CACHE_CACHE_STATUS	0x0030	W	0x00000000	Cache Status Register
CACHE_PMU_RD_NUM_CNT	0x0040	W	0x00000000	PMU read number counter status
CACHE_PMU_WR_NUM_CNT	0x0044	W	0x00000000	PMU write number counter status
CACHE_PMU_SRAM_RD_HIT_CNT	0x0048	W	0x00000000	PMU SRAM hit counter status
CACHE_PMU_HB_RD_HIT_CNT	0x004C	W	0x00000000	PMU hot buffer hit status
CACHE_PMU_STB_RD_HIT_CNT	0x0050	W	0x00000000	PMU store buffer hit status
CACHE_PMU_RD_HIT_CNT	0x0054	W	0x00000000	PMU read hit counter status
CACHE_PMU_WR_HIT_CNT	0x0058	W	0x00000000	PMU write hit counter status
CACHE_PMU_RD_MISS_PENALTY_CNT	0x005C	W	0x00000000	PMU read miss penalty counter status
CACHE_PMU_WR_MISS_PENALTY_CNT	0x0060	W	0x00000000	PMU write miss penalty counter status
CACHE_PMU_RD_LAT_CNT	0x0064	W	0x00000000	PMU read latency status
CACHE_PMU_WR_LAT_CNT	0x0068	W	0x00000000	PMU write latency status
CACHE_REVISION	0x00F0	W	0x00000103	Cache design revision register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

8.3.3 Detail Registers Description

CACHE_CACHE_CTRL

Address: Operational Base(0x23810000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	cache_mpu_mode Cortex-m4 mpu mode support 1'b0: not support mpu mode 1'b1: support mpu mode, the cache controller will cache the request if both hprot[3] and memattr[0] is high on AHB slave bus, or will bypass the request.
11	RO	0x0	reserved
10:8	RW	0x0	cache_entry_thresh Cache store buffer entry threshold control register, when data entries are more than threshold value, the write data will be write to Cache RAM

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Bit	Attr	Reset Value	Description
7	RW	0x0	stb_timeout_en Store buffer time out enable, when this bit is set enable, the data in store buffer must be flushed to Cache RAM. 1'b0: Disable 1'b1: Enable
6	RW	0x0	cache_bypass Cache bypass controller register, when this bit is set high, data will bypass the AHB interface. 1'b0: Disable 1'b1: Enable
5	RW	0x1	cache_pmu_en Cache performance monitor enable register 1'b0: Disable 1'b1: Enable
4	RW	0x0	cache_flush Cache flush enable, when this bit is set enable, the dirty data is flushed to external memory and the cache line are set invalid 1'b0: Disable 1'b1: Enable
3	RW	0x1	cache_stb_en Cache store buffer enable register 1'b0: Disable 1'b1: Enable This bit must be disable when write through mode is selected
2	RW	0x1	cache_hb_en Cache hot buffer enable register 1'b0: Disable 1'b1: Enable
1	RW	0x0	cache_wt_en Cache mode control register 1'b0: write back 1'b1: write through
0	RW	0x1	cache_en Cache enable bit 1'b0: Disable 1'b1: Enable

CACHE_CACHE_MAINTAIN0

Address: Operational Base(0x23810000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	cache_m_addr Cache maintain start address
4:3	RO	0x0	reserved
2:1	RW	0x0	cache_m_cmd Cache maintain command register 2'b00: Cache clean 2'b01: Cache invalid 2'b10: Cache clean and invalid 2'b11: Cache invalid all
0	RW	0x0	cache_m_valid Cache maintain valid register, the cache_m_cmd will be valid only this bit is set high.

CACHE_CACHE_MAINTAIN1

Address: Operational Base(0x23810000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	cache_m_offset Cache maintain offset address, the maintain address scope is from cache_m_addr to cache_m_addr + cache_m_offset

CACHE_STB_TIMEOUT_CTRL

Address: Operational Base(0x23810000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	stb_timeout_value Store buffer timeout counter value

CACHE_CACHE_INT_EN

Address: Operational Base(0x23810000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	err_record_en AHB master bus error record enable 1'b0: Disable 1'b1: Enable

CACHE_CACHE_INT_ST

Address: Operational Base(0x23810000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ahb_error_status Error status bit on ahb master bus

CACHE_CACHE_ERR_HADDR

Address: Operational Base(0x23810000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	status_haddr Address information when ahb bus error

CACHE_CACHE_STATUS

Address: Operational Base(0x23810000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	cache_flush_done Cache flush finish status register
1	RO	0x0	cache_m_busy Cache maintain busy status register
0	RO	0x0	cache_init_finish Cache initialization finish status register

CACHE_PMU_RD_NUM_CNT

Address: Operational Base(0x23810000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_num_cnt Performance monitor read nunber register

CACHE_PMU_WR_NUM_CNT

Address: Operational Base(0x23810000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_num_cnt Performance monitor write number register

CACHE_PMU_SRAM_RD_HIT_CNT

Address: Operational Base(0x23810000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_sram_rd_hit_cnt Performance monitor SRAM hit counter register

CACHE_PMU_HB_RD_HIT_CNT

Address: Operational Base(0x23810000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_hb_rd_hit_cnt Performance monitor hot buffer hit counter register

CACHE_PMU_STB_RD_HIT_CNT

Address: Operational Base(0x23810000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_stb_rd_hit_cnt Performance monitor store buffer hit counter register

CACHE_PMU_RD_HIT_CNT

Address: Operational Base(0x23810000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_hit_cnt Performance monitor read hit counter register

CACHE_PMU_WR_HIT_CNT

Address: Operational Base(0x23810000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_hit_cnt Performance monitor write hit register

CACHE_PMU_RD_MISS_PENALTY_CNT

Address: Operational Base(0x23810000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_miss_penalty_cnt Performance monitor read miss penalty count register

CACHE_PMU_WR_MISS_PENALTY_CNT

Address: Operational Base(0x23810000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_miss_penalty_cnt Performance monitor write miss penalty register

CACHE_PMU_RD_LAT_CNT

Address: Operational Base(0x23810000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_lat_cnt Performance monitor read latency register

CACHE_PMU_WR_LAT_CNT

Address: Operational Base(0x23810000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_lat_cnt Performance monitor write latency register

CACHE_REVISION

Address: Operational Base(0x23810000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000103	revision Design revision

8.4 INTMUX Register Description

8.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
INTMUX(PMU_MCU)	0x2AE90000
INTMUX(DDR_MCU)	0x2AEA0000
INTMUX(BUS_MCU)	0x2AEC0000

8.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
INTMUX_INT_ENABLE_GROUP0	0x0000	W	0x00000000	Interrupt Group0 Enable Register
INTMUX_INT_ENABLE_GROUP1	0x0004	W	0x00000000	Interrupt Group1 Enable Register
INTMUX_INT_ENABLE_GROUP2	0x0008	W	0x00000000	Interrupt Group2 Enable Register
INTMUX_INT_ENABLE_GROUP3	0x000C	W	0x00000000	Interrupt Group3 Enable Register
INTMUX_INT_ENABLE_GROUP4	0x0010	W	0x00000000	Interrupt Group4 Enable Register
INTMUX_INT_ENABLE_GROUP5	0x0014	W	0x00000000	Interrupt Group5 Enable Register
INTMUX_INT_ENABLE_GROUP6	0x0018	W	0x00000000	Interrupt Group6 Enable Register
INTMUX_INT_ENABLE_GROUP7	0x001C	W	0x00000000	Interrupt Group7 Enable Register
INTMUX_INT_ENABLE_GROUP8	0x0020	W	0x00000000	Interrupt Group8 Enable Register
INTMUX_INT_ENABLE_GROUP9	0x0024	W	0x00000000	Interrupt Group9 Enable Register
INTMUX_INT_ENABLE_GROUP10	0x0028	W	0x00000000	Interrupt Group10 Enable Register
INTMUX_INT_ENABLE_GROUP11	0x002C	W	0x00000000	Interrupt Group11 Enable Register
INTMUX_INT_FLAG_GROUP0	0x0080	W	0x00000000	Interrupt Group0 Flag Register
INTMUX_INT_FLAG_GROUP1	0x0084	W	0x00000000	Interrupt Group1 Flag Register
INTMUX_INT_FLAG_GROUP2	0x0088	W	0x00000000	Interrupt Group2 Flag Register
INTMUX_INT_FLAG_GROUP3	0x008C	W	0x00000000	Interrupt Group3 Flag Register

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Name	Offset	Size	Reset Value	Description
INTMUX_INT_FLAG_GROUP4	0x0090	W	0x00000000	Interrupt Group4 Flag Register
INTMUX_INT_FLAG_GROUP5	0x0094	W	0x00000000	Interrupt Group5 Flag Register
INTMUX_INT_FLAG_GROUP6	0x0098	W	0x00000000	Interrupt Group6 Flag Register
INTMUX_INT_FLAG_GROUP7	0x009C	W	0x00000000	Interrupt Group7 Flag Register
INTMUX_INT_FLAG_GROUP8	0x00A0	W	0x00000000	Interrupt Group8 Flag Register
INTMUX_INT_FLAG_GROUP9	0x00A4	W	0x00000000	Interrupt Group9 Flag Register
INTMUX_INT_FLAG_GROUP10	0x00A8	W	0x00000000	Interrupt Group10 Flag Register
INTMUX_INT_FLAG_GROUP11	0x00AC	W	0x00000000	Interrupt Group11 Flag Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

8.4.3 Detail Registers Description

INTMUX_INT_ENABLE_GROUP0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP2

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP3

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP4

Address: **Operational Base** + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP5

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP6

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP7

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP8

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP9

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP10

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP11

Address: **Operational Base** + offset (0x002C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_FLAG_GROUP0

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP1

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP2

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP3

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP4

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP5

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP6

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP7

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP8

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP9

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP10

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP11

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

8.5 Interface Description

There are two sets of serial debug interface for the four MCUs. When we debug using serial wire, not only set IOMUX, but also configure the bit[4:1] of SYS_GRF_SOC_CON7 to select the MCU that you want to debug. Note that, due to CPU and MCU share the debug pins, and the debug path switch to CPU by default, so you shall also configure the bit[0] of SYS_GRF_SOC_CON7 to unselect CPU path. Please refer to Chapter GRF for more detail.

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Table 8-2 MCU Serial Wire Debug Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
mcujtag_tckm0	I	SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[11:8] = 4'h9
mcujtag_tmsm0	I/O	SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/CAN1_TX_M0/I3C1_SDA_M1/GPIO2_A3_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[15:12] = 4'h9
mcujtag_tckm1	I	UART0_TX_M0/JTAG_TCK_M1/GPIO0_D4_u	PMU1_IOC_GPIO0D_IOMUX_SEL_H[3:0] = 4'ha
mcujtag_tmsm1	I/O	UART0_RX_M0/JTAG_TMS_M1/GPIO0_D5_u	PMU1_IOC_GPIO0D_IOMUX_SEL_H[7:4] = 4'ha

Notes: I=input, O=output, I/O=input/output, bidirectional

8.6 Application Notes

8.6.1 Clock and Reset Generation

Please refer to Chapter CRU for more detailed information.

8.6.2 Memory Remap

The memory map is divided into different memory types for different usage.
To avoid the memory map conflict between different processors, the source space can be remap to another. In addition, these remap operation could not take effect until the MCU soft reset.

Table 8-3 PMU_MCU Address Remap

Before Remap	Memory Type	Usage	After Remap
0x40000000 - 0x5FFFFFFF	Device XN	Peripherals	Before Remap - 0x40000000 + 0x20000000
0x20000000 - 0x3FFFFFFF	Normal WBWA	On chip RAM	Before Remap - 0x20000000 + {PMU1_SGRF_SOC_CON13[31:10],10'h0}
0x00000000 - 0x1FFFFFFF	Normal WT	ROM or flash	Before Remap - 0x0000000 + {PMU1_SGRF_SOC_CON12[31:10],10'h0}

Table 8-4 NPU_MCU Address Remap

Before Remap	Memory Type	Usage	After Remap
0x40000000 - 0x5FFFFFFF	Device XN	Peripherals	Before Remap - 0x40000000 + 0x20000000
0x20000000 - 0x3FFFFFFF	Normal WBWA	On chip RAM	Before Remap - 0x20000000 + {SYS_SGRF_SOC_CON12[31:10],10'h0}
0x00000000 - 0x1FFFFFFF	Normal WT	ROM or flash	Before Remap - 0x0000000 + {SYS_SGRF_SOC_CON11[31:10],10'h0}

Table 8-5 DDR_MCU Address Remap

Before Remap	Memory Type	Usage	After Remap
0x40000000 - 0x5FFFFFFF	Device XN	Peripherals	Before Remap - 0x40000000 + 0x20000000
0x20000000 - 0x3FFFFFFF	Normal WBWA	On chip RAM	Before Remap - 0x20000000 + {SYS_SGRF_SOC_CON9[31:10],10'h0}
0x00000000 - 0x1FFFFFFF	Normal WT	ROM or flash	Before Remap - 0x0000000 + {SYS_SGRF_SOC_CON8[31:10],10'h0}

Table 8-6 BUS_MCU Address Remap

Before Remap	Memory Type	Usage	After Remap
0x40000000 - 0x5FFFFFFF	Device XN	Peripherals	Before Remap - 0x40000000 + 0x20000000
0x20000000 - 0x3FFFFFFF	Normal WBWA	On chip RAM	Before Remap - 0x20000000 + {SYS_SGRF_SOC_CON17[31:10],10'h0}
0x00000000 - 0x1FFFFFFF	Normal WT	ROM or flash	Before Remap - 0x0000000 + {SYS_SGRF_SOC_CON16[31:10],10'h0}

Notes:

- *XN means execute-never.*

- *WT means write-through.*
- *WBWA means write-back-write-allocate.*

Note that, the peripherals space at MCU view is different to that at CPU view by default setting. There are two ways for MCU to access peripherals:

- Regard the address space 0x40000000-0x5FFFFFFF of MCU as peripherals space, then to get the peripherals address of MCU view, you need to plus the peripherals address of CPU view with 0x20000000.
- Regard the address space 0x2000000-0x3FFFFFFF of MCU as peripherals space, then the peripherals space at MCU view will be unified to that of CPU view, if you configure the SGRF of on chip RAM remap to 0x20000000.

8.6.3 Interrupt for MCU

The Int_in[356:0] are part of system interrupts(system interrupt ID 64-420), and each 32 interrupts will multiplexed into one interrupt. Please refer to "Chapter System Overview" for the detail interrupt number.

Table 8-7 PMU_MCU Interrupt

IRQ ID	IRQ Source	IRQ ID	IRQ Source
0	irq_gpio0[0]	16	Int_in[95:64] mux 1
1	irq_i2c0	17	Int_in[127:96] mux 1
2	irq_vdma	18	Int_in[159:128] mux 1
3	irq_pwm0_2ch_0	19	Int_in[191:160] mux 1
4	irq_pwm1_2ch_1	20	Int_in[223:192] mux 1
5	irq_pmu_wdt	21	Int_in[255:224] mux 1
6	irq_pmu_timer_ch1	22	Int_in[287:256] mux 1
7	irq_pmu_timer_ch0	23	Int_in[319:288] mux 1
8	irq_sdmmc_detectn_grf	24	Int_in[351:320] mux 1
9	irq_uart1	25	Int_in[383:352] mux 1
10	pmu0/1_sgrf_crc_chk_rst_req	26	reserved
11	irq_osc_chk_rst_req	27	irq_pdm0
12	irq_pmu_mcu_cache	28	irq_mailbox_bb6
13	irq_pmic	29	irq_pmu_pvtm
14	Int_in[31:0] mux 1	30	reserved
15	Int_in[63:32] mux 1	31	reserved

Table 8-8 NPU_MCU Interrupt

IRQ ID	IRQ Source	IRQ ID	IRQ Source
0	irq_rknn_mcu_cache	5	irq_rknn_core0
1	irq_npu_timer_ch1	6	irq_uart1
2	irq_npu_timer_ch0	7	irq_mailbox_bb12
3	irq_npu_wdt	8	irq_mailbox_bb13
4	irq_rknn_core1	9-31	reserved

Table 8-9 DDR_MCU Interrupt

IRQ ID	IRQ Source	IRQ ID	IRQ Source
0	Int_in[31:0] mux 1	7	Int_in[255:224] mux 1
1	Int_in[63:32] mux 1	8	Int_in[287:256] mux 1
2	Int_in[95:64] mux 1	9	Int_in[319:288] mux 1
3	Int_in[127:96] mux 1	10	Int_in[351:320] mux 1
4	Int_in[159:128] mux 1	11	Int_in[383:352] mux 1

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IRQ ID	IRQ Source	IRQ ID	IRQ Source
5	Int_in[191:160] mux 1	12-31	reserved
6	Int_in[223:192] mux 1	-	-

Table 8-10 BUS_MCU Interrupt

IRQ ID	IRQ Source	IRQ ID	IRQ Source
0	irq_gpio0[3]	16	Int_in[31:0] mux 1
1	irq_gpio1[3]	17	Int_in[63:32] mux 1
2	irq_gpio2[3]	18	Int_in[95:64] mux 1
3	irq_gpio3[3]	19	Int_in[127:96] mux 1
4	irq_gpio4[3]	20	Int_in[159:128] mux 1
5	irq_saradc	21	Int_in[191:160] mux 1
6	irq_timer_ns_1_ch3	22	Int_in[223:192] mux 1
7	irq_timer_ns_1_ch4	23	Int_in[255:224] mux 1
8	irq_spi4	24	Int_in[287:256] mux 1
9	irq_mailbox_bb0	25	Int_in[319:288] mux 1
10	irq_sdmmc	26	Int_in[351:320] mux 1
11	irq_dmac2	27	Int_in[383:352] mux 1
12	irq_i2c3	28	reserved
13	irq_uart11	29	irq_gpio0[2]
14	irq_pwm2_8ch_6	30	irq_gpio4[1]
15	irq_flexbus	31	irq_gpio4[2]

The table below show the interrupt ID translation between CPU and MCU. Int_in[0] is connected to irq_dmac0 (system interrupt 64), and Int_in[31] is connected to irq_timer_s_1_ch0 (system interrupt 95).
All Int_in are divided into 12 interrupt groups. For example, Int_in[31:0] are belong to INTMUX group 0, which means you should configure INTMUX_INT_ENABLE_GROUP0 to enable interrupt of this group. Every single bit of INTMUX_INT_ENABLE_GROUP0 is response for one interrupt source. And for BUS_MCU view，interrupts from INTMUX group 0 will trigger IRQ ID 16 of NVIC.

Table 8-11 Interrupt Translation between CPU and MCU

Int_in Bit	System Interrupt Number	Interrupt Source	INTMUX Group
Int_in[0]	64	irq_dmac0	group 0
…	…	…	…
Int_in[31]	95	irq_timer_s_1_ch0	group 0
Int_in[32]	96	irq_timer_s_1_ch0	group 1
…	…	…	…
Int_in[63]	127	irq_i2c7	group 1
…	…	…	…
Int_in[356]	420	irq_vepu1_mmu	group 11
Int_in[357] ~ Int_in[383]	reserved	reserved	group 11

Interrupt configuration flow of MCU:
1. Check the system interrupt number of target interrupt, consider it as INTID;
2. Configure bit y of INTMUX_INT_ENABLE_GROUPx in corresponding INTMUX of MCU, where x = (INTID-64)/32, y = (INTID-64)%32;
3. Enable the IRQ ID z of NVIC, where z = IRQ_ID_BASE + x;
4. Wait for interrupt trigger.

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Table 8-12 IRQ_ID_BASE of different MCU

MCU Type	IRQ_ID_BASE
PMU_MCU	14
DDR_MCU	0
BUS_MCU	16

8.6.4 Cache Initialization

The Cache is bypassed after reset and need to be initialized by the MCU. The basic initialization flow is:

1. Configure to Write-Back or Write-Through mode by setting CACHE_CACHE_CTRL.cache_wt_en and start initialization by configuring CACHE_CACHE_CTRL.cache_en to high while keeping the Cache in bypass mode (CACHE_CACHE_CTRL.cache_bypass is high). The store buffer must and only can be enabled for Write-Back mode, so you must disable the store buffer when Write-Through mode is selected. You can also enable the hot buffer for better performance.
2. Wait for cache initialization to be finished by polling CACHE_CACHE_STATUS.cache_init_finish.
3. Disable cache bypass mode by configuring CACHE_CACHE_CTRL.cache_bypass to low. Now that the Cache is enabled.
4. Simply configure CACHE_CACHE_CTRL.cache_bypass to bypass or enable the Cache again after the initialization flow.

8.6.5 Cache Maintenance

The Cache Controller support the following cache maintenance operations:

- Clean by address: push the specified cache line data to external memory if it is valid and dirty.
- Invalidate by address: unconditionally clear the valid and dirty data of the specified cache lines.
- Clean and invalidate by address: clean and then invalidate the specified cache lines.
- Invalidate all: unconditionally clear the valid and dirty data for all the cache lines.
- Clean and invalidate all (Flush): clean and then invalidate all the cache lines.

For the operation of cache clean and invalidate all, configure CACHE_CACHE_CTRL.cache_flush to high first, and then wait for flush to be done by polling CACHE_CACHE_STATUS.cache_flush_done. Finally, if the flush is done, you should configure CACHE_CACHE_CTRL.cache_flush to low.

For the other four maintenance operations, you should set the maintenance command and the address range of the cache lines by configuring CACHE_CACHE_MAINTAIN0 and CACHE_CACHE_MAINTAIN1, then start by configuring CACHE_CACHE_MAINTAIN0.cache_m_valid to high. When the operation is finished, CACHE_CACHE_MAINTAIN0.cache_m_valid will be automatically cleared to low. You can also poll CACHE_CACHE_STATUS.cache_m_busy to judge whether the operation is done.

8.6.6 Cache RAM Debug Mode

When the Cache is enabled and not in the bypass mode, you can enter the cache RAM debug mode by configuring CACHE_CACHE_RAM_DEBUG.ram_debug_en to high. In the RAM debug mode, the cache RAM can be accessed directly by the specific address, and all the other cacheable memory accesses are bypassed because the cache core is disabled. The following table shows the address map for the cache RAM debug.

Table 8-13 Address Map for the Cache RAM Debug

RAM Access Type	RAM Access Size	Address Range for Cache RAM Debug
Reserved	7KB	0x23826400 ~ 0x23827FFF
TAG RAM1	1KB	0x23826000 ~ 0x238263FF

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RAM Access Type	RAM Access Size	Address Range for Cache RAM Debug
Reserved	7KB	0x23824400 ~ 0x23825FFF
TAG RAM0	1KB	0x23824000 ~ 0x238243FF
DATA RAM1	8KB	0x23822000 ~ 0x23823FFF
DATA RAM0	8KB	0x23820000 ~ 0x23821FFF

As shown in the above table, there are 2 ways for each cache, and the size of one DATA RAM is 8KB. The following explanation may help you use the RAM debug method:

- Using the word-aligned address to access the TAG RAM.
- The bits[9:2] of the TAG RAM address are acted as the bits[12:5] of the corresponding memory address.
- Only the bits[20:0] of the TAG RAM data are available, and the bits[31:21] are always zero.
  - The bit[20] is the valid flag bit.
  - The bit[19] is the dirty flag bit.
  - The bits[18:0] are acted as the bits[31:13] of the corresponding memory address.
- The bits[12:0] of the DATA RAM address are acted as the bits[12:0] of the corresponding memory address.
- In order to get the cache line data at the wanted address, you should read the both of the TAG RAMs to find the matched address, and then read data from the corresponding DATA RAM.
- If write data to the DATA RAM, 8 copies of the 32bit data on the AHB bus will be written to the 32Byte cache line.

8.6.7 TCM

DDR MCU Subsystem implement data/instructions tightly-coupled memory to speed up code execute, but only MCU can access TCM. In addition, the base address of TCM are configurable to ease software. Refer to SYS_SGRF_SOC_CON7 for more detail.

8.6.8 Other Hints

- One interrupt request source is supported for the I/D-Cache, so you can query the interrupt register in the ISR if it is enabled. When CACHE_CACHE_INT_EN.err_record_en is high, the Cache will generate a bus error interrupt if access to a wrong address. You can read CAHCE_CACHE_INT_ST.ahb_error_status for the cache interrupt status and get the recent error address information from CACHE_CACHE_ERR_HADDR.status_haddr.
- The non-cacheable space of cache can be configured by GRF, please refer to Chapter GRF for more detail.

Table 8-14 Configuration of Cache Peripheral Space

MCU Type	Begin Address	End Address
PMU_MCU	PMU1_SGRF_SOC_CON10	PMU1_SGRF_SOC_CON11
NPU_MCU	NPU_GRF_START_ADDR	NPU_GRF_END_ADDR
BUS_MCU	SYS_SGRF_SOC_CON14	SYS_SGRF_SOC_CON15

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Chapter 9 System Debug

9.1 Overview

The chip uses the DAPLITE Technology to support real-time debug.

9.1.1 Features

- Invasive debug with core halted
- SW-DP

9.1.2 Debug Components Address Map

The following table shows the debug components address in memory map, you should add offset 0x400000 when you access Cortex-A72 Debug.

Module	Base Address
DAP_ROM	0x22800000

9.2 Block Diagram

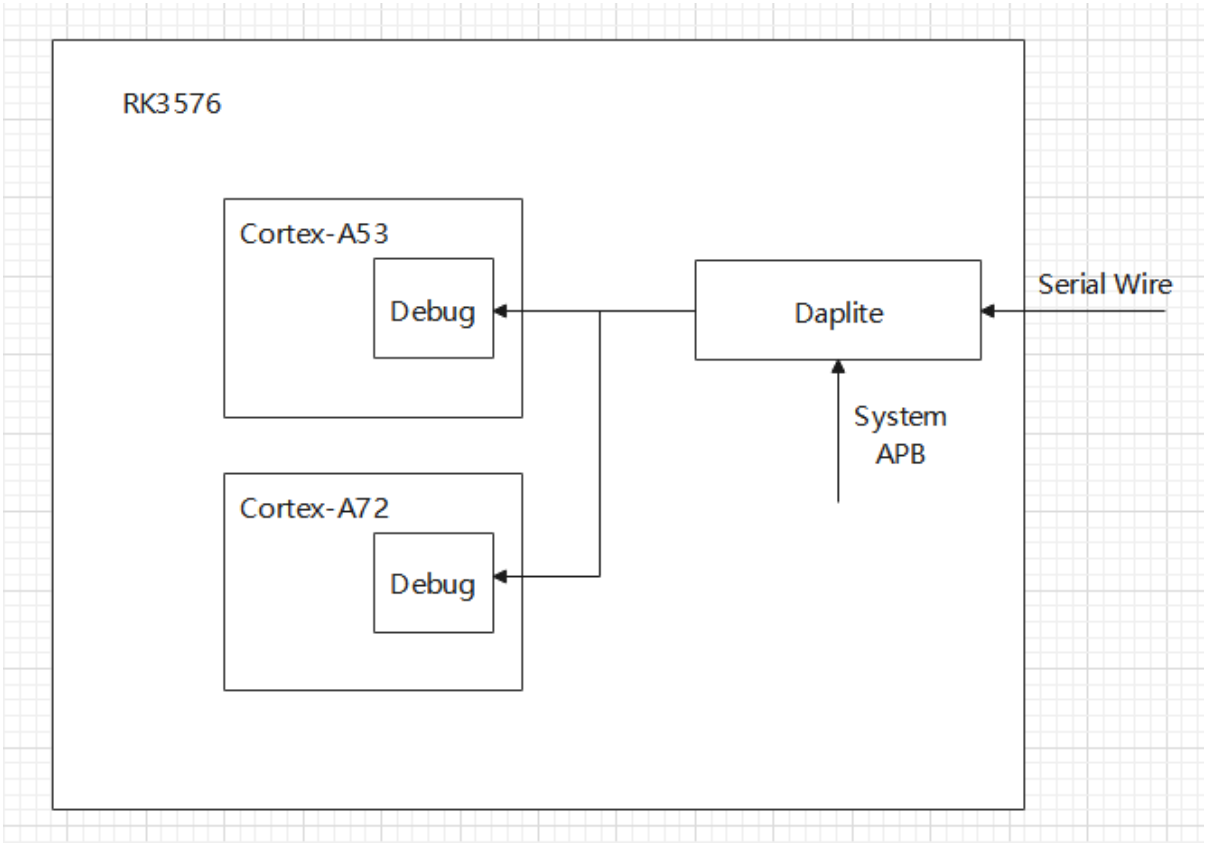

Fig. 9-1Debug system structure

9.3 Function Description

9.3.1 DAP

The DAP has following components:

- Serial Wire JTAG Debug Port(SWJ-DP)
- APB Access Port(APB-AP)
- ROM table

The debug port is the host tools interface to access the DAP-Lite. This interface controls any access ports provided within the DAP-Lite. The DAP-Lite supports a combined debug port which includes both JTAG and Serial Wire Debug(SWD), with a mechanism that supports switching between them.

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The APB-AP acts as a bridge between SWJ-DP and APB bus which translate the Debug request to APB bus.
The DAP provides an internal ROM table connected to the master Debug APB port of the APB-Mux. The Debug ROM table is loaded at address 0x00000000 and 0x80000000 of this bus and is accessible from both APB-AP and the system APB input. Bit[31] of the address bus is not connected to the ROM Table, ensuring that both views read the same value. The ROM table stores the locations of the components on the Debug APB.
More information please refer to the document CoreSight_DAPLite_TRM.pdf for the debug detail description.

9.4 Register Description

Please refer to the document CoreSight_DAPLite_TRM.pdf for the debug detail description.

9.5 Interface Description

9.5.1 DAP SWJ-DP Interface

The following figure is the DAP SWJ-DP interface, the SWJ-DP is a combined JTAG-DP and SW-DP that enable you connect either a Serial Wire Debug(SWJ) to JTAG probe to a target.

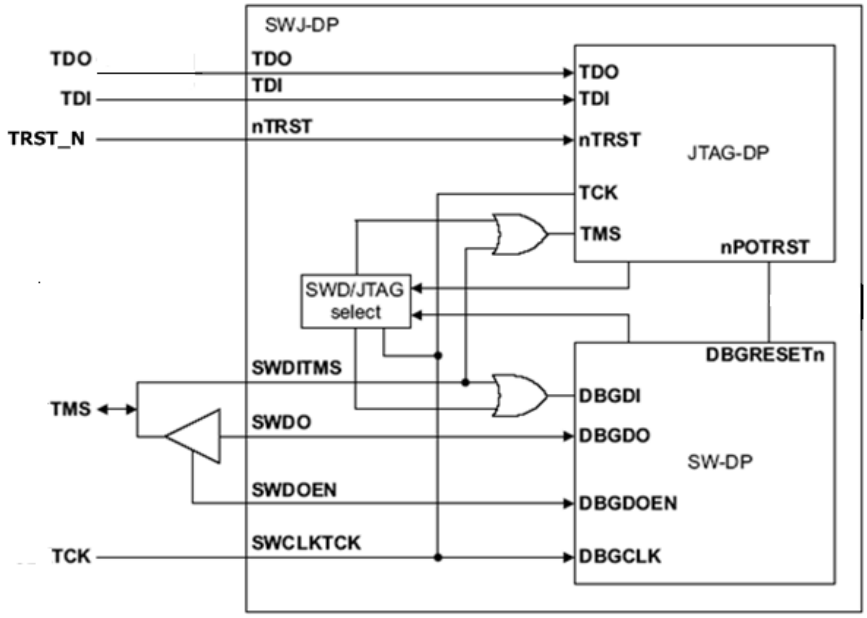

Fig. 9-2 DAP SWJ interface

9.5.2 DAP SW-DP Interface

This implementation is taken from ADIv5.1 and operates with a synchronous serial interface. This uses a single bidirectional data signal, and a clock signal.
The figure below describes the interaction between the timing of transactions on the serial wire interface, and the DAP internal bus transfers. It shows when the target responds with a WAIT acknowledgement.

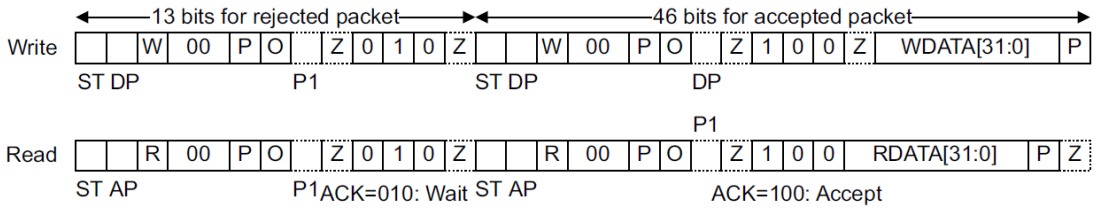

Fig. 9-3 SW-DP acknowledgement timing

Table 9-1 DAP-Lite Interface Description

Module pin	Dir	Pad name	IOMUX
jtag_tckm0	I	SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[11:8] = 4'h9
jtag_tmsm0	I/O	SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/CAN1_TX_M0/I3C1_SDA_M1/GPIO2_A3_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[15:12] = 4'h9
jtag_tckm1	I	UART0_TX_M0/JTAG_TCK_M1/GPIO0_D4_u	PMU1_IOC_GPIO0D_IOMUX_SEL_H[3:0] = 4'ha
jtag_tmsm1	I/O	UART0_RX_M0/JTAG_TMS_M1/GPIO0_D5_u	PMU1_IOC_GPIO0D_IOMUX_SEL_H[7:4] = 4'ha

By default, jtag_tckm0 and jtag_tmsm0 are forced to connect to corresponding io pad, we don't need to set IOMUX again.

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Chapter 10 Share Memory (SHRM)

10.1 Overview

System SRAM is a non-coherence cache of SOC. SHRM supports multi-set of AXI4 interface for masters to access System SRAM. SHRM exchanges data between SRAM and AXI bus and transforms AXI read-write operations to SRAM read-write operations. All masters connected to the SHRM can share the SRAM fairly.

SHRM supports the following features:

- Interface Type
  - Support AXI4 interface
  - Support 2-set AXI4 interface
  - Support 256bit data width
- Operation Type
  - Support FIXED, INCR and WRAP operation type
  - Support all AxSize less than data width
  - Support AxLen inside {[0:15]} for FIXED, {[0:255]} for INCR and {0,1,3,7,15} for WRAP
  - Support outstanding read-write operation for each master(16 deep)
  - Support sequential execution and response in read and write channel
  - Support read-write data consistence check in a master, but no support between different masters
- SRAM specification
  - Support 512KB and etc. size of SRAM
  - Support 4-bank SRAM for high bandwidth

10.2 Block Diagram

SHRM comprises with:

- AXI Slave: AXI Slave Interface and AXI to SRAM operation transform
- ARBITER : Arbiter a operation to SRAM between all read-write channel
- SRAM : storage space of SHRM

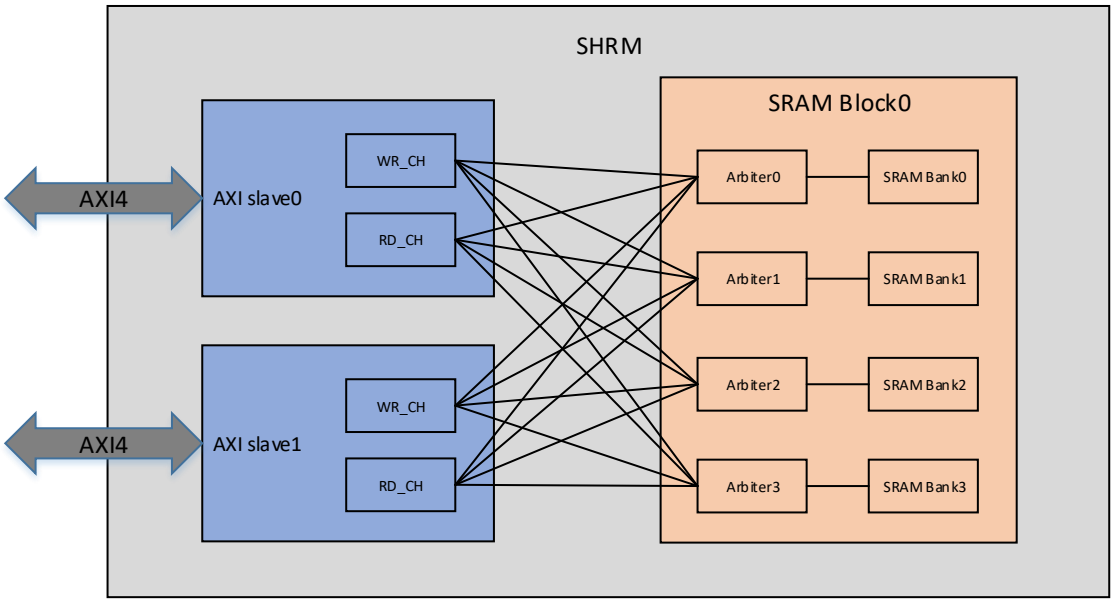

Fig. 10-1 SHRM Block Diagram

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10.3 Function Description

10.3.1 AXI Slave

AXI Slave supports a AXI4 slave interface to connect the AXI4 master and receives the read-write operations from master. AXI Slave use CMD FIFO to buffer the read-write operations from master and then transform the AXI4 operation to SRAM operation orderly. Before a read operation pushed into CMD FIFO, AXI Slave will check all address space of write operation unfinished in CMD FIFO. If there is no address conflict, AXI Slave will push the read operation into CMD FIFO, otherwise AXI Slave will block the read channel until conflict release.

10.3.2 Arbiter

Arbiter supports read-write channel of all AXI Slaves asking request to SRAM simultaneously. Arbiter use Round Robin method to grant a channel while other channel wait until it is granted. Arbiter choose the granted address and data and send to SRAM.

10.3.3 SRAM

SRAM uses multi blocks and multi banks construction to improve bandwidth and reduce address conflict. The higher bit of address will use to choose the block of SRAM, and the lower bit of address will use to choose the bank of SRAM.

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Chapter 11 Cache Coherent Interconnect (CCI500)

11.1 Overview

The CCI-500 is a programmable high bandwidth interconnect that enables hardware-coherent systems. Hardware-managed coherency can improve system performance and reduce system power by sharing onchip data. Managing coherency in hardware has the following benefits:

- Reduces external memory accesses
- Reduces the software overhead and complexity
- Enables use of big.LITTLE processing with multiple processor clusters

Also, RK3576 implements the CoreLink CPE-425 Coherent PCIe Extension, It enables a PCIe root complex or endpoint to operate with hardware IO coherency without deadlock.

11.1.1 Features

- Data coherency between little and big cluster
- Input and Output (IO) coherency with PCIe/GMAC/SATA/USB by ACE-Lite slave0
- Crossbar interconnect functionality between the masters and three slaves
- A snoop filter to reduce snoop power and improve performance for snoop misses
- DVM message transport between masters for communication between MMUs
- Quality of Service (QoS) features for shaping traffic profiles
- A Performance Monitoring Unit (PMU) to count performance-related events
- Support for ARM TrustZone® to provide Secure, Non-secure, and protected states
- A Programmers View (PV) to control coherency and interconnect functionality

11.2 Block Diagram

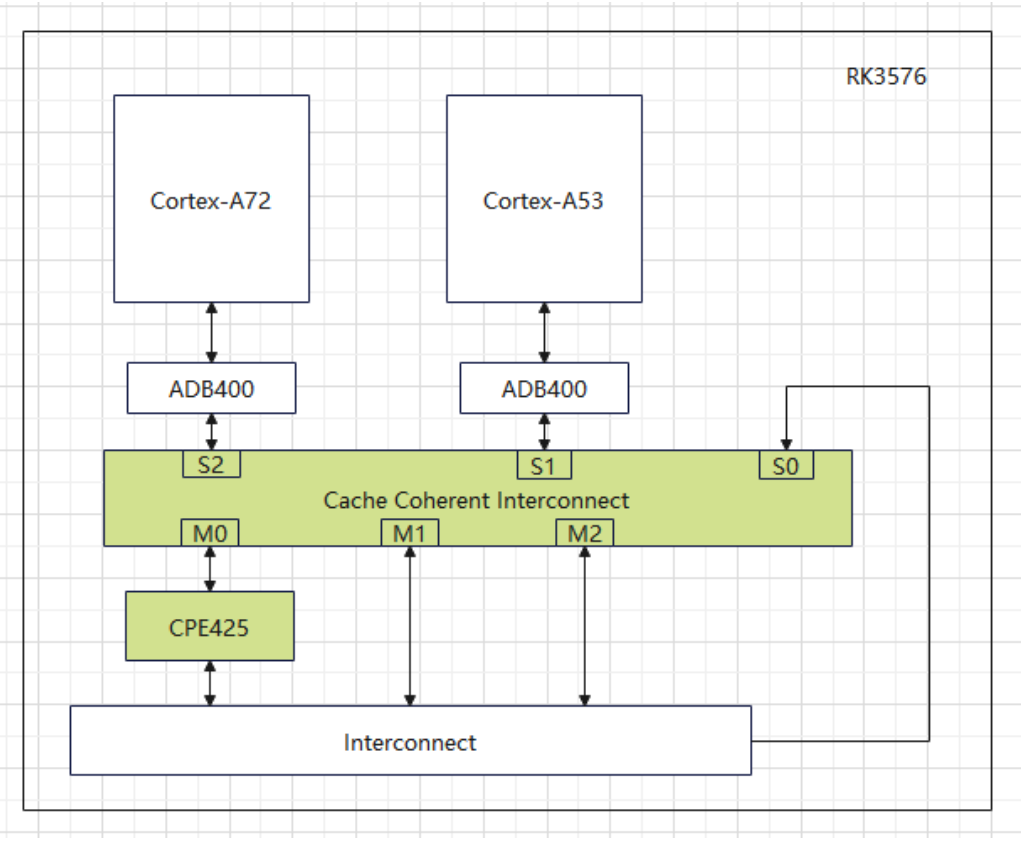

Fig. 11-1 CCI System structure

11.3 Function Description

- Please refer to the document corelink_cci500_cache_coherent_interconnect_technical_reference_manual_100023_0100_01_en.pdf for the detail function description
- Please refer to the document DTO0044B_cpe425_r0p1_to.pdf for the detail function description

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Chapter 12 DMA Controller (DMAC)

12.1 Overview

This device supports 3 Direct Memory Access (DMA) Controller. DMAC0/1/2 support transfers between memory and memory, peripheral and memory. DMAC0/1/2 is under Non-secure state after reset, and the Secure state can be changed by configurable SGRF module.

DMAC supports the following features:

- DMAC0 Supports 28 peripheral requests
- DMAC1 Supports 25 peripheral requests
- DMAC2 Supports 26 peripheral requests
- Up to 64 bits data size
- 8 channel at the same time
- Up to burst 16
- 16 interrupts output and 1 abort output
- Supports 128 MFIFO depth

DMAC supports incrementing-address burst and fixed-address burst. But in the case of access to SPI and UART at byte or half word size, DMAC only supports fixed-address burst and the address must be aligned to word.

12.2 Block Diagram

Following figure shows the block diagram of DMAC.

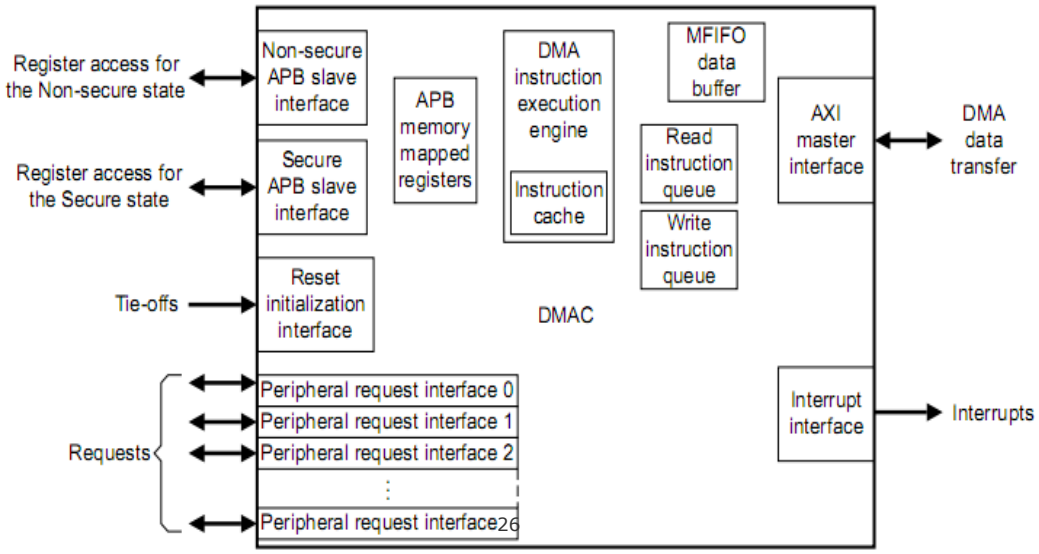

Fig. 12-1 Block Diagram of DMAC

As the DMAC supports TrustZone technology, so dual APB interfaces enable the operation of the DMAC to be partitioned into the Secure state and Non-secure state. You can use the APB interfaces to access status registers and also directly execute instructions in the DMAC. The default interface after reset is Non-secure APB interface.

12.3 Function Description

12.3.1 Introduction

The DMAC contains an instruction processing block that enables it to process program code that controls a DMA transfer. The program code is stored in a region of system memory that the DMAC accesses using its AXI interface. The DMAC stores instructions temporarily in a cache. It supports 8 channels, each channel capable of supporting a single concurrent thread of DMA operation. In addition, a single DMA manager thread exists, and you can use it to initialize the DMA channel threads. The DMAC executes up to one instruction for each AXI clock cycle. To ensure that it regularly executes each active thread, it alternates by processing the DMA manager thread and then a DMA channel thread. It uses a round-robin

process when selecting the next active DMA channel thread to execute.
The DMAC uses variable-length instructions that consist of one to six bytes. It provides a separate Program Counter (PC) register for each DMA channel. When a thread requests an instruction from an address, the cache performs a look-up. If a cache hit occurs, then the cache immediately provides the data. Otherwise, the thread is stalled while the DMAC uses the AXI interface to perform a cache line fill. If an instruction is greater than 4 bytes, or spans the end of a cache line, the DMAC performs multiple cache accesses to fetch the instruction.
When a cache line fill is in progress, the DMAC enables other threads to access the cache, but if another cache miss occurs, this stalls the pipeline until the first line fill is complete.
When a DMA channel thread executes a load or store instruction, the DMAC adds the instruction to the relevant read or write queue. The DMAC uses these queues as an instruction storage buffer prior to it issuing the instructions on the AXI bus. The DMAC also contains a Multi First-In-First-Out (MFIFO) data buffer that it uses to store data that it reads, or writes, during a DMA transfer.

12.3.2 Operating states

Following figure shows the operating states for the DMA manager thread and DMA channel threads.

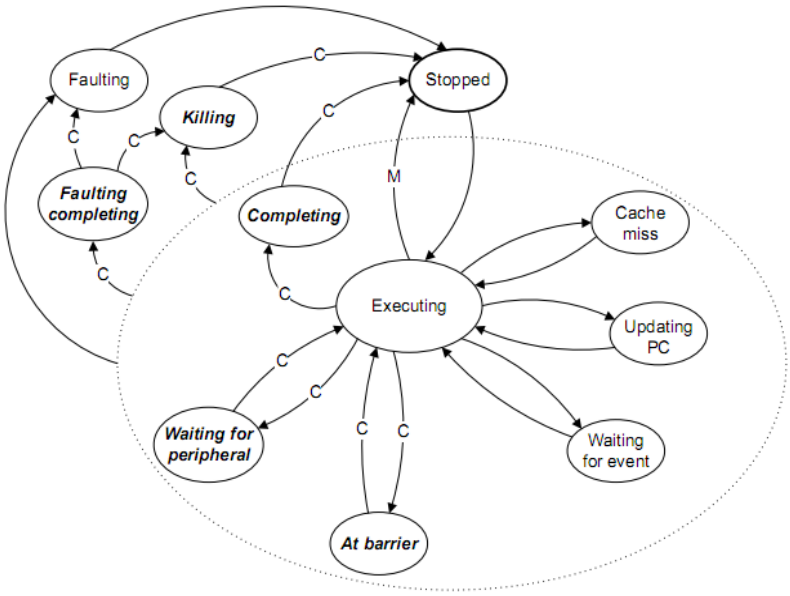

Fig. 12-2 DMAC Operation State

Notes: arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:
C DMA channel threads only.
M DMA manager thread only.

After the DMAC exits from reset, it sets all DMA channel threads to the stopped state, and DMA manager thread moves to the Stopped state.

12.4 Register Description

12.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
DMAC0_S	0x2AB80000
DMAC0_NS	0x2AB90000
DMAC1_S	0x2ABA0000
DMAC1_NS	0x2ABB0000
DMAC2_S	0x2ABC0000
DMAC2_NS	0x2ABD0000

12.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DMA_DSR	0x0000	W	0x00000200	DMA Manager Status Register
DMA_DPC	0x0004	W	0x00000000	DMA Program Counter Register
DMA_INTEN	0x0020	W	0x00000000	Interrupt Enable Register
DMA_EVENT_RIS	0x0024	W	0x00000000	Event-Interrupt Raw Status Register
DMA_INTMIS	0x0028	W	0x00000000	Interrupt Status Register
DMA_INTCLR	0x002C	W	0x00000000	Interrupt Clear Register
DMA_FSRD	0x0030	W	0x00000000	Fault Status DMA Manager Register
DMA_FSRC	0x0034	W	0x00000000	Fault Status DMA Channel Register
DMA_FTRD	0x0038	W	0x00000000	Fault Type DMA Manager Register
DMA_FTR0	0x0040	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR1	0x0044	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR2	0x0048	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR3	0x004C	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR4	0x0050	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR5	0x0054	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR6	0x0058	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR7	0x005C	W	0x00000000	Fault Type DMA Channel Register
DMA_CSR0	0x0100	W	0x00000000	Channel Status Registers
DMA_CPC0	0x0104	W	0x00000000	Channel Program Counter Registers
DMA_CSR1	0x0108	W	0x00000000	Channel Status Registers
DMA_CPC1	0x010C	W	0x00000000	Channel Program Counter Registers
DMA_CSR2	0x0110	W	0x00000000	Channel Status Registers
DMA_CPC2	0x0114	W	0x00000000	Channel Program Counter Registers
DMA_CSR3	0x0118	W	0x00000000	Channel Status Registers
DMA_CPC3	0x011C	W	0x00000000	Channel Program Counter Registers
DMA_CSR4	0x0120	W	0x00000000	Channel Status Registers
DMA_CPC4	0x0124	W	0x00000000	Channel Program Counter Registers
DMA_CSR5	0x0128	W	0x00000000	Channel Status Registers
DMA_CPC5	0x012C	W	0x00000000	Channel Program Counter Registers
DMA_CSR6	0x0130	W	0x00000000	Channel Status Registers
DMA_CPC6	0x0134	W	0x00000000	Channel Program Counter Registers
DMA_CSR7	0x0138	W	0x00000000	Channel Status Registers
DMA_CPC7	0x013C	W	0x00000000	Channel Program Counter Registers
DMA_SAR0	0x0400	W	0x00000000	Source Address Registers
DMA_DAR0	0x0404	W	0x00000000	Destination Address Registers
DMA_CCR0	0x0408	W	0x00000000	Channel Control Registers
DMA_LC0_0	0x040C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_0	0x0410	W	0x00000000	Loop Counter 1 Registers
DMA_SAR1	0x0420	W	0x00000000	Source Address Registers
DMA_DAR1	0x0424	W	0x00000000	Destination Address Registers

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Name	Offset	Size	Reset Value	Description
DMA_CCR1	0x0428	W	0x00000000	Channel Control Registers
DMA_LC0_1	0x042C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_1	0x0430	W	0x00000000	Loop Counter 1 Registers
DMA_SAR2	0x0440	W	0x00000000	Source Address Registers
DMA_DAR2	0x0444	W	0x00000000	Destination Address Registers
DMA_CCR2	0x0448	W	0x00000000	Channel Control Registers
DMA_LC0_2	0x044C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_2	0x0450	W	0x00000000	Loop Counter 1 Registers
DMA_SAR3	0x0460	W	0x00000000	Source Address Registers
DMA_DAR3	0x0464	W	0x00000000	Destination Address Registers
DMA_CCR3	0x0468	W	0x00000000	Channel Control Registers
DMA_LC0_3	0x046C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_3	0x0470	W	0x00000000	Loop Counter 1 Registers
DMA_SAR4	0x0480	W	0x00000000	Source Address Registers
DMA_DAR4	0x0484	W	0x00000000	Destination Address Registers
DMA_CCR4	0x0488	W	0x00000000	Channel Control Registers
DMA_LC0_4	0x048C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_4	0x0490	W	0x00000000	Loop Counter 1 Registers
DMA_SAR5	0x04A0	W	0x00000000	Source Address Registers
DMA_DAR5	0x04A4	W	0x00000000	Destination Address Registers
DMA_CCR5	0x04A8	W	0x00000000	Channel Control Registers
DMA_LC0_5	0x04AC	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_5	0x04B0	W	0x00000000	Loop Counter 1 Registers
DMA_SAR6	0x04C0	W	0x00000000	Source Address Registers
DMA_DAR6	0x04C4	W	0x00000000	Destination Address Registers
DMA_CCR6	0x04C8	W	0x00000000	Channel Control Registers
DMA_LC0_6	0x04CC	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_6	0x04D0	W	0x00000000	Loop Counter 1 Registers
DMA_SAR7	0x04E0	W	0x00000000	Source Address Registers
DMA_DAR7	0x04E4	W	0x00000000	Destination Address Registers
DMA_CCR7	0x04E8	W	0x00000000	Channel Control Registers
DMA_LC0_7	0x04EC	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_7	0x04F0	W	0x00000000	Loop Counter 1 Registers
DMA_DBGSTATUS	0x0D00	W	0x00000000	Debug Status Register
DMA_DBGCMD	0x0D04	W	0x00000000	Debug Command Register
DMA_DBGINST0	0x0D08	W	0x00000000	Debug Instruction-0 Register
DMA_DBGINST1	0x0D0C	W	0x00000000	Debug Instruction-1 Register
DMA_CR0	0x0E00	W	0x001FF075	Configuration Register 0
DMA_CR1	0x0E04	W	0x000000B5	Configuration Register 1
DMA_CR2	0x0E08	W	0x00000000	Configuration Register 2
DMA_CR3	0x0E0C	W	0x0000FFFF	Configuration Register 3
DMA_CR4	0x0E10	W	0xFFFFFFFF	Configuration Register 4
DMA_CRDn	0x0E14	W	0x07FF7F73	Configuration Register
DMA_WD	0x0E80	W	0x00000000	DMA Watchdog Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

12.4.3 Detail Registers Description

DMA_DSR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9	RO	0x1	dns 1'b0: DMA manager operates in the Secure state 1'b1: DMA manager operates in the Non-secure state
8:4	RO	0x00	wakeup_event 5'b00000: event[0] 5'b00001: event[1] 5'b00010: event[2] 5'b11111: event[31]
3:0	RO	0x0	dma_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101-4'b1110: reserved 4'b1111: Faulting

DMA_DPC

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_mgr Program counter for the DMA manager thread

DMA_INTEN

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	event_irq_select Bit [N] 1'b0: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit [N] to 0 if your system design does not use irq[N] to signal an interrupt request 1'b1: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets irq[N] HIGH. Set bit [N] to 1 if your system designer requires irq[N] to signal an interrupt request

DMA_EVENT_RIS

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dmasev_active Bit [N] 1'b0: Event N is inactive or irq[N] is LOW 1'b1: Event N is active or irq[N] is HIGH

DMA_INTMIS

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	irq_status Bit [N] 1'b0: Interrupt N is inactive and therefore irq[N] is LOW 1'b1: Interrupt N is active and therefore irq[N] is HIGH

DMA_INTCLR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	irq_clr Bit [N] 1'b0: The status of irq[N] does not change 1'b1: The DMAC sets irq[N] LOW if the INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of irq[N] does not change

DMA_FSRD

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	fs_mgr 1'b0: the DMA manager thread is not in the Faulting state 1'b1: the DMA manager thread is in the Faulting state

DMA_FSRC

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	fault_status Bit [N] 1'b0: No fault is present on DMA channel N. 1'b1: DMA channel N is in the Faulting or Faulting completing state

DMA_FTRD

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface
29:17	RO	0x0000	reserved
16	RO	0x0	instr_fetch_err performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response
15:6	RO	0x000	reserved
5	RO	0x0	mgr_evnt_err 1'b0: the DMA manager has appropriate security to execute DMAWFE or DMASEV 1'b1: a DMA manager thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt
4	RO	0x0	dmago_err 1'b0: the DMA manager has appropriate security to execute DMAGO 1'b1: a DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state

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Bit	Attr	Reset Value	Description
3:2	RO	0x0	reserved
1	RO	0x0	operand_invalid the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand
0	RW	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction

DMA_FTR0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

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Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR1

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.

Bit	Attr	Reset Value	Description
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.

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Bit	Attr	Reset Value	Description
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR2

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.

Bit	Attr	Reset Value	Description
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR3

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR4

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved

Bit	Attr	Reset Value	Description
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.

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Bit	Attr	Reset Value	Description
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR5

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR6

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.

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Bit	Attr	Reset Value	Description
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR7

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.

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Bit	Attr	Reset Value	Description
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_CSR0

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC0

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 0 thread

DMA_CSR1

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC1

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 1 thread

DMA_CSR2

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC2

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 2 thread

DMA_CSR3

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31

Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC3

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 3 thread

DMA_CSR4

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing

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Bit	Attr	Reset Value	Description
			b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC4

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 4 thread

DMA_CSR5

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC5

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 5 thread

DMA_CSR6

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC6

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 6 thread

DMA_CSR7

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set

Bit	Attr	Reset Value	Description
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC7

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 7 thread

DMA_SAR0

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 0

DMA_DAR0

Address: **Operational Base** + offset (0x0404)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 0

DMA_CCR0

Address: **Operational Base** + offset (0x0408)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_0

Address: **Operational Base** + offset (0x040C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_0

Address: **Operational Base** + offset (0x0410)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR1

Address: **Operational Base** + offset (0x0420)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 1

DMA_DAR1

Address: **Operational Base** + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 1

DMA_CCR1

Address: **Operational Base** + offset (0x0428)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.

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Bit	Attr	Reset Value	Description
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_1

Address: **Operational Base** + offset (0x042C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_1

Address: **Operational Base** + offset (0x0430)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR2

Address: **Operational Base** + offset (0x0440)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 2

DMA_DAR2

Address: **Operational Base** + offset (0x0444)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 2

DMA_CCR2

Address: **Operational Base** + offset (0x0448)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.

Bit	Attr	Reset Value	Description
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.

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Bit	Attr	Reset Value	Description
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_2

Address: **Operational Base** + offset (0x044C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_2

Address: **Operational Base** + offset (0x0450)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR3

Address: **Operational Base** + offset (0x0460)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 3

DMA_DAR3

Address: **Operational Base** + offset (0x0464)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 3

DMA_CCR3

Address: **Operational Base** + offset (0x0468)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.

Bit	Attr	Reset Value	Description
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_3

Address: **Operational Base** + offset (0x046C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_3

Address: **Operational Base** + offset (0x0470)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR4

Address: **Operational Base** + offset (0x0480)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 4

DMA_DAR4

Address: **Operational Base** + offset (0x0484)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 4

DMA_CCR4

Address: **Operational Base** + offset (0x0488)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_4

Address: **Operational Base** + offset (0x048C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_4

Address: **Operational Base** + offset (0x0490)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR5

Address: **Operational Base** + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 5

DMA_DAR5

Address: **Operational Base** + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 5

DMA_CCR5

Address: **Operational Base** + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_5

Address: **Operational Base** + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_5

Address: **Operational Base** + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR6

Address: **Operational Base** + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 6

DMA_DAR6

Address: **Operational Base** + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 6

DMA_CCR6

Address: **Operational Base** + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.

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Bit	Attr	Reset Value	Description
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_6

Address: **Operational Base** + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_6

Address: **Operational Base** + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR7

Address: **Operational Base** + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 7

DMA_DAR7

Address: **Operational Base** + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 7

DMA_CCR7

Address: **Operational Base** + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.

Bit	Attr	Reset Value	Description
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.

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Bit	Attr	Reset Value	Description
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_7

Address: **Operational Base** + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_7

Address: **Operational Base** + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_DBGSTATUS

Address: **Operational Base** + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	dbgstatus 1'b0: idle 1'b1: busy

DMA_DBGCMD

Address: **Operational Base** + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	WO	0x0	dbgcmd 2'b00: execute the instruction that the DBGINST [1:0] Registers contain 2'b01: reserved 2'b10: reserved 2'b11: reserved

DMA_DBGINST0

Address: **Operational Base** + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	instruction_byte1 Instruction byte 1
23:16	WO	0x00	instruction_byte0 Instruction byte 0
15:11	RO	0x00	reserved
10:8	WO	0x0	channel_number 3'b000: DMA channel 0 3'b001: DMA channel 1 3'b010: DMA channel 2 3'b111: DMA channel 7
7:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	WO	0x0	debug_thread 1'b0: DMA manager thread 1'b1: DMA channel

DMA_DBGINST1

Address: **Operational Base** + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	instruction_byte5 Instruction byte 5
23:16	WO	0x00	instruction_byte4 Instruction byte 4
15:8	WO	0x00	instruction_byte3 Instruction byte 3
7:0	WO	0x00	instruction_byte2 Instruction byte 2

DMA_CR0

Address: **Operational Base** + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:17	RO	0x0f	num_events 5'b00000: 1 interrupt output, irq[0] 5'b00001: 2 interrupt outputs, irq[1:0] 5'b00010: 3 interrupt outputs, irq[2:0] 5'b11111: 32 interrupt outputs, irq[31:0]
16:12	RO	0x1f	num_periph_req 5'b00000: 1 peripheral request interface 5'b00001: 2 peripheral request interfaces 5'b00010: 3 peripheral request interfaces 5'b11111: 32 peripheral request interfaces
11:7	RO	0x00	reserved
6:4	RO	0x7	num_chnls 3'b000: 1 DMA channel 3'b001: 2 DMA channels 3'b010: 3 DMA channels 3'b111: 8 DMA channels
3	RO	0x0	reserved
2	RO	0x1	mgr_ns_at_rst 1'b0: boot_manager_ns was LOW 1'b1: boot_manager_ns was HIGH
1	RO	0x0	boot_en 1'b0: boot_from_pc was LOW 1'b1: boot_from_pc was HIGH
0	RO	0x1	periph_req 1'b0: the DMAC does not provide a peripheral request interface 1'b1: the DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies

DMA_CR1

Address: **Operational Base** + offset (0x0E04)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RO	0xb	num_i_cache_lines 4'b0000: 1 i-cache line 4'b0001: 2 i-cache lines 4'b0010: 3 i-cache lines 4'b1111: 16 i-cache lines
3	RO	0x0	reserved
2:0	RO	0x5	i_cache_len 3'b000-3'b001: reserved 3'b010: 4 bytes 3'b011: 8 bytes 3'b100: 16 bytes 3'b101: 32 bytes 3'b110-3'b111: reserved

DMA_CR2

Address: **Operational Base** + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	boot_addr Provides the value of boot_addr[31:0] when the DMAC exited from reset

DMA_CR3

Address: **Operational Base** + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000ffff	ins Bit [N] 1'b0: Assigns event<N> or irq[N] to the Secure state 1'b1: Assigns event<N> or irq[N] to the Non-secure state

DMA_CR4

Address: **Operational Base** + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:0	RO	0xffffffff	pns Bit [N] 1'b0: Assigns peripheral request interface N to the Secure state 1'b1: Assigns peripheral request interface N to the Non-secure state

DMA_CRDn

Address: **Operational Base** + offset (0x0E14)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RO	0x07f	data_buffer_dep 10'b000000000: 1 line 10'b000000001: 2 lines 10'b111111111: 1024 lines
19:16	RO	0xf	rd_q_dep 4'b0000: 1 line 4'b0001: 2 lines 4'b1111: 16 lines
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RO	0x7	rd_cap 3'b000: 1 3'b001: 2 3'b111: 8
11:8	RO	0xf	wr_q_dep 4'b0000: 1 line 4'b0001: 2 lines 4'b1111: 16 lines
7	RO	0x0	reserved
6:4	RO	0x7	wr_cap 3'b000: 1 3'b001: 2 3'b111: 8
3	RO	0x0	reserved
2:0	RO	0x3	data_width 3'b000: reserved 3'b001: reserved 3'b010: 32-bit 3'b011: 64-bit 3'b100: 128-bit 3'b101-3'b111: reserved

DMA_WD

Address: **Operational Base** + offset (0x0E80)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	wd_irq_only 1'b0: the DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH 1'b1: the DMAC sets irq_abort HIGH

12.5 Timing Diagram

Following picture shows the relationship between dma_req and dma_ack.

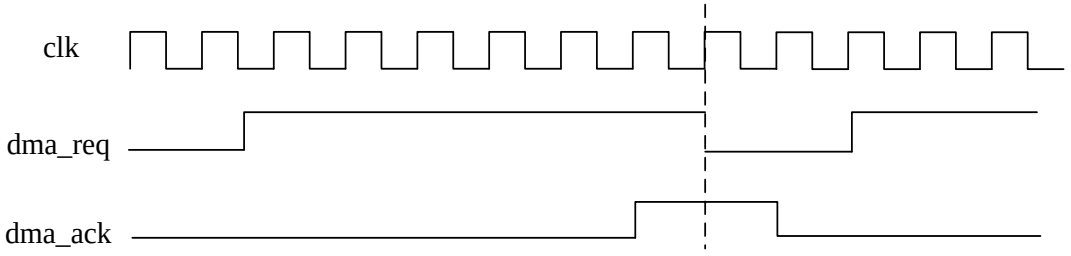

Fig. 12-3 DMAC Request and Acknowledge Timing

12.6 Application Notes

12.6.1 Using the APB Slave Interfaces

You must ensure that you use the appropriate APB interface, depending on the security state in which the boot_manager_ns initializes the DMAC to operate. For example, if the DMAC is in the secure state, you must issue the instruction using the secure APB interface, otherwise the DMAC ignores the instruction. You can use the secure APB interface, or the non-secure APB interface, to start or restart a DMA channel when the DMAC is in the Non-

secure state.

The necessary steps to start a DMA channel thread using the debug instruction registers as following:
1. Create a program for the DMA channel.
2. Store the program in a region of system memory.
3. Poll the DMAC_DBGSTATUS Register to ensure that debug is idle, that is, the dbgstatus bit is 0.
4. Write to the DMAC_DBGINST0 Register and enter the:
   - Instruction byte 0 encoding for DMAGO.
   - Instruction byte 1 encoding for DMAGO.
   - Debug thread bit to 0. This selects the DMA manager thread.
5. Write to the DBGINST1 Register with the DMAGO instruction byte [5:2] data, see Debug Instruction-1 Register o. You must set these four bytes to the address of the first instruction in the program that was written to system memory in step 2.
6. Writing zero to the DMAC_DBGCMD Register. The DMAC starts the DMA channel thread and sets the dbgstatus bit to 1.

12.6.2 Security Usage

DMA manager thread is in the secure state

If the DNS bit is 0, the DMA manager thread operates in the secure state and it only performs secure instruction fetches. When a DMA manager thread in the secure state processes:

DMAGO

It uses the status of the ns bit, to set the security state of the DMA channel thread by writing to the CNS bit for that channel.

DMAWFE

It halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit.

DMASEV

It sets the corresponding bit in the INT_EVENT_RIS Register, irrespective of the security state of the corresponding INS bit.

DMA manager thread is in the Non-secure state

If the DNS bit is 1, the DMA manager thread operates in the Non-secure state, and it only performs non-secure instruction fetches. When a DMA manager thread in the Non-secure state processes:

DMAGO

The DMAC uses the status of the ns bit, to control if it starts a DMA channel thread. If:
ns = 0
The DMAC does not start a DMA channel thread and instead it:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager
3. Sets the dmago_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.
ns = 1
The DMAC starts a DMA channel thread in the Non-secure state and programs the CNS bit to be non-secure.

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to

control if it waits for the event. If:
INS = 0
The event is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.
INS = 1
The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV
The DMAC uses the status of the corresponding INS bit, in the CR3Register, to control if it creates the event-interrupt. If:
INS = 0
The event-interrupt resource is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.
INS = 1
The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMA channel thread is in the secure state
When the CNS bit is 0, the DMA channel thread is programmed to operate in the Secure state and it only performs secure instruction fetches.
When a DMA channel thread in the secure state processes the following instructions:

DMAWFE
The DMAC halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

DMASEV
The DMAC creates the event-interrupt, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

DMAWFP
The DMAC halts execution of the thread until the peripheral signals a DMA request. When this occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

DMALDP, DMASTP
The DMAC sends a message to the peripheral to communicate that data transfer is complete, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

DMAFLUSHP
The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.
When a DMA channel thread is in the Secure state, it enables the DMAC to perform secure and non-secure AXI accesses.

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DMA channel thread is in the Non-secure state
When the CNS bit is 1, the DMA channel thread is programmed to operate in the Non-secure state and it only performs non-secure instruction fetches.
When a DMA channel thread in the Non-secure state processes the following instructions:

DMAWFE
The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:
INS = 0
The event is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
INS = 1
The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV
The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it creates the event. If:
INS = 0
The event-interrupt resource is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
INS = 1
The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMAWFP
The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it waits for the peripheral to signal a request. If:
PNS = 0
The peripheral is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC halts execution of the thread and waits for the peripheral to signal a request.

DMALDP, DMASTP
The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends an acknowledgement to the peripheral. If:
PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA

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channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC sends a message to the peripheral to communicate when the data transfer is complete.

DMAFLUSHP
The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends a flush request to the peripheral. If:
PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status.
When a DMA channel thread is in the Non-secure state, and a DMAMOV CCR instruction attempts to program the channel to perform a secure AXI transaction, the DMAC:
1. Executes a DMANOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_rdwr_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel thread to the Faulting completing state.

12.6.3 Programming Restrictions

Fixed unaligned bursts
The DMAC does not support fixed unaligned bursts. If you program the following conditions, the DMAC treats this as a programming error:
Unaligned read
- src_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DMAC_SARn(n=0~7) Register contains an address that is not aligned to the size of data that the src_burst_size field contain

Unaligned write
- dst_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DMAC_DARn(n=0~7) Register contains an address that is not aligned to the size of data that the dst_burst_size field contains

Endian swap size restrictions
If you program the endian_swap_size field in the DMAC_CCRn(n=0~7) Register, to enable a DMA channel to perform an endian swap then you must set the corresponding DMAC_SARn(n=0~7) Register and the corresponding DMAC_DARn(n=0~7) Register to contain an address that is aligned to the value that the endian_swap_size field contains.

Updating DMA channel control registers during a DMA cycle restrictions
Prior to the DMAC executing a sequence of DMALD and DMAST instructions, the values you program in to the DMAC_CCRn(n=0~7) Register, DMAC_SARn(n=0~7) Register, and DMAC_DARn(n=0~7) Register control the data byte lane manipulation that the DMAC performs when it transfers the data from the source address to the destination address. You'd better not update these registers during a DMA cycle.

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Resource sharing between DMA channels
DMA channel programs share the MFIFO data storage resource. You must not start a set of concurrently running DMA channel programs with a resource requirement that exceeds the configured size of the MFIFO. If you exceed this limit then the DMAC might lock up and generate a Watchdog abort.

12.6.4 Unaligned Transfers

For a configuration with more than one channel, if any of channels 1 to 7 is performing transfers between certain types of misaligned source and destination addresses, then the output data may be corrupted by the action of channel 0.

Data corruption might occur if all of the following are true:
1. Two beats of AXI read data are received for one of channels 1 to 7.
2. Source and destination address alignments mean that each read data beat is split across two lines in the data buffer (see Splitting data, below).
3. There is one idle cycle between the two read data beats.
4. Channel 0 performs an operation that updates channel control information during this idle cycle (see Updates to channel control information, below).

Splitting data
Depending upon the programmed values for the DMA transfer, one beat of read data from the AXI interface need to be split across two lines in the internal data buffer. This occurs when the read data beat contains data bytes which will be written to addresses that wrap around at the AXI interface data width, so that these bytes could not be transferred by a single AXI write data beat of the full interface width.

Most applications of DMA do not split data in this way, so are NOT vulnerable to data corruption from this defect.

The following cases are NOT vulnerable to data corruption because they do not split data:
- Byte lane offset between source and destination addresses is 0 when source and destination addresses have the same byte lane alignment, the offset is 0 and a wrap operation that splits data cannot occur.
- Byte lane offset between source and destination addresses is a multiple of source size.

Table 12-1 Source Size in DMAC_CCRn

Source size in DMAC_CCRn	Allowed offset between DMAC_SARn and DMAC_DARn
SS8	any offset allowed.
SS16	0,2,4,6,8,10,12,14
SS32	0,4,8,12
SS64	0,8

12.6.5 Interrupt Sharing between Channels

As the DMAC does not record which channel (or list of channels) have asserted an interrupt. So it will depend on your program and whether any of the visible information for that program can be used to determine progress, and help identify the interrupt source. There are 4 likely information sources that can be used to determine the progress made by a program:
- Program counter (PC)
- Source address
- Destination address
- Loop counters (LC)

For example, a program might emit an interrupt each time that it iterates around a loop. In this case, the interrupt service routine (ISR) would need to store the loop value of each channel when it is called, and then compare against the new value when it is next called. A change in value would indicate that the program has progressed.
The ISR must be carefully written to ensure that no interrupts are lost. The sequence of

operations is as follows:
1. Disable interrupts
2. Immediately clear the interrupt in DMA-330
3. Check the relevant registers for both channels to determine which must be serviced
4. Take appropriate action for the channels
5. Re-enable interrupts and exit ISR

12.6.6 Instruction Sets

Table 12-2 DMAC Instruction Sets

Mnemonic	Instruction	Thread Usage
DMAADDH	Add Halfword	C
DMAEND	End	M/C
DMAFLUSHP	Flush and notify Peripheral	C
DMAGO	Go	M
DMAKILL	Kill	C
DMALD	Load	C
DMALDP	Load Peripheral	C
DMALP	Loop	C
DMALPEND	Loop End	C
DMALPFE	Loop Forever	C
DMAMOV	Move	C
DMANOP	No operation	M/C
DMARMB	Read Memory Barrier	C
DMASEV	Send Event	M/C
DMAST	Store	C
DMASTP	Store and notify Peripheral	C
DMASTZ	Store Zero	C
DMAWFE	Wait For Event M	M/C
DMAWFP	Wait For Peripheral	C
DMAWMB	Write Memory Barrier	C
DMAADNH	Add Negative Halfword	C

Notes: Thread usage: C=DMA channel, M=DMA manager

12.6.7 Assembler Directives

In this document, only DMMADNH instruction is took as an example to show the way the instruction assembled. For the other instructions, please refer to pl330_trm.pdf.

DMAADNH

Add Negative Halfword adds an immediate negative 16-bit value to the DMAC_SARn(n=0~7) Register or DMAC_DARn(n=0~7) Register, for the DMA channel thread. This enables the DMAC to support 2D DMA operations, or reading or writing an area of memory in a different order to naturally incrementing addresses. See Source Address Registers and Destination Address Registers.

The immediate unsigned 16-bit value is one-extended to 32 bits, to create a value that is the two's complement representation of a negative number between -65536 and -1, before the DMAC adds it to the address using 32-bit addition. The DMAC discards the carry bit so that addresses wrap from 0xFFFFFFFF to 0x00000000. The net effect is to subtract between 65536 and 1 from the current value in the Source or Destination Address Register.

Following table shows the instruction encoding.

Table 12-3 DMAC Instruction Encoding

Imm[15:8]	Imm[7:0]	0	1	0	1	1	1	ra	0

Assembler syntax

DMAADNH <address_register>, <16-bit immediate>

where:

<address_register>

Selects the address register to use. It must be either:

SAR

DMAC_SARn(n=0~7) Register and sets ra to 0.

DAR

DMAC_DARn(n=0~7) Register and sets ra to 1.

<16-bit immediate>

The immediate value to be added to the <address_register>.

You should specify the 16-bit immediate as the number that is to be represented in the instruction encoding. For example, DMAADNH DAR, 0xFFF0 causes the value 0xFFFFFFF0 to be added to the current value of the Destination Address Register, effectively subtracting 16 from the DAR.

You can only use this instruction in a DMA channel thread.

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Chapter 13 Generic Interrupt Controller (GIC)

13.1 Overview

There is a generic interrupt controller (GIC400) in RK3576 which generates physical interrupts to Cortex-A53/Cortex-A72. It has two interfaces, the distributor interface connects to the interrupt source, and the CPU interface connects to Cortex-A53/Cortex-A72. The details of CPU interface connectivity are shown in the following table.

Table 13-1 CPU Interface Connectivity

CPU Interface Number	Connectivity
CPU interface 0	Cortex-A53 CPU0
CPU interface 1	Cortex-A53 CPU1
CPU interface 2	Cortex-A53 CPU2
CPU interface 3	Cortex-A53 CPU3
CPU interface 4	Cortex-A72 CPU0
CPU interface 5	Cortex-A72 CPU1
CPU interface 6	Cortex-A72 CPU2
CPU interface 7	Cortex-A72 CPU3

It supports the following features:

- Support 480 hardware interrupt inputs
- Support masking of any interrupts
- Support interrupts prioritization
- Support distribution of the interrupts to the target Cortex-A53/Cortex-A72 processor(s)
- Support generation of interrupts by software
- Support security extensions
- Support virtual extension

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13.2 Block Diagram

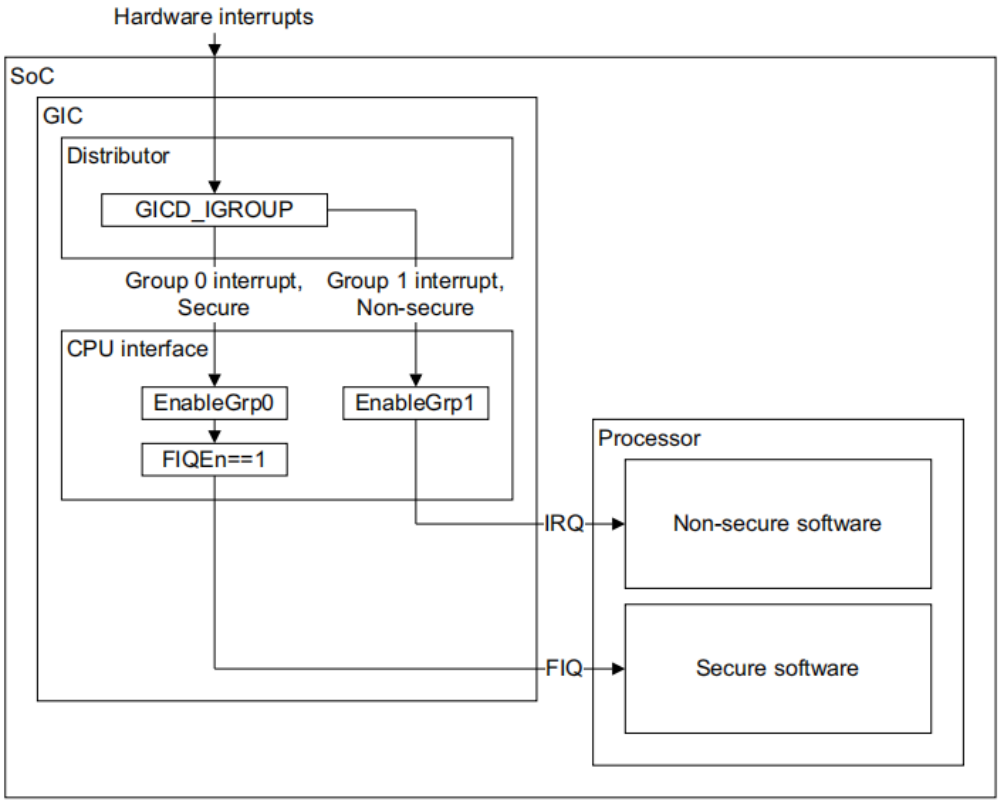

Fig. 13-1 GIC Block Diagram

13.3 Function Description

Please refer to the document IHI0048B_gic_architecture_specification.pdf and GIC400_Technical_Reference_Manual.pdf for the detail function description.

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Chapter 14 TIMER

14.1 Overview

TIMER is a programmable timer peripheral. It is usually used for generating a timing interrupt. There are two types of TIMER which are different in channel number. Both of them can be configured as a count-up or count-down timer.

TIMER supports the following features:

- Support two timer mode: free-running and user-defined
- Support two count mode: count-up and count-down
- Support configuration of loading count value
- Support mask interrupt

14.2 Block Diagram

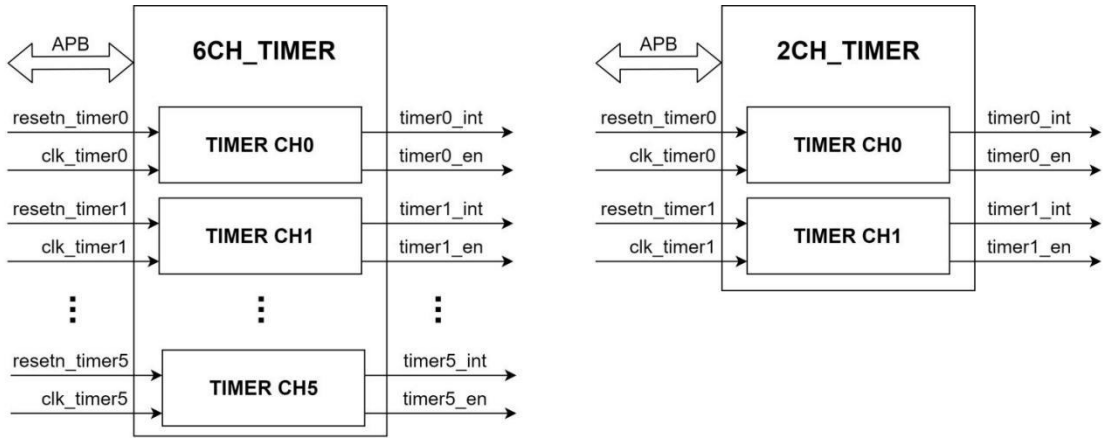

Fig. 14-1 TIMER Block Diagram

The figure above shows the block diagram of TIMER.

14.3 Function Description

14.3.1 TIMER Clock

The frequency of counting clock is switched between 100MHz and 24MHz.

14.3.2 TIMER Mode

- **User-defined Count Mode**

TIMER loads TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_ COUNT0 registers (for count-down TIMER) or zero (for count-up TIMER) as initial value. When the TIMER counts down to 0 (for count-down TIMER) or counts up to the value in TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_ LOAD_ COUNT0 (for count-up TIMER), it will not automatically reload the count value register. User need to disable timer firstly and follow the programming sequence to make timer work again.

- **Free-running Count Mode**

TIMER loads the TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_COUNT0 (for count-down TIMER) or zero (for count-up TIMER) register as initial value. TIMER will automatically reload the count value register, when timer counts down to 0 (for count-down TIMER) or counts up to the value in TIMER_TIMERn_LOAD_ COUNT1 and TIMER_TIMERn_LOAD_COUNT0 (for count-up TIMER).

14.4 Register Description

14.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
TIMER_NS_0-CH0	0x2ACC0000

Name	Base Address
TIMER_NS_0-CH1	0x2ACC1000
TIMER_NS_0-CH2	0x2ACC2000
TIMER_NS_0-CH3	0x2ACC3000
TIMER_NS_0-CH4	0x2ACC4000
TIMER_NS_0-CH5	0x2ACC5000
TIMER_NS_1-CH0	0x2ACD0000
TIMER_NS_1-CH1	0x2ACD1000
TIMER_NS_1-CH2	0x2ACD2000
TIMER_NS_1-CH3	0x2ACD3000
TIMER_NS_1-CH4	0x2ACD4000
TIMER_NS_1-CH5	0x2ACD5000

Operational Base

Name	Base Address
TIMER_S_0-CH0	0x2A4A0000
TIMER_S_0-CH1	0x2A4A1000
TIMER_S_0-CH2	0x2A4A2000
TIMER_S_0-CH3	0x2A4A3000
TIMER_S_0-CH4	0x2A4A4000
TIMER_S_0-CH5	0x2A4A5000
TIMER_S_1-CH0	0x2A4B0000
TIMER_S_1-CH1	0x2A4B1000
TIMER_S_1-CH2	0x2A4B2000
TIMER_S_1-CH3	0x2A4B3000
TIMER_S_1-CH4	0x2A4B4000
TIMER_S_1-CH5	0x2A4B5000

Operational Base

Name	Base Address
PMU_TIMER-CH0	0x27350000
PMU_TIMER-CH1	0x27351000

Operational Base

Name	Base Address
DDR_TIMER-CH0	0x2A050000
DDR_TIMER-CH1	0x2A051000

Operational Base

Name	Base Address
NPU_TIMER-CH0	0x27790000
NPU_TIMER-CH1	0x27791000

14.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TIMER_TIMERn_LOAD_COUNT0	0x0000	W	0x00000000	Low 32 bits value to be loaded into Timer
TIMER_TIMERn_LOAD_COUNT1	0x0004	W	0x00000000	High 32 bits value to be loaded into Timer
TIMER_TIMERn_CURR_VALUE0	0x0008	W	0x00000000	Low 32 bits of current value of Timer
TIMER_TIMERn_CURR_VALUE1	0x000C	W	0x00000000	High 32 bits of current value of Timer
TIMER_TIMERn_CONTROL	0x0010	W	0x00000000	Timer Control Register
TIMER_TIMERn_INTSTATUS	0x0018	W	0x00000000	Timer Interrupt Status Register

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Name	Offset	Size	Reset Value	Description
TIMER_TIMERn_REVISION	0x001C	W	0x2AF60000	Timer Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3 Detail Registers Description

TIMER_TIMERn_LOAD_COUNT0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count0 Load count low bits

TIMER_TIMERn_LOAD_COUNT1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count1 Load count high bits

TIMER_TIMERn_CURR_VALUE0

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	current_value0 Current_cnt_low bits

TIMER_TIMERn_CURR_VALUE1

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	current_value1 Current_cnt_high bits

TIMER_TIMERn_CONTROL

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	count_mode Count mode 1'b0: Count up counter 1'b1: Count down counter
2	RW	0x0	int_en Timer interrupt enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	timer_mode Timer mode 1'b0: Free-running mode 1'b1: User-defined count mode
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

TIMER_TIMERn_INTSTATUS

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	int_pd This register contains the interrupt status for Timer. Write 1 to this register will clear the interrupt.

TIMER_TIMERn_REVISION

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x2af6	svn_revision SVN revision: 16'd10998.
15:9	RO	0x00	reserved
8	RO	0x0	ch_type Indicate the timer count mode 1'b0: Count up counter 1'b1: Count down counter
7:0	RO	0x00	reserved

14.5 Application Notes

14.5.1 Clock and Reset

There are two different clock domain in TIMER: clk_timern and pclk. The frequency of these clocks are as below:

Table 14-1 Clock Source and Frequency

Module	Clock Name	Clock Source	Frequency
TIMER_NS_0	clk_timern(n=0-5)	clk_matrix_100m/ osc_xin	100M/24M
TIMER_NS_1	clk_timern(n=0,3-5)	clk_matrix_100m/ osc_xin	100M/24M
	clk_timern(n=1,2)	clk_matrix_100m/ osc_xin/ asrc_clk_matrix	100M/24M
TIMER_S_0	clk_timern(n=0-5)	clk_matrix_sec_100m/ osc_xin	100M/24M
TIMER_S_1	clk_timern(n=0-5)	clk_matrix_sec_100m/ osc_xin	100M/24M
PMU_TIMER	clk_timern(n=0-1)	clk_matrix_100m_pmu/ osc_xin	100M/24M
DDR_TIMER	clk_timern(n=0-1)	clk_matrix_100m/ osc_xin	100M/24M
NPU_TIMER	clk_timern(n=0-1)	clk_matrix_100m/ osc_xin	100M/24M

Note that compared to other timers, the clk_timer of TIMER_NS_1-CH1 and TIMER_NS_1-CH2 in PD_BUS have three clock source, the special clock source is that from asrc_clk_matrix. Please refer to Chapter CRU for detail.

When user disables the timer enables bit (bit 0 of TIMER_TIMERn_CONTROL), the timer_en output signal is de-asserted, and timer_clk will stop. When user enables the timer, the timer_en signal is asserted and timer_clk will start running.

The application is only allowed to re-configure registers when timer_en is low.

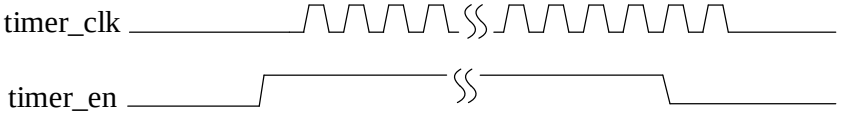

Fig. 14-2 Timing between timer_en and timer_clk

14.5.2 Programming Flow

1. Initialize the TIMER by the TIMER_TIMERn_CONTROL register:
   (1) Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
   (2) Program the timer mode—free-running or user-defined—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
   (3) Program the counting mode—count-up or count-down—by writing a "0" or "1" respectively to the count mode bit (bit 3).
   (4) Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).
2. Load the timer count value into the TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_LOAD_COUNT0 register.
3. Enable the TIMER by writing a "1" to bit 0 of TIMER_TIMERn_CONTROL.

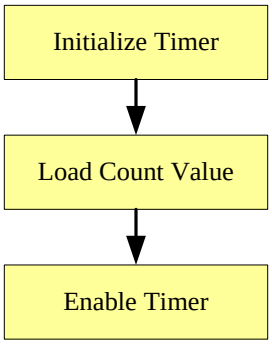

Fig. 14-3 Timer Usage Flow

14.5.3 Other Hints

The counter value of TIMER_S_1-CH5 in PD_SECURE is send to VD_GPU for GPU use.

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Chapter 15 Watchdog Timer (WDT)

15.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that caused by conflicting parts or programs in a SOC. The WDT would generate interrupt or reset signal when its counter reaches zero, then a reset controller would reset the system.

WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock can be chosen from 24MHz or 32kHz clock
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined ranges of main timeout period
- There are 6 WDTs: PMU_WDT, NPU_WDT, DDR_WDT, WDT_S, WDT_NS, BUS_WDT
- All the 6 WDTs can drive CRU to generate global software reset, and some can also generate MCU reset, correspondingly, PMU_WDT can reset PMU_MCU, NPU_WDT can reset NPU_MCU, DDR_WDT can reset DDR_MCU, BUS_WDT can reset BUS_MCU

15.2 Block Diagram

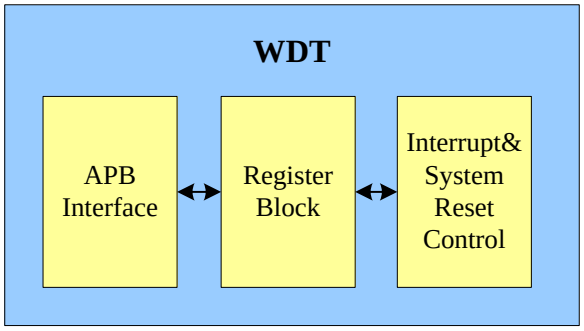

Fig. 15-1 WDT Block Diagram

WDT comprises with:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & System Reset Control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

15.3 Function Description

15.3.1 Operation

Counter

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR).

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Interrupts

The WDT can be programmed to generate an interrupt (and then a system reset) when a timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

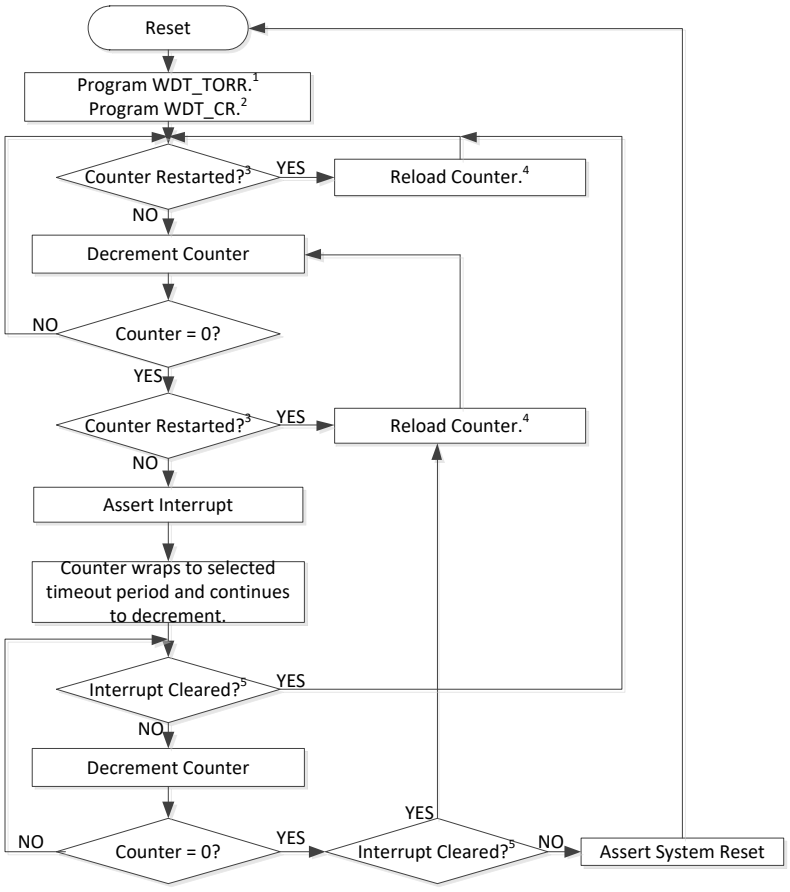
System Resets

When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

Reset Pulse Length

The reset pulse length is the number of pclk cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

15.3.2 Programming Sequence



1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 15-2 WDT Operation Flow (RMOD=1)

15.4 Register Description

15.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
PMU_WDT	0x27340000
NPU_WDT	0x27780000
DDR_WDT	0x2A040000
WDT_S	0x2A4C0000
WDT_NS	0x2ACE0000
BUS_WDT	0x2AEB0000

15.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
WDT_CR	0x0000	W	0x00000008	Control Register
WDT_TORR	0x0004	W	0x00000000	Timeout Range Register
WDT_CCVR	0x0008	W	0x0000FFFF	Current Counter Value Register
WDT_CRR	0x000C	W	0x00000000	Counter Restart Register
WDT_STAT	0x0010	W	0x00000000	Interrupt Status Register
WDT_EOI	0x0014	W	0x00000000	Interrupt Clear Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

15.4.3 Detail Registers Description

WDT_CR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x2	rst_pluse_length This is used to select the number of pclk cycles for which the system reset stays asserted. 3'b000: 2 pclk cycles 3'b001: 4 pclk cycles 3'b010: 8 pclk cycles 3'b011: 16 pclk cycles 3'b100: 32 pclk cycles 3'b101: 64 pclk cycles 3'b110: 128 pclk cycles 3'b111: 256 pclk cycles
1	RW	0x0	resp_mode Selects the output response generated to a timeout. 1'b0: Generate a system reset. 1'b1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset.
0	RW	0x0	en This bit is used to enable and disable the WDT. When disabled, the counter dose not decrement .Thus, no interrupt or system reset are generated. Once this bit has been enabled, it can be cleared only by a system reset. 1'b0: WDT disabled 1'b1: WDT enabled

WDT_TORR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	timeout_period This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values available for a 32-bit watchdog counter are: 4'b0000: 0x0000ffff 4'b0001: 0x0001ffff 4'b0010: 0x0003ffff 4'b0011: 0x0007ffff 4'b0100: 0x000fffff 4'b0101: 0x001fffff 4'b0110: 0x003fffff 4'b0111: 0x007fffff 4'b1000: 0x00ffffff 4'b1001: 0x01ffffff 4'b1010: 0x03ffffff 4'b1011: 0x07ffffff 4'b1100: 0x0fffffff 4'b1101: 0x1fffffff 4'b1110: 0x3fffffff 4'b1111: 0x7fffffff

WDT_CCVR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000ffff	cur_cnt This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read.

WDT_CRR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	cnt_restart This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

WDT_STAT

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	status This register shows the interrupt status of the WDT. 1'b1: Interrupt is active regardless of polarity. 1'b0: Interrupt is inactive.

WDT_EOI

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	int_clr This can be used to clear the interrupt without restarting the watchdog counter.

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Chapter 16 HPTIMER

16.1 Overview

HPTIMER is a programmable timer peripheral, which has special calibration function. This component is an APB slave device, and can provide count value for CPU directly.

HPTIMER supports the following features:

- Support three timer mode: normal mode, hardware adjust mode and software adjust mode
- Support two counting mode at normal mode: free-running and user-defined
- Support configuration of loading count value at normal mode
- Support several mask interrupts at different timer mode
- Support calibrate back to exact count value without software calculation in Hardware adjust mode
- Support calibrate back to exact count value with software-aided calculation in Software adjust mode
- Support common multiple configuration of slow and fast clock period
- Support providing count value for CPU use

16.2 Block Diagram

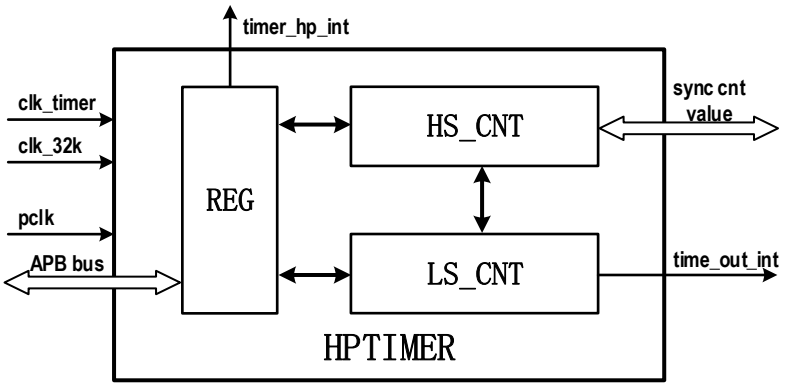

Fig. 16-1 HPTIMER Block Diagram

The figure above shows the block diagram of HPTIMER.

Register Block(REG)

This block contains several registers which are used for timer configuration, status checking and interrupt generation.

High-Speed Counter(HS_CNT)

This block contains two main counters which are working at high speed clock rate, one is used for record the current counter value that can update to CPU, the other is used to generate timing interrupt.

Low-Speed Counter(LS_CNT)

This block also contains two main counters, the different is that these counters are working at low speed clock rate, one counter is used to record the current counter value at low power mode, the other one is used as a reference counter for anti-attack.

16.3 Function Description

16.3.1 TIMER Clock

The clock frequency of clk_32k is 32KHz, and the clock frequency of clk_timer can be switched among 1GHz, 24MHz and 32KHz.

16.3.2 Timer Mode

- **Normal mode**

At this mode, HPTIMER works as a normal incremental timer. After configuration of load count, interrupt enable, and control bit. The counter will counts from 0 to load count value step by step, and generate an interrupt when the counter value reaches the load count value. If the count mode is configured as free-running, then the counter will reload to zero,

after reaching the load count, and begin a new counting loop.

- **Hardware adjust mode**

At this mode, HPTIMER works as a special incremental timer with automatic calibration by hardware.
When system is working at normal mode, the counter in high clock domain(hs_cnt) will count up normally. And the counter in low clock domain(ls_cnt) will count plus T24_GCD every T32_GCD low clock period. Since that, the hs_cnt and the ls_cnt will represent the same counter value at every T32_GCD low clock period.
When system enter low power mode, the clock frequency of hs_cnt will also switch to low frequency, but thanks to the ls_cnt, the counter value of current time will not lost. And after system recover from low power mode, the counter value of ls_cnt will automatic calibrate to hs_cnt.

- **Software adjust mode**

At this mode, HPTIMER works as a special incremental timer with calibration by software. Which means software can calibrate the counter value as you wish. The hardware will record the counter value when system enter to and recover from low power mode. And software should get this two begin and end counter values to calculate the lost time during the low power mode, and make a compensation to get the correct system time.

16.4 Register Description

16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

16.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
HPTIMER_REVISION	0x0000	W	0x2AF60201	HPTIMER Version Register
HPTIMER_CTRL	0x0004	W	0x00000000	HPTIMER Control Register
HPTIMER_INTR_EN	0x0008	W	0x00000000	Interrupt Mask Register
HPTIMER_T24_GCD	0x000C	W	0x00000000	Common Multiple div 24M
HPTIMER_T32_GCD	0x0010	W	0x00000000	Common Multiple div 32K
HPTIMER_LOAD_COUNT0	0x0014	W	0x00000000	Low 32bits of load count value
HPTIMER_LOAD_COUNT1	0x0018	W	0x00000000	High 32bits of load count value
HPTIMER_T24_DELAT_COUNT0	0x001C	W	0x00000000	Low 32bits of 24M clock delay time count value
HPTIMER_T24_DELAT_COUNT1	0x0020	W	0x00000000	High 32bits of 24M clock delay time count value
HPTIMER_CURR_32K_VALUE0	0x0024	W	0x00000000	Low 32bits of current ls_cnt value
HPTIMER_CURR_32K_VALUE1	0x0028	W	0x00000000	High 32bits of current ls_cnt value
HPTIMER_CURR_TIMER_VALUE0	0x002C	W	0x00000000	Low 32bits of current hs_cnt value
HPTIMER_CURR_TIMER_VALUE1	0x0030	W	0x00000000	High 32bits of current hs_cnt value
HPTIMER_T24_32BEGIN0	0x0034	W	0x00000000	Low 32 bits of low power begin counter value
HPTIMER_T24_32BEGIN1	0x0038	W	0x00000000	High 32 bits of low power begin counter value
HPTIMER_T32_24END0	0x003C	W	0x00000000	Low 32 bits of low power end counter value
HPTIMER_T32_24END1	0x0040	W	0x00000000	High 32 bits of low power end counter value
HPTIMER_RECORD_VALUE_VALID	0x0044	W	0x00000000	Record count value valid

Name	Offset	Size	Reset Value	Description
HPTIMER_SYNC_REQ	0x0048	W	0x00000000	Synchronize request control
HPTIMER_INTR_STATUS	0x004C	W	0x00000000	Interrupt Status Register
HPTIMER_CURR_ATATK_32K_VALUE0	0x0054	W	0x00000000	Low 32bits of current ATATK counter value
HPTIMER_CURR_ATATK_32K_VALUE1	0x0058	W	0x00000000	High 32bits of current ATATK counter value
HPTIMER_LOAD_COUNT0_32K	0x005C	W	0x00000000	Low 32bits of load count 32k value
HPTIMER_LOAD_COUNT1_32K	0x0060	W	0x00000000	High 32bits of load count 32k value
HPTIMER_CURR_COMP_H_VALUE0	0x0064	W	0x00000000	Low 32bits of hs_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_H_VALUE1	0x0068	W	0x00000000	High 32bits of hs_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_L_VALUE0	0x006C	W	0x00000000	Low 32bits of ls_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_L_VALUE1	0x0070	W	0x00000000	High 32bits of ls_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_H_32K_VALUE0	0x0074	W	0x00000000	Low 32bits of hs_cnt value when compensation enable
HPTIMER_CURR_COMP_H_32K_VALUE1	0x0078	W	0x00000000	High 32bits of hs_cnt value when compensation enable
HPTIMER_CURR_COMP_L_32K_VALUE0	0x007C	W	0x00000000	Low 32bits of ls_cnt value when compensation enable
HPTIMER_CURR_COMP_L_32K_VALUE1	0x0080	W	0x00000000	High 32bits of ls_cnt value when compensation enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

16.4.3 Detail Registers Description

HPTIMER_REVISION

Address: Operational Base(0x27400000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x2af6	svn_revision Svn revision 16'd10998
15:10	RO	0x00	reserved
9:8	RO	0x2	ch_type Channel 0 is a low power recovery self-correction count up counter.
7:0	RO	0x01	ip_function IP function. 16'd1

HPTIMER_CTRL

Address: Operational Base(0x27400000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable of the lower 16bit 1'b0: Disable 1'b1: Enable
15:7	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	hp_init_mode Control the hs_cnt initial mode 1'b0: hs_cnt will begin count together with ls_cnt 1'b1: hs_cnt will not wait for ls_cnt
5	RW	0x0	extra_cnt_ctrl Control the extra counter 1'b0: Disable 1'b1: Enable
4	RW	0x0	atatk_cnt_ctrl Control the anti-attack counter 1'b0: Enable 1'b1: Disable
3	RW	0x0	count_mode Timer count mode 1'b0: Free-running mode 1'b1: User-defined count mode
2:1	RW	0x0	timer_mode Select timer as which timer 2'b00: Normal timer 2'b01: Adjust timer with hardware adjust 2'b10: Adjust timer with software adjust
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

HPTIMER_INTR_EN

Address: Operational Base(0x27400000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	extra_count_reach_intr_en Extra timer count reach load_count interrupt enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	count_reach_32k_intr_en low speed count reach interrupt enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	sync_done_intr_en Synchronization done interrupt enable 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	count_reach_intr_en high speed count reach load_count interrupt enable 1'b0: Disable 1'b1: Enable

HPTIMER_T24_GCD

Address: Operational Base(0x27400000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_gcd The least common multiple of 24M(1G) and 32K clock cycles divided by 24M(1G) clock cycles.

HPTIMER_T32_GCD

Address: Operational Base(0x27400000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t32_gcd The least common multiple of 24M(1G) and 32K clock cycles divided by 32K clock cycles.

HPTIMER_LOAD_COUNT0

Address: Operational Base(0x27400000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count0 Low 32bits of load count value.

HPTIMER_LOAD_COUNT1

Address: Operational Base(0x27400000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count1 High 32bits of load count value.

HPTIMER_T24_DELAT_COUNT0

Address: Operational Base(0x27400000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_delay_time_count0 Low 32bits of 24M clock delay time count value.

HPTIMER_T24_DELAT_COUNT1

Address: Operational Base(0x27400000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_delay_time_count1 High 32bits of 24M clock delay time count value.

HPTIMER_CURR_32K_VALUE0

Address: Operational Base(0x27400000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_32k_value0 Low 32bits of current ls_cnt value.

HPTIMER_CURR_32K_VALUE1

Address: Operational Base(0x27400000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_32k_value1 High 32bits of current ls_cnt value.

HPTIMER_CURR_TIMER_VALUE0

Address: Operational Base(0x27400000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value0 Low 32bits of current hs_cnt value.

HPTIMER_CURR_TIMER_VALUE1

Address: Operational Base(0x27400000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value1 High 32bits of current hs_cnt value.

HPTIMER_T24_32BEGIN0

Address: Operational Base(0x27400000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t24_32begin0 Low 32 bits of hs_cnt value when 24M(1G) clock switches to 32K clock.

HPTIMER_T24_32BEGIN1

Address: Operational Base(0x27400000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t24_32begin1 High 32 bits of hs_cnt value when 24M(1G) clock switches to 32K clock.

HPTIMER_T32_24END0

Address: Operational Base(0x27400000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t32_24end0 Low 32 bits of hs_cnt value when 32K clock switches to 24M(1G) clock.

HPTIMER_T32_24END1

Address: Operational Base(0x27400000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t32_24end1 High 32 bits of hs_cnt value when 32K clock switches to 24M(1G) clock.

HPTIMER_RECORD_VALUE_VALID

Address: Operational Base(0x27400000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	W1C	0x0	curr_comp_value_32k_valid CURR_COMP_*_32K_VALUE valid 1'b0: Invalid 1'b1: Valid
2	W1C	0x0	curr_comp_value_valid CURR_COMP_*_VALUE valid 1'b0: Invalid 1'b1: Valid
1	W1C	0x0	t32_24end_valid T32_24END value valid 1'b0: Invalid 1'b1: Valid
0	W1C	0x0	t24_32begin_valid T24_32BEGIN value valid 1'b0: Invalid 1'b1: Valid

HPTIMER_SYNC_REQ

Address: Operational Base(0x27400000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable of the lower 16bit 1'b0: Disable 1'b1: Enable
15:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	hw_sync_disable 1'b0: Enable synchronization 1'b1: Disable synchronization When this bit is set to 1'b1, than no matter the value of hs_cnt and ls_cnt, the synchronization will not be executed.
8	RW	0x0	hw_sync_en Control the sync logic of hs_cnt 1'b0: Disable 1'b1: Enable When enable this bit, hardware will record the value of hs_cnt and ls_cnt at the time that a hw_sync_req occurs. And if the value of hs_cnt is larger than ls_cnt, then the synchronization to hs_cnt will not be executed.
7	RO	0x0	reserved
6	RW	0x0	hw_sync_compensation_en Enable the compensation to ls_cnt after a hw_sync_req occurs, the hardware will compare the value of hs_cnt and ls_cnt, if hs_cnt is larger than ls_cnt, then the different will be compensated to ls_cnt. 1'b0: Disable 1'b1: Enable
5	RW	0x0	low_power_compensation_en Enable the compensation to ls_cnt at the time that system enter the low power state, the hardware will compare the value of hs_cnt and ls_cnt, if hs_cnt is larger than ls_cnt, then the different will be compensated to ls_cnt. 1'b0: Disable 1'b1: Enable
4	RW	0x0	compensation_en Control the compensation logic of ls_cnt 1'b0: Disable 1'b1: Enable When enable this bit, hardware will record the value of hs_cnt and ls_cnt at the time that system enter low power state.
3:2	RO	0x0	reserved
1	R/WSC	0x0	hw_sync_req hs_cnt synchronize request by hardware, which means synchronize hs_cnt by ls_cnt value
0	R/WSC	0x0	sw_sync_req hs_cnt synchronize request by software, which means directly compensate T24_DELAT_COUNT to hs_cnt

HPTIMER_INTR_STATUS

Address: Operational Base(0x27400000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	W1C	0x0	extra_count_reach Extra cnt reach the load count value
3	W1C	0x0	count_reach_32k Ls_cnt counter value is more than load_count_32k-t24_gcd, and less than load_count_32k
2	W1C	0x0	sync_done hs_cnt synchronization done
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	W1C	0x0	count_reach Normal counter: hs_cnt reach load_count value

HPTIMER_CURR_ATATK_32K_VALUE0

Address: Operational Base(0x27400000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	current_atatk_32k_value0 Low 32bits of current atatk_cnt_32k value.

HPTIMER_CURR_ATATK_32K_VALUE1

Address: Operational Base(0x27400000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	current_atatk_32k_value1 High 32bits of current atatk_cnt_32k value.

HPTIMER_LOAD_COUNT0_32K

Address: Operational Base(0x27400000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count0_32k Low 32bits of load count 32k value.

HPTIMER_LOAD_COUNT1_32K

Address: Operational Base(0x27400000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count1_32k High 32bits of load count 32k value.

HPTIMER_CURR_COMP_H_VALUE0

Address: Operational Base(0x27400000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_value0 Low 32bits of curr_comp_h_value, which indicate the record value of hs_cnt when a hw_sync_req occurs

HPTIMER_CURR_COMP_H_VALUE1

Address: Operational Base(0x27400000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_value1 High 32bits of curr_comp_h_value, which indicate the record value of hs_cnt when a hw_sync_req occurs

HPTIMER_CURR_COMP_L_VALUE0

Address: Operational Base(0x27400000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_value0 Low 32bits of curr_comp_l_value, which indicate the record value of ls_cnt when a hw_sync_req occurs

HPTIMER_CURR_COMP_L_VALUE1

Address: Operational Base(0x27400000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_value1 High 32bits of curr_comp_l_value, which indicate the record value of ls_cnt when a hw_sync_req occurs

HPTIMER_CURR_COMP_H_32K_VALUE0

Address: Operational Base(0x27400000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_32k_value0 Low 32bits of curr_comp_h_32k_value, which indicate the record value of hs_cnt when system enter the low power state.

HPTIMER_CURR_COMP_H_32K_VALUE1

Address: Operational Base(0x27400000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_32k_value1 High 32bits of curr_comp_h_32k_value, which indicate the record value of hs_cnt when system enter the low power state.

HPTIMER_CURR_COMP_L_32K_VALUE0

Address: Operational Base(0x27400000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_32k_value0 Low 32bits of curr_comp_l_32k_value, which indicate the record value of ls_cnt when system enter the low power state.

HPTIMER_CURR_COMP_L_32K_VALUE1

Address: Operational Base(0x27400000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_32k_value1 High 32bits of curr_comp_l_32k_value, which indicate the record value of ls_cnt when system enter the low power state.

16.5 Application Notes

16.5.1 Clock and Reset

There are two different clock domains in HPTIMER: clk_timer, clk_32k. The frequency of these clocks are as below:

Table 16-1 Clock Frequency

Clock Name	Clock Source
clk_timer	1G/24M/32K
clk_32k	32K

The clock clk_timer can switch to three different frequencies according to different mode. In normal working mode, HPTIMER is working at 1G or 24M, and the exact working frequency is depending on user needs. In low power mode, HPTIMER is working at 32K. As Fig 1-2 shows below, hp_sel is clock control bit to switch between 1G and 24M, which is related to PMU1_CRU_CLKSEL_CON11. And lp_ena is clock control bit to switch between 1G/24M and 32K, which is related to PMU0_SGRF_SOC_CON1.

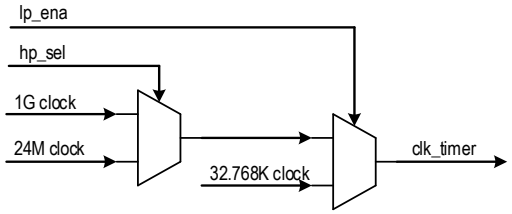

Fig. 16-2 Clock Selection of clk_timer

Please refer to chapter CRU and GRF for detail.

16.5.2 Programming Flow

- **Normal mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x0 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Load the HPTIMER count value into the HPTIMER_LOAD_COUNT1 and HPTIMER_LOAD_COUNT0 register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.

If you want to do another count, repeat steps 1 to 3.

- **Hardware adjust mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x1 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Initialize the HPTIMER by the HPTIMER_INTR_STATUS register. Write 0x5 to HPTIMER_INTR_STATUS register to clear HPTIMER_INTR_STATUS register.
3. Configure the HPTIMER GCD register.
   (1) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_timer clock cycle and configure it in HPTIMER_T24_GCD register.
   (2) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_32k clock cycle and configure it in HPTIMER_T32_GCD register.
4. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
5. Configure the PMU0GRF to assert lp_ena before the chip enters low power consumption mode.
6. The chip enters and exits the low power consumption mode at any time in between.
7. Configure the PMU0GRF to de-assert lp_ena after the chip exits low power consumption mode.
8. Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the HPTIMER count is adjusted.
9. Write 0x4 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 6 to 9.

- **Software adjust mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x2 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Initialize the HPTIMER by the HPTIMER_INTR_STATUS and BEGIN_END_VALID register. Write 0x5 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register. write 0x3 to RECORD_VALUE_VALID register to clear RECORD_VALUE_VALID register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
4. Configure the PMU0GRF to assert lp_ena before the chip enters low power consumption mode.
5. The chip enters and exits the low power consumption mode at any time in between.
6. Configure the PMU0GRF to deassert lp_ena after the chip exits low power consumption

mode.

7. Read out RECORD_VALUE_VALID register until the value of it is 0x3, which indicates that the chip has entered and exited the low power consumption mode, then you can adjust the timer count value. Then write 0x3 to RECORD_VALUE_VALID register to clear the register.
8. The count value of HPTIMER compensation.
   (1) Read out HPTIMER_T24_32BEGIN1, TIMER_ HP_T24_32BEGIN0, HPTIMER_T32_ 24END1 and HPTIMER_T32_24END0 register.
   (2) configure HPTIMER_T24_DELAT_COUNT1 and HPTIMER_T24_DELAT_COUNT0 registers to compensate for the count values according to the values of these registers read out above.
   (3) Write 0x1 to HPTIMER_SYNC_REQ register to start compensation counting.
   (4) Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the compensation count is completed.
9. Write 0x5 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 5 to 8.

- **Hardware compensation configuration**

The hardware compensation configurations are all related to the HPTIMER_SYNC_REQ register.

1. When compensation_en(bit 4) of HPTIMER_SYNC_REQ is asserted, then the hardware will record the value of hs_cnt and ls_cnt at the time that system enters low power mode, and the record value will be stored at HPTIMER_CURR_COMP_*_32K_VALUE.
2. When low_power_compensation_en(bit 5) of HPTIMER_SYNC_REQ is asserted, then the hardware will compare the value of hs_cnt and ls_cnt at the time that system enters low power mode. And if hs_cnt is greater than ls_cnt at this time, the different will be compensated to ls_cnt.
3. When hw_sync_compensation_en(bit 6) of HPTIMER_SYNC_REQ is asserted, then the hardware will compare the value of hs_cnt and ls_cnt at the time that hardware synchronization occurs. And if hs_cnt is larger than ls_cnt at this time, the different will be compensated to ls_cnt.
4. When hw_sync_en(bit 7) of TIMRE_HP_SYNC_REQ is asserted, then the hardware will record the value of hs_cnt and ls_cnt at the time that hardware synchronization occurs, and the record value will be stored at HPTIMER_CURR_COMP_*_VALUE. The other hand, if the value of hs_cnt is greater than ls_cnt，then the synchronization to hs_cnt will not be executed.
5. When hw_sync_disable(bit 8) of HPTIMER_SYNC_REQ is asserted, then no matter the value of hs_cnt and ls_cnt, the synchronization will not be executed.

- **Low power mode wakeup**

This function is used at hardware adjust mode, the programing flow is mainly as hardware adjust mode.

1. Configure HPTIMER to hardware adjust mode.
2. Configure the HPTIMER GCD register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
4. Prepare to enter low power mode:
   (1) Configure PMU to set HPTIMER as wake up source.
   (2) Configure the bit 3 of HPTIMER_INTR_EN to set count reach interrupt enable at 32K.
   (3) Configure the HPTIMER_LOAD_COUNT1_32K and HPTIMER_LOAD_COUNT0_32K to set the wake up time. (note that user must configure HPTIMER_LOAD_COUNT0_32K at last)
5. Configure the PMU0GRF to assert lp_ena before the chip enters low power consumption mode.
6. Wait for HPTIMER to wake up system.
7. Configure the PMU0GRF to de-assert lp_ena after the chip exits low power consumption mode.
8. Read out the INTR_STATUS register and write 0x8 to HPTIMER_INTR_STATUS register

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to clear count reach 32k interrupt.

9. Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the HPTIMER count is adjusted.
10. Write 0x4 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 4 to 10.

- **High performance timing interrupt**

HPTIMER provides a 32-bits High performance counter to generate timing interrupt at hardware adjust mode.

1. Configure HPTIMER to hardware adjust mode.
2. Configure the HPTIMER_LOAD_COUNT0 to set the load count.
3. Configure bit 4 of HPTIMER_INTR_EN to enable interrupt.
4. Configure bit 5 of HPTIMER_CTRL to enable the hyper performance counter to work.
5. Wait for the interrupt generate.
6. Write '1' to bit 4 of HPTIMER_INTR_STATUS to clear the interrupt status.

When the count mode of timer is configured to free-running, then the interrupt will assert every load count time, otherwise the interrupt will generate only one time.

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Chapter 17 Mailbox

17.1 Overview

The Mailbox module is a simple APB peripheral that allows CPU, MCU core to communicate with each other by writing operation to generate interrupt. The registers are accessible via APB interface.
The Mailbox has the following main features:

- Support APB interface
- Support 14 mailbox groups, each group includes one data word, one command word register and one flag bit that can represent one interrupt
- Support interrupts to CPU, and MCU core
- Support two type of interrupt trigger mode

17.2 Block Diagram

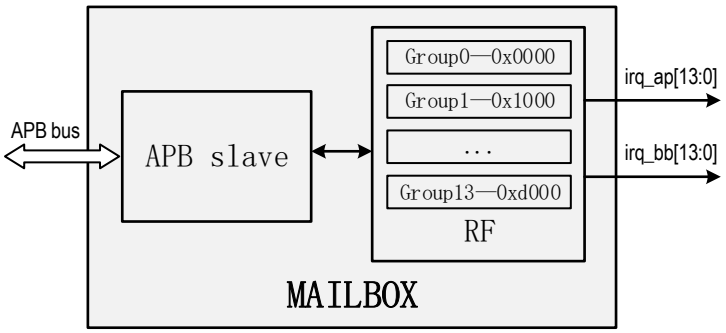

Fig. 17-1 Mailbox Block Diagram

17.3 Function Description

- Regard CPU as the "AP" side of the Mailbox. The 14 groups interrupt to CPU is:
  - Enabled when MAILBOX_B2A_INTEN is set to 1 and the corresponding IRQs is enabled in GIC.
  - Generated when there are writing operation to corresponding MAILBOX_B2A_CMD_i and MAILBOX_B2A_DAT_i orderly.
  - Cleared when writing 1 to corresponding MAILBOX_B2A_STATUS.
- Regard MCU core as the "BB" side of the Mailbox. The 14 groups interrupt to MCU core is:
  - Enabled when MAILBOX_A2B_INTEN is set to 1 and the corresponding IRQs is enabled in INTC of MCU.
  - Generated when there are writing operation to corresponding MAILBOX_A2B_CMD_i and MAILBOX_A2B_DAT_i orderly.
  - Cleared when writing 1 to corresponding MAILBOX_A2B_STATUS.
- You can also regard CPU as the "BB" side of the Mailbox and regard MCU core as the "AP" side of the Mailbox. The configuration flow is similar.
- Note that, due to the limitation of MCU IRQ numbers, not all irq_mailbox_bb are connected to MCU IRQ port directly, the rest of no direct connecting irq_mailbox_* are connected to INTMUX and mux for MCU, please refer to Chapter MCU Subsystem for more detail.

17.4 Register Description

17.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
MAILBOX_CH0	0x2AE50000
MAILBOX_CH1	0x2AE51000
MAILBOX_CH2	0x2AE52000
MAILBOX_CH3	0x2AE53000
MAILBOX_CH4	0x2AE54000
MAILBOX_CH5	0x2AE55000
MAILBOX_CH6	0x2AE56000
MAILBOX_CH7	0x2AE57000
MAILBOX_CH8	0x2AE58000
MAILBOX_CH9	0x2AE59000
MAILBOX_CH10	0x2AE5A000
MAILBOX_CH11	0x2AE5B000
MAILBOX_CH12	0x2AE5C000
MAILBOX_CH13	0x2AE5D000

17.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MAILBOX_A2B_INTEN	0x0000	W	0x00000100	AP to BB Interrupt Enable Register for Groupx
MAILBOX_A2B_STATUS	0x0004	W	0x00000000	AP to BB Interrupt Status Register for Groupx
MAILBOX_A2B_CMD	0x0008	W	0x00000000	AP to BB Command x Register
MAILBOX_A2B_DATA	0x000C	W	0x00000000	AP to BB Data x Register
MAILBOX_B2A_INTEN	0x0010	W	0x00000100	BB to AP Interrupt Enable Register for Groupx
MAILBOX_B2A_STATUS	0x0014	W	0x00000000	BB to AP Interrupt Status Register for Groupx
MAILBOX_B2A_CMD	0x0018	W	0x00000000	BB to AP Command x Register
MAILBOX_B2A_DATA	0x001C	W	0x00000000	BB to AP Data x Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

17.4.3 Detail Registers Description

MAILBOX_A2B_INTEN

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for low bit 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8	RW	0x1	a2b_trig_modex Interrupt trigger mode for groupx a2b int 1'b0: Write CMD then generate interrupt 1'b1: Write CMD firstly, then Write DAT, and then generate interrupt
7:1	RO	0x00	reserved
0	RW	0x0	a2b_intenx Interrupt enable for groupx a2b int. 1'b0: Disable 1'b1: Enable

MAILBOX_A2B_STATUS

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Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	a2b_intx Interrupt status for groupx a2b int. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_A2B_CMD

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command x register

MAILBOX_A2B_DATA

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data x register

MAILBOX_B2A_INTEN

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for low bit 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8	RW	0x1	b2a_trig_modex Interrupt trigger mode for groupx b2a int 1'b0: Write CMD then generate interrupt 1'b1: Write CMD firstly, then Write DAT, and then generate interrupt
7:1	RO	0x00	reserved
0	RW	0x0	b2a_intenx Interrupt enable for groupx b2a int. 1'b0: Disable 1'b1: Enable

MAILBOX_B2A_STATUS

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	b2a_intx Interrupt status for groupx b2a int. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_B2A_CMD

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command x register

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MAILBOX_B2A_DATA

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data x register

17.5 Application Notes

Mailbox supports two type of interrupt trigger mode:

- Normal mode:
  1. Configure bit 8 of MAILBOX_*_INTEN to '1'
  2. Write the MAILBOX_*_CMD firstly
  3. Then write the MAILBOX_*_DATA
  4. And then generate an interrupt

  Write to the MAILBOX_*_CMD register before writing to the MAILBOX_*_DATA register. If wrong order is used, then the interrupt cannot be generated successfully.
- Fast trigger mode:
  1. Configure bit 8 of MAILBOX_*_INTEN to '0'
  2. Write the MAILBOX_*_CMD
  3. And then generate an interrupt
- If you want to clear the interrupt, you can read out the MAILBOX_*_STATUS register and writing 1 to corresponding bit.

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Chapter 18 SAR-ADC

18.1 Overview

The ADC is an 8-channel single-ended 12-bit Successive Approximation Register (SAR) A/D Converter. It uses the supply and ground as its reference which avoid the use of any external reference. It converts the analog input signal into 12-bit binary digital codes at maximum conversion rate of 1MSps with 20MHz A/D converter clock. The input range is typically 0V to 1.8V.

SAR-ADC controller supports the following features:

- Support single mode and series conversion mode.
- In single mode, the conversion operates once each software access.
- End of conversion interrupt can be enabled.
- In series conversion, controller samples each channel then loops until software stop conversion.
- High/low threshold can be set, higher/lower/between high-low-threshold interrupt can be enabled.

18.2 Block Diagram

SAR-ADC block shows in the figure below. This includes:

- APB Interface
- Control FSM
- SAR-ADC PHY

Software can configure SAR-ADC controller by APB interface, then the inter FSM will communicate with SAR-ADC PHY for limited timing request.

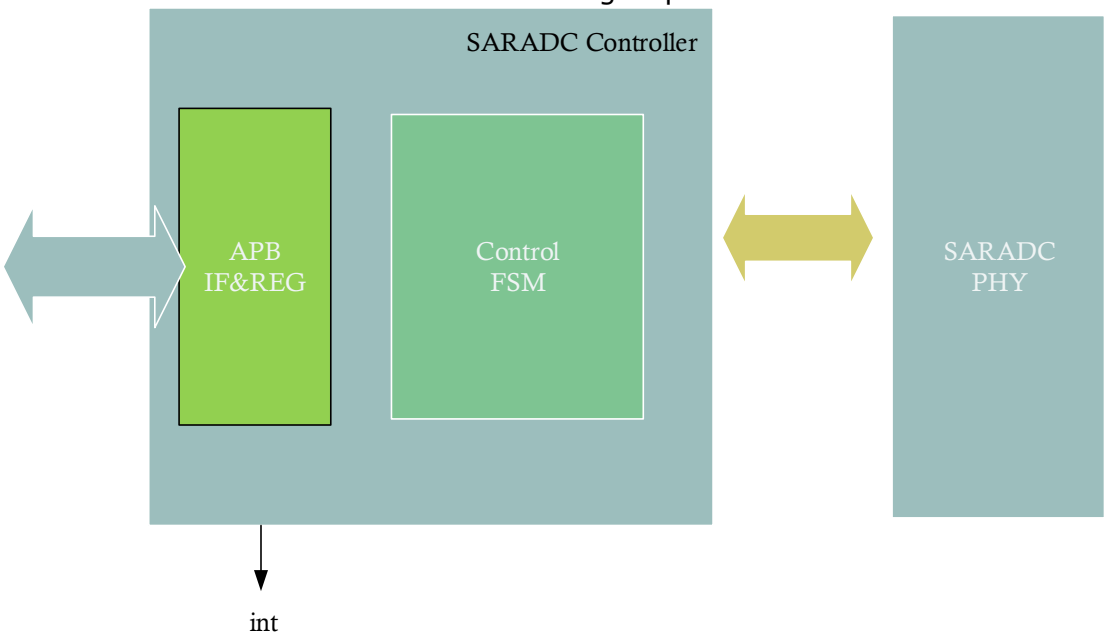

Fig. 18-1 SAR-ADC Block Diagram

18.3 Function Description

SAR-ADC block includes controller and PHY, user cannot directly access SAR-ADC PHY. Software access the SAR-ADC through SAR-ADC controller by APB interface. SAR-ADC controller will sample the conversion result from SAR-ADC PHY.

18.4 Register Description

18.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

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18.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SARADC_CONV_CON	0x0000	W	0x00000000	Conversion control
SARADC_T_PD_SOC	0x0004	W	0x00000013	Timing control for PD to SOC
SARADC_T_AS_SOC	0x0008	W	0x00000005	Timing control for assert SOC
SARADC_T_DAS_SOC	0x000C	W	0x00000007	Timing control from dis-assert SOC to change channel
SARADC_T_SEL_SOC	0x0010	W	0x00000003	Timimg control from change channel select to assert SOC
SARADC_HIGH_COMP0	0x0014	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP1	0x0018	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP2	0x001C	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP3	0x0020	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP4	0x0024	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP5	0x0028	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP6	0x002C	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP7	0x0030	W	0x00000000	High threshold for ADC output data
SARADC_LOW_COMP0	0x0054	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP1	0x0058	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP2	0x005C	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP3	0x0060	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP4	0x0064	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP5	0x0068	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP6	0x006C	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP7	0x0070	W	0x00000000	Low threshold for ADC output data
SARADC_DEBOUNCE	0x0094	W	0x00000003	Threshold debounce
SARADC_HT_INT_EN	0x0098	W	0x00000000	High threshold int enable
SARADC_LT_INT_EN	0x009C	W	0x00000000	Low threshold int enable
SARADC_MT_INT_EN	0x0100	W	0x00000000	Middle threshold int enable
SARADC_END_INT_EN	0x0104	W	0x00000000	End conversion int enable
SARADC_ST_CON	0x0108	W	0x0000001C	ADC static control
SARADC_STATUS	0x010C	W	0x00000002	ADC status
SARADC_END_INT_ST	0x0110	W	0x00000000	End conversion int state
SARADC_HT_INT_ST	0x0114	W	0x00000000	High threshold int state
SARADC_LT_INT_ST	0x0118	W	0x00000000	Low threshold int state
SARADC_MT_INT_ST	0x011C	W	0x00000000	Middle threshold int state
SARADC_DATA0	0x0120	W	0x00000000	ADC output data
SARADC_DATA1	0x0124	W	0x00000000	ADC output data

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Name	Offset	Size	Reset Value	Description
SARADC_DATA2	0x0128	W	0x00000000	ADC output data
SARADC_DATA3	0x012C	W	0x00000000	ADC output data
SARADC_DATA4	0x0130	W	0x00000000	ADC output data
SARADC_DATA5	0x0134	W	0x00000000	ADC output data
SARADC_DATA6	0x0138	W	0x00000000	ADC output data
SARADC_DATA7	0x013C	W	0x00000000	ADC output data
SARADC_AUTO_CH_EN	0x0160	W	0x00000000	Channel enable in auto channel mode

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.4.3 Detail Registers Description

SARADC_CONV_CON

Address: Operational Base(0x2AE00000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	int_lock This is used to lock the sample data when interrupt happened. 1'b0: Disable lock. 1'b1: Enable lock.
8	RW	0x0	as_pd_mode If this bit is set to 1'b1, each time conversion ends, PD will be asserts. Then next time conversion starts, PD will be set to low auto automatically. This is not used in signal mode.
7	W1C	0x0	end_conv End conversion, this is not used when CONV_CON[5] is set to 1'b1. If this bit set to 1'b1, PD will set to 1'b1 after the last conversion and this bit will be cleared to 1'b0.
6	RW	0x0	auto_channel_mode Auto channel mode. If this is enable, channel will be round auto according which is set in AUTO_CH_EN.
5	RW	0x0	single_pd_mode Single conversion mode. If this bit is set to 1, conversion only operate once, then PD single will be set to 1.
4	W1C	0x0	start_adc Enable ADC, if this bit set to one, conversion will start. Then this bit will be clear to 0.
3:0	RW	0x0	channel_sel Channel for SARADC, 16 channel is supported. This field is not used when CONV_CON[6] is set to 1. 4'd0: select channel 0. 4'd1: select channel 1. 4'd2: select channel 2. 4'd3: select channel 3. 4'd4: select channel 4. 4'd5: select channel 5. 4'd6: select channel 6. 4'd7: select channel 7.

SARADC_T_PD_SOC

Address: Operational Base(0x2AE00000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x13	t_pd_soc Timing control between power up to start-of-conversion.

SARADC_T_AS_SOC

Address: Operational Base(0x2AE00000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000005	t_as_soc Timing control for assert SOC signal.

SARADC_T_DAS_SOC

Address: Operational Base(0x2AE00000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000007	t_das_soc Timing from dis-assert SOC to channel select change.

SARADC_T_SEL_SOC

Address: Operational Base(0x2AE00000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0003	t_sel_soc Timing from channel load to SOC assert.

SARADC_HIGH_COMP0

Address: Operational Base(0x2AE00000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp0 High threshold for ADC output data for channel 0.

SARADC_HIGH_COMP1

Address: Operational Base(0x2AE00000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp1 High threshold for ADC output data for channel 1.

SARADC_HIGH_COMP2

Address: Operational Base(0x2AE00000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp2 High threshold for ADC output data for channel 2.

SARADC_HIGH_COMP3

Address: Operational Base(0x2AE00000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp3 High threshold for ADC output data for channel 3.

SARADC_HIGH_COMP4

Address: Operational Base(0x2AE00000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp4 High threshold for ADC output data for channel 4.

SARADC_HIGH_COMP5

Address: Operational Base(0x2AE00000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp5 High threshold for ADC output data for channel 5.

SARADC_HIGH_COMP6

Address: Operational Base(0x2AE00000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp6 High threshold for ADC output data for channel 6.

SARADC_HIGH_COMP7

Address: Operational Base(0x2AE00000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp7 High threshold for ADC output data for channel 7.

SARADC_LOW_COMP0

Address: Operational Base(0x2AE00000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp0 Low threshold for ADC output data for channel 0.

SARADC_LOW_COMP1

Address: Operational Base(0x2AE00000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp1 Low threshold for ADC output data for channel 1.

SARADC_LOW_COMP2

Address: Operational Base(0x2AE00000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp2 Low threshold for ADC output data for channel 2.

SARADC_LOW_COMP3

Address: Operational Base(0x2AE00000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp3 Low threshold for ADC output data for channel 3.

SARADC_LOW_COMP4

Address: Operational Base(0x2AE00000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp4 Low threshold for ADC output data for channel 4.

SARADC_LOW_COMP5

Address: Operational Base(0x2AE00000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp5 Low threshold for ADC output data for channel 5.

SARADC_LOW_COMP6

Address: Operational Base(0x2AE00000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp6 Low threshold for ADC output data for channel 6.

SARADC_LOW_COMP7

Address: Operational Base(0x2AE00000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp7 Low threshold for ADC output data for channel 7.

SARADC_DEBOUNCE

Address: Operational Base(0x2AE00000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce ADC controller will only generate interrupt data is higher/lower/between setting threshold for "debounce" times.

SARADC_HT_INT_EN

Address: Operational Base(0x2AE00000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	ht_int_en15 High threshold interrupt for channel15. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
14	RW	0x0	ht_int_en14 High threshold interrupt for channel14. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
13	RW	0x0	ht_int_en13 High threshold interrupt for channel13. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

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Bit	Attr	Reset Value	Description
12	RW	0x0	ht_int_en12 High threshold interrupt for channel12. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
11	RW	0x0	ht_int_en11 High threshold interrupt for channel11. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
10	RW	0x0	ht_int_en10 High threshold interrupt for channel10. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
9	RW	0x0	ht_int_en9 High threshold interrupt for channel9. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
8	RW	0x0	ht_int_en8 High threshold interrupt for channel8. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
7	RW	0x0	ht_int_en7 High threshold interrupt for channel7. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
6	RW	0x0	ht_int_en6 High threshold interrupt for channel6. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
5	RW	0x0	ht_int_en5 High threshold interrupt for channel5. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
4	RW	0x0	ht_int_en4 High threshold interrupt for channel4. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
3	RW	0x0	ht_int_en3 High threshold interrupt for channel3. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
2	RW	0x0	ht_int_en2 High threshold interrupt for channel2. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
1	RW	0x0	ht_int_en1 High threshold interrupt for channel1. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
0	RW	0x0	ht_int_en0 High threshold interrupt for channel0. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

SARADC_LT_INT_EN

Address: Operational Base(0x2AE00000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	lt_int_en15 Low threshold interrupt for channel15. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
14	RW	0x0	lt_int_en14 Low threshold interrupt for channel14. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
13	RW	0x0	lt_int_en13 Low threshold interrupt for channel13. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
12	RW	0x0	lt_int_en12 Low threshold interrupt for channel12. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
11	RW	0x0	lt_int_en11 Low threshold interrupt for channel11. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
10	RW	0x0	lt_int_en10 Low threshold interrupt for channel10. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
9	RW	0x0	lt_int_en9 Low threshold interrupt for channel9. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
8	RW	0x0	lt_int_en8 Low threshold interrupt for channel8. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
7	RW	0x0	lt_int_en7 Low threshold interrupt for channel7. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
6	RW	0x0	lt_int_en6 Low threshold interrupt for channel6. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
5	RW	0x0	lt_int_en5 Low threshold interrupt for channel5. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
4	RW	0x0	lt_int_en4 Low threshold interrupt for channel4. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
3	RW	0x0	lt_int_en3 Low threshold interrupt for channel3. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

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Bit	Attr	Reset Value	Description
2	RW	0x0	lt_int_en2 Low threshold interrupt for channel2. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
1	RW	0x0	lt_int_en1 Low threshold interrupt for channel1. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
0	RW	0x0	lt_int_en0 Low threshold interrupt for channel0. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

SARADC_MT_INT_EN

Address: Operational Base(0x2AE00000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mt_int_en15 Middle threshold interrupt for channel15. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
14	RW	0x0	mt_int_en14 Middle threshold interrupt for channel14. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
13	RW	0x0	mt_int_en13 Middle threshold interrupt for channel13. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
12	RW	0x0	mt_int_en12 Middle threshold interrupt for channel12. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
11	RW	0x0	mt_int_en11 Middle threshold interrupt for channel11. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
10	RW	0x0	mt_int_en10 Middle threshold interrupt for channel10. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
9	RW	0x0	mt_int_en9 Middle threshold interrupt for channel9. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
8	RW	0x0	mt_int_en8 Middle threshold interrupt for channel8. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

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Bit	Attr	Reset Value	Description
7	RW	0x0	mt_int_en7 Middle threshold interrupt for channel7. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
6	RW	0x0	mt_int_en6 Middle threshold interrupt for channel6. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
5	RW	0x0	mt_int_en5 Middle threshold interrupt for channel5. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
4	RW	0x0	mt_int_en4 Middle threshold interrupt for channel4. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
3	RW	0x0	mt_int_en3 Middle threshold interrupt for channel3. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
2	RW	0x0	mt_int_en2 Middle threshold interrupt for channel2. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
1	RW	0x0	mt_int_en1 Middle threshold interrupt for channel1. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
0	RW	0x0	mt_int_en0 Middle threshold interrupt for channel0. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

SARADC_END_INT_EN

Address: Operational Base(0x2AE00000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	end_int_en End of conversion interrupt. 1'b0: Disable end conversion intr. 1'b1: Enable end conversion intr.

SARADC_ST_CON

Address: Operational Base(0x2AE00000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x3	ictrl Control the bias current of the preamplifier in the SAR-ADC.
2:0	RW	0x4	cctrl Control the capacitance of the capacitor DAC array, which is related to the linearity of the SAR-ADC.

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SARADC_STATUS

Address: Operational Base(0x2AE00000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:2	RO	0x0	sel ADC channel select.
1	RO	0x1	pd 1'b1: ADC is power down. 1'b0: ADC is power up and in conversion.
0	RO	0x0	conv_st Conversion status 1'b1: ADC controller FSM is busy. 1'b0: ADC controller FSM is idle.

SARADC_END_INT_ST

Address: Operational Base(0x2AE00000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	end_int_st ADC end conversion interrupt status. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

SARADC_HT_INT_ST

Address: Operational Base(0x2AE00000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	ht_int_st15 High threshold interrupt state for channel15. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
14	W1C	0x0	ht_int_st14 High threshold interrupt state for channel14. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
13	W1C	0x0	ht_int_st13 High threshold interrupt state for channel13. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
12	W1C	0x0	ht_int_st12 High threshold interrupt state for channel12. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
11	W1C	0x0	ht_int_st11 High threshold interrupt state for channel11. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
10	W1C	0x0	ht_int_st10 High threshold interrupt state for channel10. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
9	W1C	0x0	ht_int_st9 High threshold interrupt state for channel9. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

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Bit	Attr	Reset Value	Description
8	W1C	0x0	ht_int_st8 High threshold interrupt state for channel8. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
7	W1C	0x0	ht_int_st7 High threshold interrupt state for channel7. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
6	W1C	0x0	ht_int_st6 High threshold interrupt state for channel6. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
5	W1C	0x0	ht_int_st5 High threshold interrupt state for channel5. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
4	W1C	0x0	ht_int_st4 High threshold interrupt state for channel4. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
3	W1C	0x0	ht_int_st3 High threshold interrupt state for channel3. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
2	W1C	0x0	ht_int_st2 High threshold interrupt state for channel2. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
1	W1C	0x0	ht_int_st1 High threshold interrupt state for channel1. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
0	W1C	0x0	ht_int_st0 High threshold interrupt state for channel0. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

SARADC_LT_INT_ST

Address: Operational Base(0x2AE00000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	lt_int_st15 Low threshold interrupt state for channel15. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
14	W1C	0x0	lt_int_st14 Low threshold interrupt state for channel14. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
13	W1C	0x0	lt_int_st13 Low threshold interrupt state for channel13. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

Bit	Attr	Reset Value	Description
12	W1C	0x0	lt_int_st12 Low threshold interrupt state for channel12. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
11	W1C	0x0	lt_int_st11 Low threshold interrupt state for channel11. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
10	W1C	0x0	lt_int_st10 Low threshold interrupt state for channel10. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
9	W1C	0x0	lt_int_st9 Low threshold interrupt state for channel9. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
8	W1C	0x0	lt_int_st8 Low threshold interrupt state for channel8. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
7	W1C	0x0	lt_int_st7 Low threshold interrupt state for channel7. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
6	W1C	0x0	lt_int_st6 Low threshold interrupt state for channel6. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
5	W1C	0x0	lt_int_st5 Low threshold interrupt state for channel5. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
4	W1C	0x0	lt_int_st4 Low threshold interrupt state for channel4. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
3	W1C	0x0	lt_int_st3 Low threshold interrupt state for channel3. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
2	W1C	0x0	lt_int_st2 Low threshold interrupt state for channel2. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
1	W1C	0x0	lt_int_st1 Low threshold interrupt state for channel1. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
0	W1C	0x0	lt_int_st0 Low threshold interrupt state for channel0. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

SARADC_MT_INT_ST

Address: Operational Base(0x2AE00000) + offset (0x011C)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	mt_int_st15 Between high and low threshold interrupt state for channel15. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
14	W1C	0x0	mt_int_st14 Between high and low threshold interrupt state for channel14. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
13	W1C	0x0	mt_int_st13 Between high and low threshold interrupt state for channel13. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
12	W1C	0x0	mt_int_st12 Between high and low threshold interrupt state for channel12. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
11	W1C	0x0	mt_int_st11 Between high and low threshold interrupt state for channel11. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
10	W1C	0x0	mt_int_st10 Between high and low threshold interrupt state for channel10. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
9	W1C	0x0	mt_int_st9 Between high and low threshold interrupt state for channel9. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
8	W1C	0x0	mt_int_st8 Between high and low threshold interrupt state for channel8. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
7	W1C	0x0	mt_int_st7 Between high and low threshold interrupt state for channel7. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
6	W1C	0x0	mt_int_st6 Between high and low threshold interrupt state for channel6. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
5	W1C	0x0	mt_int_st5 Between high and low threshold interrupt state for channel5. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
4	W1C	0x0	mt_int_st4 Between high and low threshold interrupt state for channel4. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
3	W1C	0x0	mt_int_st3 Between high and low threshold interrupt state for channel3. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

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Bit	Attr	Reset Value	Description
2	W1C	0x0	mt_int_st2 Between high and low threshold interrupt state for channel2. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
1	W1C	0x0	mt_int_st1 Between high and low threshold interrupt state for channel1. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
0	W1C	0x0	mt_int_st0 Between high and low threshold interrupt state for channel0. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

SARADC_DATA0

Address: Operational Base(0x2AE00000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data0 ADC channel 0 data.

SARADC_DATA1

Address: Operational Base(0x2AE00000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data1 ADC channel 1 data.

SARADC_DATA2

Address: Operational Base(0x2AE00000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data2 ADC channel 2 data.

SARADC_DATA3

Address: Operational Base(0x2AE00000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data3 ADC channel 3 data.

SARADC_DATA4

Address: Operational Base(0x2AE00000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data4 ADC channel 4 data.

SARADC_DATA5

Address: Operational Base(0x2AE00000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data5 ADC channel 5 data.

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SARADC_DATA6

Address: Operational Base(0x2AE00000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data6 ADC channel 6 data.

SARADC_DATA7

Address: Operational Base(0x2AE00000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data7 ADC channel 7 data.

SARADC_AUTO_CH_EN

Address: Operational Base(0x2AE00000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	auto_ch_en Enable channel in auto channel mode. Each bit can enable for one channel.

18.5 Application Notes

18.5.1 Timing Diagram

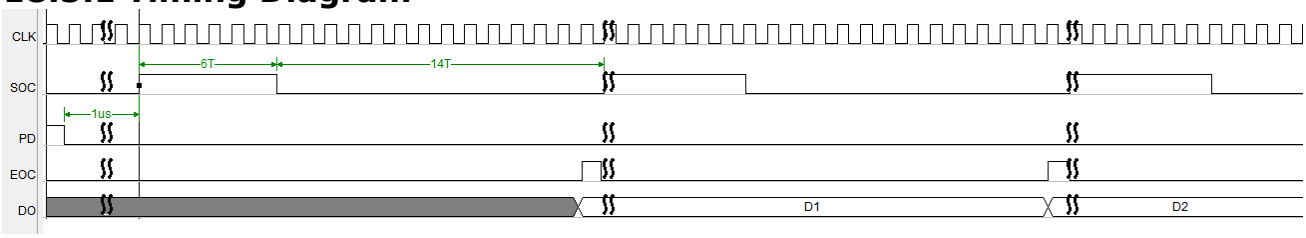

Fig. 18-2 SAR-ADC Timing Diagram

SAR-ADC timing diagram is shown in the figure above. When PD (power down) comes to low, wait 1us then assert SOC to start conversion. SOC should hold for 6 clock cycles (CLK), then after 14 clock cycle EOC pulse with conversion data (DO). CLK is suggested to be 20MHz, if frequency could not meet, set frequency close to 20MHz but not over 20MHz.

Don’t need to care the channel changing, this will be met by internal FSM. Also if software want to end conversion by setting register SARADC_CONV_CON, PD may not be asserted immediately but wait the latest conversion ends.

18.5.2 Series conversion mode

- Decide which channel should be used and whether auto_channel mode should be set. In auto_channel mode channel will be changed from 0-7 then to 0. Please refer to SARADC_CONV_CON register.
- Set SARADC_CONV_CON[4] to 1’b1, then conversion will start.
- If conversion wants to be ended, set SARADC_CONV_CON[7] to 1’b1.
- Conversion could be read from SARADC_DATAn (n is from 0-7).
- If threshold compare interrupt wants to be used, high/low threshold could be set, and interrupt should be set as application.

18.5.3 Single mode

- Decide which channel should be used and set SARADC_CONV_CON[3:0].
- Set SARADC_CONV_CON[5] to 1’b1.

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- Set SARADC_CONV_CON[4] to 1'b1, then conversion will start.
- Conversion only operates once then ends. PD will be asserted and PD status could be got by reading SARADC_STATUS.
- Conversion result could be read from SARADC_DATAn (n is from 0-7).

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Chapter 19 Temperature-Sensor ADC (TS-ADC)

19.1 Overview

TS-ADC Controller is used to control and get the temperature information. TS-ADC will convert for each enabled channel in loop after initial setting and can be stopped by software. If the temperature is high in a period of time, an interrupt is generated to the processor. If the temperature is over the high threshold for a period of time, the resulting TSHUT would be sent to CRU, and let CRU reset the entire chip, or via GPIO to PMIC. Also, if you find that the temperature is low in a period of time, an interrupt can be generated.
TS-ADC Controller supports the following features:

- Support to 6 TS-ADC channels (near chip center, big core, little core, GPU, NPU, DDR)
- The temperature for High and Low interrupt can be configured
- The temperature of system reset can be configurable
- The time interval of temperature detection can be configurable
- When detecting a high temperature, the time interval of temperature detection can be configurable
- High temperature debounce can be configurable
- An interrupt can be generated after TS-ADC converts all setting channels
- -40~125°C temperature range and 1°C temperature resolution

19.2 Block Diagram

TS-ADC controller comprises with:

- APB Interface
- TS-ADC control logic

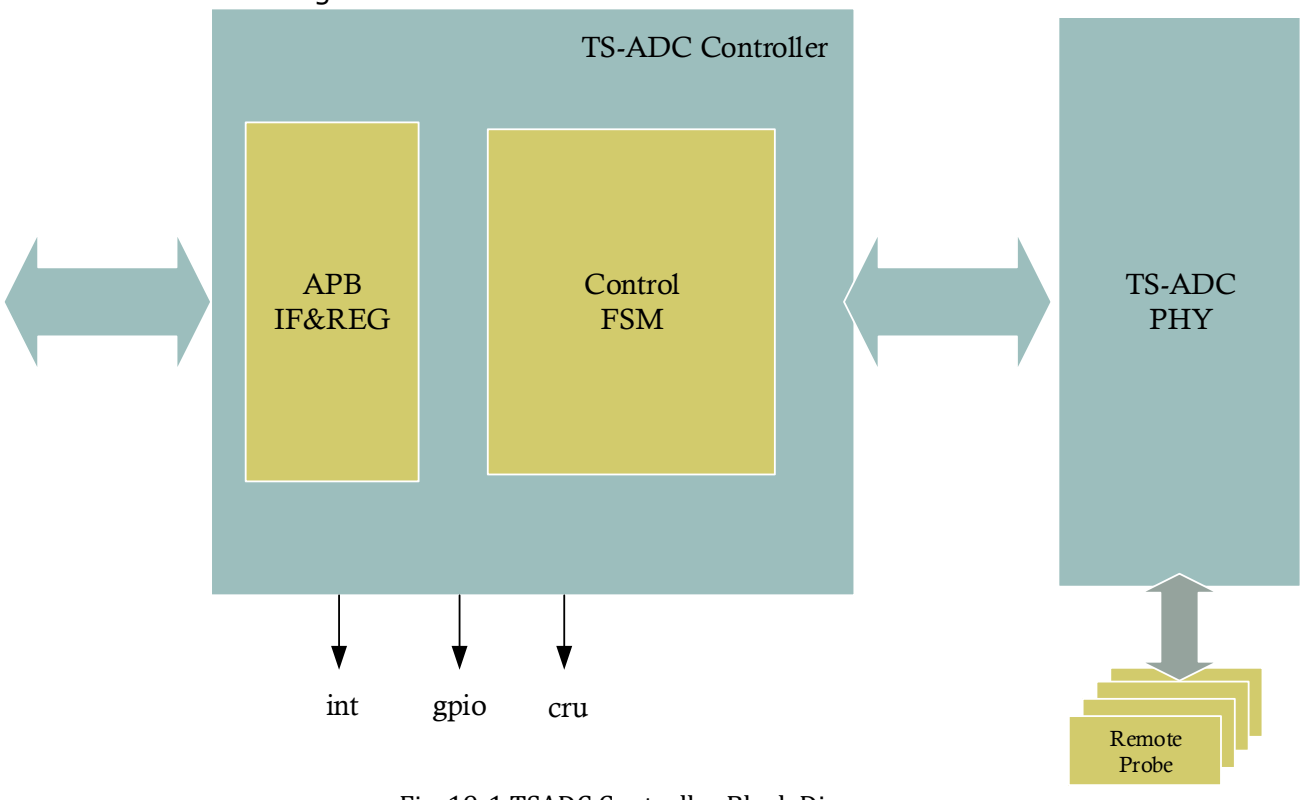

Fig. 19-1 TSADC Controller Block Diagram

19.3 Function Description

19.3.1 APB Interface

There is an APB Slave interface in TS-ADC Controller, which is used to configure the TS-ADC Controller registers and look up the temperature from the temperature sensor.

19.3.2 TS-ADC Controller

This block is used to control the TS-ADC PHY to meet the conversion timing and receive the temperature information from TS-ADC PHY.

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19.4 Register Description

19.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

19.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TSADC_USER_CON	0x0000	W	0x00000000	User control
TSADC_AUTO_CON	0x0004	W	0x00000000	Auto control
TSADC_AUTO_STATUS	0x0008	W	0x00000000	Status used in auto mode
TSADC_AUTO_SRC	0x000C	W	0x00000000	Channel select for tsadc in auto mode
TSADC_LT_EN	0x0010	W	0x00000000	Low temperature check logic enable
TSADC_HT_INT_EN	0x0014	W	0x00000000	High temperature interrupt enable
TSADC_GPIO_EN	0x0018	W	0x00000000	Temperature violation to gpio enable
TSADC_CRU_EN	0x001C	W	0x00000000	Temperature violation to cru enable
TSADC_LT_INT_EN	0x0020	W	0x00000000	Low temperature interrupt enable
TSADC_HLT_INT_PD	0x0024	W	0x00000000	High and low temperature interrupt status
TSADC_EOC_HSHUT_PD	0x0028	W	0x00000000	High temperature shut and round int status
TSADC_DATA0	0x002C	W	0x00000000	Channel0 data
TSADC_DATA1	0x0030	W	0x00000000	Channel1 data
TSADC_DATA2	0x0034	W	0x00000000	Channel2 data
TSADC_DATA3	0x0038	W	0x00000000	Channel3 data
TSADC_DATA4	0x003C	W	0x00000000	Channel4 data
TSADC_DATA5	0x0040	W	0x00000000	Channel5 data
TSADC_COMP0_INT	0x006C	W	0x00000000	High temperature interrupt threshold for channel0
TSADC_COMP1_INT	0x0070	W	0x00000000	High temperature interrupt threshold for channel1
TSADC_COMP2_INT	0x0074	W	0x00000000	High temperature interrupt threshold for channel2
TSADC_COMP3_INT	0x0078	W	0x00000000	High temperature interrupt threshold for channel3
TSADC_COMP4_INT	0x007C	W	0x00000000	High temperature interrupt threshold for channel4
TSADC_COMP5_INT	0x0080	W	0x00000000	High temperature interrupt threshold for channel5
TSADC_COMP0_SHUT	0x010C	W	0x00000000	High temperature shut threshold for channel0
TSADC_COMP1_SHUT	0x0110	W	0x00000000	High temperature shut threshold for channel1
TSADC_COMP2_SHUT	0x0114	W	0x00000000	High temperature shut threshold for channel2
TSADC_COMP3_SHUT	0x0118	W	0x00000000	High temperature shut threshold for channel3
TSADC_COMP4_SHUT	0x011C	W	0x00000000	High temperature shut threshold for channel4
TSADC_COMP5_SHUT	0x0120	W	0x00000000	High temperature shut threshold for channel5

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Name	Offset	Size	Reset Value	Description
TSADC_HIGH_INT_DEBOUNCE	0x014C	W	0x00000003	High interrupt debounce
TSADC_HIGH_TSHUT_DEBOUNCE	0x0150	W	0x00000003	High shut debounce
TSADC_AUTO_PERIOD	0x0154	W	0x00010000	Auto conversion period
TSADC_AUTO_PERIOD_HT	0x0158	W	0x00010000	Auto conversion period for high temperature
TSADC_COMP0_LOW_INT	0x015C	W	0x00000000	Low temperature threshold for channel0
TSADC_COMP1_LOW_INT	0x0160	W	0x00000000	Low temperature threshold for channel1
TSADC_COMP2_LOW_INT	0x0164	W	0x00000000	Low temperature threshold for channel2
TSADC_COMP3_LOW_INT	0x0168	W	0x00000000	Low temperature threshold for channel3
TSADC_COMP4_LOW_INT	0x016C	W	0x00000000	Low temperature threshold for channel4
TSADC_COMP5_LOW_INT	0x0170	W	0x00000000	Low temperature threshold for channel5
TSADC_T_SETUP	0x019C	W	0x0000002F	Timing for setup
TSADC_T_PW_EN	0x0200	W	0x00000027	Timing for pw_en
TSADC_T_EN_CLK	0x0204	W	0x00000001	Timing for en_clk
TSADC_T_NON_OV	0x0208	W	0x00000002	Timong for non_ov
TSADC_T_HOLD	0x020C	W	0x00000013	Timing for hold
TSADC_Q_MAX	0x0210	W	0x00000000	Max data used for data inversion
TSADC_STATIC_CON	0x0214	W	0x0280001B	Static control signal
TSADC_CLK_CH_PERIOD	0x021C	W	0x0000012B	CLK_CH_TS period control
TSADC_T_PW_CLK	0x0220	W	0x00000030	Timing for pw_clk

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

19.4.3 Detail Registers Description

TSADC_USER_CON

Address: Operational Base(0x2AE70000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:9	RO	0x00	reserved
8	RO	0x0	adc_status 1'b0: ADC stop 1'b1: Conversion in progress
7	R/WSC	0x0	start When software write 1 to this bit, start-of-conversion will be assert. This bit will be cleared after TSADC access finishing. Only when TSADC_USER_CON[5] = 1'b1, this bit takes effect.
6	RW	0x0	eoc_inten Enable eoc interrupt for each conversion. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	start_mode Start mode. 1'b0: TSADC controller will assert start_of_conversion after power up. 1'b1: The start_of_conversion will be controlled by TSADC_USER_CON[7].
4	RW	0x0	power_control ADC power control 1'b0: Power down 1'b1: Power up This bit is not enable when TSADC_AUTO_CON[0] is set to 1.
3:0	RW	0x0	input_src_sel ADC input source select in user mode. Can be changed from 0 - 15.

TSADC_AUTO_CON

Address: Operational Base(0x2AE70000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:9	RO	0x00	reserved
8	RW	0x0	tshut_polarity This bit is used to control the output signal polarity to gpio when the temperature is higher than threshold. 1'b0: Low active 1'b1: High active
7:3	RO	0x00	reserved
2	RW	0x0	round_int_en Int enable for round model. Used for auto model all channel set is sampled. 1'b1: Enable 1'b0: Disable
1	RW	0x0	q_sel 1'b0: Use tsadc_q as output (positive temperature coefficient) 1'b1: Use (q_max - tsadc_q) as output (negative temperature coefficient)
0	RW	0x0	auto_en Auto conversion enable 1'b0: TSADC controller works at user-define mode 1'b1: TSADC controller works at auto mode

TSADC_AUTO_STATUS

Address: Operational Base(0x2AE70000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ht_wram High temperature status 1'b0: TSADC data is not higher than ht shut temperature 1'b1: TSADC data is higher than ht shut temperature
2	RW	0x0	auto_status TSADC auto mode status 1'b0: Auto mode stop 1'b1: Auto mode in progress

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Bit	Attr	Reset Value	Description
1	W1C	0x0	last_tshut_cru Status for cru reset latest tshut, write 1 to clear.
0	W1C	0x0	last_tshut_gpio Status for gpio latest tshut, write 1 to clear.

TSADC_AUTO_SRC

Address: Operational Base(0x2AE70000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	auto_src Enable channel for TSADC in auto mode. Each bit can enable for one channel.

TSADC_LT_EN

Address: Operational Base(0x2AE70000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	low_temperature_vio_en Low temperature violation logic enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_HT_INT_EN

Address: Operational Base(0x2AE70000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	high_temperature_int_en High temperature interrupt enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_GPIO_EN

Address: Operational Base(0x2AE70000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	gpio_en Temperature violation to gpio enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_CRU_EN

Address: Operational Base(0x2AE70000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	cru_en Temperature violation to cru reset enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_LT_INT_EN

Address: Operational Base(0x2AE70000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	low_tempeture_int_en Low temperature interrupt enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_HLT_INT_PD

Address: Operational Base(0x2AE70000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	W1C	0x0000	lt_int_status Low temperature interrupt status for each channel.
15:0	W1C	0x0000	ht_int_status High temperature interrupt status for each channel.

TSADC_EOC_HSHUT_PD

Address: Operational Base(0x2AE70000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	W1C	0x0	round_int_pd Auto model interrupt for each round of all set channel.
16	W1C	0x0	usr_eoc_irq_pd User model end interrupt status.
15:0	W1C	0x0000	ht_shut_pd High temperature shut down status for each channel.

TSADC_DATA0

Address: Operational Base(0x2AE70000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	adc_data A/D value of the channel 0 last conversion.

TSADC_DATA1

Address: Operational Base(0x2AE70000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	adc_data A/D value of the channel 1 last conversion.

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TSADC_DATA2

Address: Operational Base(0x2AE70000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	adc_data A/D value of the channel 2 last conversion.

TSADC_DATA3

Address: Operational Base(0x2AE70000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	adc_data A/D value of the channel 3 last conversion.

TSADC_DATA4

Address: Operational Base(0x2AE70000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	adc_data A/D value of the channel 3 last conversion.

TSADC_DATA5

Address: Operational Base(0x2AE70000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	adc_data A/D value of the channel 3 last conversion.

TSADC_COMP0_INT

Address: Operational Base(0x2AE70000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_h_int_comp_src0 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP1_INT

Address: Operational Base(0x2AE70000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_h_int_comp_src1 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP2_INT

Address: Operational Base(0x2AE70000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	tsadc_h_int_comp_src2 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP3_INT

Address: Operational Base(0x2AE70000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_h_int_comp_src3 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP4_INT

Address: Operational Base(0x2AE70000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_h_int_comp_src4 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP5_INT

Address: Operational Base(0x2AE70000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_h_int_comp_src5 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP0_SHUT

Address: Operational Base(0x2AE70000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_shut_comp_src0 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP1_SHUT

Address: Operational Base(0x2AE70000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_shut_comp_src1 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is too high. TSHUT will be valid.

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TSADC_COMP2_SHUT

Address: Operational Base(0x2AE70000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_shut_comp_src2 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP3_SHUT

Address: Operational Base(0x2AE70000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_shut_comp_src3 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP4_SHUT

Address: Operational Base(0x2AE70000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_shut_comp_src4 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP5_SHUT

Address: Operational Base(0x2AE70000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_shut_comp_src5 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_HIGH_INT_DEBOUNCE

Address: Operational Base(0x2AE70000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt when temperature is higher than or equal to COMP_INT for "debounce" times.

TSADC_HIGH_TSHUT_DEBOUNCE

Address: Operational Base(0x2AE70000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate TSHUT when temperature is higher than or equal to COMP_SHUT for "debounce" times.

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TSADC_AUTO_PERIOD

Address: Operational Base(0x2AE70000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period When auto mode is enabled, this register controls the interleave between every conversion for all channel enabled of TSADC.

TSADC_AUTO_PERIOD_HT

Address: Operational Base(0x2AE70000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period This register controls the interleave between every conversion for all channel enabled of TSADC after the temperature is higher than or equal to COMP_SHUT or COMP_INT.

TSADC_COMP0_LOW_INT

Address: Operational Base(0x2AE70000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_l_int_comp_src0 TSADC low temperature level. TSADC output is lower than or equal to tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_COMP1_LOW_INT

Address: Operational Base(0x2AE70000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_l_int_comp_src1 TSADC low temperature level. TSADC output is lower than or equal to tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_COMP2_LOW_INT

Address: Operational Base(0x2AE70000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_l_int_comp_src2 TSADC low temperature level. TSADC output is lower than or equal to tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_COMP3_LOW_INT

Address: Operational Base(0x2AE70000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_l_int_comp_src3 TSADC low temperature level. TSADC output is lower than or equal to tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

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TSADC_COMP4_LOW_INT

Address: Operational Base(0x2AE70000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_l_int_comp_src4 TSADC low temperature level. TSADC output is lower than or equal to tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_COMP5_LOW_INT

Address: Operational Base(0x2AE70000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_l_int_comp_src5 TSADC low temperature level. TSADC output is lower than or equal to tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_T_SETUP

Address: Operational Base(0x2AE70000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x002f	t_setup The timing between TSADC power up and start conversion.

TSADC_T_PW_EN

Address: Operational Base(0x2AE70000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0027	t_pw_en The timing assert start conversion signal.

TSADC_T_EN_CLK

Address: Operational Base(0x2AE70000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	t_en_clk The timing between dis-assert start conversion signal (EN_TEMP_SEN_TS) and assert CLK_SEN_TS[8].

TSADC_T_NON_OV

Address: Operational Base(0x2AE70000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	t_non_ov The timing between each bit assertion of CLK_SENSE_TS.

TSADC_T_HOLD

Address: Operational Base(0x2AE70000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0013	t_hold The timing between dis-assert CLK_SENSE_TS and TSADC data valid.

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TSADC_Q_MAX

Address: Operational Base(0x2AE70000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	q_max This register used for TSADC_AUTO_CON[1] for invert output data.

TSADC_STATIC_CON

Address: Operational Base(0x2AE70000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	buf_vref_sel Offset control for temperature output code.
26:23	RW	0x5	buf_slope_sel Slope control for temperature output code.
22:21	RW	0x0	comp_i_trim Comparator current timing ports.
20:17	RW	0x0	vbe_i_trm Current timing ports for VBE in PTAT generator.
16:13	RW	0x0	verf_trim Reference voltage trimming ports for reference generator.
12:9	RW	0x0	bgr_r_trim BGR control ports in reference generator.
8:5	RW	0x0	bgr_i_trim BJT emitter current control ports in reference generator.
4:2	RW	0x6	avg_mode Average mode control ports for digital filter.
1	RW	0x1	en_dem Dynamic element matching enable port.
0	RW	0x1	en_ch Digital offset cancellation enable port.

TSADC_CLK_CH_PERIOD

Address: Operational Base(0x2AE70000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000012b	clk_ch_period Control the period of CLK_CH_TS.

TSADC_T_PW_CLK

Address: Operational Base(0x2AE70000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0030	t_pw_clk The timing for assertion of each bit of CLK_SENSE_TS.

19.5 Application Notes

19.5.1 Conversion Flow

The system works as following

1) Set the conversion channel in register TSADC_AUTO_SRC, jump channel is not suggested, the mapping between channel and modules is shown in the following table.
2) Temperature violation and other configuration may be set.
3) Set the bit[0] in register TSADC_AUTO_CON, then TS-ADC will work.
4) Then temperature information can be read from APB interface.

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5) If TS-ADC needs to be closed, set bit[0] in register TSADC_AUTO_CON to 1'b0.

Table 19-1 Channels Mapping

Channel	Module
0	near chip center
1	big core
2	little core
3	GPU
4	NPU
5	DDR

19.5.2 Timing Diagram

When TS-ADC start to work, the timing will follow the figure below.

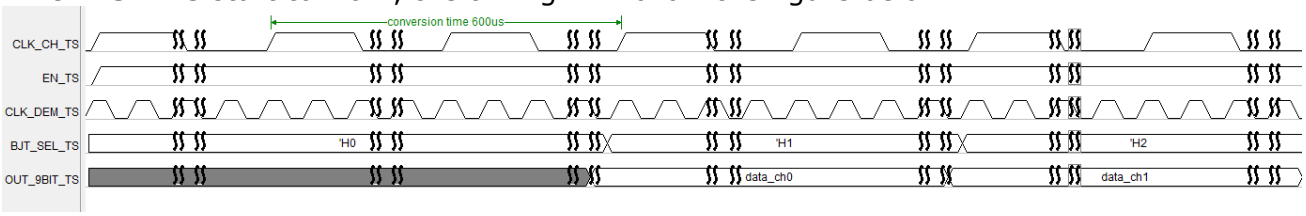

Fig. 19-2 Timing diagram for TS-ADC

When TS-ADC start to work, EN_TS comes to high. The conversion of one channel needs two CLK_CH_TS cycles and channel will change to the next one showing as BJT_SEL_TS. Output data from TS-ADC PHY will be kept until the next time this channel conversion is done.

CLK_DEM_TS is the main clock for TS-ADC, this clock frequency should be set to 2MHz which can be divided from 24MHz OSC clock. About this please refer to CRU section.

19.5.3 Temperature-to-Code Mapping

Table 19-2 Temperature Code Mapping

Temperature (℃)	ADC Output Data		
	Min	Typ(Dec)	Max
-40	-	220	-
25	-	285	-
85	-	345	-
125	-	385	-

Note:

Code to Temperature mapping of the Temperature sensor is a linear curve. Any temperature, code falling between to 2 given temperatures can be linearly interpolated. Code to Temperature mapping should be updated based on silicon results.

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Chapter 20 SPINLOCK

20.1 Overview

The hardware spinlock used for spinlock status storage. All the CPU can access spinlock to get the lock status.

20.2 Block Diagram

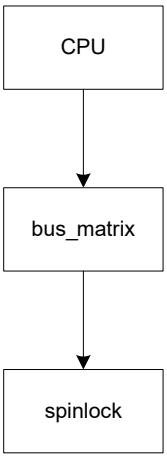

Fig. 20-1 spinlock in System

20.3 Register Description

20.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

20.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPINLOCK_STATUS_N (range of n is 0~63)	0x0+4*n	W	0x00000000	spinlock status controller register_n

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

20.3.3 Detail Register Description

SPINLOCK_STATUS_N

Address: Operational Base(0x2AB00000) + offset (0x0000+4*n)

Bit	Attr	Reset Value	Description
31:4	RO	0x000000	reserved
3:0	RW	0x0	spinlock_status when 4bits is 0, 4bits can be written with new value. when 4bits is not 0, 4bits cannot be written. when write data is 0x0000, 4bits clean to 0.

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Chapter 21 GPIO

21.1 Overview

GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. GPIO controls the output data and direction of external I/O pads. It can also read back the data on external pads using memory-mapped registers.
GPIO supports the following features:

- 32 bits APB data bus width
- Up to 32 independently configurable signals
- Software control registers with write mask for each bit of each signal
- Configurable debounce logic with a slow clock to debounce interrupts
- Configurable interrupt mode
- Four virtual OS with independent control registers can be supported
- In virtual OS mode, each OS has independent interrupt

21.2 Block Diagram

GPIO is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Interrupt Detection

Interrupt interface to or from interrupt controller.

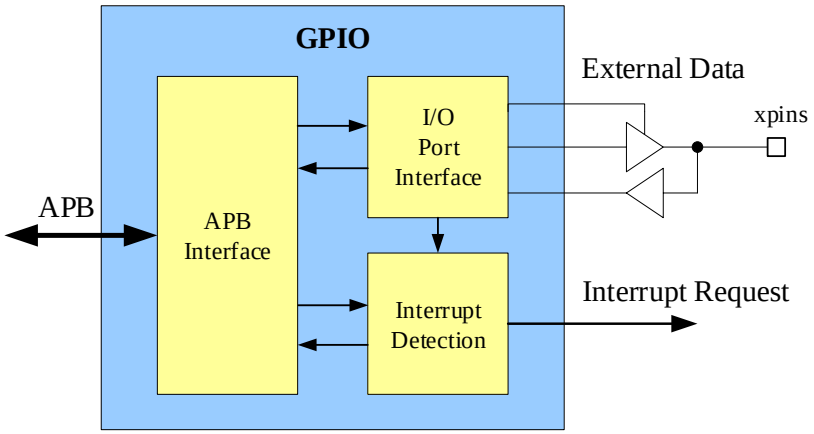

Fig. 21-1 GPIO Block Diagram

21.3 Function Description

21.3.1 Data Control

Under software control, the data and direction control for the signal are sourced from the port data registers (GPIO_SWPORT_DR_L/GPIO_SWPORT_DR_H) and direction control registers (GPIO_SWPORT_DDR_L/GPIO_SWPORT_DRR_H). The direction of the external I/O pad is controlled by the value of the port data direction registers. The data written to these memory-mapped registers gets mapped onto an output signal (gpio_port_ddr) of the GPIO peripheral. This output signal controls the direction of an external I/O pad. The default data direction is Input. The data written to the port data registers drives the output buffer (gpio_port_dr) of the I/O pad.

External data are input on the external data signal (gpio_ext_port). Reading the external signal register (GPIO_EXT_PORT) shows the value of this signal, regardless of the direction. This register is read-only, meaning that it cannot be written from the APB software interface.

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21.3.2 Interrupts

I/O port can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge
- Both the rising edge and the falling edge

The interrupts can be masked by programming the GPIO_INT_MASK_L/GPIO_INT_MASK_H registers. The interrupt status can be read before masking (GPIO_INT_RAWSTATUS) and after masking (GPIO_INT_STATUS).

For edge-sensitive interrupts, the Interrupt Service Routine (ISR) can clear the interrupt by writing a 1 to the corresponding bit of the GPIO_PORT_EOI_L/GPIO_PORT_EOI_H registers. This write operation also clears the interrupt status and raw status registers. Writing to the interrupt clear registers has no effect on level-sensitive interrupts. If level-sensitive interrupts cause the processor to interrupt, then the ISR can poll the interrupt raw status register until the interrupt source disappears, or it can write to the interrupt mask register to mask the interrupt before exiting the ISR. If the ISR exits without masking or disabling the interrupt prior to exiting, then the level-sensitive interrupt repeatedly requests an interrupt until the interrupt is cleared at the source.

The interrupts are combined into an active-high interrupt output signal. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its own mask bit.

Whenever I/O port is configured for interrupts, the data direction must be set to Input. If the data direction is reprogrammed to Output, then any pending edge-sensitive interrupts are not lost. However, no new interrupts are generated, and level-sensitive interrupts are lost.

Interrupt signals are internally synchronized to a system clock pclk_intr, which is connected to the APB bus clock pclk. Therefore, the pclk needs to be running for interrupt detection.

21.3.3 Debounce Operation

The external signal can be debounced to remove any spurious glitches that are less than half period of the external debouncing clock.

When an input interrupt signal is debounced using a slow debounce clock (external input clock dbclk or internal divided clock dbclk_div), the signal must be active for a minimum of one cycle of the debounce clock to guarantee that it is registered. Any input pulse widths less than half debounce clock period are bounced. A pulse width between half and one debounce clock width may or may not propagate, depending on its phase relationship to the debounce clock. If the input pulse spans rising edges and falling edge of the debounce clock, it is registered. If it spans only one edge, it is not registered.

The debounce function can be controlled by programming the debounce enable registers (GPIO_DEBOUNCE_L/GPIO_DEBOUNCE_H), debounce clock divide enable registers (GPIO_DBCLK_DIV_EN_L/GPIO_DBCLK_DIV_EN_H) and debounce clock divide control register (GPIO_DBCLK_DIV_CON).

21.3.4 Four OS Operation and Four Interrupts

To select this mode, virtual enable register should be set (GPIO_VIRTUAL_EN). Then all the configures can be allotted to four OS (for example OS_A, OS_B, OS_C, OS_D). OS_A will use the original address offset, OS_B will use the offset + 0x1000, OS_C will use the offset + 0x2000, OS_D will use the offset + 0x3000. The 32 bit I/O port should also be allotted to the OS by setting reg group registers (GPIO_REG_GROUP_L and GPIO_REG_GROUP_H). Once reg group is set, the I/O operation can only be used by the setting address offset.

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Each OS has its own interrupt for I/O port, this is depended on reg group.
If virtual enable register is disable, reg group can also be used to allotted I/O interrupt.
These four independent interrupts may be used for priority interrupt setting.

21.4 Register Description

21.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
GPIO0	0x27320000
GPIO1	0x2AE10000
GPIO2	0x2AE20000
GPIO3	0x2AE30000
GPIO4	0x2AE40000

21.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO_SWPORT_DR_L	0x0000	W	0x00000000	Port Data Register (Low)
GPIO_SWPORT_DR_H	0x0004	W	0x00000000	Port Data Register (High)
GPIO_SWPORT_DDR_L	0x0008	W	0x00000000	Port Data Direction Register (Low)
GPIO_SWPORT_DDR_H	0x000C	W	0x00000000	Port Data Direction Register (High)
GPIO_INT_EN_L	0x0010	W	0x00000000	Interrupt Enable Register (Low)
GPIO_INT_EN_H	0x0014	W	0x00000000	Interrupt Enable Register (High)
GPIO_INT_MASK_L	0x0018	W	0x00000000	Interrupt Mask Register (Low)
GPIO_INT_MASK_H	0x001C	W	0x00000000	Interrupt Mask Register (High)
GPIO_INT_TYPE_L	0x0020	W	0x00000000	Interrupt Level Register (Low)
GPIO_INT_TYPE_H	0x0024	W	0x00000000	Interrupt Level Register (High)
GPIO_INT_POLARITY_L	0x0028	W	0x00000000	Interrupt Polarity Register (Low)
GPIO_INT_POLARITY_H	0x002C	W	0x00000000	Interrupt Polarity Register (High)
GPIO_INT_BOTHEDGE_L	0x0030	W	0x00000000	Interrupt Both Edge Type Register (Low)
GPIO_INT_BOTHEDGE_H	0x0034	W	0x00000000	Interrupt Both Edge Type Register (High)
GPIO_DEBOUNCE_L	0x0038	W	0x00000000	Debounce Enable Register (Low)
GPIO_DEBOUNCE_H	0x003C	W	0x00000000	Debounce Enable Register (High)
GPIO_DBCLK_DIV_EN_L	0x0040	W	0x00000000	DBCLK Divide Enable Register (Low)
GPIO_DBCLK_DIV_EN_H	0x0044	W	0x00000000	DBCLK Divide Enable Register (High)
GPIO_DBCLK_DIV_CON	0x0048	W	0x00000001	DBCLK Divide Control Register
GPIO_INT_STATUS	0x0050	W	0x00000000	Interrupt Status Register
GPIO_INT_RAWSTATUS	0x0058	W	0x00000000	Interrupt Raw Status Register
GPIO_PORT_EOI_L	0x0060	W	0x00000000	Interrupt Clear Register (Low)
GPIO_PORT_EOI_H	0x0064	W	0x00000000	Interrupt Clear Register (High)
GPIO_EXT_PORT	0x0070	W	0x00000000	External Port Data Register
GPIO_VER_ID	0x0078	W	0x010219C8	Version ID Register
GPIO_STORE_ST_L	0x0080	W	0x00000000	Status Store Register (Low)
GPIO_STORE_ST_H	0x0084	W	0x00000000	Status Store Register (High)
GPIO_GPIO_REG_GROUP_L	0x0100	W	0x0000FFFF	GPIO Group Control
GPIO_GPIO_REG_GROUP_H	0x0104	W	0x0000FFFF	GPIO Group Control

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Name	Offset	Size	Reset Value	Description
GPIO_GPIO_VIRTUAL_EN	0x0108	W	0x00000000	GPIO Virtual Enable
GPIO_GPIO_REG_GROUP1_L	0x0110	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP1_H	0x0114	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP2_L	0x0118	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP2_H	0x011C	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP3_L	0x0120	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP3_H	0x0124	W	0x00000000	GPIO Group Control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

21.4.3 Detail Registers Description

GPIO_SWPORT_DR_L

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_low Output data for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the lower 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DR_H

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_high Output data for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the upper 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DDR_L

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_low Data direction for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the lower 16 bits of I/O Port.

GPIO_SWPORT_DDR_H

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_high Data direction for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the upper 16 bits of I/O Port.

GPIO_INT_EN_L

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_en_low Allows each bit of the lower 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_EN_H

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_en_high Allows each bit of the upper 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_MASK_L

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_mask_low Controls whether an interrupt on the lower 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_MASK_H

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_mask_high Controls whether an interrupt on the upper 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_TYPE_L

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_type_low Controls the type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_TYPE_H

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_type_high Controls the type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_POLARITY_L

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_polarity_low Controls the polarity of edge or level sensitivity that can occur on the lower 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_POLARITY_H

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_polarity_high Controls the polarity of edge or level sensitivity that can occur on the upper 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_BOTHEDGE_L

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_bothedge_low Controls the edge type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_low and int_polarity_low for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_low and int_polarity_low registers.

GPIO_INT_BOTHEDGE_H

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_bothedge_high Controls the edge type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_high and int_polarity_high for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_high and int_polarity_high registers.

GPIO_DEBOUNCE_L

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_low Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DEBOUNCE_H

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_high Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DBCLK_DIV_EN_L

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_low Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the lower 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_low is set to 0.

GPIO_DBCLK_DIV_EN_H

Address: **Operational Base** + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_high Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the upper 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_high is set to 0.

GPIO_DBCLK_DIV_CON

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000001	dbclk_div_con dbclk_div = dbclk / (dbclk_div_con + 1)

GPIO_INT_STATUS

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_status Interrupt status of I/O Port.

GPIO_INT_RAWSTATUS

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_rawstatus Interrupt raw status of I/O Port (premasking bits).

GPIO_PORT_EOI_L

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/WSC	0x0000	port_eoi_low Controls the clearing of edge type interrupts from the lower 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_PORT_EOI_H

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/WSC	0x0000	port_eoi_high Controls the clearing of edge type interrupts from the upper 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_EXT_PORT

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ext_port This register always reflects the value of the signals on the external I/O Port.

GPIO_VER_ID

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x010219c8	ver_id Version ID.

GPIO_STORE_ST_L

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	store_st_l This reigister can store the state for each GPIO by user writting to this register.

GPIO_STORE_ST_H

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	store_st_h This reigister can store the state for each GPIO by user writting to this register.

GPIO_GPIO_REG_GROUP_L

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xffff	gpio_reg_group_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP0 with offset 0x0000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag0 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP_H

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xffff	gpio_reg_group_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP0 with offset 0x0000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag0 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_VIRTUAL_EN

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	gpio_virtual_en 1'b1: Enable virtual, four OS supported 1'b0: Disable virtual. Only in GROUP0 with offset 0x0000.

GPIO_GPIO_REG_GROUP1_L

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio_reg_group1_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP1 with offset 0x1000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag1 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP1_H

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group1_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP1 with offset 0x1000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag1 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP2_L

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group2_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP2 with offset 0x2000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag2 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP2_H

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio_reg_group2_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP2 with offset 0x2000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag2 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP3_L

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group3_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP3 with offset 0x3000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag3 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP3_H

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group3_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP3 with offset 0x3000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag3 1'b0: GPIO interrupt connect to other interrupt

21.5 Application Notes

- Reading from an unused location or unused bits in a particular register always returns zeros. There is no error mechanism in the APB.
- Programming the GPIO registers for interrupt detection should be completed prior to enabling the interrupts in order to prevent spurious glitches on the interrupt output signal to the interrupt controller.

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Chapter 22 Digital Audio Codec

22.1 Overview

For the convenience of writing, we also name Digital Audio Codec as ACDCDIG_DSM. ACDCDIG_DSM is a 16-bit digital audio encoder which supports multiple sample rates. It is mainly composed of digital DAC. The aim of digital DAC is to process the data received from I2S/PCM interface through filters, volume control and modulation.
The ACDCDIG_DSM supports the following features.

- Support 8-bit APB and AHB bus slave interface
- Support 2-channel digital DAC
- Support I2S/PCM interface
- Support I2S/PCM master and slave mode
- Support 2-channel audio receiving in I2S mode
- Support 2-channel audio receiving in PCM mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and LRCK polarity
- Support 16 bit sample resolution
- Support programmable left and right channel exchangeable in I2S mode and PCM mode
- Support three modes of mixing for every digital DAC channel
- Support volume control
- Support programmable negative and positive volume gain

22.2 Block Diagram

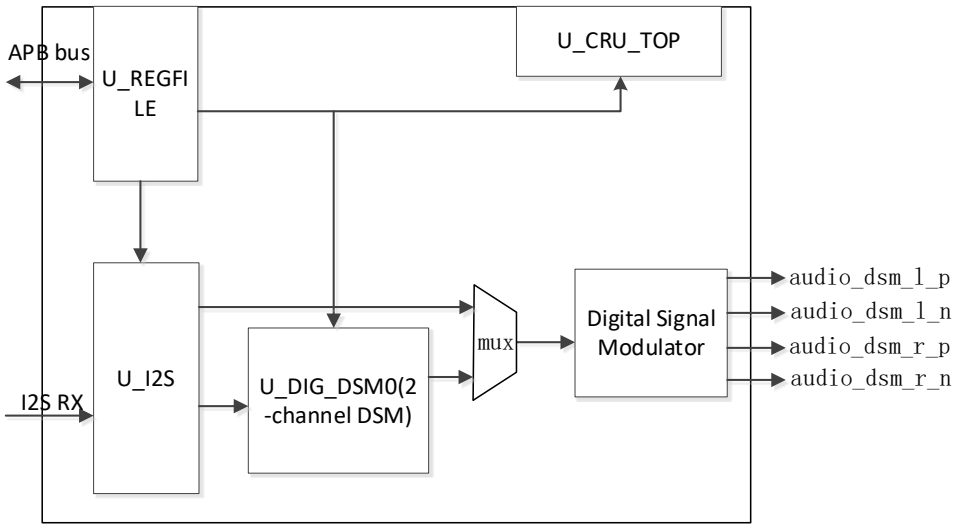

Fig. 22-1 ACDCDIG_DSM Block Diagram

ACDCDIG_DSM_RF
The ACDCDIG_DSM_RF implements the 8-bit APB/AHB slave operation through APB/AHB bus. It is responsible for configuring the operation registers of other modules.
ACDCDIG_DSM_CRU
The ACDCDIG_DSM_CRU implements clock and reset generation function. It is responsible for generating sample clock, digital DAC operation clock and I2S operation clock.
ACDCDIG_DSM
There are 2 digital DAC channels. The digital DAC receives audio data from ACDC_I2S module. It includes one CIC filter, one high-pass filter, several low-pass decimation filters and other audio signal processing related modules. The output of digital DAC is sent to DSM modular before transmitting outside.
ACDCDIG_DSM_I2S
The I2S/PCM audio interface can be configured to master mode or slave mode. In Master

Mode, SCLK and LRCK are configured as output. In slave mode, SCLK and LRCK are configured as input. The ACDCDIG_DSM_I2S module can only operate in RX mode. When in RX mode, it receives audio data from I2S RX interface and sends it to digital DAC.

DSM Modulator

It is a modulator that converts 16 bits audio sample data to 1 bit audio data.

22.3 Function description

The I2S/PCM interface of Digital Audio Codec is connected to the I2S1 controller. Please refer to the I2S chapter for detailed information about I2S and PCM format that Digital Audio Codec supports.

22.3.1 Filters of Digital DAC

I2S module receives two-channel audio data from I2S RX interface and drives it to the digital DAC which supports mixing function or directly to the DSM modulator. How to pour 2-channel audio data into 2-channel digital DAC can be achieved by programming mixing mode.

The 2-channel digital DAC includes a high-pass filter and a maximum of 5 half-band filters. The high-pass filter is used to filter DC components in audio data stream. Result of high-pass filter is sent to the digital DAC volume control module. The input of 5 half-band filters comes from output of volume control module with each perform 2-times interpolation. But not all of them are working all the time. How many of them are needed to work depends on the sample rate of digital DAC. The result of half-band filters is sent to a modulator.

22.3.2 Volume Control

For digital DAC, output of high-pass filters is fed into volume control module. The volume control module inside digital DAC contains several sub-modules such as peak detect, frequency cross zero detect, LIMITER and digital gain control. It can be digitally attenuated over a range of -96dB~0dB in 0.375dB/step for negative gain and amplified over a range of 0dB~96dB in 0.375dB/step for positive gain. Whether is attenuated or amplified can be software programmed.

22.4 Register Description

22.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

22.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
ACDCDIG_DSM_DSMVUCTL	0x0000	W	0x00000001	DAC Volume Control Register
ACDCDIG_DSM_DSMVUCTIME	0x0004	W	0x00000000	DAC Volume Control Time Limit Register
ACDCDIG_DSM_DSMDIGEN	0x0008	W	0x00000000	DAC Digital Enable Register
ACDCDIG_DSM_DSMCLKCTRL	0x000C	W	0x00000000	DAC Clock Control Register
ACDCDIG_DSM_DSMINTMOD_DIV	0x0014	W	0x00000007	DAC Integer Clock Divider Register
ACDCDIG_DSM_DSMINTSCLK_DIV	0x0020	W	0x0000001F	I2S SCLK RX Integer Divider Register
ACDCDIG_DSM_DSM_DIV	0x0024	W	0x00000003	DSM Mode Integer Divider Register
ACDCDIG_DSM_DSM_CTRL	0x0028	W	0x00000000	DSM Mode Control Register
ACDCDIG_DSM_DSMCFG1	0x0044	W	0x00000004	DAC Configure Register 1
ACDCDIG_DSM_DSMMUTE	0x0048	W	0x00000000	DAC Mute Control Register

Name	Offset	Size	Reset Value	Description
ACDCDIG_DSM_DSMMUTEST	0x004C	W	0x00000000	DAC Mute Status Register
ACDCDIG_DSM_DSMVOLL0	0x0050	W	0x00000000	Volume of DAC Left Channel 0 Register
ACDCDIG_DSM_DSMVOLL1	0x0054	W	0x00000000	Volume of DAC Left Channel 1 Register
ACDCDIG_DSM_DSMVOLL2	0x0058	W	0x00000000	Volume of DAC Left Channel 2 Register
ACDCDIG_DSM_DSMVOLL3	0x005C	W	0x00000000	Volume of DAC Left Channel 3 Register
ACDCDIG_DSM_DSMVOLR0	0x0060	W	0x00000000	Volume of DAC right Channel 0 Register
ACDCDIG_DSM_DSMVOLR1	0x0064	W	0x00000000	Volume of DAC right Channel 1 Register
ACDCDIG_DSM_DSMVOLR2	0x0068	W	0x00000000	Volume of DAC right Channel 2 Register
ACDCDIG_DSM_DSMVOLR3	0x006C	W	0x00000000	Volume of DAC right Channel 3 Register
ACDCDIG_DSM_DSMVOGP	0x0070	W	0x00000000	DAC Volume Gain Polarity Register
ACDCDIG_DSM_DSMRVOLL0	0x0074	W	0x000000FF	Internal Volume of DAC Left Channel 0 Register
ACDCDIG_DSM_DSMRVOLL1	0x0078	W	0x00000000	Internal Volume of DAC Left Channel 1 Register
ACDCDIG_DSM_DSMRVOLL2	0x007C	W	0x00000000	Internal Volume of DAC Left Channel 2 Register
ACDCDIG_DSM_DSMRVOLL3	0x0080	W	0x00000000	Internal Volume of DAC Left Channel 3 Register
ACDCDIG_DSM_DSMRVOLR0	0x0084	W	0x000000FF	Internal Volume of DAC right Channel 0 Register
ACDCDIG_DSM_DSMRVOLR1	0x0088	W	0x00000000	Internal Volume of DAC right Channel 1 Register
ACDCDIG_DSM_DSMRVOLR2	0x008C	W	0x00000000	Internal Volume of DAC right Channel 2 Register
ACDCDIG_DSM_DSMRVOLR3	0x0090	W	0x00000000	Internal Volume of DAC right Channel 3 Register
ACDCDIG_DSM_DSMLMT0	0x0094	W	0x00000000	DAC Limiter Register 0
ACDCDIG_DSM_DSMLMT1	0x0098	W	0x00000000	DAC Limiter Register 1
ACDCDIG_DSM_DSMLMT2	0x009C	W	0x00000000	DAC Limiter Register 2
ACDCDIG_DSM_DSMMIXCTRLL	0x00A0	W	0x00000000	DAC Mixing Control Register Of Left Channels
ACDCDIG_DSM_DSMMIXCTRLR	0x00A4	W	0x00000000	DAC Mixing Control Register Of right Channels
ACDCDIG_DSM_DSMHPF	0x00A8	W	0x00000000	DAC High-pass Filter Control Register
ACDCDIG_DSM_DSM_I2S_RXCR0	0x010C	W	0x0000000F	Receive Operation Control Register 0
ACDCDIG_DSM_DSM_I2S_RXCR1	0x0110	W	0x00000000	Receive Operation Control Register 1
ACDCDIG_DSM_DSM_I2S_CKR0	0x0114	W	0x00000000	Clock Generation Register 0
ACDCDIG_DSM_DSM_I2S_CKR1	0x0118	W	0x00000000	Clock Generation Register 1

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Name	Offset	Size	Reset Value	Description
ACDCDIG_DSM_DSM_I2S_XFER	0x011C	W	0x00000000	Transfer Start Register
ACDCDIG_DSM_DSM_I2S_CLR	0x0120	W	0x00000000	SCLK Domain Logic Clear Register
ACDCDIG_DSM_DSM_VERSION	0x0140	W	0x00000010	Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

22.4.3 Detail Registers Description

ACDCDIG_DSM_DSMVUCTL

Address: Operational Base(0x2A6D0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	dac_byps Digital DAC volume control bypass. 1'b0: Digital DAC volume control enable 1'b1: Digital DAC volume control bypass
1	RW	0x0	dacfade Digital DAC volume adjust mode. 1'b0: Update to new volume immediately. 1'b1: Update volume as daczdt field describes.
0	RW	0x1	daczdt Digital DAC volume cross zero detect enable. It works when dac_byps is 1'b0 and dacfade is 1'b1. 1'b0: Volume adjusts every sample. 1'b1: Volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets.

ACDCDIG_DSM_DSMVUCTIME

Address: Operational Base(0x2A6D0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacvuct Volume control time limit, valid only in fade cross zero mode. Time limit = dacvuct*(1/sample rate) Unit: Sample rate

ACDCDIG_DSM_DSMDIGEN

Address: Operational Base(0x2A6D0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	dacglben Global enable of all Digital DAC channels. Only when dacglben and the enable signal corresponding to each Digital DAC channel is valid before starting work. 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	dacen_l0r1 Digital DAC left channel 0 and right channel 1 enable. 1'b0: Disable 1'b1: Enable

ACDCDIG_DSM_DSMCLKCTRL

Address: Operational Base(0x2A6D0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	dac_cke Digital DAC operation clock enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	i2srx_cke Clock enable of internal I2S RX channel. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cke_bclkrx Clock enable of sclk_out_rx. 1'b0: Disable 1'b1: Enable
2	RW	0x0	dac_sync_ena Enable of the synchronization signal used internally generated by Digital DAC. 1'b0: Disable 1'b1: Enable
1	RO	0x0	dac_sync_status There is a counter to generate synchronization signal of Digital DAC. In order to ensure the integrity of synchronization signal, it is necessary to read back dac_sync_status to judge whether the counter stops working when dac_sync_ena is set from 1'b1 to 1'b0. If the signal is read back to 1'b0, it means that the counter stops working and the synchronization signal of Digital DAC is complete.
0	RW	0x0	dac_mod_attenu_en When enabled, the input of the Digital DAC modulator is attenuated by 6dB, and the output of the Digital DAC modulator is increased by 6dB. 1'b0: Disable 1'b1: Enable

ACDCDIG_DSM_DSMINTMOD_DIV

Address: Operational Base(0x2A6D0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x07	int_div_con Integer clock divider to provide 6.144/5.644/4.096MHz sample clock for internal filters. Make sure that int_div_con is an odd number between 7(8 times division) and 15(16 times division).

ACDCDIG_DSM_DSMINTSCLK_DIV

Address: Operational Base(0x2A6D0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	sckrxdiv Integer clock divider to generate sclk_out_rx when I2S RX works in master mode. It is ignored when in slave mode. Sckrxdiv=((frequency of input operation clock)/(frequency of sclk_out_rx))-1. Sckrxdiv can be any value from 0 to 255.

ACDCDIG_DSM_DSM_DIV

Address: Operational Base(0x2A6D0000) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	audio_dsm_div DSM mode division of Digital DAC's operation clock. The operation clock frequency of DSM module is equal to the input operation clock frequency of Digital DAC's divided by audio_dsm_div+1. It's recommended that audio_dsm_div is set 8'h3.

ACDCDIG_DSM_DSM_CTRL

Address: Operational Base(0x2A6D0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	dsm_mode_cke Clock enable of 1-bit DSM modulator 1'b0: Disable 1'b1: Enable
5:4	RW	0x0	dsm_mode Audio DSM mode selection 2'b01: Audio DSM mode 0. The input of 1-bit DSM modulator is from the last filter of Audio DAC. 2'b10: Audio DSM mode 1. The input of 1-bit DSM modulator is directly from output of I2S RX inside the ACDCDIG. Others: Reserved
3	RW	0x0	dsm_en 1-bit DSM modulator enable 1'b0: Disable 1'b1: Enable
2:0	RW	0x0	dith_sel Dith mode selection of 1-bit DSM modulator.

ACDCDIG_DSM_DSMCFG1

Address: Operational Base(0x2A6D0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x1	dacsrt Sample rates of Digital DAC when in audio DSM mode 0. This field is ignored when in audio DSM mode 1. 3'b000: 12kHz/11.024kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 32kHz/48kHz/44.1kHz 3'b011: 96kHz/88.2kHz/64kHz 3'b100: 192kHz/176.4kHz/128kHz 3'b101~3'b111: Reserved
1:0	RO	0x0	reserved

ACDCDIG_DSM_DSMMUTE

Address: Operational Base(0x2A6D0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dacunmt 1'b0: DAC normal mode 1'b1: DAC unmute mode. In this mode, DAC volume control block will adjust volume to match the value in DACVOLL* and DACVOLR*.

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Bit	Attr	Reset Value	Description
0	RW	0x0	dacmt 1'b0: DAC normal mode 1'b1: DAC mute mode

ACDCDIG_DSM_DSMMUTEST

Address: Operational Base(0x2A6D0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	unmutest_l0r1 Unmute status for Digital DAC left channel 0 and right channel 1. When unmute is done, it indicates that internal volume is equal to the value programmed in DACVOLL* and DACVOLR*. 1'b0: Unmute not done 1'b1: Unmute done
3:1	RO	0x0	reserved
0	RO	0x0	mutest_l0r1 Mute status for Digital DAC left channel 0 and right channel 1. 1'b0: Not mute 1'b1: Mute

ACDCDIG_DSM_DSMVOLL0

Address: Operational Base(0x2A6D0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv0 Volume of Digital DAC left channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DSM_DSMVOLL1

Address: Operational Base(0x2A6D0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv1 Volume of Digital DAC left channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DSM_DSMVOLL2

Address: Operational Base(0x2A6D0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	daclv2 Volume of Digital DAC left channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DSM_DSMVOLL3

Address: Operational Base(0x2A6D0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	daclv3 Volume of Digital DAC left channel 3. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DSM_DSMVOLR0

Address: Operational Base(0x2A6D0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacrv0 Volume of Digital DAC right channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DSM_DSMVOLR1

Address: Operational Base(0x2A6D0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv1 Volume of Digital DAC right channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DSM_DSMVOLR2

Address: Operational Base(0x2A6D0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv2 Volume of Digital DAC right channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DSM_DSMVOLR3

Address: Operational Base(0x2A6D0000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv3 Volume of Digital DAC right channel 3. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DSM_DSMVOGP

Address: Operational Base(0x2A6D0000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	volgpr1 Gain polarity for the volume of Digital DAC right channel 1. 1'b0: Negative gain 1'b1: Positive gain
0	RW	0x0	volgpl0 Gain polarity for the volume of Digital DAC left channel 0. 1'b0: Negative gain 1'b1: Positive gain

ACDCDIG_DSM_DSMRVOLL0

Address: Operational Base(0x2A6D0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvoll0 Internal real-time volume of Digital DAC left channel 0.

ACDCDIG_DSM_DSMRVOLL1

Address: Operational Base(0x2A6D0000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll1 Internal real-time volume of Digital DAC left channel 1.

ACDCDIG_DSM_DSMRVOLL2

Address: Operational Base(0x2A6D0000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll2 Internal real-time volume of Digital DAC left channel 2.

ACDCDIG_DSM_DSMRVOLL3

Address: Operational Base(0x2A6D0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll3 Internal real-time volume of Digital DAC left channel 3.

ACDCDIG_DSM_DSMRVOLR0

Address: Operational Base(0x2A6D0000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvolr0 Internal real-time volume of Digital DAC right channel 0.

ACDCDIG_DSM_DSMRVOLR1

Address: Operational Base(0x2A6D0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr1 Internal real-time volume of Digital DAC right channel 1.

ACDCDIG_DSM_DSMRVOLR2

Address: Operational Base(0x2A6D0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr2 Internal real-time volume of Digital DAC right channel 2.

ACDCDIG_DSM_DSMRVOLR3

Address: Operational Base(0x2A6D0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr3 Internal real-time volume of Digital DAC right channel 3.

ACDCDIG_DSM_DSMLMT0

Address: Operational Base(0x2A6D0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	limen LIMITER enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	limdct Limiter detect mode. 1'b0: (Left channel + right channel)/2 1'b0: Left channel or right channel independently

ACDCDIG_DSM_DSMLMT1

Address: Operational Base(0x2A6D0000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	atk_rate LIMITER attack rate=(power(2, atk_rate)*(8*clk)), clk is such as 4.096Mhz, 5.6448Mhz, 6.144Mhz.
3:0	RW	0x0	rls_rate LIMITER release rate=(power(2, rls_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz.

ACDCDIG_DSM_DSMLMT2

Address: Operational Base(0x2A6D0000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	max_lilmt The highest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step
3	RO	0x0	reserved
2:0	RW	0x0	min_lilmt The lowest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step

ACDCDIG_DSM_DSMMIXCTRLL

Address: Operational Base(0x2A6D0000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_l0 Digital DAC left channel 0 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

ACDCDIG_DSM_DSMMIXCTRLR

Address: Operational Base(0x2A6D0000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_r0 Digital DAC right channel 1 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

ACDCDIG_DSM_DSMHPF

Address: Operational Base(0x2A6D0000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	hpfcf High-pass filter control. 2'b00: 80Hz 2'b01: 100Hz 2'b10: 120Hz 2'b11: 140Hz
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	hpfen_l0r1 High-pass filter enable for left channel 0 and right channel 1. 1'b0: High-pass filter is disabled. 1'b1: High-pass filter is enabled.

ACDCDIG_DSM_DSM_I2S_RXCR0

Address: Operational Base(0x2A6D0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	pbm PCM bus mode 2'b00: PCM no delay mode 2'b01: PCM delay 1 mode 2'b10: PCM delay 2 mode 2'b11: PCM delay 3 mode
5	RW	0x0	tfs Transfer format select 1'b0: I2S format 1'b1: PCM format
4:0	RW	0x0f	vdw Valid data width 5'b00000~5'b01110: Reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit ..... 5'b11100: 29bit 5'b11101: 30bit 5'b11110: 31bit 5'b11111: 32bit

ACDCDIG_DSM_DSM_I2S_RXCR1

Address: Operational Base(0x2A6D0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	rcsr Channel select 2'b00: Two channel Others: Reserved
5	RO	0x0	reserved
4	RW	0x0	cex Exchange left channel and right channel in the every receive line. 1'b0: Not exchange 1'b1: Exchange
3	RO	0x0	reserved
2	RW	0x0	fbm First bit mode 1'b0: MSB 1'b1: LSB

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	ibm I2S bus mode 2'b00: I2S normal 2'b01: I2S Left justified 2'b10: I2S Right justified 2'b11: Reserved

ACDCDIG_DSM_DSM_I2S_CKR0

Address: Operational Base(0x2A6D0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	rsd I2S rx sclk divider for rx_lrck generator. 2'b00: 64 2'b01: 128 2'b10~2'b11: 256
1:0	RO	0x0	reserved

ACDCDIG_DSM_DSM_I2S_CKR1

Address: Operational Base(0x2A6D0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	mss Master/slave mode select 1'b0: Master mode(sclk output) 1'b1: Slave mode(sclk input)
2	RW	0x0	ckp Sclk polarity 1'b0: Sample data at posedge sclk and drive data at negedge sclk. 1'b1: Sample data at negedge sclk and drive data at posedge sclk.
1	RW	0x0	rlp 1'b0: Normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal: high valid) 1'b1: Opposite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal: low valid)
0	RO	0x0	reserved

ACDCDIG_DSM_DSM_I2S_XFER

Address: Operational Base(0x2A6D0000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
0	RO	0x0	reserved

ACDCDIG_DSM_DSM_I2S_CLR

Address: Operational Base(0x2A6D0000) + offset (0x0120)

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Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxc This is a self-cleared bit. Write 1'b1 to clear all receive logic. This bit can be set only when rxs is 1'b0. After writing rxc to 1'b1, wait until rxc become 1'b0 by polling rxc.
0	RO	0x0	reserved

ACDCDIG_DSM_DSM_VERSION

Address: Operational Base(0x2A6D0000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x10	ver Version of DSM.

22.5 Interface Description

The I2S RX interface of Digital Audio Codec is connected to the TX interface of I2S1 when GRF_AUDIO_CON[14] is set to 1'b1.

When operating in audio DSM mode 0 or 1, Digital Audio Codec outputs two pairs of differential signals encoded in DSM format. The following table shows the ACDCDIG_DSM interface description for audio DSM mode.

Table 22-1 Digital Audio Codec M0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
AUDIO_DSM_L_P	O	SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/CAN0_RX_M0/PWM2_CH2_M0/GPIO2_A0_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'h3
AUDIO_DSM_L_N	O	SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'h3
AUDIO_DSM_R_P	O	SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[11:8]=4'h3
AUDIO_DSM_R_N	O	SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/CAN1_TX_M0/I3C1_SDA_M1/GPIO2_A3_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[15:12]=4'h3

Table 22-2 Digital Audio Codec M1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
AUDIO_DSM_L_P	O	DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[3:0]=4'h1
AUDIO_DSM_L_N	O	DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[7:4]=4'h1

Module Pin	Direction	Pad Name	IOMUX Setting
AUDIO_DSM_R_P	O	DSM_AUD_RP_M1/HDMI_TX_SCL/I2C2_SCL_M3/CAN0_TX_M1/UART9_TX_M2/PWM2_CH0_M1/GPIO4_C2_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[11:8]=4'h1
AUDIO_DSM_R_N	O	DSM_AUD_RN_M1/HDMI_TX_SDA/I2C2_SDA_M3/CAN0_RX_M1/UART9_RX_M2/PWM2_CH1_M1/GPIO4_C3_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[15:12]=4'h1

22.6 Application Notes

22.6.1 Software Application Notes

Steps to configure Digital DAC to work in audio DSM mode 0 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program DSMINTMOD_DIV to 0x07.
3. Program DSMCLKCTRL to 0x3d.
4. Program DSMINTSCLK_DIV if Digital DAC I2S RX acts as master.
5. Program DSM_CTRL to 0x58.
6. Program DSM_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set SAI RX related registers.
7. Program DSM_I2S_CLR to clear RX logic.
8. Program DSM_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
9. Program SYS_GRF_SOC_CON2[0] to 1'b1 and program registers of SAI4 that is connected to Digital Audio Codec. Don't start transfer at this time.
10. Program DAC related registers such as DSMHPF, DSMVUCTL and DSMCFG1 to achieve basic configuration.
11. Program ACDCDIG_I2S_XFER to start I2S RX.
12. Program registers of SAI4 outside Digital Audio Codec to start TX.
13. Program DSMDIGEN to enable digital DAC channels. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio DSM mode 0 transfer are as follows.
1. Program registers of SAI4 to stop TX and ACDCDIG_I2S_XFER to stop RX.
2. Program DSM_CTRL to 0x0.
3. Program DSMDIGEN to disable digital DAC channels.
4. Program DSMCLKCTRL to 0x0. Wait DSMCLKCTRL.dac_sync_status until read back to be 1'b0.

Steps to configure Digital DAC to work in audio DSM mode 1 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program DSMCLKCTRL to 0x3d.
3. Program DSMSCLKRXINT_DIV if Digital DAC I2S RX acts as master.
4. Program DSM_CTRL to 0x68.
5. Program DSM_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set SAI RX related registers.
6. Program DSM_I2S_CLR to clear RX logic.
7. Program DSM_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
8. Program SYS_GRF_SOC_CON2[0] to 1'b1 and program registers of SAI4 to start TX.
9. Program DSM_I2S_XFER to start I2S RX. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio DSM mode 1 transfer are as follows.
1. Program registers of SAI4 to stop TX and DSM_I2S_XFER to stop RX.
2. Program DSM_CTRL to 0x0.
3. Program DSMCLKCTRL to 0x0. Wait DSMCLKCTRL.dac_sync_status until read back to be 1'b0.

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Chapter 23 Voice DMA(VDMA)

23.1 Overview

Voice DMA (VDMA) is used to transfer voice data from PDM0 to PMU_SRAM in low power mode. It can also used to transfer voice data from PDM0 to SYSTEM_SRAM or DDR in normal mode.

VDMA supports the following features:

- Support AHB bus interface
- Support read voice data from PDM0
  - Support to configure the voice source address
  - Support to configure increment or fixed for the direction of voice data address
  - Support DMA request and acknowledge
  - Support transfer 1~8 burst per DMA request
  - Support 16/24 bits voice data
- Support write voice data to PMU_SRAM, SYSTEM_SRAM or DDR
  - The start and end address of storing can be configured
  - When current storing address is up to end address, it will loop to start address and overlap previous data, it will also assert a flag
- Support a level combined interrupt
  - Support time out interrupt
  - Support transfer error interrupt
  - Support data transfer interrupt

23.2 Block Diagram

VDMA comprises with:

(3) AHB_MASTER: AHB Master Interface
(4) AHB_SRAM_IF: AHB Slave Interface
(5) VDMA_REG_BANK: Register bank
(6) DMAC_ENGINE: DMA control engine

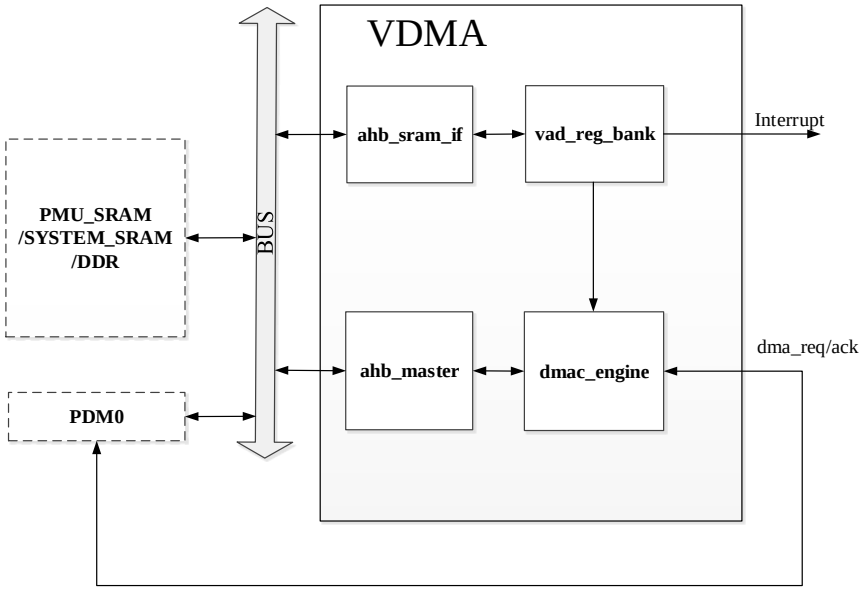

Fig. 23-1 VDMA Block Diagram

23.3 Function Description

Voice DMA (VDMA)is used to read voice data from PDM0, and then write to PMU_SRAM, SYSTEM_SRAM or DDR. The voice data can be 16 or 24 bits:

- When it's 16 bits, it must be half word transfer mode that low 16 bits in a word for left channel and high 16 bits in a word for right channel.
- When it's 24bits, it must be word transfer mode that only 24 bits data is valid in a word,

and it support left or right justified.

23.4 Register Description

23.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VDMA_CONTROL	0x0000	W	0x03000000	Control register
VDMA_VS_ADDR	0x0004	W	0x00000000	Voice source address register
VDMA_TIMEOUT	0x004C	W	0x00000000	Timeout register
VDMA_RAM_START_ADDR	0x0050	W	0x00000000	RAM start address register
VDMA_RAM_END_ADDR	0x0054	W	0x00000000	RAM end address register
VDMA_RAM_CUR_ADDR	0x0058	W	0x00000000	RAM current address register
VDMA_INT	0x0074	W	0x00000000	VDMA interrupt register
VDMA_AUX_CON0	0x0078	W	0x00000000	Auxiliary control register0
VDMA_RAM_START_ADDR_BUS	0x0080	W	0x00000000	RAM start address register for AHB bus interface write mode
VDMA_RAM_END_ADDR_BUS	0x0084	W	0x00000000	RAM end address register for AHB bus interface write mode
VDMA_RAM_CUR_ADDR_BUS	0x0088	W	0x00000000	RAM current address register for AHB bus interface write mode
VDMA_AUX_CON1	0x008C	W	0x00000000	Auxiliary control register1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

23.4.2 Detail Register Description

VDMA_CONTROL

Address: Operational Base(0x273C0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	voice_24bit_sat The mode of voice 24bit data change to 16bit 1'b0: Get the high 16bit data(divided by 256) 1'b1: Saturation from 24bit to 16bit
27	RW	0x0	voice_24bit_align_mode Align mode of channel 24bit width 1'b0: 8~31bits is valid 1'b1: 0~23bits is valid
26	RW	0x0	voice_channel_bitwidth 1'b0: 16bits 1'b1: 24bits
25:23	RW	0x6	voice_channel_num Voice channel number, the value N means N+1 channel.
22	RO	0x0	reserved
21:20	RW	0x0	vdma_mode 2'h0: Reserved 2'h1: Begin to store the data after VDMA is enable 2'h2: Don't store the data 2'h3: Reserved
19:15	RO	0x00	reserved
14	RW	0x0	source_fixaddr_en Direction of source address 1'b0: Increment 1'b1: Fixed
13:10	RW	0x0	incr_length INCR burst length, 0~15 is valid. It is valid when source_burst is set to 3'h1.

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Bit	Attr	Reset Value	Description
9:7	RW	0x0	source_burst_num Source burst number per dma_req, the value N means N+1 burst.
6:4	RW	0x0	source_burst 3'h0: SINGLE 3'h1: INCR 3'h3: INCR4 3'h5: INCR8 3'h7: INCR16 Others: Reserved
3:1	RW	0x0	source_select Voice source select 3'h0: PDM0 Others: Reserved
0	RW	0x0	vdma_en VDMA enable 1'b0: Disable 1'b1: Enable

VDMA_VS_ADDR

Address: Operational Base(0x273C0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vs_addr Voice source address

VDMA_TIMEOUT

Address: Operational Base(0x273C0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31	RW	0x0	work_timeout_en Work timeout enable 1'b0: Disable 1'b1: Enable
30	RW	0x0	idle_timeout_en Idle timeout enable 1'b0: Disable 1'b1: Enable
29:20	RW	0x000	work_timeout_thd work timeout threshold, the unit is one cycle of hclk.
19:0	RW	0x00000	idle_timeout_thd Idle timeout threshold, the unit is one cycle of hclk.

VDMA_RAM_START_ADDR

Address: Operational Base(0x273C0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_start_addr RAM start address to store voice data, the address must be double word alignment.

VDMA_RAM_END_ADDR

Address: Operational Base(0x273C0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_end_addr RAM end address to store voice data, the address must be double word alignment.

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VDMA_RAM_CUR_ADDR

Address: Operational Base(0x273C0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_cur_addr RAM current address to store voice data, The last valid double word data is at address ram_cur_addr-0x8. When the ram_loop_flag is valid, the valid voice data will be ram_cur_addr ~ ram_end_addr ~ loop to ram_begin_addr ~ ram_cur_addr-0x8. When the ramp_loop_flag is not valid, the valid voice data will be ram_begin_addr ~ ram_cur_addr-0x8.

VDMA_INT

Address: Operational Base(0x273C0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	ramp_loop_flag_bus RAM adress loop flag for AHB bus interface write mode. Only valid when bus_write_addr_mode=1'b1. 1'b0: not loop 1'b1: loop
11	W1C	0x0	vdma_data_trans_int VDMA data transfer interrupt 1'b0: interrupt not generated 1'b1: interrupt generated
10	RW	0x0	vdma_data_trans_int_en VDMA data transfer interrupt enable 1'b0: Disable 1'b1: Enable
9	RW	0x0	vdma_idle VDMA idle flag 1'b0: Not idle 1'b1: Idle
8	RO	0x0	ramp_loop_flag RAM adress loop flag 1'b0: not loop 1'b1: loop
7	W1C	0x0	work_timeout_int Work timeout interrupt 1'b0: interrupt not generated 1'b1: interrupt generated
6	W1C	0x0	idle_timeout_int Idle timeout interrupt 1'b0: interrupt not generated 1'b1: interrupt generated
5	RW	0x0	error_int Error interrupt 1'b0: interrupt not generated 1'b1: interrupt generated
4	RO	0x0	reserved
3	RW	0x0	work_timeout_int_en Wrok timeout interrupt enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	idle_timeout_int_en Idle timeout interrupt enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	error_int_en Error interrupt enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

VDMA_AUX_CON0

Address: Operational Base(0x273C0000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	ram_write_rework_addr_mode The rework address for RAM interface write mode. 1'b0: Store the data from the current address 1'b1: Store the data from the start address
13	RW	0x0	bus_write_rework_addr_mode The rework address for AHB bus interface write mode. 1'b0: Store the data from the current address 1'b1: Store the data from the start address
12	RW	0x0	bus_write_addr_mode The address selection when use AHB bus interface write mode. 1'b0: Use RAM_START_ADDR, RAM_END_ADDR, RAM_CUR_ADDR(same with RAM interface write mode). The internal address will continuous when dynamic change between AHB bus interface write mode and RAM interface write mode. 1'b1: Use RAM_START_ADDR_BUS, RAM_END_ADDR_BUS and RAM_CUR_ADDR_BUS.
11:4	RW	0x00	data_trans_kbyte_thd Data transfer number threshold, the unit is K-Byte. The value N means N+1 K-Byte. The interrupt is generated per data_trans_kbyte_thd+1 K-Bytes.
3	RO	0x0	reserved
2	RW	0x0	data_trans_trig_int_en Trigger an interrupt for data transfer, It's valid only when bus_write_en=1'b1. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dis_ram_itf Disable write voice data to Internal SRAM through RAM interface. 1'b0: Enable ram interface 1'b1: Disable ram interface
0	RW	0x0	bus_write_en Enable write voice data to Internal SRAM through AHB bus interface. 1'b0: Disable 1'b1: Enable

VDMA_RAM_START_ADDR_BUS

Address: Operational Base(0x273C0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_start_addr_bus RAM start address to store voice data, the address must be double word alignment. Only used for AHB bus interface write mode and when bus_write_addr_mode=1'b1.

VDMA_RAM_END_ADDR_BUS

Address: Operational Base(0x273C0000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_begin_addr_bus RAM start address to store voice data, the address must be double word alignment. Only used for AHB bus interface write mode and when bus_write_addr_mode=1'b1.

VDMA_RAM_CUR_ADDR_BUS

Address: Operational Base(0x273C0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_cur_addr_bus RAM current address to store voice data. Only used for AHB bus interface write mode and when bus_write_addr_mode=1'b1. The last valid double word data is at address ram_cur_addr_bus-0x8. When the ram_loop_flag_bus is valid, the valid voice data will be ram_cur_addr_bus ~ ram_end_addr_bus ~ loop to ram_begin_addr_bus ~ ram_cur_addr_bus-0x8. When the ramp_loop_flag is not valid, the valid voice data will be ram_begin_addr_bus ~ ram_cur_addr_bus-0x8.

VDMA_AUX_CON1

Address: Operational Base(0x273C0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	data_trans_int_mode_sel Data transfer number threshold selection for interrupt trigger 1'b0: data_trans_kbyte_thd 1'b1: data_trans_word_thd
15:0	RW	0x0000	data_trans_word_thd Data transfer number threshold, the unit is word. The value N means N+1 words. The interrupt is generated per trans_word_thd+1 words.

23.5 Application Notes

23.5.1 VDMA configuration usage flow

- Set VDMA_VS_ADDR.vs_addr=PDM0 base address + INCR_RXDR.
- Set VDMA_RAM_START_ADDR_BUS.ram_start_addr_bus and VDMA_RAM_END_ADDR_BUS.ram_end_addr_bus
- Set to bus write mode when enable VDMA
  Set VDMA_AUX_CON0.bus_write_en=1, and VDMA_AUX_CON0.dis_ram_itf =1 to enable VDMA as bus write mode.
- Set VDMA_CONTROL register:
  Set source_select=0x0, select PDM0
  Set source_burst=0x3, select INCR4 burst type
  Set source_burst_num=0x0, select 1 burst transfer per DMA request
  Set vdma_mode=0x1, select Mode 1
  Set voice_channel_num=0x7, all voice channel number is 8
  Set voice_channel_bitwidth=0x0, voice data width is 16 bits
  Set vdma_en=0x1, enable VDMA

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23.5.2 Data Transfer Interrupt usage flow

When VDMA is working at bus write mode. User can get data transfer interrupt by following additional configuration.

- Set VDMA_AUX_CONTROL.data_trans_trig_int_en=0x1
- Set VDMA_AUX_CONTROL.data_trans_kbyte_thd at appropriate value
- Set VDMA_INT.VDMA_data_trans_int_en=0x1

23.5.3 Timeout configuration usage flow

- Set VDMA_TIMEOUT.idle_timeout_thd=0xfffff, set VDMA_TIMEOUT.idle_timeout_en=0x1, set VDMA_INT.idle_timeout_int=0x1. After above setting, a counter is increase at AHB clock when dmac_engine is idle, the counter will be clear to 0 once dmac_engine start to read voice data. An interrupt will be asserted when the counter up to idle_timeout_thd. This idle timeout is used for PDM0 work fail (Don't assert DMA request for a long time).
- Set VDMA_TIMEOUT.work_timeout_thd=0x3ff, set VDMA_TIMEOUT.work_timeout_en=0x1, set VDMA_INT.work_timeout_int=0x1. After above setting, a counter is increase at AHB clock when dmac_engine is busy, the counter will be clear to 0 once dmac_engine is idle. An interrupt will be asserted when the counter up to work_timeout_thd. This work timeout is used for bus transmission congestion (a burst transferring is not completed for a long time).

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Chapter 24 Serial Audio Interface (SAI)

24.1 Overview

The SAI controller is designed for interfacing between the AHB bus and the serial audio interface bus.The SAI is a serial link for digital audio data transfer between devices in the system .The SAI interface (Serial Audio Interface) offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be
targeted. I2S standards, PCM, and TDM may be addressed.
SAI is widely used in the devices such as ADC, DAC, DSP, CPU, etc. With the SAI interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.

24.1.1 Features

- Support eight internal 32-bit wide and 32-location deep FIFOs, four for transmitting and the other for receiving audio data
- Support AHB bus interface
- Support 8 ~ 32 bits audio data transfer
- Support master and slave mode
- Support DMA handshaking interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combined interrupt output
- Support 8 to 32 bit audio data left or right justified in 32-bit wide FIFO
- Support two 16-bit audio data store together in one 32-bit wide location and support four 8-bit audio data store together in one 32-bit wide location
- Support TX to RX loopback bypass mode
- Support audio protocol: I2S, PCM, TDM
- Support Number of bits by frame can be configurable
- Support First active slot position in the frame is configurable
- Support up to 128 slots available with configurable size
- Support slot length 8 to 32 bits configurable
- Support slot valid data length 8 to 32 bits configurable
- Support Mono audio mode
- Support slot mask configurable
- Support First active bit position in the slot is configurable
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and FS polarity
- Support up to four lanes parallel transceivers
- Support SDI,SDO IOMUX

24.2 Block Diagram

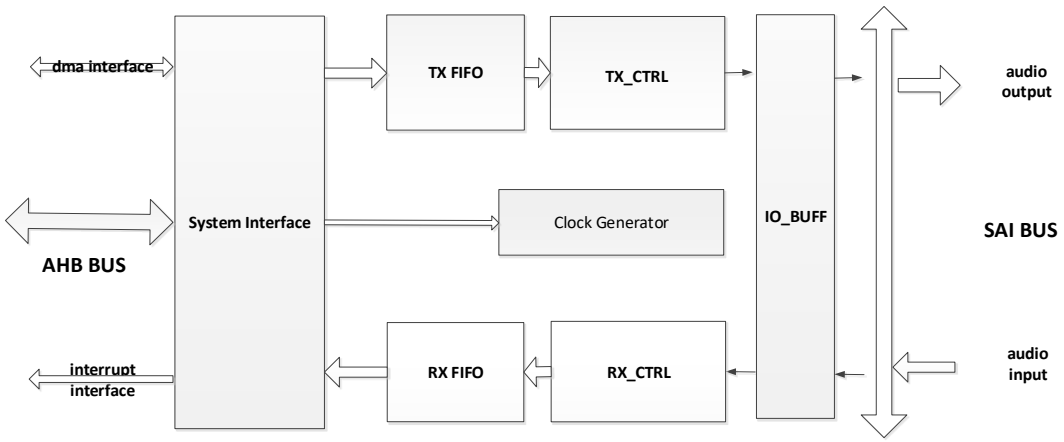

Fig.24-1 SAI Block Diagram

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System Interface
The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.
Clock Generator
The Clock Generator implements clock generation function. The input source clock to the module is MCLK_SAI, and by the divider of the module, the clock generator generates SCLK and FS to transmitter and receiver.
Transmitters
The Transmitters implement transmission operation. The transmitters can act as either a master or a slave, with I2S, PCM or TDM mode surround serial audio interface.
Receiver
The Receiver implements receive operation. The receiver can act as either a master or a slave, with I2S, PCM or TDM mode stereo serial audio interface.
Transmit FIFO
The Transmit FIFO is the buffer to store transmitted audio data. The size of the FIFO is 32bits x 32.
Receive FIFO
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 32.
IO_BUFF
SDO,SDI,LRCK_IN and LRCK_OUT Register output.

24.3 Function Description

In the SAI controller, there are two types: transmitter-master &receiver-master; transmitter-slave & receiver-slave.
In broadcasting application, the SAI controller is used as a transmitter and external or internal audio CODEC is used as a receiver. In recording application, the SAI controller is used as a receiver and external or internal audio CODEC is used as a transmitter. Either the SAI controller or the audio CODEC can act as a master or a slave, but if one is master, the other must be slave.

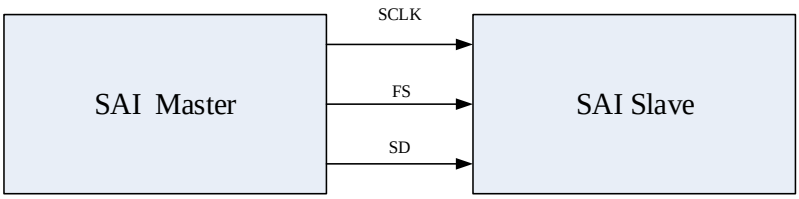

Fig.24-2 SAI transmitter-master & receiver-slave condition

When the transmitter acts as a master, it sends all signals to the receiver (the slave), and CPU controls when to send clock and data to the receiver. When acts as a slave, SD signal still goes from transmitter to receiver, but SCLK and FS signals are from the receiver (the master) to the transmitter. Based on three interface specifications, transmitting data should be ready before transmitter receives SCLK and FS signals. CPU should know when the receiver to initialize a transaction and when the transmitter to send data.
When the receiver acts as a master, it sends SCLK and FS signals to the transmitter (the slave) and receives serial data. So CPU must tell the transmitter when to start a transaction for it to prepare transmitting data then start a transfer and send clock and channel-select signals. When the receiver acts as a slave, CPU should only do initial setting and wait for all signals and then start reading data.
Before transmitting or receiving data, CPU need do initial setting to the SAI register. These includes CPU settings, SAI interface registers settings, and maybe the embedded SoC platform settings. These registers must be set before starting data transfer.
The SAI interface offers a wide set of audio protocols due to its flexibility and wide range of configurations.It can support I2S/PCM/TDM aduio protocol by different configuration.

24.3.1 I2S normal mode

This is the waveform of I2S normal mode. For FS (sai_fs_rx/sai_fs_tx) signal, it goes low to

indicate left channel and high to right channel. For SD (sai_sdo, sai_sdi) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after FS changes. The range of SD signal width is from 8 to 32bits.

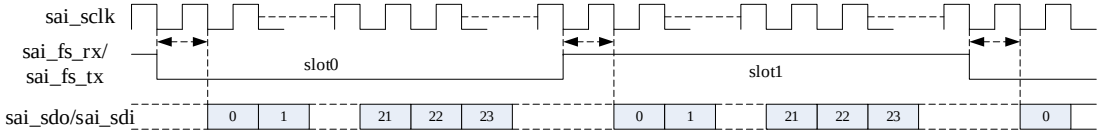

Fig.24-3 I2S Normal Mode Timing Format

24.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sai_sdo, sai_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when FS changes. The range of SD signal width is from 8 to 32bits.

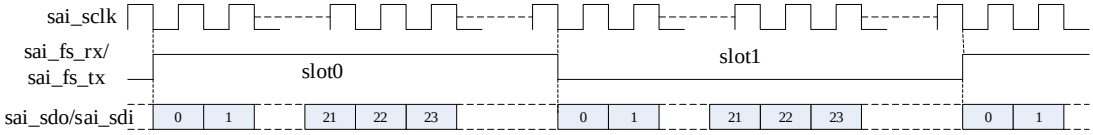

Fig.24-4 I2S Left Justified Mode Timing Format

24.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sai_sdo, sai_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the FS signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 8 to 32bits.

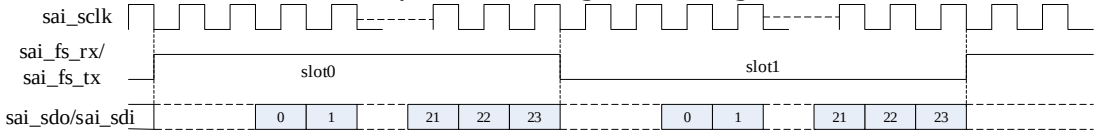

Fig.24-5 I2S Right Justified Mode Timing Format

24.3.4 PCM early mode

This is the waveform of PCM early mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (sai_sdo, sai_sdi) signal, it sends the first bit (MSB or LSB) at the same time when FS goes high. The range of SD signal width is from 8 to 32bits.

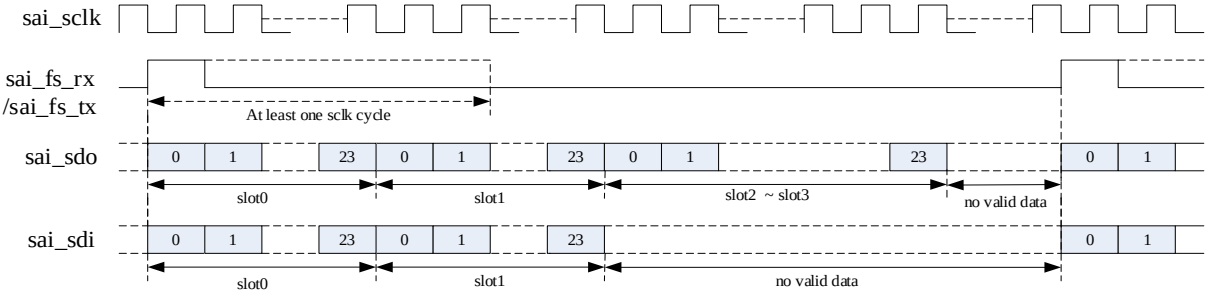

Fig.24-6 PCM Early Mode Timing Format

24.3.5 Flexibility and wide range of configurations

The SAI interface (Serial Audio Interface) offers a wide set of audio protocols due to its flexibility and wide range of configurations.Many stereo or mono audio applications may be targeted. I2S standards, PCM, and TDM may be addressed.

This is the waveform of PCM mode(SBW==VDW,FW >=SBW *SNB). For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate the start of a group of audio data.

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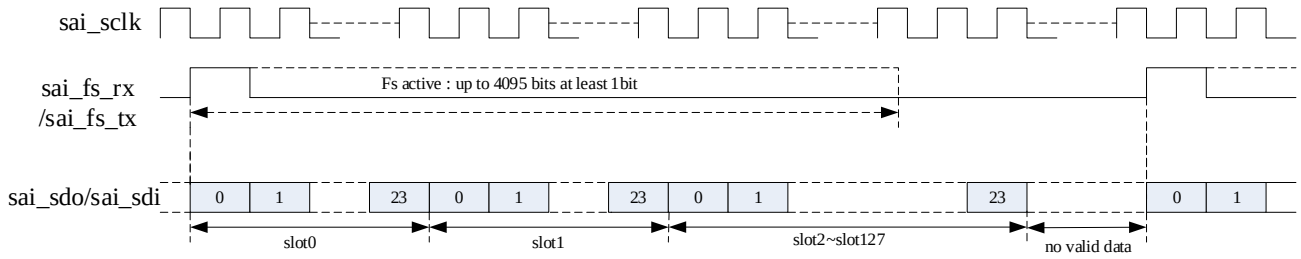

Fig.24-7 SAI PCM mode timing format

This is the waveform of I2S left mode(SBW>=VDW,FW >=SBW *SNB,VDJ==1'b1).

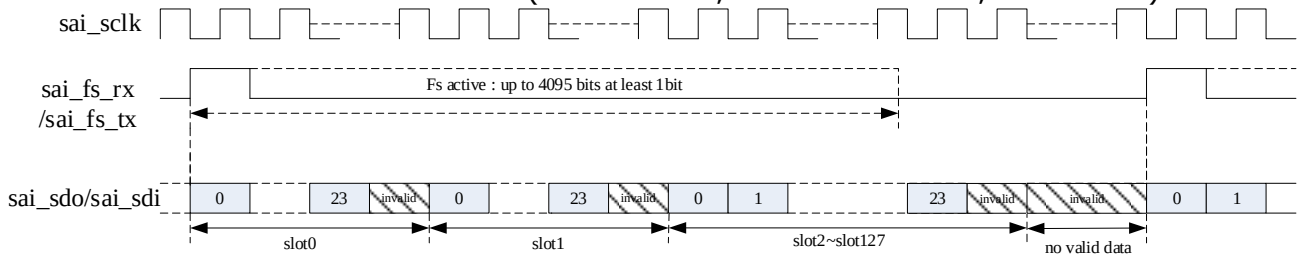

Fig.24-8 SAI I2S left mode timing format

This is the waveform of I2S right mode(SBW>=VDW,FW >=SBW *SNB,VDJ==1'b0).

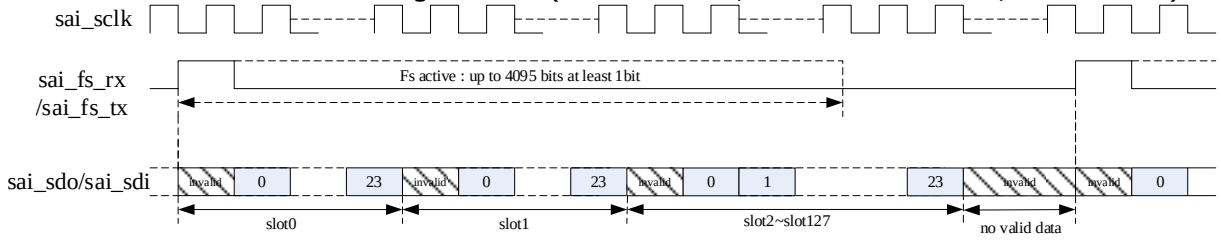

Fig.24-9 SAI I2S right mode timing format

This is the waveform of FS and SD delay time,as the posedge of FS (sai_fs_rx / sai_fs_tx) signal,we can send data at different time ,The time between the FS rise edge and the first valid bit can be configured using the fs_shift register,when fs_shift[0] == 1'b0,data send at posedge of sclk,when fs_shift[0] == 1'b1,data send at negedge of sclk.

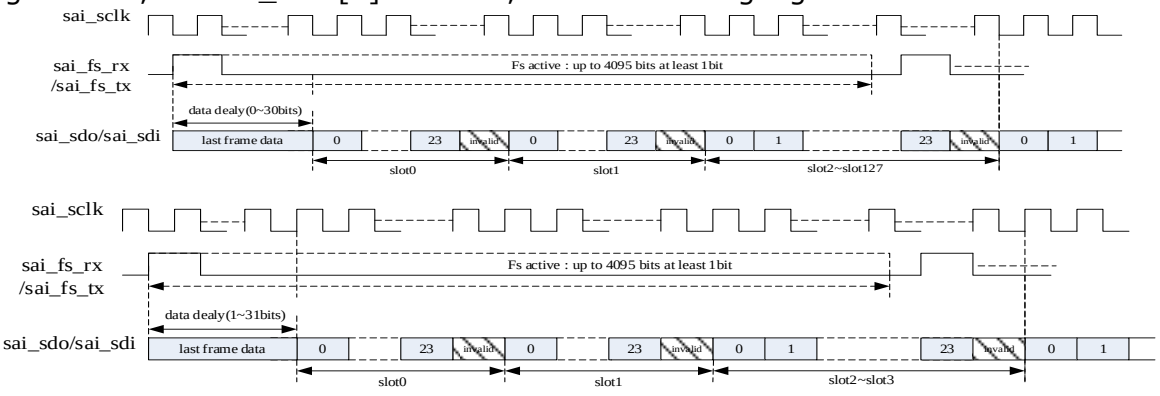

Fig.24-10 fs shift timing format

24.4 Register Description

24.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SAI0	0x2A600000
SAI1	0x2A610000
SAI2	0x2A620000
SAI3	0x2A630000

Name	Base Address
SAI4	0x2A640000
SAI5	0x27D40000
SAI6	0x27D50000
SAI7	0x27ED0000
SAI8	0x27EE0000
SAI9	0x27EF0000

24.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SAI_TXCR	0x0000	W	0x00000FFF	Transmit Operation Control Register
SAI_FSCR	0x0004	W	0x0001F03F	Transmit Frame Sync Operation Control Register
SAI_RXCR	0x0008	W	0x00000FFF	Receive Operation Control Register
SAI_MONO_CR	0x000C	W	0x00000000	Mono mode control
SAI_XFER	0x0010	W	0x00000000	Transfer Start Register
SAI_CLR	0x0014	W	0x00000000	Sclk Domain Logic Clear Register
SAI_CKR	0x0018	W	0x00000000	Clock Generation Register
SAI_TXFIFOLR	0x001C	W	0x00000000	TX FIFO Level Register
SAI_RXFIFOLR	0x0020	W	0x00000000	RX FIFO Level Register
SAI_DMACR	0x0024	W	0x00000000	DMA Control Register
SAI_INTCR	0x0028	W	0x01F00000	Interrupt Control Register
SAI_INTSR	0x002C	W	0x00000000	Interrupt Status Register
SAI_TXDR	0x0030	W	0x00000000	Transmit FIFO Data Register
SAI_RXDR	0x0034	W	0x00000000	Receive FIFO Data Register
SAI_PATH_SEL	0x0038	W	0x0000E4E4	Path select Register
SAI_TX_SLOT_MASK0	0x003C	W	0x00000000	Transmit Slot 0~31 Mask state
SAI_TX_SLOT_MASK1	0x0040	W	0x00000000	Transmit Slot 32~63 Mask state
SAI_TX_SLOT_MASK2	0x0044	W	0x00000000	Transmit Slot 64~95 Mask state
SAI_TX_SLOT_MASK3	0x0048	W	0x00000000	Transmit Slot 96~127 Mask state
SAI_RX_SLOT_MASK0	0x004C	W	0x00000000	Receive Slot 0~31 Mask state
SAI_RX_SLOT_MASK1	0x0050	W	0x00000000	Receive Slot 32~63 Mask state
SAI_RX_SLOT_MASK2	0x0054	W	0x00000000	Receive Slot 64~95 Mask state
SAI_RX_SLOT_MASK3	0x0058	W	0x00000000	Receive Slot 96~127 Mask state
SAI_TX_DATA_CNT	0x005C	W	0x00000000	Tx data counter register
SAI_RX_DATA_CNT	0x0060	W	0x00000000	Rx data counter register
SAI_SAI_TX_SHIFT	0x0064	W	0x00000000	Tx shift register
SAI_SAI_RX_SHIFT	0x0068	W	0x00000000	Rx shift register
SAI_SAI_RD_STATUS	0x006C	W	0x0000000F	
SAI_VERSION	0x0070	W	0x23073576	Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

24.4.3 Detail Registers Description

SAI_TXCR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	tx_delay_en 1'b0: NO DELAY 1'b1: DELAY fsync pos

Bit	Attr	Reset Value	Description
21:20	RW	0x0	tcsr Transmit channel select register 2'b00: One channel parallel 2'b01: Two channel parallel 2'b10: Three channel parallel 2'b11: Four channel parallel
19	RW	0x0	sjm Store justified mode (Can be written only when XFER[0] bit is 0.) 8bit~31bit DATA stored in 32 bits width FIFO. 1'b0: Right justified 1'b1: Left justified
18	RW	0x0	fbm first bit mode (Can be written only when XFER[0] bit is 0.) 1'b0: MSB 1'b1: LSB
17:11	RW	0x01	snb Transfer slot number (Can be written only when XFER[0] bit is 0.) Number of slots in a frame 7'h00: 1slot 7'h01: 2slot 7'h02: 3slot 7'h03: 4slot ..... 7'h7e: 127slot 7'h7f: 128slot
10	RW	0x1	vdj Valid data justified mode (Can be written only when XFER[0] bit is 0.) 1'b0: Right justified 1'b1: Left justified
9:5	RW	0x1f	sbw Transfer slot bits width (Can be written only when XFER[0] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit

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Bit	Attr	Reset Value	Description
4:0	RW	0x1f	vdw Slot valid data width (Can be written only when XFER[0] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit

SAI_FSCR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	edge_sel 1'h0: pos 1'h1: pos and neg
23:12	RW	0x01f	fpw Transfer frame pulse width (Can be written only when XFER[0] is 0.) 12'h000: 1bit 12'h001: 2bit 12'h002: 3bit ..... 12'hffe:4095bit 12'hfff:res
11:0	RW	0x03f	fw Transfer frame width (Can be written only when XFER[0] is 0.) 12'h000~12'h006: Reserved 12'h007: 8bit 12'h008: 9bit ..... 12'hffe: 4095bit 12'hfff: 4096bit

SAI_RXCR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	rx_delay_en 1'b0: NO DELAY 1'b1: DELAY fsync pos
21:20	RW	0x0	rcsr receive channel select register 2'b00: One channel parallel 2'b01: Two channel parallel 2'b10: Three channel parallel 2'b11: Four channel parallel

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Bit	Attr	Reset Value	Description
19	RW	0x0	sjm Store justified mode (Can be written only when XFER[2] bit is 0.) 8bit~31bit DATA stored in 32 bits width FIFO. 1'b0: Right justified 1'b1: Left justified
18	RW	0x0	fbm first bit mode (Can be written only when XFER[2] bit is 0.) 1'b0: MSB 1'b1: LSB
17:11	RW	0x01	snb receive slot number (Can be written only when XFER[2] bit is 0.) number of slots in a frame 7'h00: 1slot 7'h01: 2slot 7'h02: 3slot 7'h03: 4slot ..... 7'h7e: 127slot 7'h7f: 128slot
10	RW	0x1	vdj Valid data justified mode (Can be written only when XFER[2] bit is 0.) 1'b0: Right justified 1'b1: Left justified
9:5	RW	0x1f	sbw receive slot bits width (Can be written only when XFER[2] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit
4:0	RW	0x1f	vdw Valid fata width (Can be written only when XFER[2] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit

SAI_MONO_CR

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Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:2	RW	0x00	rx_mono_slot_sel Receive mono mode valid slot data select 7'h00: First slot data valid 7'h01: Second slot data valid ..... 7'h7f: Slot128 data valid
1	RW	0x0	rx_mono_en Receive mono audio data enable bit 1'b0: Normal mode 1'b1: Mono mode
0	RW	0x0	tx_mono_en Transmit mono audio data enable bit 1'b0: Normal mode 1'b1: Mono mode

SAI_XFER

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	rx_data_cnt_en 1'b0: Stop cnt 1'b1: Start cnt
4	RW	0x0	tx_data_cnt_en 1'b0: Stop cnt 1'b1: Start cnt
3	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
2	RW	0x0	txs 1'b0: Stop TX transfer 1'b1: Start TX transfer
1	RW	0x0	fss 1'b0: Stop frame sync 1'b1: Start frame sync
0	RW	0x0	clk_gate_en 1'b0: Stop clk 1'b1: Start clk

SAI_CLR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	fsc This is a self-cleared bit. write 1 to clear all receive logic.
1	W1C	0x0	rxc RX logic clear This is a self-cleared bit. write 1 to clear all receive logic.
0	W1C	0x0	txc TX logic clear This is a self-cleared bit. write 1 to clear all transmit logic.

SAI_CKR

Address: **Operational Base** + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:3	RW	0x000	mdiv (Can be written only when XFER[0] bit is 0.) mclk divider = (mclk/sclk)-1. For example, if mclk divider is 5, then the frequency of sclk is mclk/6.
2	RW	0x0	mss Transmit master/slave mode select (Can be written only when XFER[0] bit is 0.) 1'b0: Master mode(sclk output) 1'b1: Slave mode(sclk input)
1	RW	0x0	ckp Transmit sclk polarity (Can be written only when XFER[2] or XFER[0] bit is 0.) 1'b0: Sample data at posedge sclk and drive data at negedge sclk 1'b1: Sample data at negedge sclk and drive data at posedge sclk
0	RW	0x0	fsp Transmit fs polarity (Can be written only when XFER[2] or XFER[0] bit is 0.) 1'b0: Frame sync low active 1'b1: Frame sync high active

SAI_TXFIFOLR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	tfl3 Transmit fifo3 level Contains the number of valid data entries in the transmit fifo3.
17:12	RO	0x00	tfl2 Transmit fifo2 level Contains the number of valid data entries in the transmit fifo2.
11:6	RO	0x00	tfl1 Transmit fifo1 level Contains the number of valid data entries in the transmit fifo1.
5:0	RO	0x00	tfl0 Transmit fifo0 level Contains the number of valid data entries in the transmit fifo0.

SAI_RXFIFOLR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	rfl3 Receive fifo3 level Contains the number of valid data entries in the receive fifo3.
17:12	RO	0x00	rfl2 Receive fifo2 level Contains the number of valid data entries in the receive fifo2.
11:6	RO	0x00	rfl1 Receive fifo1 level Contains the number of valid data entries in the receive fifo1.
5:0	RO	0x00	rfl0 Receive fifo0 level Contains the number of valid data entries in the receive fifo0.

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SAI_DMACR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	rde Receive DMA enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
23:21	RO	0x0	reserved
20:16	RW	0x00	rdl Receive data level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
15:9	RO	0x00	reserved
8	RW	0x0	tde Transmit DMA enable 1'b0: Transmit DMA disabled 1'b1: Transmit DMA enabled
7:5	RO	0x0	reserved
4:0	RW	0x00	tdl Transmit data level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the TX FIFO(TX FIFO0 if CSR=00;TX FIFO1 if CSR=01,TX FIFO2 if CSR=10,TX FIFO3 if CSR=11)is equal to or below this field value.

SAI_INTCR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RW	0x1f	rft Receive fifo threshold When the number of receive fifo entries is more than or equal to this threshold plus 1, the receive fifo full interrupt is triggered.
19	RO	0x0	reserved
18	WO	0x0	rxoic RX overrun interrupt clear Write 1 to clear RX overrun interrupt.
17	RW	0x0	rxoie RX overrun interrupt enable 1'b0: Disable 1'b1: Enable
16	RW	0x0	rxfie RX full interrupt enable 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8:4	RW	0x00	tft Transmit fifo threshold When the number of transmit fifo entries is less than or equal to this threshold, the transmit fifo empty interrupt is triggered.

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Bit	Attr	Reset Value	Description
3	RO	0x0	reserved
2	W1C	0x0	txuic TX underrun interrupt clear Write 1 to clear TX underrun interrupt.
1	RW	0x0	txuie TX underrun interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	txeie TX empty interrupt enable 1'b0: Disable 1'b1: Enable

SAI_INTSR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	rxoi RX overrun interrupt 1'b0: Inactive 1'b1: Active
16	RO	0x0	rxfi RX full interrupt 1'b0: Inactive 1'b1: Active
15:2	RO	0x0000	reserved
1	RO	0x0	txui TX underrun interrupt 1'b0: Inactive 1'b1: Active
0	RO	0x0	txei TX empty interrupt 1'b0: Inactive 1'b1: Active

SAI_TXDR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdr Transmit fifo fata register When it is written, data are moved into the transmit fifo.

SAI_RXDR

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxdr Receive fifo data register When the register is read, data in the receive fifo is accessed.

SAI_PATH_SEL

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:22	RW	0x00	sdo_to_sdi_path_sel SDO_TO_SDI_PATH_SEL [23:22]:sdi0 sel sdo0 or sdo1 or sdo2 or sdo3 [25:24]:sdi1 sel sdo0 or sdo1 or sdo2 or sdo3 [27:26]:sdi2 sel sdo0 or sdo1 or sdo2 or sdo3 [29:28]:sdi3 sel sdo0 or sdo1 or sdo2 or sdo3
21:18	RW	0x0	loopback_bypass Loopback by pass enable bit Tx_sdo -> Rx_sdi loopback mode should work at fs_tx_as_common mode and tx=rx=master [18]:Loopback_en0 [19]:Loopback_en1 [20]:Loopback_en2 [21]:Loopback_en3 1'b0: No active 1'b1: Active
17	RW	0x0	sync_out_sel Tx sync out select bit 1'b0: Tx sclk and fs sync out use out signal 1'b1: Tx sclk and fs sync out use in signal
16	RW	0x0	sync_in_sel Tx sync in select bit 1'b0: Tx sclk and fs use pad signal 1'b1: Tx sclk and fs use sync input port
15:14	RW	0x3	rx_path_select3 Rx path select 2'b00: Path3 data from sdi0 2'b01: Path3 data from sdi1 2'b10: Path3 data from sdi2 2'b11: Path3 data from sdi3
13:12	RW	0x2	rx_path_select2 Rx path select 2'b00: Path2 data from sdi0 2'b01: Path2 data from sdi1 2'b10: Path2 data from sdi2 2'b11: Path2 data from sdi3
11:10	RW	0x1	rx_path_select1 Rx path select 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3
9:8	RW	0x0	rx_path_select0 Rx path select 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3
7:6	RW	0x3	tx_path_select3 TX path select 2'b00: Sdo3 output data from path0 2'b01: Sdo3 output data from path1 2'b10: Sdo3 output data from path2 2'b11: Sdo3 output data from path3

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Bit	Attr	Reset Value	Description
5:4	RW	0x2	tx_path_select2 TX path select 2'b00: Sdo2 output data from path0 2'b01: Sdo2 output data from path1 2'b10: Sdo2 output data from path2 2'b11: Sdo2 output data from path3
3:2	RW	0x1	tx_path_select1 TX path select 2'b00: Sdo1 output data from path0 2'b01: Sdo1 output data from path1 2'b10: Sdo1 output data from path2 2'b11: Sdo1 output data from path3
1:0	RW	0x0	tx_path_select0 TX path select 2'b00: Sdo0 output data from path0 2'b01: Sdo0 output data from path1 2'b10: Sdo0 output data from path2 2'b11: Sdo0 output data from path3

SAI_TX_SLOT_MASK0

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask0 Transmit slot 0~31 mask state slot 0~31 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK1

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask1 Transmit slot 32~63 mask state slot 32~63 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK2

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask2 Transmit slot 64~95 mask state slot 64~95 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK3

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask3 Transmit slot 96~127 mask state slot 96~127 mask state 0: Slot active 1: Slot mask,data is invalid

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SAI_RX_SLOT_MASK0

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask0 Receive slot 0~31 mask state Slot 0~31 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK1

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask1 Receive slot 32~63 mask state slot 32~63 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK2

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask2 Receive slot 64~95 mask state slot 64~95 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK3

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask3 Receive Slot 96~127 mask state slot 96~127 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_DATA_CNT

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	tx_data_cnt Tx data counter

SAI_RX_DATA_CNT

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data_cnt Rx data counter

SAI_SAI_TX_SHIFT

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:0	RW	0x000000	fs_shift Transfer frame sync pulse shift control 24'h00: Normal mode 24'h01: Fs 1/2 cycle shift left. 24'h02: Fs 1 cycle shift left. 24'h03: Fs 3/2 cycle shift left. .....

SAI_SAI_RX_SHIFT

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	fs_shift Transfer frame sync pulse shift control 24'h00: Normal mode 24'h01: Fs 1/2 cycle shift left. 24'h02: Fs 1 cycle shift left. 24'h03: Fs 3/2 cycle shift left. .....

SAI_SAI_RD_STATUS

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x1	rx_idle
2	RW	0x1	tx_idle
1	RW	0x1	fs_idle
0	RW	0x1	clk_idle

SAI_VERSION

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x23073576	sai_vertion SAI version

24.5 Interface Description

The following table shows the SAI0 interface description.

Table 24-1 SAI0 m0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai0_mclk	I/O	VI_CIF_D8/SDMMC1_DETN_M1/ETH0_RXCLK_M1/SAI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/SATA1_ACTLED_M0/GPIO2_B5_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[7:4]=4
sai0_sclk	I/O	VI_CIF_D7/ETH1_PTP_REFCLK_M1/ETH0_RXD3_M1/SAI0_SCLK_M0/UART7_TX_M0/UART8_RTSN_M1/I2C8_SCL_M2/GPIO2_B6_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[11:8]=4

Module Pin	Direction	Pad Name	IOMUX Setting
sai0_lrck	I/O	VI_CIF_D6/ETH0_RXD2_M1/SAI0_LRCK_M0/UART7_RX_M0/UART8_CTSN_M1/I2C8_SDA_M2/GPIO2_B7_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[15:12]=4
sai0_sdo0	O	VI_CIF_D15/SDMMC1_D0_M1/ETH0_RXD0_M1/SAI0_SDO0_M0/UART8_TX_M1/SPI4_CSN1_M3/I2C4_SCL_M2/GPIO2_A6_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[11:8]=4
sai0_sdo1	O	VI_CIF_D14/SDMMC1_D1_M1/ETH0_TXCTL_M1/SAI0_SDO1_M0/UART8_RX_M1/I2C4_SDA_M2/GPIO2_A7_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[15:12]=4
sai0_sdo2	O	VI_CIF_D10/SDMMC1_CLK_M1/ETH0_TXCLK_M1/SAI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/PCIE1_CLKREQN_M0/GPIO2_B3_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4
sai0_sdo3	O	CAM_CLK2_OUT_M1/ETH1_MCLK_M0/ETH_CLK0_25M_OUT_M1/SAI0_SDO3_M0/SPDIF_TX0_M2/UART9_CTSN_M0/SPI3_CSN1_M0/PWM2_CH7_M2/GPIO2_D7_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[15:12]=4
sai0_sdi0	I	VI_CIF_D13/SDMMC1_D2_M1/ETH0_TXD1_M1/SAI0_SDI0_M0/PDM0_SDI3_M3/UART1_TX_M1/GPIO2_B0_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[3:0]=4
sai0_sdi1	I	VI_CIF_D12/SDMMC1_D3_M1/ETH0_TXD0_M1/SAI0_SDI1_M0/PDM0_SDI2_M3/UART1_RX_M1/GPIO2_B1_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[7:4]=4
sai0_sdi2	I	VI_CIF_D11/SDMMC1_CMD_M1/ETH0_TXD3_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCIE0_CLKREQN_M0/GPIO2_B2_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[11:8]=4
sai0_sdi3	I	VI_CIF_D9/SDMMC1_PWREN_M1/ETH0_TXD2_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/SATA0_ACTLED_M0/GPIO2_B4_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[3:0]=4

Table 24-2 SAI0 m1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai0_mclk	I/O	SAI0_MCLK_M1/PDM0_CLK0_M0/UART10_TX_M2/PWM0_CH0_M0/GPIO0_C4_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[3:0]=1
sai0_sclk	I/O	SAI0_SCLK_M1/I2C3_SCL_M1/SPI0_CSN0_M0/GPIO0_C6_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[11:8]=1
sai0_lrck	I/O	SAI0_LRCK_M1/I2C3_SDA_M1/SPI0_CLK_M0/GPIO0_C7_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[15:12]=1
sai0_sdo0	O	SAI0_SDO0_M1/DP_HPDIN_M1/UART10_RX_M2/I3C0_SDA_PU_M0/GPIO0_C5_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[7:4]=1
sai0_sdo1/sai0_sdi3	I/O	SAI0_SDI3_M1/SAI0_SDO1_M1/PDM0_SDI3_M0/I2C4_SDA_M0/GPU_AVS/PWM2_CH0_M0/UART1_RTSN_M0/GPIO0_D3_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[15:12]=2 PMU1_IOC_GPIO0D_IOMUX_SEL_L[15:12]=1
sai0_sdo2/sai0_sdi2	I/O	SAI0_SDI2_M1/SAI0_SDO2_M1/PDM0_SDI2_M0/I2C4_SCL_M0/CPUBIG_AVS/PW	PMU1_IOC_GPIO0D_IOMUX_SEL_L[11:8]=2 PMU1_IOC_GPIO0D_IOMU

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Module Pin	Direction	Pad Name	IOMUX Setting
		M1_CH5_M0/UART1_CTSN_M0/GPIO0_D2_d	X_SEL_L[11:8]=1
sai0_sdo3/sai0_sdi1	I/O	SAI0_SDI1_M1/SAI0_SDO3_M1/PDM0_SDI1_M0/SPI0_MISO_M0/GPIO0_D1_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[7:4]=2 PMU1_IOC_GPIO0D_IOMUX_SEL_L[7:4]=1
sai0_sdi0	I	SAI0_SDI0_M1/PDM0_SDI0_M0/SPI0_MOSI_M0/GPIO0_D0_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[3:0]=1

Table 24-3 SAI0 m2 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai0_mclk	I/O	EMMC_D4/SAI0_MCLK_M2/SAI3_MCLK_M0/SPI0_CSN0_M2/GPIO1_A4_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[3:0]=3
sai0_sclk	I/O	EMMC_D0/FSPI0_D0/SAI0_SCLK_M2/UART7_RTSN_M1/I2C2_SCL_M1/GPIO1_A0_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[3:0]=3
sai0_lrck	I/O	EMMC_D1/FSPI0_D1/SAI0_LRCK_M2/UART7_CTSN_M1/I2C2_SDA_M1/GPIO1_A1_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[7:4]=3
sai0_sdo0	O	EMMC_D7/SAI0_SDO0_M2/SAI3_SDI_M0/SPI0_CLK_M2/GPIO1_A7_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[15:12]=3
sai0_sdo1/sai0_sdi3	I/O	EMMC_D2/FSPI0_D2/SAI0_SDO1_M2/SAI0_SDI3_M2/PDM0_SDI3_M1/UART7_TX_M1/UART6_RTSN_M2/GPIO1_A2_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[11:8]=3 TOP_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4
sai0_sdo2/sai0_sdi2	I/O	EMMC_D3/FSPI0_D3/SAI0_SDO2_M2/SAI0_SDI2_M2/PDM0_SDI1_M1/UART7_RX_M1/UART6_CTSN_M2/GPIO1_A3_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[15:12]=3 TOP_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4
sai0_sdo3/sai0_sdi1	I/O	EMMC_CLK/FSPI0_CLK/SAI0_SDO3_M2/SAI0_SDI1_M2/PDM0_CLK0_M1/PWM2_CH7_M1/GPIO1_B1_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[7:4]=3 TOP_IOC_GPIO1B_IOMUX_SEL_L[7:4]=4
sai0_sdi0	I	EMMC_STRB/SAI0_SDI0_M2/SAI3_SDO_M0/PDM0_SDI0_M1/SPI0_CSN1_M2/GPIO1_B2_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[11:8]=3

Table 24-4 SAI1 m0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai1_mclk	I/O	SAI1_MCLK_M0/SAI4_MCLK_M0/AUPLL_CLK_IN_M2/PWM2_CH5_M0/GPIO4_A2_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[11:8]=1
sai1_sclk	I/O	SAI1_SCLK_M0/FLEXBUS1_CSN_M4/SPI3_CSN0_M2/UART5_RTSN_M1/I2C2_SCL_M2/PWM2_CH4_M1/GPIO4_A3_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[15:12]=1
sai1_lrck	I/O	SAI1_LRCK_M0/FLEXBUS1_D12_M1/SPI4_CSN1_M2/UART5_CTSN_M1/I2C2_SDA_M2/PCIE1_CLKREQN_M2/GPIO4_A5_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[7:4]=1
sai1_sdo0	O	SAI1_SDO0_M0/SAI4_SDI_M0/SPI3_CLK_M2/PWM2_CH6_M0/GPIO4_A7_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[15:12]=1
sai1_sdo1/sai1_sdi3	I/O	SAI1_SDO1_M0/SAI1_SDI3_M0/PDM1_CLK1_M1/FLEXBUS1_D13_M1/SPI4_CLK_	TOP_IOC_GPIO4B_IOMUX_SEL_L[3:0]=1 TOP_IOC_GPIO4B_IOMUX_SEL_L[3:0]=2

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Module Pin	Direction	Pad Name	IOMUX Setting
		M2/UART5_TX_M1/UART6_RTSN_M0/UART2_RTSN_M1/GPIO4_B0_d	
sai1_sdo2/sai1_sdi2	I/O	SAI1_SDO2_M0/SAI1_SDI2_M0/PDM1_SDI2_M1/FLEXBUS1_D14_M1/SPI4_MOSI_M2/UART5_RX_M1/UART6_CTSN_M0/UART2_CTSN_M1/GPIO4_B1_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[7:4]=1 TOP_IOC_GPIO4B_IOMUX_SEL_L[7:4]=2
sai1_sdo3/sai1_sdi1	I/O	SAI1_SDO3_M0/SAI1_SDI1_M0/PDM1_SDI1_M1/FLEXBUS1_D15_M1/SPI4_MISO_M2/MIPI_TE_M0/GPIO4_B2_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[11:8]=1 TOP_IOC_GPIO4B_IOMUX_SEL_L[11:8]=2
sai1_sdi0	I	SAI1_SDI0_M0/SAI4_SDO_M0/PDM1_SDI0_M1/SPI4_CSN0_M2/SPI3_CSN1_M2/PWM2_CH7_M0/GPIO4_B3_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[15:12]=1

Table 24-5 SAI1 m1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai1_mclk	I/O	VO_LCDC_D3/VO_EBC_SDDO3/SAI1_MCLK_M1/DSMC_DATA1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4
sai1_sclk	I/O	VO_LCDC_D4/VO_EBC_SDDO4/SAI1_SCLK_M1/DSMC_DATA2/FLEXBUS1_D4/UART8_RTSN_M0/SPI1_CLK_M2/GPIO3_C7_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[15:12]=4
sai1_lrck	I/O	VO_LCDC_D5/VO_EBC_SDDO5/SAI1_LRCK_M1/DSMC_DATA3/FLEXBUS1_D5/UART8_TX_M0/SPI1_MOSI_M2/GPIO3_C6_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[11:8]=4
sai1_sdo0	O	VO_LCDC_D6/VO_EBC_SDDO6/SAI1_SDO0_M1/DSMC_DATA4/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4
sai1_sdo1	O	VO_LCDC_D7/VO_EBC_SDDO7/SAI1_SDO1_M1/DSMC_DATA5/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/CAN0_TX_M3/GPIO3_C4_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4
sai1_sdo2	O	VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4]=4
sai1_sdo3	O	VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/DSMC_DATA7/FLEXBUS1_D9/UART2_TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0]=4
sai1_sdi0	I	VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/U	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12]=4

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Module Pin	Direction	Pad Name	IOMUX Setting
		ART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	
sai1_sdi1	I	VO_LCDC_DEN/VO_EBC_SDLE/SAI1_SDI1_M1/DSMC_DATA0/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[3:0]=4
sai1_sdi2	I	VO_LCDC_HSYNC/VO_EBC_GDCLK/SAI1_SDI2_M1/DSMC_CLKP/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[7:4]=4
sai1_sdi3	I	VO_LCDC_VSYNC/VO_EBC_SDCLK/SAI1_SDI3_M1/DSMC_CLKN/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:8]=4

Table 24-6 SAI2 m0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai2_mclk	I/O	ETH1_MCLK_M1/SAI2_MCLK_M0/PDM0_SDI3_M2/SPDIF_RX1_M2/UART10_RTSN_M1/I2C5_SCL_M1/GPIO1_D4_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[3:0]=4
sai2_sclk	I/O	ETH1_RXCTL_M1/SAI2_SCLK_M0/UART10_RX_M1/I3C0_SDA_PU_M1/GPIO1_D1_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[7:4]=4
sai2_lrck	I/O	ETH1_MDC_M1/SAI2_LRCK_M0/I3C0_SCL_M1/PWM1_CH3_M1/GPIO1_D2_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[11:8]=4
sai2_sdo0	O	ETH1_RXD1_M1/SAI2_SDO_M0/UART10_TX_M1/GPIO1_D0_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[3:0]=4
sai2_sdi0	I	ETH1_MDIO_M1/SAI2_SDI_M0/I3C0_SDA_M1/PWM1_CH4_M1/GPIO1_D3_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[15:12]=4

Table 24-7 SAI2 m1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai2_mclk	I/O	VI_CIF_D4/ETH1_RXD3_M0/ETH0_PPSCLK_M1/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[7:4]=4
sai2_sclk	I/O	VI_CIF_D3/ETH1_RXCLK_M0/ETH0_PPSTRIG_M1/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[11:8]=4
sai2_lrck	I/O	VI_CIF_D2/ETH1_TXD2_M0/SAI2_LRCK_M1/PDM1_SDI3_M0/UART11_RTSN_M1/SPI1_MISO_M1/PWM0_CH0_M2/GPIO2_C3_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[15:12]=4
sai2_sdo0	O	VI_CIF_D1/ETH1_TXD3_M0/SAI2_SDO_M1/PDM1_SDI0_M0/UART11_TX_M1/SPI1_CSN0_M1/PWM1_CH3_M2/GPIO2_C4_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[4:0]=4

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Module Pin	Direction	Pad Name	IOMUX Setting
sai2_sdi0	I	VI_CIF_D0/ETH1_TXCLK_M0/SAI2_SDI_M1/PDM1_CLK0_M0/UART11_RX_M1/SPI1_CLK_M1/PWM1_CH4_M2/GPIO2_C5_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[7:4]=4

Table 24-8 SAI2 m2 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai2_mclk	I/O	VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[7:4]=4
sai2_sclk	I/O	VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8]=4
sai2_lrck	I/O	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12]=4
sai2_sdo0	O	VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[15:12]=4
sai2_sdi0	I	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8]=4

Table 24-9 SAI3 m0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai3_mclk	I/O	EMMC_D4/SAI0_MCLK_M2/SAI3_MCLK_M0/SPI0_CSN0_M2/GPIO1_A4_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[3:0]=4
sai3_sclk	I/O	EMMC_D5/SAI3_SCLK_M0/PDM0_SDI2_M1/SPI0_MOSI_M2/I2C9_SCL_M0/GPIO1_A5_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[7:4]=4
sai3_lrck	I/O	EMMC_D6/SAI3_LRCK_M0/PDM0_CLK1_M1/SPI0_MISO_M2/I2C9_SDA_M0/GPIO1_A6_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[11:8]=4
sai3_sdo0	O	EMMC_STRB/SAI0_SDI0_M2/SAI3_SDO_M0/PDM0_SDI0_M1/SPI0_CSN1_M2/GPIO1_B2_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[11:8]=4
sai3_sdi0	I	EMMC_D7/SAI0_SDO0_M2/SAI3_SDI_M0/SPI0_CLK_M2/GPIO1_A7_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[15:12]=4

Table 24-10 SAI3 m1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai3_mclk	I/O	ETH1_TXCLK_M1/SDMMC1_CLK_M0/SAI3	TOP_IOC_GPIO1C_IOMUX_

Module Pin	Direction	Pad Name	IOMUX Setting
		_MCLK_M1/PDM0_CLK0_M2/UART3_RX_M2/GPIO1_C1_d	SEL_L[3:0]=4
sai3_sclk	I/O	ETH1_RXD2_M1/SDMMC1_D0_M0/SAI3_SCLK_M1/I2C9_SDA_M1/SPI1_CLK_M0/PCIE1_CLKREQN_M1/PWM1_CH0_M1/GPIO1_B4_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4
sai3_lrck	I/O	ETH1_RXD3_M1/SDMMC1_D1_M0/SAI3_LRCK_M1/I2C9_SCL_M1/SPI1_MOSI_M0/PWM1_CH1_M1/GPIO1_B5_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[7:4]=4
sai3_sdo0	O	ETH1_RXCLK_M1/SDMMC1_D2_M0/SAI3_SDO_M1/UART3_CTSN_M2/SPI1_MISO_M0/PCIE0_CLKREQN_M1/GPIO1_B6_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4
sai3_sdi0	I	ETH1_TXD2_M1/SDMMC1_D3_M0/SAI3_SDI_M1/UART3_RTSN_M2/SPI1_CSN0_M0/GPIO1_B7_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4

Table 24-11 SAI3 m2 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai3_mclk	I/O	CAM_CLK1_OUT_M1/ETH_CLK1_25M_OUT_M0/ETH0_MCLK_M1/SAI3_MCLK_M2/SPDIF_RX0_M2/UART9_RTSN_M0/I3C1_SDA_PU_M0/PWM2_CH6_M2/GPIO2_D6_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[11:8]=4
sai3_sclk	I/O	VI_CIF_HREF/ETH0_MDIO_M1/SAI3_SCLK_M2/UART3_TX_M0/SPI3_CLK_M0/I2C7_SCL_M1/GPIO3_A0_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4
sai3_lrck	I/O	VI_CIF_VSYNC/ETH1_PPSTRIG_M0/ETH0_MDC_M1/SAI3_LRCK_M2/UART3_RX_M0/SPI3_MOSI_M0/I2C7_SDA_M1/GPIO3_A1_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4
sai3_sdo0	O	VI_CIF_CLKO/ETH1_PPSCLK_M0/ETH0_RXCTL_M1/SAI3_SDO_M2/SPDIF_RX1_M1/UART3_CTSN_M0/SPI3_MISO_M0/CAN1_TX_M3/MIPI_TE_M1/GPIO3_A2_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4
sai3_sdi0	I	VI_CIF_CLKI/ETH1_PTP_REFCLK_M0/ETH0_RXD1_M1/SAI3_SDI_M2/SPDIF_TX1_M1/UART3_RTSN_M0/SPI3_CSN0_M0/CAN1_RX_M3/GPIO3_A3_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4

Table 24-12 SAI3 m3 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai3_mclk	I/O	SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4
sai3_sclk	I/O	SDMMC0_CLK/FSPI1_CLK_M0/SAI3_SCLK_M3/TEST_CLK_OUT/UART5_TX_M2/I2C5_SCL_M0/SPI0_CLK_M1/I3C1_SDA_PU_M1/GPIO2_A5_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[7:4]=4

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Module Pin	Direction	Pad Name	IOMUX Setting
sai3_lrck	I/O	SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[11:8]=4
sai3_sdo0	O	SDMMC0_CMD/FSPI1_CSN0_M0/SAI3_SDO_M3/UART5_RX_M2/I2C5_SDA_M0/SPI0_CSN0_M1/PWM2_CH4_M0/GPIO2_A4_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[3:0]=4
sai3_sdi0	I	SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/CAN1_TX_M0/I3C1_SDA_M1/GPIO2_A3_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[15:12]=4

Table 24-13 SAI4 m0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai4_mclk	I/O	SAI1_MCLK_M0/SAI4_MCLK_M0/AUPLL_CLK_IN_M2/PWM2_CH5_M0/GPIO4_A2_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[11:8]=2
sai4_sclk	I/O	SAI4_SCLK_M0/PDM1_SDI3_M1/FLEXBUS0_D13_M1/SPI3_MOSI_M2/UART6_TX_M0/I2C4_SCL_M1/CAN0_TX_M2/GPIO4_A4_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[3:0]=2
sai4_lrck	I/O	SAI4_LRCK_M0/PDM1_CLK0_M1/FLEXBUS0_D14_M1/SPI3_MISO_M2/UART6_RX_M0/I2C4_SDA_M1/CAN0_RX_M2/GPIO4_A6_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[11:8]=2
sai4_sdo0	O	SAI1_SDI0_M0/SAI4_SDO_M0/PDM1_SDI0_M1/SPI4_CSN0_M2/SPI3_CSN1_M2/PWM2_CH7_M0/GPIO4_B3_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[15:12]=2
sai4_sdi0	I	SAI1_SDO0_M0/SAI4_SDI_M0/SPI3_CLK_M2/PWM2_CH6_M0/GPIO4_A7_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[15:12]=2

Table 24-14 SAI4 m1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai4_mclk	I/O	VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0]=4
sai4_sclk	I/O	VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12]=4
sai4_lrck	I/O	SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4

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Module Pin	Direction	Pad Name	IOMUX Setting
sai4_sdo0	O	VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/DSMC_INT2/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4
sai4_sdi0	I	VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0]=4

Table 24-15 SAI4 m2 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai4_mclk	I/O	DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[3:0]=2
sai4_sclk	I/O	SAI4_SCLK_M2/VP2_SYNC_OUT/I2C6_SDA_M3/SPI4_CLK_M0/CAN1_RX_M1/PWM2_CH3_M1/GPIO4_C7_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[15:12]=2
sai4_lrck	I/O	ISP_PRELIGHT_TRIG_M1/SAI4_LRCK_M2/DP_HPDIN_M0/I2C3_SCL_M3/SPI4_CSN0_M0/UART6_TX_M3/PWM2_CH6_M1/GPIO4_C4_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[3:0]=2
sai4_sdo0	O	ISP_FLASH_TRIGOUT_M1/SAI4_SDO_M2/VP0_SYNC_OUT/SATA1_ACTLED_M1/I2C3_SDA_M3/SPI4_MOSI_M0/UART6_RX_M3/PWM2_CH5_M1/GPIO4_C5_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[7:4]=2
sai4_sdi0	I	SAI4_SDI_M2/VP1_SYNC_OUT/PCIE0_CLKREQN_M3/SATA0_ACTLED_M1/I2C6_SCL_M3/SPI4_MISO_M0/CAN1_TX_M1/PWM2_CH2_M1/GPIO4_C6_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[11:8]=2

Table 24-16 SAI4 m3 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai4_mclk	I/O	CAM_CLK0_OUT_M1/ETH1_RXD1_M0/SAI4_MCLK_M3/UART6_TX_M1/I3C1_SCL_M0/PWM2_CH2_M2/GPIO2_D2_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[11:8]=4
sai4_sclk	I/O	ETH1_TXD0_M0/SAI4_SCLK_M3/UART4_CTSN_M0/I2C5_SCL_M2/PWM1_CH5_M2/GPIO2_C6_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[11:8]=4
sai4_lrck	I/O	ETH1_TXD1_M0/SAI4_LRCK_M3/UART4_RTSN_M0/I2C5_SDA_M2/PWM0_CH1_M2/GPIO2_C7_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[15:12]=4
sai4_sdo0	O	ETH1_RXD0_M0/SAI4_SDO_M3/UART4_RX_M0/I2C6_SDA_M2/PWM2_CH1_M2/GPIO2_D1_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[7:4]=4

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Module Pin	Direction	Pad Name	IOMUX Setting
sai4_sdi0	I	ETH1_TXCTL_M0/SAI4_SDI_M3/UART4_TX_M0/I2C6_SCL_M2/PWM2_CH0_M2/GPIO2_D0_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[3:0]=4

24.6 Application Notes

24.6.1 Software Application Notes

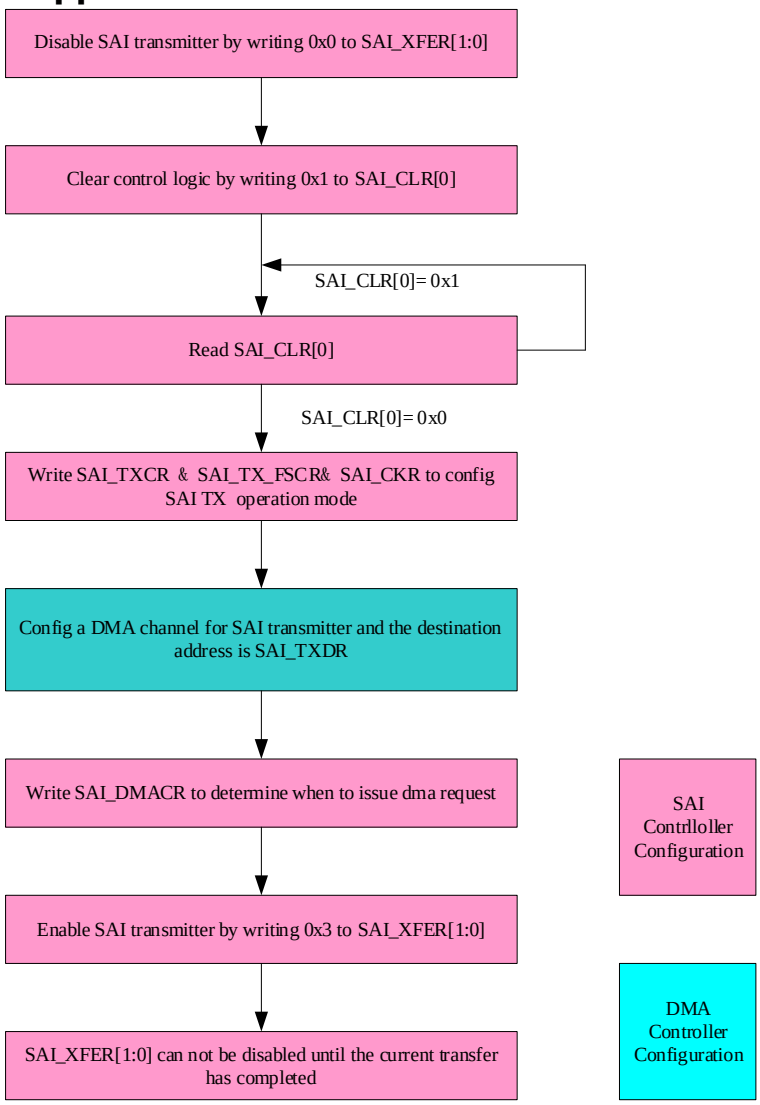
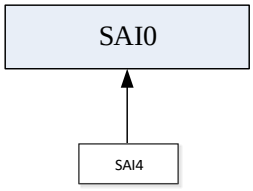


Fig.24-11 SAI controller transmit operation flow chart

Note: User should clear TX/RX logical by CLR[0]/CLR[1] and wait clear operation done before configure the other registers.

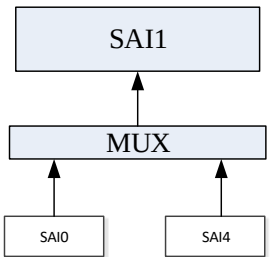
24.6.2 Cascade Function Application Notes

- *sai0 in <- sai4 out*



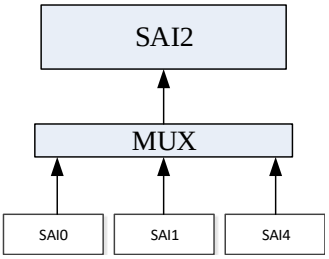
Control cascading relationships by configuring registers SYS_GRF_SOC_CON2[1]

- *sai1 in <- sai0/4 out*



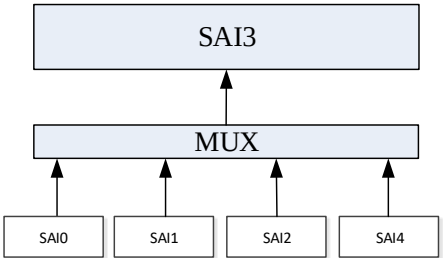
Control cascading relationships by configuring registers SYS_GRF_SOC_CON2[3:2]

- *sai2 in -> sai0/1/4 out*



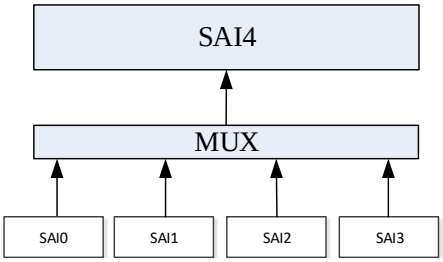
Control cascading relationships by configuring registers SYS_GRF_SOC_CON2[5:4]

- *sai3 in <- sai0/1/2/4 out*



Control cascading relationships by configuring registers SYS_GRF_SOC_CON2[8:6]

- *Sai4 in <- sai0/1/2/3 out*



Control cascading relationships by configuring registers SYS_GRF_SOC_CON2[11:9]

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Chapter 25 Pulse Density Modulation(PDM)

25.1 Overview

The Pulse Density Modulation (PDM) is a PDM interface controller and decoder that support mono PDM format. It integrates a clock generator driving the PDM microphone and embeds filters which decimate the incoming bit stream to obtain most common audio rates.
PDM supports the following features:

- Support one internal 32-bit wide and 128-location deep FIFOs for receiving audio data
- Support receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of receive FIFO full interrupt
- Support combined interrupt output
- Support AHB bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support PDM master receive mode
- Support 4 paths. Each path is composed of two digital microphone channels, the PDM can be used with four stereo or eight mono microphones. Each path is enabled or disabled independently
- Support 16 ~24 bit sample resolution
- Support sample rate:
  8khz, 16khz, 32kHz, 64kHz, 128khz, 11.025khz, 22.05khz, 44.1khz, 88.2khz, 176.4khz, 12khz, 24khz, 48khz, 96khz, 192khz
- Support two 16-bit audio data store together in one 32-bit wide location
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support programmable data sampling sensibility (rising or falling edge)

25.2 Block Diagram

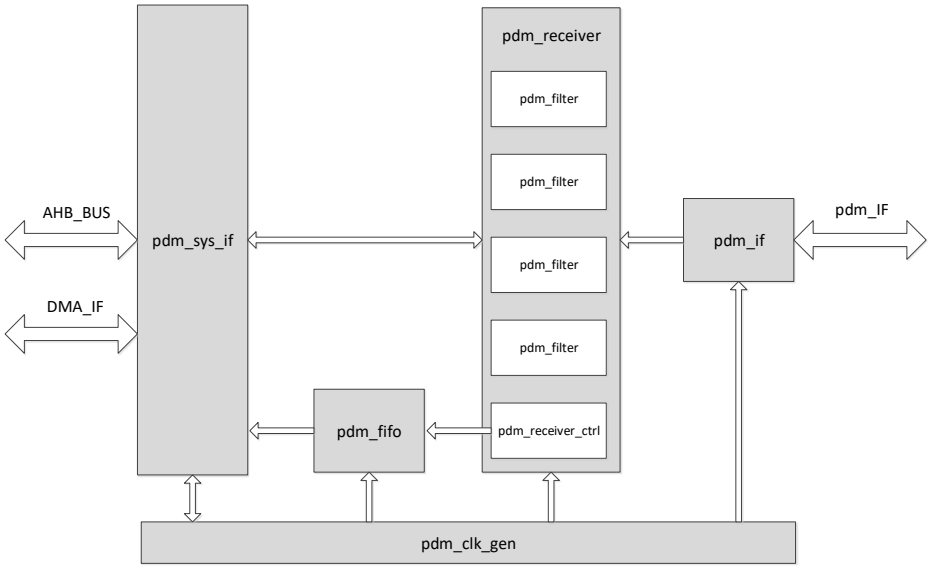

Fig. 25-1 PDM Block Diagram

System Interface
The system interface implements the APB slave operation. It contains not only control registers of receiver inside but also interrupt and DMA handshaking interface.
Receiver
The receiver can act as a decimation filter of PDM. And export PCM format data.
Receive FIFO
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 128.
PDM interface
The PDM interface implements PDM bit streams receive operation.

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25.3 Function Description

25.3.1 AHB Interface

There is an AHB slave interface in PDM. It is responsible for accessing registers and internal memories.

25.3.2 PDM Interface

The PDM interface is a 5-wire interface. The PDM module can support up to four external stereo and eight digital microphones.

Fig.1-2 and Fig.1-3 show two cases of use of the PDM, but all configurations are possible with stereo and mono digital microphones.

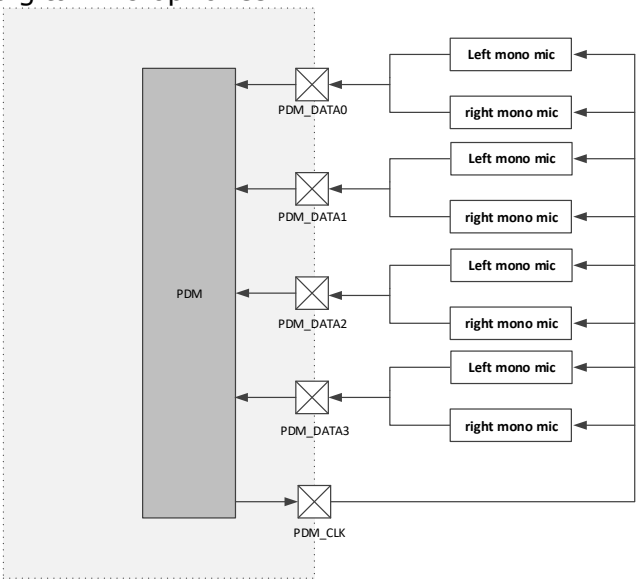

Fig. 25-2 PDM with Eight Mono MIC

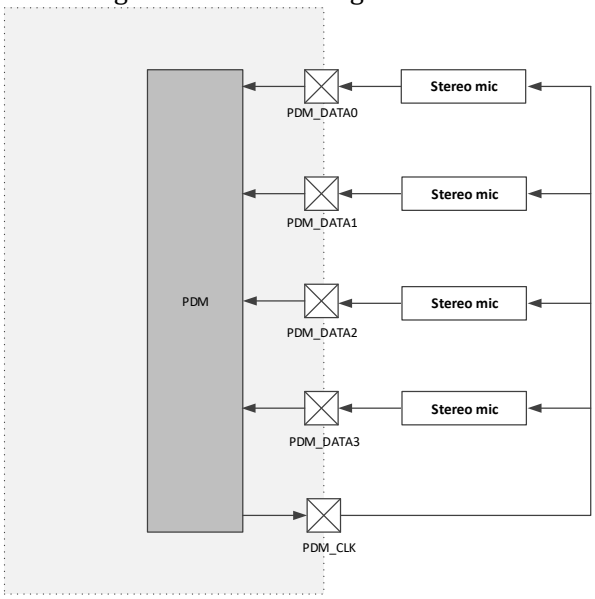

Fig. 25-3 PDM with Four Stereo MIC

The PDM interface consists of a serial-data shift clock output (PDM_CLK) and a serial data input (PDM_DATA). The clock is fanned out to both digital mics, and both digital mics' data (left channel and right channel) outputs share a single signal line. To share a single line, the digital mics tristate their output during one phase of the clock(high or low part of cycle, depending on how they are configured via their L/R input).

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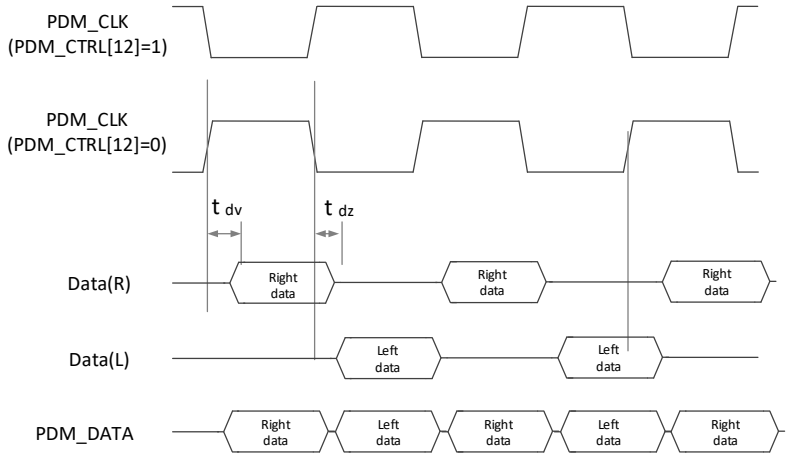

Fig. 25-4 PDM interface diagram with external MIC

25.3.3 Digital Filter

The external PDMIC generates a PDM stream of bits and transfers it in one period or one half-period of the clock provided by the PDM. The aim of the PDM is to process data from the PDM interface, decimate and filter the data, and store the processed data in the FIFO. The four paths are identical. Each path is composed of a left and a right channel. The PDM interface delivers eight parallel data of 1bit. Each bit goes to a filter. The aim of the filter is to limit the noise and export PCM format audio data.

25.3.4 Clock Configuration

MCLK is the source clock signal. PDM_CLK is the output clocks generated in the PDM and is fed to the external microphones. They are also the internal clock of the external microphones. User must take care about the value of PDM_CLK when selecting the source clock (MCLK).

Table 25-1 Relation between PDM_CLK and sample rate

PDM_CLK	Sample rate
3.072Mhz	12khz,24khz,48khz,96khz,192khz
2.8224Mhz	11.025khz,22.05khz,44.1khz,88.2khz,176.4khz
2.048Mhz	8khz,16khz,32kHz,64kHz,128khz

MCLK/PDM_CLK is more than 10;

25.4 Register Description

25.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
PDM0	0x273B0000
PDM1	0x2A6E0000

25.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PDM_SYSCONFIG	0x0000	W	0x00000002	PDM System Configure Register
PDM_CTRL	0x0004	W	0x001C8797	PDM Control Register 0
PDM_FILTER_CTRL	0x0008	W	0x57800000	PDM Clock Control Register
PDM_FIFO_CTRL	0x000C	W	0x0003E000	PDM FIFO Control Register
PDM_DATA_VALID	0x0010	W	0x00000000	PDM Path Data Valid Register
PDM_RXFIFO_DATA_REG	0x0014	W	0x00000000	PDM Receive FIFO Data Register
PDM_DATA0R	0x0018	W	0x00000000	PDM Path0 Right Channel Data Register
PDM_DATA0L	0x001C	W	0x00000000	PDM Path0 Left Channel Data Register

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Name	Offset	Size	Reset Value	Description
PDM_DATA1R	0x0020	W	0x00000000	PDM Path1 Right Channel Data Register
PDM_DATA1L	0x0024	W	0x00000000	PDM Path1 Left Channel Data Register
PDM_DATA2R	0x0028	W	0x00000000	PDM Path2 Right Channel Data Register
PDM_DATA2L	0x002C	W	0x00000000	PDM Path2 Left Channel Data Register
PDM_DATA3R	0x0030	W	0x00000000	PDM Path3 Right Channel Data Register
PDM_DATA3L	0x0034	W	0x00000000	PDM Path3 Left Channel Data Register
PDM_VERSION	0x0038	W	0x23023576	PDM Version Register
PDM_INCR_RXDR	0x0400	W	0x00000000	Increment Address Receive FIFO Data Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

25.4.3 Detail Registers Description

PDM_SYSCONFIG

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	filter_gate_en Filter gate enable If some filters not work, the filter and its corresponding memory clock will be gated if filter_gate_en is 1'b1, otherwise the clock will be still active.
3	RW	0x0	num_start software config enable bit. only vaild data when num_start = 1'b1;
2	RW	0x0	rx_start RX transfer start bit 1'b0: Stop RX transfer 1'b1: Start RX transfer
1	RW	0x1	mem_gate_en 1: memory interface clock auto gating enable 0: memory interface clock auto gating disable
0	RW	0x0	rx_clr PDM RX logic clear This is a self-cleared bit. High active. Write 1'b1: Clear RX logic Write 1'b0: No action Read 1'b1: Clear ongoing Read 1'b0: Clear done

PDM_CTRL

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:27	RW	0x0	path1_ch_sel Left and right channel data sel If path_mode_select = 2'b00 Right channel Left channel 3'b000: path3 left path2 left 3'b001: path3 right path2 left 3'b010: path3 left path2 right 3'b011: path3 right path2 right 3'b100: path2 left path3 left 3'b101: path2 right path3 left 3'b110: path2 left path3 right 3'b111: path2 right path3 right If path_mode_select = 2'b01 Right channel Left channel 3'b000: path3 left path1 left 3'b001: path3 right path1 left 3'b010: path3 left path1 right 3'b011: path3 right path1 right 3'b100: path1 left path3 left 3'b101: path1 right path3 left 3'b110: path1 left path3 right 3'b111: path1 right path3 right If path_mode_select = 2'b10 Right channel Left channel 3'b000: path2 left path1 left 3'b001: path2 right path1 left 3'b010: path2 left path1 right 3'b011: path2 right path1 right 3'b100: path1 left path2 left 3'b101: path1 right path2 left 3'b110: path1 left path2 right 3'b111: path1 right path2 right

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	path0_ch_sel Left and right channel data sel If path_mode_select = 2'b00 Right channel Left channel 3'b000: path1 left path0 left 3'b001: path1 right path0 left 3'b010: path1 left path0 right 3'b011: path1 right path0 right 3'b100: path0 left path1 left 3'b101: path0 right path1 left 3'b110: path0 left path1 right 3'b111: path0 right path1 right If path_mode_select = 2'b01 Right channel Left channel 3'b000: path2 left path0 left 3'b001: path2 right path0 left 3'b010: path2 left path0 right 3'b011: path2 right path0 right 3'b100: path0 left path2 left 3'b101: path0 right path2 left 3'b110: path0 left path2 right 3'b111: path0 right path2 right If path_mode_select = 2'b10 Right channel Left channel 3'b000: path3 left path0 left 3'b001: path3 right path0 left 3'b010: path3 left path0 right 3'b011: path3 right path0 right 3'b100: path0 left path3 left 3'b101: path0 right path3 left 3'b110: path0 left path3 right 3'b111: path0 right path3 right
23:22	RW	0x0	path_mode_select path Select 2'b00: path0 data and path1 data (path2 data and path3 data) 2'b01: path0 data and path2 data (path1 data and path3 data) 2'b10: path0 data and path3 data (path1 data and path2 data)
21	RW	0x0	split_en split enable 1'b1: Enable 1'b0: Disable
20:19	RW	0x3	rx_path_select3 RX Path Select 2'b00: Path3 data from PDM data0 2'b01: Path3 data from PDM data1 2'b10: Path3 data from PDM data2 2'b11: Path3 data from PDM data3

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Bit	Attr	Reset Value	Description
18:17	RW	0x2	rx_path_select2 RX Path Select 2'b00: Path2 data from PDM data0 2'b01: Path2 data from PDM data1 2'b10: Path2 data from PDM data2 2'b11: Path2 data from PDM data3
16:15	RW	0x1	rx_path_select1 RX Path Select 2'b00: Path1 data from PDM data0 2'b01: Path1 data from PDM data1 2'b10: Path1 data from PDM data2 2'b11: Path1 data from PDM data3
14:13	RW	0x0	rx_path_select0 RX Path Select 2'b00: Path0 data from PDM data0 2'b01: Path0 data from PDM data1 2'b10: Path0 data from PDM data2 2'b11: Path0 data from PDM data3
12	RW	0x0	pdm_ch_ex Left and right channel data exchange 1'b0: Not inverted, if mono_path_en, the output path is the Left path. 1'b1: Inverted, if mono_path_en, the output path is the Right path.
11	RW	0x0	sjm_sel Store justified mode Can be written only when SYSCONFIG[2] is 0. 16bit~31bit DATA stored in 32 bits width FIFO. If VDW select 16bit data, this bit is valid only when HWT select 1. Because if HWT is 0, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 1'b0: Right justified 1'b1: Left justified
10	RW	0x1	path3_en Path 3 enable 1'b1: Enable 1'b0: Disable
9	RW	0x1	path2_en Path 2 enable 1'b1: Enable 1'b0: Disable
8	RW	0x1	path1_en Path 1 enable 1'b1: Enable 1'b0: Disable
7	RW	0x1	path0_en Path 0 enable 1'b1: Enable 1'b0: Disable
6	RW	0x0	hwt_en Halfword word transform Only valid when VDW select 16bit data. 1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid

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Bit	Attr	Reset Value	Description
5	RW	0x0	mono_path_enable mono path enable bit. if mono path enable, path0/path1/path2/path3 only one path enable, and the right or left path depended on the lr_ch_ex reg. if data_vld_width cfg right/left data only 16bit, the data write to memory is combinde by two data, {L1, L0} or {R1, R0}.
4:0	RW	0x17	data_vld_width Can be written only when SYSCONFIG[2] is 0. Valid Data width 0~14: Reserved 15: 16bit 16: 17bit 17: 18bit 18: 19bit ..... n: (n+1)bit 23: 24bit

PDM_FILTER_CTRL

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0xaf	gain_ctrl 0: 65.625dB 1: -65.25dB .... 175: 0dB 255: 30dB step:0.375dB
22	RW	0x0	hpf_ctrll High-pass filter enable for left channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
21	RW	0x0	hpf_ctrlr High-pass filter enable for right channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
20:19	RW	0x0	hpf_ctrl0 High-pass filter configure 2'b00: 3.79Hz 2'b01: 60Hz 2'b10: 243Hz 2'b11: 493Hz
18	RW	0x0	fir_com_bps Fir compensate filter bypass 1'b0: Not bypass 1'b1: Bypass
17	RW	0x0	sig_scale_mode Signal scale mode select 1'b0: CIC outputs the normal latitude. 1'b1: Scale the CIC outputs to half of the normal latitude and scale 2 times after hpf-filter.
16:10	RW	0x00	cic_scale cic scale bits

Bit	Attr	Reset Value	Description
9:1	RW	0x000	cic_value cic filter r value
0	RW	0x0	filter_en contrl hb2 en 1'b0: off 1'b1:on

PDM_FIFO_CTRL

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RO	0x00	rfl Receive FIFO level Contains the number of valid data entries in the receive FIFO.
19:13	RW	0x1f	rdl Receive data level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
12	RW	0x0	rde Receive DMA enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
11	RO	0x0	rxoi RX overflow interrupt 1'b0: Inactive 1'b1: Active
10	RO	0x0	rxfi RX full interrupt 1'b0: Inactive 1'b1: Active
9	RW	0x0	rxoic RX overflow interrupt clear (high active, auto clear).
8:2	RW	0x00	rft Receive FIFO threshold When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO threshold interrupt is triggered.
1	RW	0x0	rxoie RX overflow interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	rxftie RX full threshold interrupt enable 1'b0: Disable 1'b1: Enable

PDM_DATA_VALID

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RC	0x0	path0_vld 1'b0: DATA0R_REG, DATA0L_REG value is invalid. 1'b1: DATA0R_REG, DATA0L_REG value is valid.

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Bit	Attr	Reset Value	Description
2	RC	0x0	path1_vld 1'b0: DATA1R_REG, DATA1L_REG value is invalid. 1'b1: DAT1R_REG, DATA1L_REG value is valid.
1	RC	0x0	path2_vld 1'b0: DATA2R_REG, DATA2L_REG value is invalid. 1'b1: DATA2R_REG, DATA2L_REG value is valid.
0	RC	0x0	path3_vld 1'b0: DATA3R_REG, DATA3L_REG value is invalid. 1'b1: DATA3R_REG, DATA3L_REG value is valid.

PDM_RXFIFO_DATA_REG

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdr Receive FIFO shadow register When the register is read, data in the receive FIFO is accessed.

PDM_DATA0R

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0r Data of the path 0 right channel

PDM_DATA0L

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0l Data of the path 0 left channel

PDM_DATA1R

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1r Data of the path 1 right channel

PDM_DATA1L

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1l Data of the path 1 left channel

PDM_DATA2R

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2r Data of the path 2 right channel

PDM_DATA2L

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2l Data of the path 2 left channel

PDM_DATA3R

Address: **Operational Base** + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3r Data of the path 3 right channel

PDM_DATA3L

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3l Data of the path 3 left channel

PDM_VERSION

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x23023576	ver PDM version

PDM_INCR_RXDR

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	receive_fifo_data FIFO data can be read from these registers. This register is used when the access address is increment.

25.5 Interface Description

The following table shows the PDM interface description.

Table 25-2 PDM0 M0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
O_pdm_clk(0)	O	SAI0_MCLK_M1/PDM0_CLK0_M0/UART10_TX_M2/PWM0_CH0_M0/GPIO0_C4_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[3:0]=4'h3
O_pdm_clk(1)	O	PDM0_CLK1_M0/HDMI_TX_CEC_M1/SPI0_CSN1_M0/PWM0_CH1_M0/GPIO0_C3_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[15:12]=4'h3
I_pdm_data0	I	SAI0_SDI0_M1/PDM0_SDI0_M0/SPI0_MOSI_M0/GPIO0_D0_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[3:0]=4'h3
I_pdm_data1	I	SAI0_SDI1_M1/SAI0_SDO3_M1/PDM0_SDI1_M0/SPI0_MISO_M0/GPIO0_D1_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[7:4]=4'h3
I_pdm_data2	I	SAI0_SDI2_M1/SAI0_SDO2_M1/PDM0_SDI2_M0/I2C4_SCL_M0/CPUBIG_AVS/PWM1_CH5_M0/UART1_CTSN_M0/GPIO0_D2_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[11:8]=4'h3
I_pdm_data3	I	SAI0_SDI3_M1/SAI0_SDO1_M1/PDM0_SDI3_M0/I2C4_SDA_M0/GPU_AVS/PWM2_CH0_M0/UART1_RTSN_M0/GPIO0_D3_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[15:12]=4'h3

Table 25-3 PDM0 M1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
O_pdm_clk(0)	O	EMMC_CLK/FSPI0_CLK/SAI0_SDO3_M2/SAI0_SDI1_M2/PDM0_CLK0_M1/PWM2_CH7_M1/GPIO1_B1_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[7:4]=4'h5
O_pdm_clk(1)	O	EMMC_D6/SAI3_LRCK_M	TOP_IOC_GPIO1A_IOMUX_S

		0/PDM0_CLK1_M1/SPI0_MISO_M2/I2C9_SDA_M0/GPIO1_A6_u	EL_H[11:8]=4'h5
I_pdm_data0	I	EMMC_STRB/SAI0_SDI0_M2/SAI3_SDO_M0/PDM0_SDI0_M1/SPI0_CSN1_M2/GPIO1_B2_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[11:8]=4'h5
I_pdm_data1	I	EMMC_D3/FSPI0_D3/SAI0_SDO2_M2/SAI0_SDI2_M2/PDM0_SDI1_M1/UART7_RX_M1/UART6_CTSN_M2/GPIO1_A3_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4'h5
I_pdm_data2	I	EMMC_D5/SAI3_SCLK_M0/PDM0_SDI2_M1/SPI0_MOSI_M2/I2C9_SCL_M0/GPIO1_A5_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[7:4]=4'h5
I_pdm_data3	I	EMMC_D2/FSPI0_D2/SAI0_SDO1_M2/SAI0_SDI3_M2/PDM0_SDI3_M1/UART7_TX_M1/UART6_RTSN_M2/GPIO1_A2_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4'h5

Table 25-4 PDM0 M2 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
O_pdm_clk(0)	O	ETH1_TXCLK_M1/SDMMC1_CLK_M0/SAI3_MCLK_M1/PDM0_CLK0_M2/UART3_RX_M2/GPIO1_C1_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[7:4]=4'h5
O_pdm_clk(1)	O	ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'h5
I_pdm_data0	I	ETH1_TXCTL_M1/FSPI1_D2_M1/PDM0_SDI0_M2/UART2_TX_M0/I2C8_SCL_M1/SATA_CPPOD/GPIO1_C6_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[11:8]=4'h5
I_pdm_data1	I	ETH1_RXD0_M1/FSPI1_D3_M1/PDM0_SDI1_M2/UART2_RX_M0/I2C8_SDA_M1/SATA_CPDET/GPIO1_C7_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[15:12]=4'h5
I_pdm_data2	I	ETH1_TXD3_M1/SDMMC1_CMD_M0/PDM0_SDI2_M2/UART3_TX_M2/SPI1_CSN1_M0/PWM0_CH0_M1/GPIO1_C0_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[3:0]=4'h5
I_pdm_data3	I	ETH1_MCLK_M1/SAI2_MCLK_M0/PDM0_SDI3_M2/SPDIF_RX1_M2/UART10_RTSN_M1/I2C5_SCL_M1/GPIO1_D4_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[3:0]=4'h5

Table 25-5 PDM0 M3 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
O_pdm_clk(0)	O	VI_CIF_D8/SDMMC1_DETN_M1/ETH0_RXCLK_M1/SAI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/SATA1_ACTLED_M0/GPIO2_B5_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[7:4]=4'h5
O_pdm_clk(1)	O	VI_CIF_D10/SDMMC1_CLK_M1/ETH0_TXCLK_M1/S	TOP_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4'h5

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		AI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/PCIE1_CLKREQN_M0/GPIO2_B3_d	
I_pdm_data0	I	VI_CIF_D9/SDMMC1_PWREN_M1/ETH0_TXD2_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/SATA0_ACTLED_M0/GPIO2_B4_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[3:0]=4'h5
I_pdm_data1	I	VI_CIF_D11/SDMMC1_CMD_M1/ETH0_TXD3_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCIE0_CLKREQN_M0/GPIO2_B2_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[11:8]=4'h5
I_pdm_data2	I	VI_CIF_D12/SDMMC1_D3_M1/ETH0_TXD0_M1/SAI0_SDI1_M0/PDM0_SDI2_M3/UART1_RX_M1/GPIO2_B1_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[7:4]=4'h5
I_pdm_data3	I	VI_CIF_D13/SDMMC1_D2_M1/ETH0_TXD1_M1/SAI0_SDI0_M0/PDM0_SDI3_M3/UART1_TX_M1/GPIO2_B0_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[3:0]=4'h5

Table 25-6 PDM1 M0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
O_pdm_clk(0)	O	VI_CIF_D0/ETH1_TXCLK_M0/SAI2_SDI_M1/PDM1_CLK0_M0/UART11_RX_M1/SPI1_CLK_M1/PWM1_CH4_M2/GPIO2_C5_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[7:4]=4'h5
O_pdm_clk(1)	O	VI_CIF_D4/ETH1_RXD3_M0/ETH0_PPSCLK_M1/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[7:4]=4'h5
I_pdm_data0	I	VI_CIF_D1/ETH1_TXD3_M0/SAI2_SDO_M1/PDM1_SDI0_M0/UART11_TX_M1/SPI1_CSN0_M1/PWM1_CH3_M2/GPIO2_C4_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[3:0]=4'h5
I_pdm_data1	I	VI_CIF_D5/ETH1_RXD2_M0/ETH0_PTP_REFCLK_M1/PDM1_SDI1_M0/UART9_RX_M0/PWM1_CH0_M2/GPIO2_C0_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[3:0]=4'h5
I_pdm_data2	I	VI_CIF_D3/ETH1_RXCLK_M0/ETH0_PPSTRIG_M1/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[11:8]=4'h5
I_pdm_data3	I	VI_CIF_D2/ETH1_TXD2_M0/SAI2_LRCK_M1/PDM1_SDI3_M0/UART11_RTSN_M1/SPI1_MISO_M1/PWM0_CH0_M2/GPIO2_C3_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[15:12]=4'h5

Table 25-7 PDM1 M1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
O_pdm_clk(0)	O	SAI4_LRCK_M0/PDM1_CLK0_M1/FLEXBUS0_D14_M	TOP_IOC_GPIO4A_IOMUX_SEL_H[11:8]=4'h3

		1/SPI3_MISO_M2/UART6_RX_M0/I2C4_SDA_M1/CAN0_RX_M2/GPIO4_A6_d	
O_pdm_clk(1)	O	SAI1_SDO1_M0/SAI1_SDI3_M0/PDM1_CLK1_M1/FLEXBUS1_D13_M1/SPI4_CLK_M2/UART5_TX_M1/UART6_RTSN_M0/UART2_RTSN_M1/GPIO4_B0_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'h3
I_pdm_data0	I	SAI1_SDI0_M0/SAI4_SDO_M0/PDM1_SDI0_M1/SPI4_CSN0_M2/SPI3_CSN1_M2/PWM2_CH7_M0/GPIO4_B3_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'h3
I_pdm_data1	I	SAI1_SDO3_M0/SAI1_SDI1_M0/PDM1_SDI1_M1/FLEXBUS1_D15_M1/SPI4_MISO_M2/MIPI_TE_M0/GPIO4_B2_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[11:8]=4'h3
I_pdm_data2	I	SAI1_SDO2_M0/SAI1_SDI2_M0/PDM1_SDI2_M1/FLEXBUS1_D14_M1/SPI4_MOSI_M2/UART5_RX_M1/UART6_CTSN_M0/UART2_CTSN_M1/GPIO4_B1_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[7:4]=4'h3
I_pdm_data3	I	SAI4_SCLK_M0/PDM1_SDI3_M1/FLEXBUS0_D13_M1/SPI3_MOSI_M2/UART6_TX_M0/I2C4_SCL_M1/CAN0_TX_M2/GPIO4_A4_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[3:0]=4'h3

Table 25-8 PDM1 M2 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
O_pdm_clk(0)	O	VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[7:4]=4'h4
O_pdm_clk(1)	O	VO_LCDC_D20/VO_EBC_VCOM/ETH0_RXCTL_M0/PDM1_CLK1_M2/DSMC_DATA13/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[15:12]=4'h4
I_pdm_data0	I	VO_LCDC_D16/VO_EBC_SDCE0/ETH0_TXCTL_M0/PDM1_SDI0_M2/DSMC_DATA10/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[15:12]=4'h4
I_pdm_data1	I	VO_LCDC_D17/VO_EBC_SDCE1/ETH0_RXD0_M0/PDM1_SDI1_M2/DSMC_DATA11/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[11:8]=4'h4
I_pdm_data2	I	VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8]=4'h4
I_pdm_data3	I	VO_LCDC_D22/VO_EBC_	TOP_IOC_GPIO3A_IOMUX_S

		GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	EL_H[7:4]=4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

25.6 Application Notes

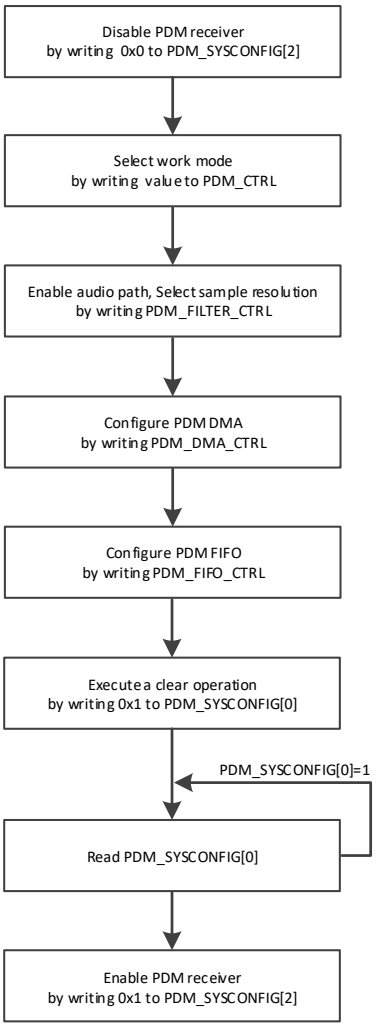

Fig. 25-5 PDM operation flow

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Chapter 26 Sony/Philips Digital Interface Transmitter (SPDIF TX)

26.1 Overview

The SPDIF_TX is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to carry stereophonic programmes, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible.
When used for other purposes, the interface is primarily intended to carry audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to carry data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
In all cases, the clock references and auxiliary information are transmitted along with the programme.MCLK is the operation clock of SPDIF_TX .

Table 26-1 Maximum Frequency of MCLK for the SPDIF_TX

SPDIF	Maximum frequency of MCLK
SPDIF_TX	100MHz

Each SPDIF_TX supports following features.

- Support one internal 32-bit wide and 32-location deep sample data buffer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support AHB and APB bus interface
- Support biphase format stereo audio data output
- Support DMA handshake interface and configurable DMA water level
- Support sample data buffer empty and block terminate interrupt
- Support combine interrupt output
- Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
- Support 48, 44.1, 32kHz sample rate
- Support MCLK frequencies of 12.288Mhz, 8.192Mhz and 11.2896Mhz
- Support 16, 20, 24 bits audio data transfer
- Support frame transmission frequency, fixed to 128 times of audio data sampling rate

26.2 Block Diagram

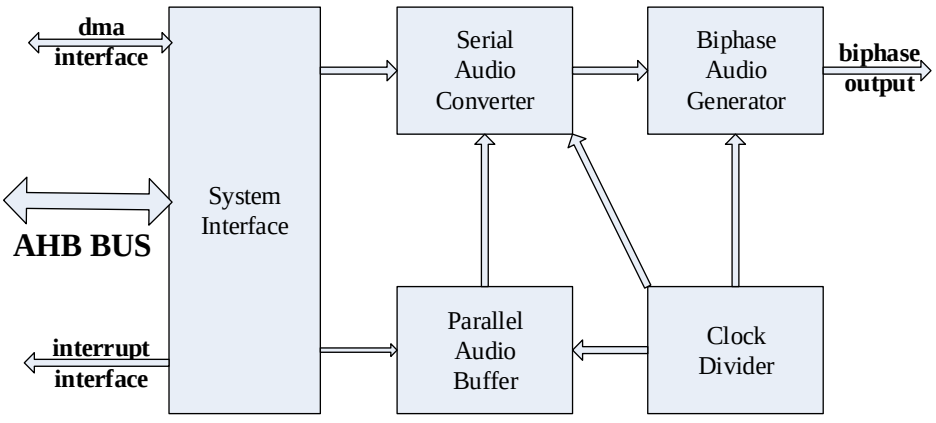

Fig.26-1 SPDIF_TX Block Diagram

The SPDIF_TX is composed of following module.

System Interface

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

Clock Divider

The clock divider implements clock generation function. It divides the source clock MCLK to generate the working clock used for the digital audio data transformation and transmission.

Parallel Audio Buffer

The parallel audio buffer stores the audio data to be transmitted. The size of the FIFO is 32bits x 32.

Serial Audio Converter

The serial audio converter converts the parallel audio data from the parallel audio buffer to the serial audio data.

Biphase Audio Generator

The biphase audio generator reads serial audio data from the serial audio converter and generates biphase audio data based on IEC-60958 standard.

26.3 Function Description

26.3.1 Frame Format

A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of transmission of frames corresponds exactly to the source sampling frequency.
In the 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. The first sub-frame(left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information. The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

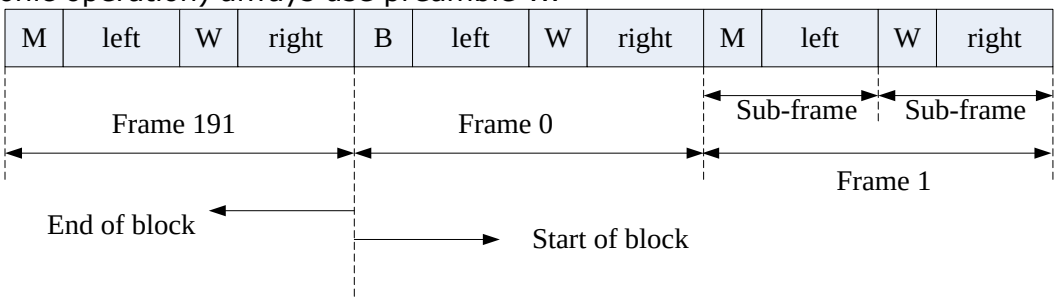

Fig.26-2 SPDIF_TX Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

26.3.2 Sub-frame Format

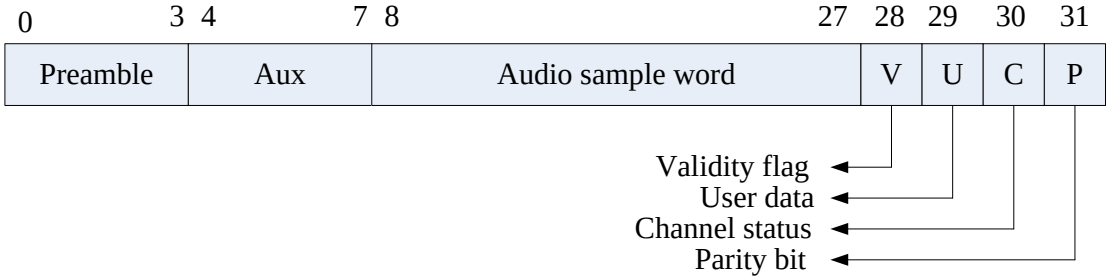

Fig.26-3 SPDIF_TX Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8.Time slot 4 to 7

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may be used for other application. Under these circumstances, the bits in the time slot 4 to 7 are designated auxiliary sample bits.
If the source provides fewer bits than the interface allows (either 24 or 20), the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

26.3.3 Channel Coding

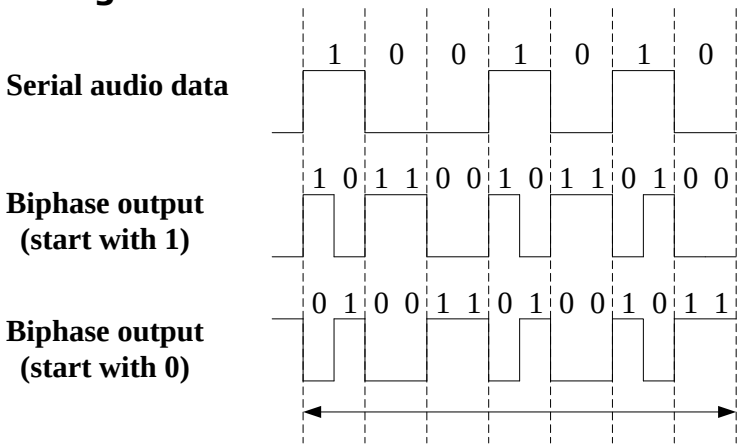

Fig.26-4 SPDIF_TX Channel Coding

To minimize the direct current component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.
Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'.However, it is different from the first if the bit is logical '1'.

26.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.
To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.
A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

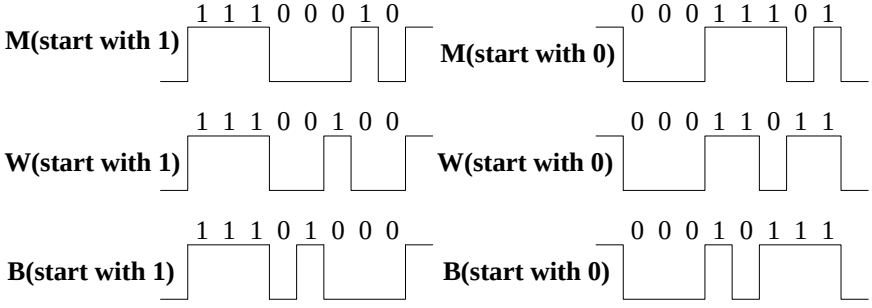

Fig.26-5 SPDIF_TX Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

26.4 Register Description

26.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SPDIF_TX0	0x2A670000
SPDIF_TX1	0x2A680000
SPDIF_TX2	0x27D20000
SPDIF_TX3	0x27EA0000
SPDIF_TX4	0x27EB0000
SPDIF_TX5	0x27EC0000

26.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPDIF_TX_CFGR	0x0000	W	0x00000000	Transfer Configuration Register
SPDIF_TX_SDBLR	0x0004	W	0x00000000	Sample Date Buffer Level Register
SPDIF_TX_DMACR	0x0008	W	0x00000000	DMA Control Register
SPDIF_TX_INTCR	0x000C	W	0x00000000	Interrupt Control Register
SPDIF_TX_INTSR	0x0010	W	0x00000000	Interrupt Status Register
SPDIF_TX_XFER	0x0018	W	0x00000000	Transfer Start Register
SPDIF_TX_SMPDR	0x0020	W	0x00000000	Sample Data Register
SPDIF_TX_VLDFRn	0x0060	W	0x00000000	Validity Flag Register n
SPDIF_TX_USRDRn	0x0090	W	0x00000000	User Data Register n
SPDIF_TX_CHNSRn	0x00C0	W	0x00000000	Channel Status Register n
SPDIF_TX_BURTSINFO	0x00D0	W	0x00000000	This define the channel burst info when the channel conveys non-linear PCM.
SPDIF_TX_REPETTION	0x0104	W	0x00000000	This register provides the repetition of the bitstream when channel conveys non-linear PCM. In the design, it is define the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design.
SPDIF_TX_BURTSINFO_SHD	0x0108	W	0x00000000	This define the channel burst info when the channel conveys non-linear PCM.
SPDIF_TX_REPETTION_SHD	0x010C	W	0x00000000	This register provides the repetition of the bitstream when channel conveys non-linear PCM
SPDIF_TX_USRDR_SHDn	0x0190	W	0x00000000	Shadow User Data Register n

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.4.3 Detail Registers Description

SPDIF_TX_CFGR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	MCD Fmclk/Fsdo This parameter can be calculated by Fmclk/(Fs*128). Fs=the sample frequency be wanted
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	PRECHANGE 0: no linear PCM length 1: 192 block
8	RW	0x0	PCMTYPE 0: linear PCM 1: non-linear PCM
7	WO	0x0	CLR Write 1 to clear mclk domain logic. Read return zero.
6	RW	0x0	CSE 0: disable 1: enable The bit should be set to 1 when the channel conveys non-linear PCM
5	RW	0x0	UDE 0: disable 1: enable
4	RW	0x0	VFE 0: disable 1: enable
3	RW	0x0	ADJ 0: Right justified 1: Left justified
2	RW	0x0	HWT 0: disable 1: enable It is valid only when the valid data width is 16bit.
1:0	RW	0x0	VDW 00: 16bit 01: 20bit 10: 24bit 11: reserved The valid data width is 16bit only for non-linear PCM

SPDIF_TX_SDBLR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	SDBLR Contains the number of valid data entries in the sample data buffer.

SPDIF_TX_DMACR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	TDE 0: Transmit DMA disabled 1: Transmit DMA enabled
4:0	RW	0x00	TDL This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the Sample Date Buffer is equal to or below this field value

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SPDIF_TX_INTCR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	W1C	0x0	UDTIC Write '1' to clear the user data interrupt.
16	W1C	0x0	BTTIC Write 1 to clear the interrupt.
15:10	RO	0x00	reserved
9:5	RW	0x00	SDBT Sample Date Buffer Threshold for empty interrupt
4	RW	0x0	SDBEIE 0: disable 1: enable
3	RW	0x0	BTTIE When enabled, an interrupt will be asserted when the block transfer is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM. 0: disable 1: enable
2	RW	0x0	UDTIE 0: disable 1: enable If enabled, an interrupt will be asserted when the content of the user data register is fed into the corresponding shadow register
1:0	RO	0x0	reserved

SPDIF_TX_INTSR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SDBEIS 0: inactive 1: active
3	RW	0x0	BTTIS 0: inactive 1: active
2	RW	0x0	UDTIS 0: inactive 1: active
1:0	RO	0x0	reserved

SPDIF_TX_XFER

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	XFER Transfer Start Register

SPDIF_TX_SMPDR

Address: **Operational Base** + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SMPDR Sample Data Register

SPDIF_TX_VLDFRn

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VLDFR_SUB_1 Validity Flag Register 0
15:0	RW	0x0000	VLDFR_SUB_0 Validity Flag for Subframe 0

SPDIF_TX_USRDRn

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	USR_SUB_1 User Data Bit for Subframe 1
15:0	RW	0x0000	USR_SUB_0 User Data Bit for Subframe 0

SPDIF_TX_CHNSRn

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CHNSR_SUB_1 Channel Status Bit for Subframe 1
15:0	RW	0x0000	CHNSR_SUB_0 Channel Status Bit for Subframe 0

SPDIF_TX_BURTSINFO

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PD Preamble Pd for non-linear pcm, indicating the length of burst payload in unit of bytes or bits.
15:13	RW	0x0	BSNUM This field indicates the bitstream number. Usually the birstream number is 0.
12:8	RW	0x00	DATAINFO This field gives the data-type-dependent info
7	RW	0x0	ERRFLAG 0: indicates a valid burst-payload 1: indicates that the burst-payload may contain errors

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	DATATYPE 0000000: null data 0000001: AC-3 data 0000011: Pause data 0000100: MPEG-1 layer 1 data 0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 0000110: MPEG-2 data with extension 0000111: MPEG-2 AAC 0001000: MPEG-2, layer-1 low sampling frequency 0001001: MPEG-2, layer-2 low sampling frequency 0001010: MPEG-2, layer-3 low sampling frequency 0001011: DTS type I 0001100: DTS type II 0001101: DTS type III 0001110: ATRAC 0001111: ATRAC 2/3 0010000: ATRAC-X 0010001: DTS type IV 0010010: WMA professional type I 0110010: WMA professional type II 1010010: WMA professional type III 1110010: WMA professional type IV 0010011: MPEG-2 AAC low sampling frequency 0110011: MPEG-2 AAC low sampling frequency 1010011: MPEG-2 AAC low sampling frequency 1110011: MPEG-2 AAC low sampling frequency 0010100: MPEG-4 AAC 0110100: MPEG-4 AAC 1010100: MPEG-4 AAC 1110100: MPEG-4 AAC 0010101: Enhanced AC-3 0010110: MAT others: reserved

SPDIF_TX_REPETTION

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	REPETTION This define the repetition period when the channel conveys non-linear PCM

SPDIF_TX_BURTSINFO_SHD

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	PD Preamble Pd for non-linear pcm, indicating the length of burst payload in unit of bytes or bits.
15:13	RO	0x0	BSNUM This field indicates the bitstream number. Usually the birstream number is 0.
12:8	RO	0x00	DATAINFO This field gives the data-type-dependent info

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Bit	Attr	Reset Value	Description
7	RO	0x0	ERRFLAG 0: indicates a valid burst-payload 1: indicates that the burst-payload may contain errors
6:0	RO	0x00	DATATYPE 0000000: null data 0000001: AC-3 data 0000011: Pause data 0000100: MPEG-1 layer 1 data 0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 0000110: MPEG-2 data with extension 0000111: MPEG-2 AAC 0001000: MPEG-2, layer-1 low sampling frequency 0001001: MPEG-2, layer-2 low sampling frequency 0001010: MPEG-2, layer-3 low sampling frequency 0001011: DTS type I 0001100: DTS type II 0001101: DTS type III 0001110: ATRAC 0001111: ATRAC 2/3 0010000: ATRAC-X 0010001: DTS type IV 0010010: WMA professional type I 0110010: WMA professional type II 1010010: WMA professional type III 1110010: WMA professional type IV 0010011: MPEG-2 AAC low sampling frequency 0110011: MPEG-2 AAC low sampling frequency 1010011: MPEG-2 AAC low sampling frequency 1110011: MPEG-2 AAC low sampling frequency 0010100: MPEG-4 AAC 0110100: MPEG-4 AAC 1010100: MPEG-4 AAC 1110100: MPEG-4 AAC 0010101: Enhanced AC-3 0010110: MAT others: reserved

SPDIF_TX_REPETTION_SHD

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	REPETTION This register provides the repetition of the bitstream when channel conveys non-linear PCM. In the design, it is define the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design.

SPDIF_TX_USRDR_SHDn

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	USR_SUB_1 User Data Bit for Subframe 1
15:0	RO	0x0000	USR_SUB_0 User Data Bit for Subframe 0

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26.5 Interface Description

SPDIF_TX are used to communicate with audio equipment outside this chip. Following table shows the interface of SPDIF_TX.

Table 26-2 SPDIF_TX0 m0 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdo	O	SPDIF_TX0_M0/FLEXBUS0_D15_M1/UART2_TX_M1/I2C3_SCL_M0/PCIE0_CLKREQN_M2/CAN1_TX_M2/GPIO4_B5_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4’ h1

Table 26-3 SPDIF_TX0 m1 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdo	O	VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/DSMC_INT2/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4’ h2

Table 26-4 SPDIF_TX0 m2 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdo	O	CAM_CLK2_OUT_M1/ETH1_MCLK_M0/ETH_CLK0_25M_OUT_M1/SAI0_SDO3_M0/SPDIF_TX0_M2/UART9_CTSN_M0/SPI3_CSN1_M0/PWM2_CH7_M2/GPIO2_D7_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[15:12]=4’ h5

Table 26-5 SPDIF_TX1 m0 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdo	O	VO_LCDC_D14/VO_EBC_SDDO14/ETH0_TXD0_M0/SPDIF_TX1_M0/DSMC_DATA8/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4’ h4

Table 26-6 SPDIF_TX1 m1 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdo	O	VI_CIF_CLKI/ETH1_PTP_REFCLK_M0/ETH0_RXD1_M1/SAI3_SDI_M2/SPDIF_TX1_M1/UART3_RTSN_M0/SPI3_CSN0_M0/CAN1_RX_M3/GPIO3_A3_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4’ h5

Table 26-7 SPDIF_TX1 m2 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdo	O	ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4’ h6

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26.6 Application Notes

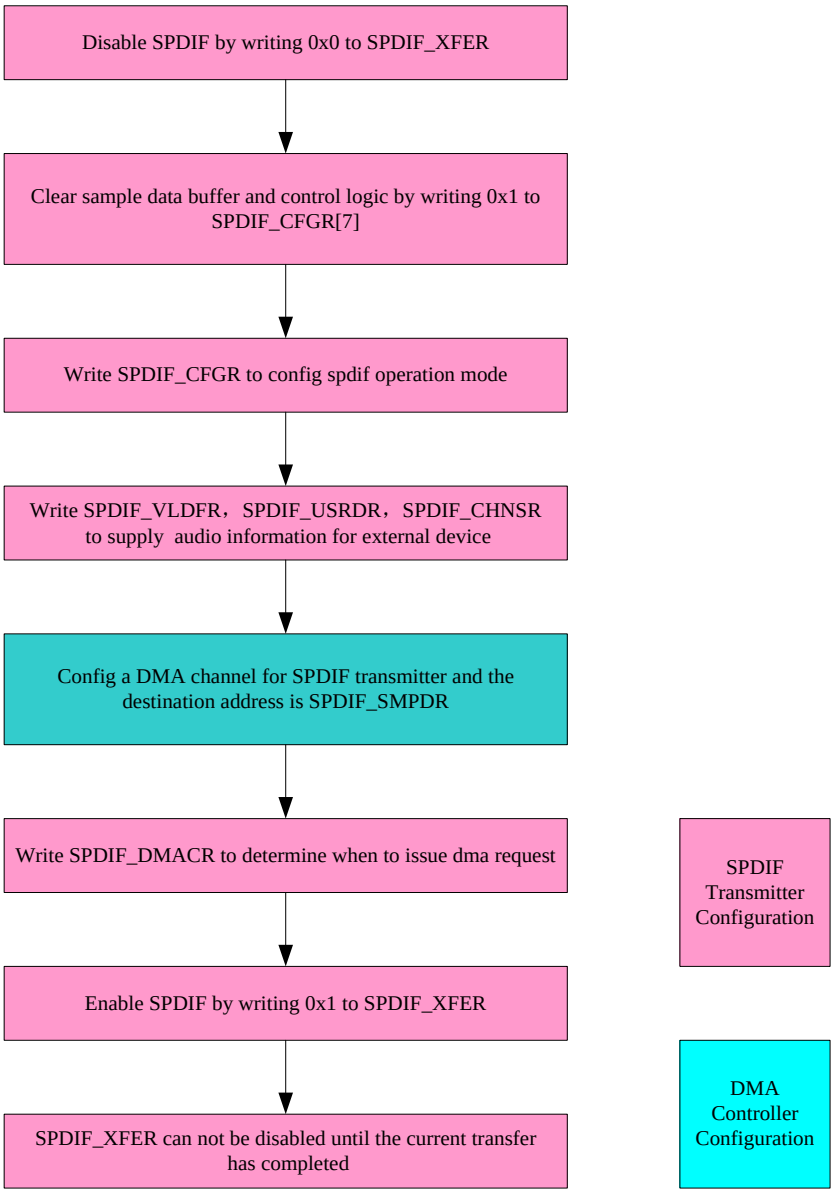

Fig.26-6 SPDIF_TX operation flow chart

The above figure shows the operation flow of SPDIF_TX operation. Note that the configuration register can be written only when the transfer is stopped.

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Chapter 27 SPDIF Receiver

27.1 Overview

The SPDIF_RX is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to receive monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to receive signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to receive stereophonic programmes, with a resolution of up to 24 bits per sample.
When used for other purposes, the interface is primarily intended to receive audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to receive data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
There are 3 SPDIF_RX in total. That are SPDIF_RX0, SPDIF_RX1 accessing IO and SPDIF_RX2 accessing HDPTXPHY . Each of them supports following features.

- Support AHB Bus Interface
- Support one internal 30-bit wide and 32-location deep FIFO for receiving audio data
- Support combined interrupt output
- Support DMA handshaking interface and configurable DMA water level
- Support liner PCM(IEC60958) and non-liner PCM(IEC61937)
- Support 16~24 bits audio sample length for liner PCM application
- Support 16 bits audio sample length for non-liner PCM application
- Support up to 384kHz sample rate with the corresponding reference clock equal to 384KHz*64*2*10, that is 491.52MHz
- Support the frequency of reference clock is at least 10 times the frequency of the biphase encoding clock, but not more than 256 times
- Support recovering clock and audio data from input bitstream

Table 27-1 Maximum Frequency of MCLK for the SPDIF_RX

SPDIF	Maximum frequency of MCLK
SPDIF_RX	500MHz

27.2 Block Diagram

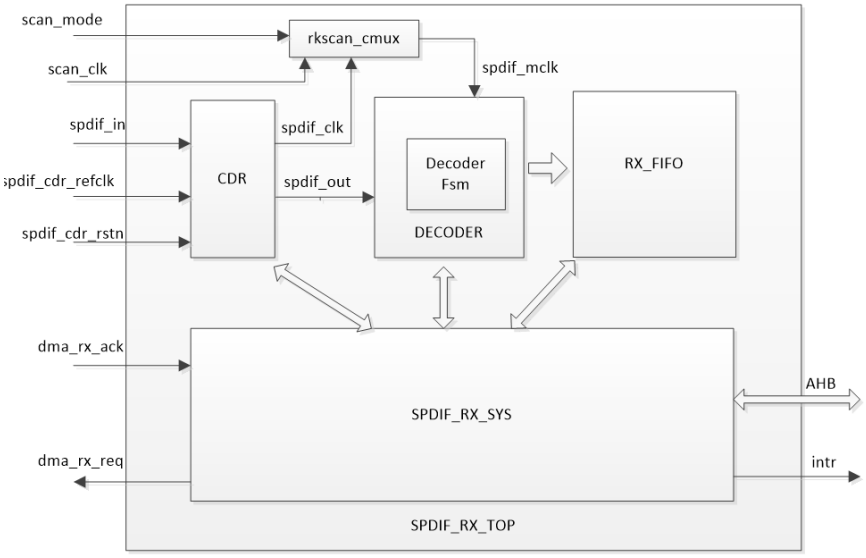

Fig.27-1 SPDIF_RX Block Diagram

The SPDIF_RX is composed of following modules.

SPDIF_RX_SYS

The module implements the AHB slave operation. It contains not only control registers of SPDIF_RX inside but also interrupt and DMA handshaking interface.

CDR

The CDR is short for clock and data recovery. Clock and data can be recovered from the input bitstream by using a high frequency reference clock.

DECODER

The clock recovered from the CDR is used as the working clock to decode the input bitstream such as extracting audio data, the corresponding preamble code, V/U/C/P flags and other audio information.

RX_FIFO

The RX FIFO stores the audio data extracted from input bitstream. The size of the FIFO is 30bitsx32.

27.3 Function description

27.3.1 Frame Format

SPDIF_RX follows the same protocol(IEC60958/IEC61937) as SPDIF_TX. A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of receiving of frames corresponds exactly to the source sampling frequency.

In the 2-channel operation mode, the samples received from both channels are arranged by time multiplexing in consecutive sub-frames. The first subframe(left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information. The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

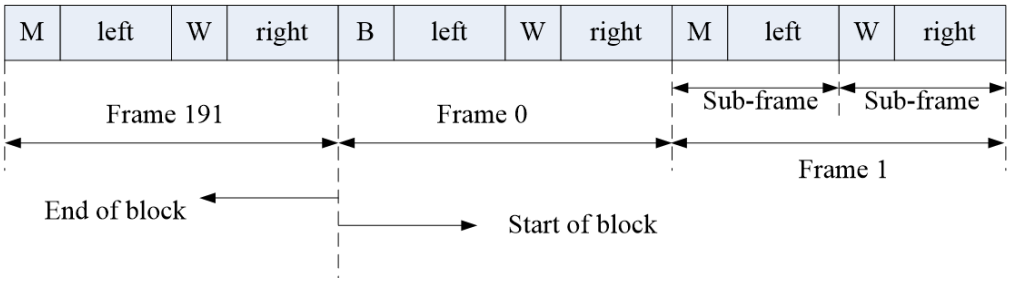

Fig.27-2 SPDIF_RX Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

27.3.2 Sub-frame Format

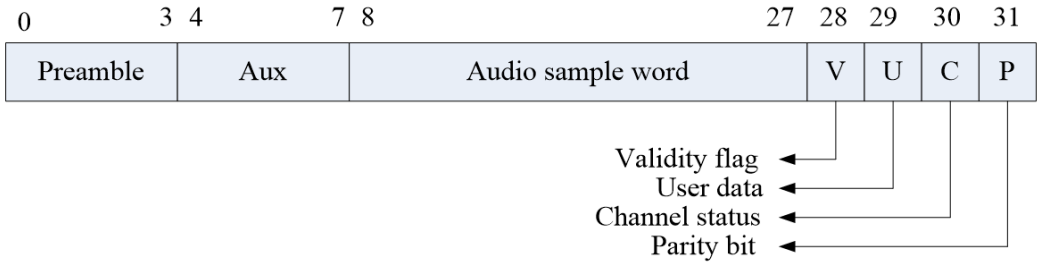

Fig.27-3 SPDIF_RX Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8. Time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to

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7 are designated auxiliary sample bits.
If the source provides fewer bits than the interface allows (either 24 or 20), the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

27.3.3 Channel Coding

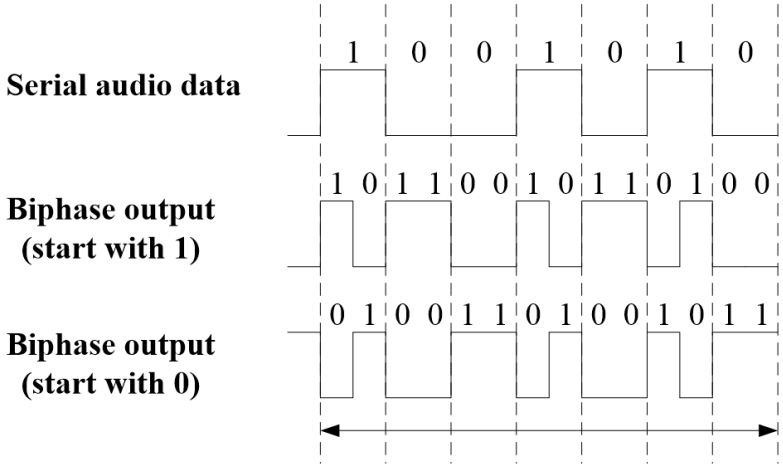

Fig.27-4 SPDIF_RX Channel Coding

To minimize the direct current component on the transmission/receiving line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.
Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'.However, it is different from the first if the bit is logical '1'.

27.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.
To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.
A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

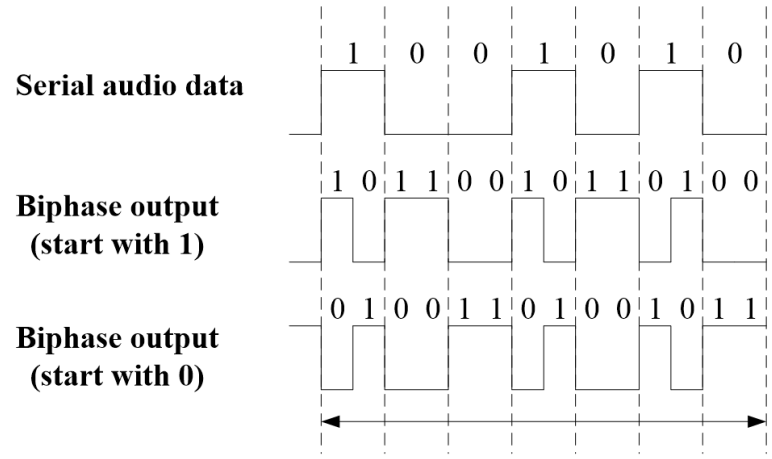

Fig.27-5 SPDIF_RX Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

27.4 Register Description

27.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SPDIF_RX0	0x2A650000
SPDIF_RX1	0x2A660000
SPDIF_RX2	0x27D30000

27.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPDIF_RX_VERSION	0x0000	W	0x00000100	Version Register
SPDIF_RX_CFGR	0x0004	W	0x00000000	Transfer Configuration Register
SPDIF_RX_CLR	0x0008	W	0x00000000	Clear Register
SPDIF_RX_CDR	0x000C	W	0x000000A1	Clock And Data Recovery Register
SPDIF_RX_CDRST	0x0010	W	0x03FF00FF	Clock And Data Recovery Status Register
SPDIF_RX_DMACR	0x0014	W	0x00000000	DMA Control Register
SPDIF_RX_FIFOCTRL	0x0018	W	0x00000000	FIFO Control Register
SPDIF_RX_INTEN	0x001C	W	0x00000000	Interrupt Enable Register
SPDIF_RX_INTMASK	0x0020	W	0x00000000	Interrupt Mask Register
SPDIF_RX_INTSR	0x0024	W	0x00000000	Interrupt Status Register
SPDIF_RX_INTCLR	0x0028	W	0x00000000	Interrupt Clear Register
SPDIF_RX_SMPDR	0x002C	W	0x00000000	Sample Data Register
SPDIF_RX_USRDRn	0x0030	W	0x00000000	User Data Register n(n=0~11)
SPDIF_RX_CHNSRn	0x0060	W	0x00000000	Channel Status Register n(n=0~11)
SPDIF_RX_BURTSINFO	0x0100	W	0x00000000	Channel Burst Info Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

27.4.3 Detail Registers Description

SPDIF_RX_VERSION

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000100	VER Version of SPDIF_RX

SPDIF_RX_CFGR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	TWAD 1'b0: Only audio data transmitted to FIFO. 1'b1: Block start, channel number and VUCP transmitted with audio data to FIFO.
0	RW	0x0	EN 1'b0: Disable SPDIF_RX 1'b1: Enable SPDIF_RX

SPDIF_RX_CLR

Address: **Operational Base** + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	RXSC This is a software self-cleared bit. Write 1'b1 to clear all receive logic.

SPDIF_RX_CDR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	JITTRSH CDR jitter threshold. It is valid only when BYPASS is 1'b0.
23:16	RW	0x00	MIDRGE CDR jitter middle range. It is valid only when BYPASS is 1'b0.
15:11	RO	0x00	reserved
10:9	RO	0x0	CS CDR state 2'b00: Idle state. CDR is idle and waits for rising edge of SPDIF_RX input bitstream. 2'b01: Detect state 2'b10: Measurement state 2'b11: Synchronization state
8:7	RO	0x1	JITST CDR jitter status 2'b01: Low 2'b10: High 2'b11: Normal It is valid only when BYPASS is 1'b0.
6	RO	0x0	FULL CDR FIFO full status. 1'b0: Not full 1'b1: Full It is valid only when BYPASS is 1'b0.
5	RO	0x1	EMPTY CDR FIFO empty status. 1'b0: Not empty 1'b1: Empty It is valid only when BYPASS is 1'b0.
4:2	RW	0x0	AVGWIN Average the non-jitter recovered clk from bitstream at a period of AVGWIN time.
1	RW	0x0	AVGSEL Select if the min or average number of cycles from the calculation of SPDIF_RX input bitstream pulse width. 1'b0: Minimum number of cycles 1'b1: Average number of cycles, that is (max+min)/4.
0	RW	0x1	BYPASS Write 1'b1 to enable CDR non-jitter bypass mode. It's recommended that this bit set to 1'b1. Please ensure that this bit is set to 1'b1 before starting receiving data.

SPDIF_RX_CDRST

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x03ff	NOSTRTHR The threshold counter determines the latency between input bitstream idle and exit synchronous status. Make sure that this value is large than 16'h03ff.
15:8	RO	0x00	MAXCNT The value indicates the number of reference clock cycles to oversample the maximum pulse width of bitstream.
7:0	RO	0xff	MINCNT The value indicates the number of reference clock cycles to oversample the minimum pulse width of bitstream.

SPDIF_RX_DMACR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	RDE 1'b0: Receive DMA disabled. 1'b1: Receive DMA enabled.
4:0	RW	0x00	RDL This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1. That is, dma_rx_req is generated when the number of valid data entries in the sample date buffer is equal to or above this field value + 1.

SPDIF_RX_FIFOCTRL

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RO	0x00	RFL Contains the number of valid data entries in the receive FIFO.
7:5	RO	0x0	reserved
4:0	RW	0x00	RFT When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO full interrupt is triggered.

SPDIF_RX_INTEN

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	UBCIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if current user bit is different from previous one.
9	RW	0x0	ESYNCIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate when entering synchronous state.

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Bit	Attr	Reset Value	Description
8	RW	0x0	BTEIE 1'b0: Disable 1'b1: Enable When enabled, an interrupt will generate when the block receive is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM.
7	RW	0x0	NSYNCIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if CDR change from synchronization state to idle state.
6	RW	0x0	BMDEIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if a bi-phase mark decoding error has occurred.
5	RW	0x0	RXOIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if CDR FIFO is overrun.
4	RW	0x0	RXFIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if CDR FIFO is full.
3	RW	0x0	NPSPIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if non-liner PCM sync word is received.
2	RW	0x0	NVLDIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if validity bit received from bitstream is 1'b1.
1	RW	0x0	CSCIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if current channel status bit is different from previous one.
0	RW	0x0	PEIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if a parity error has occurred.

SPDIF_RX_INTMASK

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	UBCIMSK 1'b0: Unmask 1'b1: Mask

Bit	Attr	Reset Value	Description
9	RW	0x0	ESYNCIMSK 1'b0: Unmask 1'b1: Mask
8	RW	0x0	BTEIMSK 1'b0: Unmask 1'b1: Mask
7	RW	0x0	NSYNCIMSK 1'b0: Unmask 1'b1: Mask
6	RW	0x0	BMDEIMSK 1'b0: Unmask 1'b1: Mask
5	RW	0x0	RXOIMSK 1'b0: Unmask 1'b1: Mask
4	RW	0x0	RXFIMSK 1'b0: Unmask 1'b1: Mask
3	RW	0x0	NPSPIMSK 1'b0: Unmask 1'b1: Mask
2	RW	0x0	NVLDIMSK 1'b0: Unmask 1'b1: Mask
1	RW	0x0	CSCIMSK 1'b0: Unmask 1'b1: Mask
0	RW	0x0	PEIMSK 1'b0: Unmask 1'b1: Mask

SPDIF_RX_INTSR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RO	0x0	UBCISR 1'b0: Inactive 1'b1: Active
9	RO	0x0	ESYNCISR 1'b0: Inactive 1'b1: Active
8	RO	0x0	BTEISR 1'b0: Inactive 1'b1: Active
7	RO	0x0	NSYNCISR 1'b0: Inactive 1'b1: Active
6	RO	0x0	BMDEISR 1'b0: Inactive 1'b1: Active
5	RO	0x0	RXOIS 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
4	RO	0x0	RXFIS 1'b0: Inactive 1'b1: Active
3	RO	0x0	NPSPIS 1'b0: Inactive 1'b1: Active
2	RO	0x0	NVLDIS 1'b0: Inactive 1'b1: Active
1	RO	0x0	CSCIS 1'b0: Inactive 1'b1: Active
0	RO	0x0	PEIS 1'b0: Inactive 1'b1: Active

SPDIF_RX_INTCLR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	UBCICLR Write 1'b1 to clear user bit change interrupt.
9	RW	0x0	ESYNCICLR Write 1'b1 to clear entering synchronous state interrupt.
8	RW	0x0	BTEICLR Write 1'b1 to clear block transfer/repetition period end interrupt.
7	RW	0x0	NSYNCICLR Write 1'b1 to clear CDR not synchronization interrupt.
6	RW	0x0	BMDEICLR Write 1'b1 to clear bi-phase mark decoding interrupt.
5	RW	0x0	RXOICLR Write 1'b1 to clear receive overrun interrupt.
4	RW	0x0	RXFICLR Write 1'b1 to clear receive full interrupt.
3	RW	0x0	NPSPICLR Write 1'b1 to clear non-liner PCM sync word received interrupt.
2	RW	0x0	NVLDICLR Write 1'b1 to clear validity bit received interrupt.
1	RW	0x0	CSCICLR Write 1'b1 to clear channel status change interrupt.
0	RW	0x0	PEICLR Write 1'b1 to clear parity error interrupt.

SPDIF_RX_SMPDR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	SMPDR Sample Data Register

SPDIF_RX_USRDRn

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	USR_SUB_1 User data bit for subframe 1

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	USR_SUB_0 User data bit for subframe 0

SPDIF_RX_CHNSRn

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CHNSR_SUB_1 Channel status bit for subframe 1
15:0	RO	0x0000	CHNSR_SUB_0 Channel status bit for subframe 0

SPDIF_RX_BURTSINFO

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PD Preamble Pd for non-linear PCM, indicating the length of burst payload in unit of bytes or bits.
15:13	RW	0x0	BSNUM This field indicates the bitstream number. Usually the bitstream number is 0.
12:8	RO	0x00	DATAINFO This field gives the data-type-dependent info.
7	RO	0x0	ERRFLAG 1'b0: Indicates a valid burst-payload. 1'b1: Indicates that the burst-payload may contain errors.

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Bit	Attr	Reset Value	Description
6:0	RO	0x00	DATATYPE 7'b0000000: Null data 7'b0000001: AC-3 data 7'b0000011: Pause data 7'b0000100: MPEG-1 layer 1 data 7'b0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 7'b0000110: MPEG-2 data with extension 7'b0000111: MPEG-2 AAC 7'b0001000: MPEG-2, layer-1 low sampling frequency 7'b0001001: MPEG-2, layer-2 low sampling frequency 7'b0001010: MPEG-2, layer-3 low sampling frequency 7'b0001011: DTS type I 7'b0001100: DTS type II 7'b0001101: DTS type III 7'b0001110: ATRAC 7'b0001111: ATRAC 2/3 7'b0010000: ATRAC-X 7'b0010001: DTS type IV 7'b0010010: WMA professional type I 7'b0110010: WMA professional type II 7'b1010010: WMA professional type III 7'b1110010: WMA professional type IV 7'b0010011: MPEG-2 AAC low sampling frequency 7'b0110011: MPEG-2 AAC low sampling frequency 7'b1010011: MPEG-2 AAC low sampling frequency 7'b1110011: MPEG-2 AAC low sampling frequency 7'b0010100: MPEG-4 AAC 7'b0110100: MPEG-4 AAC 7'b1010100: MPEG-4 AAC 7'b1110100: MPEG-4 AAC 7'b0010101: Enhanced AC-3 7'b0010110: MAT Others: Reserved

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Bit	Attr	Reset Value	Description
6:0	RO	0x00	DATATYPE 7'b0000000: Null data 7'b0000001: AC-3 data 7'b0000011: Pause data 7'b0000100: MPEG-1 layer 1 data 7'b0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 7'b0000110: MPEG-2 data with extension 7'b0000111: MPEG-2 AAC 7'b0001000: MPEG-2, layer-1 low sampling frequency 7'b0001001: MPEG-2, layer-2 low sampling frequency 7'b0001010: MPEG-2, layer-3 low sampling frequency 7'b0001011: DTS type I 7'b0001100: DTS type II 7'b0001101: DTS type III 7'b0001110: ATRAC 7'b0001111: ATRAC 2/3 7'b0010000: ATRAC-X 7'b0010001: DTS type IV 7'b0010010: WMA professional type I 7'b0110010: WMA professional type II 7'b1010010: WMA professional type III 7'b1110010: WMA professional type IV 7'b0010011: MPEG-2 AAC low sampling frequency 7'b0110011: MPEG-2 AAC low sampling frequency 7'b1010011: MPEG-2 AAC low sampling frequency 7'b1110011: MPEG-2 AAC low sampling frequency 7'b0010100: MPEG-4 AAC 7'b0110100: MPEG-4 AAC 7'b1010100: MPEG-4 AAC 7'b1110100: MPEG-4 AAC 7'b0010101: Enhanced AC-3 7'b0010110: MAT Others: Reserved

27.5 Interface Description

Table 27-2 SPDIF_RX0 m0 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdi	O	SPDIF_RX0_M0/FLEXBUS0_CSN_M4/UART2_RX_M1/I2C3_SDA_M0/CAN1_RX_M2/GPIO4_B4_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4’ h1

Table 27-3 SPDIF_RX0 m1 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdi	O	SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4’ h2

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Table 27-4 SPDIF_RX0 m2 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdi	O	CAM_CLK1_OUT_M1/ETH_CLK1_25M_OUT_M0/ETH0_MCLK_M1/SAI3_MCLK_M2/SPDIF_RX0_M2/UART9_RTSN_M0/I3C1_SDA_PU_M0/PWM2_CH6_M2/GPIO2_D6_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[11:8]=4'h5

Table 27-5 SPDIF_RX1 m0 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdi	O	VO_LCDC_D15/VO_EBC_SDDO15/ETH0_TXD1_M0/SPDIF_RX1_M0/DSMC_DATA9/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[3:0]=4'h4

Table 27-6 SPDIF_RX1 m1 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdi	O	VI_CIF_CLKO/ETH1_PPSCLK_M0/ETH0_RXCTL_M1/SAI3_SDO_M2/SPDIF_RX1_M1/UART3_CTSN_M0/SPI3_MISO_M0/CAN1_TX_M3/MIPI_TE_M1/GPIO3_A2_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'h5

Table 27-7 SPDIF_RX1 m2 Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdi	O	ETH1_MCLK_M1/SAI2_MCLK_M0/PDM0_SDI3_M2/SPDIF_RX1_M2/UART10_RTSN_M1/I2C5_SCL_M1/GPIO1_D4_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[3:0]=4'h6

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27.6 Application Notes

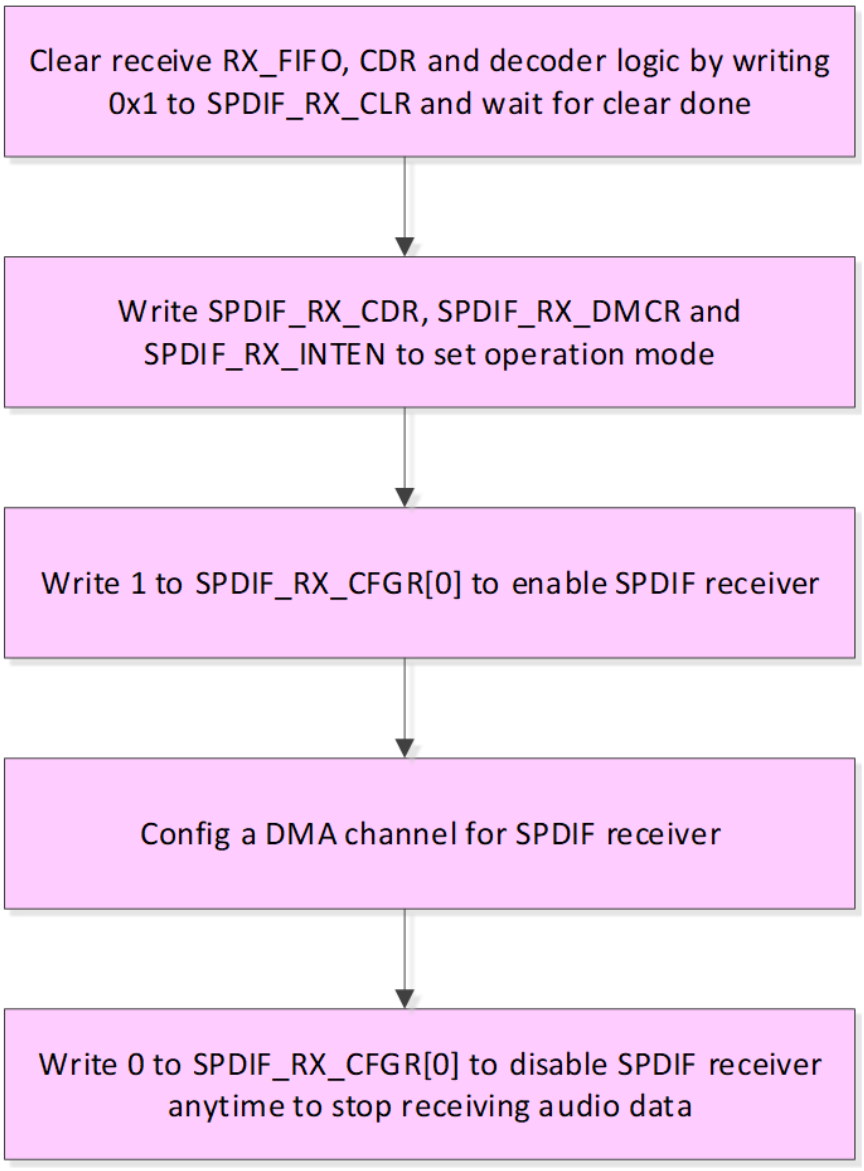

Fig.27-6 SPDIF_RX operation flow chart

The above figure shows the operation flow of SPDIF_RX operation.

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Chapter 28 Asynchronous Sample Rate Converter (ASRC)

28.1 Overview

ASRC converts digital audio data from one sample frequency to another. The input and output sample frequencies can be an arbitrary fraction of one another or the same frequency, but based on different clocks.
ASRC fetches audio data through AHB bus and acts as an intermediary for the audio devices such as SAI, PDM, SPDIF, etc.
With the ASRC controller, we can also connect audio devices and the embedded SOC platform together and provide an audio interface solution for the system.

28.1.1 Features

- Support one 32-bit AHB-Lite bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support up to 8 channels with the same ratio, which can be defined into 2/4/6/8
- Support sample rate and resample rate range from 8 to 384KHz, typical rate
  @8KHz, 16KHz, 32KHz, 64KHz, 128KHz
  @12KHz, 24KHz, 48KHz, 96KHz, 192KHz, 384KHz
  @11.025KHz, 22.05KHz, 44.1KHz, 88.2KHz, 176.4KHz, 352.8KHz
- Support up-conversion, down-conversion, and 1:1 asynchronous conversion
- Support conversion ratio ranging from 1:8 (down) to 8:1 (up) with 22-bit resolution
- Low deterministic latency related to ratio
- THD+N: -120dB
- Support real-time transmission mode, which transmit or receive audio data from either devices or memory with ratio track
- Support memory fetch mode with manual ratio without track
- Support input/output 16/20/24 bits wide audio data transfer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support audio data left or right justified in 32-bit wide FIFO
- Support half channels internal 48-bit wide and 16-location deep FIFOs for transmitting, and half channels 48-bit wide and 32-location deep FIFOs for receiving audio data
- Support fix and incremental address access to transmit and receive FIFOs
- Support ratio_init_done, ratio_update_done, asrc_out_start, conv_done, conv_error, fifo_in_empty, fifo_in_full, fifo_out_empty, fifo_out_full, ratio_unlock, src_lrck_unlock, dst_lrck_unlock interrupt and all interrupts can be masked
- Support combined interrupt output

28.2 Block Diagram

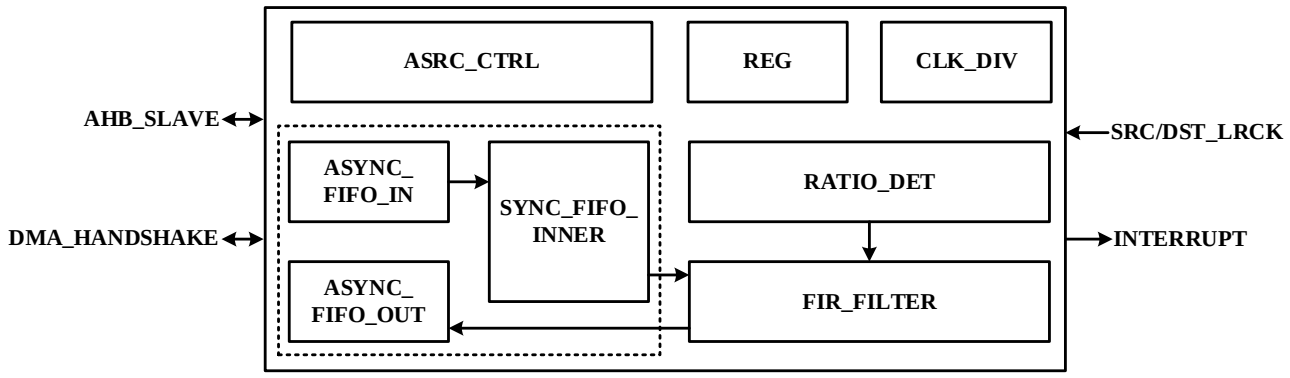

Fig. 28-1 ASRC Block Diagram

System Interface
The system interface implements the interactions with SOC platform. It contains not only AHB slave operation which controls registers and audio data transfer, but also interrupt and DMA handshaking interface.
Clock Divider Block (CLK_DIV)
The Clock Divider implements clock frequency divider function. The source clock of this module are src_lrck and dst_lrck, and by the divider, it generates clocks with the same

frequency as sample rate or resample rate.

Register Block (REG)

The Register is responsible for the main ASRC functionality including control, status and interrupt generation.

Controller Block (ASRC_CTRL)

The Controller is the main control block of variable sampling filter, its main functions include filtering output judgment, coefficient position calculation and interpolation filtering.

Ratio Detector Block (RATIO_DET)

The main function of Ratio Detector is to initialize and track ratio related parameters. In the initialization stage, the related parameters is fetched from register configuration. And in the tracking stage, the ratio tracking is realized through the periodic detection of src_lrck and dst_lrck. At the same time, the waterline of output FIFO is monitored for negative feedback adjustment.

FIR Filter Block (FIR_FILTER)

The FIR Filter acts as a poly-phase filter, which interpolates the correct phase and applies the calculated filter coefficients to the set of input samples to form an output sample.

Inner FIFO Block (SYNC_FIFO_INNER)

The Inner FIFO is the buffer to store audio data for FIR Filter. The size of the FIFO is 48bits x 512, and the number of the FIFO is half channels.

Input FIFO Block (ASYNC_FIFO_IN)

The Input FIFO is the buffer to store received audio data. The size of the FIFO is 48bits x 16, and the number of the FIFO is half channels.

Output FIFO Block (ASYNC_FIFO_OUT)

The Output FIFO is the buffer to store transmitted audio data. The size of the FIFO is 48bits x 32, and the number of the FIFO is half channels.

28.3 Function Description

In the ASRC controller, there are two main modes: memory fetch mode and real-time transmission mode.

28.3.1 Memory fetch mode

In memory fetch mode, the converter is based on manual ratio, ratio tracking is disabled, so src_lrck or dst_lrck is unused. ASRC acts as device when transmitting or receiving audio data from system memory, so both dma_tx_req and dma_rx_req are started by ASRC. The faster the frequency of working clock, the faster the conversion will be completed.

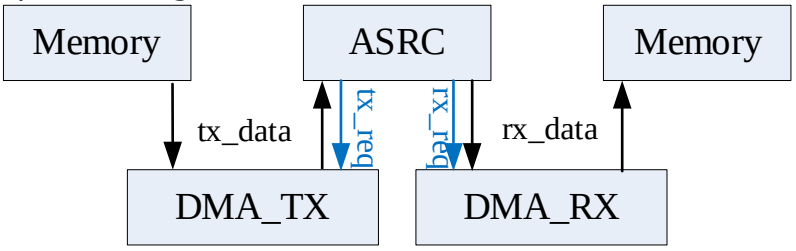

Fig. 28-2 ASRC memory fetch mode structure

Based on memory fetch mode, we extends a new sub-patterns called loop mode. With loop mode, multiple discrete audio files can be converted by one configuration, or one continuous audio files can be split into multiple parts and converted by one configuration. The most significant application is to convert more channel real-time audio data than ASRC defined by time division multiplexing. Audio data at both ends of file should be recalled additionally for continuous output.

28.3.2 Real-time transmission mode

In real-time transmission mode, the converter is based on manual ratio and track ratio, ratio tracking is enabled, so src_lrck or dst_lrck is used. The faster the frequency of working clock, the more precise the tracking will be completed. It can be divided into four sub-patterns based on the device types at the source and destination ends, called MEM2MEM, MEM2DST, SRC2MEM and SRC2DST for short.

- MEM2MEM

Memory serves as both source device and destination device. ASRC acts as device when

transmitting or receiving audio data from memory, so both dma_tx_req and dma_rx_req are started by ASRC. Both src_lrck and dst_lrck originate from CRU.

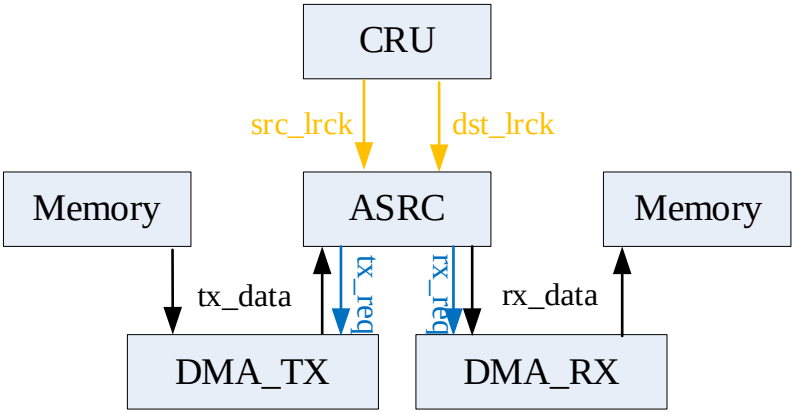

Fig. 28-3 ASRC MEM2MEM mode structure

- MEM2DST

Memory serves as source device, and peripheral serves as destination device. ASRC acts as device when receiving audio data from memory, so dma_tx_req is started by ASRC, and dma_rx_req is started by peripheral. src_lrck originates from CRU, and dst_lrck originates from peripheral.

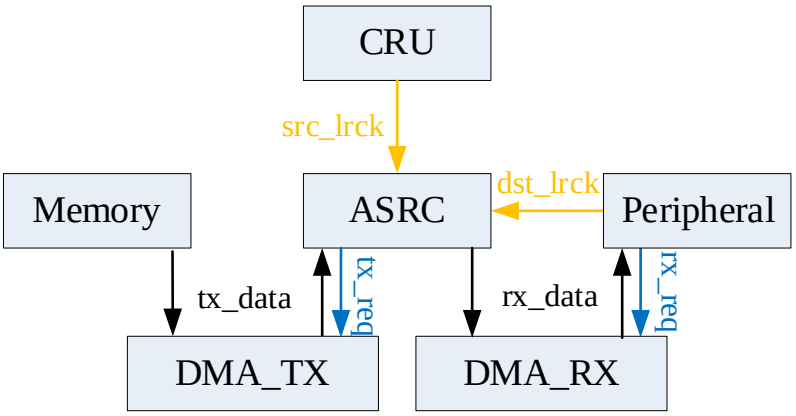

Fig. 28-4 ASRC MEM2DST mode structure

- SRC2MEM

Peripheral serves as source device, and memory serves as destination device. ASRC acts as device when transmitting audio data to memory, so dma_tx_req is started by peripheral, and dma_tx_req is started by ASRC. src_lrck originates from device, and dst_lrck originates from CRU.

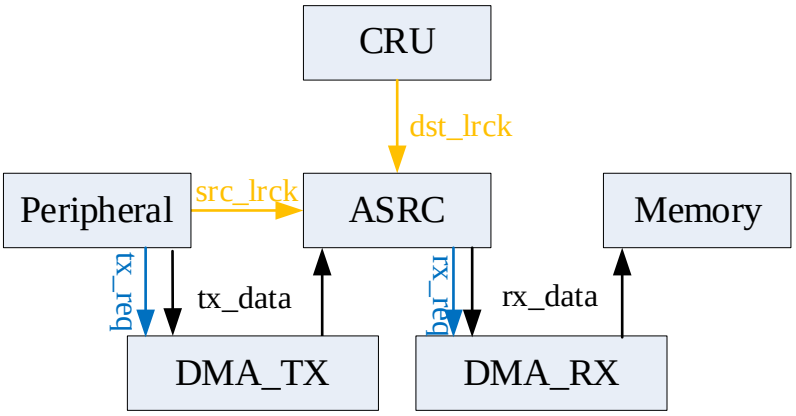

Fig. 28-5 ASRC SRC2MEM mode structure

- SRC2DST

Peripheral serves as both source device and destination device. ASRC acts as memory when transmitting or receiving audio data from memory, so both dma_tx_req and dma_rx_req are started by peripheral. Both src_lrck and dst_lrck originate from peripheral.

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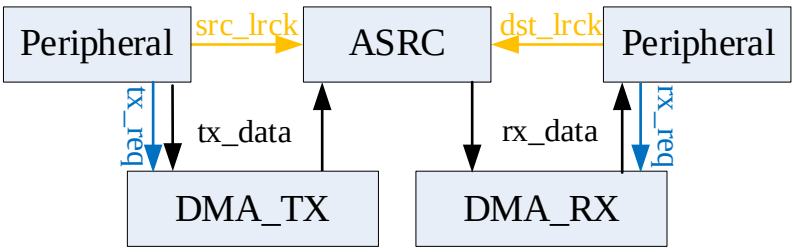

Fig. 28-6 ASRC SRC2DST mode structure

28.4 Register Description

28.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
ASRC4CH0	0x2A690000
ASRC4CH1	0x2A6A0000
ASRC2CH0	0x2A6B0000
ASRC2CH1	0x2A6C0000

28.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
ASRC_VERSION	0x0000	W	0x00000001	Version register
ASRC_ASRC_CON	0x0004	W	0x00200030	ASRC control register
ASRC_CLKDIV_CON	0x0008	W	0x00000000	LRCK divider control register
ASRC_DATA_FMT	0x000C	W	0x00000000	Data format register
ASRC_LOOP_CON0	0x0010	W	0x00000000	Loop control register 0
ASRC_LOOP_CON1	0x0014	W	0x00000000	Loop control register 1
ASRC_LOOP_CON2	0x0018	W	0x00000000	Loop control register 2
ASRC_MANUAL_RATIO	0x0020	W	0x00000000	Manual ratio register
ASRC_SAMPLE_RATE	0x0024	W	0x0002EE00	Sample rate register
ASRC_RESAMPLE_RATE	0x0028	W	0x0002EE00	Resample rate register
ASRC_TRACK_PERIOD	0x002C	W	0x000003FF	ASRC track period register
ASRC_RATIO_MARGIN	0x0030	W	0x003FFFFF	Ratio margin register
ASRC_LRCK_MARGIN	0x0034	W	0x00001F1F	LRCK margin register
ASRC_FETCH_LEN	0x0040	W	0x00000000	Fetch length register
ASRC_DMA_THRESH	0x0050	W	0x7030B333	DMA thresh register
ASRC_INT_CON	0x0060	W	0x00000000	Interrupt control register
ASRC_INT_ST	0x0064	W	0x00000000	Interrupt status register
ASRC_ASRC_ST	0x0070	W	0x00000000	ASRC status register
ASRC_RATIO_ST	0x0080	W	0x00000000	Ratio status register
ASRC_RESAMPLE_RATE_ST	0x0084	W	0x00000000	Resample rate status register
ASRC_THETA_CNT_ST	0x0090	W	0x00000000	Theta counter status register
ASRC_DECI_THETA_ACC_ST	0x0094	W	0x00000000	Decimal theta accumulator status register
ASRC_FIFO_IN_WRCNT	0x00A0	W	0x00000000	Input FIFO write counter register
ASRC_FIFO_IN_RDCNT	0x00A4	W	0x00000000	Input FIFO read counter register
ASRC_FIFO_OUT_WRCNT	0x00B0	W	0x00000000	Output FIFO write counter register
ASRC_FIFO_OUT_RDCNT	0x00B4	W	0x00000000	Output FIFO read counter register
ASRC_FIFO_IN_FIXED_DR	0x00C0	W	0x00000000	Input FIFO fixed address data register
ASRC_FIFO_OUT_FIXED_DR	0x00C4	W	0x00000000	Output FIFO fixed address data register

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Name	Offset	Size	Reset Value	Description
ASRC_FIFO_IN_INCR_DR	0x1000	W	0x00000000	Input FIFO increment address data register
ASRC_FIFO_OUT_INCR_DR	0x5000	W	0x00000000	Output FIFO increment address data register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

28.4.3 Detail Registers Description

ASRC_VERSION

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000001	version ASRC version number.

ASRC_ASRC_CON

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:20	RW	0x2	ratio_filt_win Ratio filter sliding window select. 2'b00: Window width 2 2'b01: Window width 4 2'b10: Window width 8 2'b11: Window width 16
19	RW	0x0	ratio_track_mode Ratio track mode select. 1'b0: Update src_lrck_cnt and dst_lrck_cnt once track period reached 1'b1: Update src_lrck_cnt and dst_lrck_cnt only when the value change by more than one from the previous value
18	RW	0x0	ratio_exc_dis Ratio exceed detect disable. This bit works only when ratio_track_dis equal 0. 1'b0: Disable 1'b1: Enable
17	RW	0x0	ratio_filt_dis Ratio track filter disable. This bit works only when ratio_track_dis equal 0. 1'b0: Disable 1'b1: Enable
16	RW	0x0	ratio_track_dis Ratio track disable. 1'b0: Disable 1'b1: Enable
15:10	RO	0x00	reserved
9	RW	0x0	asrc_out_stop ASRC stop sending data to destination device. This bit works only when asrc_mode equal 0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	asrc_in_stop ASRC stop receiving data from source device. This bit works only when asrc_mode equal 0. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5:4	RW	0x3	chan_num Channel number select. 2'b00: 2 channel used 2'b01: 4 channel used 2'b10: 6 channel used 2'b11: 8 channel used
3:2	RW	0x0	real_time_mode Real-time transmission mode select. This bit works only when asrc_mode equal 0. 2'b00: Memory as source device, Memory as destination device 2'b01: Peripheral as source device, Memory as destination device 2'b10: Memory as source device, Peripheral as destination device 2'b11: Peripheral as source device, Peripheral as destination device
1	RW	0x0	asrc_mode ASRC mode select. 1'b0: Real-time transmission mode 1'b1: Memory fetch mode
0	RW	0x0	asrc_en ASRC enable. 1'b0: Disable 1'b1: Enable In loop mode, this bit must be set after loop_en. When asrc_en equal 0, FIFO buffers in ASRC are self-cleared.

ASRC_CLKDIV_CON

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	dst_lrck_div_en dst_lrck divider enable. 1'b0: Disable 1'b1: Enable
30:16	RW	0x0000	dst_lrck_div_con dst_lrck divider. dst_lrck_div_con=Fdst_lrck/resample_rate-1.
15	RW	0x0	src_lrck_div_en src_lrck divider enable. 1'b0: Disable 1'b1: Enable
14:0	RW	0x0000	src_lrck_div_con src_lrck divider. src_lrck_div_con=Fsrc_lrck/sample_rate-1.

ASRC_DATA_FMT

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	OSJM Output serial port data store justified mode, which indicate LSB of output data.
23:21	RO	0x0	reserved
20:16	RW	0x00	ISJM Input serial port data store justified mode, which indicate LSB of input data.
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	OFMT Output serial port data format. 1'b0: Low bits data valid to AHB bus, high bits data invalid. 1'b1: 32 bit data valid to AHB bus. Low 16 bit for left channel and high 16 bit for right channel.
11:9	RO	0x0	reserved
8	RW	0x0	IFMT Input serial port data format. 1'b0: Low bits data valid from AHB bus, high bits data invalid. 1'b1: 32 bit data valid from AHB bus. Low 16 bit for left channel and high 16 bit for right channel.
7:6	RO	0x0	reserved
5:4	RW	0x0	OWL Output serial port data word length. 2'b00: 24 bits 2'b01: 20 bits 2'b10: 16 bits 2'b01: Reserved
3:2	RO	0x0	reserved
1:0	RW	0x0	IWL Input serial port data word length. 2'b00: 24 bits 2'b01: 20 bits 2'b10: 16 bits 2'b01: Reserved

ASRC_LOOP_CON0

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	loop_end_con Loop end mode. Each loop is controlled independently, bit 0~7 is corresponding to loop time 0~7. 1'b0: Convert the end part of a file 1'b1: Not convert the end part of a file
7:0	R/WSC	0x00	loop_start_con Loop start mode. Each loop is controlled independently, bit 0~7 is corresponding to loop time 0~7. 1'b0: Convert the start part of a file 1'b1: Not convert the start part of a file

ASRC_LOOP_CON1

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	chan_times Channel times, which means the actual channel to be converted is (chan_times+1) much as (chan_num+1).
7	RO	0x0	reserved
6:4	RW	0x0	loop_times Loop times, which means (loop_times+1) conversion is done continuously.
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	R/WSC	0x0	loop_en ASRC loop enable. This bit is automatically cleared when loop conversion done. 1'b0: Disable 1'b1: Enable

ASRC_LOOP_CON2

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	R/WSC	0x0000	loop_gap_thresh ASRC loop gap thresh, which set gap counter between two conversion.

ASRC_MANUAL_RATIO

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	manual_ratio Manual ratio with fixed-point 26Q22. High 4 bits shows integer part, low 22 bits shows decimal part. manual_ratio=sample_rate/resample_rate.

ASRC_SAMPLE_RATE

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x2ee00	sample_rate Sample rate range from 8KHz to 384KHz.

ASRC_RESAMPLE_RATE

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x2ee00	resample_rate Resample rate range from 8KHz to 384KHz.

ASRC_TRACK_PERIOD

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ratio_track_div Ratio track divider, which scale down the frequency of src_lrck and dst_lrck for higher precision of ratio tracking.
15:12	RO	0x0	reserved
11:0	RW	0x3ff	ratio_track_period Ratio track period, which means track information updates every (ratio_track_period+1)*(ratio_track_div+1) clock.

ASRC_RATIO_MARGIN

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x3fffff	ratio_margin Ratio margin with fixed-point 22Q22, which shows decimal part of ratio. Ratio unlock occurs when the difference between calc_ratio and manual_ratio exceeds ratio_margin.

ASRC_LRCK_MARGIN

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	dst_lrck_margin_dis Destination clock drift detect disable. 1'b0: Disable 1'b1: Enable
14:13	RO	0x0	reserved
12:8	RW	0x1f	dst_lrck_margin Destination clock drift margin. Dst_lrck unlock occurs when the variation of dst_lrck exceeds dst_lrck_margin.
7	RW	0x0	src_lrck_margin_dis Source clock drift detect disable. 1'b0: Disable 1'b1: Enable
6:5	RO	0x0	reserved
4:0	RW	0x1f	src_lrck_margin Source clock drift margin. Src_lrck unlock occurs when the variation of src_lrck exceeds src_lrck_margin.

ASRC_FETCH_LEN

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	fetch_length Memory fetch length, is used only when asrc_mode equal 1. It indicates the number of input data per channel. As data is written by AHB bus in word, the equation is as follows: fetch_length=INPUT_WORD_NUM*(IFMT+1)/(2*(chan_num+1))

ASRC_DMA_THRESH

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:26	RW	0x1c	asrc_pos_thresh Output FIFO positive thresh, unit channel_num. Exceed postive occurs once the number of valid data entries in the output FIFO is above this field value. Asrc_pos_thresh ought to be higher than 28.
25	RO	0x0	reserved
24:20	RW	0x03	asrc_neg_thresh Output FIFO negative thresh, unit channel_num. Exceed negative occurs once the number of valid data entries in the output FIFO is below this field value. Asrc_neg_thresh ought to be lower than 3.
19:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16:12	RW	0x0b	asrc_out_thresh ASRC start output thresh, unit channel_num. Output will start once the number of valid data entries in the output FIFO is above this field value. Asrc_out_thresh ought to be higher than dma_rx_thresh.
11:8	RW	0x3	asrc_in_thresh ASRC start thresh, unit channel_num. Conversion will start once the number of valid data entries in the input FIFO is above this field value. Asrc_in_thresh ought to be equal or lower than dma_tx_thresh.
7:4	RW	0x3	dma_rx_thresh DMA rx request thresh, unit channel_num. The watermark level = dma_rx_thresh+1; that is, dma_rx_req is generated when the number of valid data entries in the output FIFO is equal to or above this field value + 1.
3:0	RW	0x3	dma_tx_thresh DMA tx request thresh, unit channel_num. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the input FIFO is equal to or below this field value.

ASRC_INT_CON

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	dst_lrck_unlock_en Enable dst_lrck unlock interrupt. 1'b0: Disable 1'b1: Enable
11	RW	0x0	src_lrck_unlock_en Enable src_lrck unlock interrupt. 1'b0: Disable 1'b1: Enable
10	RW	0x0	ratio_unlock_en Enable ratio unlock interrupt. 1'b0: Disable 1'b1: Enable
9	RW	0x0	fifo_out_empty_en Enable output FIFO empty interrupt. 1'b0: Disable 1'b1: Enable
8	RW	0x0	fifo_out_full_en Enable output FIFO full interrupt. 1'b0: Disable 1'b1: Enable
7	RW	0x0	fifo_in_empty_en Enable input FIFO empty interrupt. 1'b0: Disable 1'b1: Enable
6	RW	0x0	fifo_in_full_en Enable input FIFO full interrupt. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	ratio_update_done_en Enable ratio update done interrupt. 1'b0: Disable 1'b1: Enable
4	RW	0x0	ratio_change_done_en Enable ratio change done interrupt. 1'b0: Disable 1'b1: Enable
3	RW	0x0	ratio_init_done_en Enable ratio init done interrupt. 1'b0: Disable 1'b1: Enable
2	RW	0x0	conv_error_en Enable conversion error interrupt. 1'b0: Disable 1'b1: Enable
1	RW	0x0	conv_done_en Enable conversion done interrupt. 1'b0: Disable 1'b1: Enable
0	RW	0x0	asrc_out_start_en Enable asrc output start interrupt. 1'b0: Disable 1'b1: Enable

ASRC_INT_ST

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	dst_lrck_unlock_st dst_lrck unlock interrupt status. Level interrupt which can be clear by mask dst_lrck_unlock_en of INT_CON.
11	RO	0x0	src_lrck_unlock_st src_lrck unlock interrupt status. Level interrupt which can be clear by mask src_lrck_unlock_en of INT_CON.
10	RO	0x0	ratio_unlock_st Ratio unlock interrupt status. Level interrupt which can be clear by mask ratio_unlock_en of INT_CON.
9	W1C	0x0	fifo_out_empty_st Output FIFO empty interrupt status.
8	W1C	0x0	fifo_out_full_st Output FIFO full interrupt status.
7	W1C	0x0	fifo_in_empty_st Input FIFO empty interrupt status.
6	W1C	0x0	fifo_in_full_st Input FIFO full interrupt status.
5	W1C	0x0	ratio_update_done_st Ratio update interrupt status.
4	W1C	0x0	ratio_change_done_st Ratio change interrupt status.

Bit	Attr	Reset Value	Description
3	RO	0x0	ratio_init_done_st Ratio init done interrupt status. Level interrupt which can be clear by mask ratio_init_done_en of INT_CON.
2	W1C	0x0	conv_error_st Conversion error interrupt status.
1	RO	0x0	conv_done_st Conversion done interrupt status. Level interrupt which can be clear by mask conv_done_en of INT_CON.
0	RO	0x0	asrc_out_start_st ASRC output start interrupt status. Level interrupt which can be clear by mask asrc_out_start_en of INT_CON.

ASRC_ASRC_ST

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RO	0x0	ratio_state Ratio track state. 2'h0: IDLE 2'h1: RATIO_INIT 2'h2: RATIO_TRACK 2'h3: RATIO_STOP
28	RO	0x0	exceed_pos Output FIFO positive exceed status.
27	RO	0x0	exceed_neg Output FIFO negative exceed status.
26:22	RO	0x00	pos_thresh Output FIFO positive thresh status, unit channel_num.
21:17	RO	0x00	neg_thresh Output FIFO negative thresh status, unit channel_num.
16:12	RO	0x00	fifo_out_level Output FIFO level, contains the number of valid data entries in the receive FIFO, unit channel_num.
11:8	RO	0x0	fifo_in_level Input FIFO level, contains the number of valid data entries in the transmit FIFO, unit channel_num.
7	RO	0x0	dma_rx_ack DMA rx acknowledge status.
6	RO	0x0	dma_rx_req DMA rx request status.
5	RO	0x0	dma_tx_ack DMA tx acknowledge status.
4	RO	0x0	dma_tx_req DMA tx request status.
3	RO	0x0	reserved
2	RO	0x0	filt_delay_done ASRC filter delay done status.
1	RO	0x0	asrc_out_start ASRC out start status.
0	RO	0x0	asrc_in_start ASRC in start status.

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ASRC_RATIO_ST

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RO	0x0000000	ratio_st Calculate ratio with fixed-point 26Q22. High 4 bits shows integer part, low 22 bits shows decimal part.

ASRC_RESAMPLE_RATE_ST

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	resample_rate_st Calculate resample rate status.

ASRC_THETA_CNT_ST

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RO	0x0000000	theta_cnt_st Theta counter status.

ASRC_DECI_THETA_ACC_ST

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	deci_theta_acc_st Decimal theta accumulator status.

ASRC_FIFO_IN_WRCNT

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_in_wrcnt Input FIFO write counter status, unit channel_num.

ASRC_FIFO_IN_RDCNT

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_in_rdcnt Input FIFO read counter status, unit channel_num.

ASRC_FIFO_OUT_WRCNT

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_out_wrcnt Output FIFO write counter status, unit channel_num.

ASRC_FIFO_OUT_RDCNT

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_out_rdcnt Output FIFO read counter status, unit channel_num.

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ASRC_FIFO_IN_FIXED_DR

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_in_data Input FIFO fixed address data register.

ASRC_FIFO_OUT_FIXED_DR

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fifo_out_data Output FIFO fixed address data register.

ASRC_FIFO_IN_INCR_DR

Address: **Operational Base** + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_in_data Input FIFO increment address data register, which range from 0x1000 to 0x4FFF.

ASRC_FIFO_OUT_INCR_DR

Address: **Operational Base** + offset (0x5000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fifo_out_data Output FIFO increment address data register, which range from 0x5000 to x8FFF.

28.5 Application Notes

28.5.1 LRCK multiplexing selector

There are src_lrck and dst_lrck interface which source from audio device or CRU. In real-time transmission mode, the multiplexing selector shown as follow need to be set.

Table 28-1 ASRC4ch0 src_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
SYS_GRF_SOC_CON9	4:0	5'd0: SAI0 5'd1: SAI1 5'd2: SAI2 5'd3: SAI3 5'd4: SAI4 5'd5: SAI5 5'd6: SAI6 5'd7: SAI7 5'd8: SAI8 5'd9: SAI9 5'd10: PDM0 5'd11: PDM1 5'd12: SPDIF_RX0 5'd13: SPDIF_RX1 5'd14: SPDIF_RX2 5'd15: lclk_asrc_src_0 5'd16: lclk_asrc_src_1

Table 28-2 ASRC4ch0 dst_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
SYS_GRF_SOC_CON9	9:5	5'd0: SAI0 5'd1: SAI1

Register Name	MUX Setting	LRCK Source Select
		5'd2: SAI2 5'd3: SAI3 5'd4: SAI4 5'd5: SAI5 5'd6: SAI6 5'd7: SAI7 5'd8: SAI8 5'd9: SAI9 5'd10: SPDIF_TX0 5'd11: SPDIF_TX1 5'd12: SPDIF_TX2 5'd13: SPDIF_TX3 5'd14: SPDIF_TX4 5'd15: SPDIF_TX5 5'd16: lclk_asrc_src_0 5'd17: lclk_asrc_src_1

Table 28-3 ASRC4ch1 src_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
SYS_GRF_SOC_CON9	14:10	5'd0: SAI0 5'd1: SAI1 5'd2: SAI2 5'd3: SAI3 5'd4: SAI4 5'd5: SAI5 5'd6: SAI6 5'd7: SAI7 5'd8: SAI8 5'd9: SAI9 5'd10: PDM0 5'd11: PDM1 5'd12: SPDIF_RX0 5'd13: SPDIF_RX1 5'd14: SPDIF_RX2 5'd15: lclk_asrc_src_0 5'd16: lclk_asrc_src_1

Table 28-4 ASRC4ch1 dst_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
SYS_GRF_SOC_CON10	4:0	5'd0: SAI0 5'd1: SAI1 5'd2: SAI2 5'd3: SAI3 5'd4: SAI4 5'd5: SAI5 5'd6: SAI6 5'd7: SAI7 5'd8: SAI8 5'd9: SAI9 5'd10: SPDIF_TX0 5'd11: SPDIF_TX1 5'd12: SPDIF_TX2 5'd13: SPDIF_TX3 5'd14: SPDIF_TX4 5'd15: SPDIF_TX5 5'd16: lclk_asrc_src_0 5'd17: lclk_asrc_src_1

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Table 28-5 ASRC2ch0 src_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
SYS_GRF_SOC_CON10	9:5	5'd0: SAI0 5'd1: SAI1 5'd2: SAI2 5'd3: SAI3 5'd4: SAI4 5'd5: SAI5 5'd6: SAI6 5'd7: SAI7 5'd8: SAI8 5'd9: SAI9 5'd10: PDM0 5'd11: PDM1 5'd12: SPDIF_RX0 5'd13: SPDIF_RX1 5'd14: SPDIF_RX2 5'd15: lclk_asrc_src_0 5'd16: lclk_asrc_src_1

Table 28-6 ASRC2ch0 dst_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
SYS_GRF_SOC_CON10	14:10	5'd0: SAI0 5'd1: SAI1 5'd2: SAI2 5'd3: SAI3 5'd4: SAI4 5'd5: SAI5 5'd6: SAI6 5'd7: SAI7 5'd8: SAI8 5'd9: SAI9 5'd10: SPDIF_TX0 5'd11: SPDIF_TX1 5'd12: SPDIF_TX2 5'd13: SPDIF_TX3 5'd14: SPDIF_TX4 5'd15: SPDIF_TX5 5'd16: lclk_asrc_src_0 5'd17: lclk_asrc_src_1

Table 28-7 ASRC2ch1 src_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
SYS_GRF_SOC_CON11	4:0	5'd0: SAI0 5'd1: SAI1 5'd2: SAI2 5'd3: SAI3 5'd4: SAI4 5'd5: SAI5 5'd6: SAI6 5'd7: SAI7 5'd8: SAI8 5'd9: SAI9 5'd10: PDM0 5'd11: PDM1 5'd12: SPDIF_RX0 5'd13: SPDIF_RX1

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Register Name	MUX Setting	LRCK Source Select
		5'd14: SPDIF_RX2 5'd15: lclk_asrc_src_0 5'd16: lclk_asrc_src_1

Table 28-8 ASRC2ch1 dst_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
SYS_GRF_SOC_CON12	9:5	5'd0: SAI0 5'd1: SAI1 5'd2: SAI2 5'd3: SAI3 5'd4: SAI4 5'd5: SAI5 5'd6: SAI6 5'd7: SAI7 5'd8: SAI8 5'd9: SAI9 5'd10: SPDIF_TX0 5'd11: SPDIF_TX1 5'd12: SPDIF_TX2 5'd13: SPDIF_TX3 5'd14: SPDIF_TX4 5'd15: SPDIF_TX5 5'd16: lclk_asrc_src_0 5'd17: lclk_asrc_src_1

28.5.2 LRCK Divider

In real-time transmission mode, src_lrck and dst_lrck are treated as data for ratio tracking. Frequency of src_lrck must be the same as sample rate, and frequency of dst_lrck must be the same as resample rate. To guarantee this, two clock dividers are integrating into ASRC. In following condition, the divider ought to be set and we need to wait for the clock to stabilize before start ASRC.

- Using pdm as source device, set src_lrck_div_con to (pdm_oversample_rate-1).
- Using spdif_rx as source device, set src_lrck_div_con to 127.
- Using spdif_tx as destination device, set dst_lrck_div_con to (128*spdif_tx_div-1).

28.5.3 Tracking period configure

Ratio tracking period is determined by the value of ratio_track_period and ratio_track_div, which means track information updates every (ratio_track_period+1)*(ratio_track_div+1) working clock. The longer the period, the more precise the tracking. To meet the ratio resolution, the following format should be meet:

(ratio_track_period+1)*(ratio_track_div+1) >=

Twclk*Fsrc_lrck*(1/Resolution+Fsrc_lrck/(Resolution*Fdst_lrck)+1)

Where Twclk is the period of working clock, Resolution is the bit wide of ratio, Fsrc_lrck is the frequency of src_lrck, and Fdst_lrck is the frequency of dst_lrck. Note that the smaller ratio_track_div is, the better, given the equation.

Once lrck sources from CRU for audio device like USB or MAC, fractional divider in the clock path may be used for seamless switching. Ratio tracking period must be an integer multiple of the frequency division period for tracking accuracy.

28.5.4 DMA configure

For transmitting data to ASRC and receiving data from ASRC, two DMA channels are need called DMA_TX and DMA_RX here. DMA mode for various ASRC mode is shown below.

Table 28-9 ASRC DMA Mode Description

ASRC Mode	DMA_TX	DMA_RX
memory fetch mode	M2P	P2M
MEM2MEM	M2P	P2M
MEM2DST	M2P	M2P
SRC2MEM	P2M	P2M
SRC2DST	P2M	M2P

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Once interacting with audio device, ASRC acts as memory and device issues DMA request. Once interacting with memory, ASRC acts as peripheral and issues DMA request according to dma_tx_thresh and dma_rx_thresh.
Both dma_tx_thresh and dma_rx_thresh are in the unit of chan_num. That is, the relation between DMA BURST and DMA thresh is shown below:

dma_tx_thresh=(DMA BURST)*(IFMT+1)/(chan_num+1)-1
dma_rx_thresh=(DMA BURST)*(OFMT+1)/(chan_num+1)-1

Note that in the condition chan_num=0, OFMT=1, ratio=1:8, DMA BURST is limited to 4.

28.5.5 Memory fetch mode configure

- **configure order**
  - set and start DMA_TX and DMA_RX;
  - set and start ASRC;
- **ASRC start configure**
  - set used channel number, chan_num;
  - set data format, OFMT, IFMT, OWL, IWL, OSJM and ISJM;
  - set manual_ratio, sample_rate and resample_rate;
  - set thresh, dma_rx_thresh, dma_tx_thresh, asrc_out_thresh and asrc_in_thresh;
  - set asrc_mode to 1;
  - set conversion length, fetch_length;
  - set conv_done_en to enable conversion done interrupt;
  - In loop mode, set continuous conversion times(loop_times), file channel number divided by used channel number(chan_times), file type(loop_start mode and loop_end_mode) and conversion interval(loop_gap_thresh), then enable loop_en;
  - set asrc_en to enable ASRC;
- **ASRC end configure**
  Waiting for conv_done and DMA_RX done interrupt, set asrc_en to disable ASRC;

28.5.6 Real-time transmission mode configure

- **configure order**
  - set the source of src_lrck and dst_lrck; set the division of src_lrck and dst_lrck if needed;
  - set and start DMA_TX and DMA_RX;
  - set and start ASRC;
  - set and start destination device in the mode MEM2DST or SRC2DST;
  - set and start source device in the mode SRC2MEM or SRC2DST;
- **ASRC start configure**
  - set used channel number, chan_num;
  - set data format, OFMT, IFMT, OWL, IWL, OSJM and ISJM;
  - set manual_ratio, sample_rate and resample_rate;
  - set thresh, dma_rx_thresh, dma_tx_thresh, asrc_out_thresh and asrc_in_thresh;
  - set asrc_mode to 0; set real_time_mode;
  - set ratio_track_period and ratio_track_div;
  - set ratio_track_dis to disable ratio tracking, set ratio_filt_dis to disable ratio tracking filt, or set ratio_exc_dis to disable ratio track feedback if needed;
  - set conv_done_en to enable conversion done interrupt;
  - In loop mode, set continuous conversion times(loop_times), file channel number divided by used channel number(chan_times), file type(loop_start mode and loop_end_mode) and conversion interval(loop_gap_thresh), then enable loop_en;
  - set asrc_en to enable ASRC;
- **ASRC end configure**
  - set asrc_in_stop to end conversion if source device stop;
  - set asrc_out_stop to end conversion if destionation device stop;
  - waiting for conv_done and DMA_RX done interrupt, set asrc_en to disable ASRC;

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Chapter 29 Flexible Serial Peripheral Interface（FSPI）

29.1 Overview

The FSPI is a flexible serial peripheral interface host controller to interface with external device.

The FSPI supports the following features:

- Support various vendor devices with flexible command sequencer engine
  - Serial NOR Flash
  - Serial NAND Flash
  - Serial pSRAM
  - Serial SRAM
- Support SDR mode
- Support Single/Dual/Quad IO mode
- Support a 32-bit AHB slave to read and write controller register bank and initiate command sequence, including transfer data from/to external device indirectly
- Support a 32-bit AHB master with embedded DMA engine to transfer data from/to external device indirectly
- Support independent clock for system bus HCLK and controller core SCLK
- Support maskable interrupts generation
- Support sampling clock with optionally configurable delay line
- Support 2 CS# operation

29.2 Block Diagram

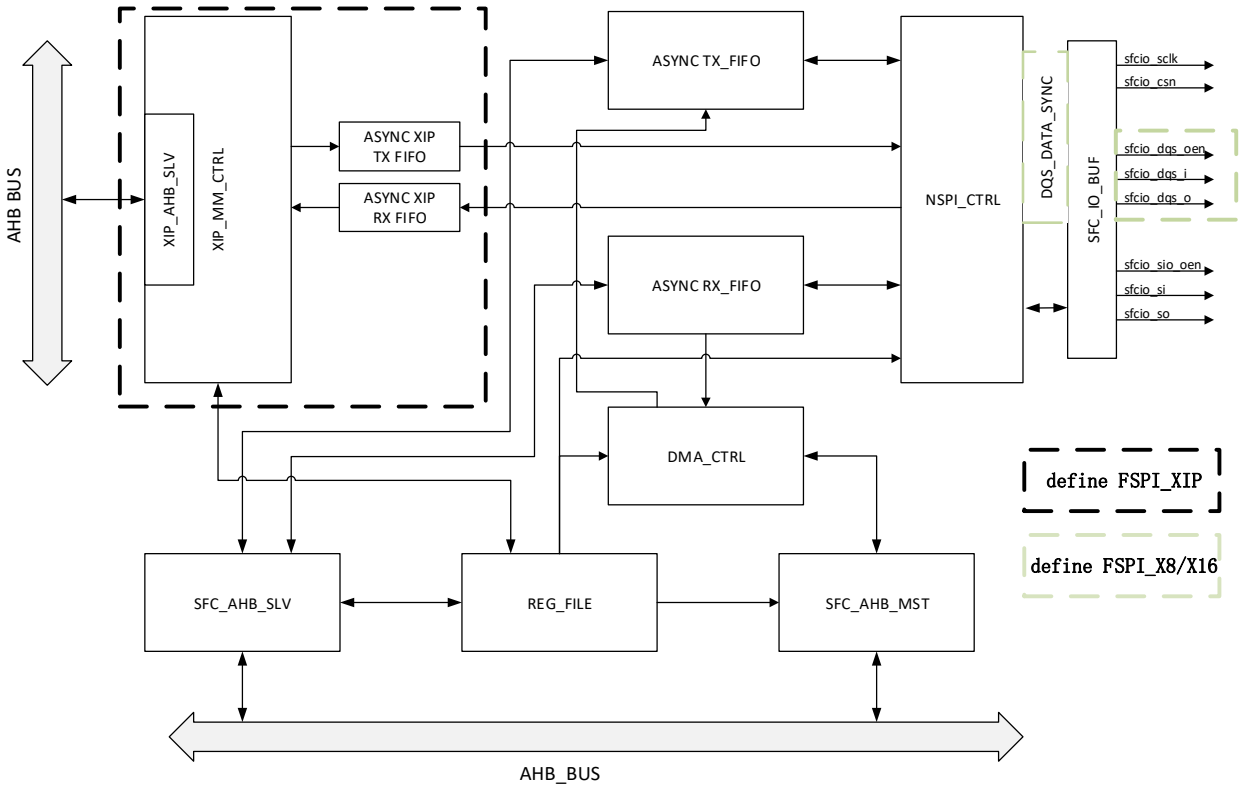

Fig. 29-1 FSPI Architecture

Memory-Mapped AHB slave is available when XIP feature is present. In current chip, this feature is not provided.

DQS sample logic is available when FSPI_X8 feature is present. In current chip, this feature is not provided.

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29.3 Function Description

29.3.1 AHB Slave

The AHB slave block is used to configure the register of controller to generate flexible command sequence, process the interrupt exception, target various device feature and AC timing specification. It is also used to write CMD/ADDR/DATA to TX FIFO and read DATA from RX FIFO which buffer the DATA from external device.

29.3.2 AHB Master

When the embedded DMA CTRL is used to transfer DATA, the AHB master is used to transfer data to other system region, such as internal SRAM, peripheral, external DRAM.

29.3.3 REG File

The REG File is configurable register bank to control the store the static configuration and dynamic status of controller.

29.3.4 DMA CTRL

A block takes responsible for splitting a long length transfer trans into AHB bus transaction and interfacing with ASYNC TX or RX FIFO.

29.3.5 FIFO

There are four FIFO in the FSPI controller. ASYNC TX FIFO and ASYNC RX FIFO is for normal transaction that initiated by command sequence driver. The ASYNC MM (Memory-Mapped) TX FIFO and ASYNC MM (Memory-Mapped) RX FIFO is only used to buffer DATA from or to external device initiated by system bus master directly.

29.3.6 NSPI CTRL

Sequence decode engine which generates specialized timing sequence for various device. The NSPI decode the transaction from TX FIFO and Memory-Mapped Controller and convert it to relative CMD/ADDR/DATA frame based on the configuration.

29.4 Register Description

29.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
FSPI0	0x2A340000
FSPI1	0x2A300000

29.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
FSPI_CTRL0	0x0000	W	0x00000000	Control Register for CS0 Device
FSPI_IMR	0x0004	W	0x000001FF	Interrupt Mask Register
FSPI_ICLR	0x0008	W	0x00000000	Interrupt Clear Register
FSPI_FTLR	0x000C	W	0x00001010	FIFO Threshold Level Register
FSPI_RCVR	0x0010	W	0x00000000	FSPI Recover Register
FSPI_AX0	0x0014	W	0x00000000	FSPI Auxiliary Data Value for CS0 Device
FSPI_ABIT0	0x0018	W	0x00000000	Extend Address Bits for CS0 Device
FSPI_ISR	0x001C	W	0x00000000	Interrupt Status
FSPI_FSR	0x0020	W	0x00000001	FIFO Status Register
FSPI_SR	0x0024	W	0x00000000	FSPI Status Register
FSPI_RISR	0x0028	W	0x00000000	Raw Interrupt Status Register

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Name	Offset	Size	Reset Value	Description
FSPI_VER	0x002C	W	0x00030010	Version Register
FSPI_QOP	0x0030	W	0x00000000	Quad Line Operation IO Level Pre-set Register
FSPI_EXT_CTRL	0x0034	W	0x00004023	Extend Control Register
FSPI_DLL_CTRL0	0x003C	W	0x00000001	Delay Line Control Register for CS0 Device
FSPI_EXT_AX	0x0044	W	0x0000F0FF	Extend Auxiliary Data Control Register
FSPI_SCLK_INATM_CNT	0x0048	W	0xFFFFFFFF	SCLK Inactive Timeout Counter
FSPI_XMMC_WCMD0	0x0050	W	0x00000000	Memory Mapped Control Write Command Register for CS0 Device
FSPI_XMMC_RCMD0	0x0054	W	0x00000000	Memory Mapped Control Read Command Register for CS0 Device
FSPI_XMMC_CTRL	0x0058	W	0x000072E0	Memory Mapped Control Register
FSPI_MODE	0x005C	W	0x00000000	Controller Working Mode Register
FSPI_DEVRGN	0x0060	W	0x00000017	Device Region Size Register
FSPI_DEVSIZE0	0x0064	W	0x00000012	Device Size Register for CS0 Device
FSPI_TME0	0x0068	W	0x00000000	Timeout Enable Control Register for CS0 Device
FSPI_XMMC_RX_WTMRK	0x0070	W	0x00000002	Memory Mapped Mode Receiver FIFO Water Mark Register
FSPI_DUMM_CTRL	0x0074	W	0x00000000	Dummy Cycle Control Register
FSPI_CMD_EXT	0x0078	W	0x00000000	Command Extend Register
FSPI_TRC_CTRL	0x007C	W	0x00000000	TRC Cycle Control Register
FSPI_DMATR	0x0080	W	0x00000000	DMA Trigger Register
FSPI_DMAADDR	0x0084	W	0x00000000	DMA Address Register
FSPI_LEN_CTRL	0x0088	W	0x00000000	Length Control Register
FSPI_LEN_EXT	0x008C	W	0x00000000	Length Extended Register
FSPI_XMMCSR	0x0094	W	0x00000000	Memory Mapped Status Register
FSPI_HYPER_RSVD_ADDR	0x0098	W	0x00000000	Hyperbus Reserved Address Bit
FSPI_VDMC0	0x009C	W	0x00000000	Vendor Device Mode Control Register
FSPI_CMD	0x0100	W	0x00000000	Indirect Command Register
FSPI_ADDR	0x0104	W	0x00000000	Address Register
FSPI_DATA	0x0108	W	0x00000000	Data Register
FSPI_CTRL1	0x0200	W	0x00000000	Control Register for CS1 Device
FSPI_AX1	0x0214	W	0x00000000	FSPI Auxiliary Data Value for CS1 Device
FSPI_ABIT1	0x0218	W	0x00000000	Extend Address Bits for CS1 Device
FSPI_DLL_CTRL1	0x023C	W	0x00000001	Delay Line Control Register for CS1 Device

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Name	Offset	Size	Reset Value	Description
FSPI_XMMC_WCMD1	0x0250	W	0x00000000	Memory Mapped Control Write Command Register for CS1 Device
FSPI_XMMC_RCMD1	0x0254	W	0x00000000	Memory-Mapped Command Control Register for CS1 Device
FSPI_DEVSIZE1	0x0264	W	0x00000012	Device Size Register for CS1 Device
FSPI_TME1	0x0268	W	0x00000000	Timeout Enable Control Register for CS1 Device
FSPI_VDMC1	0x029C	W	0x00000000	

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

29.4.3 Detail Registers Description

FSPI_CTRL0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	WP_EN WP# Port Enable 1'b0: Disable 1'b1: Enable. The WP# port will always drived by QOP[SO123] when QOP[SO123BP] is setted to disable.
28:27	RW	0x0	CMD_CTRL Indirect Command Field Controll 2'b00: Conmmand controlled by CMD[CMD] 2'b01: Conmmand controlled by CMD[CMD] and combine with 8 bit address 2'b10: Conmmand controlled by CMD_EXT/XMMC_WCMD/XMMC_RCMD[CMDF_EXT] according to different mode. Command length is 16 bit 2'b11: Reserved
26	RW	0x0	HYPER_RSVD_EN Hyperbus Reserved Address Bit Enable 1'b0: Disable 1'b1: Enable
25	RW	0x0	HYPER_ADDR_EN Address Remap in Hyperbus Mode 1'b0: Disable 1'b1: Enable
24	RW	0x0	INTRNL_CLK_MODE Internal CLK Mode 1'b0: Use the IOBUF core_clk to Sample the Data 1'b1: Use the Sclk from IOPAD to Sample the Data.

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Bit	Attr	Reset Value	Description
23:22	RW	0x0	DUMM_OVLP Dummy Phase Overlap with Address Phase. 3'd0: Dummy phase will start after address phase. 3'd1: Dummy phase will overlap a cycle with address phase. 3'd2: Dummy phase will overlap 2 cycles with address phase. 3'd3: Dummy phase will overlap 3 cycles with address phase. To set the overlap cycles between dummy phase and address phase.
21	RW	0x0	DBL_DUMM_CTRL Double dummy cycle controller 1'b0: dummy cycle always equal to CMD[DUMM]. 1'b1: dummy cycle will be twice of CMD[DUMM] when dqs is high.
20	RW	0x0	ADDR_STR Cmd phase work in STR mode in DTR mode. 1'b0: Disable 1'b1: Enable. The CTRL0/1[DTR_MODE] must set to 1'b1
19	RW	0x0	CMD_STR Cmd phase work in STR mode in DTR mode. 1'b0: Disable 1'b1: Enable. The CTRL0/1[DTR_MODE] must set to 1
18	RW	0x0	DTR_RDC_SEL Read Clk Select in DTR Mode 1'b0: Use external synchronous clock to sample the data. Quad DTR mode does not support this mode. 1'b1: Use internal clk to sample the data.
17	RW	0x0	DQS_MODE DQS MODE 1'b0: DQS can be drived by controller and device 1'b1: DQS is always drived by device
16	RW	0x0	DATAB16 16 Bit Data Line Width. 1'b0: Data Line Width controlled by CTRL0[DATB] 1'b1: 16 bits, x16 mode
15	RW	0x0	ADRB16 16 Bit Address Line Width. 1'b0: Address Line Width controlled by CTRL0[ADRB] 1'b1: 16 bits, x16 mode
14	RW	0x0	CMDB16 16 Bit Command Line Width. 1'b0: Command Line Width controlled by CTRL0[CMDB] 1'b1: 16 bits, x16 mode

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: 8 bits, x8 mode Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: 8 bits, x8 mode Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: 8 bits, x8 mode Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3	RW	0x0	DAT_ORDER The Order of Data in a Cycle 1'b0: Date in a cycle is from low byte to high byte 1'b1: Date in a cycle is from high byte to low byte
2	RW	0x0	DTR_MODE DTR mode enable 1'b0: STR mode 1'b1: DTR mode

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Bit	Attr	Reset Value	Description
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_IMR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ILLGL_WRM Illegal Register Write Interrupt Mask 1'b0: Illegal register write interrupt is not masked 1'b1: Illegal register write interrupt is masked Only valid when IP support the Secure Function.
8	RO	0x0	reserved
7	RW	0x1	DMAM DMA Finish Interrupt Mask 1'b0: DMA finish interrupt is not masked 1'b1: DMA finish interrupt is masked Only valid in indirect access mode.
6	RW	0x1	NSPIM NSPI Interrupt Mask 1'b0: NSPI interrupt is not masked 1'b1: NSPI interrupt is masked Valid in indirect access mode and memory mapped mode.
5	RW	0x1	AHBM AMBA AHB Error Interrupt Mask 1'b0: AMBA AHB Error interrupt is not masked 1'b1: AMBA AHB Error interrupt is masked Only valid in indirect access mode.

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Bit	Attr	Reset Value	Description
4	RW	0x1	TRANSM Transfer Finish Interrupt Mask 1'b0: Transfer finish interrupt is not masked 1'b1: Transfer finish interrupt is masked Only valid in indirect access mode.
3	RW	0x1	TXEM Transmit FIFO Empty Interrupt Mask 1'b0: Transmit FIFO empty interrupt is not masked 1'b1: Transmit FIFO empty interrupt is masked Only valid in indirect access mode.
2	RW	0x1	TXOM Transmit FIFO Overflow Interrupt Mask 1'b0: Transmit FIFO overflow interrupt is not masked 1'b1: Transmit FIFO overflow interrupt is masked Only valid in indirect access mode.
1	RW	0x1	RXUM Receive FIFO Underflow Interrupt Mask 1'b0: Receive FIFO underflow interrupt is not masked 1'b1: Receive FIFO underflow interrupt is masked Only valid in indirect access mode.
0	RW	0x1	RXFM Receive FIFO Full Interrupt Mask 1'b0: Receive FIFO full interrupt is not masked 1'b1: Receive FIFO full interrupt is masked Only valid in indirect access mode.

FSPI_ICLR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	W1C	0x0	ILLGL_WRC Illegal Register Write Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the ILLGL_WRS.
8	RO	0x0	reserved
7	W1C	0x0	DMAC DMA Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the DMAS

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Bit	Attr	Reset Value	Description
6	W1C	0x0	NSPIC NSPI Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the NSPIS.
5	W1C	0x0	AHBC AMBA AHB Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the AHBS.
4	W1C	0x0	TRANSC Transfer Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TRANSS.
3	W1C	0x0	TXEC Transmit FIFO Empty Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXES.
2	W1C	0x0	TXOC Transmit FIFO Overflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXOS.
1	W1C	0x0	RXUC Receive FIFO Underflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXUS.
0	W1C	0x0	RXFC Receive FIFO Full Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXFS.

FSPI_FTLR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0x10	RXFTLR Receive FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of receive FIFO entries is bigger than or equal to this value, the receive FIFO full interrupt is triggered.
7:0	RW	0x10	TXFTLR Transmit FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

FSPI_RCVR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	R/WSC	0x0	RCVR FSPI Recover Write any values to trigger the recovery of SMC NSPI state machine, FIFO state and other logic state.

FSPI_AX0

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT0

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	ABIT Address Bits Extend 6'h0: 1 bit 6'h1: 2 bits ... 6'h3f: 64 bits When ADDRB have no option for address bits number, use this field to set the right address bits number. Only valid when ADDRB is set to 2'b11.

FSPI_ISR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ILLGL_WRS Illegal Register Write Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
8	RO	0x0	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
6	RO	0x0	NSPIS NSPI Transaction Decode Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

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Bit	Attr	Reset Value	Description
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
0	RW	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

FSPI_FSR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	RXWLVL RX FIFO Water Level 5'h0: FIFO is empty 5'h1: 1 entry is taken ... 5'h10: 16 entry is taken, FIFO is full
15:13	RO	0x0	reserved
12:8	RO	0x00	TXWLVL TX FIFO Water Level 5'h0: FIFO is full 5'h1: 1 entry is left ... 5'h10: 16 entry is left, FIFO is empty
7:4	RO	0x0	reserved
3	RO	0x0	RXFS Receive FIFO Full Status 1'b0: RX FIFO is not full 1'b1: RX FIFO is full
2	RO	0x0	RXES Receive FIFO Empty Status 1'b0: RX FIFO is not empty 1'b1: RX FIFO is empty
1	RO	0x0	TXES Transmit FIFO Empty Status 1'b0: TX FIFO is not empty 1'b1: TX FIFO is empty
0	RO	0x1	TXFS Transmit FIFO Full Status 1'b0: TX FIFO is not full 1'b1: TX FIFO is full

FSPI_SR

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Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	SR Status Register 1'b0: NSPI Controller is idle 1'b1: NSPI Controller is busy When controller is busy, don't change the setting of control register. When NSPI is idle, the software can initiate new transaction to external device.

FSPI_RISR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ILLGL_WRS Illegal Register Write Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
8	RO	0x0	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
6	RO	0x0	NSPIS NSPI Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

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Bit	Attr	Reset Value	Description
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
0	RO	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

FSPI_VER

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RO	0x0	X16_CAP The X16 CAP of FSPI 1'b0: Unsupported 1'b1: Supported
18	RO	0x1	X8_CAP The X8 CAP of FSPI 1'b0: Unsupported 1'b1: Supported
17	RO	0x1	X4_CAP The X4 CAP of FSPI 1'b0: Unsupported 1'b1: Supported
16	RO	0x1	RSVD Reserved Bit
15:0	RO	0x0010	VER The Version ID of FSPI

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FSPI_QOP

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SO123BP SO123 Bypass Mode 1'b0: Disable bypass 1'b1: Enable bypass Default is enabled.
0	RW	0x0	SO123 D1/D2/D3 Data Value During Inactive When CS is Active 1'b0: Set to "0" 1'b1: Set to "1" The value of SO1, SO2 and SO3 during command and address bits input.

FSPI_EXT_CTRL

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	CSH_CLK_EN Sclk Toggle Enable when CS is HIGH 1'b0: Sclk will hold when CS is HIGH 1'b1: Sclk will toggle when CS is HIGH
18	RO	0x0	reserved
17:16	RW	0x0	CSH_EXT Chip Select Hold Time Extend: 1'h0: Default mode ; 1'h1: Extend 1 cycle ; 1'h2: Extend 2 cycle ; 1'h3: Extend 3 cycle ; To improve the transform IO timing, the application can set this field to extend chip select hold time.
15	RW	0x0	CSS_EXT Chip Select Setup Time Extend: 1'h0: Default mode ; 1'h1: Extend 1 cycle ; To improve the transform IO timing, the application can set this field to extend chip select setup time.
14	RW	0x1	SR_GEN_MODE Status Register Generation Mode 1'b0: Compatible mode with old controller 1'b1: Robust generation to indicates the status of controller If set to "1", the controller will only clear the SR bit after operation sequence done and CS is high.

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Bit	Attr	Reset Value	Description
13	RW	0x0	TRANS_INT_MODE Transmit Done Interrupt Generation Mode 1'b0: Trigger NSPI end in data done 1'b1: Trigger NSPI end in CS inactive Default Generation is compatible with old controller.
12	RO	0x0	reserved
11:8	RW	0x0	SWITCH_IO_O2I_CNT Switch IO Attribute Cycles in O2I Idle Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in O2I idle phase.
7:4	RW	0x2	SWITCH_IO_DUMM_CNT Switch IO Attribute Cycles in Dummy Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in Dummy data phase.
3:0	RW	0x3	CS_DESEL_CTRL CS Inactive Control 4'h0: 1 cycle 4'h1: 2 cycles 4'h2: 3 cycles 4'h3: 4 cycles ... 4'hf: 16 cycles The target cycles to hold CS inactive after de-assert the CS. Default value are 4 SCLK cycles that is enough for normal device.

FSPI_DLL_CTRL0

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RW	0x0	DQS1_SMP_SEL DQS1 Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling DQS1 source selection.

Bit	Attr	Reset Value	Description
30:25	RO	0x00	reserved
24:16	RW	0x000	DQS1_DLL_CFG DQS1 Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.
15	RW	0x0	SCLK_SMP_SEL SCLK Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_EXT_AX

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xf0	AX_SETUP_PAT Auxiliary Setup Data Pattern The AX data pattern that setup the continuous/enhance/XIP read mode
7:0	RW	0xff	AX_CANCEL_PAT Auxiliary Cancel Data Pattern The AX data pattern that cancel the continuous/enhance/XIP read mode.

FSPI_SCLK_INATM_CNT

Address: **Operational Base** + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	SCLK_INATM_CNT SCLK Inactive Timeout Counter When CS is active and SCLK is hold in high or low due to TX FIFO is empty or RX FIFO is full, if SCLK_INATM_EN is enabled, and timeout occurs, the controller will go back to idle and RX FIFO is flushed.

FSPI_XMMC_WCMD0

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CMDF_EXT Command Command data in memory mapped access mode when command length is 16 bit.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD0

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CMDF_EXT Command Command data in memory mapped access mode when command length is 16 bit.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_CTRL

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	PFT_EN Prefetch Enable 1'b0: Disable 1'b1: Enable Should disable prefetch if controller communicate with pSRAM which need refresh.
5	RW	0x1	DEV_HWEN Device AMBA AHB HWRITE Enable 1'b0: Disable 1'b1: Enable
4:0	RO	0x00	reserved

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FSPI_MODE

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	XMMC_MODE_EN Memory Mapped Mode Enable 1'b0: Disable, indirect access mode 1'b1: Enable, Memory-Mapped mode Before switching from indirect access mode to Memory-Mapped mode, the application should make sure the controller is in idle state and no pending transaction. If switch from Memory-Mapped to indirect access mode, software should initiate a dummy read by CPU before that.

FSPI_DEVRGN

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DEC_CTRL Decode Control 2'b00: 1 CS# 2'b01: 2 CS# 2'b10: 4 CS# 2'b11: Reserved Only valid in XMMC mode.
7:5	RO	0x0	reserved
4:0	RW	0x17	RSIZE Region Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes In Memory-Mapped mode, the CS is controlled by AHB address bus, region size is used to generate CS.

FSPI_DEVSIZE0

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G byte Device size is used to generate slop over status.

FSPI_TME0

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

FSPI_XMMC_RX_WTMRK

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	RX_FULL_WTMRK Memory Mapped Mode Receiver FIFO Water Mark. Default is enough.

FSPI_DUMM_CTRL

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:1	RW	0x00	DUMM_EXT Dummy Cycles 7'h0: No dummy cycle ... 7'h8: 8 cycles ... 7'h127: 127 cycles Dummy bit cycles in indirect access mode.

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Bit	Attr	Reset Value	Description
0	RW	0x0	DUMM_SEL Dummy Cycle Controll Selection 1'b0: Dummy Cycle controlled by CMD[DUMM] 1'b1: Dummy Cycle controlled by DUMM_EXT

FSPI_CMD_EXT

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	CMDF_EXT Command Command data in indirect access mode when command length is 16 bit.

FSPI_TRC_CTRL

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:1	RW	0x0000	TRC_CYCLE The minimum transfer cycle 16'd0: 1 Cycle 16'd1: 2 Cycles ..... 16'd100: 101 Cycles ..... The target cycles to hold the controller in working state in a transfer.
0	RW	0x0	TRC_EN The minimum cycle in a transfer enable 1'b0: disable 1'b1: enable

FSPI_DMATR

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	DMATR DMA Trigger Write "1" to start the DMA transfer.

FSPI_DMAADDR

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAADDR DMA Address The destination or source data address in current system.

FSPI_LEN_CTRL

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	TRB_SEL Total Transfer Bytes Selection 1'b0: TRB controlled by CMD[TRB] 1'b1: TRB controlled by LEN_EXT

FSPI_LEN_EXT

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRB_EXT Total Transfer Bytes Extended 32'd0: No data 32'd1: 1 Byte 32'd2: 2 Bytes ... Total data bytes number that will write to /read from the device.

FSPI_XMMCSR

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/WSC	0x0	SLOPOVER1 Slop Over Register for CS1 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.
0	R/WSC	0x0	SLOPOVER0 Slop Over Register for CS0 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.

FSPI_HYPER_RSVD_ADDR

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	HYPER_RSVD_ADDR Hyperbus Reserved Address Bit

FSPI_VDMC0

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	MID MID 4'h1: Infineon/Cypress 4'h3: ISSI 4'h6: Winbond 4'hd: APM Others: Reserved

FSPI_CMD

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	WO	0x0	CS Device Chip Select. 2'b00: Chip select 0 2'b01: Chip select 1 2'b10: Reserved 2'b11: Reserved
29:16	WO	0x0000	TRB Total Transfer Bytes 14'd0: No data 14'd1: 1 Byte 14'd2: 2 Bytes ... Total data bytes number that will write to or read from the device.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in indirect access mode. If there is not address command to send, set to zero.

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Bit	Attr	Reset Value	Description
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	WO	0x0	WR Write or Read 1'b0: Read 1'b1: Write
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in indirect access mode.
7:0	WO	0x00	CMD Command Command data in indirect access mode.

FSPI_ADDR

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ADDR Address Register Indirect access start address data for current command sequence.

FSPI_DATA

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DATA Data Register Device data read or write from/to device.

FSPI_CTRL1

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	WP_EN WP# Port Enable 1'b0: Disable 1'b1: Enable. The WP# port will always drived by QOP[SO123] when QOP[SO123BP] is setted to disable.

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Bit	Attr	Reset Value	Description
28:27	RW	0x0	CMD_CTRL Indirect Command Field Controll 2'b00: Conmmand controlled by CMD[CMD] 2'b01: Conmmand controlled by CMD[CMD] and combine with 8 bit address 2'b10: Conmmand controlled by CMD_EXT/XMMC_WCMD/XMMC_RCMD[CMDF_EXT] according to different mode. Command length is 16 bit 2'b11: Reserved
26	RW	0x0	HYPER_RSVD_EN Hyperbus Reserved Address Bit Enable 1'b0: Disable 1'b1: Enable
25	RW	0x0	HYPER_ADDR_EN Address Remap in Hyperbus Mode 1'b0: Disable 1'b1: Enable
24	RW	0x0	INTRNL_CLK_MODE Internal CLK Mode 1'b0: Use the IOBUF core_clk to Sample the Data 1'b1: Use the Sclk from IOPAD to Sample the Data.
23:22	RW	0x0	DUMM_OVLP Dummy Phase Overlap with Address Phase. 3'd0: Dummy phase will start after address phase. 3'd1: Dummy phase will overlap a cycle with address phase. 3'd2: Dummy phase will overlap 2 cycles with address phase. 3'd2: Dummy phase will overlap 3 cycles with address phase. To set the overlap cycles between dummy phase and address phase.
21	RW	0x0	DBL_DUMM_CTRL Double dummy cycle controller 1'b0: dummy cycle always equal to CMD[DUMM]. 1'b1: dummy cycle will be twice of CMD[DUMM] when dqs is high.
20	RW	0x0	ADDR_STR Cmd phase work in STR mode in DTR mode. 1'b0: Disable 1'b1: Enable. The CTRL0/1[DTR_MODE] must set to 1'b1
19	RW	0x0	CMD_STR Cmd phase work in STR mode in DTR mode. 1'b0: Disable 1'b1: Enable. The CTRL0/1[DTR_MODE] must set to 1

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Bit	Attr	Reset Value	Description
18	RW	0x0	DTR_RDC_SEL Read Clk Select in DTR Mode 1'b0: use DQS to sample the data 1'b1: use SCLK to sample the data
17	RW	0x0	DQS_MODE DQS MODE 1'b0: DQS can be drived by controller and device 1'b1: DQS is always drived by device
16	RW	0x0	DATAB16 16 Bit Data Line Width. 1'b0: Data Line Width controlled by CTRL0[DATB] 1'b1: 16 bits, x16 mode
15	RW	0x0	ADRB16 16 Bit Address Line Width. 1'b0: Address Line Width controlled by CTRL0[ADRB] 1'b1: 16 bits, x16 mode
14	RW	0x0	CMDB16 16 Bit Command Line Width. 1'b0: Command Line Width controlled by CTRL0[CMDB] 1'b1: 16 bits, x16 mode
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3	RW	0x0	DAT_ORDER The Order of Data in a Cycle 1'b0: Date in a cycle is from low byte to high byte 1'b1: Date in a cycle is from high byte to low byte
2	RW	0x0	DTR_MODE DTR mode enable 1'b0: STR mode 1'b1: DTR mode
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_AX1

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT1

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	ABIT Address Bits Extend 6'h0: 1 bit 6'h1: 2 bits ... 6'h3f: 64 bits When ADDRB have no option for address bits number, use this field to set the right address bits number. Only valid when ADDRB is set to 2'b11.

FSPI_DLL_CTRL1

Address: **Operational Base** + offset (0x023C)

Bit	Attr	Reset Value	Description
31	RW	0x0	DQS1_SMP_SEL DQS1 Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling DQS1 source selection.
30:25	RO	0x00	reserved
24:16	RW	0x000	DQS1_DLL_CFG DQS1 Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.
15	RW	0x0	SCLK_SMP_SEL SCLK sampling selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_XMMC_WCMD1

Address: **Operational Base** + offset (0x0250)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CMDF_EXT Command Command data in memory mapped access mode when command length is 16 bit.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD1

Address: **Operational Base** + offset (0x0254)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CMDF_EXT Command Command data in memory mapped access mode when command length is 16 bit.

Bit	Attr	Reset Value	Description
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_DEVSIZE1

Address: **Operational Base** + offset (0x0264)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes Device size is used to generate slop over status.

FSPI_TME1

Address: **Operational Base** + offset (0x0268)

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Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

FSPI_VDMC1

Address: **Operational Base** + offset (0x029C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	MID MID 4'h1: Infineon/Cypress 4'h3: ISSI 4'h6: Winbond 4'hd: APM Others: Reserved

29.5 Interface Description

Table 29-1 FSPI Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sfc0_sclk	O	EMMC_CLK/FSPI0_CLK/SAI0_SDO3_M2/SAI0_SDI1_M2/PDM0_CLK0_M1/PWM2_CH7_M1/GPIO1_B1_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[7:4]=4'h2
sfc0_cs0n	O	EMMC_RSTN/FSPI0_CSN0/UART6_RX_M2/I2C7_SDA_M0/MIPI_TE_M3/PWM2_CH1_M0/GPIO1_B3_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h2
sfc0_cs1n	O	EMMC_CMD/FSPI0_RSTN/FSPI0_CSN1/UART6_TX_M2/I2C7_SCL_M0/GPIO1_B0_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[3:0]=4'h2
sfc0_rstn	O	EMMC_CMD/FSPI0_RSTN/FSPI0_CSN1/UART6_TX_M2/I2C7_SCL_M0/GPIO1_B0_u	NOTE:Use GPIO1_B0 to reset device in maskrom
sfc0_sio0	I/O	EMMC_D0/FSPI0_D0/SAI0_SCLK_M2/UART7_RTSN_M1/I2C2_SCL_M1/GPIO1_A0_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[3:0]=4'h2
sfc0_sio1	I/O	EMMC_D1/FSPI0_D1	TOP_IOC_GPIO1A_IOMUX_SEL_L[

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Module Pin	Direction	Pad Name	IOMUX Setting
		/SAI0_LRCK_M2/UART7_CTSN_M1/I2C2_SDA_M1/GPIO1_A1_u	7:4]=4'h2
sfc0_sio2	I/O	EMMC_D2/FSPI0_D2/SAI0_SDO1_M2/SAI0_SDI3_M2/PDM0_SDI3_M1/UART7_TX_M1/UART6_RTSN_M2/GPIO1_A2_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4'h2
sfc0_sio3	I/O	EMMC_D3/FSPI0_D3/SAI0_SDO2_M2/SAI0_SDI2_M2/PDM0_SDI1_M1/UART7_RX_M1/UART6_CTSN_M2/GPIO1_A3_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4'h2
sfc1_sclk_m0	O	SDMMC0_CLK/FSPI1_CLK_M0/SAI3_SCLK_M3/TEST_CLK_OUT/UART5_TX_M2/I2C5_SCL_M0/SPI0_CLK_M1/I3C1_SDA_PU_M1/GPIO2_A5_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[7:4]=4'h2
sfc1_cs0n_m0	O	SDMMC0_CMD/FSPI1_CSN0_M0/SAI3_SDO_M3/UART5_RX_M2/I2C5_SDA_M0/SPI0_CSN0_M1/PWM2_CH4_M0/GPIO2_A4_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[3:0]=4'h2
sfc1_sio0_m0	I/O	SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/CAN0_RX_M0/PWM2_CH2_M0/GPIO2_A0_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'h2
sfc1_sio1_m0	I/O	SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'h2
sfc1_sio2_m0	I/O	SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[11:8]=4'h2

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Module Pin	Direction	Pad Name	IOMUX Setting
sfc1_sio3_m0	I/O	SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/CAN1_TX_M0/I3C1_SDA_M1/GPIO2_A3_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[15:12]=4'h2
sfc1_sclk_m1	O	ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'h3
sfc1_cs0n_m1	O	ETH1_PPSTRIG_M1/SDMMC1_DETN_M0/FSPI1_CSN0_M1/UART4_CTSN_M1/I2C6_SDA_M1/SPI2_CSN0_M1/GPIO1_C3_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[15:12]=4'h3
sfc1_cs1n_m1	O	ETH1_PPSCLK_M1/SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_CSN1_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[11:8]=4'h3
sfc1_rstn_m1	O	ETH1_PPSCLK_M1/SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_CSN1_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	NOTE:Use GPIO1_C2 to reset device in maskrom
sfc1_sio0_m1	I/O	ETH1_TXD0_M1/FSPI1_D0_M1/UART4_TX_M1/UART2_RTSN_M0/SPI2_MOSI_M1/PCIE0_BUTTONRSTN/GPIO1_C4_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[3:0]=4'h3
sfc1_sio1_m1	I/O	ETH1_TXD1_M1/FSPI1_D1_M1/UART4_RX_M1/UART2_CTSN_M0/SPI2_MISO_M1/PCIE1_BUTTONRSTN/GPIO1_C5_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[7:4]=4'h3
sfc1_sio2_m1	I/O	ETH1_TXCTL_M1/FSPI1_D2_M1/PDM0_SDI0_M2/UART2_TX_M0/I2C8_SCL_M1/SATA_CPPOD/GPIO1_C6_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[11:8]=4'h3

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Module Pin	Direction	Pad Name	IOMUX Setting
sfc1_sio3_m1	I/O	ETH1_RXD0_M1/FSPI1_D3_M1/PDM0_SDI1_M2/UART2_RX_M0/I2C8_SDA_M1/SATA_CPDET/GPIO1_C7_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[15:12]=4'h3

Notes: I=input, O=output, I/O=input/output, bidirectional

29.6 Application Notes

29.6.1 Typical Program Flow Without DMA

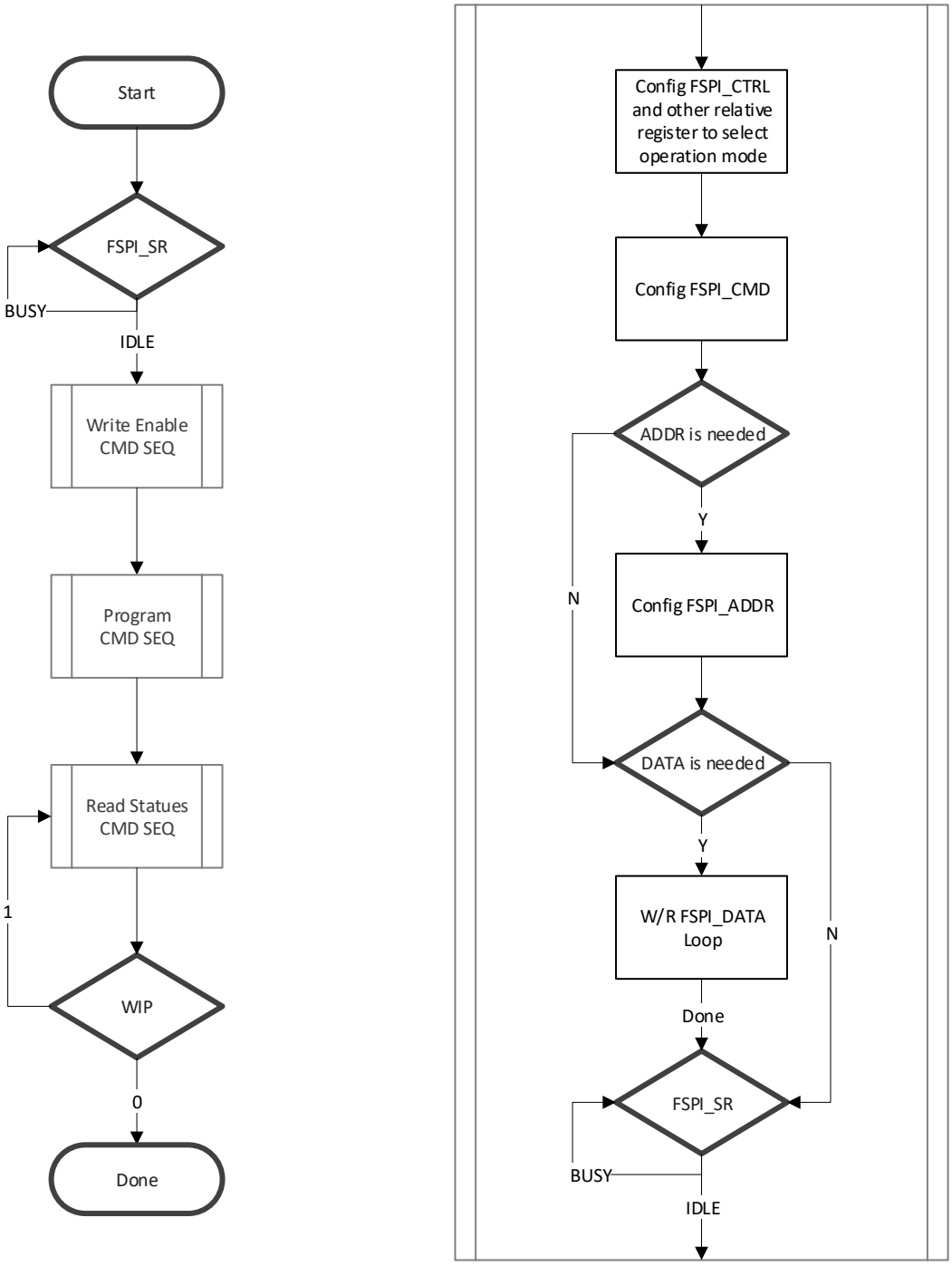

Fig. 29-2 Program Flow

All the AHB bus write data to FSPI_CMD, FSPI_ADDR and FSPI_DATA will be marked with different header and then pushed into transmit FIFO by writing order.

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29.6.2 Typical READ Flow Without DMA

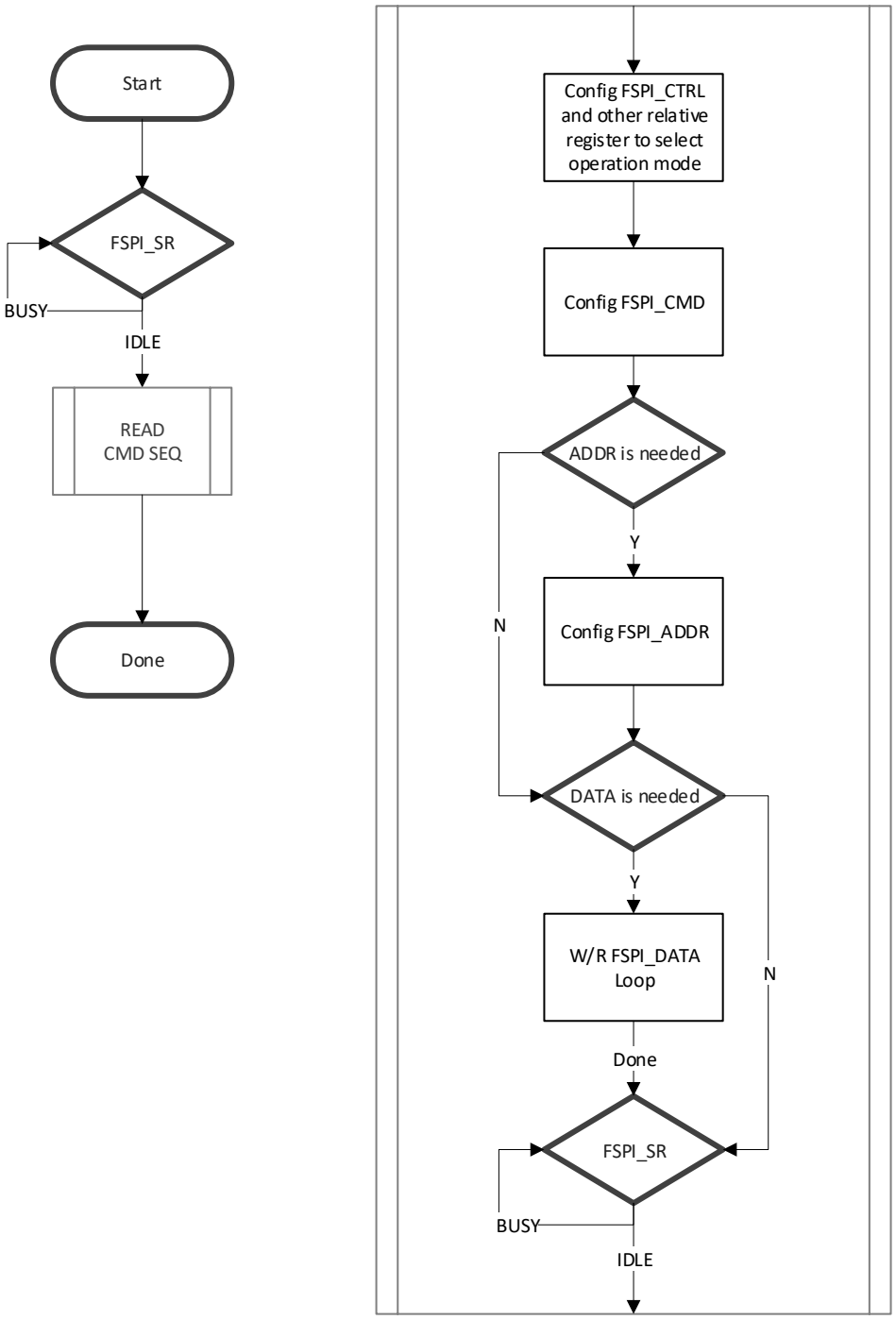

Fig. 29-3 Read Flow

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29.6.3 Command Flow with DMA

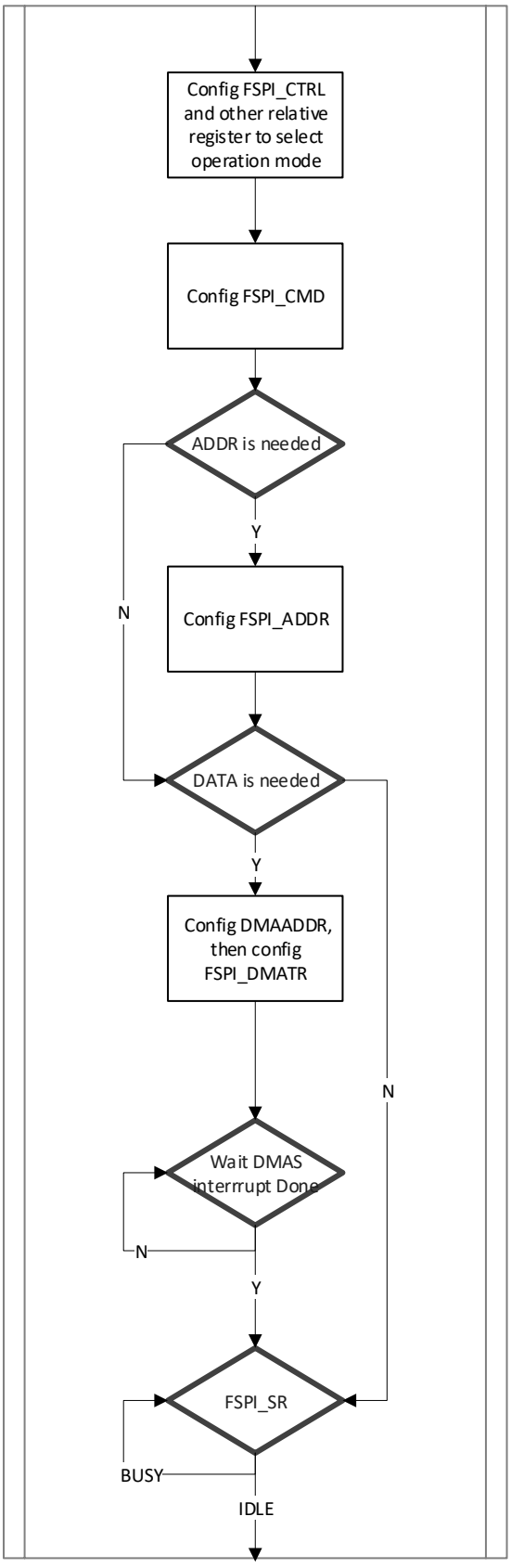

Fig. 29-4 Command with DMA Flow

The total transfer bytes is decided by TRB register in FSPI_CMD and must be aligned to 2 bytes.

29.6.4 SPI Mode and Sampling Phase Control

The register SPIM in FSPI_CTRL will decide the default value of SCLK when CS# is inactive. When SPIM=0, the default value is 0, means Mode 0. When SPIM=1, the default value is 1,

means SPI Mode 3.

The register SHIFTPAHSE in FSPI_CTRL will decide when to sample the SIO data. If SHIFTPAHSE=0, it will sample the data at the posedge of SCLK sampling clock. If SHIFTPHASE=1, it will sample the data at the negedge of SCLK sampling. The phase delay of sampling clock SCLK is configurable by SMP_DLL_CFG. It is strongly recommended that the SMP_DLL_CFG is set to 1 when SCLK_SMP_SEL is in bypass mode.

Individual FSPI_DLL_CTRL[n] allows flexibly control the DLL for each CSn channel, and the DLL is switched dynamically when the CSn is in operation.

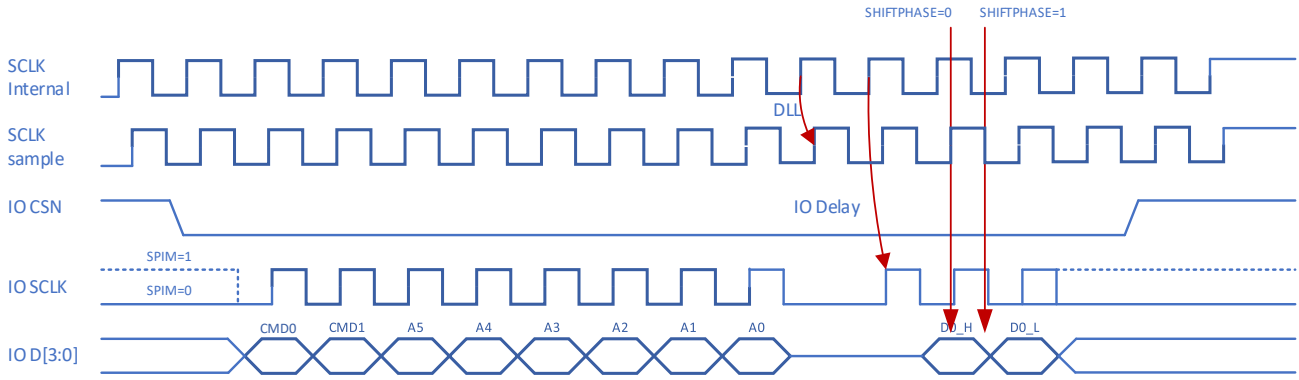

Fig. 29-5 SPI mode

29.6.5 Idle Cycles

The FSPI_CTRL register is a global control register, when the controller is in busy state (FSPI_SR), FSPI_CTRL cannot be set. The field IDLE_CYCLE (FSPI_CTRL[7:4]) of this register are used to configure the idle level cycles of FSPI core clock (SCLK) before reading the first bit of the read command.

Like the following picture shows, the highlighted line of the SCLK is the idle cycles, during these cycles, the chip pad is switched to output. When IDLE_CYCLE =0, it means there will be no idle level cycles.

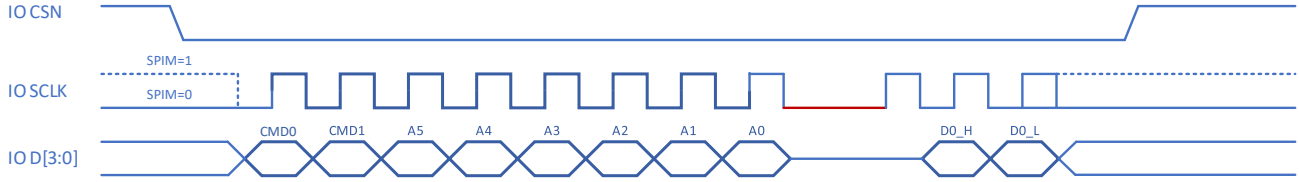

Fig. 29-6 Idle cycles

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Chapter 30 Serial Peripheral Interface (SPI)

30.1 Overview

The serial peripheral interface is an APB slave device. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of slave select signals or the first edge of the serial clock. The slave select line is held high when the SPI is idle or disabled. This SPI controller can work as either master or slave mode.

SPI Controller supports the following features:

- Support Motorola SPI, TI Synchronous Serial Protocol and National Semiconductor Micro wire interface
- Support 32-bit APB bus
- Support two internal 16-bit wide and 64-location deep FIFOs, one for transmitting and the other for receiving serial data
- Support two chip select signals in master mode
- Support 4,8,16 bit serial data transfer
- Support configurable interrupt polarity
- Support asynchronous APB bus and SPI clock
- Support master and slave mode
- Support DMA handshake interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow, interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combining interrupt output
- Support up to half of SPI clock frequency transfer in master mode and one quarter of SPI clock frequency transfer in slave mode
- Support full and half duplex mode transfer
- Stop transmitting SCLK if transmit FIFO is empty or receive FIFO is full in master mode
- Support configurable delay from chip select active to SCLK active in master mode
- Support configurable period of chip select inactive between two parallel data in master mode
- Support big and little endian, MSB and LSB first transfer
- Support two 8-bit audio data store together in one 16-bit wide location
- Support sample MISO 0~3 SPI clock cycles later
- Support configurable SCLK polarity and phase
- Support fix and incremental address access to transmit and receive FIFO
- Support timeout mechanism in slave mode
- Support BYPASS slave mode, in which MISO and MOSI logic is drive by sclk_in directly instead of spi_clk

30.2 Block Diagram

The SPI Controller comprises with:

- AMBA APB interface and DMA Controller Interface
- Transmit and receive FIFO controllers and an FSM controller
- Register block
- Shift control and interrupt

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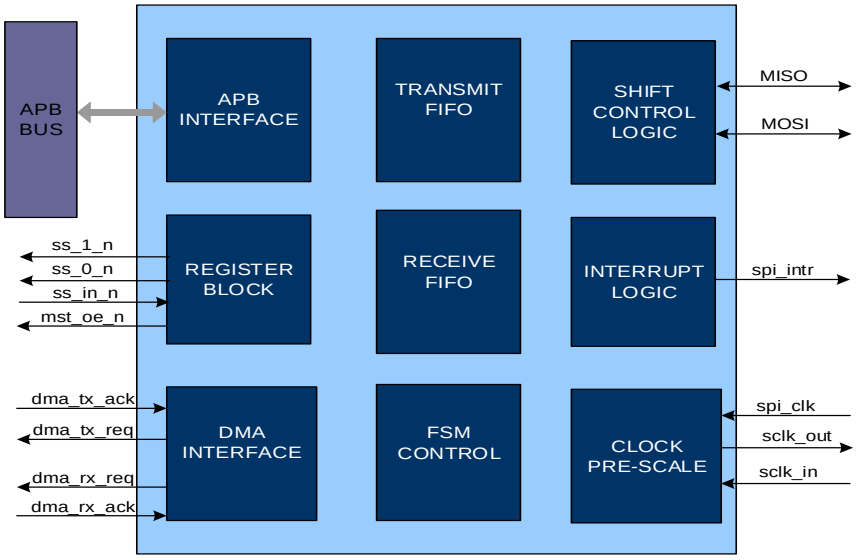

Fig. 30-1 SPI Controller Block Diagram

APB INTERFACE

The host processor accesses data, control, and status information on the SPI through the APB interface. The SPI supports APB data bus widths of 32 bits and 8 or 16 bits when reading or writing internal FIFO if data frame size (SPI_CTRL0[1:0]) is set to 8 bits.

DMA INTERFACE

This block has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA Controller.

FIFO LOGIC

For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the transmit FIFO. Data received from the external serial device into the SPI is pushed into the receive FIFO. Both FIFOs are 64x16bits.

FSM CONTROL

Control the state’s transformation of the design.

REGISTER BLOCK

All registers in the SPI are addressed at 32-bit boundaries to remain consistent with the APB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

SHIFT CONTROL

Shift control logic shift the data from the transmit FIFO or to the receive FIFO. This logic automatically right-justifies receive data in the receive FIFO buffer.

INTERRUPT CONTROL

The SPI supports combined and individual interrupt requests, each of which can be masked. The combined interrupt request is the OR relationship between all other SPI interrupts after masking.

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30.3 Function Description

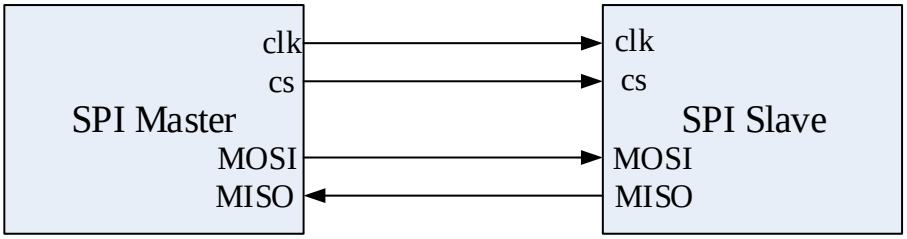

Fig. 30-2 SPI Master and Slave Interconnection

The SPI controller support dynamic switching between master and slave in a system. The diagram shows how the SPI controller connects with other SPI devices.

Operation Modes

The SPI can be configured in the following two fundamental modes of operation: Master Mode when SPI_CTRLR0 [20] is 1'b0, Slave Mode when SPI_CTRLR0 [20] is 1'b1.

Transfer Modes

The SPI operates in the following three modes when transferring data on the serial bus.
1). Transmit and Receive
When SPI_CTRLR0 [19:18] == 2'b00, both transmit and receive logic are valid.
2). Transmit Only
When SPI_CTRLR0 [19:18] == 2'b01, the receive data are invalid and should not be stored in the receive FIFO.
3). Receive Only
When SPI_CTRLR0 [19:18] == 2'b10, the transmit data are invalid.

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as:
When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})
When SPI Controller works as slave, the F_{spi_clk}>= 6 × (maximum F_{sclk_in})

With the SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical serial clock phase (SCPH) and clock polarity (SCPOL) values. The data frame can be 4/8/16 bits in length.

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the MISO and MOSI lines prior to the first serial clock edge. The following two figures show a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for configuration parameters SCPOL = 0 and SCPOL = 1.

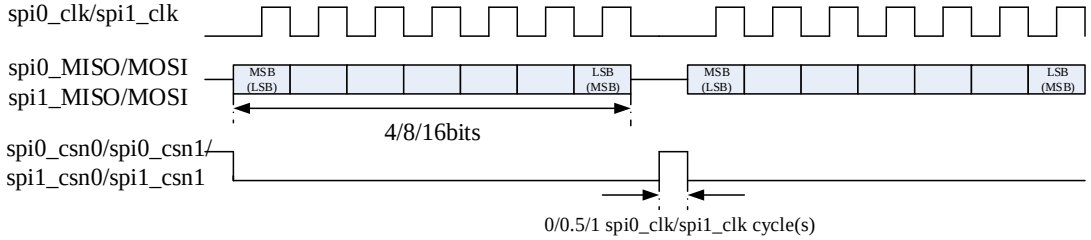

Fig. 30-3 SPI Format (SCPH=0 SCPOL=0)

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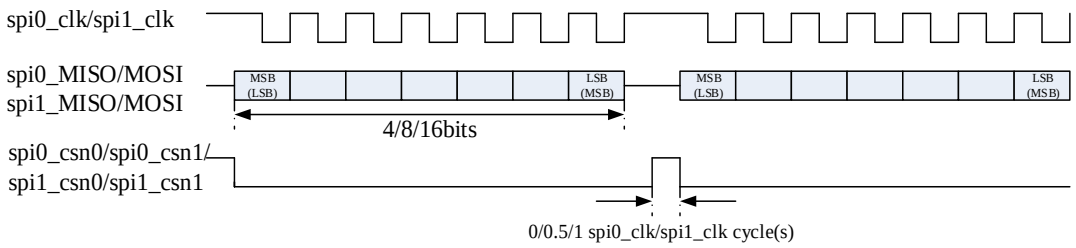

Fig. 30-4 SPI Format (SCPH=0 SCPOL=1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the SPI format when the configuration parameter SCPH = 1.

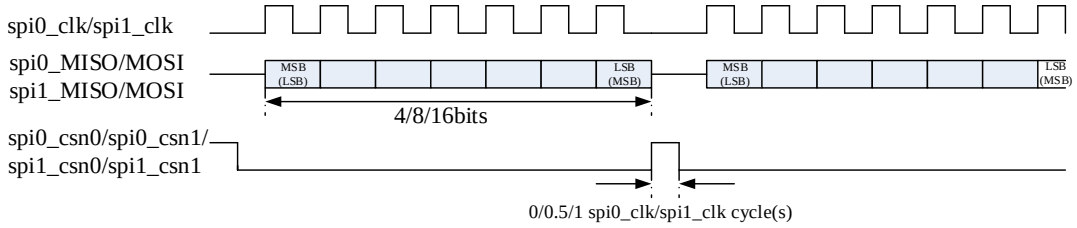

Fig. 30-5 SPI Format (SCPH=1 SCPOL=0)

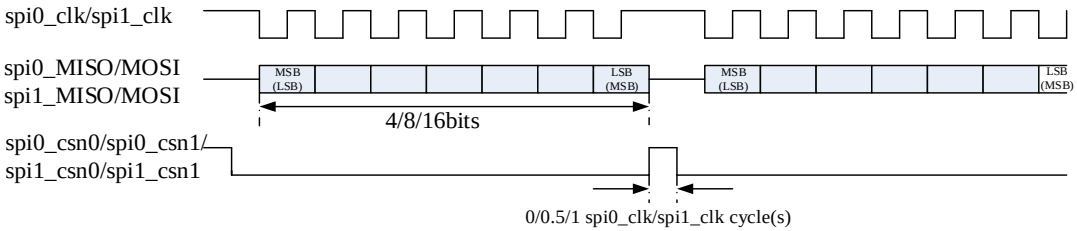

Fig. 30-6 SPI Format (SCPH=1 SCPOL=1)

30.4 Register Description

30.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SPI0	0x2ACF0000
SPI1	0x2AD00000
SPI2	0x2AD10000
SPI3	0x2AD20000
SPI4	0x2AD30000

30.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI_CTRLR0	0x0000	W	0x00000002	Control Register 0
SPI_CTRLR1	0x0004	W	0x00000000	Control Register 1
SPI_ENR	0x0008	W	0x00000000	SPI Enable Register
SPI_SER	0x000C	W	0x00000000	Slave Enable Register
SPI_BAUDR	0x0010	W	0x00000000	Baud Rate Select
SPI_TXFTLR	0x0014	W	0x00000000	Transmit FIFO Threshold Level
SPI_RXFTLR	0x0018	W	0x00000000	Receive FIFO Threshold Level
SPI_TXFLR	0x001C	W	0x00000000	Transmit FIFO Level

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Name	Offset	Size	Reset Value	Description
SPI_RXFLR	0x0020	W	0x00000000	Receive FIFO Level
SPI_SR	0x0024	W	0x0000004C	SPI Status
SPI_IPR	0x0028	W	0x00000000	Interrupt Polarity
SPI_IMR	0x002C	W	0x00000000	Interrupt Mask
SPI_ISR	0x0030	W	0x00000000	Interrupt Status
SPI_RISR	0x0034	W	0x00000001	Raw Interrupt Status
SPI_ICR	0x0038	W	0x00000000	Interrupt Clear
SPI_DMACR	0x003C	W	0x00000000	DMA Control
SPI_DMATDLR	0x0040	W	0x00000000	DMA Transmit Data Level
SPI_DMARDLR	0x0044	W	0x00000000	DMA Receive Data Level
SPI_VERSION	0x0048	W	0x00110002	IP Version
SPI_TIMEOUT	0x004C	W	0x00000000	Timeout Control Register
SPI_BYPASS	0x0050	W	0x00000000	Bypass Control Register
SPI_TXDR	0x0400	W	0x00000000	Transmit FIFO Data
SPI_RXDR	0x0800	W	0x00000000	Receive FIFO Data

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

30.4.3 Detail Registers Description

SPI_CTRLR0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	lbk Loop back mode select. 1'b0: Normal mode. 1'b1: Loop back mode, rxd is connected to txd.
24:23	RW	0x0	soi Port ss_in output inverted. 1'b0: Corresponding bit of ss_in is not inverted. 1'b1: Corresponding bit of ss_in is inverted.
22	RW	0x0	sm Port sclk_in is masked by SS_N or not. 1'b0: sclk_in is masked. 1'b1: sclk_in is not masked.
21	RW	0x0	mtm Valid when frame format is set to National Semiconductors Microwire. 1'b0: Non-sequential transfer 1'b1: Sequential transfer
20	RW	0x0	opm Master and slave mode select. 1'b0: Master mode 1'b1: Slave mode
19:18	RW	0x0	xfm Transmit and receive mode select. 2'b00 : Transmit & Receive 2'b01 : Transmit only 2'b10 : Receive only 2'b11 : Reserved
17:16	RW	0x0	frf 2'b00: Motorola SPI 2'b01: Texas Instruments SSP 2'b10: National Semiconductors Microwire 2'b11: Reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	rsd When SPI is configured as a master, if the rxd data cannot be sampled by the sclk_out edge at the right time, this register should be configured to define the number of the spi_clk cycles after the active sclk_out edge to sample rxd data later when SPI works at high frequency. 2'b00: Do not delay 2'b01: 1 cycle delay 2'b10: 2 cycles delay 2'b11: 3 cycles delay
13	RW	0x0	bht Valid when data frame size is 8bit. 1'b0: APB 16bit write/read, SPI 8bit write/read. 1'b1: APB 8bit write/read, SPI 8bit write/read.
12	RW	0x0	fbm 1'b0: First bit is MSB. 1'b1: First bit is LSB.
11	RW	0x0	em Serial endian mode can be configured by this bit. APB endian mode is always little endian. 1'b0: Little endian 1'b1: Big endian
10	RW	0x0	ssd Valid when the frame format is set to Motorola SPI and SPI used as a master. 1'b0: The period between ss_n active and sclk_out active is half sclk_out cycles. 1'b1: The period between ss_n active and sclk_out active is one sclk_out cycle.
9:8	RW	0x0	csm Valid when the frame format is set to Motorola SPI and SPI used as a master. 2'b00: ss_n keep low after every frame data is transferred. 2'b01: ss_n be high for half sclk_out cycles after every frame data is transferred. 2'b10: ss_n be high for one sclk_out cycle after every frame data is transferred. 2'b11: Reserved
7	RW	0x0	scpol Valid when the frame format is set to Motorola SPI. 1'b0: Inactive state of serial clock is low. 1'b1: Inactive state of serial clock is high.
6	RW	0x0	scph Valid when the frame format is set to Motorola SPI. 1'b0: Serial clock toggles in middle of first data bit. 1'b1: Serial clock toggles at start of first data bit.

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Bit	Attr	Reset Value	Description
5:2	RW	0x0	cfs Selects the length of the control word for the Microwire frame format. 4'b0000~0010: Reserved 4'b0011: 4-bit serial data transfer 4'b0100: 5-bit serial data transfer 4'b0101: 6-bit serial data transfer 4'b0110: 7-bit serial data transfer 4'b0111: 8-bit serial data transfer 4'b1000: 9-bit serial data transfer 4'b1001: 10-bit serial data transfer 4'b1010: 11-bit serial data transfer 4'b1011: 12-bit serial data transfer 4'b1100: 13-bit serial data transfer 4'b1101: 14-bit serial data transfer 4'b1110: 15-bit serial data transfer 4'b1111: 16-bit serial data transfer
1:0	RW	0x2	dfs Selects the data frame length. 2'b00: 4bit data 2'b01: 8bit data 2'b10: 16bit data 2'b11: Reserved

SPI_CTRLR1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ndm When Transfer Mode is receive only, this register field sets the number of data frames to be continuously received by the SPI. The SPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 4GB of data in a continuous transfer.

SPI_ENR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	enr Enables and disables all SPI operations. Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_SER

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	ser Slave Enable Register.The register enable the individual slave select output lines, 2 slave-select output pins are available.This register is valid only when SPI is configured as a master device.

SPI_BAUDR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	baudr SPI Clock Divider. This register is valid only when the SPI is configured as a master device.The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fspi_clk/BAUDR Where BAUDR is any even value between 2 and 65534. For example: for Fspi_clk = 3.6864MHz and BAUDR =2 Fsclk_out = 3.6864/2= 1.8432MHz

SPI_TXFTLR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	txftlr When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

SPI_RXFTLR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rxftlr When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

SPI_TXFLR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	txflr Contains the number of valid data entries in the transmit FIFO.

SPI_RXFLR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	rxflr Contains the number of valid data entries in the receive FIFO.

SPI_SR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x1	ssi 1'b0: ss_in_n is low. 1'b1: ss_in_n is high.
5	RO	0x0	stb 1'b0: Slave TX not busy. 1'b1: Slave TX busy.

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Bit	Attr	Reset Value	Description
4	RO	0x0	rff 1'b0: Receive FIFO is not full. 1'b1: Receive FIFO is full.
3	RO	0x1	rfe 1'b0: Receive FIFO is not empty. 1'b1: Receive FIFO is empty.
2	RO	0x1	tfe 1'b0: Transmit FIFO is not empty. 1'b1: Transmit FIFO is empty.
1	RO	0x0	tff 1'b0: Transmit FIFO is not full. 1'b1: Transmit FIFO is full.
0	RO	0x0	bsf When set, indicates that a serial transfer is in progress; when cleared, indicates that the SPI is idle or disabled. 1'b0: SPI is idle or disabled. 1'b1: SPI is actively transferring data.

SPI_IPR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ipr Interrupt Polarity Register. 1'b0: Active Interrupt Polarity Level is HIGH. 1'b1: Active Interrupt Polarity Level is LOW.

SPI_IMR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfim 1'b0: TX finish interrupt is masked. 1'b1: TX finish interrupt is not masked.
6	RW	0x0	sspim 1'b0: ss_in_n posedge interrupt is masked. 1'b1: ss_in_n posedge interrupt is not masked.
5	RW	0x0	toim 1'b0: SPI timeout interrupt is masked. 1'b1: SPI timeout interrupt is not masked.
4	RW	0x0	rffim 1'b0: spi_rxf_intr interrupt is masked. 1'b1: spi_rxf_intr interrupt is not masked.
3	RW	0x0	rfoim 1'b0: spi_rxo_intr interrupt is masked. 1'b1: spi_rxo_intr interrupt is not masked.
2	RW	0x0	rfuim 1'b0: spi_rxu_intr interrupt is masked. 1'b1: spi_rxu_intr interrupt is not masked.
1	RW	0x0	tfoim 1'b0: spi_txo_intr interrupt is masked. 1'b1: spi_txo_intr interrupt is not masked.
0	RW	0x0	tfeim 1'b0: spi_txe_intr interrupt is masked. 1'b1: spi_txe_intr interrupt is not masked.

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SPI_ISR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfis 1'b0: TX finish interrupt is not active after masking. 1'b1: TX finish interrupt is active after masking.
6	RW	0x0	sspis 1'b0: ss_in_n posedge interrupt is not active after masking. 1'b1: ss_in_n posedge interrupt is active after masking.
5	RW	0x0	tois 1'b0: spi timeout interrupt is not active after masking. 1'b1: spi timeout interrupt is active after masking.
4	RO	0x0	rffis 1'b0: spi_rxf_intr interrupt is not active after masking. 1'b1: spi_rxf_intr interrupt is full after masking.
3	RO	0x0	rfois 1'b0: spi_rxo_intr interrupt is not active after masking. 1'b1: spi_rxo_intr interrupt is active after masking.
2	RO	0x0	rfuis 1'b0: spi_rxu_intr interrupt is not active after masking. 1'b1: spi_rxu_intr interrupt is active after masking.
1	RO	0x0	tfois 1'b0: spi_txo_intr interrupt is not active after masking. 1'b1: spi_txo_intr interrupt is active after masking.
0	RO	0x0	tfeis 1'b0: spi_txe_intr interrupt is not active after masking. 1'b1: spi_txe_intr interrupt is active after masking.

SPI_RISR

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfris 1'b0: TX finish interrupt is not active prior to masking. 1'b1: TX finish interrupt is active prior to masking.
6	RW	0x0	sspris 1'b0: ss_in_n posedge interrupt is not active prior to masking. 1'b1: ss_in_n posedge interrupt is active prior to masking.
5	RW	0x0	toris 1'b0: spi_timeout interrupt is not active prior to masking. 1'b1: spi_timeout interrupt is active prior to masking.
4	RO	0x0	rffris 1'b0: spi_rxf_intr interrupt is not active prior to masking. 1'b1: spi_rxf_intr interrupt is full prior to masking.
3	RO	0x0	rforis 1'b0: spi_rxo_intr interrupt is not active prior to masking. 1'b1: spi_rxo_intr interrupt is active prior to masking.
2	RO	0x0	rfuris 1'b0: spi_rxu_intr interrupt is not active prior to masking. 1'b1: spi_rxu_intr interrupt is active prior to masking.
1	RO	0x0	tforis 1'b0: spi_txo_intr interrupt is not active prior to masking. 1'b1: spi_txo_intr interrupt is active prior to masking.

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Bit	Attr	Reset Value	Description
0	RO	0x1	tferis 1'b0: spi_txe_intr interrupt is not active prior to masking. 1'b1: spi_txe_intr interrupt is active prior to masking.

SPI_ICR

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	WO	0x0	ctxfi Write 1 to Clear TX finish Interrupt.
5	WO	0x0	csspi Write 1 to Clear ss_in_n posedge Interrupt.
4	WO	0x0	ctoi Write 1 to Clear Timeout Interrupt.
3	WO	0x0	ctfoi Write 1 to Clear Transmit FIFO Overflow Interrupt.
2	WO	0x0	crfoi Write 1 to Clear Receive FIFO Overflow Interrupt.
1	WO	0x0	crfui Write 1 to Clear Receive FIFO Underflow Interrupt.
0	WO	0x0	cci Write 1 to Clear Combined Interrupt.

SPI_DMACR

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	tde 1'b0: Transmit DMA disabled. 1'b1: Transmit DMA enabled.
0	RW	0x0	rde 1'b0: Receive DMA disabled. 1'b1: Receive DMA enabled.

SPI_DMATDLR

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	tdl This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and transmit DMA is enabled (DMACR[1] = 1).

SPI_DMARDLR

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rdl This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and receive DMA is enabled (DMACR[0]=1).

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SPI_VERSION

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00110002	version IP Version

SPI_TIMEOUT

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	toe Timeout Enable. 1'b0: Timeout counter is inactive. 1'b1: Timeout counter will be active after the first rising edge of sclk_in.
15:0	RW	0x0000	tov Timeout Threshold Value. If sclk_in keep inactive for a threshold time , timeout interrupt will be triggered .The timeout threshold time is TOV*pclk_period*16.

SPI_BYPASS

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	txcp TX Clock Polarity. This bit is only valid in bypass mode. 1'b0: TX logic use raw sclk_in. 1'b1: TX logic use inverted sclk_in.
3	RW	0x0	rxcp RX Clock Polarity. This bit is only valid in bypass mode. 1'b0: RX logic use raw sclk_in. 1'b1: RX logic use inverted sclk_in.
2	RW	0x0	end Endian Mode. This bit is only valid in bypass mode. 1'b0: Work in little endian mode. 1'b1: Work in big endian mode.
1	RW	0x0	fbm First Bit Mode. This bit is only valid in bypass mode. 1'b0: First bit is LSB. 1'b1: First bit is MSB.
0	RW	0x0	byen Bypass Enable. 1'b0: Normal mode. 1'b1: Bypass mode, SPI serial/parallel convert logic is drive by SCLK.

SPI_TXDR

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	WO	0x0000	txdr When it is written to, data are moved into the transmit FIFO.

SPI_RXDR

Address: **Operational Base** + offset (0x0800)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rxdr When the register is read, data in the receive FIFO is accessed.

30.5 Interface Description

Table 30-1 SPI0 interface description

Module Pin	I/O	Pad Name	IOMUX Setting
IOMUX0			
spi_sclk	I/O	SAI0_LRCK_M1/I2C3_SDA_M1/SPI0_CLK_M0/GPIO0_C7_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[15:12]=4'hb
spi_mosi	I/O	SAI0_SDI0_M1/PDM0_SDI0_M0/SPI0_MOSI_M0/GPIO0_D0_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[3:0]=4'hb
spi_miso	I/O	SAI0_SDI1_M1/SAI0_SDO3_M1/PDM0_SDI1_M0/SPI0_MISO_M0/GPIO0_D1_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[7:4]=4'hb
spi_csn0	I/O	SAI0_SCLK_M1/I2C3_SCL_M1/SPI0_CSN0_M0/GPIO0_C6_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[11:8]=4'hb
spi_csn1	I/O	PDM0_CLK1_M0/HDMI_TX_CEC_M1/SPI0_CSN1_M0/PWM0_CH1_M0/GPIO0_C3_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[15:12]=4'hb
IOMUX1			
spi_sclk	I/O	SDMMC0_CLK/FSPI1_CLK_M0/SAI3_SCLK_M3/TEST_CLK_OUT/UART5_TX_M2/I2C5_SCL_M0/SPI0_CLK_M1/I3C1_SDA_PU_M1/GPIO2_A5_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[7:4]=4'hc
spi_mosi	I/O	SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/CAN0_RX_M0/PWM2_CH2_M0/GPIO2_A0_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'hc
spi_miso	I/O	SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'hc
spi_csn0	I/O	SDMMC0_CMD/FSPI1_CSN0_M0/SAI3_SDO_M3/UART5_RX_M2/I2C5_SDA_M0/SPI0_CSN0_M1/PWM2_CH4_M0/GPIO2_A4_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[3:0]=4'hc
spi_csn1	I/O	SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[11:8]=4'hc
IOMUX2			
spi_sclk	I/O	EMMC_D7/SAI0_SDO0_M2/SAI3_SDI_M0/SPI0_CLK_M2/GPIO1_A7	TOP_IOC_GPIO1A_IOMUX_SEL_H[15:12]=4'h9

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		_u	
spi_mosi		EMMC_D5/SAI3_SCLK_M0/PDM0_SDI2_M1/SPI0_MOSI_M2/I2C9_SCL_M0/GPIO1_A5_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[7:4]=4'h9
spi_miso		EMMC_D6/SAI3_LRCK_M0/PDM0_CLK1_M1/SPI0_MISO_M2/I2C9_SDA_M0/GPIO1_A6_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[11:8]=4'h9
spi_csn0		EMMC_D4/SAI0_MCLK_M2/SAI3_MCLK_M0/SPI0_CSN0_M2/GPIO1_A4_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[3:0]=4'h9
spi_csn1		EMMC_STRB/SAI0_SDI0_M2/SAI3_SDO_M0/PDM0_SDI0_M1/SPI0_CSN1_M2/GPIO1_B2_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[11:8]=4'h9

Table 30-2 SPI1 interface description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
spi_sclk		ETH1_RXD2_M1/SDMMC1_D0_M0/SAI3_SCLK_M1/I2C9_SDA_M1/SPI1_CLK_M0/PCIE1_CLKREQN_M1/PWM1_CH0_M1/GPIO1_B4_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4'hb
spi_mosi		ETH1_RXD3_M1/SDMMC1_D1_M0/SAI3_LRCK_M1/I2C9_SCL_M1/SPI1_MOSI_M0/PWM1_CH1_M1/GPIO1_B5_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[7:4]=4'hb
spi_miso		ETH1_RXCLK_M1/SDMMC1_D2_M0/SAI3_SDO_M1/UART3_CTSN_M2/SPI1_MISO_M0/PCIE0_CLKREQN_M1/GPIO1_B6_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4'hb
spi_csn0		ETH1_TXD2_M1/SDMMC1_D3_M0/SAI3_SDI_M1/UART3_RTSN_M2/SPI1_CSN0_M0/GPIO1_B7_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4'hb
spi_csn1		ETH1_TXD3_M1/SDMMC1_CMD_M0/PDM0_SDI2_M2/UART3_TX_M2/SPI1_CSN1_M0/PWM0_CH0_M1/GPIO1_C0_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[3:0]=4'hb
IOMUX1			
spi_sclk		VI_CIF_D0/ETH1_TXCLK_M0/SAI2_SDI_M1/PDM1_CLK0_M0/UART11_RX_M1/SPI1_CLK_M1/PWM1_CH4_M2/GPIO2_C5_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[7:4]=4'ha
spi_mosi		VI_CIF_D3/ETH1_RXCLK_M0/ETH0_PPSTRIG_M1/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[11:8]=4'ha
spi_miso		VI_CIF_D2/ETH1_TXD2_M0/SAI2_LRCK_M1/PDM1_SDI3_M0/UART11_RTSN_M1/SPI1_MISO_M1/PWM0_CH0_M2/GPIO2_C3_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[15:12]=4'ha
spi_csn0		VI_CIF_D1/ETH1_TXD3_M0/SAI2_SDO_M1/PDM1_SDI0_M0/UART11_TX_M1/SPI1_CSN0_M1/PWM1_CH3_M2/GPIO2_C4_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[3:0]=4'ha
spi_csn1		VI_CIF_D4/ETH1_RXD3_M0/ETH0	TOP_IOC_GPIO2C_IOM

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		_PPSCLK_M1/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	UX_SEL_L[7:4]=4'ha
IOMUX2			
spi_sclk		VO_LCDC_D4/VO_EBC_SDDO4/SAI1_SCLK_M1/DSMC_DATA2/FLEXBUS1_D4/UART8_RTSN_M0/SPI1_CLK_M2/GPIO3_C7_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[15:12]=4'ha
spi_mosi		VO_LCDC_D5/VO_EBC_SDDO5/SAI1_LRCK_M1/DSMC_DATA3/FLEXBUS1_D5/UART8_TX_M0/SPI1_MOSI_M2/GPIO3_C6_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[11:8]=4'ha
spi_miso		VO_LCDC_D6/VO_EBC_SDDO6/SAI1_SDO0_M1/DSMC_DATA4/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4'ha
spi_csn0		VO_LCDC_D3/VO_EBC_SDDO3/SAI1_MCLK_M1/DSMC_DATA1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4'ha
spi_csn1		SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4'ha

Table 30-3 SPI2 interface description

Module Pin		**Pad Name**	**IOMUX Setting**
IOMUX0			
spi_sclk		SPI2_CLK_M0/I2C1_SCL_M0/GPIO0_B2_z	PMU0_IOC_GPIO0B_IOMUX_SEL_L[11:8]=4'h9
spi_mosi		SPI2_MOSI_M0/I2C1_SDA_M0/GPIO0_B3_z	PMU0_IOC_GPIO0B_IOMUX_SEL_L[15:12]=4'h9
spi_miso		SPI2_MISO_M0/I2C0_SDA_M0/GPIO0_B1_z	PMU0_IOC_GPIO0B_IOMUX_SEL_L[7:4]=4'h9
spi_csn0		AUPLL_CLK_IN_M1/SPI2_CSN0_M0/I2C0_SCL_M0/GPIO0_B0_z	PMU0_IOC_GPIO0B_IOMUX_SEL_L[3:0]=4'h9
spi_csn1		SDMMC0_DETN/SPI2_CSN1_M0/GPIO0_A7_u	PMU0_IOC_GPIO0A_IOMUX_SEL_H[15:12]=4'h9
IOMUX1			
spi_sclk		ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'hb

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spi_mosi		ETH1_TXD0_M1/FSPI1_D0_M1/UART4_TX_M1/UART2_RTSN_M0/SPI2_MOSI_M1/PCIE0_BUTTONRSTN/GPIO1_C4_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[3:0]=4'hb
spi_miso		ETH1_TXD1_M1/FSPI1_D1_M1/UART4_RX_M1/UART2_CTSN_M0/SPI2_MISO_M1/PCIE1_BUTTONRSTN/GPIO1_C5_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[7:4]=4'hb
spi_csn0		ETH1_PPSTRIG_M1/SDMMC1_DETN_M0/FSPI1_CSN0_M1/UART4_CTSN_M1/I2C6_SDA_M1/SPI2_CSN0_M1/GPIO1_C3_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[15:12]=4'hb
spi_csn1		ETH1_PPSCLK_M1/SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_CSN1_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[11:8]=4'hb
IOMUX2			
spi_sclk		VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0]=4'ha
spi_mosi		VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0]=4'ha
spi_miso		VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4]=4'ha
spi_csn0		VO_LCDC_D7/VO_EBC_SDDO7/SAI1_SDO1_M1/DSMC_DATA5/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/CAN0_TX_M3/GPIO3_C4_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4'ha
spi_csn1		VO_LCDC_D22/VO_EBC_GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[7:4]=4'ha

Table 30-4 SPI3 interface description

Module Pin		**Pad Name**	**IOMUX Setting**
IOMUX0			
spi_sclk		VI_CIF_HREF/ETH0_MDIO_M1/SAI3_SCLK_M2/UART3_TX_M0/SPI3_CLK_M0/I2C7_SCL_M1/GPIO3_A0_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'ha
spi_mosi		VI_CIF_VSYNC/ETH1_PPSTRIG_M0/ETH0_MDC_M1/SAI3_LRCK_M2	TOP_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'ha

		/UART3_RX_M0/SPI3_MOSI_M0/I2C7_SDA_M1/GPIO3_A1_d	
spi_miso		VI_CIF_CLKO/ETH1_PPSCLK_M0/ETH0_RXCTL_M1/SAI3_SDO_M2/SPDIF_RX1_M1/UART3_CTSN_M0/SPI3_MISO_M0/CAN1_TX_M3/MIPI_TE_M1/GPIO3_A2_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'ha
spi_csn0		VI_CIF_CLKI/ETH1_PTP_REFCLK_M0/ETH0_RXD1_M1/SAI3_SDI_M2/SPDIF_TX1_M1/UART3_RTSN_M0/SPI3_CSN0_M0/CAN1_RX_M3/GPIO3_A3_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[15:11]=4'ha
spi_csn1		CAM_CLK2_OUT_M1/ETH1_MCLK_M0/ETH_CLK0_25M_OUT_M1/SAI0_SDO3_M0/SPDIF_TX0_M2/UART9_CTSN_M0/SPI3_CSN1_M0/PWM2_CH7_M2/GPIO2_D7_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[15:12]=4'ha
IOMUX1			
spi_sclk		VO_LCDC_DEN/VO_EBC_SDLE/SAI1_SDI1_M1/DSMC_DATA0/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[3:0]=4'ha
spi_mosi		VO_LCDC_VSYNC/VO_EBC_SDCLK/SAI1_SDI3_M1/DSMC_CLKN/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:8]=4'ha
spi_miso		VO_LCDC_HSYNC/VO_EBC_GDCLK/SAI1_SDI2_M1/DSMC_CLKP/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[7:4]=4'ha
spi_csn0		VO_LCDC_D13/VO_EBC_SDDO13/ETH0_TXCLK_M0/DSMC_DQS1/FLEXBUS0_CLK/SPI3_CSN0_M1/PWM0_CH1_M3/GPIO3_B6_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'ha
spi_csn1		VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12]=4'ha
IOMUX2			
spi_sclk		SAI1_SDO0_M0/SAI4_SDI_M0/SPI3_CLK_M2/PWM2_CH6_M0/GPIO4_A7_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[15:12]=4'h9
spi_mosi		SAI4_SCLK_M0/PDM1_SDI3_M1/FLEXBUS0_D13_M1/SPI3_MOSI_M2/UART6_TX_M0/I2C4_SCL_M1/CAN0_TX_M2/GPIO4_A4_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[3:0]=4'h9
spi_miso		SAI4_LRCK_M0/PDM1_CLK0_M1/FLEXBUS0_D14_M1/SPI3_MISO_M2/UART6_RX_M0/I2C4_SDA_M1/CAN0_RX_M2/GPIO4_A6_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[11:8]=4'h9
spi_csn0		SAI1_SCLK_M0/FLEXBUS1_CSN_	TOP_IOC_GPIO4A_IOM

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		M4/SPI3_CSN0_M2/UART5_RTSN_M1/I2C2_SCL_M2/PWM2_CH4_M1/GPIO4_A3_d	UX_SEL_L[15:12]=4'h9
spi_csn1		SAI1_SDI0_M0/SAI4_SDO_M0/PDM1_SDI0_M1/SPI4_CSN0_M2/SPI3_CSN1_M2/PWM2_CH7_M0/GPIO4_B3_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'ha

Table 30-5 SPI4 interface description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
spi_sclk		SAI4_SCLK_M2/VP2_SYNC_OUT/I2C6_SDA_M3/SPI4_CLK_M0/CAN1_RX_M1/PWM2_CH3_M1/GPIO4_C7_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[15:12]=4'hc
spi_mosi		ISP_FLASH_TRIGOUT_M1/SAI4_SDO_M2/VP0_SYNC_OUT/SATA1_ACTLED_M1/I2C3_SDA_M3/SPI4_MOSI_M0/UART6_RX_M3/PWM2_CH5_M1/GPIO4_C5_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[7:4]=4'hc
spi_miso		SAI4_SDI_M2/VP1_SYNC_OUT/PCIE0_CLKREQN_M3/SATA0_ACTLED_M1/I2C6_SCL_M3/SPI4_MISO_M0/CAN1_TX_M1/PWM2_CH2_M1/GPIO4_C6_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[11:8]=4'hc
spi_csn0		ISP_PRELIGHT_TRIG_M1/SAI4_LRCK_M2/DP_HPDIN_M0/I2C3_SCL_M3/SPI4_CSN0_M0/UART6_TX_M3/PWM2_CH6_M1/GPIO4_C4_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[3:0]=4'hc
spi_csn1		DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[3:0]=4'hc
IOMUX1			
spi_sclk		VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[7:4]=4'ha
spi_mosi		VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12]=4'ha
spi_miso		VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8]=4'ha
spi_csn0		VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UA	TOP_IOC_GPIO_IOMUX_SEL_[]=4'h

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		RT10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	
spi_csn1		VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:8]=4'ha
IOMUX2			
spi_sclk		SAI1_SDO1_M0/SAI1_SDI3_M0/PDM1_CLK1_M1/FLEXBUS1_D13_M1/SPI4_CLK_M2/UART5_TX_M1/UART6_RTSN_M0/UART2_RTSN_M1/GPIO4_B0_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'h9
spi_mosi		SAI1_SDO2_M0/SAI1_SDI2_M0/PDM1_SDI2_M1/FLEXBUS1_D14_M1/SPI4_MOSI_M2/UART5_RX_M1/UART6_CTSN_M0/UART2_CTSN_M1/GPIO4_B1_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[7:4]=4'h9
spi_miso		SAI1_SDO3_M0/SAI1_SDI1_M0/PDM1_SDI1_M1/FLEXBUS1_D15_M1/SPI4_MISO_M2/MIPI_TE_M0/GPIO4_B2_d/PCIE1_PERSTN_M2/GPIO4_B2_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[11:8]=4'h9
spi_csn0		SAI1_SDI0_M0/SAI4_SDO_M0/PDM1_SDI0_M1/SPI4_CSN0_M2/SPI3_CSN1_M2/PWM2_CH7_M0/GPIO4_B3_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'h9
spi_csn1		SAI1_LRCK_M0/FLEXBUS1_D12_M1/SPI4_CSN1_M2/UART5_CTSN_M1/I2C2_SDA_M2/PCIE1_CLKREQN_M2/GPIO4_A5_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[7:4]=4'h9
IOMUX3			
spi_sclk		VI_CIF_D10/SDMMC1_CLK_M1/ETH0_TXCLK_M1/SAI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/PCIE1_CLKREQN_M0/GPIO2_B3_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4'ha
spi_mosi		VI_CIF_D9/SDMMC1_PWREN_M1/ETH0_TXD2_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/SATA0_ACTLED_M0/GPIO2_B4_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[3:0]=4'ha
spi_miso		VI_CIF_D8/SDMMC1_DETN_M1/ETH0_RXCLK_M1/SAI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/SATA1_ACTLED_M0/GPIO2_B5_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[7:4]=4'ha
spi_csn0		VI_CIF_D11/SDMMC1_CMD_M1/ETH0_TXD3_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCIE0_CLKREQN_M0/GPIO2_B2_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[11:8]=4'ha
spi_csn1		VI_CIF_D15/SDMMC1_D0_M1/ETH0_RXD0_M1/SAI0_SDO0_M0/UART8_TX_M1/SPI4_CSN1_M3/I2C	TOP_IOC_GPIO2A_IOMUX_SEL_H[11:8]=4'ha

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		4_SCL_M2/GPIO2_A6_d	

30.6 Application Notes

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as:

When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})

When SPI Controller works as slave, the F_{spi_clk}>= 6 × (maximum F_{sclk_in})

Master Transfer Flow

When configured as a serial-master device, the SPI initiates and controls all serial transfers. The serial bit-rate clock, generated and controlled by the SPI, is driven out on the sclk_out line. When the SPI is disabled (SPI_ENR = 0), no serial transfers can occur and sclk_out is held in "inactive" state, as defined by the serial protocol under which it operates.

Slave Transfer Flow

When the SPI is configured as a slave device, all serial transfers are initiated and controlled by the serial bus master.

When the SPI serial slave is selected during configuration, it enables its transmit data onto the serial bus. All data transfers to and from the serial slave are regulated on the serial clock line (sclk_in), driven from the serial-master device. Data are propagated from the serial slave on one edge of the serial clock line and sampled on the opposite edge.

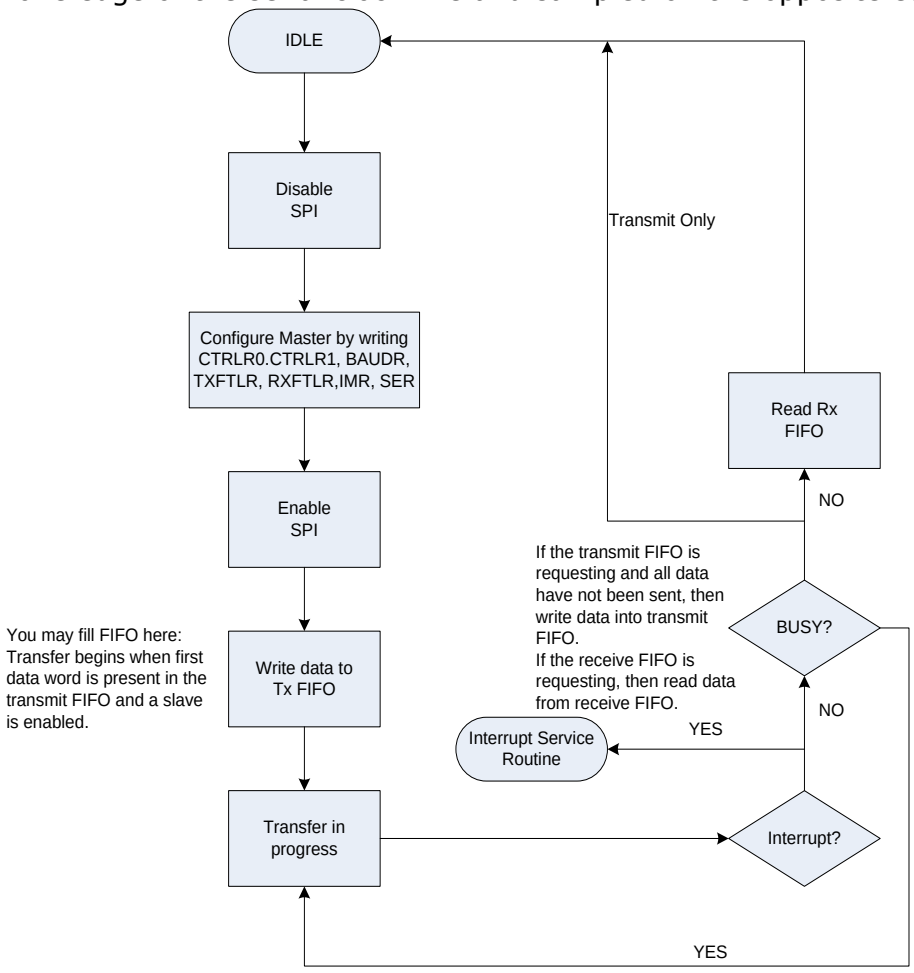

Fig. 30-7 SPI Master Transfer Flow Diagram

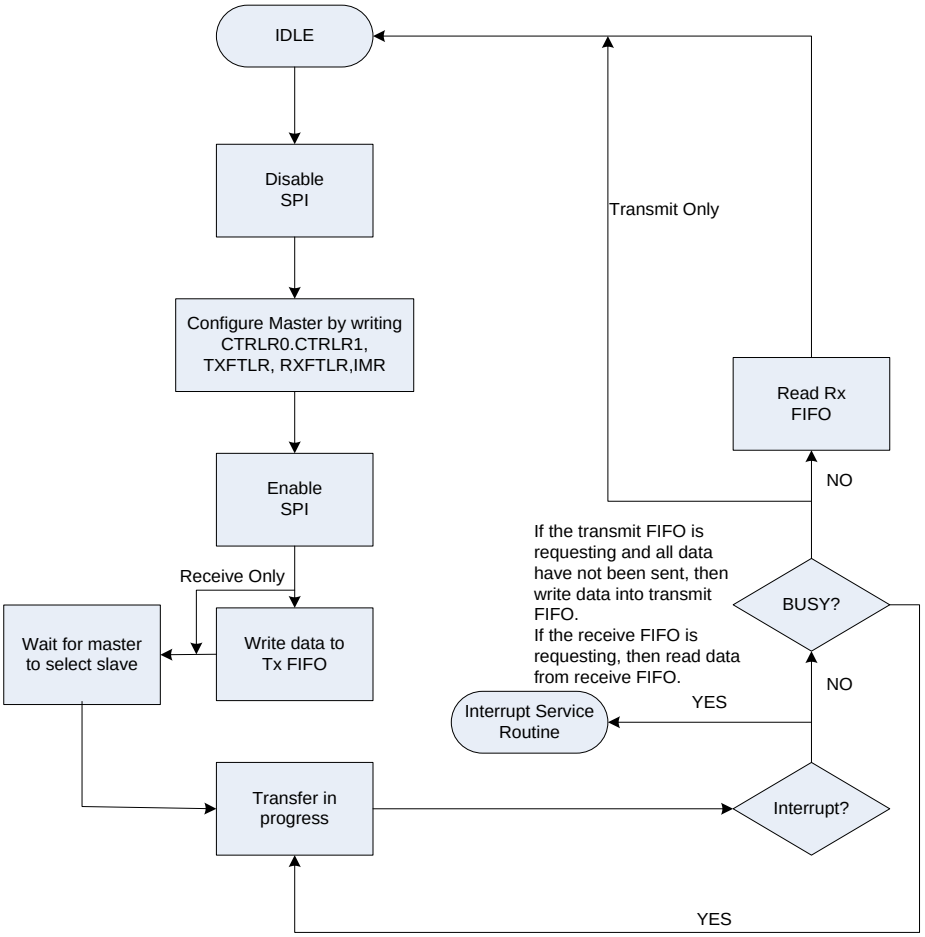

Fig. 30-8 SPI Slave Transfer Flow Diagram

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Chapter 31 Improved Inter-Integrated Circuit (I3C)

31.1 Overview

The Improved Inter-Integrated Circuit (I3C) is a two wired (SCL and SDA), bi-directional serial bus that provides an efficient and simple method of information exchange between devices. This I3C bus controller supports master mode acting as a bridge between AMBA bus and generic I3C bus system.

I3C Controller supports the following features:

- Support 2 independent I3C: I3C0 and I3C1, with 5 pairs of IO.
- Item Compatible with I2C-bus and I3C-bus
- AMBA AHB target interface
- Support master mode of I2C bus and I3C bus
- Software programmable clock frequency
- Built-in CMDFIFO, TXFIFO, RXFIFO, IBIFIFO, supports for one time to complete multiple TX and RX transmission. Depth for CMDFIFO is 11. Depth for TXFIFO/RXFIFO/IBIFIFO is 16.
- Support legacy I2C messaging mode
- Support Single Data Rate messaging (SDR)
- Support In-Band Interrupt(IBI)
- Support Hot-Join(HJ)
- Support Dynamic Address Assignment Mode□
- Support early termination of Read transmission
- Support Controller Clock Stalling in SDR Mode
- Support Target Reset without additional wires
- Support error detection and recovery methods for CE0, CE1, CE2
- Support Async Mode 0 for IBI
- Support clock stretching and wait state generation only on pure i2c bus
- Interrupt or DMA request or polling driven multiple bytes data transfer
- Filter out glitch on SCL and SDA
- Support up to 10 targets online

31.2 Block Diagram

The figure below is I3C controller architecture.

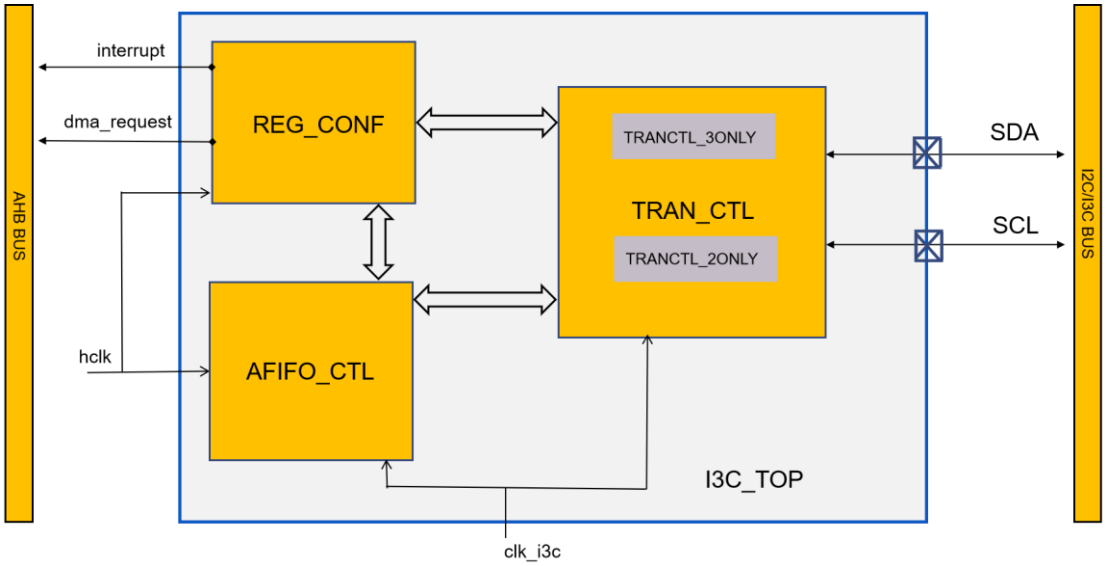

Fig. 31-1 I3C architecture

31.2.1 REG_CONF

REG_CONF module is used to control the I3C controller operation by the host with AHB interface. It implements the register set and the interrupt functionality. The REG_CONF component operates synchronously with hclk.

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31.2.2 TRAN_CTL

TRAN_CTL module implements the I3C controller operation for transmit data to and receive data from other I2C devices and I3C devices. The I3C controller controller operates synchronously with clk_i3c.

31.2.3 AFIFO_CTL

AFIFO_CTL module implements data interaction of internal MEMORY array and external transmission. The built-in FIFOs are asynchronous first-in-first-out modules.

31.2.4 I3C_TOP

I3C_TOP module is the top module of the I3C controller.

31.3 Function Description

This chapter provides a description about the functions and behavior under various conditions. The I3C controller supports only Controller function. It supports the I2C transmission and I3C transmission. The maximum clock frequency and transfer rate of I2C transmission can be up to 400Kbit/sec. The maximum clock frequency and transfer rate of I3C transmission is decided by the bus type. If the bus is a mixed slow bus, its clock frequency is same as the I2C transmission. If the bus is a mixed fast bus or i3c pure bus, it need to meet timing of SCL Clock High Period and SCL Clock Low Period of the protocol.
The operations of I3C controller is divided to 2 parts and described separately: initialization and controller mode programming.

31.3.1 Initialization

The I3C controller is based on AMBA AHB bus architecture and usually a part of SOC. So before I3C operates, some system setting and configuration must be conformed, which includes:

- I3C interrupt connection type: CPU interrupt scheme should be considered. If the I3C interrupt is connected to extra Interrupt Controller module, we need to decide the INTC vector.
- I3C Clock Rate: The I3C controller uses the AHB clock to configure controller and uses clk_i3c as the working clock. The correct register settings are subject to the system requirements.

31.3.2 Controller Mode Programming

- SCL Clock
  When it is I2C transmission on any bus, the SCL frequency is determined by CLKDIV_FM register.
  When it is I3C transmission on mixed slow bus, the SCL frequency is determined by CLKDIV_FM register.
  When it is I3C transmission on mixed fast bus or pure i3c bus, the SCL frequency is determined by both CLKDIV_PP register and CLKDIV_OD register. Specially, if it is mixed fast bus, the first transmission must be sending 7E/W address only and SCL must be divided by CLKDIV_FM with fm_start_en bit in MODULE_CTL register enable.
  The SCL frequency is calculated by the following formula:
  SCL HIGH Divisor = 4*(CLKDIVH + 1);
  SCL LOW Divisor = 4*(CLKDIVL + 1);
  clk_i3c = 100MHz~400MHz.
  SCL = clk_i3c/ (SCL HIGH Divisor +SCL LOW Divisor) .
  The value of CLKDIVH and CLKDIVL should meet the requirements of the agreement.
  Others, CLKSTALL_CONF_I3C register can be configured to hold SCL low before ACK bit

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and T-bit to meet the online timing for i3c transmission.
If this transmission uses CLKDIV_FM, then its time-related configuration is decided by TIME_CONF_FM register. Similarly, if this transmission uses CLKDIV_PP and CLKDIV_OD, its time-related configuration is decided by TIME_CONF_PPOD register.

- Data Receiver Register Access
  The number of bytes to be received from target is decided by byte_len bits of CMD. When the I3C controller receives data, these data will be filled into RXFIFO in the form of word. Note that the data of different CMDs will be divided into different words. Byte fills from high bit to low bit in the order of received bits. Word fills from high byte to low byte in the order of received bytes spelled in front. If the remaining data is less than 32 bits at the end, it will fill up 0 at high level.
  CPU and DMA can get the data from RXDATA FIFO. If you want the controller to receive over 16 words data in one transmission, you must get the data out in a timely manner.
  The default transfer is to use the CPU, if you want to use DMA, you need to configure the relevant registers.

- Transmit Transmitter Register
  The number of bytes to be transferred to target is decided by byte_len bits of CMD. Data to be transmitted are written to TXDATA FIFO by CPU or DMA. The controller transmits data from TXDATA FIFO byte by byte and will transmit bits from high bit to low bit of the lowest byte first.
  If you want the controller to transmit over 16 words data in one transmission, you must write data to TXFIFO in a timely manner.

- Command Set Register
  Data that be set into CMDFIFO decides the operation mode is read or write and decides the number of bytes will be transmitted on the SDA line. Also it decides how to react when NACK or other unexpected behaviour happens, continue or stop? Command execution in CMDFIFO order.

- In-Band Interrupt(IBI) Related Register
  If you want to response to the IBI request of target correctly, you must configure IBIMAP1-5 registers and enable ibi_ready bit in REG_READY_CONF register. Otherwise, the controller will NACK all IBI request. Some other IBI-related configurations are in the IBI_CONF register, including how to response to Hot-Join.

- Dynamic Address Assignment Related Register
  If you want to assign dynamic address to targets by send ENTDAA CCC, you must configure DEV_IDn_RR0(n from 1 to 10) registers. The target who wins the arbitration first will be assigned the DEV_ID1_RR0 address. You can get target's UID, BCR,DCR from DEV_IDn_RR1 and DEV_IDn_RR2 register(n from 1 to 10). You can also change the register used for the first assignment address by configuring the DAA_CONF register.

- Start Command
  After setting all the required registers, write 1 to REG_READY_CONF[0](note mask). Then write 1 to MODULE_CTL[0], the controller will send START command. And the controller will execute the commands in CMDFIFO in turn. When to STOP is decided by online status

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and your choices in command.

If a transmission has some special requirements, for example, if you want the SCL of START+ADDRESS is divided by CLKDIV_FM register, you should choose to write 1'b1 to MODULE_CTL[1].

- Force Stop Command

  When the controller is working and the user wants to stop the current transmission, then user can write 1 to MODULE_CTL[3], and the controller will send a STOP at the moment allowed.

- I2C/I3C Operation Mode

  There are six operation modes, and they are decided by CMDFIFO[10:8]. Two of the six mode belong to I2C.

  - When COMMAND[10:8] is 3'b100, it means that the controller wants to transmit data in i2c mode and the number of bytes is decided by COMMAND[29:20]. If target NACK address and the value of COMMAND[15] and COMMAND[19] are equal to 1, the controller will ignore this NACK and continue this transmission. Also, after finishing this command, controller will send RESTART and continue next command. Otherwise, the controller will send STOP.
  - When COMMAND[10:8] is 3'b101, it means that the controller wants to receive data in i2c mode. The response to last byte is decided by COMMAND[14].
  - When COMMAND[10:8] is 3'b000, it means that the controller wants to transmit data in i3c mode. The transmission process is similar to I2C TX. If target NACK address and the value of COMMAND[17] and COMMAND[19] are equal to 1, controller will ignore this NACK and continue this transmission. Otherwise, the controller will send STOP.
  - When COMMAND[10:8] is 3'b001, it means that the controller wants to receive data in i3c mode. The transmission process is similar to I2C RX. But if target send byte with T=0 before the last byte and the value of COMMAND[16] and COMMAND[19] are equal to 1, controller will ignore it and send RESTART to continue next command. Otherwise, it will send STOP.
  - When COMMAND[10:8] is 3'b010, it means receiving UID,BCR,DCR for ENTDAA procedure. The address must be 7E/R. After sending this address, the controller will trigger clock to receive 48 bit UID, 8 bit BCR and 8bit DCR. Then the controller transmit assigned dynamic address from DEV_IDn_RR0 to target. If target NACK this assigned dynamic address once, controller will retry this command. But if target NACK twice, controller will send STOP.
  - When COMMAND[10:8] is 3'b011, it means sending address only. If the address is 7E and target NACK it, controller will send STOP and the STOP will be HDR EXIT PATTERN. So the i3c_ack2nak bit must be 1'b0.

- Master Interrupt Condition

  There are 16 interrupt status recorded in INT_STATUS register related to master mode. INT_STATUS[19:16] mean the command ID stopped. INT_STATUS[27:24] mean the command ID that cause error first and the error includes target NACK address, target NACK TXDATA and target let T=0 before the last RXDATA byte.

  - Transmission finish interrupt (Bit 0): The bit is asserted after Controller send STOP.
  - target request START interrupt (Bit 1): The bit is asserted when target drives SDA line low on the idle bus and controller disable auto-IBI function.
  - IBI finished interrupt (Bit 2): The bit is asserted after controller finishing the whole IBI procedure.
  - I2C Mode own IBI interrupt(Bit 3): The bit is asserted when SDA online is different from what controller send during I2C ADDRESS procedure.
  - Data error interrupt(Bit 4): The bit is asserted when SDA online is different from what

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controller send during I3C TXDATA procedure and I2C TXDATA procedure.

- TXFIFO error interrupt (Bit 5): The bit is asserted when TXFIFO is empty, but controller still want to read data from it during I3C TX procedure.
- RXFIFO error interrupt (Bit 6): The bit is asserted when RXFIFO is full, but controller still want to write data to it during I3C RX procedure.
- IBIFIFO error interrupt (Bit 7): The bit is asserted when IBIFIFO is full, but controller still want to write data to it during I3C IBIRX procedure.
- Target hold SCL interrupt (Bit 8): The bit is asserted when target drives SCL LOW too long to exceed the value of slv_hold_scl_db when controller wants SCL HIGH on pure I2C bus. Others, the bit is asserted when target drives SCL LOW when controller wants SCL HIGH on pure I3C bus or mixed bus. The judgment time of the latter is 3/4 of controller's SCL_HIGH.
- ENTDAA NACK twice interrupt (Bit 9): The bit is asserted when target NACK the dynamic address been assigned twice during ENTDAA procedure.
- NACK address interrupt (Bit 10): The bit is asserted when target NACK address.
- Early TX or RX or IBIRX interrupt (Bit 11): The bit is asserted when target NACK TXDATA during I2C TX procedure or when target send byte with T=0 before the last byte during I3C RX procedure or I3C IBIRX procedure. Whether it is caused by monitor device, check bit[23].
- Hsize error interrupt(Bit 12): The bit is asserted when the number of RXFIFO/ IBIFIFO's byte left is less than hsize expects. Also this is used when the number of byte that need to be sent to TXFIFO is less than hsize expects. Check bit[30:28] for specific types.
- One command finish interrupt (Bit 13): The bit is asserted when one command finished.
- Timeout for I2C interrupt (Bit 14): The bit is asserted when the number cycles that controller hold SCL is over wait_thld_i2c.
- FIFO need CPU interrupt (Bit 15): TXFIFO or RXFIFO or IBIFIFO need CPU to get or send. Check bit[22:20] for specific types.

- I2C/I3C controller data transfer waveform
  - Bit transferring
    - Data Validity

      The SDA line must be stable during the high period of SCL, and the data on SDA line can only be changed when SCL is in low state.

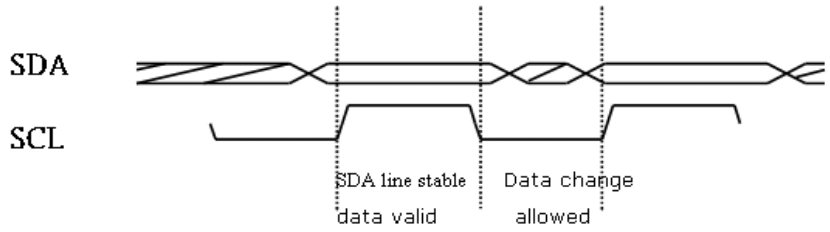

Fig. 31-2 I2C/I3C DATA Validity

    - START and STOP conditions

      START condition occurs when SDA goes low while SCL is in high period. Normal STOP condition is generated when SDA line goes high while SCL is in high state.

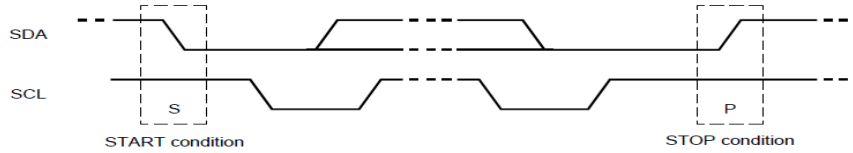

Fig. 31-3 I2C/I3C Start and stop conditions

Special STOP such as HDR Exit Pattern and Target Reset Pattern is different from normal STOP. The Target Reset Pattern begins with fourteen SDA transitions while SCL is kept Low, and ends with a Repeated START followed by a STOP which triggers the actual Reset action. The HDR Exit Pattern begins with seven SDA transitions while SCL is kept Low, and ends with a STOP when SCL is in high state.

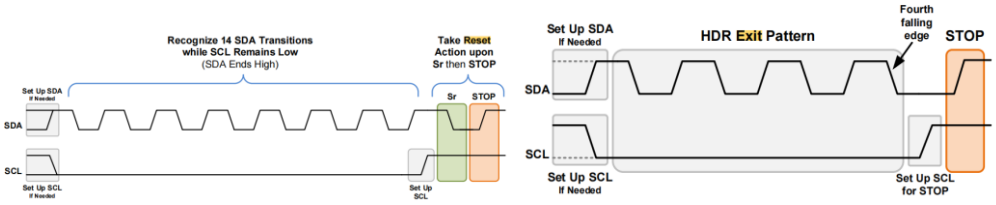

Fig. 31-4 I3C Target Reset Pattern and HDR Exit Pattern

In order to correctly complete the target reset function, the user is required to pay attention to the configuration of the command, avoid being stopped in advance and failing to reset the target.

- I2C Data transfer
  - Byte transfer

    The transmitter on I2C bus might initiate multi byte to transfer to a receiver. The transfer starts with a START command followed by target's address and ends in a STOP command. After each byte transfer, the receiver must reply an ACK or NACK to transmitter.

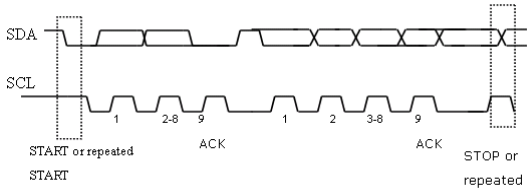

Fig. 31-5 I2C byte transfer

  - Acknowledge

    After a byte of data transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK or NACK signal on SDA line, if the receiver pulls SDA line to low, it means "ACK", on the contrary, it's "NOT ACK".

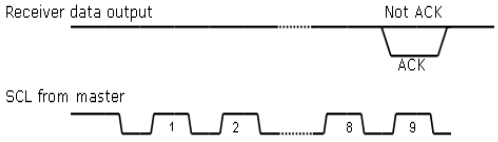

Fig. 31-6 I2C byte transfer with Acknowledge

- I3C Data transfer
  - Byte transfer

    Byte transfer in I3C SDR Mode is similar to I2C mode. The difference is in the following sections: behavior at moment C9, processing of I3C target In-

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Band interrupt request and bus initialization sequence with Dynamic Address Assignment.

- Acknowledge or Transition bit

  After address transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK or NACK signal on SDA line, if the receiver pulls SDA line to low, it means "ACK", on the contrary, it's "NOT ACK".

  After a byte of write data transferred (clocks labeled as 1~8), the ninth bit of data is referred to as the T-Bit, Parity, sent by the controller, calculated using odd parity. Parity can help in detecting noise-caused errors on the line. The value of this Parity bit shall be the XOR of the 8 Data bits with 1, i.e.: XOR({Data[7:0], 1'b1})..

  After a byte of read data transferring (clocks labeled as 1~8), the ninth bit of data is referred to as the T-Bit. If T=1, it means target still has byte to transfer. If T=0, it means target has no byte to transfer. If T=1 and the I3C Controller wants to abort the message, then it shall drive SDA Low after the rising edge of SCL, thereby terminating the message with a Repeated START, as shown in figure 7. This also applies to IBI read data.

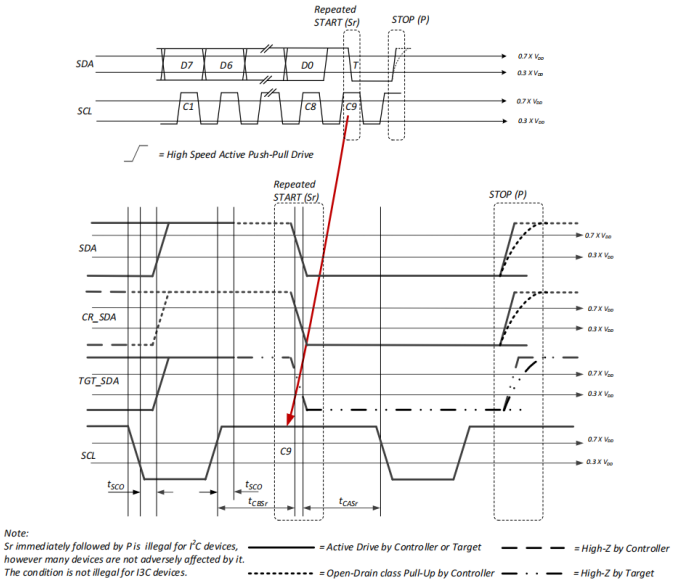

Fig. 31-7 T-bit equal to 1 while master end read with Repeat Start

- Data During Dynamic Address Assignment transmission

  During ENTDAA read procedure, the 48-bits Provisioned ID shall be transferred continuously, starting with the most significant bit (bit[47]), with no delimitation or ACK/NACK pulse. Then BCR and DCR shall be transferred in the same way. For the winning Device, the Controller shall drive the 7-bit Dynamic Address, followed by a parity bit (PAR), which is calculated as odd parity. The value of this Parity bit is the inverse of the XOR of the 7 bits, i.e.:~XOR(dynamic_address[7:1]).

  Dynamic Address Assignment transmission is shown in figure 8.

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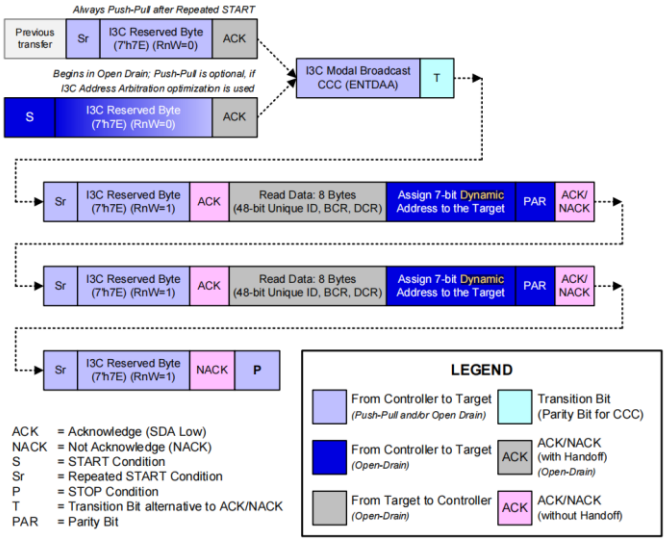

Fig. 31-8 Dynamic Address Assignment transmission

- Address during IBI/HJ/CR

  In order to request an interrupt, an I3C Target shall emit its address into the arbitrated address header following a START (but not following a Repeated START). If the controller lost arbitration, it will give up the drive during the first 8 SCL clock of address procedure and the 9th clock will become up to the controller to decide whether or not to ACK target requests. If ACK, the controller then must receive data from this target.

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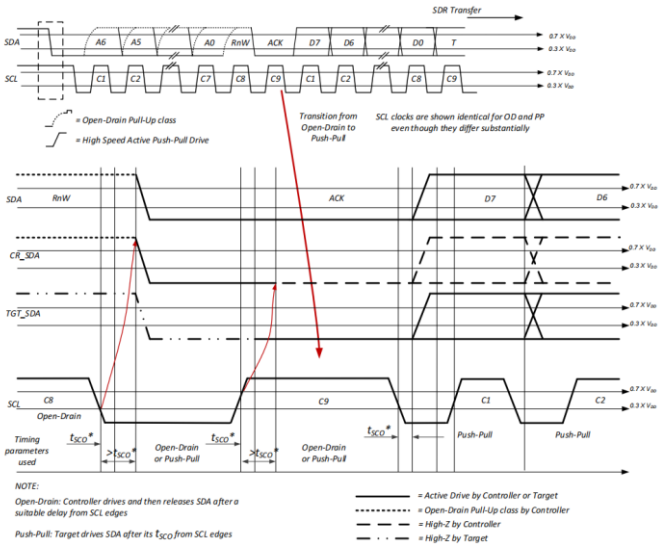

Fig. 31-9 Controller ACK IBI

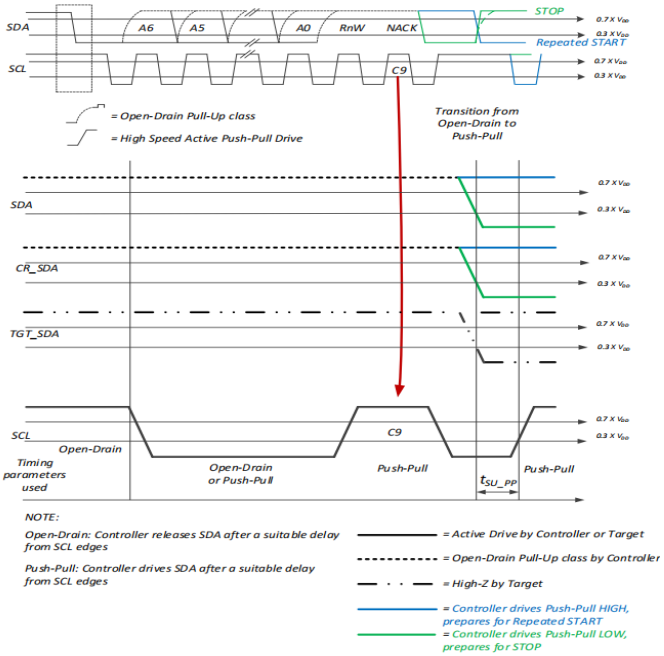

Fig. 31-10 Controller NACK IBI

31.4 Register Description

31.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
RKI3C0	0x2ABE0000
RKI3C1	0x2ABF0000

31.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKI3C_MODULE_CTL	0x0000	W	0x00000000	Module control register

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Name	Offset	Size	Reset Value	Description
RKI3C_MODULE_CONF	0x0004	W	0x00000020	Module information configure register
RKI3C_TOUT_CONF_I3C	0x0008	W	0x00004E20	I3C timeout information configure register
RKI3C_CLKSTALL_CONF_I3C	0x000C	W	0x00000000	I3C clock stall information configure register
RKI3C_SLVHOLD_SCL_CONF	0x0010	W	0x00001011	I2C target hold SCL information configure register
RKI3C_WAIT_THLD_I2C	0x0014	W	0x00004E20	Wait time threshold during I2C transaction register
RKI3C_CMD	0x0020	W	0x00000000	Command register, only support 11 command one time
RKI3C_TXDATA	0x0024	W	0x00000000	TXDATA Register
RKI3C_RXDATA	0x0028	W	0x00000000	RXDATA register
RKI3C_IBIDATA	0x002C	W	0x00000000	IBIDATA register
RKI3C_FIFO_TRIG_DMA	0x0030	W	0x00000000	Number of FIFO trigger one time by DMA Register
RKI3C_TXFIFO_NUM_DMA	0x0034	W	0x00000000	TXFIFO data number by DMA configure register
RKI3C_RXFIFO_NUM_DMA	0x0038	W	0x00000000	RXFIFO data number by DMA configure register
RKI3C_IBIFIFO_NUM_DMA	0x003C	W	0x00000000	IBIFIFO data number by DMA configure register
RKI3C_FIFO_TRIG_CPU	0x0040	W	0x00000000	Number of FIFO trigger one time by CPU register
RKI3C_TXFIFO_NUM_CPU	0x0044	W	0x00000000	TXFIFO data number by CPU configure register
RKI3C_RXFIFO_NUM_CPU	0x0048	W	0x00000000	RXFIFO data number by CPU configure register
RKI3C_IBIFIFO_NUM_CPU	0x004C	W	0x00000000	IBIFIFO data number by CPU configure register
RKI3C_RKDMA_CONF	0x0050	W	0x00000000	RKDMA type configure register
RKI3C_CLKDIV_OD	0x0054	W	0x000A0004	Clock divider register for Open-Drain mode
RKI3C_CLKDIV_PP	0x0058	W	0x00040004	Clock divider register for Push-Pull mode
RKI3C_CLKDIV_FM	0x005C	W	0x003E003E	Clock divider register for Fast-Mode mode
RKI3C_TIME_CONF_PPOD	0x0060	W	0x00000215	I3C Fast-Mode time information configure register
RKI3C_TIME_CONF_FM	0x0064	W	0x00004505	I2C mode and I3C Slow-Mode time information configure register
RKI3C_DAA_CONF	0x0068	W	0x00000000	Assigned dynamic address information configure register
RKI3C_BUS_FREE_CONF	0x006C	W	0x00000104	Bus free configure register
RKI3C_BUS_FLT_CONF	0x0070	W	0x00000000	I3C filter information configure register
RKI3C_REG_READY_CONF	0x0074	W	0x00000000	Register ready configure register
RKI3C_FLUSH_CTL	0x0078	W	0x00000000	Flush control register
RKI3C_INT_EN	0x0090	W	0x00000000	Interrupt status register
RKI3C_INT_STATUS	0x0094	W	0x00000000	Interrupt status register
RKI3C_IBI_CONF	0x009C	W	0x00000002	IBI-related items configure register

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Name	Offset	Size	Reset Value	Description
RKI3C_IBI_MAP1	0x0100	W	0x00000000	Target IBI information register 1
RKI3C_IBI_MAP2	0x0104	W	0x00000000	Target IBI information register 2
RKI3C_IBI_MAP3	0x0108	W	0x00000000	Target IBI information register 3
RKI3C_IBI_MAP4	0x010C	W	0x00000000	Target IBI information register 4
RKI3C_IBI_MAP5	0x0110	W	0x00000000	Target IBI information register 5
RKI3C_DEV_ID1_RR0	0x0120	W	0x00000000	I3C device1 register0. DEV_IDn_RR0 = 0x0120 + 16*n, n range from 1 to 10
RKI3C_DEV_ID1_RR1	0x0124	W	0x00000000	I3C device1 register1. DEV_IDn_RR1 = 0x0124 + 16*n, n range from 1 to 10
RKI3C_DEV_ID1_RR2	0x0128	W	0x00000000	I3C device1 register2. DEV_IDn_RR2 = 0x0128 + 16*n, n range from 1 to 10
RKI3C_VERSION	0x0200	W	0x00000005	Version of I3C controller
RKI3C_CMD1_STATUS	0x0230	W	0x00000000	Command1 status register. CMDn_STATUS = 0x0230 + 4*n, n range from 1 to 11
RKI3C_ASYNC_REF_CNT	0x0260	W	0x00000000	Async mode 0 timestamp interpolation register
RKI3C_FIFO_STATUS	0x0264	W	0x000010AA	FIFO status register
RKI3C_IBI_STATUS	0x0268	W	0x00000000	IBI status register
RKI3C_DAA_STATUS	0x026C	W	0x00000000	Dynamic address assignment status register
RKI3C_RXDAT_OVER	0x0270	W	0x00000000	RXDATA overflow register
RKI3C_IBIRX_OVER	0x0274	W	0x00000000	IBIDATA overflow register
RKI3C_LINE_STATUS	0x0278	W	0x00000000	SCL/SDA line status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

31.4.3 Detail Registers Description

RKI3C_MODULE_CTL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sreset 1'b1: Soft reset enable When this bit is written to 1'b1, it soft reset module. After finishing, it self-clear.
4	RW	0x0	retry_en 1'b1: Retry enable When this bit is written to 1, module will generate start signal. After finishing this transaction, it self-clear. Also it can be cleared with sreset. The difference between start and retry is whether the command needs to be replaced. Retry can only be used when the last transfer is stopped by IBI or by slave's NACK to address.
3	RW	0x0	force_stop 1'b1: Force stop enable If this bit's value is 1, immediately enter the STOP state on any allowed node. And, for ADDR and DATA status, the current byte needs to be completed. After finishing this transaction, it self-clear. Also it can be cleared by sreset.

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Bit	Attr	Reset Value	Description
2	RW	0x0	ely_monitor_start_en 1'b1: Start enable with enabling early termination capability of monitoring devices When this bit is written to 1'b1, it raises a START. During this transaction, a Monitoring Device can request early termination of a Read transfer at T-bit. After finishing this transaction, it self-clear. Also it can be cleared by sreset.
1	RW	0x0	fm_start_en 1'b1: Start enable in FM speed When this bit is written to 1'b1, it raises a START. This is used to send START in FM mode speed after initialization to enable i2c legacy devices' spike filter. After finishing this transaction, it self-clear. Also it can be cleared by sreset.
0	RW	0x0	start_en 1'b1: Start enable When this bit is written to 1, module will generate start signal. After finishing this transaction, it self-clear. Also it can be cleared by sreset.

RKI3C_MODULE_CONF

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	mask 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	i2c_clkgate_en 1'b0: Disable 1'b1: Enable Use to clock gate tranctl_2only module.
13	RW	0x0	i3c_clkgate_en 1'b0: Disable 1'b1: Enable Use to clock gate tranctl_3only module.
12	RW	0x0	all_clkgate_en 1'b0: Disable 1'b1: Enable Use to clock gate tranctl module.
11	RW	0x0	slverr_hdscl_odpp 1'b0: when error happens, change i3c scl_oe to 0, which means od 1'b1: when error happens, maintain i3c scl_oe 1, which means pp Use for not pure i2c bus.
10:9	RO	0x0	reserved
8	RW	0x0	speci_stop_athigh 1'b0: SCL LOW 1'b1: SCL HIGH The value determines HDR EXIT PATTERN and TARGET RESET PATTERN's SDA pull up at SCL HIGH or SCL LOW.
7	RW	0x0	i3c_stop_ppod 1'b0: I3C STOP's HIGH is calculated by CLKDIV_PP 1'b1: I3C STOP's HIGH is calculated by CLKDIV_OD

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Bit	Attr	Reset Value	Description
6	RW	0x0	i3c_addrack_ppod_rest 1'b0: I3C ADDR ACK bit's LOW&HIGH is calculated by CLKDIV_PP 1'b1: I3C ADDR ACK bit's LOW&HIGH is calculated by CLKDIV_OD Use for I3C ADDR ACK bit after RESTART.
5	RW	0x1	i3c_addrack_ppod_start 1'b0: I3C ADDR ACK bit's HIGH is calculated by CLKDIV_PP 1'b1: I3C ADDR ACK bit's HIGH is calculated by CLKDIV_OD Use for I3C ADDR ACK bit after START.
4	RW	0x0	daa_oddiv_en 1'b0: ENTDAA procedure's RESTART+ADDR's SCL is calculated by CLKDIV_PP 1'b1: ENTDAA procedure's RESTART+ADDR's SCL is calculated by CLKDIV_OD
3	RO	0x0	reserved
2:1	RW	0x0	bus_type 2'b00: I3c pure bus (I3C mode use CLKDIVPP and CLKDIVOD) 2'b01: I3c mixed fast bus(both I3C Devices and Legacy I2C Devices with 50ns Spike Filter) (I3C mode use CLKDIVPP and CLKDIVOD, I2C mode use CLKDIVFM) 2'b10: I3c mixed slow bus(both I3C Devices and Legacy I2C Devices without 50ns Spike Filter) (both I3C mode and I2C mode use CLKDIVFM) 2'b11: I2c pure bus (I2C mode use CLKDIVFM) Slave hold SCL LOW can only be perimitted on pure i2c bus or smbus.
0	RW	0x0	module_en 1'b1: Module enable Only when this is equal to 1'b1, tranctl module will work.

RKI3C_TOUT_CONF_I3C

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	i3c_over_stop_disable 1'b0: Enable 1'b1: Disable If enable, when timeout happens, the controller will undo hold scl and then stop. If disable, the controller will hold scl until fifo meet requirement.
23:0	RW	0x004e20	tout_cycle T = tout_cycle * Tclk_i3c This is used for timeout in i3c mode. The original SCL low time plus the tout_cycle time cannot exceed activity interval, 1us for activity S0, 100us for activity for S1. For example, when RXFIFO is full, before next rxfifo_wr, controller hold scl low at most tout_cycle, if RXFIFO is still full, cancel holdscl to meet timing. The default value is used for 200MHz and 100us.

RKI3C_CLKSTALL_CONF_I3C

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:8	RW	0x0000	clkstall_num T = clkstall_num * Tclk_i3c controller SCL stall low for clkstall_num cycles
7:6	RO	0x0	reserved
5	RW	0x0	daa_before_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	rdtbit_after_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	rdtbit_before_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	wrtbit_before_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	ack_before_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	is_clkstall 1'b0: Disable 1'b1: Enable

RKI3C_SLVHOLD_SCL_CONF

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000808	slv_hold_scl_db T = slv_hold_scl_db)* Tclk_i3c. If slave hold scl over this threshold and the bus type is pure i2c bus, the controller will rise slavehdscl_irqpd.
0	RW	0x1	h0_check_scl 1'b0: Check if SCL has been pull down by slave at the whole SCL_HIGH 1'b1: Check if SCL has been pull down by slave only at the scl_h0 of SCL_HIGH

RKI3C_WAIT_THLD_I2C

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x004e20	wait_thld_i2c When controller hold scl low during i2c transaction over this wait_thld_i2c value, controller will rise interrupt to remind.

RKI3C_CMD

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	WO	0x000	byte_len Byte length for this command's transfer
19	WO	0x0	ack2next 1'b0: Stop 1'b1: Continue RESTART

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Bit	Attr	Reset Value	Description
18	WO	0x0	i3c_end2ibi This determines action after finishing ibi transmission. 1'b0: Stop 1'b1: Continue
17	WO	0x0	i3c_ack2nak If it is broadcast address 7'h7E, this value must 1'b0 1'b0: Stop 1'b1: Ignore
16	WO	0x0	i3c_ack2early This bit is asserted to how to handle when slave send T=0 before the last byte controller wants. 1'b0: Stop 1'b1: Ignore
15	WO	0x0	i2c_ack2nak 1'b0: Stop 1'b1: Ignore this NACK If slave NACK i2c tx command and resp is ignore, finish this tx transaction. If slave NACK i2c rx command and resp is ignore, restart or stop is decided by ack2next bit.
14	WO	0x0	i2c_ack2last 1'b0: ACK 1'b1: NACK Last byte acknowledge control in i2c master receive mode.
13	WO	0x0	is_reset 1'b0: Not use target reset pattern 1'b1: Use target reset pattern When the value is 1'b1, then if stop at this command, this STOP will use target reset pattern.
12	WO	0x0	is_hdrexit 1'b0: Not use HDR Exit Pattern 1'b1: Use HDR Exit Pattern When the value is 1'b1,then if stop at this command, this STOP will use HDR Exit pattern.
11	WO	0x0	is_sync_dt_tran When this bit is equal to 1, it means this CMD trans DT Sub-Command Byte and its delay time value. The delay time value(tx's second byte) will be replace by inner calculated delay time value
10:8	WO	0x0	tran_mode 3'b000: I3c SDR transmit transfer(address + Tx data) 3'b001: I3c SDR receive transfer(address + Rx data) 3'b010: I3c ENTDAA procedure 3'b011: I3c address only(Rnw bit must be write) 3'b100: I2c/smbus transmit 3'b101: I2c/smbus receiv0 Others: Reserved
7:1	WO	0x00	txaddr Address of the accessed slave
0	WO	0x0	rnw 1'b0: Write 1'b1: Read

RKI3C_TXDATA

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	txdata 32 bits data to be transmitted during I2C/I3C TX procedure

RKI3C_RXDATA

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata 32 bits data received during I2C/I3C RX procedure

RKI3C_IBIDATA

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ibidata 32 bits data received during IBI procedure

RKI3C_FIFO_TRIG_DMA

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	WO	0x0	tx_start_thld_mask 1'b1: Write access enable
27:24	WO	0x0	ibififo_trig_mask 1'b1: Write access enable
23:20	WO	0x0	rxfifo_trig_mask 1'b1: Write access enable
19:16	WO	0x0	txfifo_trig_mask 1'b1: Write access enable
15:12	RW	0x0	tx_start_thld If txfifo_num_dma is not equal to zero, only when the number of data that DMA has sent to TXFIFO is bigger than tx_start_thld, the controller will send START.
11:8	RW	0x0	ibififo_trig This value means how many words the DMA moves at a time from IBIFIFO. If ibififo_trig=0, it means DMA moves one word at a time. If ibififo_trig=4'f, it means DMA moves 16 word at a time.
7:4	RW	0x0	rxfifo_trig This value means how many words the DMA moves at a time from RXFIFO. If rxfifo_trig=0, it means DMA moves one word at a time. If rxfifo_trig=4'f, it means DMA moves 16 word at a time.
3:0	RW	0x0	txfifo_trig This value means how many words the DMA moves at a time to TXFIFO. If txfifo_trig=0, it means DMA moves one word at a time. If txfifo_trig=4'f, it means DMA moves 16 word at a time.

RKI3C_TXFIFO_NUM_DMA

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dma_txcnt The value means how many word have been sent to TXFIFO by DMA. It will be cleared when write this register.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	dma_txnum Num of data will be sent by DMA to TXFIFO(unit: 32bits) If dma_txnum=0, it means no data need to be send to TXFIFO by DMA. max='h3ff(byte)*11(cmd num) < 'h1000(byte)

RKI3C_RXFIFO_NUM_DMA

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dma_rxcnt The value means how many word have been received from TXFIFO by DMA, zero data as a supplement is not included. It will be cleared when write this register.
15:0	RW	0x0000	dma_rxnum Num of data will be moved out by DMA from RXFIFO(unit: 32bits) If dma_rxnum=0, it means no data need to be received from RXFIFO by DMA. max='h3ff(byte)*11(cmd num) < 'h1000(byte)

RKI3C_IBIFIFO_NUM_DMA

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RO	0x00	dma_ibicnt The value means how many word have been received from IBIFIFO by DMA. It will be cleared when write this register.
15:7	RO	0x000	reserved
6:0	RW	0x00	dma_ibinum Num of data will be moved out by DMA from IBIFIFO(unit: 32bits, word) If dma_ibinum=0, it means no data need to be received from IBIFIFO by DMA. max ibipllen = 'h7f(byte)<'h40(word)

RKI3C_FIFO_TRIG_CPU

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	WO	0x000	mask 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x0	ibififo_trig_cpu When IBIFIFO's space to empty is greater than this value and word have been received from IBIFIFO is less than ibififo_num_cpu, the controller will trigger interrupt. (unit word)
7:4	RW	0x0	rxfifo_trig_cpu When RXFIFO's space to empty is greater than this value and word have been received from RXFIFO is less than rxfifo_num_cpu, the controller will trigger interrupt. (unit word)
3:0	RW	0x0	txfifo_trig_cpu When TXFIFO's space to full is greater than this value and words have been transmitted to TXFIFO is less than txfifo_num_cpu, the controller will trigger interrupt. (unit word)

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RKI3C_TXFIFO_NUM_CPU

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	cpu_txcnt The value means how many word have been sent to TXFIFO by CPU after write this regitser. It will be cleared when write this register.
15:0	RW	0x0000	cpu_txnum Num of data will be sent by CPU to TXFIFO after write this regitser(unit: 32bits).

RKI3C_RXFIFO_NUM_CPU

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	cpu_rxcnt The value means how many word have been received from TXFIFO by CPU. It will be cleared when write this register.
15:0	RW	0x0000	cpu_rxnum Num of data will be moved out by CPU from RXFIFO after write this regitser(unit: 32bits).

RKI3C_IBIFIFO_NUM_CPU

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	cpu_rxcnt The value means how many word have been received from TXFIFO by CPU. It will be cleared when write this register.
15:0	RW	0x0000	cpu_rxnum Num of data will be moved out by CPU from IBIFIFO after write this regitser(unit: 32bits).

RKI3C_RKDMA_CONF

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	rx_pad_en When i3c slave let T=0 before expected, and you still want to get enough rxdata, then enable this bit, the controller will send you enough data by supplementing zero.
11	RO	0x0	reserved
10	RW	0x0	tx_hsize_err_irqen This is used when the number of byte that need to be sent to TXFIFO is less than hsize expects, whether or not you want the controller to rise interrupt.
9	RW	0x0	ibi_hsize_err_irqen This is used when the number of IBIFIFO's byte left is less than hsize expects, whether or not you want the controller to rise interrupt.
8	RW	0x0	rx_hsize_err_irqen This is used when the number of RXFIFO's byte left is less than hsize expects, whether or not you want the controller to rise interrupt.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	tx_resp_error_en 1'b0: Disbale 1'b1: Enable This is used when the number of byte that need to be sent to TXFIFO is less than hsize expects, whether or not you want the controller to send resp error for the ahb bus.
5	RW	0x0	ibi_resp_error_en 1'b0: Disbale 1'b1: Enable This is used when the number of IBIFIFO's byte left is less than hsize expects, whether or not you want the controller to send resp error for the ahb bus.
4	RW	0x0	rx_resp_error_en 1'b0: Disbale 1'b1: Enable This is used when the number of RXFIFO's byte left is less than hsize expects, whether or not you want the controller to send resp error for the ahb bus.
3	RW	0x0	nordma_tx_choice_en 1'b0: DMA disable to trans data to TXFIFO by CPU 1'b1: Nomal DMA enbale to trans data to TXFIFO by DMA
2	RW	0x0	nordma_ibi_choice_en 1'b0: DMA disable to get data from IBIFIFO by CPU 1'b1: Nomal DMA enbale to get data from IBIFIFO by DMA
1	RW	0x0	nordma_rx_choice_en 1'b0: DMA disable to get data from RXFIFO by CPU 1'b1: Nomal DMA enbale to get data from RXFIFO by DMA
0	RO	0x0	reserved

RKI3C_CLKDIV_OD

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x000a	clkdivl_od SCL low level clock count in open-drain timing mode for I3C target on I3C pure bus or I3C mixed fast bus. T(SCL_LOW) = Tclk_i3c * (clkdivl_od + 1) * 4
15:0	RW	0x0004	clkdivh_od SCL high level clock count in open-drain timing mode for I3C target on I3C pure bus or I3C mixed fast bus. T(SCL_HIGH) = Tclk_i3c * (clkdivh_od + 1) * 4

RKI3C_CLKDIV_PP

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	clkdivl_pp SCL low level clock count in push-pull timing mode for I3C target on I3C pure bus or I3C mixed fast bus. T(SCL_LOW) = Tclk_i3c * (clkdivl_pp + 1) * 4
15:0	RW	0x0004	clkdivh_pp SCL high level clock count in push-pull timing mode for I3C target on I3C pure bus or I3C mixed fast bus. T(SCL_HIGH) = Tclk_i3c * (clkdivh_pp + 1) * 4

RKI3C_CLKDIV_FM

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x003e	clkdivl_fm SCL low level clock count when communicating with i3c device on I3C mixed slow bus or i2c legancy device. Also it will be used for first broadcast address on I3C mixed fast bus. T(SCL_LOW) = Tclk_i3c * (clkdivl_fm + 1) * 4
15:0	RW	0x003e	clkdivh_fm SCL high level clock count when communicating with i3c device on I3C mixed slow bus or i2c legancy device. Also it will be used for first broadcast address on I3C mixed fast bus. T(SCL_HIGH) = Tclk_i3c * (clkdivh_fm+ 1) * 4

RKI3C_TIME_CONF_PPOD

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	mask 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x1	i3c_speci_stopclk_pp Used to config each sda high or low duration when using hdr exit pattern/target reset pattern 1'bn: T= (n + 1) * T(SCL_LOW). Note: 0 <= n <= 1 T(SCL_LOW) is calculated by CLK_DIV_PP when bus type is i3c pure bus or i3c fast bus.
8	RW	0x0	i3c_slave_clock_pd Used to config sda mode change when controller ACK slave's ibi request and when controller wants to receive ibidata. It needs to be greater than tSCO and greater than or equal to i3c_data_clock. During SCL LOW: Tsu = (2-n) * 0.25 * T(LOW) . During SCL HIGH: Thd = (1+n) * 0.25 * T(HIGH) . 1'bn: T = (n + 2) * 0.25 * T(SCL_HIGH) . Note: 0 <= n <= 1 T(SCL_LOW) is calculated by CLK_DIV_ODwhen bus type is i3c pure bus or i3c fast bus. T(SCL_HIGH) is calculated by CLK_DIV_OD or CLK_DIV_PP depends on the state of START when bus type is i3c pure bus or i3c fast bus.
7	RW	0x0	i3c_data_clock_pp Used to config sda change state when scl is low, used to adjust sda setup/hold time during push-pull mode 1'bn: Tsu_pp= (2-n) * 0.25 * T(SCL_LOW) . Note: 0 <= n <= 1 T(SCL_LOW) calculated by CLK_DIV_PP when SCL is calculated by CLK_DIV_PP.
6	RW	0x0	i3c_data_clock_od Used to config sda change state when scl is low, used to adjust sda setup/hold time during open-drain mode 1'bn: Tsu_od= (2-n) * 0.25 * T(SCL_LOW) . Note: 0 <= n <= 1 T(SCL_LOW) calculated by CLK_DIV_OD when SCL is calculated by CLK_DIV_OD.

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Bit	Attr	Reset Value	Description
5:4	RW	0x1	i3c_stop_clock_pd Clock before STOP condition. Tcpb = (stop_clock_od + 1) * T(SCL_HIGH). T(SCL_HIGH) is calculated by CLK_DIV_OD or CLK_DIV_PP is decided by MODULE_CONF[12] when bus type is i3c pure bus or i3c fast bus.
3:2	RW	0x1	i3c_restart_clock_pd Clock before/after RESTART condition Tcbsr = (restart_clock_pd + 0.75) * T(SCL_HIGH). Tcasr = (restart_clock_pd + 1.25) * T(SCL_HIGH). T(SCL_HIGH) is calculated by CLK_DIV_PP when bus type is i3c pure bus or i3c mixed fast bus with oddaa_en!=0. T(SCL_HIGH) is calculated by CLK_DIV_OD when bus type is i3c pure bus or i3c mixed fast bus with oddaa_en=0.
1:0	RW	0x1	i3c_start_clock_od Clock after START condition Tcas = (start_clock_od + 1.25) * T(SCL_HIGH). T(SCL_HIGH) is calculated by CLK_DIV_OD when bus type is i3c pure bus or i3c fast bus.

RKI3C_TIME_CONF_FM

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	mask 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	i3c_speci_stopclk_fm Used to config each sda high or low duration when using hdr exit pattern/target reset pattern 1'bn: T= (n + 1) * T(SCL_LOW). Note: 0 <= n <= 1 T(SCL_LOW) is calculated by CLK_DIV_FM when bus type is i3c mixed limited bus.
13	RW	0x0	i3c_slave_clock_fm Used to config sda mode change when controller ACK slave's ibi request and when controller wants to receive ibidata. The only requirement is greater than tSCO. During SCL LOW: Tsu = (2-n) * 0.25 * T(LOW) . During SCL HIGH: Thd = (1+n) * 0.25 * T(HIGH) . 1'bn: T = (n + 2) * 0.25 * T(SCL_HIGH) . Note: 0 <= n <= 1 T(SCL_LOW) and T(SCL_HIGH) is calculated by CLK_DIV_FM when bus type is i3c mixed limited(slow) bus.
12	RW	0x0	i3c_data_clock_fm Used to config sda change state when scl is low, used to adjust setup/hold time. 1'bn: Tsu_dat = (2-n) * 0.25 * T(SCL_LOW). Note: 0 <= n <= 1 T(SCL_LOW) is calculated by CLK_DIV_FM when bus type is i3c mixed limited bus and controller interacts with i3c devices.
11:10	RW	0x1	i3c_stop_clock_fm Tsu_sto = (stop_clock_fm + 1) * T(SCL_HIGH). T(SCL_HIGH) is calculated by CLK_DIV_FM when bus type is i3c mixed limited bus and controller interacts with i3c devices.

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Bit	Attr	Reset Value	Description
9:8	RW	0x1	i3c_start_clock_fm Tsu_sta = (start_clock_fm + 0.75) * T(SCL_HIGH). Thd_sta = (start_clock_fm + 1.25) * T(SCL_HIGH) . T(SCL_HIGH) is calculated by CLK_DIV_FM when bus type is i3c mixed limited bus and controller interacts with i3c devices.
7:5	RO	0x0	reserved
4	RW	0x0	i2c_data_clock_fm Used to config sda change state when scl is low, used to adjust setup/hold time. 1'bn: Tsu_dat = (2-n) * 0.25 * T(SCL_LOW) . Note: 0 <= n <= 1 T(SCL_LOW) calculated by CLK_DIV_FM when controller interacts with I2C legacy devices.
3:2	RW	0x1	i2c_stop_clock_fm Tsu_sto = (stop_clock+ 1) * T(SCL_HIGH) . T(SCL_HIGH) calculated by CLK_DIV_FM when controller interacts with I2C legacy devices.
1:0	RW	0x1	i2c_start_clock_fm Tsu_sta = (start_clock + 0.75) * T(SCL_HIGH) . Thd_sta = (start_clock + 1.25) * T(SCL_HIGH) . T(SCL_HIGH) calculated by CLK_DIV_FM when controller interacts with I2C legacy devices.

RKI3C_DAA_CONF

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	daareset_en 1'b0: Disable 1'b0: Enable This is used when previously using RSTDAA or other operations to change device's dynamic address. It will be cleared by sreset or end of transaction.
3:0	RW	0x0	daareset_num From which device to assign new dynamic address 4'b1: New dynamic address is from DEV_ID2_RR0 4'b2: New dynamic address is from DEV_ID3_RR0

RKI3C_BUS_FREE_CONF

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	bus_free_enable 1'b0: Disable, don't need to count IDLE cycle for next transaction 1'b1: Enable, need to count IDLE cycle for next transaction
15:0	RW	0x0104	bus_free_cycle When the bus stays in IDLE status for bus_free_cycle of clk_i3c, this module can start a next START. The default value is used for 200MHz and 1.3us.

RKI3C_BUS_FLT_CONF

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	bus_flt_en SCL edge glitch filter enable. 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	bus_flt_r Filter scl rising edge glitches of width less than flt_r * Tclk_i3c.
3:0	RW	0x0	bus_flt_f Filter scl falling edge glitches of width less than flt_f * Tclk_i3c

RKI3C_REG_READY_CONF

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	mask 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	ibi_ready 1'b0: Forbid ACK ibi request 1'b1: Allow ACK ibi request After finish setting all registers related to IBI or getting all ibi txdata, write 1 to this bit. Then controller can deal with IBI-request normally. Otherwise, it will NACK all IBI-request. The purpose is leaving enough time for ibi status or ibi data to be read before next ibi or leaving enough time to set ibimap register before first ibi. It will be cleared by ibi transaction's end_flag or sreset.
0	RW	0x0	i3c_reg_ready 1'b0: Forbid all i2c/i3c transaction 1'b1: All static registers has been configured It will be cleared by transaction's end_flag or sreset.

RKI3C_FLUSH_CTL

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	WO	0x0	ahb_ibi_status_flush Refreshing the AHB REG section involving the status of the IBIFIFO to not affect the next type of transmission such as byte It can also been cleared by sreset or by writing ibi_ready to REG_READY_CONF.
10	WO	0x0	ahb_rxtx_status_flush Refreshing the AHB REG section involving the status of the RXFIFO/TXFIFO to not affect the next type of transmission such as byte They can also been cleared by sreset.
9	WO	0x0	fifo_num_flush_ibi When enable, it will clear all FIFO_NUM REG related to IBI.
8	WO	0x0	fifo_num_flush_txrx When enable, it will clear all FIFO_NUM REG related to TX/RX.
7	RO	0x0	reserved
6	WO	0x0	ibimap_flush 1'b0: Not flush 1'b1: Flush IBIMAP1-5

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Bit	Attr	Reset Value	Description
5	WO	0x0	devuid_flush 1'b0: Not flush 1'b1: Flush DEV_ID_RR1/DEV_ID_RR2, id from 1-10
4	WO	0x0	cmdstatus_flush 1'b0: Not flush 1'b1: Flush CMDSTATUS1-11
3	WO	0x0	ibififo_flush 1'b0: Not flush 1'b1: Flush IBIFIFO
2	WO	0x0	rxfifo_flush 1'b0: Not flush 1'b1: Flush RXFIFO
1	WO	0x0	txfifo_flush 1'b0: Not flush 1'b1: Flush TXFIFO
0	WO	0x0	cmdfifo_flush 1'b0: Not flush 1'b1: Flush CMDFIFO

RKI3C_INT_EN

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	mask 1'b1: Write access enable
15	RW	0x0	cpu_fifotrig_ien 1'b0: Disable 1'b1: Enable
14	RW	0x0	i2c_wait_overt_ien 1'b0: Disable 1'b1: Enable Controller will hold scl low in order for TXFIFO to have data during tx procedure or RXFIFO to be not full during rx procedure.
13	RW	0x0	cmdend_ien 1'b0: Disable 1'b1: Enable
12	RW	0x0	hsize_error_ien 1'b0: Disable 1'b1: Enable This is used when the number of RXFIFO/IBIFIFO's byte left is less than hsize expects.
11	RW	0x0	ely_tran_ien 1'b0: Disable 1'b1: Enable
10	RW	0x0	addrnak_ien 1'b0: Disable 1'b1: Enable
9	RW	0x0	entdaa_nak2_ien 1'b0: Disable 1'b1: Enable Use for ENTDAA procedure and happen when slave NACK the address assigned to it twice.

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Bit	Attr	Reset Value	Description
8	RW	0x0	slavehdscl_ien 1'b0: Disable 1'b1: Enable Use for device hold scl low over threshold time on not pure i2c bus. Use for device error hold scl low on not pure i2c bus.
7	RW	0x0	ibififo_error_ien 1'b0: Disable 1'b1: Enable IBIFIFO error means when IBIFIFO is full, module still wants to write data into it. Use for IBI DATA FIFO overflow.
6	RW	0x0	rxfifo_error_ien 1'b0: Disable 1'b1: Enable RXFIFO error means when RXFIFO is full, module still wants to write data into it.
5	RW	0x0	txfifo_error_ien 1'b0: Disable 1'b1: Enable TXFIFO error means when TXFIFO is empty, module still wants to read from it. This happens during i3c tx prcedure when needed tx byte length is larger than the number of data have been written to TXFIFO.
4	RW	0x0	dataerr_ien 1'b0: Disable 1'b1: Enable Data on SDA bus is different from txbyte during TX procedure.
3	RW	0x0	i2cibi_error_ien 1'b0: Disable 1'b1: Enable When controller visits i2c device, one i3c device send ibi and win the arbitration.
2	RW	0x0	ibifin_ien 1'b0: Disable 1'b1: Enable
1	RW	0x0	slvreq_start_ien 1'b0: Disable 1'b1: Enable Use for this condition that when bus is IDLE, slave drop SDA low.
0	RW	0x0	end_ien 1'b0: Disable 1'b1: Enable

RKI3C_INT_STATUS

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	hsize_err_tx hsize_error_irqpd happens during visiting TXFIFO self-cleared when write 1'b1 to bit[12] hsize_error_irqpd
29	RO	0x0	hsize_err_ibi hsize_error_irqpd happens during visiting IBIFIFO self-cleared when write 1'b1 to bit[12] hsize_error_irqpd

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Bit	Attr	Reset Value	Description
28	RO	0x0	hsize_err_rx hsize_error_irqpd happens during visiting RXFIFO self-cleared when write 1'b1 to bit[12] hsize_error_irqpd
27:24	W1C	0x0	errcmd_id 4'hn: first error happen at which command,write 4'b1 to clear it The error includes slave NACK address, i3c rxearly, i2c_txearly.
23	RO	0x0	ely_monitor_irq Early rx happens when RESTART happens at T-bit before the last byte controller wants during i3c operation and it is caused by monitor device. It can be cleared when you write 1 to bit[11] ely_tran_irqpd.
22	RO	0x0	cpu_fifotrig_ibi 1'b1: means cpu_fifotrig_irqpd happens for IBIFIFO
21	RO	0x0	cpu_fifotrig_tx 1'b1: means cpu_fifotrig_irqpd happens for TXFIFO
20	RO	0x0	cpu_fifotrig_rx 1'b1: means cpu_fifotrig_irqpd happens for RXFIFO
19:16	W1C	0x0	lastcmd_id 4'hn: Stop at which command,write 4'b1 to clear it
15	RO	0x0	cpu_fifotrig_irqpd 1'b0: No interrupt available 1'b1: TXFIFO/RXFIFO/IBIFIFO need CPU to work RXFIFO/IBIFIFO's data num is greater than or equal to its watermark level, or the transaction has been finished and still have data in this FIFO. Or TXFIFO's empty space is over its watermark level and still need to sent data to this FIFO. See bit[22:20] for specific types. Note that even if you write 1 to it, as long as the master meet the above conditions, the bit will write 1 again.
14	RO	0x0	i2c_wait_overt_irqpd 1'b0: No interrupt available 1'b1: Timeout in I2C happens Controller will hold scl low at some special conditions, when it hold scl over wait_thld_i2c, rise this interrupt. It can be cleared only by sreset, fstop or fifo meet requirement. Note that even if you write 1 to it, as long as the master can not continue its transaction, the bit will write 1 again.
13	W1C	0x0	cmdend_irqpd 1'b0: No interrupt available 1'b1: one command had been finished
12	W1C	0x0	hsize_error_irqpd 1'b0: No interrupt available 1'b1: hsize error interrupt appear, write 1 to clear it This is used when the number of RXFIFO/IBIFIFO's byte left is less than hsize expects. Also this is used when the number of byte that need to be sent to TXFIFO is less than hsize expects. See bit[30:28] for specific types.

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Bit	Attr	Reset Value	Description
11	W1C	0x0	ely_tran_irqpd 1'b0: No interrupt available 1'b1: early tx or rx or ibirx interrupt appear, write 1 to clear it Early rx happens when slave send byte with T=0 before the last byte controller wants during i3c operation, includes monitor device let it happen. Whether it is caused by monitor device, see bit[23]. Early tx happens when slave NACK data sent to it during i2c operation. Early ibirx happens when slave send byte with T=0 before the last byte controller wants during ibi operation.
10	W1C	0x0	addrnak_irqpd 1'b0: No interrupt available 1'b1: slave nack address interrupt appear, write 1 to clear it
9	W1C	0x0	entdaa_nak2_irqpd 1'b0: No interrupt available 1'b1: Assigned address been NACK twice interrupt appear, write 1 to clear it
8	W1C	0x0	slavehdscl_irqpd 1'b0: No interrupt available 1'b1: Slave hold scl interrupt appear, write 1 to clear it Note that even if you write 1 to clear it, as long as the slave continues to hold scl low, the bit will write 1 again
7	W1C	0x0	ibififo_error_irqpd 1'b0: No interrupt available 1'b1: IBIFIFO error interrupt appear, write 1 to clear it IBIFIFO error means when IBIFIFO is full, module still wants to write data into it.
6	W1C	0x0	rxfifo_error_irqpd 1'b0: No interrupt available 1'b1: RXFIFO error interrupt appear, write 1 to clear it RXFIFO error means when RXFIFO is full, module still wants to write data into it.
5	W1C	0x0	txfifo_error_irqpd 1'b0: No interrupt available 1'b1: TXFIFO error interrupt appear, write 1 to clear it TXFIFO error means when TXFIFO is empty, module still wants to read from it.
4	W1C	0x0	dataerr_irqpd 1'b0: No interrupt available 1'b1: Transimit data on SDA line inconsistent with sent interrupt appear, write 1 to clear it Include i2c tx transaction and i3c tx transaction.
3	W1C	0x0	i2cibi_irqpd 1'b0: No interrupt available 1'b1: ibi happen during i2c transaction interrupt appear, write 1 to clear it This error means when controller want to interact with i2c slave, i3c slave send ibi and win the arbitration. The controller will NACK the ibi request. The data in the IBISTATUS reg has nothing to do with this interrupt.
2	W1C	0x0	ibifin_irqpd 1'b0: No interrupt available 1'b1: Ibi finish interrupt appear, write 1 to clear it

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Bit	Attr	Reset Value	Description
1	W1C	0x0	slvreq_start_irqpd 1'b0: No interrupt available 1'b1: Slave drive SDA to request START interrupt appear, write 1 to clear it
0	W1C	0x0	end_irqpd 1'b0: No interrupt available 1'b1: Transmission finish interrupt appear, write 1 to clear it

RKI3C_IBI_CONF

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	WO	0x0	mask 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	async_mode_en 1'b0: Disable 1'b1: Enable Enable means that controller will record how many cycles between first SCL Rising Edge After ACK and first SCL Rising Edge After MDB T Bit.
2	RW	0x0	autopend_stop_en 1'b0: Disable 1'b1: Enable If enable, then when IBI's MDB[7:5]==3'b101, stop transmission after finishing IBI procedure and wait CPU's command.
1	RW	0x1	resp2hj 1'b0: ACK to hot-join 1'b1: NACK to hot-join
0	RW	0x0	autoibi_en 1'b0: Disable 1'b1: Enable controller deal with IBI-request automatically when target drops SDA low on IDLE bus Must write 1'b1 after all registers related to IBI has been configured.

RKI3C_IBI_MAP1

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	devid2_pllen Device2's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
23	RW	0x0	devid2_resp Preset response to IBI request initiated by slave device 2 1'b0: ACK 1'b1: NACK
22:16	RW	0x00	devid2_addr Device2's dynamic address
15:8	RW	0x00	devid1_pllen Device1's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.

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Bit	Attr	Reset Value	Description
7	RW	0x0	devid1_resp Preset response to IBI request initiated by slave device 1 1'b0: ACK 1'b1: NACK
6:0	RW	0x00	devid1_addr Device1's dynamic address

RKI3C_IBI_MAP2

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	devid4_pllen Device4's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
23	RW	0x0	devid4_resp Preset response to IBI request initiated by slave device 4 1'b0: ACK 1'b1: NACK
22:16	RW	0x00	devid4_addr Device4's dynamic address
15:8	RW	0x00	devid3_pllen Device3's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
7	RW	0x0	devid3_resp Preset response to IBI request initiated by slave device 3 1'b0: ACK 1'b1: NACK
6:0	RW	0x00	devid3_addr Device3's dynamic address

RKI3C_IBI_MAP3

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	devid6_pllen Device6's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
23	RW	0x0	devid6_resp Preset response to IBI request initiated by slave device 6 1'b0: ACK 1'b1: NACK
22:16	RW	0x00	devid6_addr Device6's dynamic address
15:8	RW	0x00	devid5_pllen Device5's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
7	RW	0x0	devid5_resp Preset response to IBI request initiated by slave device 5 1'b0: ACK 1'b1: NACK
6:0	RW	0x00	devid5_addr Device5's dynamic address

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RKI3C_IBI_MAP4

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	devid8_pllen Device8's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
23	RW	0x0	devid8_resp Preset response to IBI request initiated by slave device 8 1'b0: ACK 1'b1: NACK
22:16	RW	0x00	devid8_addr Device8's dynamic address
15:8	RW	0x00	devid7_pllen Device7's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
7	RW	0x0	devid7_resp Preset response to IBI request initiated by slave device 7 1'b0: ACK 1'b1: NACK
6:0	RW	0x00	devid7_addr Device7's dynamic address

RKI3C_IBI_MAP5

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	devid10_pllen Device10's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
23	RW	0x0	devid10_resp Preset response to IBI request initiated by slave device 10 1'b0: ACK 1'b1: NACK
22:16	RW	0x00	devid10_addr Device10's dynamic address
15:8	RW	0x00	devid9_pllen Device9's payload length This is the maximum read length for IBI READ, including MDB and additional bytes.
7	RW	0x0	devid9_resp Preset response to IBI request initiated by slave device 9 1'b0: ACK 1'b1: NACK
6:0	RW	0x00	devid9_addr Device9's dynamic address

RKI3C_DEV_ID1_RR0

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	is_i3c_mode 1'b0: This addr means i2c static addr 1'b1: This addr means i3c dynamic addr
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	dev1_daa When is_i3c_mode=1'b1, this means dynamic address will be assigned to Device 1. When is_i3c_mode=1'b0, this means i2c static addr.

RKI3C_DEV_ID1_RR1

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dev1_uidh Device1's Dev ID bit[47:16] It can be cleared by write 1 to FLUSH_CTL REG's bit[5] devuid_flush.

RKI3C_DEV_ID1_RR2

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dev1_uidl Device1's Dev ID bit[15:0] It can be cleared by write 1 to FLUSH_CTL REG's bit[5] devuid_flush.
15:8	RO	0x00	dev1_bcr Device1's BCR It can be cleared by write 1 to FLUSH_CTL REG's bit[5] devuid_flush.
7:0	RO	0x00	dev1_dcr Device1's DCR It can be cleared by write 1 to FLUSH_CTL REG's bit[5] devuid_flush.

RKI3C_VERSION

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0005	version_number Version number of this i3c controller.

RKI3C_CMD1_STATUS

Address: **Operational Base** + offset (0x0230)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	cmd1_lennak_i2c Slave NACK at which tx byte. Only for I2C, because I3C data do not have ACK/NACK bit when sending or receiving data.
19:8	RO	0x000	cmd1_lentran Length of byte has been received when rx or length of byte has been transmitted when tx. And 0 for DAA RX procedure.
7	RO	0x0	cmd1_rnw 1'b0: This cmd's Rnw is W 1'b1: This cmd's Rnw is R
6	RO	0x0	cmd1_finish 1'b1: means this command has been finished

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Bit	Attr	Reset Value	Description
5:4	RO	0x0	cmd1_daanak 2'b00: Target ACK addr assigned 2'b01: Target NACK addr assigned once(only happen when early_term) 2'b10: Target NACK addr assigned twice 2'b11: Reserved This will only happen under I3C mode
3	RO	0x0	cmd1_force_stop 1'b0: No force stop happen 1'b1: Force stop happen at this command
2	RO	0x0	cmd1_txearly_i2c 1'b0: Tx completed 1'b1: Tx terminated early This will only happen under I2C mode when target NACK txdata
1	RO	0x0	cmd1_rxearly_i3c 1'b0: Rx completed 1'b1: Rx terminated early This will only happen under I3C mode when slave let T=0 before last byte
0	RO	0x0	cmd1_addrnak 1'b0: Target ACK addr 1'b1: Target NACK addr

RKI3C_ASYNC_REF_CNT

Address: **Operational Base** + offset (0x0260)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	async_ref_cnt The value means number of clk_i3c cycles from IBI ACK's next SCL rise time to IBI MDB T-bit's next SCL rise time. It can be cleared by sreset.

RKI3C_FIFO_STATUS

Address: **Operational Base** + offset (0x0264)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	ibififo_space2empty The amount of word contained in the IBIFIFO, i.e. the number of data that can be read by DMA or CPU. Value 0 means IBI FIFO is empty.
23:21	RO	0x0	reserved
20:16	RO	0x00	rxfifo_space2empty The amount of word contained in the RXFIFO, i.e. the number of data that can be read by DMA or CPU. Value 0 means RXFIFO is empty.
15:13	RO	0x0	reserved
12:8	RO	0x10	txfifo_space2full The remaining space in the TXFIFO, i.e. how many words can still be written in. Value 0 means TXFIFO is full.
7	RO	0x1	cmdempty 1'b0: CMDFIFO not empty 1'b1: CMDFIFO empty

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Bit	Attr	Reset Value	Description
6	RO	0x0	cmdfull 1'b0: CMDFIFO not full 1'b1: CMDFIFO full
5	RO	0x1	ibiempty 1'b0: IBIFIFO not empty 1'b1: IBIFIFO empty
4	RO	0x0	ibifull 1'b0: IBIFIFO not full 1'b1: IBIFIFO full
3	RO	0x1	rxempty 1'b0: RXFIFO not empty 1'b1: RXFIFO empty
2	RO	0x0	rxfull 1'b0: RXFIFO not full 1'b1: RXFIFO full
1	RO	0x1	txempty 1'b0: TXFIFO not empty 1'b1: TXFIFO empty
0	RO	0x0	txfull 1'b0: TXFIFO not full 1'b1: TXFIFO full

RKI3C_IBI_STATUS

Address: **Operational Base** + offset (0x0268)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	i2c_ibiaddr 7 bit addr & Rnw
23:20	RO	0x0	reserved
19:16	RO	0x0	slave_id if it is Device 1, then slave_id=1. if its type is hot-join or master-request or its addr does not belog to ibimap, then slave_id=0.
15:8	RO	0x00	ibi_rxbyte_len the number of bytes received during this IBI procedure
7:5	RO	0x0	reserved
4	RO	0x0	ibi_pend_flag 1'b0: MDB not means pend reading 1'b1: MDB means pend reading
3	RO	0x0	ibi_rxely Early ibirx happens when slave send byte with T=0 before the last byte controller wants during ibi operation.
2	RO	0x0	ibi_resp 1'b0: ACK 1'b1: NACK
1:0	RO	0x0	ibi_type 2'b00: Ibi interrupt 2'b01: Hot join 2'b10: Master-request Others: Reserved

RKI3C_DAA_STATUS

Address: **Operational Base** + offset (0x026C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:4	RO	0x0	daanak_cnt 2'b00: Target ACK addr assigned 2'b01: Target NACK addr assigned once(only happen when force_stop) 2'b10: Target NACK addr assigned twice 2'b11: Reserved
3:0	RO	0x0	daa_assigned_cnt Means the Dynamic Address Assigned Procedure stopped at which device.

RKI3C_RXDAT_OVER

Address: **Operational Base** + offset (0x0270)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata_over Record overflow rxdata when RXFIFO is full, so it will be valid only when rxfifo_error happen. Can be cleared by rxfifo_flush.

RKI3C_IBIRX_OVER

Address: **Operational Base** + offset (0x0274)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ibirx_over Record overflow ibi rxdata when IBIFIFO is full, so it will be valid only when ibififo_error happen Can be cleared by ibififo_flush.

RKI3C_LINE_STATUS

Address: **Operational Base** + offset (0x0278)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	sda_in_f record SDA line value
0	RO	0x0	scl_in_f record SCL line value

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31.5 Interface Description

Table 31-1 I3C Interface Description

Module pin	Direction	Pin name	IOMUX
IOMUX0			
I3C0_SCL_M0	I/O	I2C0_SCL_M1/UART8_TX_M2/I3C0_SCL_M0/GPIO0_C1_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L [7:4] = 4'hb
I3C0_SDA_M0	I/O	I2C0_SDA_M1/UART8_RX_M2/I3C0_SDA_M0/GPIO0_C2_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L [11:8] = 4'hb
I3C0_SDAPULL_M0	I/O	SAI0_SDO0_M1/DP_HPDIN_M1/UART10_RX_M2/I3C0_SDA_PU_M0/GPIO0_C5_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H [7:4] = 4'hb
I3C1_SCL_M0	I/O	CAM_CLK0_OUT_M1/ETH1_RXD1_M0/SAI4_MCLK_M3/UART6_TX_M1/I3C1_SCL_M0/PWM2_CH2_M2/GPIO2_D2_d	TOP_IOC_GPIO2D_IOMUX_SEL_L [11:8] = 4'hc
I3C1_SDA_M0	I/O	ETH1_RXCTL_M0/UART6_RX_M1/I3C1_SDA_M0/PWM2_CH3_M2/GPIO2_D3_d	TOP_IOC_GPIO2D_IOMUX_SEL_L [15:12] = 4'hc
I3C1_SDAPULL_M0	I/O	CAM_CLK1_OUT_M1/ETH_CLK1_25M_OUT_M0/ETH0_MCLK_M1/SAI3_MCLK_M2/SPDIF_RX0_M2/UART9_RTSN_M0/I3C1_SDA_PU_M0/PWM2_CH6_M2/GPIO2_D6_d	TOP_IOC_GPIO2D_IOMUX_SEL_H [11:8] = 4'hc
IOMUX1			
I3C0_SCL_M1	I/O	ETH1_MDC_M1/SAI2_LRCK_M0/I3C0_SCL_M1/PWM1_CH3_M1/GPIO1_D2_d	TOP_IOC_GPIO1D_IOMUX_SEL_L [11:8] = 4'ha
I3C0_SDA_M1	I/O	ETH1_MDIO_M1/SAI2_SDI_M0/I3C0_SDA_M1/PWM1_CH4_M1/GPIO1_D3_d	TOP_IOC_GPIO1D_IOMUX_SEL_L [15:12] = 4'ha
I3C0_SDAPULL_M1	I/O	ETH1_RXCTL_M1/SAI2_SCLK_M0/UART10_RX_M1/I3C0_SDA_PU_M1/GPIO1_D1_d	TOP_IOC_GPIO1D_IOMUX_SEL_L [7:4] = 4'ha
I3C1_SCL_M1	I/O	SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L [11:8] = 4'he
I3C1_SDA_M1	I/O	SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/CAN1_TX_M0/I3C1_SDA_M1/GPIO2_A3_d	TOP_IOC_GPIO2A_IOMUX_SEL_L [15:12] = 4'he
I3C1_SDAPULL_M1	I/O	SDMMC0_CLK/FSPI1_CLK_M0/SAI3_SCLK_M3/TEST_CLK_OUT/UART5_TX_M2/I2C5_SCL_M0/SPI0_CLK_M1/I3C1_SDA_PU_M1/GPIO2_A5_d	TOP_IOC_GPIO2A_IOMUX_SEL_H [7:4] = 4'he
IOMUX2			
I3C1_SCL_M2	I/O	VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L [15:12] = 4'hb

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Module pin	Direction	Pin name	IOMUX
I3C1_SDA_M2	I/O	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L [11:8] = 4'hb
I3C1_SDAPULL_M2	I/O	VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L [7:4] = 4'hb

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31.6 Application Notes

The I3C controller core operation flow chart below is to describe how the software configures and performs an I3C transmission or an I2C transmission through this I3C controller core. Note that it is forbidden to have both I2C transmission and I3C transmission between one START and STOP.

There are some configuration sequences to be aware of:

- Configure the FLUSH_CTL register first to clear the previous status.
- If you use DMA to send data to TXFIFO, you must configure the relevant registers after writing all CMD data.
- If you enable i3c_reg_ready bit of REG_READY_CONF register, then before transmission stops, transport-related configuration registers can no longer be configured, such as CMD FIFO and time-related registers.
- If you want to support next IBI transmission, you must enable ibi_ready bit in REG_READY_CONF register. Otherwise the controller will NACK all In-Band Interrupt request.
- If you want to reset the controller module, in addition to system reset, you can also implement the reset function through setting 1'b1 to sreset bit in MODULE_CTL register and all bits in FLUSH_CTL register. It will not reset other configured registers.

Descriptions of transmitting in I2C mode and transmitting in I3C mode are shown below. Users are strongly advised to follow the tips below:

- Transmit in I2C mode (MODULE_CONF[2:1]!=2'b00, not pure i3c bus) (CMD[10:8]=3'b100 I2C_TX or 3'b101 I2C_RX)

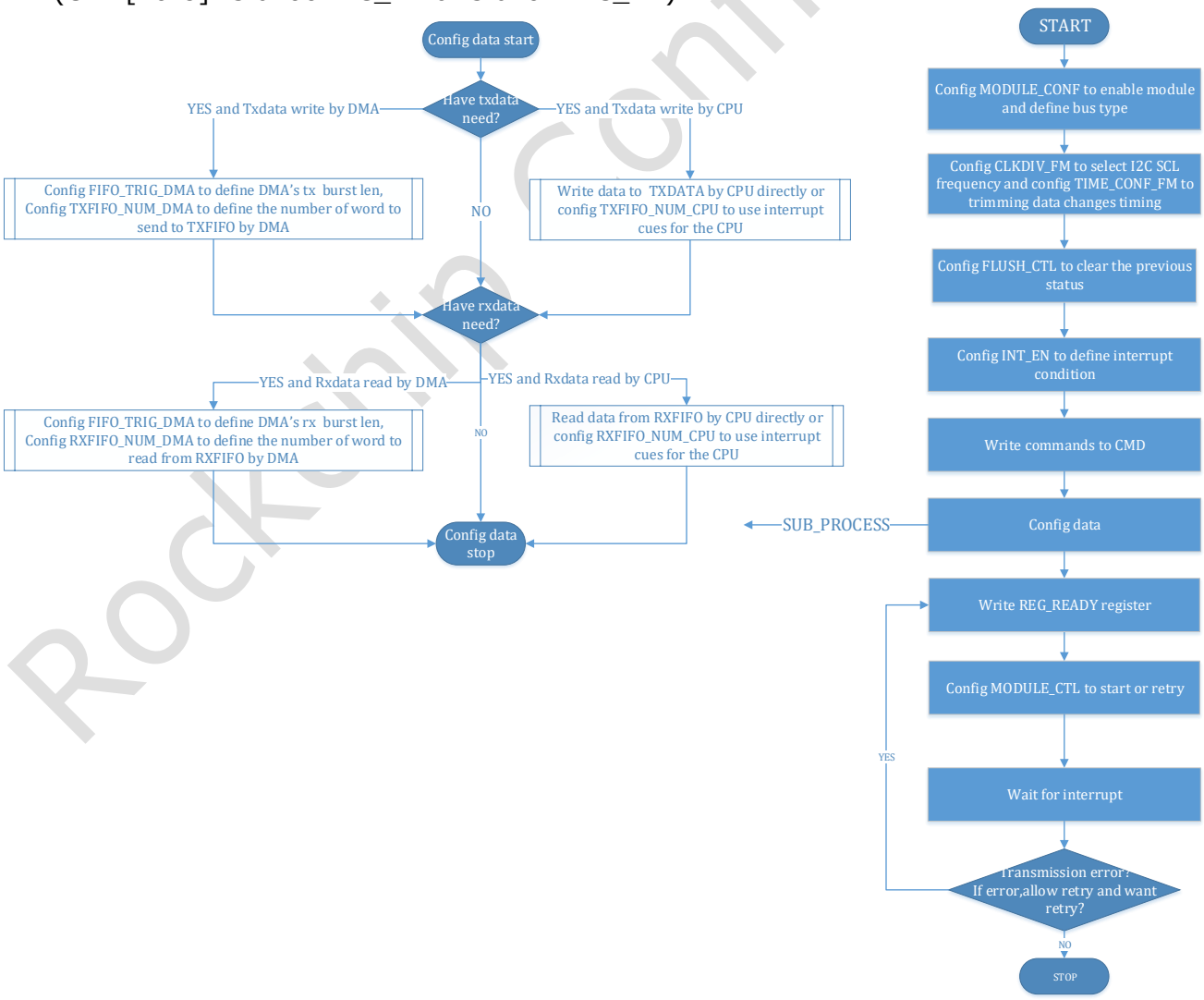

Fig. 31-11 I2C Flow

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- The data interaction between the internal FIFO and the external DMA runs through the entire transmission process if users choose to use DMA by configuring RKDMA_CONF register.
- The conditions for the retry are as follows: For I2C TX, you can enable retry function only when the reason that causes the transmission to stop is due to target NACKed address, and the controller's response to this was a direct STOP, which means no data belongs to this command had been sent. For I2C RX, you can enable retry function only when the reason that causes the transmission to stop is due to target NACKed address, and the controller's response to this was a direct STOP and rx_pad_en bit in RKDMA_CONF register was been set to 1'b0. In other cases, the retry function is prohibited. When you enable retry function, you don't need to configure FLUSH_CTL[11:10].

- Transmit in I3C mode (MODULE_CONF[2:1]!=2'b11, not pure i2c bus) (CMD[10:8]=3'b000 I3C_TX or 3'b001 I3C_RX or 3'b010 ENTDAA RX or 3'b011 address only)

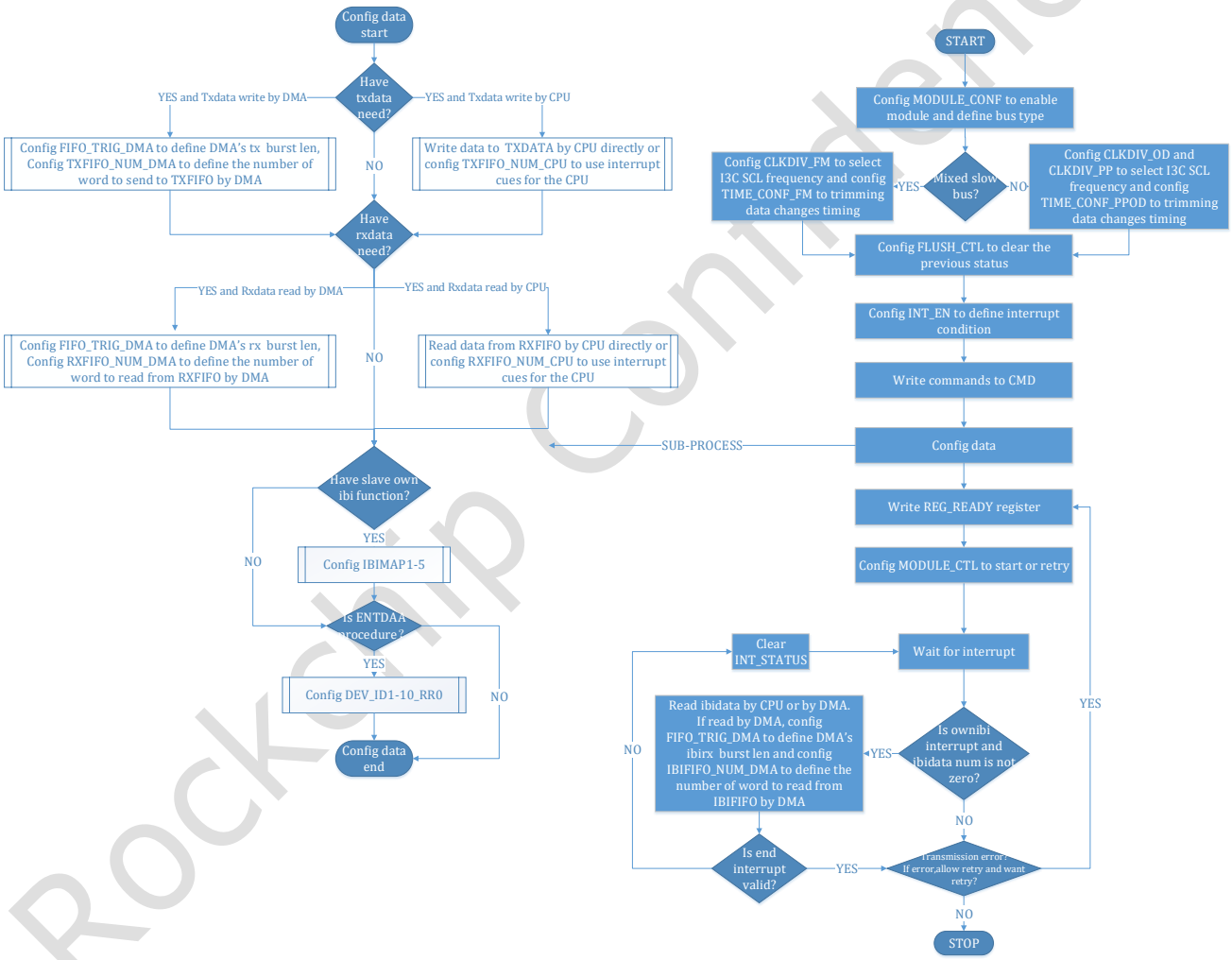

Fig. 31-12 I3C Flow

- If the bus is mixed fast bus, the first command after wake up must be send 7E/W address only in FM mode to tell i2c target to enable its 50ns spike filter.
- If the bus is mixed slow bus, SCL frequency during i3c transmission is the same as the frequency during i2c transmission, so user only need to configure CLKDIV_FM. Otherwise, if the bus is a pure i3c bus or a mixed fast bus, user need to configure both CLKDIV_PP and CLKDIV_OD to meet the requirement of i3c transmission. And the frequency of this condition's START+ADDRESS procedure will be divided by CLKDIV_OD.
- Since the target might support the 100 μs read-abort approach, the controller can

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not hold SCL low too long. Cycles of tout_cycle in TOUT_CONF_I3C to add SCL low time should be smaller than read-abort need time.

- If you have sent RSTDAA CCC or perform other operations that changed the dynamic address , you should configure DAA_CONF to reset number of devices that had been assigned dynamic address to the correct value. Otherwise, next ENTDAA procedure will be error.
- The conditions are as follows if you want to enable retry function: For I3C TX, the reason for the stop of the transmission is that target NACKed address, and the controller's response to this was a direct STOP which means no data belongs to this command had been sent. For I3C RX, the reason that causes the transmission to stop is due to target NACKed address, and the controller's response to this was a direct STOP and rx_pad_en bit in RKDMA_CONF register was been set to 1'b0. For I3C IBI, the reason that causes the transmission to stop is that one target's IBI request happened and after the IBI procedure, the controller chose a direct STOP. In other cases, the retry function is prohibited. When you enable retry function, you don't need to configure FLUSH_CTL[11:10].

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Chapter 32 Inter-Integrated Circuit (I2C)

32.1 Overview

The Inter-Integrated Circuit (I2C) is a two wired (SCL and SDA), bi-directional serial bus that provides an efficient and simple method of information exchange between devices. This I2C bus controller supports master mode acting as a bridge between AMBA protocol and generic I2C bus system.

I2C Controller supports the following features:

- Support 10 independent I2C: I2C0~9, with 36 pairs of IO.
- Item Compatible with I2C-bus
- AMBA APB slave interface
- Support master mode of I2C bus
- Software programmable clock frequency and transfer rate up to 400Kbit/sec
- Support 7 bits and 10 bits addressing modes
- Interrupt or polling driven multiple bytes data transfer
- Clock stretching and wait state generation
- Filter out glitch on SCL and SDA

32.2 Block Diagram

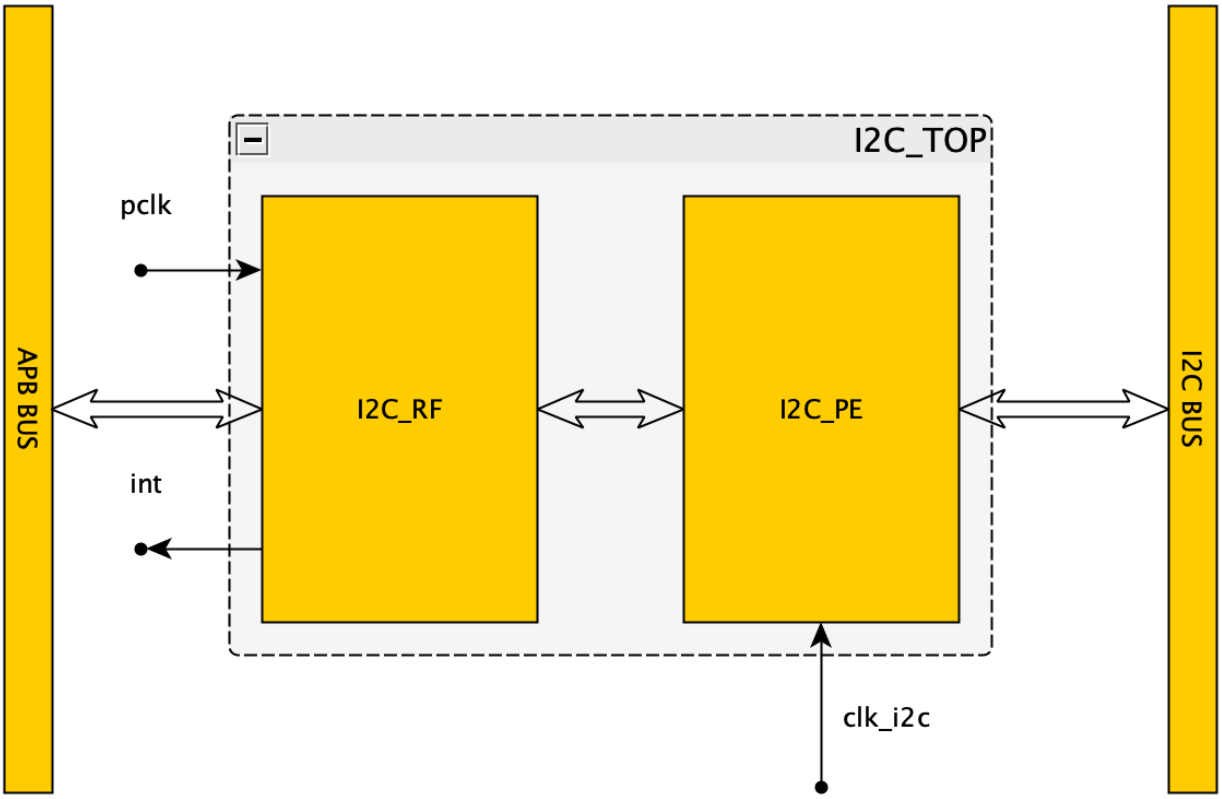

Fig.32-1 I2C architecture

32.2.1 I2C_RF

I2C_RF module is used to control the I2C controller operation by the host with APB interface. It implements the register set and the interrupt functionality. The I2C_RF component operates synchronously with the pclk.

32.2.2 I2C_PE

I2C_PE module implements the I2C master operation for transmit data to and receive data from other I2C devices. The I2C master controller operates synchronously with the clk_i2c.

32.2.3 I2C_TOP

I2C_TOP module is the top module of the I2C controller.

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32.3 Function Description

This chapter provides a description about the functions and behavior under various conditions.
The I2C controller supports only Master function. It supports the 7-bits/10-bits addressing mode and support general call address. The maximum clock frequency and transfer rate can be up to 400Kbit/sec.
The operations of I2C controller is divided to 2 parts and described separately: initialization and master mode programming.

32.3.1 Initialization

The I2C controller is based on AMBA APB bus architecture and usually is part of a SOC. So before I2C operates, some system setting and configuration must be conformed, which includes:

- I2C interrupt connection type: CPU interrupt scheme should be considered. If the I2C interrupt is connected to extra Interrupt Controller module, we need decide the INTC vector.
- I2C Clock Rate: The I2C controller uses the APB clock to configure controller and uses clk_i2c as the working clock. The correct register setting is subject to the system requirement.

32.3.2 Master Mode Programming

- SCL Clock
  When the I2C controller is programmed in Master mode, the SCL frequency is determined by I2C_CLKDIV register. The SCL frequency is calculated by the following formula:
  SCL Divisor = 8*(CLKDIVL + 1 + CLKDIVH + 1); clk_i2c = 100MHz~200MHz.
  SCL = clk_i2c/ SCLK Divisor.

- Data Receiver Register Access
  When the I2C controller received MRXCNT bytes data, CPU can get the data through register RXDATA0 ~ RXDATA7. The controller can receive up to 32 bytes' data in one transaction.
  When MRXCNT register is written, the I2C controller will start to drive SCL to receive data.

- Transmit Transmitter Register
  Data to transmit are written to TXDATA0~7 by CPU. The controller can transmit up to 32 bytes' data in one transaction. The lower byte will be transmitted first.
  When MTXCNT register is written, the I2C controller will start to transmit data.

- Start Command
  Write 1 to I2C_CON[3], the controller will send I2C start command.

- Stop Command
  Write 1 to I2C_CON[4], the controller will send I2C stop command.

- I2C Operation mode
  There are four i2c operation modes.
  - When I2C_CON[2:1] is 2'b00, the controller will transmit all valid data in TXDATA0~TXDATA7 byte by byte. The controller will transmit lower byte first.
  - When I2C_CON[2:1] is 2'b01, the controller will transmit device address in MRXADDR first (Write/Read bit = 0) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enters receive mode.

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- When I2C_CON[2:1] is 2'b10, the controller is in receive mode, it will trigger clock to read MRXCNT byte data.
- When I2C_CON[2:1] is 2'b11, the controller will transmit device address in MRXADDR first (Write/Read bit = 1) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enters receive mode.

- Read/Write Command
  - When I2C_OPMODE(I2C_CON[2:1]) is 2'b01 or 2'b11, the Read/Write command bit is decided by controller itself.
  - In RX only mode (I2C_CON[2:1] is 2'b10), the Read/Write command bit is decided by MRXADDR[0].
  - In TX only mode (I2C_CON[[2:1] is 2'b00), the Read/Write command bit is decided by TXDATA[0].

- Master Interrupt Condition

  There are 7 interrupt bits in I2C_ISR register related to master mode.
  - Byte transmitted finish interrupt (Bit 0): The bit is asserted when Master completed transmitting a byte.
  - Byte received finish interrupt (Bit 1): The bit is asserted when Master completed receiving a byte.
  - MTXCNT bytes data transmitted finish interrupt (Bit 2): The bit is asserted when Master completed transmitting MTXCNT bytes.
  - MRXCNT bytes data received finish interrupt (Bit 3): The bit is asserted when Master completed receiving MRXCNT bytes.
  - Start interrupt (Bit 4): The bit is asserted when Master finished asserting start command to I2C bus.
  - Stop interrupt (Bit 5): The bit is asserted when Master finished asserting stop command to I2C bus.
  - NAK received interrupt (Bit 6): The bit is asserted when Master received a NAK handshake.

- Last byte acknowledge control
  - If I2C_CON[5] is 1, the I2C controller will transmit NAK handshake to slave when the last byte received in RX only mode.
  - If I2C_CON[5] is 0, the I2C controller will transmit ACK handshake to slave when the last byte received in RX only mode.

- How to handle NAK handshake received
  - If I2C_CON[6] is 1, the I2C controller will stop all transactions when NAK handshake received. And the software should take responsibility to handle the problem.
  - If I2C_CON[6] is 0, the I2C controller will ignore all NAK handshake received.

- I2C controller data transfer waveform
  - Bit transferring
    - Data Validity

      The SDA line must be stable during the high period of SCL, and the data on SDA line can only be changed when SCL is in low state.

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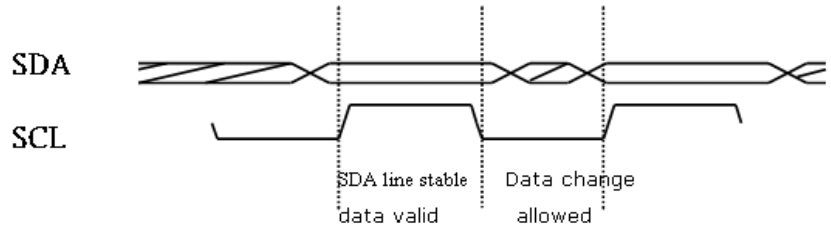

Fig.32-2 I2C DATA Validity

- START and STOP conditions
  START condition occurs when SDA goes low while SCL is in high period. STOP condition is generated when SDA line goes high while SCL is in high state.

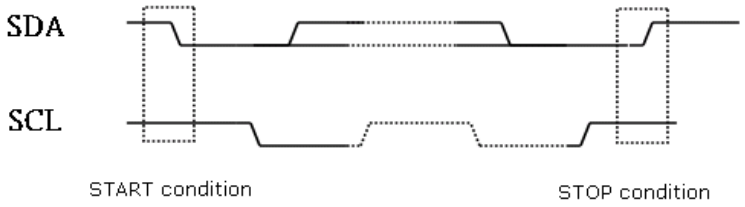

Fig.32-3 I2C Start and stop conditions

- Data transfer
  - Acknowledge
    After a byte of data transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK signal on SDA line, if the receiver pulls SDA line to low, it means "ACK", on the contrary, it's "NOT ACK".

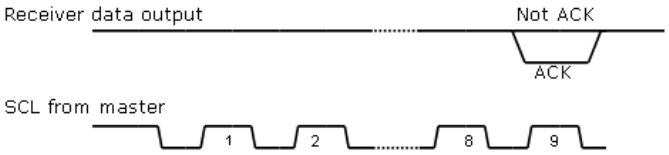

Fig.32-4 I2C Acknowledge

  - Byte transfer
    The master own I2C bus might initiate multi byte to transfer to a slave. The transfer starts from a "START" command and ends in a "STOP" command. After every byte transfer, the receiver must reply an ACK to transmitter.

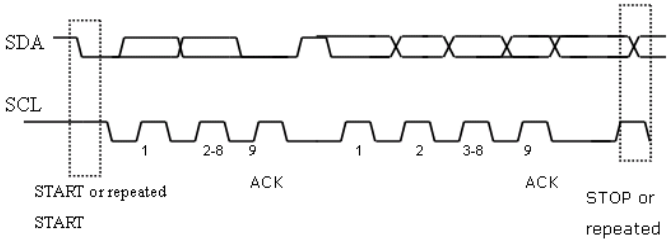

Fig.32-5 I2C byte transfer

32.4 Register Description

32.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

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Name	Base Address
I2C0	0x27300000
I2C1	0x2AC40000
I2C2	0x2AC50000
I2C3	0x2AC60000
I2C4	0x2AC70000
I2C5	0x2AC80000
I2C6	0x2AC90000
I2C7	0x2ACA0000
I2C8	0x2ACB0000
I2C9	0x2AE80000

32.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKI2C_CON	0x0000	W	0x00060000	Control register
RKI2C_CLKDIV	0x0004	W	0x00000001	Clock divider register I2C CLK = PCLK / (16*CLKDIV)
RKI2C_MRXADDR	0x0008	W	0x00000000	The slave address accessed for master rx mode
RKI2C_MRXRADDR	0x000C	W	0x00000000	The slave register address accessed for master rx mode
RKI2C_MTXCNT	0x0010	W	0x00000000	Master transmit count, specify the total bytes to be transmit (0~32)
RKI2C_MRXCNT	0x0014	W	0x00000000	Master rx count, specify the total bytes to be recieved(0~32)
RKI2C_IEN	0x0018	W	0x00000000	Interrupt enable register
RKI2C_IPD	0x001C	W	0x00000000	Interrupt pending register
RKI2C_FCNT	0x0020	W	0x00000000	Finished count: the count of data which has been transmitted or received for debug purpose
RKI2C_SCL_OE_DB	0x0024	W	0x00000020	Slave hold debounce configure register
RKI2C_TXDATA0	0x0100	W	0x00000000	I2C tx data register 0
RKI2C_TXDATA1	0x0104	W	0x00000000	I2C tx data register 1
RKI2C_TXDATA2	0x0108	W	0x00000000	I2C tx data register 2
RKI2C_TXDATA3	0x010C	W	0x00000000	I2C tx data register 3
RKI2C_TXDATA4	0x0110	W	0x00000000	I2C tx data register 4
RKI2C_TXDATA5	0x0114	W	0x00000000	I2C tx data register 5
RKI2C_TXDATA6	0x0118	W	0x00000000	I2C tx data register 6
RKI2C_TXDATA7	0x011C	W	0x00000000	I2C tx data register 7
RKI2C_RXDATA0	0x0200	W	0x00000000	I2C rx data register 0
RKI2C_RXDATA1	0x0204	W	0x00000000	I2C rx data register 1
RKI2C_RXDATA2	0x0208	W	0x00000000	I2C rx data register 2
RKI2C_RXDATA3	0x020C	W	0x00000000	I2C rx data register 3
RKI2C_RXDATA4	0x0210	W	0x00000000	I2C rx data register 4
RKI2C_RXDATA5	0x0214	W	0x00000000	I2C rx data register 5
RKI2C_RXDATA6	0x0218	W	0x00000000	I2C rx data register 6
RKI2C_RXDATA7	0x021C	W	0x00000000	I2C rx data register 7
RKI2C_ST	0x0220	W	0x00000000	Status debug register
RKI2C_DBGCTRL	0x0224	W	0x00000000	Debug config register
RKI2C_CON1	0x0228	W	0x00000000	Control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

32.4.3 Detail Registers Description

RKI2C_CON

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Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0006	version Rki2c version information.
15:14	RW	0x0	stop_setup Stop setup config. TSU;sto = (stop_setup + 1) * T(SCL_HIGH) + Tclk_i2c.
13:12	RW	0x0	start_setup Start setup config. TSU;sta = (start_setup + 1) * T(SCL_HIGH) + Tclk_i2c. THD;sta = (start_setup + 2) * T(SCL_HIGH) - Tclk_i2c.
11:8	RW	0x0	data_upd_st SDA update point config. Used to config sda change state when scl is low, used to adjust setup/hold time. 4'bn: Thold = (n + 1) * T(SCL_LOW) / 8. Note: 0 <= n <= 5
7	RO	0x0	reserved
6	RW	0x0	act2nak Operation when NAK handshake is received. 1'b0: Ignored. 1'b1: Stop transaction.
5	RW	0x0	ack Last byte acknowledge control in master receive mode. 1'b0: ACK 1'b1: NAK
4	RW	0x0	stop Stop enable, when this bit is written to 1, I2C will generate stop signal.
3	RW	0x0	start Start enable, when this bit is written to 1, I2C will generate start signal.
2:1	RW	0x0	i2c_mode I2c mode select. 2'b00: Transmit only. 2'b01: Transmit address (device + register address) --> Restart --> Transmit address -> Receive only. 2'b10: Receive only. 2'b11: Transmit address (device + register address, write/read bit is 1) --> Restart --> Transmit address (device address) --> Receive data.
0	RW	0x0	i2c_en I2c module enable. 1'b0: Disable 1'b1: Enable

RKI2C_CLKDIV

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CLKDIVH SCL high level clock count. T(SCL_HIGH) = Tclk_i2c * (CLKDIVH + 1) * 8.
15:0	RW	0x0001	CLKDIVL SCL low level clock count. T(SCL_LOW) = Tclk_i2c * (CLKDIVL + 1) * 8.

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RKI2C_MRXADDR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	addhvld Address high byte valid. 1'b0: Invalid 1'b1: Valid
25	RW	0x0	addmvld Address middle byte valid. 1'b0: Invalid 1'b1: Valid
24	RW	0x0	addlvld Address low byte valid. 1'b0: Invalid 1'b1: Valid
23:0	RW	0x000000	saddr Master address register. The lowest bit indicate write or read. 24 bits address register.

RKI2C_MRXRADDR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	sraddhvld Address high byte valid. 1'b0: Invalid 1'b1: Valid
25	RW	0x0	sraddmvld Address middle byte valid. 1'b0: Invalid 1'b1: Valid
24	RW	0x0	sraddlvld Address low byte valid. 1'b0: Invalid 1'b1: Valid
23:0	RW	0x000000	sraddr Slave register address accessed. 24 bits register address

RKI2C_MTXCNT

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	mtxcnt Master transmit count. 6 bits counter

RKI2C_MRXCNT

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	mrxcnt Master rx count. 6 bits counter

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RKI2C_IEN

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	slavehdsdaen Slave hold sda interrupt enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	slavehdsclen Slave hold scl interrupt enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	nakrcvien NAK handshake received interrupt enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	stopien Stop operation finished interrupt enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	startien Start operation finished interrupt enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	mbrfien MRXCNT data received finished interrupt enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	mbtfien MTXCNT data transfer finished interrupt enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	brfien Byte rx finished interrupt enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	btfien Byte tx finished interrupt enable. 1'b0: Disable 1'b1: Enable

RKI2C_IPD

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	slavehdsdaipd Slave hold sda interrupt pending bit. 1'b0: No interrupt available. 1'b1: Slave hold sda interrupt appear, write 1 to clear.
7	RW	0x0	slavehdsclipd Slave hold scl interrupt pending bit. 1'b0: No interrupt available. 1'b1: Slave hold scl interrupt appear, write 1 to clear.

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Bit	Attr	Reset Value	Description
6	W1C	0x0	nakrcvipd NAK handshake received interrupt pending bit. 1'b0: No interrupt available. 1'b1: NAK handshake received interrupt appear, write 1 to clear.
5	W1C	0x0	stopipd Stop operation finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Stop operation finished interrupt appear, write 1 to clear.
4	W1C	0x0	startipd Start operation finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Start operation finished interrupt appear, write 1 to clear.
3	W1C	0x0	mbrfipd MRXCNT data received finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: MRXCNT data received finished interrupt appear, write 1 to clear.
2	W1C	0x0	mbtfipd MTXCNT data transfer finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: MTXCNT data transfer finished interrupt appear, write 1 to clear.
1	W1C	0x0	brfipd Byte rx finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Byte rx finished interrupt appear, write 1 to clear.
0	W1C	0x0	btfipd Byte tx finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Byte tx finished interrupt appear, write 1 to clear.

RKI2C_FCNT

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	fcnt The count of data which has been transmitted or received for debug purpose.

RKI2C_SCL_OE_DB

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x20	scl_oe_db Slave hold scl debounce. Cycles for debounce (unit: Tclk_i2c).

RKI2C_TXDATA0

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata0 Data0 to be transmitted. 32 bits data

RKI2C_TXDATA1

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Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata1 Data1 to be transmitted. 32 bits data

RKI2C_TXDATA2

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata2 Data2 to be transmitted. 32 bits data

RKI2C_TXDATA3

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata3 Data3 to be transmitted. 32 bits data

RKI2C_TXDATA4

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata4 Data4 to be transmitted. 32 bits data

RKI2C_TXDATA5

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata5 Data5 to be transmitted. 32 bits data

RKI2C_TXDATA6

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata6 Data6 to be transmitted. 32 bits data

RKI2C_TXDATA7

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata7 Data7 to be transmitted. 32 bits data

RKI2C_RXDATA0

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata0 Data0 received. 32 bits data

RKI2C_RXDATA1

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Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata1 Data1 received. 32 bits data

RKI2C_RXDATA2

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata2 Data2 received. 32 bits data

RKI2C_RXDATA3

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata3 Data3 received. 32 bits data

RKI2C_RXDATA4

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata4 Data4 received. 32 bits data

RKI2C_RXDATA5

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata5 Data5 received. 32 bits data

RKI2C_RXDATA6

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata6 Data6 received. 32 bits data

RKI2C_RXDATA7

Address: **Operational Base** + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata7 Data7 received. 32 bits data

RKI2C_ST

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	scl_st SCL status. 1'b0: SCL status low. 1'b0: SCL status high.

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Bit	Attr	Reset Value	Description
0	RO	0x0	sda_st SDA status. 1'b0: SDA status low. 1'b0: SDA status high.

RKI2C_DBGCTRL

Address: **Operational Base** + offset (0x0224)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	h0_check_scl 1'b0: Check if scl been pull down by slave at the whole SCL_HIGH. 1'b1: Check if scl been pull down by slave only at the h0 of SCL_HIGH(SCL_HIGH including h0~h7).
13	RW	0x0	nak_release_scl 1'b0: Hold scl as low when recieved nack. 1'b1: Release scl as high when recieved nack.
12	RW	0x0	flt_en SCL edage glitch filter enable. 1'b0: Disable 1'b1: Enable
11:8	RW	0x0	slv_hold_scl_th Slave hold scl threshold = slv_hold_scl_db * Tclk_i2c.
7:4	RW	0x0	flt_r Filter scl rising edge glitches of width less than flt_r * Tclk_i2c.
3:0	RW	0x0	flt_f Filter scl falling edge glitches of width less than flt_f * Tclk_i2c.

RKI2C_CON1

Address: **Operational Base** + offset (0x0228)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	auto_stop_nak Auto stop when i2c master recieved nak from slave. Work when CON1[0]=1'b1. 1'b0: Do not auto stop when recieved nak. 1'b1: Auto stop when recieved nak.
1	RW	0x0	auto_stop_tx_end Auto stop when i2c master tx end. Work when CON1[0]=1'b1. 1'b0: Do not auto stop when tx end. 1'b1: Auto stop when tx end.
0	RW	0x0	auto_stop Auto stop when i2c master recieved nak from slave or tx end. 1'b0: Do not auto stop when recieved nak or tx end. 1'b1: Auto stop when recieved nak or tx end.

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32.5 Interface Description

Table 32-1 I2C Interface Description

Module pin	Pad Name	IOMUX Setting
I2C0_SCL_M0	AUPLL_CLK_IN_M1/SPI2_CSN0_M0/I2C0_SCL_M0/GPIO0_B0_z	PMU0_IOC_GPIO0B_IOMUX_SEL_L[3:0] = 0xb
I2C0_SDA_M0	SPI2_MISO_M0/I2C0_SDA_M0/GPIO0_B1_z	PMU0_IOC_GPIO0B_IOMUX_SEL_L[7:4] = 0xb
I2C0_SCL_M1	I2C0_SCL_M1/UART8_TX_M2/I3C0_SCL_M0/GPIO0_C1_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[7:4] = 0x9
I2C0_SDA_M1	I2C0_SDA_M1/UART8_RX_M2/I3C0_SDA_M0/GPIO0_C2_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[11:8] = 0x9
I2C1_SCL_M0	SPI2_CLK_M0/I2C1_SCL_M0/GPIO0_B2_z	PMU0_IOC_GPIO0B_IOMUX_SEL_L[11:8] = 0xb
I2C1_SDA_M0	SPI2_MOSI_M0/I2C1_SDA_M0/GPIO0_B3_z	PMU0_IOC_GPIO0B_IOMUX_SEL_L[15:12] = 0xb
I2C1_SCL_M1	REF_CLK1_OUT/I2C1_SCL_M1/UART4_TX_M2/PWM1_CH0_M0/GPIO0_B4_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[3:0] = 0x9
I2C1_SDA_M1	REF_CLK2_OUT/I2C1_SDA_M1/UART4_RX_M2/PWM1_CH1_M0/GPIO0_B5_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[7:4] = 0x9
I2C2_SCL_M0	I2C2_SCL_M0/UART1_TX_M0/NPU_AVS/PWM1_CH4_M0/GPIO0_B7_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[15:12] = 0x9
I2C2_SDA_M0	I2C2_SDA_M0/UART1_RX_M0/CPULIT_AVS/PWM1_CH3_M0/GPIO0_C0_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[3:0] = 0x9
I2C2_SCL_M1	EMMC_D0/FSPI0_D0/SAI0_SCLK_M2/UART7_RTSN_M1/I2C2_SCL_M1/GPIO1_A0_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[3:0] = 0xa
I2C2_SDA_M1	EMMC_D1/FSPI0_D1/SAI0_LRCK_M2/UART7_CTSN_M1/I2C2_SDA_M1/GPIO1_A1_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[7:4] = 0xa
I2C2_SCL_M2	SAI1_SCLK_M0/FLEXBUS1_CSN_M4/SPI3_CSN0_M2/UART5_RTSN_M1/I2C2_SCL_M2/PWM2_CH4_M1/GPIO4_A3_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[15:12] = 0xb
I2C2_SDA_M2	SAI1_LRCK_M0/FLEXBUS1_D12_M1/SPI4_CSN1_M2/UART5_CTSN_M1/I2C2_SDA_M2/PCIE1_CLKREQN_M2/GPIO4_A5_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[7:4] = 0xb
I2C2_SCL_M3	DSM_AUD_RP_M1/HDMI_TX_SCL/I2C2_SCL_M3/CAN0_TX_M1/UART9_TX_M2/PWM2_CH0_M1/GPIO4_C2_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[11:8] = 0xb
I2C2_SDA_M3	DSM_AUD_RN_M1/HDMI_TX_SDA/I2C2_SDA_M3/CAN0_RX_M1/UART9_RX_M2/PWM2_CH1	VCCIO6_IOC_GPIO4C_IOM

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	_M1/GPIO4_C3_d	UX_SEL_L[15:12] = 0xb
I2C3_SCL_M0	SPDIF_TX0_M0/FLEXBUS0_D15_M1/UART2_TX_M1/I2C3_SCL_M0/PCIE0_CLKREQN_M2/CAN1_TX_M2/GPIO4_B5_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[7:4] = 0xb
I2C3_SDA_M0	SPDIF_RX0_M0/FLEXBUS0_CSN_M4/UART2_RX_M1/I2C3_SDA_M0/CAN1_RX_M2/GPIO4_B4_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[3:0] = 0xb
I2C3_SCL_M1	SAI0_SCLK_M1/I2C3_SCL_M1/SPI0_CSN0_M0/GPIO0_C6_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[11:8] = 0x9
I2C3_SDA_M1	SAI0_LRCK_M1/I2C3_SDA_M1/SPI0_CLK_M0/GPIO0_C7_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[15:12] = 0x9
I2C3_SCL_M2	VO_LCDC_DEN/VO_EBC_SDLE/SAI1_SDI1_M1/DSMC_DATA0/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 0xb
I2C3_SDA_M2	VO_LCDC_HSYNC/VO_EBC_GDCLK/SAI1_SDI2_M1/DSMC_CLKP/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 0xb
I2C3_SCL_M3	ISP_PRELIGHT_TRIG_M1/SAI4_LRCK_M2/DP_HPDIN_M0/I2C3_SCL_M3/SPI4_CSN0_M0/UART6_TX_M3/PWM2_CH6_M1/GPIO4_C4_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[3:0] = 0xb
I2C3_SDA_M3	ISP_FLASH_TRIGOUT_M1/SAI4_SDO_M2/VP0_SYNC_OUT/SATA1_ACTLED_M1/I2C3_SDA_M3/SPI4_MOSI_M0/UART6_RX_M3/PWM2_CH5_M1/GPIO4_C5_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[7:4] = 0xb
I2C4_SCL_M0	SAI0_SDI2_M1/SAI0_SDO2_M1/PDM0_SDI2_M0/I2C4_SCL_M0/CPUBIG_AVS/PWM1_CH5_M0/UART1_CTSN_M0/GPIO0_D2_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[11:8] = 0x9
I2C4_SDA_M0	SAI0_SDI3_M1/SAI0_SDO1_M1/PDM0_SDI3_M0/I2C4_SDA_M0/GPU_AVS/PWM2_CH0_M0/UART1_RTSN_M0/GPIO0_D3_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[15:12] = 0x9
I2C4_SCL_M1	SAI4_SCLK_M0/PDM1_SDI3_M1/FLEXBUS0_D13_M1/SPI3_MOSI_M2/UART6_TX_M0/I2C4_SCL_M1/CAN0_TX_M2/GPIO4_A4_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[3:0] = 0xb
I2C4_SDA_M1	SAI4_LRCK_M0/PDM1_CLK0_M1/FLEXBUS0_D14_M1/SPI3_MISO_M2/UART6_RX_M0/I2C4_SDA_M1/CAN0_RX_M2/GPIO4_A6_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[11:8] = 0xb
I2C4_SCL_M2	VI_CIF_D15/SDMMC1_D0_M1/ETH0_RXD0_M1/SAI0_SDO0_M0/UART8_TX_M1/SPI4_CSN1_M3/I2C4_SCL_M2/GPIO2_A6_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[11:8] = 0xb
I2C4_SDA_M2	VI_CIF_D14/SDMMC1_D1_M1/ETH0_TXCTL_M1/SAI0_SDO1_M0/UART8_RX_M1/I2C4_SDA_M2/GPIO2_A7_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[15:12] = 0xb
I2C4_SCL_M3	VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/DSMC_DATA7/FLEXBUS1_D9/UART2_TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0] = 0xb
I2C4_SDA_M3	VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12] = 0xb
I2C5_SCL_M0	SDMMC0_CLK/FSPI1_CLK_M0/SAI3_SCLK_M3/TEST_CLK_OUT/UART5_TX_M2/I2C5_SCL_M0/SPI0_CLK_M1/I3C1_SDA_PU_M1/GPIO2_A5_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[7:4] = 0xb

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I2C5_SDA_M0	SDMMC0_CMD/FSPI1_CSN0_M0/SAI3_SDO_M3/UART5_RX_M2/I2C5_SDA_M0/SPI0_CSN0_M1/PWM2_CH4_M0/GPIO2_A4_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[3:0] = 0xb
I2C5_SCL_M1	ETH1_MCLK_M1/SAI2_MCLK_M0/PDM0_SDI3_M2/SPDIF_RX1_M2/UART10_RTSN_M1/I2C5_SCL_M1/GPIO1_D4_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[3:0] = 0xa
I2C5_SDA_M1	ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4] = 0xa
I2C5_SCL_M2	ETH1_TXD0_M0/SAI4_SCLK_M3/UART4_CTSN_M0/I2C5_SCL_M2/PWM1_CH5_M2/GPIO2_C6_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[11:8] = 0xb
I2C5_SDA_M2	ETH1_TXD1_M0/SAI4_LRCK_M3/UART4_RTSN_M0/I2C5_SDA_M2/PWM0_CH1_M2/GPIO2_C7_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[15:12] = 0xb
I2C5_SCL_M3	VO_LCDC_D7/VO_EBC_SDDO7/SAI1_SDO1_M1/DSMC_DATA5/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/CAN0_TX_M3/GPIO3_C4_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[3:0] = 0xb
I2C5_SDA_M3	VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 0xb
I2C6_SCL_M0	CLK_32K_IN/CLK0_32K_OUT/I2C6_SCL_M0/GPIO0_A2_d	PMU0_IOC_GPIO0A_IOMUX_SEL_L[11:8] = 0xb
I2C6_SDA_M0	PWR_CTRL3/I2C6_SDA_M0/GPIO0_A5_d	PMU0_IOC_GPIO0A_IOMUX_SEL_H[7:4] = 0xb
I2C6_SCL_M1	ETH1_PPSCLK_M1/SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_CSN1_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[11:8] = 0xa
I2C6_SDA_M1	ETH1_PPSTRIG_M1/SDMMC1_DETN_M0/FSPI1_CSN0_M1/UART4_CTSN_M1/I2C6_SDA_M1/SPI2_CSN0_M1/GPIO1_C3_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[15:12] = 0xa
I2C6_SCL_M2	ETH1_TXCTL_M0/SAI4_SDI_M3/UART4_TX_M0/I2C6_SCL_M2/PWM2_CH0_M2/GPIO2_D0_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[3:0] = 0xb
I2C6_SDA_M2	ETH1_RXD0_M0/SAI4_SDO_M3/UART4_RX_M0/I2C6_SDA_M2/PWM2_CH1_M2/GPIO2_D1_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[7:4] = 0xb
I2C6_SCL_M3	SAI4_SDI_M2/VP1_SYNC_OUT/PCIE0_CLKREQN_M3/SATA0_ACTLED_M1/I2C6_SCL_M3/SPI4_MISO_M0/CAN1_TX_M1/PWM2_CH2_M1/GPIO4_C6_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[11:8] = 0xb
I2C6_SDA_M3	SAI4_SCLK_M2/VP2_SYNC_OUT/I2C6_SDA_M3/SPI4_CLK_M0/CAN1_RX_M1/PWM2_CH3_M1/GPIO4_C7_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[15:12] = 0xb
I2C7_SCL_M0	EMMC_CMD/FSPI0_RSTN/FSPI0_CSN1/UART6_TX_M2/I2C7_SCL_M0/GPIO1_B0_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[3:0] = 0xa
I2C7_SDA_M0	EMMC_RSTN/FSPI0_CSN0/UART6_RX_M2/I2C7_SDA_M0/MIPI_TE_M3/PWM2_CH1_M0/GPIO1_B3_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[15:12] = 0xa
I2C7_SCL_M1	VI_CIF_HREF/ETH0_MDIO_M1/SAI3_SCLK_M2/UART3_TX_M0/SPI3_CLK_M0/I2C7_SCL_M1/GPIO3_A0_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[3:0] = 0xb
I2C7_SDA_M1	VI_CIF_VSYNC/ETH1_PPSTRIG_M0/ETH0_MDC_M1/SAI3_LRCK_M2/UART3_RX_M0/SPI3_M	TOP_IOC_GPIO3A_IOMUX_

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	OSI_M0/I2C7_SDA_M1/GPIO3_A1_d	SEL_L[7:4] = 0xb
I2C7_SCL_M2	SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0] = 0xb
I2C7_SDA_M2	VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/DSMC_INT2/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[7:4] = 0xb
I2C7_SCL_M3	DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[3:0] = 0xb
I2C7_SDA_M3	DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[7:4] = 0xb
I2C8_SCL_M0	SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/CAN0_RX_M0/PWM2_CH2_M0/GPIO2_A0_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[3:0] = 0xb
I2C8_SDA_M0	SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4] = 0xb
I2C8_SCL_M1	ETH1_TXCTL_M1/FSPI1_D2_M1/PDM0_SDI0_M2/UART2_TX_M0/I2C8_SCL_M1/SATA_CPPOD/GPIO1_C6_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[11:8] = 0xa
I2C8_SDA_M1	ETH1_RXD0_M1/FSPI1_D3_M1/PDM0_SDI1_M2/UART2_RX_M0/I2C8_SDA_M1/SATA_CPDET/GPIO1_C7_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[15:12] = 0xa
I2C8_SCL_M2	VI_CIF_D7/ETH1_PTP_REFCLK_M1/ETH0_RXD3_M1/SAI0_SCLK_M0/UART7_TX_M0/UART8_RTSN_M1/I2C8_SCL_M2/GPIO2_B6_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[11:8] = 0xb
I2C8_SDA_M2	VI_CIF_D6/ETH0_RXD2_M1/SAI0_LRCK_M0/UART7_RX_M0/UART8_CTSN_M1/I2C8_SDA_M2/GPIO2_B7_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[15:12] = 0xb
I2C8_SCL_M3	VO_LCDC_D16/VO_EBC_SDCE0/ETH0_TXCTL_M0/PDM1_SDI0_M2/DSMC_DATA10/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[15:12] = 0xb
I2C8_SDA_M3	VO_LCDC_D17/VO_EBC_SDCE1/ETH0_RXD0_M0/PDM1_SDI1_M2/DSMC_DATA11/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[11:8] = 0xb
I2C9_SCL_M0	EMMC_D5/SAI3_SCLK_M0/PDM0_SDI2_M1/SPI0_MOSI_M2/I2C9_SCL_M0/GPIO1_A5_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[7:4] = 0xa
I2C9_SDA_M0	EMMC_D6/SAI3_LRCK_M0/PDM0_CLK1_M1/SPI0_MISO_M2/I2C9_SDA_M0/GPIO1_A6_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[11:8] = 0xa
I2C9_SCL_M1	ETH1_RXD3_M1/SDMMC1_D1_M0/SAI3_LRCK_M1/I2C9_SCL_M1/SPI1_MOSI_M0/PWM1_CH1_M1/GPIO1_B5_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[7:4] = 0xa
I2C9_SDA_M1	ETH1_RXD2_M1/SDMMC1_D0_M0/SAI3_SCLK_M1/I2C9_SDA_M1/SPI1_CLK_M0/PCIE1_CLKREQN_M1/PWM1_CH0_M1/GPIO1_B4_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[3:0] = 0xa
I2C9_SCL_M2	ISP_FLASH_TRIGOUT_M0/ETH1_MDIO_M0/UART6_CTSN_M1/I2C9_SCL_M2/PWM2_CH5_M2/GPIO2_D5_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[7:4] = 0xb

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I2C9_SDA_M2	ISP_PRELIGHT_TRIG_M0/ETH1_MDC_M0/UART6_RTSN_M1/I2C9_SDA_M2/PWM2_CH4_M2/GPIO2_D4_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[3:0] = 0xb
I2C9_SCL_M3	VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 0xb
I2C9_SDA_M3	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 0xb

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32.6 Application Notes

The I2C controller core operation flow chart below is to describe how the software configures and performs an I2C transaction through this I2C controller core. Descriptions are divided into 3 sections, transmit only mode, receive only mode, and mix mode. Users are strongly advised to follow:

- Transmit only mode (I2C_CON[1:0]=2'b00)

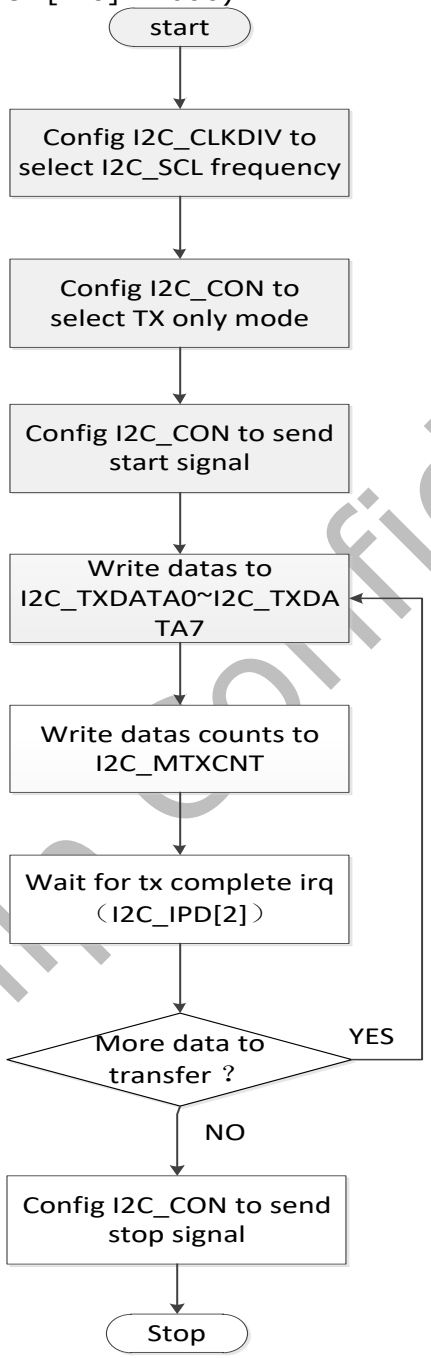

Fig.32-6 I2C Flow chat for transmit only mode

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- Receive only mode (I2C_CON[1:0]=2'b10)

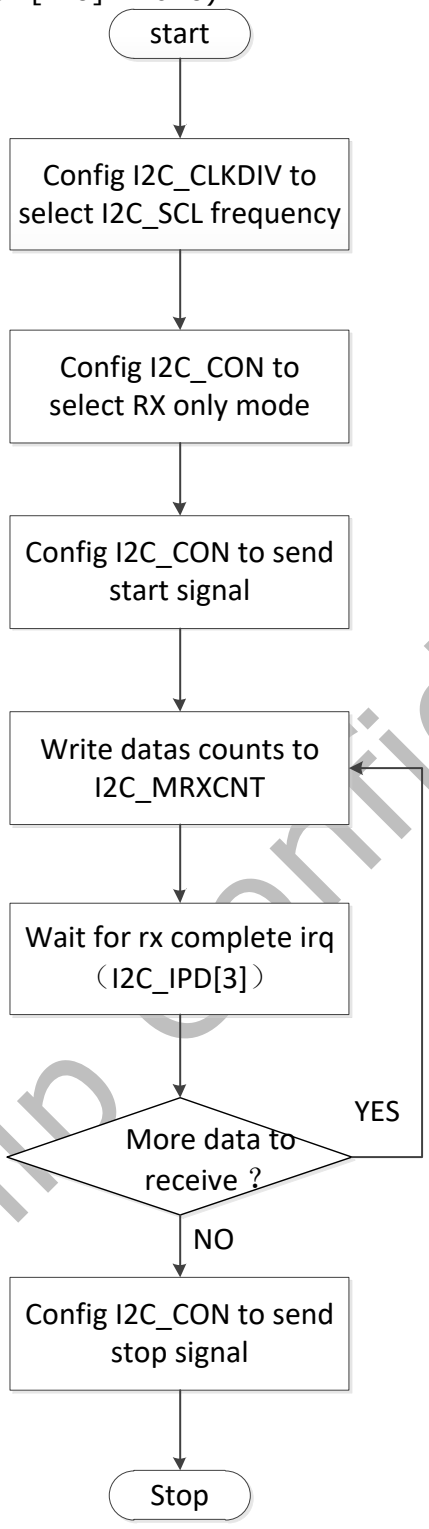

Fig.32-7 I2C Flow chat for receive only mode

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- Mix mode (I2C_CON[1:0]=2'b01 or I2C_CON[1:0]=2'b11)

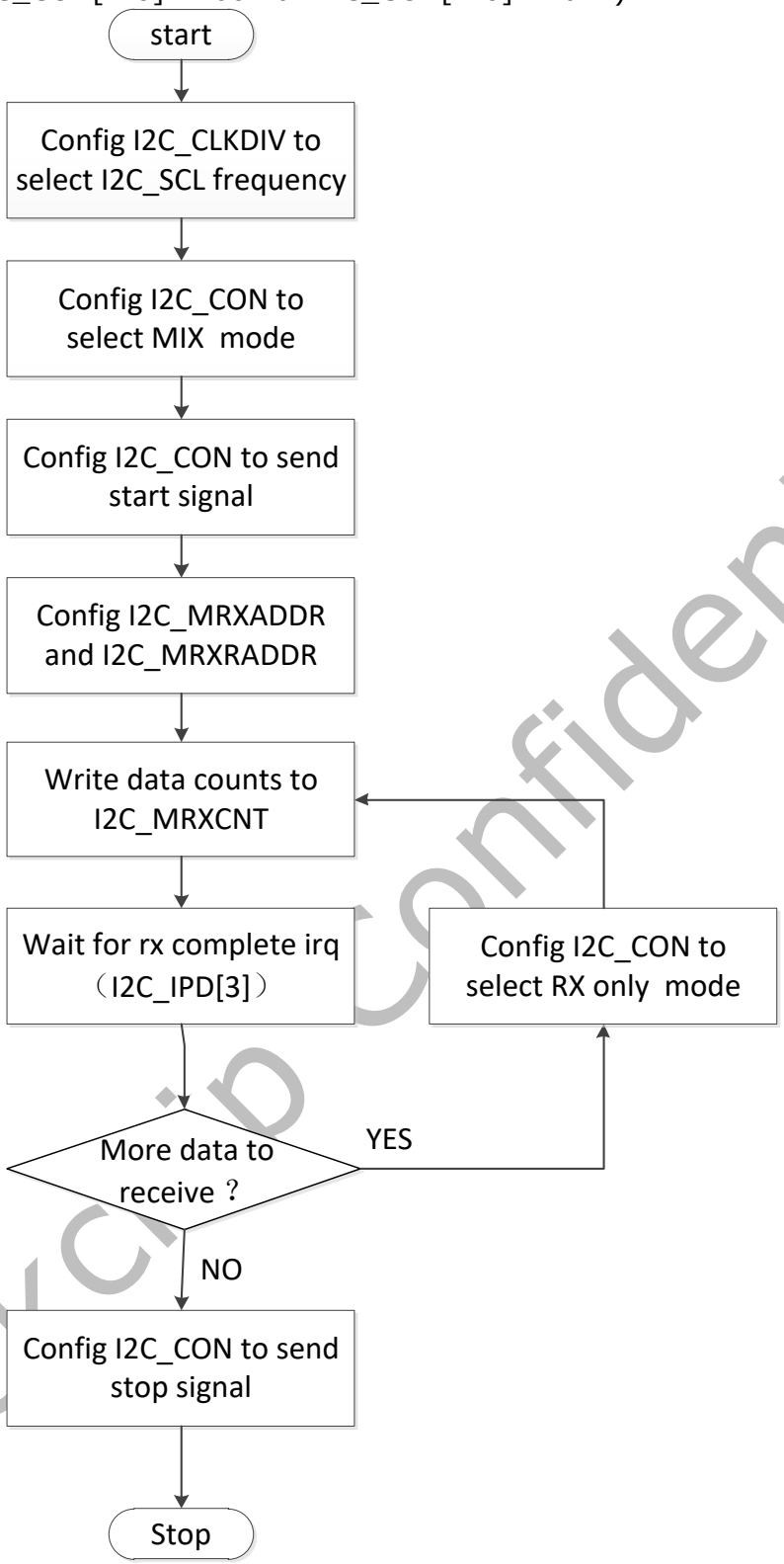

Fig.32-8 I2C Flow chat for mix mode

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Chapter 33 UART

33.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

UART Controller supports the following features:

- Support 12 independent UART controller: UART0-UART11
- All contain two 64 Bytes FIFOs for data receive and transmit
- UART1-UART11 support auto flow-control
- UART1-UART11 support RS485 function
- Support bit rates 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps, 8Mbps
- Support programmable baud rates, even with non-integer clock divider
- Standard asynchronous communication bits (start, stop and parity)
- Support interrupt-based or DMA-based mode
- Support 5-8 bits width transfer

33.2 Block Diagram

This section provides a description about the functions and behavior under various conditions. The UART Controller comprises with:

- AMBA APB interface
- FIFO controllers
- Register block
- Modem synchronization block and baud clock generation block
- Serial receiver and serial transmitter

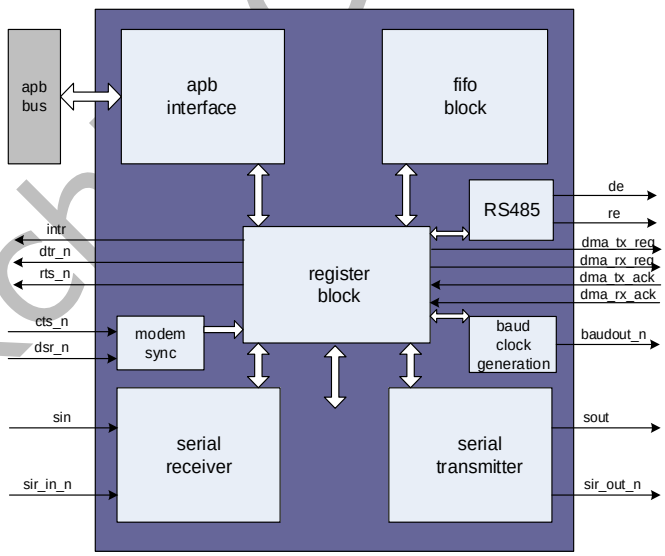

Fig. 33-1 UART Architecture

APB INTERFACE

The host processor accesses data, control, and status information on the UART through the APB interface. The UART supports APB data bus widths of 8, 16, and 32 bits.

Register block

Be responsible for the main UART functionality including control, status and interrupt generation.

Modem Synchronization block

Synchronizes the modem input signal.

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FIFO block
Be responsible for FIFO control and storage (when using internal RAM) or signaling to control external RAM (when used).

Baud Clock Generator
Generates the transmitter and receiver baud clock along with the output reference clock signal (baudout_n).

Serial Transmitter
Converts the parallel data, written to the UART, into serial form and adds all additional bits, as specified by the control register, for transmission.

Serial Receiver
Converts the serial data character (as specified by the control register) received to parallel form. Parity error detection, framing error detection and line break detection is carried out in this block.

33.3 Function Description

UART Serial Protocol
Because the serial communication is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. An additional parity bit may be added to the serial character. This bit appears after the last data bit and before the stop bit(s) in the character structure to perform simple error checking on the received data, as shown in Figure.

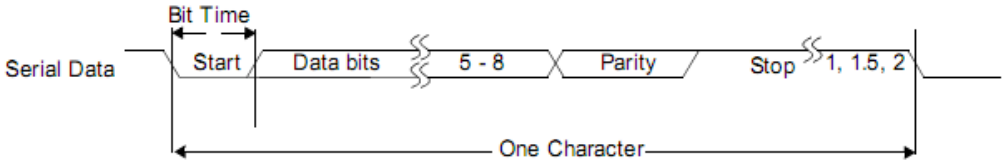

Fig. 33-2 UART Serial protocol

Baud Clock
The baud rate is controlled by the serial clock (sclk or pclk in a single clock implementation) and the Divisor Latch Register (DLH and DLL). As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit.

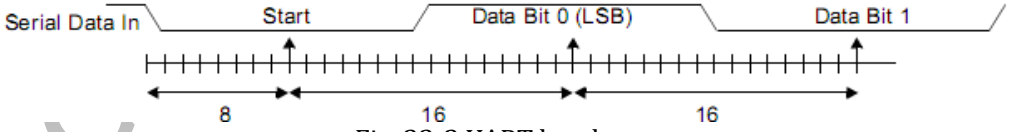

Fig. 33-3 UART baud rate

FIFO Support
1. NONE FIFO MODE
If FIFO support is not selected, then no FIFOs are implemented and only a single receive data byte and transmit data byte can be stored at a time in the RBR and THR.

2. FIFO MODE
The FIFO depth of is 64bytes. The FIFO mode of all the UART is enabled by register FCR[0].

Interrupts
The following interrupt types can be enabled with the IER register.
- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)
- Transmitter Holding Register Empty at/below threshold (in Programmable THRE Interrupt mode)

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- Modem Status

DMA Support

The UART supports DMA signaling with the use of two output signals (dma_tx_req_n and dma_rx_req_n) to indicate when data is ready to be read or when the transmit FIFO is empty.

The dma_tx_req_n signal is asserted under the following conditions:

- When the Transmitter Holding Register is empty in non-FIFO mode.
- When the transmitter FIFO is empty in FIFO mode with Programmable THRE interrupt mode disabled.
- When the transmitter FIFO is at, or below the programmed threshold with Programmable THRE interrupt mode enabled.

The dma_rx_req_n signal is asserted under the following conditions:

- When there is a single character available in the Receive Buffer Register in non-FIFO mode.
- When the Receiver FIFO is at or above the programmed trigger level in FIFO mode.

Auto Flow Control

The UART can be configured to have a 16750-compatible Auto RTS and Auto CTS serial data flow control mode available. If FIFOs are not implemented, then this mode cannot be selected. When Auto Flow Control mode has been selected, it can be enabled with the Modem Control Register (MCR[5]). Following figure shows a block diagram of the Auto Flow Control functionality.

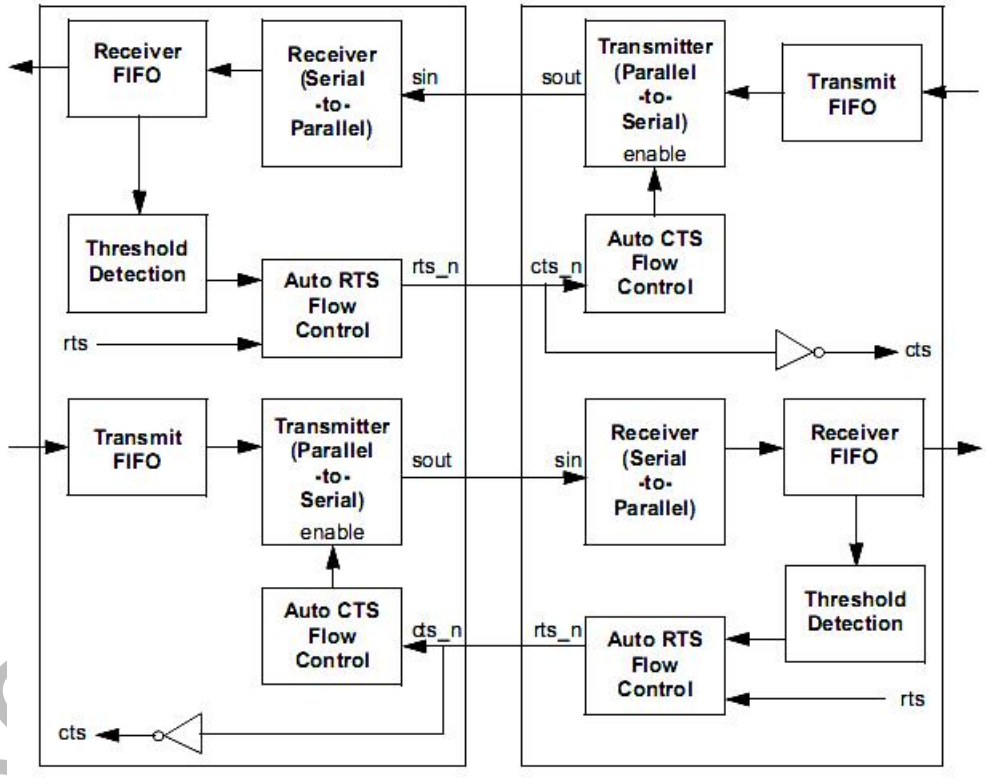

Fig. 33-4 UART Auto flow control block diagram

Auto RTS – Becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- RTS (MCR[1] bit and MCR[5]bit are both set)
- FIFOs are enabled (FCR[0]) bit is set)
- SIR mode is disabled (MCR[6] bit is not set)

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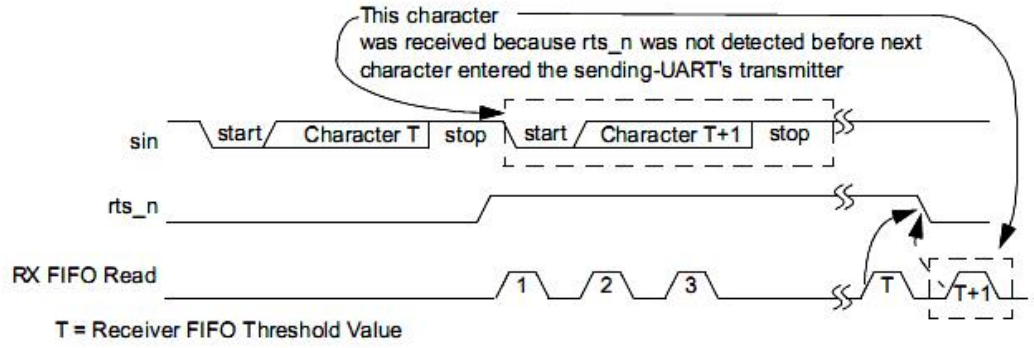

Fig. 33-5 UART AUTO RTS TIMING

Auto CTS – becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- AFCE (MCR[5] bit is set)
- FIFOs are enabled through FIFO Control Register FCR[0] bit
- SIR mode is disabled (MCR[6] bit is not set)

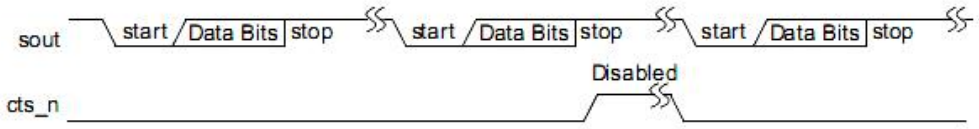

Fig. 33-6 UART AUTO CTS TIMING

RS485 Mode

The RS485 standard supports serial communication over a twisted pair configuration. The difference between the RS232 and RS485 standards is its use of a balanced line for transmission. This usage is also known as the differential format that sends the same signal on two separate lines with phase delay and then compares the signals at the end, subtracts any noise, and adds them to regain signal strength. This process allows the RS485 standard to be viable over significantly longer distances than its short range RS232 counterpart.

UART supports hardware mode and software mode.

- Hardware mode, DE and RE are mutually exclusive. By default 'de' and 're' will be disabled. When at user mode, user should programs the DE to active the 'de', while at auto mode, DE will assert when transfer starts. Once the TX FIFO becomes empty and the stop bit be sampled, 're' signal gets enabled and 'de' signal will be disabled, automatically. In this mode, hardware will consider the de-inactive timing and turn around timing, which are programmed in the DET and TAT register, respectively. When 'de' is valid, it is useless to configure RE, and vice versa.
- Software mode, transmit and receive can happen simultaneously. The user can enable DE, RE at any point of time. Turn around timing as programmed in the TAT register and de-inactive timing as programmed in the DET are not applicable in this mode.

33.4 Register Description

33.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
UART0	0x2AD40000
UART1	0x27310000
UART2	0x2AD50000
UART3	0x2AD60000
UART4	0x2AD70000

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Name	Base Address
UART5	0x2AD80000
UART6	0x2AD90000
UART7	0x2ADA0000
UART8	0x2ADB0000
UART9	0x2ADC0000
UART10	0x2AFC0000
UART11	0x2AFD0000

33.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
UART_RBR	0x0000	W	0x00000000	Receive Buffer Register
UART_DLL	0x0000	W	0x00000000	Divisor Latch Low
UART_THR	0x0000	W	0x00000000	Transmit Buffer Register
UART_DLH	0x0004	W	0x00000000	Divisor Latch High
UART_IER	0x0004	W	0x00000000	Interrupt Enable Register
UART_FCR	0x0008	W	0x00000000	FIFO Enable
UART_IIR	0x0008	W	0x00000001	Interrupt Identity Register
UART_LCR	0x000C	W	0x00000000	Line Control Register
UART_MCR	0x0010	W	0x00000000	Modem Control Register
UART_LSR	0x0014	W	0x00000060	Line Status Register
UART_MSR	0x0018	W	0x00000000	Modem Status Register
UART_SCR	0x001C	W	0x00000000	Scratchpad Register
UART_SRBR	0x0030	W	0x00000000	Shadow Receive Buffer Register
UART_STHR	0x0030	W	0x00000000	Shadow Transmit Holding Register
UART_FAR	0x0070	W	0x00000000	FIFO Access Register
UART_TFR	0x0074	W	0x00000000	Transmit FIFO Read
UART_RFW	0x0078	W	0x00000000	Receive FIFO write
UART_USR	0x007C	W	0x00000006	UART Status Register
UART_TFL	0x0080	W	0x00000000	Transmit FIFO level
UART_RFL	0x0084	W	0x00000000	Receive FIFO level
UART_SRR	0x0088	W	0x00000000	Software Reset Register
UART_SRTS	0x008C	W	0x00000000	Shadow Request to Send
UART_SBCR	0x0090	W	0x00000000	Shadow Break Control Register
UART_SDMAM	0x0094	W	0x00000000	Shadow DMA Mode
UART_SFE	0x0098	W	0x00000000	Shadow FIFO enable
UART_SRT	0x009C	W	0x00000000	Shadow RCVR Trigger
UART_STET	0x00A0	W	0x00000000	Shadow TX Empty Trigger
UART_HTX	0x00A4	W	0x00000000	Halt TX
UART_DMASA	0x00A8	W	0x00000000	DMA Software Acknowledge
UART_TCR	0x00AC	W	0x00000000	Transceiver Control Register
UART_DE	0x00B0	W	0x00000000	Driver Output Enable Register
UART_RE	0x00B4	W	0x00000000	Receiver Output Enable Register
UART_DET	0x00B8	W	0x00000000	Driver Output Enable Timing Register
UART_TAT	0x00BC	W	0x00000000	Turn Around Timing Register
UART_CPR	0x00F4	W	0x00043FF2	Component Parameter Register
UART_UCV	0x00F8	W	0x3430322A	UART Component Version
UART_CTR	0x00FC	W	0x44570110	Component Type Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

33.4.3 Detail Registers Description

UART_RBR

Address: **Operational Base** + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	data_input Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

UART_DLL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	baud_rate_divisor_l Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

UART_THR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	data_output Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full.. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_DLH

Address: **Operational Base** + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	baud_rate_divisor_h Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

UART_IER

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	prog_thre_int_en Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. 1'b0: Disabled 1'b1: Enabled
6:4	RO	0x0	reserved
3	RW	0x0	modem_status_int_en Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	receive_line_status_int_en Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
1	RW	0x0	trans_hold_empty_int_en Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	receive_data_available_int_en Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1'b0: Disabled 1'b1: Enabled

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UART_FCR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	WO	0x0	rcvr_trigger at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to "DMA Support". The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full
5:4	WO	0x0	tx_empty_trigger TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to " DMA Support" . The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full
3	WO	0x0	dma_mode DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support. 1'b0: Mode 0 1'b1: Mode 1
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	fifo_en FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

UART_IIR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	fifos_en FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 2'b00: Disabled 2'b11: Enabled
5:4	RO	0x0	reserved
3:0	RO	0x1	int_id Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 4'b0000: Modem status 4'b0001: No interrupt pending 4'b0010: THR empty 4'b0100: Received data available 4'b0110: Receiver line status 4'b0111: Busy detect 4'b1100: Character timeout The interrupt priorities are split into four levels that are detailed in Table X. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

UART_LCR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	div_lat_access Divisor Latch Access Bit. Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	RW	0x0	break_ctrl Break Control Bit.This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	RW	0x0	stick_parity If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	RW	0x0	even_parity_sel Even Parity Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.

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Bit	Attr	Reset Value	Description
3	RW	0x0	parity_en Parity Enable. Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 1'b0: Parity disabled 1'b1: Parity enabled
2	RW	0x0	stop_bits_num Number of stop bits. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 1'b0: 1 stop bit. 1'b1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit.
1:0	RW	0x0	data_length_sel Data Length Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 2'b00: 5 bits 2'b01: 6 bits 2'b10: 7 bits 2'b11: 8 bits

UART_MCR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sir_mode_en SIR Mode Enable. Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in "IrDA 1.0 SIR Protocol". 1'b0: IrDA SIR Mode disabled 1'b1: IrDA SIR Mode enabled
5	RW	0x0	auto_flow_ctrl_en Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in "Auto Flow Control". 1'b0: Auto Flow Control Mode disabled 1'b1: Auto Flow Control Mode enabled

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Bit	Attr	Reset Value	Description
4	RW	0x0	loopback LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	RW	0x0	out2 OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 1'b0: Out2_n de-asserted (logic 1) 1'b1: Out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	RW	0x0	out1 OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 1'b0: Out1_n de-asserted (logic 1) 1'b1: Out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	RW	0x0	req_to_send Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	RW	0x0	data_terminal_ready Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 1'b0: dtr_n de-asserted (logic 1) 1'b1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive

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UART_LSR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	receiver_fifo_error Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 1'b0: No error in RX FIFO 1'b1: Error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	RO	0x1	trans_empty Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	RO	0x1	trans_hold_reg_empty Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	RO	0x0	break_int Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.

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Bit	Attr	Reset Value	Description
3	RO	0x0	framing_error Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No framing error 1'b1: Framing error Reading the LSR clears the FE bit.
2	RO	0x0	parity_error Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No parity error 1'b1: Parity error Reading the LSR clears the PE bit.
1	RO	0x0	overrun_error Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 1'b0: No overrun error 1'b1: Overrun error Reading the LSR clears the OE bit.
0	RO	0x0	data_ready Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 1'b0: No data ready 1'b1: Data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

UART_MSR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RO	0x0	data_carrior_detect Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 1'b0: dcd_n input is de-asserted (logic 1) 1'b1: dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	RO	0x0	ring_indicator Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 1'b0: ri_n input is de-asserted (logic 1) 1'b1: ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	RO	0x0	data_set_ready Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the UART. 1'b0: dsr_n input is de-asserted (logic 1) 1'b1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	RO	0x0	clear_to_send Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART. 1'b0: cts_n input is de-asserted (logic 1) 1'b1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RO	0x0	delta_data_carrier_detect Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 1'b0: No change on dcd_n since last read of MSR 1'b1: Change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.

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Bit	Attr	Reset Value	Description
2	RO	0x0	trailing_edge_ring_indicator Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 1'b0: No change on ri_n since last read of MSR 1'b1: Change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	RO	0x0	delta_data_set_ready Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 1'b0: No change on dsr_n since last read of MSR 1'b1: Change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RO	0x0	delta_clear_to_send Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 1'b0: No change on ctsdsr_n since last read of MSR 1'b1: Change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

UART_SCR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	temp_store_space Scratchpad register.This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

UART_SRBR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	shadow_rbr This is a shadow register for the RBR and has been allocated sixteen 32-bit locations (0x30-0x6c) so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs.

UART_STHR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	shadow_thr This is a shadow register for the THR and has been allocated sixteen 32-bit locations(0x30-0x6c) so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_FAR

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fifo_access_test_en Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 1'b0: FIFO access mode disabled 1'b1: FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty.

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UART_TFR

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	trans_fifo_read Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR.

UART_RFW

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	WO	0x0	receive_fifo_framing_error Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	WO	0x0	receive_fifo_parity_error Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	WO	0x00	receive_fifo_write Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

UART_USR

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	receive_fifo_full Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. 1'b0: Receive FIFO not full 1'b1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.

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Bit	Attr	Reset Value	Description
3	RO	0x0	receive_fifo_not_empty Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. 1'b0: Receive FIFO is empty 1'b1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	RO	0x1	trasn_fifo_empty Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	RO	0x1	trans_fifo_not_full Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. 1'b0: Transmit FIFO is full 1'b1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	RO	0x0	uart_busy UART Busy. This is indicates that a serial transfer is in progress, when cleared indicates that the UART is idle or inactive. 1'b0: UART is idle or inactive 1'b1: UART is busy (actively transferring data) Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the UART has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the UART. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock.

UART_TFL

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	trans_fifo_level Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.

UART_RFL

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	receive_fifo_level Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.

UART_SRR

Address: **Operational Base** + offset (0x0088)

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Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	uart_reset UART Reset. This asynchronously resets the UART and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.

UART_SRTS

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_req_to_send Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.

UART_SBCR

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	shadow_break_ctrl Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver.

UART_SDMAM

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_dma_mode Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). 1'b0: Mode 0 1'b1: Mode 1

UART_SFE

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_fifo_en Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.

UART_SRT

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	shadow_rcvr_trigger Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated.This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full

UART_STET

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	shadow_tx_empty_trigger Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated.This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full

UART_HTX

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	halt_tx_en This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 1'b0: Halt TX disabled 1'b1: Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation.

UART_DMASA

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	WO	0x0	dma_software_ack This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

UART_TCR

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	auto_de Assert DE Automatically Enable. When data is written to the TXFIFO, the DE will automatically asserted, meanwhile, the RE will automatically de-asserted. 1'b0: Disable. 1'b1: Enable.
4	RW	0x0	re_pol Receiver Enable Polarity. 1'b0: re signal is active low. 1'b1: re signal is active high.
3	RW	0x0	de_pol Driver Enable Polarity. 1'b0: de signal is active high. 1'b1: de signal is active low.
2	RW	0x0	xfer_mode Transfer Mode. 1'b0: Hardware mode, DE and RE are mutually exclusive. By default 'de' and 're' will be disabled. User should programs the DE to active the 'de'. Once the TX FIFO becomes empty and the stop bit be sampled, 're' signal gets enabled and 'de' signal will be disabled, automatically. In this mode, hardware will consider the de-inactive timing and turn around timing (applied for 4 wire mode only), which are programmed in the DET and TAT register, respectively. When 'de' is valid, it is useless to configure RE, and vice versa. 1'b1: Software mode, transmit and receive can happen simultaneously. The user can enable DE, RE at any point of time. Turn around timing as programmed in the TAT register and de-inactive timing as programmed in the DET are not applicable in this mode.
1	RW	0x0	re_en Receiver Enable. 1'b0: RE signal disable, DE control both transmit and receive process. Correspondingly, assert DE for transmit state, while de-assert DE for receive state. In this scenario, RE-associated logics and TAT register will hold constant for lower power consumption. 1'b1: RE signal enable, DE control the transmit process, and RE control the receive process.
0	RW	0x0	rs485_en RS485 Enable. 1'b0: In this mode, the transfers are still in the RS232 mode. The registers of DE, RE, DET and TAT are reserved. 1'b1: In this mode, the transfers will happen in RS485 mode.

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UART_DE

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	de The 'de' register bit is used to control assertion and de-assertion of 'de' signal. 1'b0: De-assert 'de' signal. 1'b1: Assert 'de' signal.

UART_RE

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	re The 're' register bit is used to control assertion and de-assertion of 're' signal. 1'b0: De-assert 're' signal. 1'b1: Assert 're' signal.

UART_DET

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	de_inact_time This field controls the amount of time (in terms of number of pclk periods) between the finish flag after the sampling point of the stop bit on the sout to the falling edge of Driver output enable signal. Note that, the mentioned finish flag, i.e. the actual starting effective point of the count, is located at the position of (DLL+1) sclk periods before the full stop bit ends, followed by 3~4 synchronization pclk periods. The actual time is the programmed value + 1.

UART_TAT

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	de2re_time Turn around time (in terms of pclk) for DE De-assertion to RE assertion. The actual time is the programmed value + 1.

UART_CPR

Address: **Operational Base** + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x04	fifo_mode 8'h4 means FIFO mode is 64.
15:14	RO	0x0	reserved
13	RO	0x1	dma_extra 1'b1 means DMA_EXTRA enabled.
12	RO	0x1	uart_add_encoded_params 1'b1 means UART_ADD_ENCODED_PARAMS enabled.
11	RO	0x1	shadow 1'b1 means SHADOW mode enabled.

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Bit	Attr	Reset Value	Description
10	RO	0x1	fifo_stat 1'b1 means FIFO_STAT enabled.
9	RO	0x1	fifo_access 1'b1 means FIFO ACCESS enabled.
8	RO	0x1	new_feat 1'b1 means Additional features enabled.
7	RO	0x1	sir_lp_mode 1'b1 means SIR_LP mode enabled.
6	RO	0x1	sir_mode 1'b1 means SIR mode enabled.
5	RO	0x1	thre_mode 1'b1 means THRE mode enabled.
4	RO	0x1	afce_mode 1'b1 means AFCE mode enabled.
3:2	RO	0x0	reserved
1:0	RO	0x2	apb_data_width 2'b10 means APB data width is 32bit.

UART_UCV

Address: **Operational Base** + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3430322a	ver ASCII value for each number in the version.

UART_CTR

Address: **Operational Base** + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x44570110	peripheral_id This register contains the peripherals identification code.

33.5 Interface Description

Table 33-1 UART0 Interface Description

Module Pin	I	Pad Name	IOMUX Setting
IOMUX0			
uart_rx	I	UART0_RX_M0/JTAG_TMS_M1/GPIO0_D5_u	PMU1_IOC_GPIO0D_IOMUX_SEL_H[7:4]=4'h9
uart_tx	O	UART0_TX_M0/JTAG_TCK_M1/GPIO0_D4_u	PMU1_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4'h9
IOMUX1			
uart_rx	I	SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/CAN0_RX_M0/PWM2_CH2_M0/GPIO2_A0_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'h9
uart_tx	O	SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'h9

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Table 33-2 UART1 Interface Description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
uart_rx		I2C2_SDA_M0/UART1_RX_M0/CPULIT_AVS/PWM1_CH3_M0/GPIO0_C0_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[3:0]=4'ha
uart_tx		I2C2_SCL_M0/UART1_TX_M0/NPU_AVS/PWM1_CH4_M0/GPIO0_B7_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[15:12]=4'ha
uart_cts_n		SAI0_SDI2_M1/SAI0_SDO2_M1/PDM0_SDI2_M0/I2C4_SCL_M0/PCIE0_WAKEN_M0/CPUBIG_AVS/PWM1_CH5_M0/UART1_CTSN_M0/GPIO0_D2_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[11:8]=4'hd
uart_re			
uart_rts_n		SAI0_SDI3_M1/SAI0_SDO1_M1/PDM0_SDI3_M0/I2C4_SDA_M0/PCIE1_WAKEN_M0/GPU_AVS/PWM2_CH0_M0/UART1_RTSN_M0/GPIO0_D3_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[15:12]=4'hd
uart_de			
IOMUX1			
uart_rx		VI_CIF_D12/SDMMC1_D3_M1/ETH0_TXD0_M1/SAI0_SDI1_M0/PDM0_SDI2_M3/UART1_RX_M1/GPIO2_B1_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[7:4]=4'h9
uart_tx		VI_CIF_D13/SDMMC1_D2_M1/ETH0_TXD1_M1/SAI0_SDI0_M0/PDM0_SDI3_M3/UART1_TX_M1/GPIO2_B0_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[3:0]=4'h9
uart_cts_n		VI_CIF_D11/SDMMC1_CMD_M1/ETH0_TXD3_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCIE0_CLKREQN_M0/GPIO2_B2_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[11:8]=4'h9
uart_re			
uart_rts_n		VI_CIF_D10/SDMMC1_CLK_M1/ETH0_TXCLK_M1/SAI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/PCIE1_CLKREQN_M0/GPIO2_B3_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4'h9
uart_de			
IOMUX2			
uart_rx		VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8]=4'h9
uart_tx		VO_LCDC_D20/VO_EBC_VCOM/ETH0_RXCTL_M0/PDM1_CLK1_M2/DSMC_DATA13/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[15:12]=4'h9
uart_cts_n		VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0]=4'h9
uart_re			

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		3_A4_d	
uart_rts_n		VO_LCDC_D22/VO_EBC_GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[7:4]=4'h9
uart_de			

Table 33-3 UART2 Interface Description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
uart_rx		ETH1_RXD0_M1/FSPI1_D3_M1/PDM0_SDI1_M2/UART2_RX_M0/I2C8_SDA_M1/SATA_CPDET/GPIO1_C7_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[15:12]=4'h9
uart_tx		ETH1_TXCTL_M1/FSPI1_D2_M1/PDM0_SDI0_M2/UART2_TX_M0/I2C8_SCL_M1/SATA_CPPOD/GPIO1_C6_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[11:8]=4'h9
uart_cts_n		ETH1_TXD1_M1/FSPI1_D1_M1/UART4_RX_M1/UART2_CTSN_M0/SPI2_MISO_M1/PCIE1_BUTTONRSTN/GPIO1_C5_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[7:4]=4'ha
uart_re			
uart_rts_n		ETH1_TXD0_M1/FSPI1_D0_M1/UART4_TX_M1/UART2_RTSN_M0/SPI2_MOSI_M1/PCIE0_BUTTONRSTN/GPIO1_C4_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[3:0]=4'ha
uart_de			
IOMUX1			
uart_rx		SPDIF_RX0_M0/FLEXBUS0_CSN_M4/UART2_RX_M1/I2C3_SDA_M0/CAN1_RX_M2/GPIO4_B4_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'ha
uart_tx		SPDIF_TX0_M0/FLEXBUS0_D15_M1/UART2_TX_M1/I2C3_SCL_M0/PCIE0_CLKREQN_M2/CAN1_TX_M2/GPIO4_B5_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4'ha
uart_cts_n		SAI1_SDO2_M0/SAI1_SDI2_M0/PDM1_SDI2_M1/FLEXBUS1_D14_M1/SPI4_MOSI_M2/UART5_RX_M1/UART6_CTSN_M0/UART2_CTSN_M1/GPIO4_B1_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[7:4]=4'hc
uart_re			
uart_rts_n		SAI1_SDO1_M0/SAI1_SDI3_M0/PDM1_CLK1_M1/FLEXBUS1_D13_M1/SPI4_CLK_M2/UART5_TX_M1/UART6_RTSN_M0/UART2_RTSN_M1/GPIO4_B0_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'hc
uart_de			
IOMUX2			
uart_rx		VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12]=4'h9
uart_tx		VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/D	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0]=4'h9

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		SMC_DATA7/FLEXBUS1_D9/UART2_TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	
uart_cts_n		VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[15:12]=4'h9
uart_re			
uart_rts_n		VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8]=4'h9
uart_de			

Table 33-4 UART3 Interface Description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
uart_rx		VI_CIF_VSYNC/ETH1_PPSTRIG_M0/ETH0_MDC_M1/SAI3_LRCK_M2/UART3_RX_M0/SPI3_MOSI_M0/I2C7_SDA_M1/GPIO3_A1_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'h9
uart_tx		VI_CIF_HREF/ETH0_MDIO_M1/SAI3_SCLK_M2/UART3_TX_M0/SPI3_CLK_M0/I2C7_SCL_M1/GPIO3_A0_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'h9
uart_cts_n		VI_CIF_CLKO/ETH1_PPSCLK_M0/ETH0_RXCTL_M1/SAI3_SDO_M2/SPDIF_RX1_M1/UART3_CTSN_M0/SPI3_MISO_M0/CAN1_TX_M3/MIPI_TE_M1/GPIO3_A2_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'h9
uart_re			
uart_rts_n		VI_CIF_CLKI/ETH1_PTP_REFCLK_M0/ETH0_RXD1_M1/SAI3_SDI_M2/SPDIF_TX1_M1/UART3_RTSN_M0/SPI3_CSN0_M0/CAN1_RX_M3/GPIO3_A3_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4'h9
uart_de			
IOMUX1			
uart_rx		VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/DSMC_INT2/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4'h9
uart_tx		SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4'h9
uart_cts_n		VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12]=4'ha
uart_re			

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uart_rts_n		VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/DSMC_DATA7/FLEXBUS1_D9/UART2_TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0]=4'ha
uart_de			
IOMUX2			
uart_rx		ETH1_TXCLK_M1/SDMMC1_CLK_M0/SAI3_MCLK_M1/PDM0_CLK0_M2/UART3_RX_M2/GPIO1_C1_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[7:4]=4'h9
uart_tx		ETH1_TXD3_M1/SDMMC1_CMD_M0/PDM0_SDI2_M2/UART3_TX_M2/SPI1_CSN1_M0/PWM0_CH0_M1/GPIO1_C0_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[3:0]=4'h9
uart_cts_n		ETH1_RXCLK_M1/SDMMC1_D2_M0/SAI3_SDO_M1/UART3_CTSN_M2/SPI1_MISO_M0/PCIE0_CLKREQN_M1/GPIO1_B6_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4'h9
uart_re			
uart_rts_n		ETH1_TXD2_M1/SDMMC1_D3_M0/SAI3_SDI_M1/EMMC_TESTDATA_OUT/FSPI0_TESTDATA_OUT/FSPI1_TESTDATA_OUT_M1/UART3_RTSN_M2/SPI1_CSN0_M0/PCIE0_WAKEN_M1/GPIO1_B7_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4'h9
uart_de			

Table 33-5 UART4 Interface Description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
uart_rx		ETH1_RXD0_M0/SAI4_SDO_M3/UART4_RX_M0/I2C6_SDA_M2/PWM2_CH1_M2/GPIO2_D1_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[7:4]=4'h9
uart_tx		ETH1_TXCTL_M0/SAI4_SDI_M3/UART4_TX_M0/I2C6_SCL_M2/PWM2_CH0_M2/GPIO2_D0_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[3:0]=4'h9
uart_cts_n		ETH1_TXD0_M0/SAI4_SCLK_M3/UART4_CTSN_M0/I2C5_SCL_M2/PWM1_CH5_M2/GPIO2_C6_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[11:8]=4'h9
uart_re			
uart_rts_n		ETH1_TXD1_M0/SAI4_LRCK_M3/UART4_RTSN_M0/I2C5_SDA_M2/PWM0_CH1_M2/GPIO2_C7_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[15:12]=4'h9
uart_de			
IOMUX1			
uart_rx		ETH1_TXD1_M1/FSPI1_D1_M1/UART4_RX_M1/UART2_CTSN_M0/SPI2_MISO_M1/PCIE1_BUTTONRSTN/GPIO1_C5_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[7:4]=4'h9
uart_tx		ETH1_TXD0_M1/FSPI1_D0_M1/UART4_TX_M1/UART2_RTSN_M0/SPI2_MOSI_M1/PCIE0_BUTTONRSTN/GPIO1_C4_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[3:0]=4'h9
uart_cts_n		ETH1_PPSTRIG_M1/SDMMC1_DETN_M0/FSPI1_CSN0_M1/UART4_CTSN_M1/I2C6_SDA_M1/SPI2_CSN0_M1/GPIO1_C3_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[15:12]=4'h9
uart_re			

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uart_rts_n		ETH1_PPSCLK_M1/SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_RSTN_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[11:8]=4'h9
uart_de			
IOMUX2			
uart_rx		REF_CLK2_OUT/I2C1_SDA_M1/UART4_RX_M2/PWM1_CH1_M0/GPIO0_B5_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[7:1]=4'ha
uart_tx		REF_CLK1_OUT/I2C1_SCL_M1/UART4_TX_M2/PWM1_CH0_M0/GPIO0_B4_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[3:0]=4'ha

Table 33-6 UART5 Interface Description

Module Pin		**Pad Name**	**IOMUX Setting**
IOMUX0			
uart_rx		VO_LCDC_DEN/VO_EBC_SDLE/SAI1_SDI1_M1/DSMC_DATA0/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[3:0]=4'h9
uart_tx		VO_LCDC_HSYNC/VO_EBC_GDCLK/SAI1_SDI2_M1/DSMC_CLKP/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[7:4]=4'h9
uart_cts_n		VO_LCDC_VSYNC/VO_EBC_SDCLK/SAI1_SDI3_M1/DSMC_CLKN/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:2]=4'h9
uart_re			
uart_rts_n		VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12]=4'h9
uart_de			
IOMUX1			
uart_rx		SAI1_SDO2_M0/SAI1_SDI2_M0/PDM1_SDI2_M1/FLEXBUS1_D14_M1/SPI4_MOSI_M2/UART5_RX_M1/UART6_CTSN_M0/UART2_CTSN_M1/GPIO4_B1_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[7:1]=4'ha
uart_tx		SAI1_SDO1_M0/SAI1_SDI3_M0/PDM1_CLK1_M1/FLEXBUS1_D13_M1/SPI4_CLK_M2/UART5_TX_M1/UART6_RTSN_M0/UART2_RTSN_M1/GPIO4_B0_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'ha
uart_cts_n		SAI1_LRCK_M0/FLEXBUS1_D12_M1/SPI4_CSN1_M2/UART5_CTSN_M1/I2C2_SDA_M2/PCIE1_CLKREQN_M2/GPIO4_A5_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[7:4]=4'ha
uart_re			
uart_rts_n		SAI1_SCLK_M0/FLEXBUS1_CSN_M4/SPI3_CSN0_M2/UART5_RTSN_M1/I2C2_SCL_M2/PWM2_CH4_M1/GPIO4_A3_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[15:12]=4'ha
uart_de			

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IOMUX2			
uart_rx		SDMMC0_CMD/FSPI1_CSN0_M0/SAI3_SDO_M3/UART5_RX_M2/I2C5_SDA_M0/SPI0_CSN0_M1/PWM2_CH4_M0/GPIO2_A4_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[3:0]=4'h9
uart_tx		SDMMC0_CLK/FSPI1_CLK_M0/SAI3_SCLK_M3/TEST_CLK_OUT/UART5_TX_M2/I2C5_SCL_M0/SPI0_CLK_M1/I3C1_SDA_PU_M1/GPIO2_A5_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[7:4]=4'h9
uart_cts_n		SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/CAN1_TX_M0/I3C1_SDA_M1/GPIO2_A3_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[15:12]=4'ha
uart_re			
uart_rts_n		SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[11:8]=4'ha
uart_de			

Table 33-7 UART6 Interface Description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
uart_rx		SAI4_LRCK_M0/PDM1_CLK0_M1/FLEXBUS0_D14_M1/SPI3_MISO_M2/UART6_RX_M0/I2C4_SDA_M1/CAN0_RX_M2/GPIO4_A6_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[11:8]=4'ha
uart_tx		SAI4_SCLK_M0/PDM1_SDI3_M1/FLEXBUS0_D13_M1/SPI3_MOSI_M2/UART6_TX_M0/I2C4_SCL_M1/CAN0_TX_M2/GPIO4_A4_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[3:0]=4'ha
uart_cts_n		SAI1_SDO2_M0/SAI1_SDI2_M0/PDM1_SDI2_M1/FLEXBUS1_D14_M1/SPI4_MOSI_M2/UART5_RX_M1/UART6_CTSN_M0/UART2_CTSN_M1/GPIO4_B1_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[7:4]=4'hb
uart_re			
uart_rts_n		SAI1_SDO1_M0/SAI1_SDI3_M0/PDM1_CLK1_M1/FLEXBUS1_D13_M1/SPI4_CLK_M2/UART5_TX_M1/UART6_RTSN_M0/UART2_RTSN_M1/GPIO4_B0_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'hb
uart_de			
IOMUX1			
uart_rx		ETH1_RXCTL_M0/UART6_RX_M1/I3C1_SDA_M0/PWM2_CH3_M2/GPIO2_D3_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[15:12]=4'h9
uart_tx		CAM_CLK0_OUT_M1/ETH1_RXD1_M0/SAI4_MCLK_M3/UART6_TX_M1/I3C1_SCL_M0/PWM2_CH2_M2/GPIO2_D2_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[11:8]=4'h9
uart_cts_n		ISP_FLASH_TRIGOUT_M0/ETH1_MDIO_M0/UART6_CTSN_M1/I2C9_SCL_M2/PWM2_CH5_M2/GPIO2_D5_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[7:4]=4'h9
uart_re			
uart_rts_n		ISP_PRELIGHT_TRIG_M0/ETH1_MDC_M0/UART6_RTSN_M1/I2C9_SDA_	TOP_IOC_GPIO2D_IOMUX_SEL_H[3:0]=4'h

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uart_de		M2/PWM2_CH4_M2/GPIO2_D4_d	9
IOMUX2			
uart_rx		EMMC_RSTN/FSPI0_CSN0/UART6_RX_M2/I2C7_SDA_M0/MIPI_TE_M3/PWM2_CH1_M0/GPIO1_B3_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h9
uart_tx		EMMC_CMD/FSPI0_RSTN/FSPI0_CSN1/UART6_TX_M2/I2C7_SCL_M0/GPIO1_B0_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[3:0]=4'h9
uart_cts_n		EMMC_D3/FSPI0_D3/SAI0_SDO2_M2/SAI0_SDI2_M2/PDM0_SDI1_M1/UART7_RX_M1/UART6_CTSN_M2/GPIO1_A3_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4'ha
uart_re			
uart_rts_n		EMMC_D2/FSPI0_D2/SAI0_SDO1_M2/SAI0_SDI3_M2/PDM0_SDI3_M1/UART7_TX_M1/UART6_RTSN_M2/GPIO1_A2_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4'ha
uart_de			
IOMUX3			
uart_rx		ISP_FLASH_TRIGOUT_M1/SAI4_SDO_M2/VP0_SYNC_OUT/SATA1_ACTLED_M1/I2C3_SDA_M3/SPI4_MOSI_M0/UART6_RX_M3/PWM2_CH5_M1/GPIO4_C5_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[7:4]=4'hd
uart_tx		ISP_PRELIGHT_TRIG_M1/SAI4_LRCK_M2/DP_HPDIN_M0/I2C3_SCL_M3/SPI4_CSN0_M0/UART6_TX_M3/PWM2_CH6_M1/GPIO4_C4_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[3:0]=4'hd

Table 33-8 UART7 Interface Description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
uart_rx		VI_CIF_D6/ETH0_RXD2_M1/SAI0_LRCK_M0/UART7_RX_M0/UART8_CTSN_M1/I2C8_SDA_M2/GPIO2_B7_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[15:12]=4'h9
uart_tx		VI_CIF_D7/ETH1_PTP_REFCLK_M1/ETH0_RXD3_M1/SAI0_SCLK_M0/UART7_TX_M0/UART8_RTSN_M1/I2C8_SCL_M2/GPIO2_B6_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[11:8]=4'h9
uart_cts_n		VI_CIF_D9/SDMMC1_PWREN_M1/ETH0_TXD2_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/SATA0_ACTLED_M0/GPIO2_B4_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[3:0]=4'h9
uart_re			
uart_rts_n		VI_CIF_D8/SDMMC1_DETN_M1/ETH0_RXCLK_M1/SAI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/SATA1_ACTLED_M0/GPIO2_B5_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[7:4]=4'h9
uart_de			
IOMUX1			
uart_rx		EMMC_D3/FSPI0_D3/SAI0_SDO2_M2/SAI0_SDI2_M2/PDM0_SDI1_M1/UART7_RX_M1/UART6_CTSN_M2/GPIO1_A3_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4'h9
uart_tx		EMMC_D2/FSPI0_D2/SAI0_SDO1_M2/SAI0_SDI3_M2/PDM0_SDI3_M1/U	TOP_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4'h

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		ART7_TX_M1/UART6_RTSN_M2/GPIO1_A2_u	9
uart_cts_n		EMMC_D1/FSPI0_D1/SAI0_LRCK_M2/UART7_CTSN_M1/I2C2_SDA_M1/GPIO1_A1_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[7:4]=4'h9
uart_re			
uart_rts_n		EMMC_D0/FSPI0_D0/SAI0_SCLK_M2/UART7_RTSN_M1/I2C2_SCL_M1/GPIO1_A0_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[3:0]=4'h9
uart_de			
IOMUX2			
uart_rx		SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/CAN0_RX_M0/PWM2_CH2_M0/GPIO2_A0_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'ha
uart_tx		SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'ha

Table 33-9 UART8 Interface Description

Module Pin		**Pad Name**	**IOMUX Setting**
IOMUX0			
uart_rx		VO_LCDC_D6/VO_EBC_SDDO6/SAI1_SDO0_M1/DSMC_DATA4/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4'h9
uart_tx		VO_LCDC_D5/VO_EBC_SDDO5/SAI1_LRCK_M1/DSMC_DATA3/FLEXBUS1_D5/UART8_TX_M0/SPI1_MOSI_M2/GPIO3_C6_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[11:8]=4'h9
uart_cts_n		VO_LCDC_D3/VO_EBC_SDDO3/SAI1_MCLK_M1/DSMC_DATA1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4'h9
uart_re			
uart_rts_n		VO_LCDC_D4/VO_EBC_SDDO4/SAI1_SCLK_M1/DSMC_DATA2/FLEXBUS1_D4/UART8_RTSN_M0/SPI1_CLK_M2/GPIO3_C7_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[15:12]=4'h9
uart_de			
IOMUX1			
uart_rx		VI_CIF_D14/SDMMC1_D1_M1/ETH0_TXCTL_M1/SAI0_SDO1_M0/UART8_RX_M1/I2C4_SDA_M2/GPIO2_A7_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[15:12]=4'h9
uart_tx		VI_CIF_D15/SDMMC1_D0_M1/ETH0_RXD0_M1/SAI0_SDO0_M0/UART8_TX_M1/SPI4_CSN1_M3/I2C4_SCL_M2/GPIO2_A6_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[11:8]=4'h9
uart_cts_n		VI_CIF_D6/ETH0_RXD2_M1/SAI0_LRCK_M0/UART7_RX_M0/UART8_CTSN_M1/I2C8_SDA_M2/GPIO2_B7_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[15:12]=4'ha
uart_re			

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uart_rts_n		VI_CIF_D7/ETH1_PTP_REFCLK_M1/ETH0_RXD3_M1/SAI0_SCLK_M0/UART7_TX_M0/UART8_RTSN_M1/I2C8_SCL_M2/GPIO2_B6_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[11:8]=4'ha
uart_de			
IOMUX2			
uart_rx		I2C0_SDA_M1/UART8_RX_M2/I3C0_SDA_M0/GPIO0_C2_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[11:8]=4'ha
uart_tx		I2C0_SCL_M1/UART8_TX_M2/I3C0_SCL_M0/GPIO0_C1_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[7:4]=4'ha

Table 33-10 UART9 Interface Description

Module Pin		**Pad Name**	**IOMUX Setting**
IOMUX0			
uart_rx		VI_CIF_D5/ETH1_RXD2_M0/ETH0_PTP_REFCLK_M1/PDM1_SDI1_M0/UART9_RX_M0/PWM1_CH0_M2/GPIO2_C0_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[3:0]=4'h9
uart_tx		VI_CIF_D4/ETH1_RXD3_M0/ETH0_PPSCLK_M1/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[7:4]=4'h9
uart_cts_n		CAM_CLK2_OUT_M1/ETH1_MCLK_M0/ETH_CLK0_25M_OUT_M1/SAI0_SDO3_M0/SPDIF_TX0_M2/UART9_CTSN_M0/SPI3_CSN1_M0/PWM2_CH7_M2/GPIO2_D7_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[15:8]=4'h9
uart_re			
uart_rts_n		CAM_CLK1_OUT_M1/ETH_CLK1_25M_OUT_M0/ETH0_MCLK_M1/SAI3_MCLK_M2/SPDIF_RX0_M2/UART9_RTSN_M0/I3C1_SDA_PU_M0/PWM2_CH6_M2/GPIO2_D6_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[11:8]=4'h9
uart_de			
IOMUX1			
uart_rx		VO_LCDC_D17/VO_EBC_SDCE1/ETH0_RXD0_M0/PDM1_SDI1_M2/DSMC_DATA11/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[11:8]=4'h9
uart_tx		VO_LCDC_D16/VO_EBC_SDCE0/ETH0_TXCTL_M0/PDM1_SDI0_M2/DSMC_DATA10/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[15:12]=4'h9
uart_cts_n		VO_LCDC_D14/VO_EBC_SDDO14/ETH0_TXD0_M0/SPDIF_TX1_M0/DSMC_DATA8/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'h9
uart_re			
uart_rts_n		VO_LCDC_D15/VO_EBC_SDDO15/ETH0_TXD1_M0/SPDIF_RX1_M0/DSMC_DATA9/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[3:0]=4'h9
uart_de			
IOMUX2			
uart_rx		DSM_AUD_RN_M1/HDMI_TX_SDA/I	VCCIO6_IOC_GPIO4C

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		2C2_SDA_M3/CAN0_RX_M1/UART9_RX_M2/PWM2_CH1_M1/GPIO4_C3_d	_IOMUX_SEL_L[15:12]=4'hd
uart_tx		DSM_AUD_RP_M1/HDMI_TX_SCL/I2C2_SCL_M3/CAN0_TX_M1/UART9_TX_M2/PWM2_CH0_M1/GPIO4_C2_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[11:8]=4'hd

Table 33-11 UART10 Interface Description

Module Pin		Pad Name	IOMUX Setting
IOMUX0			
uart_rx		VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0]=4'h9
uart_tx		VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[7:4]=4'h9
uart_cts_n		VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8]=4'ha
uart_re			
uart_rts_n		VO_LCDC_D20/VO_EBC_VCOM/ETH0_RXCTL_M0/PDM1_CLK1_M2/DSMC_DATA13/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[15:12]=4'ha
uart_de			
IOMUX1			
uart_rx		ETH1_RXCTL_M1/SAI2_SCLK_M0/UART10_RX_M1/I3C0_SDA_PU_M1/GPIO1_D1_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[7:4]=4'h9
uart_tx		ETH1_RXD1_M1/SAI2_SDO_M0/UART10_TX_M1/GPIO1_D0_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[3:0]=4'h9
uart_cts_n		ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'h9
uart_re			
uart_rts_n		ETH1_MCLK_M1/SAI2_MCLK_M0/PDM0_SDI3_M2/SPDIF_RX1_M2/UART10_RTSN_M1/I2C5_SCL_M1/GPIO1_D4_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[3:0]=4'h9
uart_de			
IOMUX2			
uart_rx		SAI0_SDO0_M1/DP_HPDIN_M1/UART10_RX_M2/I3C0_SDA_PU_M0/GPIO0_C5_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[7:4]=4'ha
uart_tx		SAI0_MCLK_M1/PDM0_CLK0_M0/UART10_TX_M2/PWM0_CH0_M0/GPIO0_C4_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[3:0]=4'ha

Table 33-12 UART11 Interface Description

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Module Pin		Pad Name	IOMUX Setting
IOMUX0			
uart_rx		VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4]=4'h9
uart_tx		VO_LCDC_D7/VO_EBC_SDDO7/SAI1_SDO1_M1/DSMC_DATA5/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/CAN0_TX_M3/GPIO3_C4_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4'h9
uart_cts_n		VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12]=4'h9
uart_re			
uart_rts_n		VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8]=4'h9
uart_de			
IOMUX1			
uart_rx		VI_CIF_D0/ETH1_TXCLK_M0/SAI2_SDI_M1/PDM1_CLK0_M0/UART11_RX_M1/SPI1_CLK_M1/PWM1_CH4_M2/GPIO2_C5_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[7:4]=4'h9
uart_tx		VI_CIF_D1/ETH1_TXD3_M0/SAI2_SDO_M1/PDM1_SDI0_M0/UART11_TX_M1/SPI1_CSN0_M1/PWM1_CH3_M2/GPIO2_C4_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[3:0]=4'h9
uart_cts_n		VI_CIF_D3/ETH1_RXCLK_M0/ETH0_PPSTRIG_M1/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[11:8]=4'h9
uart_re			
uart_rts_n		VI_CIF_D2/ETH1_TXD2_M0/SAI2_LRCK_M1/PDM1_SDI3_M0/UART11_RTSN_M1/SPI1_MISO_M1/PWM0_CH0_M2/GPIO2_C3_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[15:12]=4'h9
uart_de			
IOMUX2			
uart_rx		DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[7:4]=4'hd
uart_tx		DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[3:0]=4'hd

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33.6 Application Notes

33.6.1 No FIFO Mode Transfer Flow

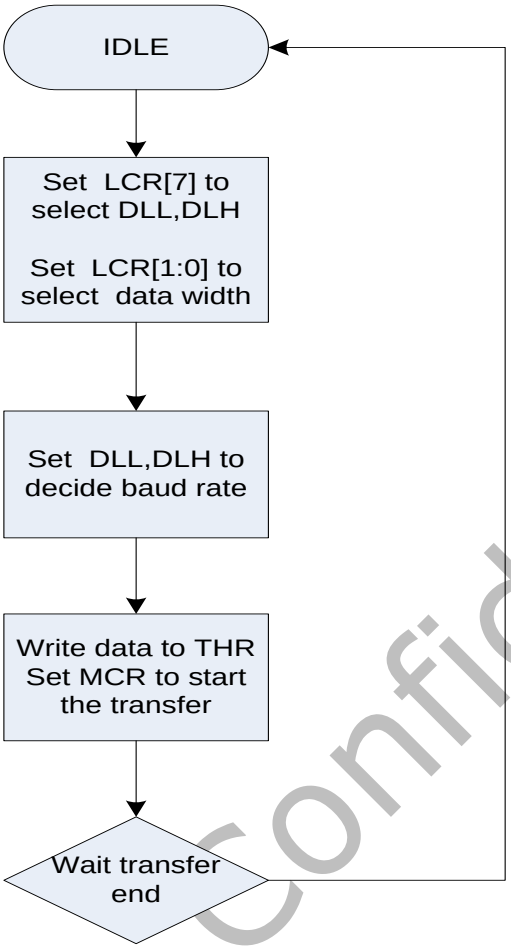

Fig. 33-7 UART None FIFO mode

33.6.2 FIFO Mode Transfer Flow

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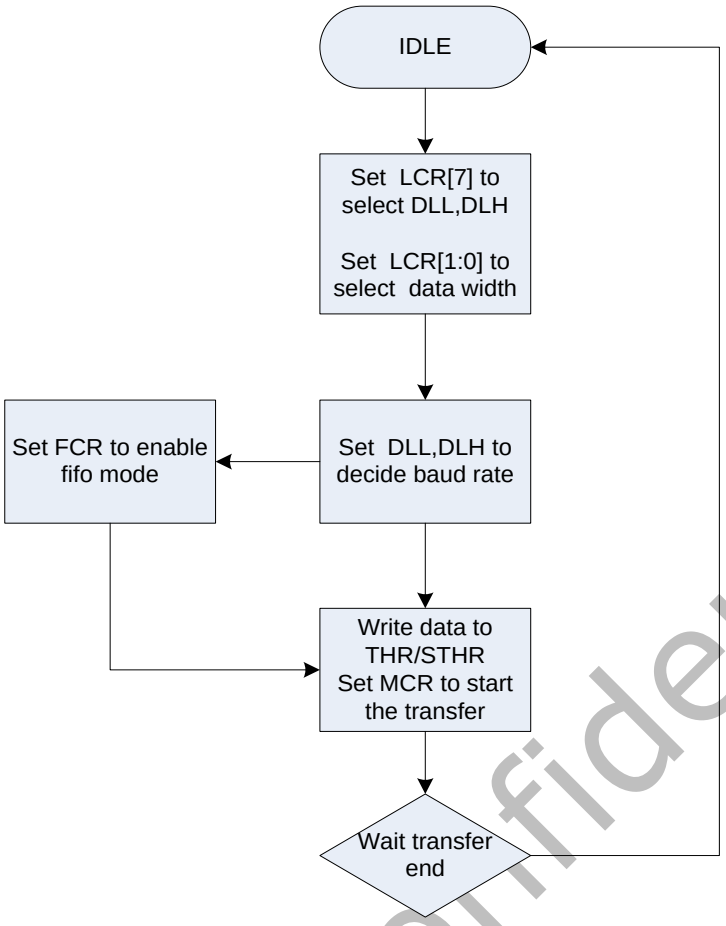

Fig. 33-8 UART FIFO mode

The UART is an APB slave performing:

Serial-to-parallel conversion on data received from a peripheral device. Parallel-to-serial conversion on data transmitted to the peripheral device. The CPU reads and writes data and control/status information through the APB interface. The transmitting and receiving paths are buffered with internal FIFO memories enabling up to 64-bytes to be stored independently in both transmit and receive modes. A baud rate generator can generate a common transmit and receive internal clock input. The baud rates will depend on the internal clock frequency. The UART will also provide transmit, receive and exception interrupts to system. A DMA interface is implemented for improving the system performance.

33.6.3 Baud Rate Calculation

UART clock generation

UARTs source clocks (SCLK) can be selected from different PLL outputs, or from XIN24M. SCLK can be divided to different frequency, please refer to CRU chapter.

UART baud rate configuration

The following table provides some reference configuration for different UART baud rates.

Table 33-13 UART Baud Rate Configuration

Baud Rate	Reference Configuration
115.2 Kbps	Configure PLL to get 1188MHz clock output; Divide 1188MHz clock by 1536/24750 to get 73.728MHz clock by shared fractional divider; Divide 73.728MHz clock by 20 to get 3.6864MHz clock by independent integer divider; Configure UART_DLL to 2.
460.8 Kbps	Configure PLL to get 1188MHz clock output; Divide 1188MHz clock by 1536/24750 to get 73.728MHz clock by shared fractional divider; Divide 73.728MHz clock by 10 to get 460.8KHz clock by independent integer divider; Configure UART_DLL to 1.

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921.6 Kbps	Configure PLL to get 1188MHz clock output; Divide 1188MHz clock by 1536/24750 to get 73.728MHz clock by shared fractional divider; Divide 73.728MHz clock by 5 to get 921.6KHz clock by independent integer divider; Configure UART_DLL to 1.
1.5 Mbps	Configure PLL to get 1000MHz clock output; Divide 1000MHz clock by 24/125 to get 192MHz clock by shared fractional divider; Divide 192MHz clock by 8 to get 24MHz clock by independent integer divider; Configure UART_DLL to 1.
3 Mbps	Configure PLL to get 1000MHz clock output; Divide 1000MHz clock by 24/125 to get 192MHz clock by shared fractional divider; Divide 192MHz clock by 4 to get 48MHz clock by independent integer divider; Configure UART_DLL to 1.
4 Mbps	Configure PLL to get 1000MHz clock output; Divide 1000MHz clock by 24/125 to get 192MHz clock by shared fractional divider; Divide 192MHz clock by 3 to get 64MHz clock by independent integer divider; Configure UART_DLL to 1.
8 Mbps	Configure PLL to get 1000MHz clock output; Divide 1000MHz clock by 16/125 to get 128MHz clock by shared fractional divider; Divide 128MHz clock by 1 to get 128MHz clock by independent integer divider; Configure UART_DLL to 1.

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Chapter 34 Pulse Width Modulation (PWM)

34.1 Overview

The Pulse-Width Modulator (PWM) provides a way to generate a pulse periodic waveform for motor control, it can also act as a digital-to-analog converter with some external components.

The PWM Module supports the following common features:

- Support input capture mode
  - Support measures the high/low polarity effective cycles of input waveform
  - Support generates an interrupt at the transition of input waveform polarity
  - Support a 32-bits high polarity capture counter
  - Support a 32-bits low polarity capture counter
  - Support an input filter to remove glitch
- Support continuous mode and one-shot output mode
  - Support a 32-bits period counter
  - Support a 32-bits duty counter
  - Support configure the polarity in inactive state and duty cycle
  - Support center or left aligned mode
  - Support a 16-bit first dimensional repeat counter and an interrupt for reload operation
  - Support a 16-bit second dimensional repeat counter and an interrupt for one-shot operation
  - Support global synchronization of various channels
- Supports two-stage frequency division of working clock

RK3576 support three PWM controllers, they support some individual feature as following:

- PWM0
  - Support 2 channels
  - Support power key capture mode
- PWM1
  - Support 6 channels
  - Support generates waveform through lookup table
  - Support biphasic counter
  - Support clock frequency meter
  - Support clock counter
- PWM2
  - Support 8 channels
  - Support power key capture mode
  - Support IR transmission in NEC with full repeat, NEC with simple repeat, TC9012 or SONY mode
  - Support biphasic counter

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34.2 Block Diagram

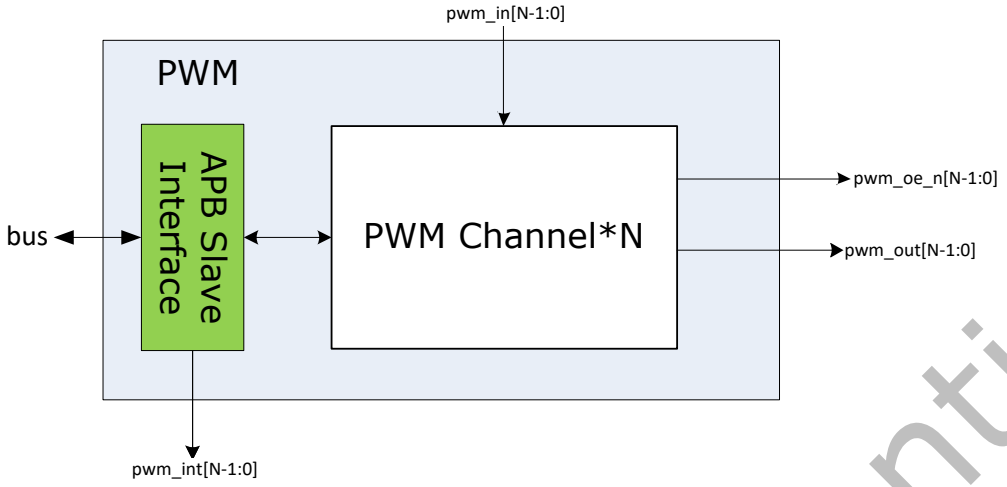

Fig. 34-1 PWM Block Diagram

The host processor gets access to PWM register through the APB slave interface with 32-bit bus width. PWM controller support 1~8 channels, and the offset address of each channel is 4k-byte as interval. PWM supports one interrupt for each channel, user should refer to interrupt register to know the raw interrupt status when an interrupt is asserted.

34.3 Function Description

The PWM supports three operation modes: capture mode, one-shot mode and continuous mode. For the one-shot mode and the continuous mode, the PWM output can be configured as the left-aligned mode or the center-aligned mode.

PWM also supports some additional function, such as clock counter, clock frequency meter and biphasic Counter.

34.3.1 Capture mode

The capture mode is used to measure the PWM channel input waveform high/low effective cycles with the PWM channel clock and asserts an interrupt when the polarity of the input waveform changes. The number of the high effective cycles is recorded in the PWM_HPC register, while the number of the low effective cycles is recorded in the PWM_LPC register.

Notes: the PWM input waveform is doubled buffered when the PWM channel is working in order to filter unexpected shot-time polarity transition, and therefore the interrupt is asserted several cycles after the input waveform polarity changes, and so does the change of the values of PWM_HPC and PWM_LPC.

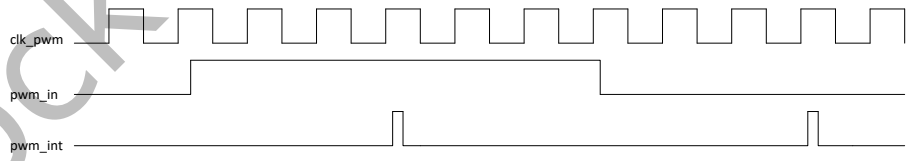

Fig. 34-2 PWM Capture Mode

The PWM support 32-bits power key capture mode. User can configure 16 power keys to match, the interrupt will be asserted when the capture value matches any one.

34.3.2 Continuous mode

In continuous mode, the PWM channel generates a series of the pulses continuously as expected once the channel is enabled. It supports left-aligned mode or center-aligned mode.

For the left-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWM_CTRL.duty_pol). Once duty cycle number (PWM_DUTY) is reached, the output is switched to the opposite polarity. After the period number (PWM_PERIOD) is reached, the output is again switched to the opposite polarity to start another period of desired pulse.

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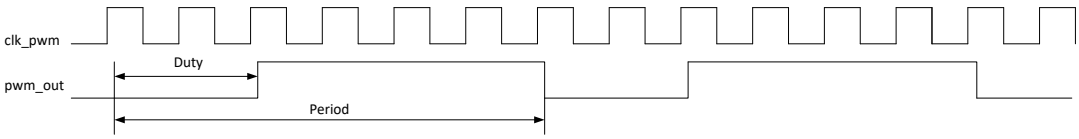

Fig. 34-3 PWM Continuous Left-aligned Output Mode

For the center-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWM_CTRL.duty_pol). Once one half of duty cycle number (PWM_DUTY) is reached, the output is switched to the opposite polarity. Then if there is one half of duty cycle left for the whole period, the output is again switched to the opposite polarity. Finally, after the period number (PWM_PERIOD) is reached, the output starts another period of desired pulse.

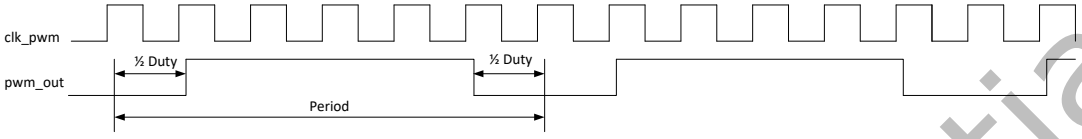

Fig. 34-4 PWM Continuous Center-aligned Output Mode

PWM support a 16 bits first dimensional repeat counter. An reload interrupt is generated every N+1 periods of the waveform when PWM_RPT.rpt_first_dimensional is configured to N. User can update the duty and period configuration for next N+1 periods when receive the interrupt.

PWM also support generates waveform through lookup table, the duty and period can be updated by lookup table automatic every N+1 periods of the waveform.

Continuous mode will generate the waveform continuously until disabled by user. It's will fix to inactive polarity (PWM_CTRL.inactive_pol) when it's disabled.

34.3.3 One-shot mode

In one-shot mode, the PWM channel generates limited periods of waveforms.

In addition to the first dimensional repeat counter, it also supports a 16 bits second dimensional repeat counter. PWM channel will stop and assert an interrupt after second dimensional counter reach M+1 when PWM_RPT.rpt_second_dimensional is configured to M. The total waveform periods are (N + 1) multi by (M + 1).

The reload interrupt and lookup table is also supported in one-shot mode.

The left-aligned and the center-aligned is also supported in one-shot mode.

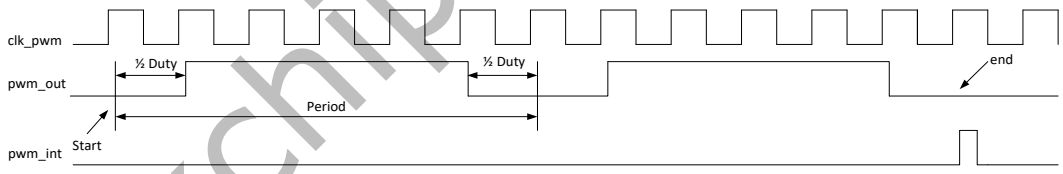

Fig. 34-5 PWM One-shot Center-aligned Output Mode

34.3.4 Clock Counter

PWM support a 64-bits counter which clock can select from any PWM channel input and a clock from system CRU.

34.3.5 Clock frequency meter

PWM support a 32-bits frequency meter which clock can select from any PWM channel input and a clock from system CRU. It supports a reference clock and timer to schedule a period time, user can calculate the frequency by gets the counter value that counted by the measured clock in the period time.

34.3.6 Biphasic Counter

PWM support biphasic counter which uses two channels to compose an A/B phase channel. The biphasic counter register is only located at A channel, User only needs to configure the IOMUX of B channel.

PWM1 controller support 3 biphasic counters: Channel 0 and Channel 3 compose an A/B phase bidirectional counter. Channel 1 and Channel 4 compose an A/B phase bidirectional counter. Channel 2 and Channel 5 compose an A/B phase bidirectional counter.

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PWM2 controller support 4 biphasic counters: Channel 0 and Channel 4 compose an A/B phase bidirectional counter. Channel 1 and Channel 5 compose an A/B phase bidirectional counter. Channel 2 and Channel 6 compose an A/B phase bidirectional counter. Channel 3 and Channel 7 compose an A/B phase bidirectional counter.
Biphasic counter support 5 mode as following:

- Mode 0: Single phase increase mode with A-phase.

When A-phase input is OFF->ON, the count increases by 1. In this mode, it can be used as clock frequency meter or clock counter.

- Mode 1: Single phase increase/decrease mode with A-phase.

When the B-phase input is OFF and the A-phase input is OFF->ON, the count increases by 1.
When the B-phase input is ON and the A-phase input is OFF->ON, the count decreases by 1

- Mode 2: Dual phase with A/B-phase mode.

When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1

- Mode 3: Dual phase with A/B-phase 2 times frequency mode.

When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1;
When the A-phase input is OFF and the B-phase input is ON->OFF, the count increases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1;
When the A-phase input is OFF and the B-phase input is OFF ->ON, the count decreases by 1.

- Mode 4: Dual phase with A/B-phase 4 times frequency mode.

When the input of phase B is OFF and phase A is OFF->ON, the count increases by 1.
When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1.
When the input of phase B is ON and phase A is ON->OFF, the count increases by 1.
When the A-phase input is OFF and the B-phase input is ON_.OFF, the count increases by 1.
When the A-phase input is OFF and the B-phase input is OFF->ON, the count decreases by 1.
When the input of phase B is ON and phase A is OFF->ON, the count decreases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1.
When the input of phase B is OFF and the input of phase A is ON->OFF, the count decreases by 1.

34.4 Register Description

34.4.1 Internal Address Mapping

Slave address can be divided into different length for different controller, which is shown as follows.

Operational Base

Name	Base Address
PWM0	0x27330000
PWM1	0x2ADD0000
PWM2	0x2ADE0000

Slave address can be divided into different length for different channels in one controller, which is shown as follows.

Table 34-1 PWM Channel Address Map

Channel	Offset Address
Channel 0	0x0000
Channel 1	0x1000
Channel 2	0x2000

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Channel	Offset Address
Channel 3	0x3000
Channel 4	0x4000
Channel 5	0x5000
Channel 6	0x6000
Channel 7	0x7000

34.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PWM_VERSION_ID	0x0000	W	0x04000044	Version ID Register
PWM_ENABLE	0x0004	W	0x00000000	Enable Register
PWM_CLK_CTRL	0x0008	W	0x00000000	Clock Control Register
PWM_CTRL	0x000C	W	0x00000000	Control Register
PWM_PERIOD	0x0010	W	0x00000000	Period Register
PWM_DUTY	0x0014	W	0x00000000	Duty Register
PWM_OFFSET	0x0018	W	0x00000000	Output Offset Register
PWM_RPT	0x001C	W	0x00000000	Repeat Register
PWM_FILTER_CTRL	0x0020	W	0x00000000	Filter Control Register
PWM_CNT	0x0024	W	0x00000000	Counter Register
PWM_ENABLE_DELAY	0x0028	W	0x00000000	Enable Delay Register
PWM_HPC	0x002C	W	0x00000000	High Polarity Capture Register
PWM_LPC	0x0030	W	0x00000000	Low Polarity Capture Register
PWM_BIPHASIC_COUNTER_CTRL0	0x0040	W	0x00000000	Biphasic counter control 0 register
PWM_BIPHASIC_COUNTER_CTRL1	0x0044	W	0x00000000	Biphasic counter control 1 register
PWM_BIPHASIC_COUNTER_TIMER_VALUE	0x0048	W	0x00000000	Biphasic counter timer value register
PWM_BIPHASIC_COUNTER_RESULT_VALUE	0x004C	W	0x00000000	Biphasic counter result value register
PWM_BIPHASIC_COUNTER_RESULT_VALUE_SYNC	0x0050	W	0x00000000	Biphasic counter result value register
PWM_INTSTS	0x0070	W	0x00000000	Interrupt Status Register
PWM_INT_EN	0x0074	W	0x00000000	Interrupt Enable Register
PWM_INT_MASK	0x0078	W	0x00000000	Interrupt Mask Register
PWM_WAVE_MEM_ARBITER	0x0080	W	0x00000000	Waveform Generator Memory Arbiter Register
PWM_WAVE_MEM_STATUS	0x0084	W	0x00000000	Waveform Generator Memory Status Register
PWM_WAVE_CTRL	0x0088	W	0x00000010	Waveform Generator control register
PWM_WAVE_MAX	0x008C	W	0x00000000	Waveform Generator maximum register

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Name	Offset	Size	Reset Value	Description
PWM_WAVE_MIN	0x0090	W	0x00000000	Waveform Generator minimum register
PWM_WAVE_OFFSET	0x0094	W	0x00000000	Waveform Generator offset register
PWM_WAVE_MIDDLE	0x0098	W	0x00000000	Waveform Generator middle register
PWM_WAVE_HOLD	0x009C	W	0x00000000	Waveform Generator hold register
PWM_GLOBAL_ARBITER	0x00C0	W	0x00000000	Global Arbiter Register
PWM_GLOBAL_CTRL	0x00C4	W	0x00000000	Global Control Register
PWM_PWRMATCH_ARBITER	0x0100	W	0x00000000	Power Key Match Arbiter Register
PWM_PWRMATCH_CTRL	0x0104	W	0x00000000	Power Key Match Control Register
PWM_PWRMATCH_LPRE	0x0108	W	0x238C22C4	Power Key Match of Low Preload Register
PWM_PWRMATCH_HPRE	0x010C	W	0x11F81130	Power Key Match of High Preload Register
PWM_PWRMATCH_LD	0x0110	W	0x029401CC	Power Key Match of Low Data Register
PWM_PWRMATCH_HD_ZERO	0x0114	W	0x029401CC	Power Key Match of High Data for Zero Register
PWM_PWRMATCH_HD_ONE	0x0118	W	0x06FE0636	Power Key Match of High Data for One Register
PWM_PWRMATCH_VALUE0	0x011C	W	0x00000000	Power Key Match Value 0 Register
PWM_PWRMATCH_VALUE1	0x0120	W	0x00000000	Power Key Match Value 1 Register
PWM_PWRMATCH_VALUE2	0x0124	W	0x00000000	Power Key Match Value 2 Register
PWM_PWRMATCH_VALUE3	0x0128	W	0x00000000	Power Key Match Value 3 Register
PWM_PWRMATCH_VALUE4	0x012C	W	0x00000000	Power Key Match Value 4 Register
PWM_PWRMATCH_VALUE5	0x0130	W	0x00000000	Power Key Match Value 5 Register
PWM_PWRMATCH_VALUE6	0x0134	W	0x00000000	Power Key Match Value 6 Register
PWM_PWRMATCH_VALUE7	0x0138	W	0x00000000	Power Key Match Value 7 Register
PWM_PWRMATCH_VALUE8	0x013C	W	0x00000000	Power Key Match Value 8 Register
PWM_PWRMATCH_VALUE9	0x0140	W	0x00000000	Power Key Match Value 9 Register
PWM_PWRMATCH_VALUE10	0x0144	W	0x00000000	Power Key Match Value 10 Register

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Name	Offset	Size	Reset Value	Description
PWM_PWRMATCH_VALUE11	0x0148	W	0x00000000	Power Key Match Value 11 Register
PWM_PWRMATCH_VALUE12	0x014C	W	0x00000000	Power Key Match Value 12 Register
PWM_PWRMATCH_VALUE13	0x0150	W	0x00000000	Power Key Match Value 13 Register
PWM_PWRMATCH_VALUE14	0x0154	W	0x00000000	Power Key Match Value 14 Register
PWM_PWRMATCH_VALUE15	0x0158	W	0x00000000	Power Key Match Value 15 Register
PWM_PWRCAPTURE_VALUE	0x015C	W	0x00000000	Power Key Capture Value Register
PWM_IR_TRANS_ARBITER	0x0180	W	0x00000000	Power Key Match Control Register
PWM_IR_TRANS_CTRL0	0x0184	W	0x00001F00	IR Transmission control 0 register
PWM_IR_TRANS_CTRL1	0x0188	W	0x00000000	IR Transmission control 1 register
PWM_IR_TRANS_PRE	0x018C	W	0x11942328	IR transmission preload period
PWM_IR_TRANS_SPRE	0x0190	W	0x000008CA	IR transmission simple preload low period
PWM_IR_TRANS_LD	0x0194	W	0x00000230	IR Trans Out Data Low Period
PWM_IR_TRANS_HD	0x0198	W	0x069A0230	IR Trans Out High Period
PWM_IR_TRANS_BURST_FRAME	0x019C	W	0x2261A5E0	IR transmission frame and burst period
PWM_IR_TRANS_DATA_VALUE	0x01A0	W	0x00000000	IR Trans Output Data Value
PWM_IR_TRANS_STATUS	0x01A4	W	0x00000001	IR Trans Status
PWM_FREQ_ARBITER	0x01C0	W	0x00000000	Frequency Meter Arbiter Control Register
PWM_FREQ_CTRL	0x01C4	W	0x00000000	Frequency Meter control register
PWM_FREQ_TIMER_VALUE	0x01C8	W	0x00000000	Frequency Meter timer value register
PWM_FREQ_RESULT_VALUE	0x01CC	W	0x00000000	Frequency Meter result value register
PWM_COUNTER_ARBITER	0x0200	W	0x00000000	Counter Arbiter Control Register
PWM_COUNTER_CTRL	0x0204	W	0x00000000	Counter control register
PWM_COUNTER_LOW	0x0208	W	0x00000000	Counter Low register
PWM_COUNTER_HIGH	0x020C	W	0x00000000	Counter High register
PWM_WAVE_MEM	0x0400	W	0x00000000	Waveform Generator Memory Arbiter Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

34.4.3 Detail Registers Description

PWM_VERSION_ID

Address: **Operational Base** + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:24	RO	0x04	main_version Main version
23:16	RO	0x00	minor_version Minor version
15	RO	0x0	reserved
14	RO	0x0	biphasic_counter_support Biphasic counter support
13	RO	0x0	filter_support Filter support
12	RO	0x0	wave_support Waveform generator support
11	RO	0x0	counter_support Counter support
10	RO	0x0	freq_meter_support Frequency meter support
9	RO	0x0	power_key_support Power key support
8	RO	0x0	ir_trans_support IR transmission support
7:4	RO	0x4	channel_index Channel index
3:0	RO	0x4	channel_num_support Channel number support

PWM_ENABLE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	pwm_cnt_rd_en PWM channel CNT read enable. The CNT can be read for debug. 1'b0: Disabled 1'b1: Enabled
4	W1T	0x0	pwm_global_join_en PWM join global control enable. When this bit is set to 1, the PWM channel is enabled by pwm_global_en instead of pwm_en, and the following register can be updated at the posedge of pwm_global_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET

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Bit	Attr	Reset Value	Description
3	RW	0x0	force_clk_en 1'b0: Disabled, when PWM channel is inactive state, the clk_pwm to PWM Clock pre-scale module is blocked to reduce power consumption. 1'b1: Enabled, the clk_pwm to PWM Clock pre-scale module is always enabled.
2	W1T	0x0	pwm_ctrl_update_en PWM control update enable. The bit will be auto cleaned. The following register can be updated at the posedge of pwm_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET
1	RW	0x0	pwm_en PWM enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.
0	RW	0x0	pwm_clk_en PWM clock enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_CLK_CTRL

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_global_sel Clock global selection 1'b0: Select current channel scale clock 1'b1: Select global channel scale clock
14:13	RW	0x0	clk_src_sel Clock source selection 2'b00: Select clk_pwm as root clock source, Clock is from PLL and the frequency can be configured. 2'b01: Select clk_pwm_osc as root clock source, Clock is from crystal oscillator and the frequency is fixed. 2'b10: Select clk_pwm_rc as root clock source, Clock is from RC oscillator and the frequency is fixed.

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Bit	Attr	Reset Value	Description
12:4	RW	0x000	scale This field defines the scale factor applied to pre-scaled clock. The value N means the clock is divided by 2*N. it is valid from 1~256.
3	RO	0x0	reserved
2:0	RW	0x0	prescale This field defines the pre-scale factor applied to input clock. The value N means that the input clock is divided by 2^N.

PWM_CTRL

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8:6	RW	0x0	pwm_in_sel PWM in channel selection, the default value is corresponding channel, User can configure to another channel. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5 3'b110: PWM channel 6 3'b111: PWM channel 7
5	RW	0x0	aligned_vld_n 0: Aligned Mode Valid 1: Aligned Mode Invalid
4	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
3	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive

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Bit	Attr	Reset Value	Description
2	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
1:0	RW	0x0	pwm_mode 2'b00: One shot mode, PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt. 2'b01: Continuous mode, PWM produces the waveform continuously. 2'b10: Capture mode, PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved

PWM_PERIOD

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD This value defines the period of the output waveform for continuous mode or one-shot mode. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is considered and bit [0] always considered as 0.

PWM_DUTY

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY This value defines the duty cycle of the output waveform for continuous mode or one-shot mode. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is considered.

PWM_OFFSET

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	channel_output_offset If PWM is operated at the continuous mode or one-shot mode, this value defines the offset of the output waveform. This value is based on the PWM clock. The value ranges from 0 to (period-duty). This register takes effective when output aligned mode is invalid.

PWM_RPT

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Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rpt_second_dimensional This field defines the second dimensional repeated effective periods of output waveform. It can be used only in one-shot mode. The second dimensional waveform counter will increase 1 when first dimensional waveform counter reach rpt_first_dimensional. When reach rpt_second_dimensional, the PWM channel will be disabled and the one-shot interrupt will be asserted. The value N means N+1 repeated effective periods. The total waveform number will be (rpt_first_dimensional+1) multiply by (rpt_second_dimensional+1).
15:0	RW	0x0000	rpt_first_dimensional This field defines the first dimensional repeated effective periods of output waveform. When reach rpt_first_dimensional, the waveform counter will wrap back to 0 and restart counting and the reload interrupt will be asserted. User can update the configuration in the interrupt. It can be used in one-shot mode and Continuous mode. The value N means N+1 repeated effective periods.

PWM_FILTER_CTRL

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:4	RW	0x00	filter_number Filter window number
3:1	RO	0x0	reserved
0	RW	0x0	filter_enable 1'b0: Disabled 1'b1: Enabled

PWM_CNT

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_ENABLE_DELAY

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Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	pwm_enable_delay PWM enable delay

PWM_HPC

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HPC This value indicates the effective high polarity cycles of input waveform for capture mode. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_LPC

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LPC This value indicates the effective low polarity cycles of input waveform for capture mode. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_BIPHASIC_COUNTER_CTRL0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	biphasic_counter_mode0_edge_sel biphasic counter phase edge selection for mode 0 1'b0: Posedge 1'b1: Negedge
8	RW	0x0	biphasic_counter_clk_force_en Biphasic counter clock force enable
7	W1T	0x0	biphasic_counter_sync_en Biphasic counter synchronous enable

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Bit	Attr	Reset Value	Description
6	W1T	0x0	timer_clk_switch_mode Timer clock switch mode, it can set to 1'b1 only when biphasic_counter_mode is mode0. 1'b0: Normal mode 1'b1: Switch timer clock and measured clock. It can be used to provide testing accuracy or reduce testing time when the frequency of measured clock is low. It can also be used in scenarios where the start time of the measured clock is uncertain
5:3	RW	0x0	biphasic_counter_mode Biphasic counter mode 3'h0: Mode0 3'h1: Mode1 3'h2: Mode2 3'h3: Mode3 3'h4: Mode4 Other: Reserved
2	RW	0x0	biphasic_counter_clk_sel Biphasic counter clock selection 1'b0: Select clk_pwm, clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_osc, clock is from crystal oscillator and the frequency is fixed.
1	RW	0x0	biphasic_counter_continuous_mode Biphasic counter continuous mode
0	W1T	0x0	biphasic_counter_en Biphasic counter enable.

PWM_BIPHASIC_COUNTER_CTRL1

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:4	RW	0x00	biphasic_counter_filter_number Filter window number
3:1	RO	0x0	reserved
0	RW	0x0	biphasic_counter_filter_enable 1'b0: Disabled 1'b1: Enabled

PWM_BIPHASIC_COUNTER_TIMER_VALUE

Address: **Operational Base** + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	biphasic_counter_timer_value Biphasic counter timer value, the unit is one cycle of biphasic counter timer clock.

PWM_BIPHASIC_COUNTER_RESULT_VALUE

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	biphasic_counte_result_value Biphasic counter result value, it can read only after interrupt biphasic_counter_intsts is asserted.

PWM_BIPHASIC_COUNTER_RESULT_VALUE_SYNC

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	biphasic_counte_result_value_sync Biphasic counter result value with synchronized processing, it can read in real time when biphasic_counter_sync_en is set to 1.

PWM_INTSTS

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	W1C	0x0	biphasic_counter_intsts Biphasic counter interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
8	W1C	0x0	wave_middle_intsts Waveform address access middle address value interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
7	W1C	0x0	wave_max_intsts Waveform address access maximum address interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
6	W1C	0x0	it_trans_end_intsts IR Transmission end interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
5	W1C	0x0	pwr_intsts Power key match interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated

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Bit	Attr	Reset Value	Description
4	W1C	0x0	freq_intsts Frequency meter interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
3	W1C	0x0	reload_intsts Reload interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
2	W1C	0x0	oneshot_end_intsts Waveform end interrupt status for one-shot mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated
1	W1C	0x0	cap_hpc_intsts HPC interrupt status for capture mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated
0	W1C	0x0	cap_lpc_intsts LPC interrupt status for capture mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated

PWM_INT_EN

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	biphasic_couner_int_en Biphasic counter interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
8	RW	0x0	wave_middle_int_en Waveform address access middle address enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
7	RW	0x0	wave_max_int_en Waveform address access maximum address interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
6	RW	0x0	it_trans_end_int_en IR Transmission end interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled

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Bit	Attr	Reset Value	Description
5	RW	0x0	pwr_int_en Power key match interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
4	RW	0x0	freq_int_en Frequency meter interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
3	RW	0x0	reload_int_en Reload interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
2	RW	0x0	oneshot_end_int_en Waveform end interrupt enable for one-shot mode. 1'b0: Interrupt disabled 1'b1: Interrupt enabled
1	RW	0x0	cap_hpc_int_en HPC interrupt enable for capture mode 1'b0: Interrupt disabled 1'b1: Interrupt enabled
0	RW	0x0	cap_lpc_int_en LPC interrupt enable for capture mode 1'b0: Interrupt disabled 1'b1: Interrupt enabled

PWM_INT_MASK

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	biphasic_counter_int_mask Biphasic counter interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
8	RW	0x0	wave_middle_int_mask Waveform address access middle address mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
7	RW	0x0	wave_max_int_mask Waveform address access maximum address interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
6	RW	0x0	it_trans_end_int_mask IR Transmission end interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
5	RW	0x0	pwr_int_mask Power key match interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
4	RW	0x0	freq_int_mask Frequency meter interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
3	RW	0x0	reload_Int_mask Reload interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
2	RW	0x0	oneshot_end_mask Waveform end interrupt mask for one-shot mode. 1'b0: Interrupt not mask 1'b1: Interrupt mask
1	RW	0x0	cap_hpc_int_mask HPC interrupt mask for capture mode 1'b0: Interrupt not mask 1'b1: Interrupt mask
0	RW	0x0	cap_lpc_int_mask LPC interrupt mask for capture mode 1'b0: Interrupt not mask 1'b1: Interrupt mask

PWM_WAVE_MEM_ARBITER

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	wave_mem_read_lock Each bit controls the read lock of waveform generator memory. Once one channel obtains arbitration, other channels cannot read waveform generator memory. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	wave_mem_grant Each bit controls the grant of waveform generator memory for one channel. Once one channel obtains arbitration, other channels cannot write waveform generator memory. 1'b0: Don't Grant 1'b1: Grant

PWM_WAVE_MEM_STATUS

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	access_done Indicate the access to waveform generator memory is done.

PWM_WAVE_CTRL

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RW	0x00	wave_period_amplify Waveform generator table period value amplify, the value N means amplify by 2^N.
10:6	RW	0x00	wave_duty_amplify Waveform generator table duty value amplify, the value N means amplify by 2^N.
5:4	RW	0x1	wave_mem_clk_sel Waveform generator memory clock selection 2'b00: Select clk_pwm 2'b01: Select clk_pwm_osc 2'b10: Select clk_pwm_rc
3	RW	0x0	wave_update_mode Waveform generator update mode 1'b0: The address will wrap back to minimum address when increase to maximum address, and then increase again. 1'b1: The address will change to decreasing when increasing to the maximum address. it will return to increasing when decrease to the minimum value.
2	RW	0x0	wave_width_mode Waveform generator width mode 1'b0: 8bits 1'b1: 16bits Note: The table is 8bit, User can compose 16 bits with two adjacent addresses

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Bit	Attr	Reset Value	Description
1	RW	0x0	wave_period_en Waveform generator period enable. The period cycle of the output waveform is controlled by waveform generator table instead of register PWM_PERIOD when this bit is set to 1. The period will be updated every waveform number of rpt_first_dimensional.
0	RW	0x0	wave_duty_en Waveform generator duty enable. The duty cycle of the output waveform is controlled by waveform generator table instead of register PWM_DUTY when this bit is set to 1. The duty will be updated every waveform number of rpt_first_dimensional.

PWM_WAVE_MAX

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	wave_period_max The maximum index of period.
15:10	RO	0x00	reserved
9:0	RW	0x000	wave_duty_max The maximum index of duty.

PWM_WAVE_MIN

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	wave_period_min The minimum index of period.
15:10	RO	0x00	reserved
9:0	RW	0x000	wave_duty_min The minimum index of duty.

PWM_WAVE_OFFSET

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	wave_offset The initial offset index of duty and period

PWM_WAVE_MIDDLE

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	wave_middle The middle index of duty and period.

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PWM_WAVE_HOLD

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	middle_hold The time to hold at middle index. the unit is waveform number of rpt_first_dimensional
15:8	RW	0x00	min_hold The time to hold at minimum index. the unit is waveform number of rpt_first_dimensional
7:0	RW	0x00	max_hold The time to hold at maximum index. the unit is waveform number of rpt_first_dimensional

PWM_GLOBAL_ARBITER

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	global_read_lock Each bit controls the read lock of global control registers. Once one channel obtains arbitration, other channels cannot read global registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	global_grant Each bit controls the grant of global control for one channel. Once one channel obtains arbitration, other channels cannot write global registers. 1'b0: Don't Grant 1'b1: Grant

PWM_GLOBAL_CTRL

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	W1T	0x0	global_pwm_ctrl_update_en PWM global control update enable. The bit will be auto cleaned. The following register can be updated at the posedge of pwm_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET

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Bit	Attr	Reset Value	Description
0	RW	0x0	global_pwm_en Global PWM enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWRMATCH_ARBITER

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	pwrkey_read_lock Each bit controls the read lock of power key function. Once one channel obtains arbitration, other channels cannot read power key registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	pwrkey_grant Each bit controls the grant of power key function for one channel. Once one channel obtains arbitration, other channels cannot write power key registers. 1'b0: Don't Grant 1'b1: Grant

PWM_PWRMATCH_CTRL

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	pwrkey_int_ctrl 1'b0: Assert interrupt after key capture with power key match 1'b1: Assert interrupt after key capture without power key match
2	RW	0x0	pwrkey_capture_ctrl 1'b0: Capture the value after interrupt 1'b1: Capture the value directly
1	RW	0x0	pwrkey_polarity 1'b0: PWM in polarity is positive 1'b1: PWM in polarity is negative
0	RW	0x0	pwrkey_enable 1'b0: Disabled 1'b1: Enabled

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PWM_PWRMATCH_LPRE

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x238c	cnt_max The maximum counter value
15:0	RW	0x22c4	cnt_min The minimum counter value

PWM_PWRMATCH_HPRE

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x11f8	cnt_max The maximum counter value
15:0	RW	0x1130	cnt_min The minimum counter value

PWM_PWRMATCH_LD

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value
15:0	RW	0x01cc	cnt_min The minimum counter value

PWM_PWRMATCH_HD_ZERO

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value
15:0	RW	0x01cc	cnt_min The minimum counter value

PWM_PWRMATCH_HD_ONE

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x06fe	cnt_max The maximum counter value
15:0	RW	0x0636	cnt_min The minimum counter value

PWM_PWRMATCH_VALUE0

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value0 Power key match value 0

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PWM_PWRMATCH_VALUE1

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value1 Power key match value 1

PWM_PWRMATCH_VALUE2

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value2 Power key match value 2

PWM_PWRMATCH_VALUE3

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value3 Power key match value 3

PWM_PWRMATCH_VALUE4

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value4 Power key match value 4

PWM_PWRMATCH_VALUE5

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value5 Power key match value 5

PWM_PWRMATCH_VALUE6

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value6 Power key match value 6

PWM_PWRMATCH_VALUE7

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value7 Power key match value 7

PWM_PWRMATCH_VALUE8

Address: **Operational Base** + offset (0x013C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value8 Power key match value 8

PWM_PWRMATCH_VALUE9

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value9 Power key match value 9

PWM_PWRMATCH_VALUE10

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value10 Power key match value 10

PWM_PWRMATCH_VALUE11

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value11 Power key match value 11

PWM_PWRMATCH_VALUE12

Address: **Operational Base** + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value12 Power key match value 12

PWM_PWRMATCH_VALUE13

Address: **Operational Base** + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value13 Power key match value 13

PWM_PWRMATCH_VALUE14

Address: **Operational Base** + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value14 Power key match value 14

PWM_PWRMATCH_VALUE15

Address: **Operational Base** + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value15 Power key match value 15

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PWM_PWRCAPTURE_VALUE

Address: **Operational Base** + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pwrkey_capture_value Power key capture value

PWM_IR_TRANS_ARBITER

Address: **Operational Base** + offset (0x0180)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	it_trans_read_lock Each bit controls the read lock of IR transmission function. Once one channel obtains arbitration, other channels cannot read power key registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	ir_trans_grant Each bit controls the grant of IR transmission function for one channel. Once one channel obtains arbitration, other channels cannot write power key registers. 1'b0: Don't Grant 1'b1: Grant

PWM_IR_TRANS_CTRL0

Address: **Operational Base** + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	ir_trans_clk_en_force PWM IR Trans Out Function clock enable force.
12:8	RW	0x1f	ir_trans_length_within_one_frame 0x00~0x1F is corresponding to data length 1~32
7:4	RW	0x0	ir_trans_format PWM IR Trans format 4'h0: NEC with simple repeat code 4'h1: NEC with full repeat code 4'h2: TC9012 4'h3: SONY Others: reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	it_trans_mode 1'b0: One shot mode, PWM produces the waveform within the repeated times defined by ir_trans_rtp_cnt. 1'b1: Continuous mode, PWM produces the waveform continuously.
2	RW	0x0	it_trans_inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
1	RW	0x0	ir_trans_duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
0	RW	0x0	ir_trans_out_enable 1'b0: disable PWM IR Trans Out Function 1'b1: enable PWM IR Trans Out Function

PWM_IR_TRANS_CTRL1

Address: **Operational Base** + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	ir_trans_rpt This field defines the repeated number for IR transmission. The value N means N+1 repeated effective periods.

PWM_IR_TRANS_PRE

Address: **Operational Base** + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RW	0x1194	ir_trans_out_high_preload IR Trans Out High Preload Register
15:0	RW	0x2328	ir_trans_out_low_preload IR Trans Out Low Preload Register

PWM_IR_TRANS_SPRE

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x08ca	ir_trans_out_high_simple_preload PWM IR Trans Out High Simple Preload Register

PWM_IR_TRANS_LD

Address: **Operational Base** + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0230	ir_trans_out_data_low_period IR Trans Out Data Low Period Register

PWM_IR_TRANS_HD

Address: **Operational Base** + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x069a	ir_trans_out_high_period_for_one IR Trans Out High Period for One Register
15:0	RW	0x0230	ir_trans_out_high_period_for_zero IR Trans Out High Period for Zero Register

PWM_IR_TRANS_BURST_FRAME

Address: **Operational Base** + offset (0x019C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x226	ir_trans_out_burst_period PWM IR Trans Out Burst Period Register
19:18	RO	0x0	reserved
17:0	RW	0x1a5e0	ir_trans_out_frame_period PWM IR Trans Out Frame Period

PWM_IR_TRANS_DATA_VALUE

Address: **Operational Base** + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ir_trans_out_value PWM IR Trans Out Value Register

PWM_IR_TRANS_STATUS

Address: **Operational Base** + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	ir_state_idle 1'b0: PWM IR Trans Busy 1'b1: PWM IR Trans Idle

PWM_FREQ_ARBITER

Address: **Operational Base** + offset (0x01C0)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	freq_read_lock Each bit controls the read lock of frequency meter function. Once one channel obtains arbitration, other channels cannot read frequency meter registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	freq_grant Each bit controls the grant of frequency meter function for one channel. Once one channel obtains arbitration, other channels cannot write frequency meter registers. 1'b0: Don't Grant 1'b1: Grant

PWM_FREQ_CTRL

Address: **Operational Base** + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	freq_timer_clk_sel Frequency meter timer clock selection 1'b0: Select clk_pwm, clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_osc, clock is from crystal oscillator and the frequency is fixed.
6	W1T	0x0	freq_timer_clk_switch_mode Timer clock switch mode 1'b0: Normal mode 1'b1: Switch timer clock and measured clock. It Can be used to provide testing accuracy or reduce testing time when the frequency of measured clock is low. It can also be used in scenarios where the start time of the measured clock is uncertain

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	freq_channel_sel Frequency Meter channel selection. It's valid only when freq_clk_sel set to 1'b0. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5 3'b110: PWM channel 6 3'b111: PWM channel 7
2	RO	0x0	reserved
1	RW	0x0	freq_clk_sel Frequency Meter clock selection 1'b0: Input from PWM IO 1'b1: Frequency clock from CRU
0	W1T	0x0	freq_en Frequency Meter enable.

PWM_FREQ_TIMER_VALUE

Address: **Operational Base** + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	freq_timer_value Frequency Meter timer value, the unit is one cycle frequency meter timer clock.

PWM_FREQ_RESULT_VALUE

Address: **Operational Base** + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	freq_result_value The frequency result value, the unit is one cycle of tested clock. Once the freq_intsts interrupt is asserted, User can get the frequency by this value. When timer_clk_switch_mode set to 1'b0, the frequency result is (freq_timer*freq_result_value)/freq_timer_value. When timer_clk_switch_mode set to 1'b1, the frequency result is (freq_timer*freq_timer_value)/freq_result_value. Notes: freq_osc is the frequency of SOC crystal oscillator.

PWM_COUNTER_ARBITER

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	counter_read_lock Each bit controls the read lock of counter function. Once one channel obtains arbitration, other channels cannot read counter registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	counter_grant Each bit controls the grant of counter for one channel. Once one channel obtains arbitration, other channels cannot write counter registers. 1'b0: Don't Grant 1'b1: Grant

PWM_COUNTER_CTRL

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	W1T	0x0	counter_clr Counter value clear.
5:3	RW	0x0	counter_channel_sel Counter channel selection. It's valid only when counter_clk_sel set to 1'b00. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5 3'b110: PWM channel 6 3'b111: PWM channel 7
2:1	RW	0x0	counter_clk_sel Counter clock selection 1'b0: Input from PWM IO 1'b1: Counter clock from CRU
0	RW	0x0	counter_en Counter enable.

PWM_COUNTER_LOW

Address: **Operational Base** + offset (0x0208)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	counter_low_bits Indicates low 32bits of counter value. The value of counter ranges from 0 to 2^64-1, The unit is one cycle of tested clock

PWM_COUNTER_HIGH

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	counter_high_bits Indicates high 32bits of the counter value. The value of counter ranges from 0 to 2^64-1, The unit is one cycle of tested clock

PWM_WAVE_MEM

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	wave_mem_base_address Waveform Generator memory base address

34.5 Interface Description

Table 34-2 PWM_M0 Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
PWM0_CH0_M0	I/O	SAI0_MCLK_M1/PDM0_CLK0_M0/UART10_TX_M2/PWM0_CH0_M0/GPIO0_C4_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[3:0] = 0xc
PWM0_CH1_M0	I/O	PDM0_CLK1_M0/HDMI_TX_CEC_M1/SPI0_CSN1_M0/PWM0_CH1_M0/GPIO0_C3_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[15:12] = 0xc
PWM1_CH0_M0	I/O	REF_CLK1_OUT/I2C1_SCL_M1/UART4_TX_M2/PWM1_CH0_M0/GPIO0_B4_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[3:0] = 0xc
PWM1_CH1_M0	I/O	REF_CLK2_OUT/I2C1_SDA_M1/UART4_RX_M2/PWM1_CH1_M0/GPIO0_B5_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[7:4] = 0xc
PWM1_CH2_M0	I/O	SDMMC0_PWREN/SDMMC1_DETN_M2/HDMI_TX_HPDIN_M1/EDP_TX_HPDIN_M1/PWM1_CH2_M0/GPIO0_B6_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[11:8] = 0xc
PWM1_CH3_M0	I/O	I2C2_SDA_M0/UART1_RX_M0/CPULIT_AVS/PWM1_CH3_M0/GPIO0_C0_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[3:0] = 0xc
PWM1_CH4_M0	I/O	I2C2_SCL_M0/UART1_TX_M0/NPU_AVS/PWM1_CH4_M0/GPIO0_B7_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[15:12] = 0xc

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Module Pin	Direction	Pin Name	IOMUX Setting
PWM1_CH5_M0	I/O	SAI0_SDI2_M1/SAI0_SDO2_M1/PDM0_SDI2_M0/I2C4_SCL_M0/CPUBIG_AVS/PWM1_CH5_M0/UART1_CTSN_M0/GPIO0_D2_d	PMU1_IOC_GPIO0D_IOMUX_SEL_L[11:8] = 0xc
PWM2_CH0_M0	I/O	SAI0_SDI3_M1/SAI0_SDO1_M1/PDM0_SDI3_M0/I2C4_SDA_M0/GPU_AVS/PWM2_CH0_M0/UART1_RTSN_M0/GPIO0_D3_d	PMU1_IOC_GPIO0C_IOMUX_SEL_L[15:12] = 0xc
PWM2_CH1_M0	I/O	EMMC_RSTN/FSPI0_CSN0/UART6_RX_M2/I2C7_SDA_M0/MIPI_TE_M3/PWM2_CH1_M0/GPIO1_B3_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[15:12] = 0xc
PWM2_CH2_M0	I/O	SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/CAN0_RX_M0/PWM2_CH2_M0/GPIO2_A0_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[3:0] = 0xe
PWM2_CH3_M0	I/O	SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4] = 0xe
PWM2_CH4_M0	I/O	SDMMC0_CMD/FSPI1_CSN0_M0/SAI3_SDO_M3/UART5_RX_M2/I2C5_SDA_M0/SPI0_CSN0_M1/PWM2_CH4_M0/GPIO2_A4_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[3:0] = 0xe
PWM2_CH5_M0	I/O	SAI1_MCLK_M0/SAI4_MCLK_M0/AUPLL_CLK_IN_M2/PWM2_CH5_M0/GPIO4_A2_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[11:8] = 0xd
PWM2_CH6_M0	I/O	SAI1_SDO0_M0/SAI4_SDI_M0/SPI3_CLK_M2/PWM2_CH6_M0/GPIO4_A7_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[15:12] = 0xd
PWM2_CH7_M0	I/O	SAI1_SDI0_M0/SAI4_SDO_M0/PDM1_SDI0_M1/SPI4_CSN0_M2/SPI3_CSN1_M2/PWM2_CH7_M0/GPIO4_B3_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[15:12] = 0xd

Table 34-2 PWM_M1 Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
PWM0_CH0_M1	I/O	ETH1_TXD3_M1/SDMMC1_CMD_M0/PDM0_SDI2_M2/UART3_TX_M2/SPI1_CSN1_M0/PWM0_CH0_M1/GPIO1_C0_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[3:0] = 0xd
PWM0_CH1_M1	I/O	DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[7:4] = 0xe
PWM1_CH0_M1	I/O	ETH1_RXD2_M1/SDMMC1_D0_M0/SAI3_SCLK_M1/I2C9_SDA_M1/SPI1_CLK_M0/PCIE1_CLKREQN_M1/PWM1_CH0_M1/GPIO1_B4_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[3:0] = 0xd
PWM1_CH1_M1	I/O	ETH1_RXD3_M1/SDMMC1_D1_M0/SAI3_LRCK_M1/I2C9_SCL_M1/SPI1_MOSI_M0/PWM1_CH1_M1/GPIO1_B5_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[7:4] = 0xd

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Module Pin	Direction	Pin Name	IOMUX Setting
PWM1_CH2_M1	I/O	ETH1_PPSCLK_M1/SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_CSN1_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[11:8] = 0xd
PWM1_CH3_M1	I/O	ETH1_MDC_M1/SAI2_LRCK_M0/I3C0_SCL_M1/PWM1_CH3_M1/GPIO1_D2_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[11:8] = 0xd
PWM1_CH4_M1	I/O	ETH1_MDIO_M1/SAI2_SDI_M0/I3C0_SDA_M1/PWM1_CH4_M1/GPIO1_D3_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[15:12] = 0xd
PWM1_CH5_M1	I/O	DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[3:0] = 0xe
PWM2_CH0_M1	I/O	DSM_AUD_RP_M1/HDMI_TX_SCL/I2C2_SCL_M3/CAN0_TX_M1/UART9_TX_M2/PWM2_CH0_M1/GPIO4_C2_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[11:8] = 0xe
PWM2_CH1_M1	I/O	DSM_AUD_RN_M1/HDMI_TX_SDA/I2C2_SDA_M3/CAN0_RX_M1/UART9_RX_M2/PWM2_CH1_M1/GPIO4_C3_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[15:12] = 0xe
PWM2_CH2_M1	I/O	SAI4_SDI_M2/VP1_SYNC_OUT/PCIE0_CLKREQN_M3/SATA0_ACTLED_M1/I2C6_SCL_M3/SPI4_MISO_M0/CAN1_TX_M1/PWM2_CH2_M1/GPIO4_C6_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[11:8] = 0xe
PWM2_CH3_M1	I/O	SAI4_SCLK_M2/VP2_SYNC_OUT/I2C6_SDA_M3/SPI4_CLK_M0/CAN1_RX_M1/PWM2_CH3_M1/GPIO4_C7_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[15:12] = 0xe
PWM2_CH4_M1	I/O	SAI1_SCLK_M0/FLEXBUS1_CSN_M4/SPI3_CSN0_M2/UART5_RTSN_M1/I2C2_SCL_M2/PWM2_CH4_M1/GPIO4_A3_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[15:12] = 0xd
PWM2_CH5_M1	I/O	ISP_FLASH_TRIGOUT_M1/SAI4_SDO_M2/VP0_SYNC_OUT/SATA1_ACTLED_M1/I2C3_SDA_M3/SPI4_MOSI_M0/UART6_RX_M3/PWM2_CH5_M1/GPIO4_C5_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[7:4] = 0xe
PWM2_CH6_M1	I/O	ISP_PRELIGHT_TRIG_M1/SAI4_LRCK_M2/DP_HPDIN_M0/I2C3_SCL_M3/SPI4_CSN0_M0/UART6_TX_M3/PWM2_CH6_M1/GPIO4_C4_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[3:0] = 0xe
PWM2_CH7_M1	I/O	EMMC_CLK/FSPI0_CLK/SAI0_SDO3_M2/SAI0_SDI1_M2/PDM0_CLK0_M1/PWM2_CH7_M1/GPIO1_B1_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[7:4] = 0xc

Table 34-3 PWM_M2 Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
PWM0_CH0_M2	I/O	VI_CIF_D2/ETH1_TXD2_M0/SAI2_LRCK_M1/PDM1_SDI3_M0/UART11_RTSN_M1/SPI1_MISO_M1/PWM0_CH0_M2/GPIO2_C3_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[15:12] = 0xd
PWM0_CH1_M2	I/O	ETH1_TXD1_M0/SAI4_LRCK_M3/UART4_RTSN_M0/I2C5_SDA_M2/PWM0_CH1_M2/GPIO2_C7_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[15:12] = 0xd
PWM1_CH0_M2	I/O	VI_CIF_D5/ETH1_RXD2_M0/ETH0_PTP_REFCLK_M1/PDM1_SDI1_M0/UART9_RX_M0/PWM1_CH0_M2/GPIO2_C0_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[3:0] = 0xd

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Module Pin	Direction	Pin Name	IOMUX Setting
PWM1_CH1_M2	I/O	VI_CIF_D4/ETH1_RXD3_M0/ETH0_PPSCLK_M1/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[7:4] = 0xd
PWM1_CH2_M2	I/O	VI_CIF_D3/ETH1_RXCLK_M0/ETH0_PPSTRIG_M1/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[11:8] = 0xd
PWM1_CH3_M2	I/O	VI_CIF_D1/ETH1_TXD3_M0/SAI2_SDO_M1/PDM1_SDI0_M0/UART11_TX_M1/SPI1_CSN0_M1/PWM1_CH3_M2/GPIO2_C4_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[3:0] = 0xd
PWM1_CH4_M2	I/O	VI_CIF_D0/ETH1_TXCLK_M0/SAI2_SDI_M1/PDM1_CLK0_M0/UART11_RX_M1/SPI1_CLK_M1/PWM1_CH4_M2/GPIO2_C5_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[7:4] = 0xd
PWM1_CH5_M2	I/O	ETH1_TXD0_M0/SAI4_SCLK_M3/UART4_CTSN_M0/I2C5_SCL_M2/PWM1_CH5_M2/GPIO2_C6_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[11:8] = 0xd
PWM2_CH0_M2	I/O	ETH1_TXCTL_M0/SAI4_SDI_M3/UART4_TX_M0/I2C6_SCL_M2/PWM2_CH0_M2/GPIO2_D0_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[3:0] = 0xd
PWM2_CH1_M2	I/O	ETH1_RXD0_M0/SAI4_SDO_M3/UART4_RX_M0/I2C6_SDA_M2/PWM2_CH1_M2/GPIO2_D1_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[7:4] = 0xd
PWM2_CH2_M2	I/O	CAM_CLK0_OUT_M1/ETH1_RXD1_M0/SAI4_MCLK_M3/UART6_TX_M1/I3C1_SCL_M0/PWM2_CH2_M2/GPIO2_D2_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[11:8] = 0xd
PWM2_CH3_M2	I/O	ETH1_RXCTL_M0/UART6_RX_M1/I3C1_SDA_M0/PWM2_CH3_M2/GPIO2_D3_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[15:12] = 0xd
PWM2_CH4_M2	I/O	ISP_PRELIGHT_TRIG_M0/ETH1_MDC_M0/UART6_RTSN_M1/I2C9_SDA_M2/PWM2_CH4_M2/GPIO2_D4_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[3:0] = 0xd
PWM2_CH5_M2	I/O	ISP_FLASH_TRIGOUT_M0/ETH1_MDIO_M0/UART6_CTSN_M1/I2C9_SCL_M2/PWM2_CH5_M2/GPIO2_D5_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[7:4] = 0xd
PWM2_CH6_M2	I/O	CAM_CLK1_OUT_M1/ETH_CLK1_25M_OUT_M0/ETH0_MCLK_M1/SAI3_MCLK_M2/SPDIF_RX0_M2/UART9_RTSN_M0/I3C1_SDA_PU_M0/PWM2_CH6_M2/GPIO2_D6_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[11:8] = 0xd
PWM2_CH7_M2	I/O	CAM_CLK2_OUT_M1/ETH1_MCLK_M0/ETH_CLK0_25M_OUT_M1/SAI0_SDO3_M0/SPDIF_TX0_M2/UART9_CTSN_M0/SPI3_CSN1_M0/PWM2_CH7_M2/GPIO2_D7_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[15:12] = 0xd

Table 34-3 PWM_M3 Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
PWM0_CH0_M3	I/O	VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0] = 0xc
PWM0_CH1_M3	I/O	VO_LCDC_D13/VO_EBC_SDDO13/ETH0_TXCLK_M0/DSMC_DQS1/FLEXBUS0_CLK/SPI3_CSN0_M1/PWM0_CH1_M3/GPIO3_B6_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[11:8] = 0xc

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Module Pin	Direction	Pin Name	IOMUX Setting
PWM1_CH0_M3	I/O	VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 0xc
PWM1_CH1_M3	I/O	VO_LCDC_D22/VO_EBC_GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[7:4] = 0xc
PWM1_CH2_M3	I/O	VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8] = 0xc
PWM1_CH3_M3	I/O	VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[7:4] = 0xc
PWM1_CH4_M3	I/O	VO_LCDC_D15/VO_EBC_SDDO15/ETH0_TXD1_M0/SPDIF_RX1_M0/DSMC_DATA9/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[3:0] = 0xc
PWM1_CH5_M3	I/O	VO_LCDC_D14/VO_EBC_SDDO14/ETH0_TXD0_M0/SPDIF_TX1_M0/DSMC_DATA8/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4] = 0xc
PWM2_CH0_M3	I/O	VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 0xc
PWM2_CH1_M3	I/O	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 0xc
PWM2_CH2_M3	I/O	VO_LCDC_D6/VO_EBC_SDDO6/SAI1_SDO0_M1/DSMC_DATA4/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[7:4] = 0xc
PWM2_CH3_M3	I/O	VO_LCDC_D3/VO_EBC_SDDO3/SAI1_MCLK_M1/DSMC_DATA1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[3:0] = 0xc
PWM2_CH4_M3	I/O	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 0xc
PWM2_CH5_M3	I/O	VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[15:12] = 0xc

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Module Pin	Direction	Pin Name	IOMUX Setting
PWM2_CH6_M3	I/O	VO_LCDC_VSYNC/VO_EBC_SDCLK/SAI1_SDI3_M1/DSMC_CLKN/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:8] = 0xc
PWM2_CH7_M3	I/O	VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12] = 0xc

Notes: I=input, O=output, I/O=input/output.

34.6 Application Notes

34.6.1 PWM Capture Mode Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.pwm_mode to 2'b10 to select capture mode.
4. Set PWM_INT_EN.cap_lpc_int_en/cap_hpc_int_en to 1'b1 to enable the interrupt.
5. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
6. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt status. User should read the PWM_HPC register to know the effective high cycles of input waveforms when cap_hpc_intsts is asserted and read the PWM_LPC register to know the effective low cycles when cap_lpc_intsts is asserted. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
7. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

34.6.2 PWM Power key Capture Mode Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division. The clock frequency should be 1 MHz after division.
3. Set PWM_CTRL.pwm_mode to 2'b10 to select capture mode.
4. Set PWM_PWRMATCH_ARBITER.pwrkey_grant to 8'b01 to set channel 0 for capture.
5. Set PWM_INT_EN.pwr_int_en to 1'b1 to enable the interrupt.
6. Set PWM_PWRMATCH_VALUE0~15 registers for the 16 power key match value.
7. Set max_cnt and min_cnt of follow register: PWM_PWRMATCH_LPRE, PWM_PWRMATCH_HPRE, PWM_PWRMATCH_LD, PWM_PWRMATCH_HD_ZERO, PWM_PWRMATCH_HD_ONE. It doesn't need to set these registers if the default value can meet the requirement.
8. Set PWM_PWRMATCH_CTRL.pwrkey_polarity for the polarity of power key signal.
9. Set PWM_PWRMATCH_CTRL.pwrkey_enable to 1'b1 to enable power key mode.
10. Set PWM_FILTER_CTRL.filter_number/filter_enable to enable filter. (Optional).
11. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
12. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt status, and refer to PWM_PWRCAPTURE_VALUE to know the power key capture value. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
13. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

34.6.3 PWM Continuous Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD and PWM_DUTY register.
5. Set PWM_RPT.rpt_first_dimensional for reload operation (Optional).
6. Set PWM_CTRL.pwm_mode to 2'b01 to select continuous mode.
7. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.

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8. Set PWM_PERIOD and DUTY, then set PWM_ENABLE.pwm_ctrl_update_en to 1'b1 to update configuration (Optional).
9. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

34.6.4 PWM One-shot Mode Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD and PWM_DUTY register.
5. Set PWM_RPT.rpt_first_dimensional for reload operation (Option).
6. Set PWM_RPT.rpt_second_dimensional.
7. Set PWM_CTRL.pwm_mode to 2'b00 to select one shot mode.
8. Set INT_EN.oneshot_end_int_en to 1'b1 to enable interrupt.
9. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
10. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt. PWM_CTRL.pwm_en/pwm_clk_en is automatically cleared.

34.6.5 Multi-channel synchronous start Usage Flow

1. Set PWM_ENABLE.pwm_en of all synchronous channels to 1'b0 to disable the PWM channel.
2. Set PWM_CTRL.pwm_mode/output_mode/duty_pol/inactive_pol, PWM_PERIOD and PWM_DUTY register of all synchronous channels.
3. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel of channel 0 to configure the clock selection and division.
4. Set PWM_Enable.pwm_global_join_en of all synchronous channels to 1'b1.
5. Enable the INT_EN.oneshot_end_int_en of channel 0 to enable interrupt generation if the channel is desired to work in the one-shot mode.
6. Set PWM_ENABLE.pwm_clk_en of channel 0 to 1'b1 to enable clock.
7. Set PWM_GLOBAL_ARBITER.global_grant to 8'h01 to set channel 0 as main channel.
8. Set PWM_GLOBAL_CTRL.global_pwm_en to enable all synchronous channels.
9. Set PWM_PERIOD and DUTY to all synchronous channel, then set PWM_GLOBAL_CTRL.global_pwm_ctrl_update_en to 1'b1 to update configuration of all synchronous channels (Optional).
10. If user want to disable PWM channel, set PWM_GLOBAL_CTRL.global_pwm_en to 1'b0, then set PWM_CTRL.pwm_clk_en of channel 0 to 1'b0 to disable clock.

34.6.6 IR transmission Usage Flow

1. Set PWM_CTRL.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division. The clock frequency should be 1 MHz after division.
3. Set PWM_CTRL.pwm_clk_en to 1'b1 to enable clock.
4. Set PWM_IR_TRANS_ARBITER.ir_trans_grant to 8'b01 to set channel 0 for transmission.
5. Set PWM_IR_TRANS_CTRL0.format/it_trans_mode/ir_trans_duty_pol/ ir_trans_length_within_one_frame/it_trans_inactive_pol
6. Set PWM_IR_TRANS_DATA_VALUE.ir_trans_out_value to the data which need to transmit.
7. Set the PWM_IR_TRANS_CTRL0.ir_trans_rpt if the channel is desired to work in the one-shot mode.
8. Set PWM_IR_TRANS_CTRL0.transout_en to 1'b1 to enable PWM IR transmission.
9. If user want to disable the output waveform, set PWM_IR_TRANS_CTRL0.transout_en to 1'b0, the channel will be disable at the end of one frame.

34.6.7 Clock counter Usage Flow

1. Set PWM_COUNTER_ARBITER.counter_grant to 8'h01 to use channel 0.
2. Set PWM_COUNTER_CTRL.counter_clk_sel/counter_channel_sel to select clock.
3. Set PWM_COUNTER_CTRL.counter_en to 1'b1 to enable clock counter.
4. Refer to PWM_COUNTER_LOW/ PWM_COUNTER_HIGH to gets the counter value.
5. If user want to disable clock counter, set PWM_COUNTER_CTRL.counter_en to 1'b0, then

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set PWM_COUNTER_ARBITER.counter_grant to 8'h0.

34.6.8 Clock Frequency meter Usage Flow

1. Set PWM_FREQ_ARBITER.freq_grant to 8'h01 to use channel 0.
2. Set PWM_FREQ_CTRL.freq_clk_sel/freq_channel_sel to select clock.
3. Set PWM_FREQ_CTRL.freq_timer_clk_sel to select timer clock.
4. Set PWM_FREQ_TIMER_VALUE.freq_timer_value to set timer.
5. Set PWM_INT_EN.freq_int_en to enable interrupt.
6. Set PWM_FREQ_CTRL.freq_en to 1'b1 to enable clock frequency meter.
7. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. Then refer PWM_FREQ_RESULT_VALUE.freq_result_value to get result. The frequency can be calculated as formula: frequency_timer* freq_result_value/ freq_timer_value. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
8. If user want to disable clock frequency meter, set PWM_FREQ_ARBITER.freq_grant to 8'h0.

34.6.9 Biphasic Counter Usage Flow

1. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_clk_sel to select clock.
2. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_mode to select mode.
3. Set PWM_BIPHASIC_COUNTER_CTRL1.biphasic_counter_filter_number/ biphasic_counter_filter_enable to set the filter.
4. Set PWM_BIPHASIC_COUNTER_TIMER_VALUE. biphasic_counter_timer_value to set timer.
5. Set PWM_INT_EN.biphasic_couner_int_en to enable interrupt.
6. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_en to 1'b1 to enable biphasic counter.
7. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. Then refer PWM_BIPHASIC_COUNTER_RESULT_VALUE to get the result. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.

34.6.10 Generates Waveform Through Lookup Table Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD register, the value should be 1~256.
5. Set PWM_WAVE_CTRL.wave_duty_en to 1'b1 to enable duty to reload through lookup table.
6. Set PWM_WAVE_CTRL.wave_update_mode to 1'b1.
7. Set PWM_WAVE_MAX.wave_duty_max.
8. Set PWM_WAVE_MIN.wave_duty_min.
9. Set the duty value in lookup table from offset address wave_duty_min to wave_duty_max. The base address of lookup table is PWM_WAVE_MEM.
10. Set PWM_RPT.rpt_first_dimensional for reloading interval.
11. Set PWM_CTRL.pwm_mode to 2'b01 to select continuous mode.
12. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.

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Chapter 35 RKCAN

35.1 Overview

CAN (Rockchip Controller Area Network) bus is a robust vehicle bus standard designed to allow microcontrollers and devices to communicate with each other in applications without a host computer. It is a message-based protocol, designed originally for multiplex electrical wiring within automobiles to save on copper, but is also used in many other contexts.
RKCAN controller supports the following features:

- Support CAN and CANFD protocol
- Support AHB slave interface
- Support AHB master interface
- Support classical and can-fd transmit or receive standard frame
- Support classical and can-fd transmit or receive extended frame
- Support transmit or receive data frame, remote frame, overload frame, error frame and frame interval
- Support transmit or receive error count
- Support acceptance filter
- Support bit error, bit stuffing error, form error, ack error and crc error
- Support interrupt and all interrupt can be masked
- Support controller status query
- Support error code check
- Support self test mode
- Support single sample and three sample configurable
- Support SJW(reSynchronization Jump Width) configurable
- Support BRP(system prescaler coefficient) configurable
- Support bit timing configurable
- Support loop-back mode for self-test operation
- Support silent mode for debug
- Support auto retransmission mode
- Support auto bus on after bus-off state
- Support 2 transmit buffers
- Support Internal Storage Mode
- Support protocol exception event
- Support DMA

35.2 Function Description

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

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35.2.1 Block Diagram

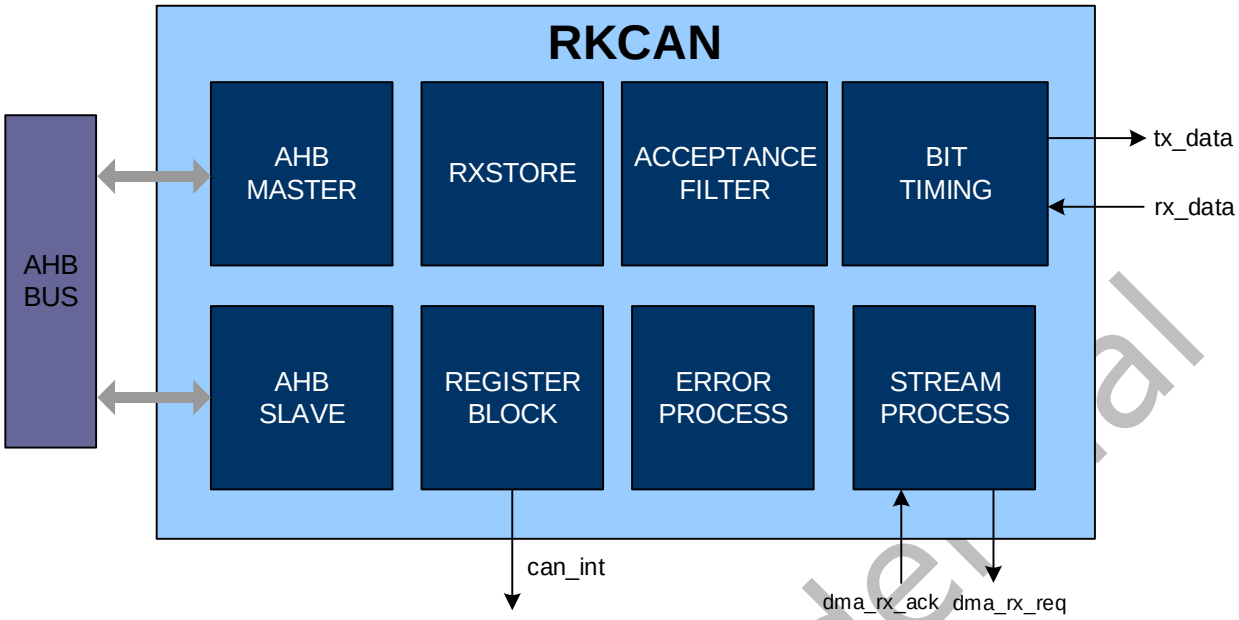

Fig. 35-1 RKCAN Controller Block Diagram

This version of RKCAN controller includes the previous version of CAN logic in compliance with old software application and also includes new CANFD logic which support transmitting and receiving both CAN and CANFD frame.

35.2.2 ACCEPTANCE FILTER

The Acceptance Filter (ATF) is a receive filter module. RKCAN can filter the received CAN frames based on four identifiers: ID, RTR, and DLC. There are five sets of ID_RTR registers and one set of DLC registers for configuring the filter mode of RKCAN.The filtering mode based on ID and RTR has two types: List Mode and Mask Mode. The current ATF Mask register can be configured as either a mask mode or a list mode through the ATFMn.mask bit.

(1) Mask Mode: ATFM is used as the mask register of ATF, and RKCAN provides five sets of configurable ‘filter-mask’ registers.

(2) List Mode: ATFM is used as the filter register, and RKCAN provides ten configurable ‘filter’ registers."

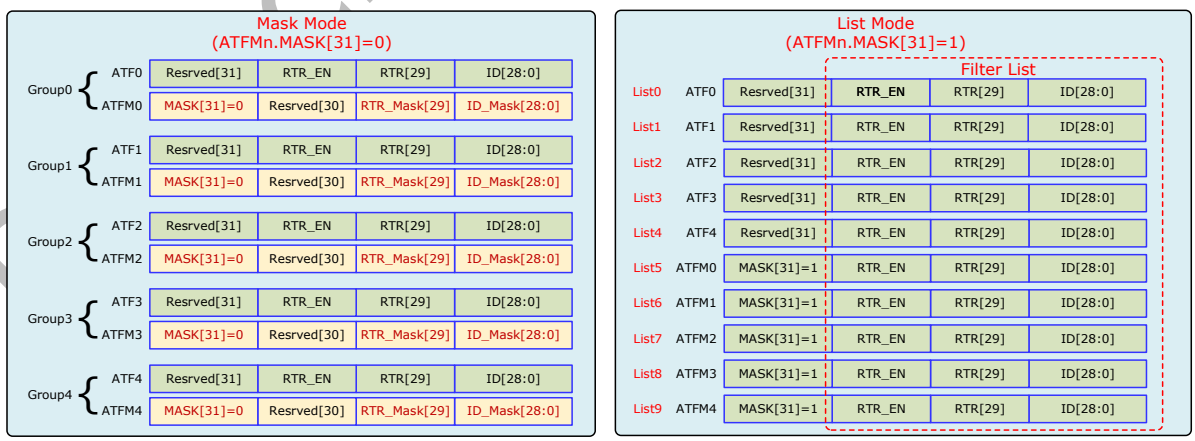

Fig. 35-2 ATF Mode

When filtering based on DLC, there are also two modes: Over Mode and Less Mode. The ATF_DLC.en bit is used to enable the DLC filter, the ARF_DLC.mode bit is used to select between the two modes, and the ATF_DLC.dlc[3:0] is used to configure the filter threshold.

(1) Over Mode: When ARF_DLC.mode is 0, if the dlc value of the received CAN frame is greater than or equal to ATF_DLC.dlc[3:0], the CAN frame can be received by RKCAN and

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stored in memory.

(2) Less Mode: When ARF_DLC.mode is 1, if the dlc value of the received CAN frame is less than or equal to ATF_DLC.dlc[3:0], the CAN frame can be received by RKCAN and stored in memory.

ATF_CTL[9:0] is used to control the switch status of ATF0~4 and ATFM0~4.

35.2.3 BIT TIMING

35.2.3.1 Bit Timing Logic

The CAN FD protocol defines two bit rates, the first for the ARBITRATION-PHASE with a longer bit time and the second for the data phase with the same or with a shorter bit time. The definition for the first bit rate is the same as for the NOMINAL BIT RATE and the NOMINAL BIT TIME in the CAN protocol specification. The definition for the second bit rate, the DATA BIT RATE WITH the DATA BIT TIME, requires a separate configuration register set.

The bit timing logic controls the sampling point position through the buffer bits in the timing register to ensure the accuracy of the data sampling. The bit timing logic receives the clock frequency division signal for identification, sets the bus timing parameters, establishes synchronization parameters, and adjusts the bus transmission rate. At the same time, the bus is monitored and the message to be sent is transmitted to the bus at the set timing.

According to the provisions of the CAN protocol: the CAN bus is always at a high level when no message is sent, and the continuous recessive bit is monitored on the bus. At this time, the bus is in an idle state, and the arbitration priority is low, ready to receive data at any time. When the bus detects a transition from a recessive bit to a dominant bit, it is proved that the frame start bit starts transmitting, and the bus performs a hard synchronization in the bit start sync segment. Then, in the process of receiving the message, once the edge of the transition close to the sampling point is detected and the edge of the edge and the synchronization segment have a phase error lower than the synchronization width (SJW is taken when the value exceeds SJW), the controller executes once resynchronization, resynchronization can be performed multiple times during one data transmission.

35.2.3.2 Bit Timing Definition

The transmission time of each bit is divided into 4 parts:

$$t_{nbt} = t_{sync_seg} + t_{prop_seg} + t_{phase_seg1} + t_{phase_seg2}$$

t_{sync_seg}, t_{prop_seg}, t_{phase_seg1} and t_{phase_seg2} are integer multiples of the unit time(t_{sclk}), and this unit time is a specific multiple of the system clock, which is determined by the division factor BRP in the bus timing register: 1. The counter is obtained by the BRP operation; 2. The system clock clk is counted by the counter; 3. When the limit is reached, a clock with a period of t_{sclk} is generated.

In the system design, considering the cyclical occurrence of each time period, a state machine with three states is used in the bit timing design. The three states correspond to the sync segment(sync_seg) and the phase buffer segment 1 (phase_seg1=phase_seg1+prog_seg) and the phase buffer segment 2 (phase_seg2), respectively. Where PHASE_SEG1 range: 1~16; PHASE_SEG2 range: 1~8; BRP range: 1~64.

$$t_{sync_seg} = 1 \times t_{sclk}$$

$$t_{prop_seg} + t_{phase_seg1} = t_{sclk} \times (8 \times TSEG1.3 + 4 \times TSEG1.2 + 2 \times TSEG1.1 + TSEG1.0 + 1)$$

$$t_{phase_seg2} = t_{sclk} \times (4 \times TSEG2.2 + 2 \times TSEG2.1 + TSEG1.0 + 1)$$

Define a counter to count t_{sclk}. When the count reaches the TSEG1, TSEG2 defined in the bus timing register and the length of the synchronization segment defined in the design, the system will generate the corresponding transition conditions: go_seg1, go_seg2, go_sync.

By judging these transition conditions, the control state machine cycles through the above three states.

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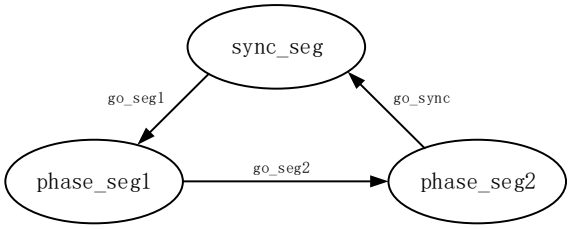

Fig. 35-3 Bit timing FSM

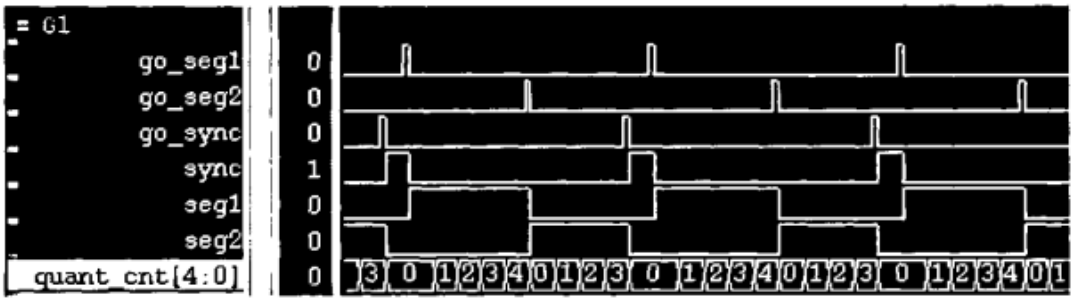

Fig. 35-4 Bit timing waveform diagram

35.2.3.3 Bit time transition

The first part of a CAN FD frame, until the BRS bit, is transmitted with the NOMINAL BIT RATE. The bit rate is switched if the BRS bit is recessive, until the CRC DELIMITER is reached or until the CAN FD controller sees an error condition that results in the starting of an ERROR FRAME. CAN FD ERROR FRAMES, as well as ACK FIELD, END OF FRAME, OVERLOAD FRAMES, and all frames in CAN format are transmitted with the NOMINAL BIT RATE.

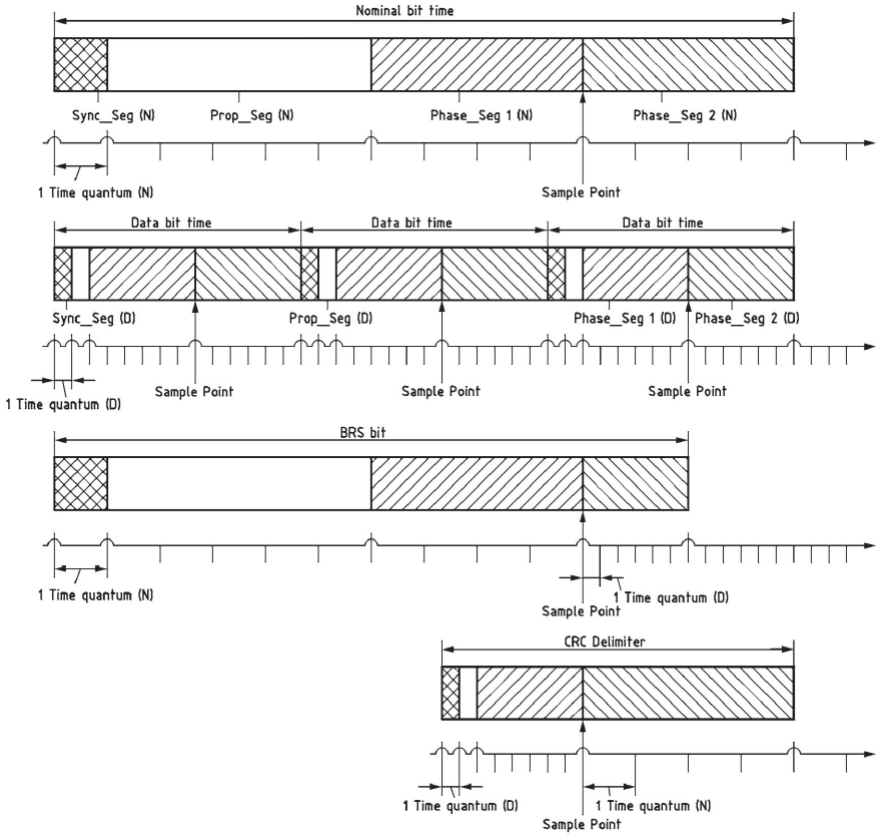

Fig. 35-5 Bit Timing

35.2.3.4 Sampling Point and Sending Point

Sampling Point: According to the agreement, the sample point sample_point should be between phase_seg1 and phase_seg2. It is designed to be in the position of phase_seg2 synchronization. The sampling pulse width is defined as one system clock cycle.
Considering the accuracy of sampling, you can use the method of taking three samples to

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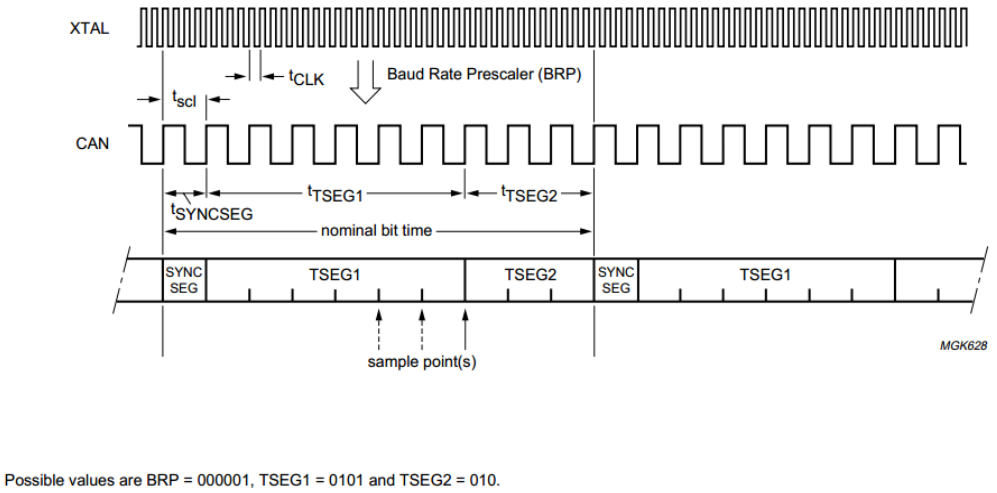
take the mean. The interval between each sample point is one t_{sclk}.



Possible values are BRP = 000001, TSEG1 = 0101 and TSEG2 = 010.

Fig. 35-6 Three sampling diagram

Sending Point: The location of the transmission point(tx_point) should be at the beginning of each bit time according to the protocol, and it is designed to synchronize it with the go_sync signal. In addition, if it is in sync or resynchronize, tx_point will be valid immediately.

35.2.3.5 Bit Synchronization

With the synchronization method, one or more nodes that satisfy the synchronization condition align their synchronization segments with the transmission data on the bus at a specific time. Synchronization occurs on the 1-to-0 transition edge in order to control the distance from the transition edge to the sample point. Two synchronization methods are defined in the CAN bus communication protocol: hard synchronization and resynchronization.

Hard_sync: All nodes must be synchronized to the leading edge of the starting frame of the node that first started transmitting the message. At the beginning of each frame of data, a synchronization action is taken between the nodes.

Hard synchronization implementation method: determine whether the bus state meets the frame start condition specified in the protocol, and the node is not in the state of the data to be transmitted. At this time, a hard synchronization flag signal hard_sync is generated, and the pulse width is a system clock; The hard_sync entry is added to the control condition of the go_seg1 signal, and go_seg1 is valid immediately when the hard_sync signal is '1'. Therefore, once the hard synchronization condition is met, the system enters the phase_seg1 segment, thereby achieving synchronization.

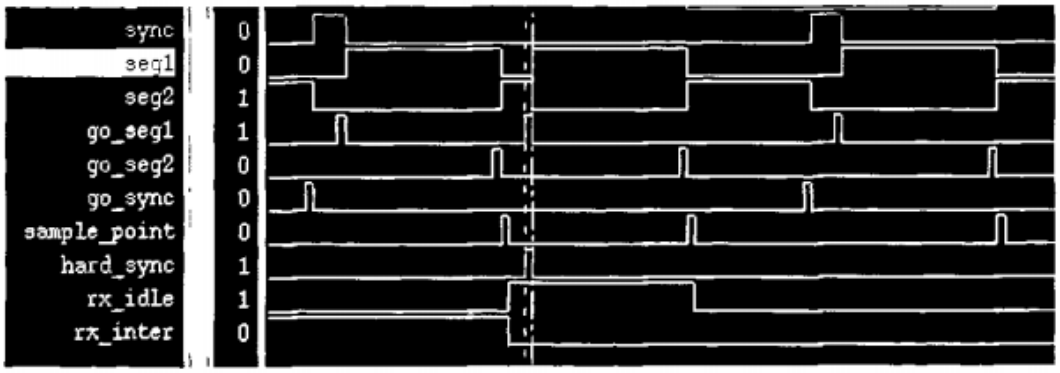


Fig. 35-7 Hard_sync waveform diagram

Resynchronization: In addition to generating hard synchronization at the beginning of each frame of data, the CAN bus communication protocol also specifies the transmission of data for each frame. When the timing coordination between the nodes is not ideal, it will be resynchronized, so that the cooperation between the nodes is in a good state.

For the receiver, the bus changes it received should occur in the sync segment. Once the

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receiver's status violates this rule, the receiver will perform a resynchronization.
Two situations that require resynchronization:

1. The jump of the bus value '1' to '0' occurs between the sync segment and the sample point, which is a delay jump;
2. The jump of the bus value '1' to '0' occurs between the sample point and the sync segment, which is an early jump.

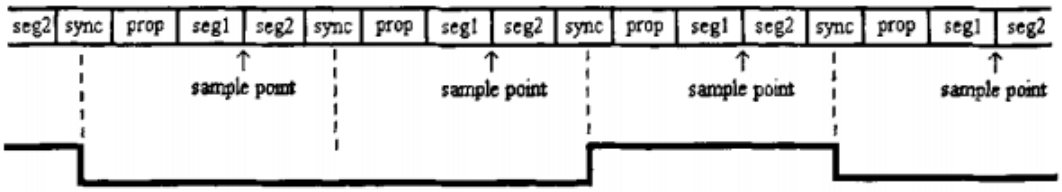

Fig. 35-8 Resynchronization

Resynchronization method:

1. Condition for resynchronization: the receiver is in a mode of receiving data (not inter-frame space or bus idle), and a resynchronization flag signal 'resync' is generated when a jump of the bus value '1' to '0' occurs;
2. According to the position of the resynchronization flag signal, it is determined that the abnormal jump is a delay jump or an early jump;
3. Counting the delay or the length of the advance by the counter;
4. In this bit, phase_seg1 is added with a delay time or phase_seg2 is subtracted from the advance time to obtain a new phase buffer time for the bit, thereby achieving synchronization.

35.2.3.6 Transmitter Delay Compensation

During the data phase of a CAN FD transmission, only one node is transmitting; all others are receiving. Therefore, the propagation delay does not limit the maximum data rate. When transmitting via pin, TXCAN, the CAN FD Controller module receives the transmitted data from its local CAN transceiver via pin, RXCAN. The received data are delayed by the CAN
transceiver's loop delay. In case this delay is greater than 1 + DTSEG1, a bit error will be detected.
In order to enable a data phase bit time that is shorter than the transceiver loop delay, the Transmitter Delay Compensation (TDC) is implemented. Instead of sampling after DTSEG1, a
Secondary Sample Point (SSP) is calculated and used for sampling during the data phase of a
CAN FD message.

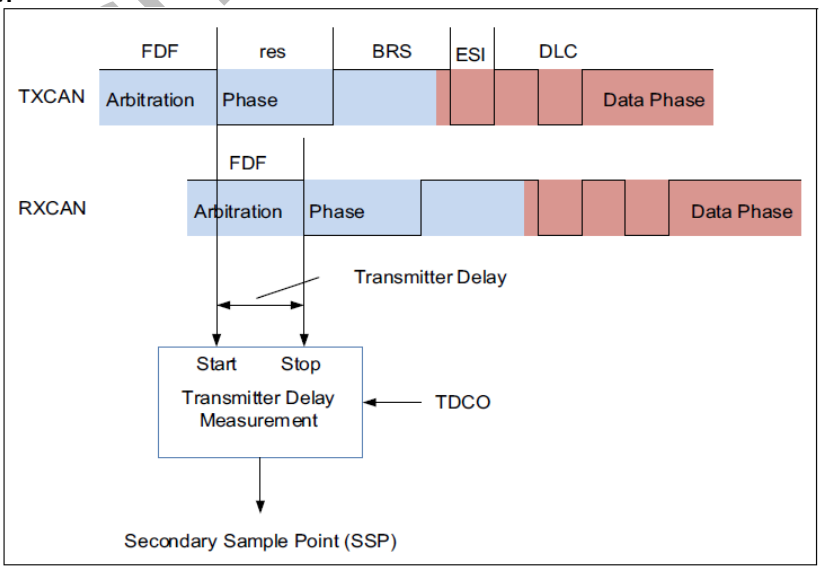

Fig. 35-9 Measurement of Transceiver Delay

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35.2.4 RXSTORE

35.2.4.1 Internal Storage Mode

To store the frame data received by RKCAN only in the internal SRAM, the STR_CTL.stm needs to be configured as 0. The frame data received by RKCAN will only be stored in the internal SRAM. The size of the internal SRAM is 256x32bit. The CPU can query the remaining amount of data in the internal SRAM through the STR_STAT.intm_left_cnt register. After the CPU reads the data, the STR_STAT.intm_left_cnt will decrease accordingly. At the same time, the way the internal SRAM stores data can be divided into four data storage formats: Flexible, CAN Fixed, CANFD Fixed, and Mixed. Use STR_CTL_ism_sel[1:0] to select among the four formats, the specific explanations are as follows:

(1) Flexible: The data of each frame is seamlessly stored in the SRAM according to its volume.

(2) CAN Fixed: A fixed 4 words are used to store a frame of data.

(3) CANFD Fixed: A fixed 18 words are used to store a frame of data.

(4) Mixed: CAN frames use 4 words to store a frame of data, and CANFD frames use 18 words to store a frame of data. It should be noted that when the external storage mode is turned on, the internal SRAM will still be used for data caching, and the STR_CTL_ism_sel[1:0] can still be used to select the format of the data cached in the internal SRAM, but the external memory uses a fixed 18 words to store a frame of data.

35.2.4.2 External Storage Mode

To store the frame data received by RKCAN in external memory (DDR or System Memory), the STORE_CTL.stm needs to be configured as 1, and registers such as TXTHR, START_ADDR, and EXTM_SIZE need to be configured. RKCAN will first store the received frame data in the internal SRAM. When the amount of data received by RKCAN exceeds the threshold set by TXTHR, it will automatically write the data stored in the internal SRAM to the external memory through AHB Master, and update the WADDR register to the tail address of the part of the external memory that has been written with data. At the same time, it updates the status of the two empty/full flags STR_STAT.extm_empty and STR_STAT.extm_full. RKCAN sends an interrupt to the CPU. The CPU can determine the amount of data that can be read by querying the value of the WADDR register. After the CPU completes the frame data reading, it needs to write the latest CPU_RD_ADDR value into the RADDR register of RKCAN. RKCAN will calculate the empty/full status of the memory based on the values of the RADDR and WADDR registers. The CPU can query the amount of data in the external memory through STR_STAT.extm_left_cnt, and query the remaining amount of data in the internal SRAM through STR_STAT.intm_left_cnt.
This feature is currently only used for debugging. For specific application details, please consult Rockchip.

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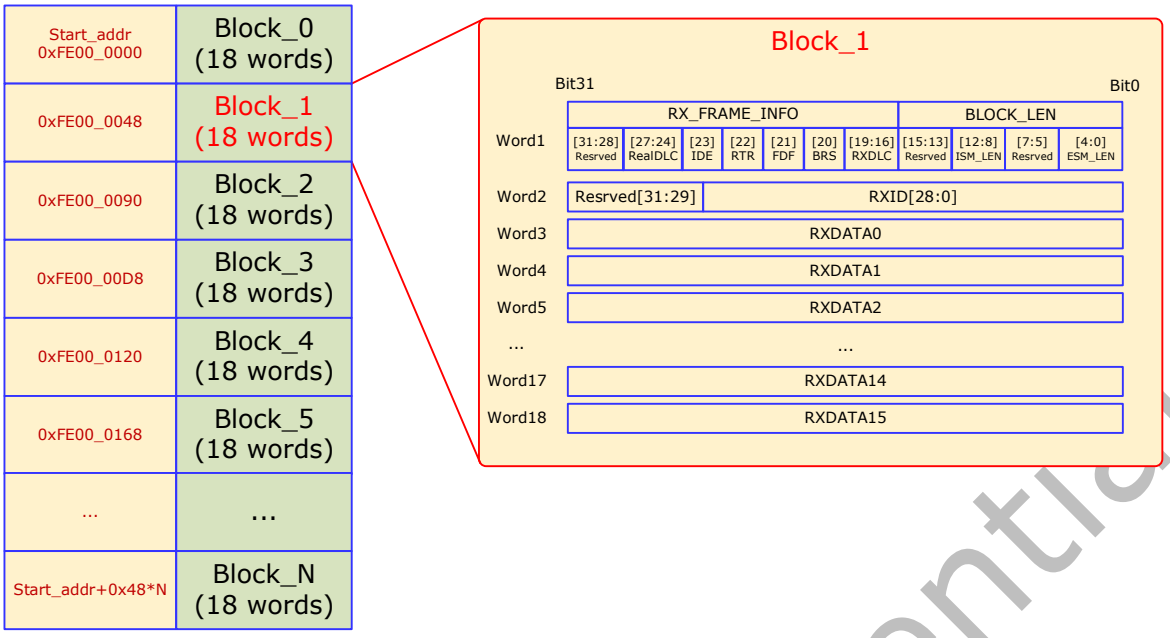

Fig. 35-10 Data storage format under external storage mode

35.2.4.3 ESM Timeout Mechanism

RKCAN also has a timeout mechanism to prevent the RKCAN receive buffer from overflowing when the CPU does not read data for a long time. The timeout threshold is configured through the BUF_TIMEOUT register. In internal storage mode, if the CPU does not read the data in the internal SRAM for a long time, a timeout interrupt will occur; in external storage mode, if the CPU does not update the value of the CPU_RD_ADDR register for a long time, a timeout interrupt will occur. The same interrupt flag is used in both modes.

35.2.5 ERROR PROCESS

There are five types of errors. Multiple errors can occur at the same time.

- **BIT ERROR**:
  A unit that is sending a bit on the bus also monitors the bus. A BIT ERROR has to be detected at that bit time, when the bit value that is monitored is different form the bit value that is sent. An exception is the sending of a 'recessive' bit during the stuffed bit stream of the ARBITRATION FIELD of during the ACK SLOT. Then no BIT ERROR occurs when a 'dominant' bit is monitored. A TRANSMITTER sending a PASSIVE ERROR FLAG and detecting a 'dominant' bit does not interpret this as a BIT ERROR.
- **BIT STUFF ERROR**:
  A STUFF ERROR has to be detected at the bit time of the 6^{th} consecutive equal bit level in a message field that should be coded by the method of bit stuffing.
- **FORM ERROR**:
  A FORM ERROR has to be detected when a fixed-form bit field contains one or more illegal bits. (Exception is the detection of a dominant bit during the last bit of END OF FRAME by a RECEIVER, or the detection of a dominant bit during the last bit of ERROR DELIMITER or OVERLOAD DELIMITER by any node). When the value of a fixed STUFF-BIT in the CAN FD format CRC SEQUENCE is equal to its preceding bit, this shall also be detected as a FORM-ERROR.
- **ACK ERROR**:
  An ACK ERROR has to be detected by a transmitter whenever it does not monitor a 'dominant' bit during the ACK SLOT.
- **CRC ERROR**:
  The CRC sequence consists of the result of the CRC calculation by the transmitter. The receivers calculate the CRC in the same way as the transmitter. A CRC ERROR has to be detected, if the calculated result is not the same as that received in the CRC sequence.

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35.3 Register Description

35.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows. address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
CAN0	0x2AC00000
CAN1	0x2AC10000

35.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKCAN_MODE	0x0000	W	0x00000000	Mode Configure Register
RKCAN_CMD	0x0004	W	0x00000000	Request Command Register
RKCAN_STATE	0x0008	W	0x00000000	Controller State Register
RKCAN_INT	0x000C	W	0x00000000	Interrupt State Register
RKCAN_INT_MASK	0x0010	W	0x00000000	Interrupt Mask Registers
RKCAN_FD_NOMINAL_BIT_TIMING	0x0100	W	0x00000000	CANFD Nominal Bit Timing Configure Register
RKCAN_FD_DATA_BITTIMING	0x0104	W	0x00000000	CANFD Data Bit Timing Configure Register
RKCAN_FD_TDC	0x0108	W	0x00000000	Transmitter Delay Compensation Configure Register
RKCAN_FD_BRS_CFG	0x010C	W	0x0000000B	Transmitter Delay Compensation Configure Register
RKCAN_FD_LOOP_CNT	0x0110	W	0x00000000	Transmitter Delay Compensation Configure Register
RKCAN_DMA_CTRL	0x011C	W	0x00000000	DMA Mode Control Register
RKCAN_FD_TXFRAMEINFO	0x0200	W	0x00000000	CANFD TX Frame Information Configuration Register
RKCAN_FD_TXID	0x0204	W	0x00000000	CANFD Transmit ID Register
RKCAN_FD_TXDATA0	0x0208	W	0x00000000	CANFD Transmit DATA0
RKCAN_FD_TXDATA1	0x020C	W	0x00000000	CANFD Transmit DATA1
RKCAN_FD_TXDATA2	0x0210	W	0x00000000	CANFD Transmit DATA2
RKCAN_FD_TXDATA3	0x0214	W	0x00000000	CANFD Transmit DATA3
RKCAN_FD_TXDATA4	0x0218	W	0x00000000	CANFD Transmit DATA4
RKCAN_FD_TXDATA5	0x021C	W	0x00000000	CANFD Transmit DATA5
RKCAN_FD_TXDATA6	0x0220	W	0x00000000	CANFD Transmit DATA6
RKCAN_FD_TXDATA7	0x0224	W	0x00000000	CANFD Transmit DATA7
RKCAN_FD_TXDATA8	0x0228	W	0x00000000	CANFD Transmit DATA8
RKCAN_FD_TXDATA9	0x022C	W	0x00000000	CANFD Transmit DATA9
RKCAN_FD_TXDATA10	0x0230	W	0x00000000	CANFD Transmit DATA10
RKCAN_FD_TXDATA11	0x0234	W	0x00000000	CANFD Transmit DATA11
RKCAN_FD_TXDATA12	0x0238	W	0x00000000	CANFD Transmit DATA12
RKCAN_FD_TXDATA13	0x023C	W	0x00000000	CANFD Transmit DATA13
RKCAN_FD_TXDATA14	0x0240	W	0x00000000	CANFD Transmit DATA14
RKCAN_FD_TXDATA15	0x0244	W	0x00000000	CANFD Transmit DATA15
RKCAN_FD_RXFRAMEINFO	0x0300	W	0x00000000	CANFD RX Frame Information Configuration Register
RKCAN_FD_RXID	0x0304	W	0x00000000	CANFD Receive ID
RKCAN_FD_RXTIMESTAMP	0x0308	W	0x00000000	CANFD Receive Timestamp Reserved

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Name	Offset	Size	Reset Value	Description
RKCAN_FD_RXDATA0	0x030C	W	0x00000000	CANFD Receive Data Reg0
RKCAN_FD_RXDATA1	0x0310	W	0x00000000	CANFD Receive Data Reg1
RKCAN_FD_RXDATA2	0x0314	W	0x00000000	CANFD Receive Data Reg2
RKCAN_FD_RXDATA3	0x0318	W	0x00000000	CANFD Receive Data Reg3
RKCAN_FD_RXDATA4	0x031C	W	0x00000000	CANFD Receive Data Reg4
RKCAN_FD_RXDATA5	0x0320	W	0x00000000	CANFD Receive Data Reg5
RKCAN_FD_RXDATA6	0x0324	W	0x00000000	CANFD Receive Data Reg6
RKCAN_FD_RXDATA7	0x0328	W	0x00000000	CANFD Receive Data Reg7
RKCAN_FD_RXDATA8	0x032C	W	0x00000000	CANFD Receive Data Reg8
RKCAN_FD_RXDATA9	0x0330	W	0x00000000	CANFD Receive Data Reg9
RKCAN_FD_RXDATA10	0x0334	W	0x00000000	CANFD Receive Data Reg10
RKCAN_FD_RXDATA11	0x0338	W	0x00000000	CANFD Receive Data Reg11
RKCAN_FD_RXDATA12	0x033C	W	0x00000000	CANFD Receive Data Reg12
RKCAN_FD_RXDATA13	0x0340	W	0x00000000	CANFD Receive Data Reg13
RKCAN_FD_RXDATA14	0x0344	W	0x00000000	CANFD Receive Data Reg14
RKCAN_FD_RXDATA15	0x0348	W	0x00000000	CANFD Receive Data Reg15
RKCAN_RX_STR_RDATA	0x0400	W	0x00000000	RX Storage Read Data
RKCAN_STR_CTL	0x0600	W	0x00000080	Storage Ctrl Register
RKCAN_STR_STATE	0x0604	W	0x00000000	Storage Ctrl Register
RKCAN_STR_TIMEOUT	0x0608	W	0x00002710	Storage Timeout Threshold Register
RKCAN_STR_WTM	0x060C	W	0x000168ED	Storage Water Mark Register
RKCAN_EXTM_START_ADDR	0x0610	W	0x00000000	External Memory Start Address
RKCAN_EXTM_SIZE	0x0614	W	0x000001F8	External Memory Size Register
RKCAN_EXTM_WADDR	0x0618	W	0x00000000	External Memory AHB Write Address
RKCAN_EXTM_RADDR	0x061C	W	0x00000000	External Memory Soft Read Address
RKCAN_EXTM_AHB_TXTHR	0x0620	W	0x00000000	AHB Master Transmit Threshold Level
RKCAN_EXTM_LEFT_CNT	0x0624	W	0x00000000	External Memory Left Counter
RKCAN_ATF0	0x0700	W	0x00000000	Acceptance Filter 0 Code Register
RKCAN_ATF1	0x0704	W	0x00000000	Acceptance Filter 1 Code Register
RKCAN_ATF2	0x0708	W	0x00000000	Acceptance Filter 2 Code Register
RKCAN_ATF3	0x070C	W	0x00000000	Acceptance Filter 3 Code Register
RKCAN_ATF4	0x0710	W	0x00000000	Acceptance Filter 4 Code Register
RKCAN_ATFM0	0x0714	W	0x1FFFFFFF	Acceptance Filter 0 Mask Register
RKCAN_ATFM1	0x0718	W	0x1FFFFFFF	Acceptance Filter 1 Mask Register
RKCAN_ATFM2	0x071C	W	0x1FFFFFFF	Acceptance Filter 2 Mask Register
RKCAN_ATFM3	0x0720	W	0x1FFFFFFF	Acceptance Filter 3 Mask Register
RKCAN_ATFM4	0x0724	W	0x1FFFFFFF	Acceptance Filter 4 Mask Register
RKCAN_ATF_DLC	0x0728	W	0x00000000	Acceptance DLC Filter Function
RKCAN_ATF_CTL	0x072C	W	0x00000000	Acceptance Filter Configure Register
RKCAN_AUTO_RETX_CFG	0x0808	W	0x00000320	Configure Register for Auto Retransmission Function
RKCAN_AUTO_RETX_STATE0	0x080C	W	0x00000000	Auto Retransmission Status Register 0
RKCAN_AUTO_RETX_STATE1	0x0810	W	0x00000000	Auto Retransmission Status Register 0
RKCAN_OLF_CFG	0x0814	W	0x00000000	Overload Frame Configuration Register

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Name	Offset	Size	Reset Value	Description
RKCAN_RXINT_CTRL	0x0818	W	0x00000100	Multi Frame Interrupt(MFI) Configure Register
RKCAN_RXINT_TIMEOUT	0x081C	W	0x0000FFFF	MFI Timeout Threshold Register
RKCAN_ERROR_CODE	0x0900	W	0x00000000	RX Error Code Register
RKCAN_ERROR_MASK	0x0904	W	0x00000000	Error Mask Register
RKCAN_RXERRORCNT	0x0910	W	0x00000000	Receive Error Counter Register
RKCAN_TXERRORCNT	0x0914	W	0x00000000	Transmit Error Counter Register
RKCAN_ARBIT_FAIL_STATE	0x0918	W	0x00000000	Arbiter Fail Code Register
RKCAN_RTL_VERSION	0x0F0C	W	0xCFDBA0EB	CAN RTL version

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

35.3.3 Detail Registers Description

RKCAN_MODE

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	noack_mode When noack_mode is enabled, if the internal receive buffer of RKCAN is full and a new frame is received, RKCAN will no longer respond with an ACK. 1'b0: Disable 1'b1: Enable
14	RW	0x0	force_passive_err Force RKCAN into error passive station 1'b0: Disable 1'b1: Enable
13	RW	0x0	force_active_err Force RKCAN into error active station 1'b0: Disable 1'b1: Enable
12	RW	0x0	crcerr_pass_mode 1'b0: Send Passive Error when CRC Error detected 1'b1: Not send Passive Error when CRC Error detected
11	RW	0x0	crcerr_ack_mode 1'b0: Not send ACK when CRC Error detected 1'b1: Send ACK when CRC Error detected
10	RW	0x0	pass_err_mode 1'b0: PASSIVE Error Flag use recessive bits 1'b1: PASSIVE Error Flag use dominant bits
9	RW	0x0	dis_pee Disable Protocol Exception Event Detection/Generation 1'b0: PEE detection/generation is enabled. If the CANFD receiver detects the res bit as 1, it goes to Bus Integration state (PEE_config) and waits for Bus Idle condition (11 consecutive nominal recessive bits). The error counter remains unchanged. 1'b1: Disable Protocol Exception Event detection/generation by CANFD receiver if "res" bit in CANFD frame is detected as 1. In this case, CANFD receiver generates Form error.

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Bit	Attr	Reset Value	Description
8	RW	0x0	rett_mode Restricted Operation Mode In Restricted Operation Mode, RKCAN is able to transmit and to receive DATA FRAMES and REMOTE FRAMES and it gives ACKNOWLEDGE to valid frames, but it does not send ACTIVE ERROR FRAMES or OVERLOAD FRAMES. The error counters are not incremented or decremented. 1'b0: Disable 1'b1: Enable
7	RW	0x0	auto_bus_on Auto Bus On Enable 1'b0: After the RKCAN has entered bus_off state, the software can start a bus_off_recovery sequence by resetting the work_mode to 0. 1'b1: Automatic reset TEC/REC to bus_on after 128 occurrence of 11 consecutive recessive bits have been monitored on the bus.
6	RO	0x0	reserved
5	RW	0x0	rxstx_mode Receive Self Transmit data mode 1'b0: Disable 1'b1: Enable. When the RKCAN sends data, it can also receive the data sent by itself.
4	RW	0x0	lback_mode Loopback Mode 1'b0: Disable 1'b1: Enable
3	RW	0x0	silent_mode Silent Mode 1'b0: Disable 1'b1: Enable
2	RW	0x0	self_test Reserved Self check ACK slot when TX frame Using ERROR_MASK[4]can achieve the same function When in self_test mode, the receiver does not need to return an ACK signal when receiving data. Therefore, no error ack will occur in self_test mode. When in 'lback_mode' or 'silent_mode', it needs to enable 'self_test' mode when sending frame.
1	RW	0x0	sleep_mode Sleep Mode This is the Sleep mode request bit 1'b0: No such request 1'b1: Request core to be in Sleep mode This bit is cleared when the core wakes up from Sleep mode.
0	RW	0x0	work_mode Work Mode 1'b0: Idle mode, CAN stop transmit and registers can be configured 1'b1: Work mode, CAN enter the working mode, Receive/transmit data

RKCAN_CMD

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	R/WSC	0x0	tx1_req Transmit request enable 1'b0: Disable 1'b1: Enable When 'tx1_req' is enable, the RKCAN buffer1 is in the transmit mode and cannot receive frames from other CANs. When the RKCAN buffer1 transmission frame complete, 'tx1_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.
0	R/WSC	0x0	tx0_req Transmit request enable 1'b0: Disable 1'b1: Enable When 'tx0_req' is enable, the RKCAN buffer0 is in the transmit mode and cannot receive frames from other CANs. When the RKCAN buffer0 transmission frame complete, 'tx0_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.

RKCAN_STATE

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	sleep_state Sleep state 1'b0: None 1'b1: CAN controller is in the sleep state
4	RO	0x0	bus_off_state Bus off state 1'b0: None 1'b1: Bus off state: When the error counter is incremented to 255, the CAN controller will enter the bus off state, generate an error warning interrupt and enter reset mode, waiting for the CPU to restart. (rx/tx_err_cnt >=32'd255)
3	RO	0x0	error_warning_state Error warning state 1'b0: None 1'b1: Error state: At least one error counter has reached the error warning threshold (rx/tx_err_cnt >=32'd96)
2	RO	0x0	tx_period Transmit state 1'b0: Not in transmit state 1'b1: CAN controller is in the transmit state
1	RO	0x0	rx_period Receive state 1'b0: Not in receive state 1'b1: CAN controller is in the receive state
0	RO	0x0	tx_buffer_full Transmit buffer full flag bit 1'b0: Not full 1'b1: TX buffer is full. There is data in buffer waiting to be sent or being sent.

RKCAN_INT

Address: **Operational Base** + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	W1C	0x0	busoff_rcy_int BusOff Timer Recovery Interrupt 1'b0: None 1'b1: BusOff timer recovery Write 1 then clear
18	W1C	0x0	esm_wtm_int External Stotage watermark Interrupt 1'b0: None 1'b1: The data in external storage reaches the watermark Write 1 then clear
17	W1C	0x0	ism_wtm_int Internal Stotage watermark Interrupt 1'b0: None 1'b1: The data in internal storage reaches the watermark Write 1 then clear
16	W1C	0x0	busint_int Enter Bus Integration Interrupt 1'b0: None 1'b1: Indicates RKCAN enter the bus integration state. Write 1 then clear
15	W1C	0x0	rxstr_timeout_int RX Storage Timeout Interrupt 1'b0: None 1'b1: Indicates that data remain in rx storage timeout. Write 1 then clear
14	W1C	0x0	mfi_timeout_int Multi Frame Interrupt(MFI) Mode Timeout Interrupt
13	W1C	0x0	mfi_int Multi Frame Interrupt(MFI)
12	W1C	0x0	auto_retx_fail_int Automatic Transmit Failure Interrupt
11	W1C	0x0	wakeup_int Wakeup Interrupt 1'b0: None 1'b1: Indicates that the core entered Normal mode from Sleep mode. Write 1 then clear
10	W1C	0x0	bus_off_recovery_int Bus off Recover Interrupt 1'b0: None 1'b1: Indicates that the core is recovered from Bus-off mode Write 1 then clear
9	W1C	0x0	bus_off_int Bus Off Interrupt 1'b0: None 1'b1: Indicates that the CAN core entered Bus-off mode Write 1 then clear
8	W1C	0x0	rxstr_overflow_int RX Storage Overflow Interrupt. 1'b0: None 1'b1: Indicates that a message has been lost. This condition occurs when a new message with ID matching to Receive Storage is received and the Receive Storage is full. Write 1 then clear

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Bit	Attr	Reset Value	Description
7	W1C	0x0	rxstr_full_int RX Storage full Interrupt. 1'b0: None 1'b1: Indicates that RX Storage is full based on watermark setting Write 1 then clear
6	W1C	0x0	error_int Bus Error Interrupt 1'b0: None 1'b1: CAN bus error interrupt. This interrupt is generated when a bus error is detected. Error details can refer to the ERROR_CODE register. Write 1 then clear
5	W1C	0x0	tx_arbit_fail_int Transmit Arbitration loss Interrupt 1'b0: None 1'b1: Arbitration loss interrupt. This interrupt is generated when the loss of arbitration is turned into a receiver Write 1 then clear
4	W1C	0x0	passive_error_int Passive Error Interrupt 1'b0: None 1'b1: Passive error interrupt. This interrupt is generated when the controller enters an error passive state (at least one error counter reaches 127) or returns from the error passive state to the error active state. Write 1 then clear
3	W1C	0x0	overload_int Overload Frame Interrupt 1'b0: None 1'b1: CAN bus overload interrupt. This interrupt is generated when a overload frame is generated. Write 1 then clear
2	W1C	0x0	error_warning_int Error warning interrupt 1'b0: None 1'b1: Error_warning_int. This interrupt is generated when the error_warning_state bits change. Write 1 then clear
1	W1C	0x0	tx_finish_int Transmit finish interrupt 1'b0: None 1'b1: Transmit finish interrupt. CAN controller sends the message. Write 1 then clear
0	W1C	0x0	rx_finish_int Receive Finish Interrupt 1'b0: None 1'b1: Receive finish int. CAN controller has received the message and the rx_buffer is full. Write 1 then clear

RKCAN_INT_MASK

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19	RW	0x0	busoff_rcy_int_mask 1'b0: Unmasked 1'b1: Masked
18	RW	0x0	esm_wtm_int_mask 1'b0: Unmasked 1'b1: Masked
17	RW	0x0	ism_wtm_int_mask 1'b0: Unmasked 1'b1: Masked
16	RW	0x0	busint_int_mask 1'b0: Unmasked 1'b1: Masked
15	RW	0x0	rxstr_timeout_int_mask 1'b0: Unmasked 1'b1: Masked
14	RW	0x0	mfi_timeout_int_mask 1'b0: Unmasked 1'b1: Masked
13	RW	0x0	mfi_int_mask 1'b0: Unmasked 1'b1: Masked
12	RW	0x0	auto_retx_fail_int_mask 1'b0: Unmasked 1'b1: Masked
11	RW	0x0	wakeup_int_mask 1'b0: Unmasked 1'b1: Masked
10	RW	0x0	bus_off_recovery_int_mask 1'b0: Unmasked 1'b1: Masked
9	RW	0x0	bus_off_int_mask 1'b0: Unmasked 1'b1: Masked
8	RW	0x0	rxstr_overflow_int_mask 1'b0: Unmasked 1'b1: Masked
7	RW	0x0	rxstr_full_int_mask 1'b0: Unmasked 1'b1: Masked
6	RW	0x0	error_int_mask 1'b0: Unmasked 1'b1: Masked
5	RW	0x0	tx_arbit_fail_int_mask 1'b0: Unmasked 1'b1: Masked
4	RW	0x0	passive_error_int_mask 1'b0: Unmasked 1'b1: Masked
3	RW	0x0	overload_int_mask 1'b0: Unmasked 1'b1: Masked
2	RW	0x0	error_warning_int_mask 1'b0: Unmasked 1'b1: Masked

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Bit	Attr	Reset Value	Description
1	RW	0x0	tx_finish_int_mask 1'b0: Unmasked 1'b1: Masked
0	RW	0x0	rx_finish_int_mask 1'b0: Unmasked 1'b1: Masked

RKCAN_FD_NOMINAL_BITTIMING

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	sample_mode RKCAN controller sampling mode configuration register. When enabling triple sampling, it is necessary to configure the positions of two additional sampling points using the FD_BRS_CFG[30:5] register. 1'b0: Single sample mode 1'b1: Three sample mode
30:24	RW	0x00	sjw SJW: Resynchronization Jump Width Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error.
23:16	RW	0x00	brq brp: system prescale coefficient Tsclk = 2 x Tclk x (brp + 1)
15	RO	0x0	reserved
14:8	RW	0x00	tseg2 Phase buffer segment 2 Tphase_seg2 = Tsclk x (tseg2 + 1)
7:0	RW	0x00	tseg1 Phase buffer segment 1 Tphase_seg1 = Tsclk x (tseg1 + 1)

RKCAN_FD_DATA_BITTIMING

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	brs_tseg1 tseg1 for BRS Bit
23	RW	0x0	brs_mode BRS bit sampling point setting 1'b0: Sampling BRS bit according to the position specified in the protocol 1'b1: The sampling point of BRS bit will be advanced
22	RW	0x0	ackslot_sync_dis 1'b0: Enable Hardsync when ACK_SLOT 1'b1: Disable Hardsync when ACK_SLOT
21	RO	0x0	reserved
20:17	RW	0x0	sjw SJW: Resynchronization Jump Width Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error.
16:9	RW	0x00	brq brp: system prescale coefficient Tsclk = 2 x Tclk x (brp + 1)

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Bit	Attr	Reset Value	Description
8:5	RW	0x0	tseg2 Phase buffer segment 2 Tphase_seg2 = Tsclk x (tseg2 + 1)
4:0	RW	0x00	tseg1 Phase buffer segment 1 Tphase_seg1 = Tsclk x (tseg1 + 1)

RKCAN_FD_TDC

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	lcnt_clr Loop Delay Counter Clear
7	RW	0x0	lcnt_meas_en Loop Delay Counter Enable
6:1	RW	0x00	tdc_offset Transmitter Delay Compensation Offset This offset is specified in CAN clock cycles and is added to the measured transmitter delay to place the Secondary Sample Point (SSP) at appropriate position (for example, set this to half data bit time in terms of CAN clock cycles to place SSP in the middle of the data bit).
0	RW	0x0	tdc_enable Transmitter Delay Compensation (TDC) Enable 1'b0: TDC is disabled 1'b1: Enables TDC function as specified in the CAN FD standard

RKCAN_FD_BRS_CFG

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31	RW	0x0	triple_sync_mode ReSync Enable for triple_sample mode.
30:26	RW	0x00	sp2_dtseg2 Sample Point 2 data phase tseg2
25:18	RW	0x00	sp2_ntseg1 Sample Point 2 tseg1
17:13	RW	0x00	sp1_dtseg2 Sample Point 1 data phase tseg2
12:5	RW	0x00	sp1_ntseg1 Sample Point 1 tseg1
4	RO	0x0	reserved
3	RW	0x1	resync_mode Resync Mode. 1'b0: Resynchronization only on the falling edge 1'b1: Resynchronization on both rising and falling edges
2	RO	0x0	reserved
1	RW	0x1	brs_possync_en BRS Bit Posedge Sync Enable
0	RW	0x1	brs_negsync_en BRS Bit negedge Sync Enable

RKCAN_FD_LOOP_CNT

Address: **Operational Base** + offset (0x0110)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	loop_delay_cnt Loop Delay Counter

RKCAN_DMA_CTRL

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	dma_rx_en DMA receive request enable 1'b0: Disable 1'b1: Enable When dma_rx_mode is enable, the RKCAN is in the DMA receive mode. Also, when RKCAN is set work_mode to reset_mode, rx_req is clear.
8:0	RW	0x000	dma_thr DMA transfer start threshold

RKCAN_FD_TXFRAMEINFO

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RW	0x0	tx_rtr 1'b0: Data frame 1'b1: Remote frame
5	RW	0x0	tx_fdf Extended Data Length/FD Frame Format This bit distinguishes between CAN format and CANFD format frames. 1'b0: CAN format frame 1'b1: CAN FD format frame
4	RW	0x0	tx_brs Bit Rate Switch The BRS bit decides whether the bit rate is switched inside a CAN FD format frame or not (provided BRSD bit is not set in MSR register). 1'b0: Bit rate is not switched inside a CAN FD frame. 1'b1: Bit rate is switched from the standard bit rate of the Arbitration phase to the preconfigured alternate bit rate of the Data phase inside a CAN FD frame. Note: BRS does not exist in CAN format frames and should be set to 0.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	txdata_length Transmit data length configure register(unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

RKCAN_FD_TXID

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	tx_id can_tx_id[28:0]

RKCAN_FD_TXDATA0

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data0 tx_data0[31:0]

RKCAN_FD_TXDATA1

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data1 tx_data1[31:0]

RKCAN_FD_TXDATA2

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data2 tx_data2[31:0]

RKCAN_FD_TXDATA3

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data3 tx_data3[31:0]

RKCAN_FD_TXDATA4

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data4 tx_data4[31:0]

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RKCAN_FD_TXDATA5

Address: **Operational Base** + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data5 tx_data5[31:0]

RKCAN_FD_TXDATA6

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data6 tx_data6[31:0]

RKCAN_FD_TXDATA7

Address: **Operational Base** + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data7 tx_data7[31:0]

RKCAN_FD_TXDATA8

Address: **Operational Base** + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data8 tx_data8[31:0]

RKCAN_FD_TXDATA9

Address: **Operational Base** + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data9 tx_data9[31:0]

RKCAN_FD_TXDATA10

Address: **Operational Base** + offset (0x0230)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data10 tx_data10[31:0]

RKCAN_FD_TXDATA11

Address: **Operational Base** + offset (0x0234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data11 tx_data11[31:0]

RKCAN_FD_TXDATA12

Address: **Operational Base** + offset (0x0238)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data12 tx_data12[31:0]

RKCAN_FD_TXDATA13

Address: **Operational Base** + offset (0x023C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data13 tx_data13[31:0]

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RKCAN_FD_TXDATA14

Address: **Operational Base** + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data14 tx_data14[31:0]

RKCAN_FD_TXDATA15

Address: **Operational Base** + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data15 tx_data15[31:0]

RKCAN_FD_RXFRAMEINFO

Address: **Operational Base** + offset (0x0300)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	rxframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RO	0x0	rx_rtr 1'b0: Data frame 1'b1: Remote frame
5	RO	0x0	rx_fdf Extended Data Length/FD Frame Format This bit distinguishes between CAN format and CAN FD format frames. 1'b1: CAN FD format frame 1'b0: CAN format frame
4	RO	0x0	rx_brs Bit Rate Switch The BRS bit decides whether the bit rate is switched inside a CAN FD format frame or not (provided BRSD bit is not set in MSR register). 1'b0: Bit rate is not switched inside a CAN FD frame. 1'b1: Bit rate is switched from the standard bit rate of the Arbitration phase to the preconfigured alternate bit rate of the Data phase inside a CAN FD frame. Note: BRS does not exist in CAN format frames and should be set
3:0	RO	0x0	rxdata_length Transmit data length configure register (unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

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RKCAN_FD_RXID

Address: **Operational Base** + offset (0x0304)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	rx_id can_rx_id[28:0]

RKCAN_FD_RXTIMESTAMP

Address: **Operational Base** + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	timestamp Reserved

RKCAN_FD_RXDATA0

Address: **Operational Base** + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data0 rx_data0[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA1

Address: **Operational Base** + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data1 rx_data1[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA2

Address: **Operational Base** + offset (0x0314)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data2 rx_data2[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA3

Address: **Operational Base** + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data3 rx_data3[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA4

Address: **Operational Base** + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data4 rx_data4[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA5

Address: **Operational Base** + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data5 rx_data5[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA6

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Address: **Operational Base** + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data6 rx_data6[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA7

Address: **Operational Base** + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data7 rx_data7[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA8

Address: **Operational Base** + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data8 rx_data8[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA9

Address: **Operational Base** + offset (0x0330)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data9 rx_data9[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA10

Address: **Operational Base** + offset (0x0334)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data10 rx_data10[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA11

Address: **Operational Base** + offset (0x0338)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data11 rx_data11[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA12

Address: **Operational Base** + offset (0x033C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data12 rx_data12[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA13

Address: **Operational Base** + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data13 rx_data13[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA14

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Address: **Operational Base** + offset (0x0344)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data14 rx_data14[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA15

Address: **Operational Base** + offset (0x0348)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data15 rx_data15[31:0] This register refresh after receiving the next frame

RKCAN_RX_STR_RDATA

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_str_rdata RX strorage read data value

RKCAN_STR_CTL

Address: **Operational Base** + offset (0x0600)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	str_timeout_mode RX storage not read timeout threshold Mode. 1'b0: Disable 1'b1: Enable
7:6	RW	0x2	esm_sel External Storage Mode(ESM) Data Format Select 2'b00: Flexible 2'b01: CAN Fixed 2'b10: CANFD Fixed 2'b11: Mixed
5	RO	0x0	reserved
4	RW	0x0	srst RX Storage Soft Reset Bit 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	ism_sel Internal Storage Mode(ISM) Data Format Select 2'b00: Flexible; cover_mode must disable 2'b01: CAN Fixed 2'b10: CANFD Fixed 2'b11: Mixed. cover_mode must disable
1	RW	0x0	stm Storage Mode 1'b0: Internal Storage Mode 1'b1: External Storage Mode. RKCAN can use AHB Master interface to write the received frame data to External Memory(DDR or System Memory)
0	RW	0x0	buff_mode_en RX Buffer Mode Enable 1'b0: Disable 1'b1: Enable. RKCAN only a set of RXDATA0~15 registers used as buffers to store received data, instead of internal SRAM or external memory.

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RKCAN_STR_STATE

Address: **Operational Base** + offset (0x0604)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:17	RO	0x000	intm_frame_cnt Remaining frame count in RXFIFO. Unit: Frame Only Support when cover_mode disable
16:8	RO	0x000	intm_left_cnt The amount of data remaining in the Internal SRAM. Unit:Word
7:4	RO	0x0	reserved
3	RO	0x0	extm_full External Memory Full Flag 1'b0: Not Full 1'b1: Full
2	RO	0x0	extm_empty External Memory Empty Flag 1'b0: Not Empty 1'b1: Empty
1	RO	0x0	intm_full Internal Memory Full Flag 1'b0: Not Full 1'b1: Full
0	RO	0x0	intm_empty Internal Memory Empty Flag 1'b0: Not Empty 1'b1: Empty

RKCAN_STR_TIMEOUT

Address: **Operational Base** + offset (0x0608)

Bit	Attr	Reset Value	Description
31:0	RW	0x00002710	str_timeout_thr RX storage not read timeout threshold value

RKCAN_STR_WTM

Address: **Operational Base** + offset (0x060C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:9	RW	0x0000b4	esm_watermark External Storage Watermark Register. Unit:Word
8:0	RW	0x0ed	ism_watermark Internal Storage Watermark Register. The configurable range is from 0 to 256. Unit:Word In ISM mode, when the amount of valid data in the RXFIFO is greater than the threshold set by ism_watermark, RKCAN will generate an ism_wtm_int interrupt.

RKCAN_EXTM_START_ADDR

Address: **Operational Base** + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	start_addr External Memory Start Address Used as the Start Address of AHB master output rxdata

RKCAN_EXTM_SIZE

Address: **Operational Base** + offset (0x0614)

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Bit	Attr	Reset Value	Description
31:0	RW	0x000001f8	ext_mem_size Configuration size of external storage space. Unit:Word Must be power of 18

RKCAN_EXTM_WADDR

Address: **Operational Base** + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	can_waddr RKCAN AHB Write Address

RKCAN_EXTM_RADDR

Address: **Operational Base** + offset (0x061C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cpu_raddr CPU Read Address

RKCAN_EXTM_AHB_TXTHR

Address: **Operational Base** + offset (0x0620)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ahb_txthr(V2) When the number of RXFIFO entries is greater than or equal to this value, the RKCAN will automatically transfer the data in the RXFIFO to the external via the AHB Master interface. The value ranges is 0~511.(Unit:byte)

RKCAN_EXTM_LEFT_CNT

Address: **Operational Base** + offset (0x0624)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RO	0x000000	extm_left_cnt The amount of remaining data in external storage.(Unit:Word)

RKCAN_ATF0

Address: **Operational Base** + offset (0x0700)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 0 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATF1

Address: **Operational Base** + offset (0x0704)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 1 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATF2

Address: **Operational Base** + offset (0x0708)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 2 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATF3

Address: **Operational Base** + offset (0x070C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 3 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATF4

Address: **Operational Base** + offset (0x0710)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 4 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

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RKCAN_ATFM0

Address: **Operational Base** + offset (0x0714)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF0M[30:0] is used to configure the mask filed of each rule for ATF0; 1'b1: List Mode, Register ATF0M[30:0] is used as acceptance filter ATF5.
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M0 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM1

Address: **Operational Base** + offset (0x0718)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF1M[30:0] is used to configure the mask filed of each rule for ATF1; 1'b1: List Mode, Register ATF1M[30:0] is used as acceptance filter ATF6;
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M1 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM2

Address: **Operational Base** + offset (0x071C)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF2M[30:0] is used to configure the mask filed of each rule for ATF2; 1'b1: List Mode, Register ATF2M[30:0] is used as acceptance filter ATF7.

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Bit	Attr	Reset Value	Description
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M2 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM3

Address: **Operational Base** + offset (0x0720)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF3M[30:0] is used to configure the mask filed of each rule for ATF3; 1'b1: List Mode, Register ATF3M[30:0] is used as acceptance filter ATF8.
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M3 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM4

Address: **Operational Base** + offset (0x0724)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF4M[30:0] is used to configure the mask filed of each rule for ATF4; 1'b1: List Mode, Register ATF4M[30:0] is used as acceptance filter ATF9.
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M4 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)

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Bit	Attr	Reset Value	Description
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATF_DLC

Address: **Operational Base** + offset (0x0728)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	atf_dlc_mode 1'b0: Over Mode, DLC filter process is only passed if the DLC value of the message accepted is equal to or higher than the value of ATF_DLC.atf_dlc; 1'b1: Less Mode, DLC filter process is only passed if the DLC value of the message accepted is equal to or less than the value of ATF_DLC.atf_dlc.
4	RW	0x0	atf_dlc_en DLC Filter Enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	atf_dlc Configure DLC value of received message

RKCAN_ATF_CTL

Address: **Operational Base** + offset (0x072C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	atf9_en Acceptance Filter 9 Disable 1'b0: Disable 1'b1: Enable
8	RW	0x0	atf8_en Acceptance Filter 8 Disable 1'b0: Disable 1'b1: Enable
7	RW	0x0	atf7_en Acceptance Filter 7 Disable 1'b0: Disable 1'b1: Enable
6	RW	0x0	atf6_en Acceptance Filter 6 Disable 1'b0: Disable 1'b1: Enable
5	RW	0x0	atf5_en Acceptance Filter 5 Disable 1'b0: Disable 1'b1: Enable
4	RW	0x0	atf4_en Acceptance Filter 4 Disable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	atf3_en Acceptance Filter 3 Disable 1'b0: Disable 1'b1: Enable
2	RW	0x0	atf2_en Acceptance Filter 2 Disable 1'b0: Disable 1'b1: Enable
1	RW	0x0	atf1_en Acceptance Filter 1 Disable 1'b0: Disable 1'b1: Enable
0	RW	0x0	atf0_en Acceptance Filter 0 Enable 1'b0: Disable 1'b1: Enable

RKCAN_AUTO_RETX_CFG

Address: **Operational Base** + offset (0x0808)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	retx_cnt_self_clr retx_cnt clear bit
18:3	RO	0x0064	retx_time_limit Auto Retx Time Threshold
2	RW	0x0	auto_retx_cnt_clr Set to 1 to clear the Auto Retransmission Conter(auto_retx_cnt)
1	RW	0x0	retx_limit_en 1'b0: Diable retx_time_limit. Keep resending until the transmission is successful; 1'b1: Enable retx_time_limit. Stop retransmission when the number of retransmissions reaches the threshold.
0	RW	0x0	auto_retx_mode Auto Retransmission Mode 1'b0: Disable 1'b1: Enable

RKCAN_AUTO_RETX_STATE0

Address: **Operational Base** + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	noack_cnt No ACK Counter
15:0	RO	0x0000	auto_retx_cnt Automatic Retransmission Counter

RKCAN_AUTO_RETX_STATE1

Address: **Operational Base** + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	txerr_cnt TX Error Counter
15:0	RO	0x0000	arbit_fail_cnt Arbit Fail Counter

RKCAN_OLF_CFG

Address: **Operational Base** + offset (0x0814)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	tx_wait_thr Used to configure the number of bits for transmission wait.
15:13	RO	0x0	reserved
12	RO	0x0	tx_wait_clr tx_wait_cnt Clear
11	RO	0x0	tx_wait_mode Transmit wait mode. 1'b0: Immediate transmission 1'b1: Wait for "tx_wait_thr" bits before transmitting
10	RW	0x0	ovd_time 1'b0: Transmit one overload frame at a time 1'b1: Continuously transmit two overload frame at a time
9	RW	0x0	auto_ovd_mode Auto transmit Overload frame mode 1'b0: Disable 1'b1: Enable
8:0	RW	0x000	ovd_tx_thr Overload Frame Transmit Threshold Level. The configurable range is from 0 to 256. Unit:Word When the remaining space of the RXFIFO is less than the threshold set by ovd_tx_thr, RKCAN will automatically send an overload frame.

RKCAN_RXINT_CTRL

Address: **Operational Base** + offset (0x0818)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	mfi_timeout_mode Multi Frame Interrupt(MFI) Timeout Mode 1'b0: Disable 1'b1: Enable
16	RW	0x0	mfi_mode Multi Frame Interrupt(MFI) Mode 1'b0: Generate an interrupt when a frame is received; 1'b1: Generate an interrupt when N frames are received, N is configured by RXINT.rxint_num.
15:0	RW	0x0100	rxint_num Used to configure mulit frame interrupt mode

RKCAN_RXINT_TIMEOUT

Address: **Operational Base** + offset (0x081C)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000ffff	threshold Timeout Threshold for MFI Mode

RKCAN_ERROR_CODE

Address: **Operational Base** + offset (0x0900)

Bit	Attr	Reset Value	Description
31	RW	0x0	tx_crc_error_flag When RKCAN is the transmitter, CRC error is detected. 1'b0: No CRC Error 1'b1: An CRC Error has occurred

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Bit	Attr	Reset Value	Description
30	RW	0x0	rx_crc_error_flag When RKCAN is the receiver, CRC error is detected. 1'b0: No CRC Error 1'b1: An CRC Error has occurred
29	RO	0x0	error_phase 1'b0: Arbitration Phase 1'b1: Data Phase
28:26	RO	0x0	error_type Error type: 3'b000: BIT ERROR 3'b001: BIT STUFF ERROR 3'b010: FORM ERROR 3'b011: ACK ERROR 3'b100: CRC ERROR
25	RW	0x0	error_direction 'error_direction' is used to indicate whether RKCAN was in a sending or receiving state when an error occurred. 1'b0: TX Node 1'b1: RX Node
24:19	RO	0x00	tx_state Indicate the status of TX FSM when an error occurs 6'b000001: TRANSMIT_IDLE 6'b000010: TRANSMIT_SOF_DLC 6'b000100: TRANSMIT_DATA 6'b001000: TRANSMIT_STUFF_COUNT 6'b010000: TRANSMIT_CRC 6'b100000: TRANSMIT_ACK_EOF
18:0	RO	0x00000	rx_state Indicate the status of RX FSM when an error occurs 19'b0000000000000000001: RECEIVE_STOP 19'b0000000000000000010: RECEIVE_BUS_INT 19'b0000000000000000100: RECEIVE_BUS_IDLE 19'b0000000000000001000: RECEIVE_SOF_IDE 19'b0000000000000010000: RECEIVE_ID2_RTR 19'b0000000000000100000: RECEIVE_FDF 19'b0000000000001000000: RECEIVE_RES 19'b0000000000010000000: RECEIVE_BRS_ESI 19'b0000000000100000000: RECEIVE_DLC 19'b0000000001000000000: RECEIVE_DATA 19'b0000000010000000000: RECEIVE_STUFF_COUNT 19'b0000000100000000000: RECEIVE_CRC 19'b0000001000000000000: RECEIVE_CRC_LIM 19'b0000010000000000000: RECEIVE_ACK_SLOT 19'b0000100000000000000: RECEIVE_ACK_LIM 19'b0001000000000000000: RECEIVE_EOF 19'b0010000000000000000: RECEIVE_SPACE 19'b0100000000000000000: RECEIVE_OVERLOAD 19'b1000000000000000000: RECEIVE_ERROR

RKCAN_ERROR_MASK

Address: **Operational Base** + offset (0x0904)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	ack_error Error mask for ack error 1'b0: Unmasked 1'b1: Masked
3	RW	0x0	form_error Error mask for form error 1'b0: Unmasked 1'b1: Masked
2	RW	0x0	crc_error Error mask for crc error 1'b0: Unmasked 1'b1: Masked
1	RW	0x0	stuff_error Error mask for stuff error 1'b0: Unmasked 1'b1: Masked
0	RW	0x0	bit_error Error mask for bit error 1'b0: Unmasked 1'b1: Masked

RKCAN_RXERRORCNT

Address: **Operational Base** + offset (0x0910)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	rx_err_cnt Receive Error Counter (REC) Actual state of the Receive Error Counter. Value between 0 and 127.

RKCAN_TXERRORCNT

Address: **Operational Base** + offset (0x0914)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	tx_err_cnt Transmit Error Counter (TEC) Actual state of the Transmit Error Counter. Value between 0 and 255.

RKCAN_ARBIT_FAIL_STATE

Address: **Operational Base** + offset (0x0918)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	arbit_fail_code This register indicates the bit position of arbitration section where the arbitration was lost.

RKCAN_RTL_VERSION

Address: **Operational Base** + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RO	0xcfdba0eb	version RKCAN Version = 32'hCFD_B_A0_E5

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35.4 Interface Description

35.5 Application Notes

35.5.1 Controller initialization flow

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

After the initialization is completed, the controller enters the working mode, sends the frame to be sent to the buffer, and then sets the "send request" flag of the command register to start transmitting.

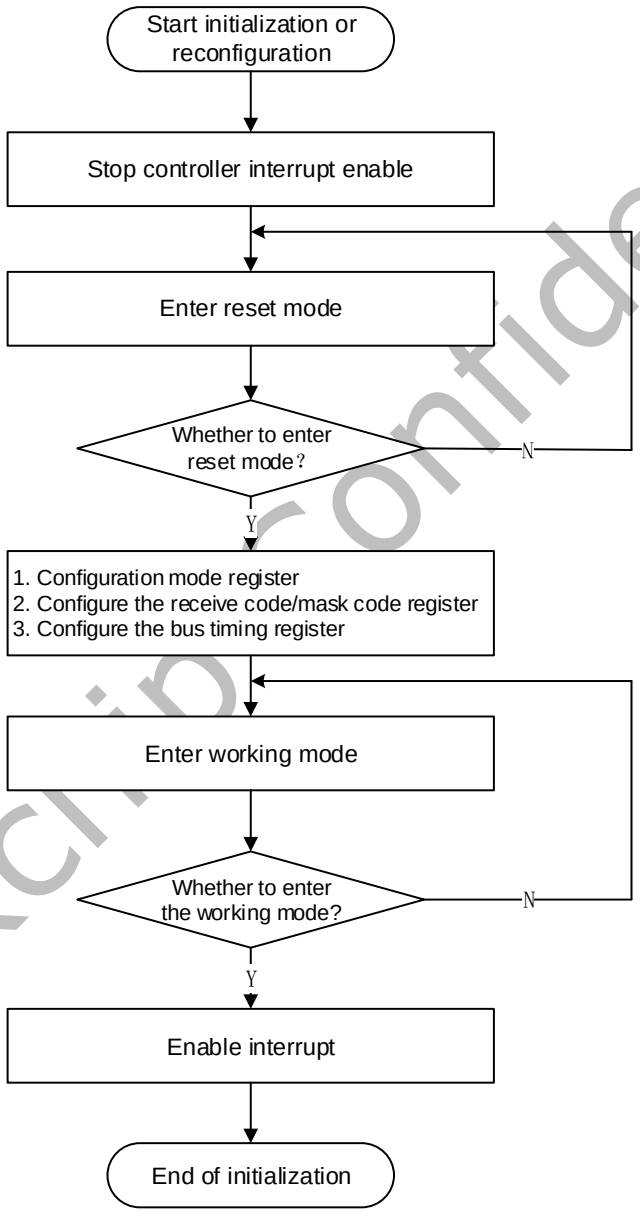

Fig. 35-11 Initialization Flow

35.5.2 Loop-back Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

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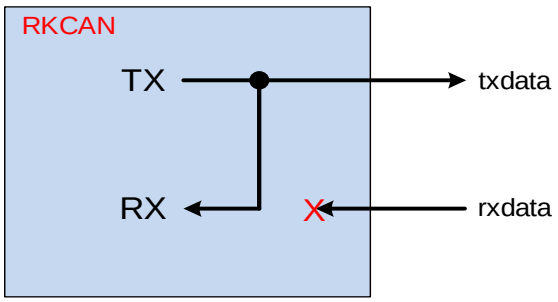

Fig. 35-12 Loop-back Mode

35.5.3 Silent Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

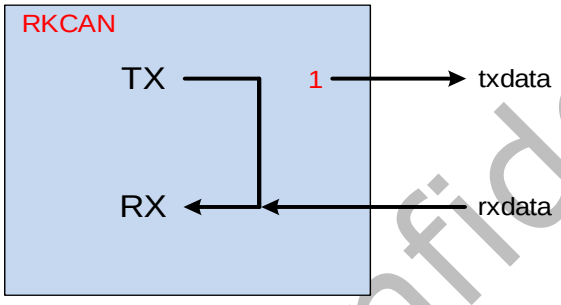

Fig. 35-13 Silent Mode

35.5.4 RXSTX Mode

(1)rxstx_mode=0, RKCAN cannot receive the data sent by itself;
(2)rxstx_mode=1, RKCAN can receive the data sent by itself, and when the ID of the frame is the same as the ID_CODE of RKCAN itself, RKCAN will store the frame information into RX storage.

35.5.5 Auto Retx Mode

RKCAN supports two automatic retransmission modes:
(1) Unlimited Retransmission Mode: There is no limit to the number of retransmissions until the retransmission is successful.
(2) Limited Retransmissions Mode: The threshold for the number of automatic retransmissions can be configured. If the limit threshold is reached and the retransmission is still not successful, the retransmission will stop, and a retransmission failure interrupt will be issued. RKCAN will also count the reasons and corresponding times that cause the transmission failure during the retransmission process, such as arbitration failure, NoACK, or bus error, etc.

35.5.6 Bus Off Recovery Mechanism

RKCAN supports three configurable Bus_off recovery mechanisms, which are:
(1) Automatic Recovery: When the RKCAN node detects 11 recessive bits (no active messages on the CAN bus) appearing consecutively 128 times, it can automatically exit the Bus_off state.
(2) Timed Recovery: The timing length can be set by configuring the register. After the timer expires, RKCAN exits the Bus_off state. The software can implement fast recovery and slow recovery functions using the timed recovery mode.
(3) Manual Recovery: In manual recovery mode, RKCAN will not automatically exit the Bus-off state. It can only exit the Bus-off state by configuring the manual recovery register.

35.5.7 Sleep Mode

After enabling Sleep Mode, RKCAN will automatically enter a low-power mode when the bus is idle, turning off the internal clock. The internal clock will automatically turn on when

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there is a data frame on the bus or when a data frame needs to be sent.

35.5.8 Multi-frame Mode

RKCAN supports an interrupt being issued upon receiving each frame, and it can also be configured to issue an interrupt only after receiving N frames in multi-frame mode. This can reduce the number of interrupts and reduce software intervention. The related configuration can be found in the register RXINT_CTRL register and RXINT_TIMEOUT.

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Chapter 36 Double Data Rate Serial Memory Controller (DSMC)

36.1 Overview

The DSMC module provides function and operation for interfacing to the DSMC memory devices, and the Rockchip Localbus devices. The DSMC achieves high speed read/write throughput by double data rate interface

The main feature is shown below

- Support the double data rate interface
- Support up to select 4 chips
- Support 8-wire and 16-wire serial transfer mode
- Support configurable write/read contiguous address merging transaction
- Support configurable write/read boundary address splitting transaction
- Support to transform WRAP transfer to INCR transfer
- Support byte access
- Support configurable DQS input clock delay line
- For Localbus devices, support to assert the selecting signals CS simultaneously in the write transaction
- For Localbus devices, support 3 clock mode : normal mode, always-on mode, no-edge-clk mode
- For Localbus devices, support to request DMAC to transfer data when receiving interrupt 0/1
- For Localbus devices, support configurable serial address width: 16 bits or 32 bits in different region

36.2 Block Diagram

DSMC is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- AXI Interface

The AXI Interface is a XIP interface to access internal device. Its data bus width is 64 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Core

The core module is used to control the data stream of TX/RX datapath.

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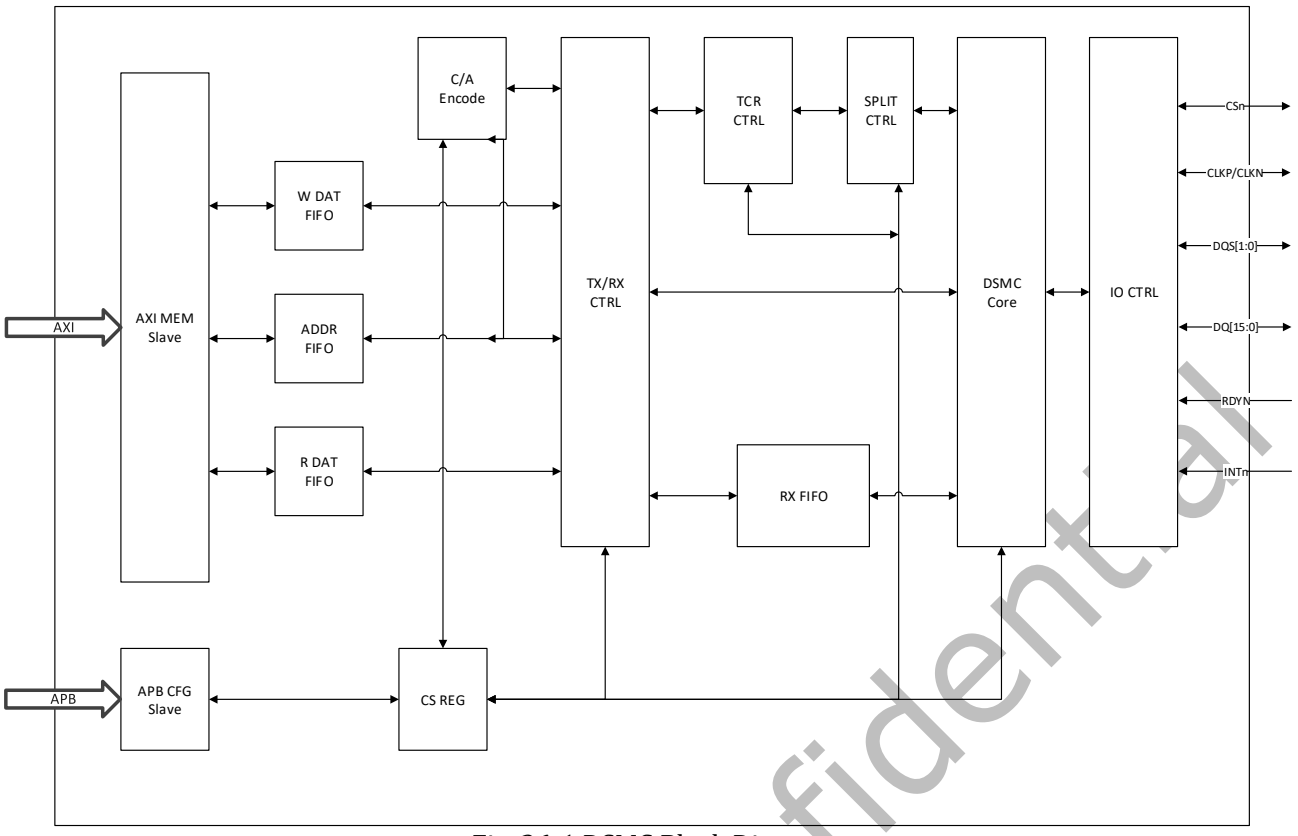

Fig. 36-1 DSMC Block Diagram

36.3 Function Description

The DSMC module is high throughput memory interface. It provides execute in place (XIP) and block copy access to DSMC memory devices (HyperRAM and HyperFlash). The DSMC module is compliant to the Cypress DSMC™ Specification. Meanwhile, it could access Rockchip Localbus devices, and transfer instructions or bulk data with high speed.

36.3.1 DSMC Core

This section describes physical interface of DSMC module. The DSMC core generates DSMC timing from control signals

36.3.1.1 Read

DSMC Core module asserts CSn, CLKP/CLKN, and DQ. Then, it outputs 3 words command/address, and reads 1 or more data by the timing of DQS. The DSMC Core puts the transaction request from AXI bus, such as the burst type and the burst length, to the C/A cycle on DSMC as is shown below.

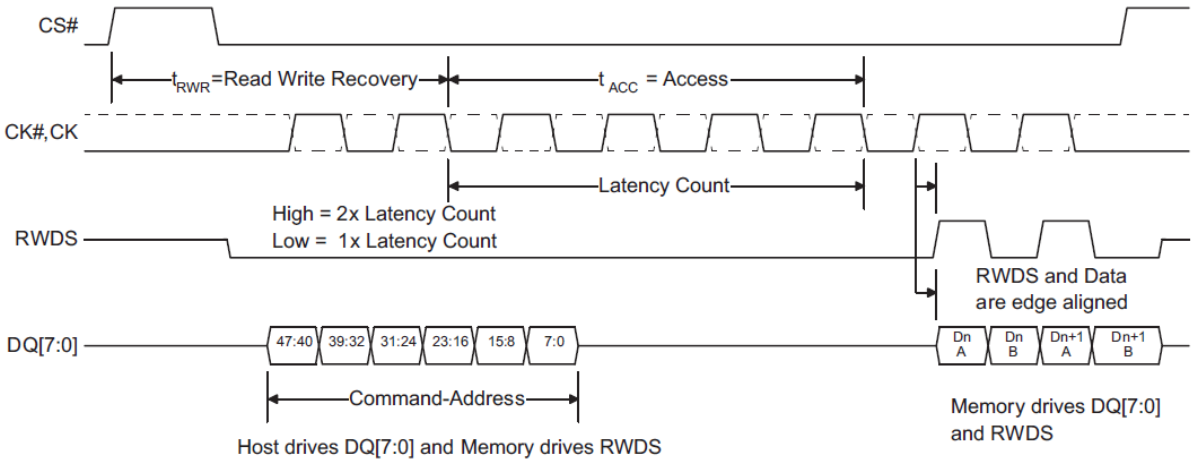

Fig. 36-2 HyperRAM Read Waveform

36.3.1.2 Write

This section describes the write operation of DSMC Core. The DSMC Core asserts CSn,

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CLKP/CLKN, and DQ. Then, it outputs 3 words command/address, and writes 1 or more data. For HyperRAM write operation, there is initial clock latency before writing data.

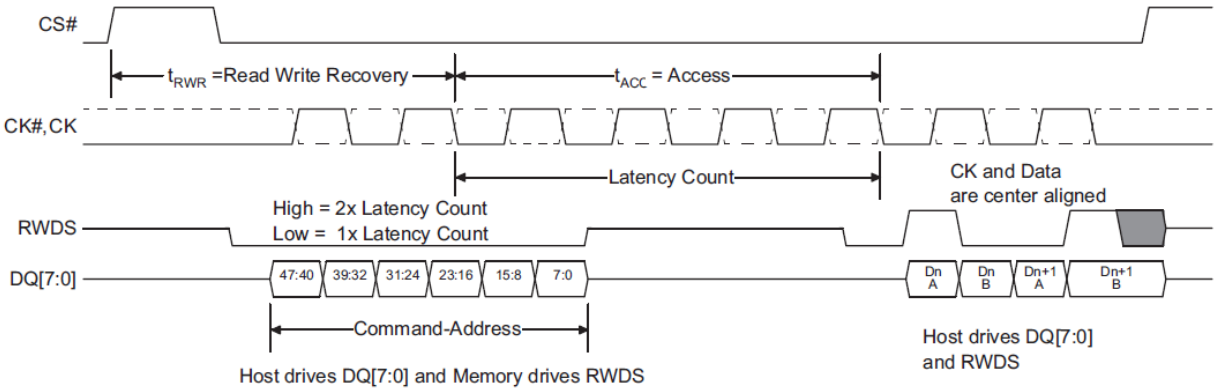

Fig. 36-3 HyperRAM Write Waveform

36.3.1.3 Byte Mask

This DSMC Memory Interface Controller outputs DQS signal as a byte mask during write operation. When byte access is requested from Main Controller, not write data is masked by DQS=HIGH. When target device is HyperFlash, byte masked data is written to device because of only supporting 16-bit access (byte masked data is fill in all 1 bit). In the HyperRAM Write Waveform, the D_n A and D_{n+1} B is invalid data which is masked.

36.3.2 TX/RX Controller

The TX/RX Controller performs operation control by state machine, and flow control of data between AXI bus and DSMC. In addition, when next access address is accepted by multiple outstanding address on AXI bus, it could be merged to the present transaction to improve the bandwidth if the address of subsequent access is continuous address to the present access.

36.3.3 C/A Encoder

DSMC memory device uses 6 bytes of command/address information to define the transactions characteristics. Table below shows the assignments of CA bit in DSMC Memory Interface Controller.

Table 36-1 C/A Format of DSMC for Hyper Device

C/A Bit	Name	Assignment
47	R/W#	0: Write, 1: Read
46	Target	CRT in DSMC_MCRn
45	Burst Type	0: WRAP, 1: INCR
44	RFU	0
43-16	Page Address	Address [31:4]
15	RFU	0
14-13	RFU	3
12-3	RFU	0
2-0	Column Address	Address [3:1]

note: The CA bit function of different devices slightly differs, and the exact meaning nead to be referred to the datasheet of the device.

36.3.4 FIFO

This section describes the FIFO for processing transaction request

36.3.4.1 ADDR FIFO

ADR FIFO is a synchronizer module from AXI clock domain to DSMC clock domain. This FIFO has 46-bit width. This FIFO stores the control data which includes address, length, burst type and r/w flag. From these data, the control signals are generated for Main Controller.

36.3.4.2 W DAT FIFO

This FIFO is used to store the write data, valid information and strobe information written from the master in order to receive the command sequence of write buffer programming without a wait on AXI interface. The valid information indicates the 8-bit data is valid or not. The strobe information is used for strobe data from AXI interface to DSMC Core. When

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valid and strobe is 1, the 8-bit data is written data

36.3.4.3 R DAT FIFO

This FIFO is used to store the data read from RX FIFO and the error detection information, and data stored is outputted according to timing of ACLK on AXI interface. This error information is transferred to HOST by RRESP signals.

36.3.5 Localbus

36.3.5.1 Region division

The internal space of Localbus device could be divided into different region, and they could be applied in suitable case. The size of regions is configure by DSMC_DEV_SIZE and DSMC_SLV_RGN_DIVn. The attribution of different region could be set to DPRA, REG or FIFO.

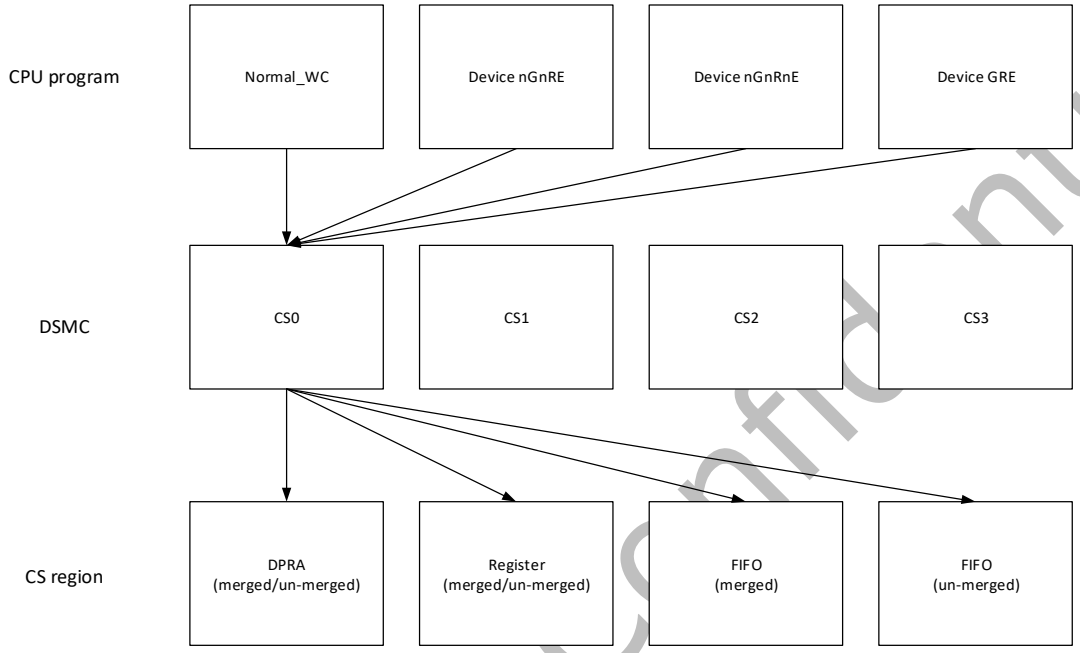

Fig. 36-4 Region division of Localbus device

36.3.5.2 CA Encoder

Table 36-2 C/A Format of DSMC for Localbus Device

C/A Bit	Name	Assignment
47	R/W#	0: Read, 1: Write
46	Target	CRT in DSMC_MCRn
45	Burst Type	0: WRAP, 1: INCR
44	Space Type	0: FIFO, 1: DPRA
43	FIFO Merge	0: No Merge, 1: Merge
42	RFU	0
41-40	Region	Region 0/1/2/3
39-32	Length	Burst length
31-0	Address	Address [31:0]

36.3.5.3 Back pressure

The back pressure mechanism is used to make full use of FIFO region space.

In the read transaction, when the FIFO is empty and could not provide data to the DSMC interface, the slave could enter the wait state, in which slave stop to send DQS clock, and latch the output DQ data. When the FIFO is recovered, the slave could continue sending the DQS and DQ, which could save bandwidth comparing to restart another burst.

In the write transaction, when the FIFO is full and could not receive data from the DSMC interface, the asynchronous signal DSMC_RDYN would be asserted. When the DSMC received, it would not send DQ and DSMC_CLK until the DSMC_RDYN is not asserted, which means there are enough space in the slave FIFO to accept data.

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36.4 Register Description

36.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

36.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DSMC_VER	0x0000	W	0x00000100	IP Version Register
DSMC_CSR	0x0008	W	0x00000000	Controller Status Register
DSMC_TAR	0x0010	W	0x00000000	Transaction Allocation Register
DSMC_AXICTL	0x0014	W	0x00000020	AXI Transcation Control Register
DSMC_CLK_MD	0x0020	W	0x00000000	Clock Mode Register
DSMC_DEV_SIZE	0x0030	W	0x00000017	Device Region Size Register
DSMC_INT_EN	0x0040	W	0x00000000	Interrupt Enable Register
DSMC_INT_STATUS	0x0044	W	0x00000000	Interrupt Status Register
DSMC_INT_MASK	0x0048	W	0x00000000	Interrupt Mask Register
DSMC_DMA_EN	0x0050	W	0x00000000	DMA Request Enable Register
DSMC_DMA_REQ_NUM0	0x0054	W	0x00000000	DMA Request Number Register 0
DSMC_DMA_REQ_NUM1	0x0058	W	0x00000000	DMA Request Number Register 1
DSMC_VDMC0	0x1000	W	0x00000226	Vendor Device Mode Control Register, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MCR0	0x1010	W	0x00000003	CS0# Memory Configuration Register, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MTR0	0x1014	W	0x00000022	CS0# Memory Base Address, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_WAIT_TIME0	0x1018	W	0x000007FF	CS0# Memory Base Address, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_BDRTCR0	0x1020	W	0x00000002	Boundary Transfer Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MRGTCR0	0x1024	W	0x00000000	Merge Transfer Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_WRAP2INCR0	0x1028	W	0x00000000	The function register of changing WRAP to INCR, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RDS_DLL0_CTL0	0x1030	W	0x80000010	RDS Clock DLL Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000

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Name	Offset	Size	Reset Value	Description
DSMC_RDS_DLL1_CTL0	0x1034	W	0x80000010	RDS Clock DLL Control Register 1, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_SLV_RGN_DIV0	0x1040	W	0x00000002	The division of slave region , and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN0_ATTR0	0x1050	W	0x00000000	The attribution of region 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN1_ATTR0	0x1054	W	0x00000000	The attribution of region 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN2_ATTR0	0x1058	W	0x00000000	The attribution of region 2, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN3_ATTR0	0x105C	W	0x00000000	The attribution of region 3, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

36.4.3 Detail Registers Description

DSMC_VER

Address: Operational Base(0x2A280000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000100	version IP Version

DSMC_CSR

Address: Operational Base(0x2A280000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	wrstoerr Write RSTO error. This bit indicates whether HyperBus memory is under reset state in the latest write operation. 1'b0: Normal operation 1'b1: HyperBus memory is under reset When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
25	RO	0x0	wtrserr Write Transaction Error. This bit indicates whether AXI protocol is acceptable by HyperBus Memory Controller IP in the latest write transaction. 1'b0: Normal operation 1'b1: This protocol is not supported When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.

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Bit	Attr	Reset Value	Description
24	RO	0x0	wdecerr Write Decode Error. This bit indicates whether access address is acceptable in the latest write transaction. 1'b0: Normal operation 1'b1: Access address is not reachable When this bit is set, HyperBus Memory Controller IP responds by AXI DECERR.
23:17	RO	0x00	reserved
16	RO	0x0	wact Write is Active. This bit indicates whether write transaction is in progress or not. 1'b0: Write is idle 1'b1: Write is active
15:12	RO	0x0	reserved
11	RO	0x0	rdsstall RDS Stall. This bit indicates whether read data transfer from HyperBus memory is stalled (RDS remains LOW) in the latest read transaction. 1'b0: Normal operation 1'b1: RDS is stalled When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
10	RO	0x0	rrstoerr Read RSTO error. This bit indicates whether HyperBus memory is under reset state in the latest read operation. 1'b0: Normal operation 1'b1: HyperBus memory is under reset When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
9	RO	0x0	rtrserr Read Transaction Error. This bit indicates whether AXI protocol is acceptable by HyperBus Memory Controller IP in the latest read transaction. 1'b0: Normal operation 1'b1: This protocol is not supported When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
8	RO	0x0	rdecerr Read Decode Error. This bit indicates whether access address is acceptable in the latest read transaction. 1'b0: Normal operation 1'b1: Access address is not reachable When this bit is set, HyperBus Memory Controller IP responds by AXI DECERR.
7:1	RO	0x00	reserved
0	RO	0x0	ract Read is Active. This bit indicates whether read transaction is in progress or not. 1'b0: Read is idle 1'b1: Read is active

DSMC_TAR

Address: Operational Base(0x2A280000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	rta Read Transaction Allocation. 2'b00: 1 read transaction 2'b01: 2 read transactions 2'b10: 3 read transactions 2'b11: 4 read transactions
3:2	RO	0x0	reserved
1:0	RW	0x0	wta Write Transaction Allocation. 2'b00: 1 write transaction 2'b01: 2 write transactions 2'b10: 3 write transactions 2'b11: 4 write transactions

DSMC_AXICTL

Address: Operational Base(0x2A280000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rd_no_err The axi read response will be tied 0 if this bit is enabled. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:4	RW	0x2	write_bvalid_ctl 2'b00: Generate the bvalid after the burst data TX end in IO 2'b01: Generate the bvalid after the TX state machine accept the request FIFO 2'b10: Generate the bvalid after burst write granted by arbiter 2'b11: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	nowait_write_data_done_en 1'b0: Disable 1'b1: Enable Only support "0" in current project

DSMC_CLK_MD

Address: Operational Base(0x2A280000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	clk_mode This register is only configured in local bus application. 2'b00: Normal-toggle Mode, the ck only toggles when cs is asserted 2'b01: Always-on Mode, the ck is always on 2'b10: No-edge-clk Mode, the ck is always on except for the cs changing edge 2'b11: Reserved

DSMC_DEV_SIZE

Address: Operational Base(0x2A280000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x17	dev_size Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 2G bytes In Memory-Mapped mode, the CS is controlled by AXI address bus, region size is used to generate CS.

DSMC_INT_EN

Address: Operational Base(0x2A280000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	rdstall_int_en This bit is used to control the read stall time out interrupt enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en3 This bit is used to control the interrupt3. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
2	RW	0x0	int_en2 This bit is used to control the interrupt2. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
1	RW	0x0	int_en1 This bit is used to control the interrupt1. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
0	RW	0x0	int_en0 This bit is used to control the interrupt0. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable

DSMC_INT_STATUS

Address: Operational Base(0x2A280000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	W1C	0x0	rdstall_int_status Read stall time out interrupt status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.

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Bit	Attr	Reset Value	Description
3	W1C	0x0	int_status3 Interrupt 3 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.
2	W1C	0x0	int_status2 Interrupt 2 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.
1	W1C	0x0	int_status1 Interrupt 1 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.
0	W1C	0x0	int_status0 Interrupt 0 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.

DSMC_INT_MASK

Address: Operational Base(0x2A280000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	rdstall_int_mask This register is used to mask the read stall interrupt. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
3	RW	0x0	int_mask3 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
2	RW	0x0	int_mask2 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
1	RW	0x0	int_mask1 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
0	RW	0x0	int_mask0 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked

DSMC_DMA_EN

Address: Operational Base(0x2A280000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dma_req_en1 This bit is used to control the DMA request from interrrupt1. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	dma_req_en0 This bit is used to control the DMA request from interrrupt0. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable

DSMC_DMA_REQ_NUM0

Address: Operational Base(0x2A280000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	dma_req_num0 This register is used to indicate the DMA request number when DSMC accepts the interrupt0 from local bus slave. This register is only valid in local bus application.

DSMC_DMA_REQ_NUM1

Address: Operational Base(0x2A280000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	dma_req_num1 This register is used to indicate the DMA request number when DSMC accepts the interrupt1 from local bus slave. This register is only valid in local bus application.

DSMC_VDMC0

Address: Operational Base(0x2A280000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x1	latency_fixed Only valid to APM pSRAM Read Memory. 1'b0: Variable 1'b1: Fixed
8	RW	0x0	reset_cmd_mode Generate reset Command to Device. Only valid in APM mid when CR register mode is set. If this bit is set, any write access in CR mode will initiate the FF command sequence.
7:4	RW	0x2	protocol Device Type 4'h0: Reserved 4'h1: OPI_Xccela (reserved) 4'h2: HyperBus (reserved) 4'h3: Local Bus Others: Reserved
3:0	RW	0x6	mid MID 4'h1: Infineon/Cypress 4'h3: ISSI 4'h6: Winbond 4'hd: APM Others: Reserved

DSMC_MCR0

Address: Operational Base(0x2A280000) + offset (0x1010)

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Bit	Attr	Reset Value	Description
31	RW	0x0	maxen Maximum length Enable 1'b0: No configurable CS# low time 1'b1: Configurable CS# low time When this bit 1, CS# low time can be configurable by MAXLEN bit.
30:27	RO	0x0	reserved
26:18	RW	0x000	maxlen Maximum Length This bit indicates maximum read/write transaction length to memory. This bit is ignored when MAXEN bit is 0. 9'h000: 2 Byte (1 HyperBus CK) 9'h001: 4 Byte (2 HyperBus CK) 9'h002: 6 Byte (3 HyperBus CK) ..... 9'h1ff: 1024 Byte (512 HyperBus CK)
17	RW	0x0	tcmo True Continuous Merge Option. 1'b0: No merging WRAP and INCR 1'b1: Merging WRAP and INCR Note that this function can be used with the HyperBus memory with specific function. Please confirm whether it is corresponding HyperBus memory before enabling this function. If set to 1, it means the controller can merge the Wrap and INCR opperation.
16	RW	0x0	acs Asymmetry Cache Support. 1'b0: No asymmetry cache system support. 1'b1: Asymmetry cache system support. This function should be disabled if the HyperBus memory itself supports the asymmetry cache system. If this bit set to 1, then the HyperBus memory interface controller accepts the wrap read transaction, and compares the required wrap size with the wrap size of HyperBus memory in register; When the wrap size is the same, HyperBus memory interface controller requires the wrap burst read to HyperBus memory; When the wrap size differs, HyperBus memory interface controller emulates wrap burst read by requesting two continuous burst read to HyperBus memory
15:6	RO	0x000	reserved
5	RW	0x0	crt Configuration Register Target. 1'b0: Memory space 1'b1: CR space This bit indicates whether the read or write operation accesses the memory or CR space. This bit is mapped to CA[46] bit in HyperRAM. When using HyperFlash, this bit should be set to 0.
4	RW	0x0	devtype Device Type. 1'b0: HyperFlash 1'b1: HyperRAM Device type for control target. Only support "1" in current project

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Bit	Attr	Reset Value	Description
3	RW	0x0	iowidth IO Width. 1'b0: x8 interface 1'b1: x16 interface Note that "1'b1: x16 interface" can be set when DEVTYPE is set to "1'b1: HyperRAM"
2	RW	0x0	exclusive_dqs This bit field indicates the number of valid dqs bit when io width is 16 bits, and it is only valid in local bus application. 1'b0: 2 bits 1'b1: 1 bit
1:0	RW	0x3	wrapsize Wrap Size. 2'b00: Reserved 2'b01: 32(Clocks), 64 bytes for x8 and 128 bytes for x16 2'b10: 8(Clocks), 16 bytes for x8 and 32 bytes for x16 2'b11: 16(Clocks), 32 bytes for x8 and 64 bytes for x16 The wrap burst length of HyperBus memory. This bit is ignored when the asymmetry cache support bit is 0. When the asymmetry cache support is 1, this bit should be set the same as wrap size of configuration register in HyperBus memory.

DSMC_MTR0

Address: Operational Base(0x2A280000) + offset (0x1014)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	rcshi Read Chip Select High Between Operations. This bit indicates CS# high time for read between operations. 0x0 corresponds to 1.5 clock cycle, 0xF corresponds to 16.5 clock cycle.
27:24	RW	0x0	wcshi Write Chip Select High Between Operations. This bit indicates CS# high time for write between operations. 0x0 corresponds to 1.5 clock cycle, 0xF corresponds to 16.5 clock cycle.
23:20	RW	0x0	rcss Read Chip Select Setup to next CK rising edge. This bit indicates CS# setup time for read from CS# assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle.
19:16	RW	0x0	wcss Write Chip Select Setup to next CK rising edge. This bit indicates CS# setup time for write from CS# assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle.
15:12	RW	0x0	rcsh Read Chip Select Hold after CK falling edge. This bit indicates CS# hold time for read to CS# de-assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle.
11:8	RW	0x0	wcsh Write Chip Select Hold after CK falling edge. This bit indicates CS# hold time for write to CS# de-assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle.

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Bit	Attr	Reset Value	Description
7:4	RW	0x2	rltcy Read Latency Cycle. Only uses in HyperRAM. This bit indicates initial latency code for write access. This bit is ignored when MCRX.DEVTYPE is 0 (HyperFlash). 4'h0: 5 clock latency 4'h1: 6 clock latency 4'h2: 7 clock latency 4'h3: 8 clock latency 4'h4: 9 clock latency 4'h5: 10 clock latency 4'hb: 0 clock latency 4'hc: 1 clock latency 4'hd: 2 clock latency 4'he: 3 clock latency 4'hf: 4 clock latency Others: Reserved
3:0	RW	0x2	wltcy Write Latency Cycle. Only uses in HyperRAM. This bit indicates initial latency code for write access. This bit is ignored when MCRX.DEVTYPE is 0 (HyperFlash). 4'h0: 5 clock latency 4'h1: 6 clock latency 4'h2: 7 clock latency 4'h3: 8 clock latency 4'h4: 9 clock latency 4'h5: 10 clock latency 4'hb: 0 clock latency 4'hc: 1 clock latency 4'hd: 2 clock latency 4'he: 3 clock latency 4'hf: 4 clock latency Others: Reserved

DSMC_WAIT_TIME0

Address: Operational Base(0x2A280000) + offset (0x1018)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x7ff	rdstall_wait_time This bit filed is used to configure the max wait time of the read stall status.

DSMC_BDRTCR0

Address: Operational Base(0x2A280000) + offset (0x1020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	rd_bdr_xfer_en Enable Cross Row Address Data Read Transfer. 1'b0: Disable 1'b1: Enable
4	RW	0x0	wr_bdr_xfer_en Enable Cross Row Address Data Write Transfer. 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x2	col_bit_num The valid column address bit, also the cycle numbers in the port. 3'h0: 6 bit 3'h1: 7 bit 3'h2: 8 bit 3'h3: 9 bit 3'h4: 10 bit 3'h5: 11 bit Others: Reserved

DSMC_MRGTCR0

Address: Operational Base(0x2A280000) + offset (0x1024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_merge_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	write_merge_en 1'b0: Disable 1'b1: Enable

DSMC_WRAP2INCR0

Address: Operational Base(0x2A280000) + offset (0x1028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	wrap2incr_en This bit is used to enable the function of changing WRAP transfer to INCR transfer. This register is only configured in local bus application. 1'b0: Disable 1'b1: Enable

DSMC_RDS_DLL0_CTL0

Address: Operational Base(0x2A280000) + offset (0x1030)

Bit	Attr	Reset Value	Description
31	RW	0x1	rds_0_clk_smp_sel DQ[7:0] Sampling Clock Selection 1'b0: Without DLL 1'b1: With DLL
30:8	RO	0x000000	reserved
7:0	RW	0x10	rds_0_clk_delay_num RDS Clock 0 Delay Line Cell Number

DSMC_RDS_DLL1_CTL0

Address: Operational Base(0x2A280000) + offset (0x1034)

Bit	Attr	Reset Value	Description
31	RW	0x1	rds_1_clk_smp_sel DQ[7:0] Sampling Clock Selection 1'b0: Without DLL 1'b1: With DLL
30:8	RO	0x000000	reserved
7:0	RW	0x10	rds_1_clk_delay_num RDS Clock 0 Delay Line Cell Number

DSMC_SLV_RGN_DIV0

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Address: Operational Base(0x2A280000) + offset (0x1040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x2	slv_rgn_div This register is only valid in local bus application. This bit filed indicate the region division of the slave memory. 2'b00: 1 2'b01: 2 2'b10: 4 Others: Reserved

DSMC_RGN0_ATTR0

Address: Operational Base(0x2A280000) + offset (0x1050)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn0_addr_width This bit is used to indicate the address width of the CA phase when access region 0. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn0_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only when write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rgn0_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region0. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn0_be_ctrled The cs0 accessing region0 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn0_ctrl The cs0 accessing region0 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn0_attr This register is only valid in local bus application. The attribution of the region0 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN1_ATTR0

Address: Operational Base(0x2A280000) + offset (0x1054)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	rgn1_addr_width This bit is used to indicate the address width of the CA phase when access region 1. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn1_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only whe write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rgn1_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region1. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn1_be_ctrled The cs0 accessing region1 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn1_ctrl The cs0 accessing region1 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn1_attr This register is only valid in local bus application. The attribution of the region1 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN2_ATTR0

Address: Operational Base(0x2A280000) + offset (0x1058)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn2_addr_width This bit is used to indicate the address width of the CA phase when access region 2. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn2_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only when write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rgn2_wr_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	rgn2_be_ctrled The cs0 accessing region2 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn2_ctrl The cs0 accessing region2 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn2_attr This register is only valid in local bus application. The attribution of the region1 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN3_ATTR0

Address: Operational Base(0x2A280000) + offset (0x105C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn3_addr_width This bit is used to indicate the address width of the CA phase when access region 3. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn3_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only when write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rng3_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn3_be_ctrled The cs0 accessing region3 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn3_ctrl The cs0 accessing region3 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	rgn3_attr This register is only valid in local bus application. The attribution of the region3 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

36.5 Interface Description

Table 36-3 DSMC interface description

Module Pin	Direction	Pin Name	IOMUX Setting
CLKP	O	VO_LCDC_HSYNC/VO_EBC_GDCLK/SAI1_SDI2_M1/DSMC_CLKP/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[7:4]=4'h5
CLKN	O	VO_LCDC_VSYNC/VO_EBC_SDCLK/SAI1_SDI3_M1/DSMC_CLKN/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:8]=4'h5
CS0	O	VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[15:12]=4'h5
CS1	O	VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0]=4'h5
CS2	O	VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[7:4]=4'h5
CS3	O	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8]=4'h5
RESETN	O	VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12]=4'h5

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Module Pin	Direction	Pin Name	IOMUX Setting
DQS0	I/O	VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12]=4'h5
DQS1	I/O	VO_LCDC_D13/VO_EBC_SDDO13/ETH0_TXCLK_M0/DSMC_DQS1/FLEXBUS0_CLK/SPI3_CSN0_M1/PWM0_CH1_M3/GPIO3_B6_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'h5
DQ0	I/O	VO_LCDC_DEN/VO_EBC_SDLE/SAI1_SDI1_M1/DSMC_DATA0/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[3:0]=4'h5
DQ1	I/O	VO_LCDC_D3/VO_EBC_SDDO3/SAI1_MCLK_M1/DSMC_DATA1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4'h5
DQ2	I/O	VO_LCDC_D4/VO_EBC_SDDO4/SAI1_SCLK_M1/DSMC_DATA2/FLEXBUS1_D4/UART8_RTSN_M0/SPI1_CLK_M2/GPIO3_C7_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[15:12]=4'h5
DQ3	I/O	VO_LCDC_D5/VO_EBC_SDDO5/SAI1_LRCK_M1/DSMC_DATA3/FLEXBUS1_D5/UART8_TX_M0/SPI1_MOSI_M2/GPIO3_C6_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[11:8]=4'h5
DQ4	I/O	VO_LCDC_D6/VO_EBC_SDDO6/SAI1_SDO0_M1/DSMC_DATA4/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4'h5
DQ5	I/O	VO_LCDC_D7/VO_EBC_SDDO7/SAI1_SDO1_M1/DSMC_DATA5/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/CAN0_TX_M3/GPIO3_C4_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4'h5
DQ6	I/O	VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4]=4'h5
DQ7	I/O	VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/DSMC_DATA7/FLEXBUS1_D9/UART2_	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0]=4'h5

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Module Pin	Direction	Pin Name	IOMUX Setting
		TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	
DQ8	I/O	VO_LCDC_D14/VO_EBC_SDDO14/ETH0_TXD0_M0/SPDIF_TX1_M0/DSMC_DATA8/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'h5
DQ9	I/O	VO_LCDC_D15/VO_EBC_SDDO15/ETH0_TXD1_M0/SPDIF_RX1_M0/DSMC_DATA9/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[3:0]=4'h5
DQ10	I/O	VO_LCDC_D16/VO_EBC_SDCE0/ETH0_TXCTL_M0/PDM1_SDI0_M2/DSMC_DATA10/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[15:12]=4'h5
DQ11	I/O	VO_LCDC_D17/VO_EBC_SDCE1/ETH0_RXD0_M0/PDM1_SDI1_M2/DSMC_DATA11/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[11:8]=4'h5
DQ12	I/O	VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[7:4]=4'h5
DQ13	I/O	VO_LCDC_D20/VO_EBC_VCOM/ETH0_RXCTL_M0/PDM1_CLK1_M2/DSMC_DATA13/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[15:12]=4'h5
DQ14	I/O	VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8]=4'h5
DQ15	I/O	VO_LCDC_D22/VO_EBC_GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[7:4]=4'h5
INT0	I	SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4'h5

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Module Pin	Direction	Pin Name	IOMUX Setting
		/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	
INT1	I	VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8]=4'h5
INT2	I	VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/DSMC_INT2/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4'h5
INT3	I	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12]=4'h5
RDYN	I	VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0]=4'h5

Notes: I=input, O=output, I/O=input/output, bidirectional.

36.6 Application Notes

36.6.1 Typical Program Flow for Hyper Device

1. Configure the DSMC_DEV_SIZE according to the size of device applied.
2. Configure the DSMC_MRGTCRx to support merge operation, and the DSMC_BDRTCRx to support crossing the boundary.
3. Configure the DSMC_MTRx to adjust the transfer timing.
4. Configure DSMC_MCRx to access the slave configure register.
5. Set the slave configuration to be consistent with the host, such as write and read latency.
6. Configure DSMC_MCRx to access the slave memory space.

36.6.2 Typical Program Flow for Localbus Device

1. Configure the DSMC_DEV_SIZE according to the size of device applied.
2. Configure the DSMC_MRGTCRx to support merge operation, and the DSMC_BDRTCRx to support crossing the boundary.
3. Configure the DSMC_MTRx to adjust the transfer timing.
4. Configure the DSMC_VDMCx to Localbus.
5. Enable the DSMC_WRAP2INCRx function if the slave required.
6. Configure DSMC_MCRx to access the slave configure register.
7. Keep the configuration parameter of the slave is the same as the master.
8. Configure DSMC_MCRx to access the slave memory space.

36.6.3 Chip Select selection

This section describes how to select Chip Select. This controller can’t assert two Chip Select

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at the same time except for the Localbus write.
When the device size is configured, the 2 address bits higher than device size are used as chip select signals.

36.6.4 Configurable CS# Low Time

This section describes configurable CS# low time. HyperRAM has a regulation for CS# low time (t_{CSM}). To meet CS# low time, a read/write transaction can be regulated by setting MCRx.MAXLEN bit. By MCRx.MAXLEN bit, one transaction is split multi transactions.

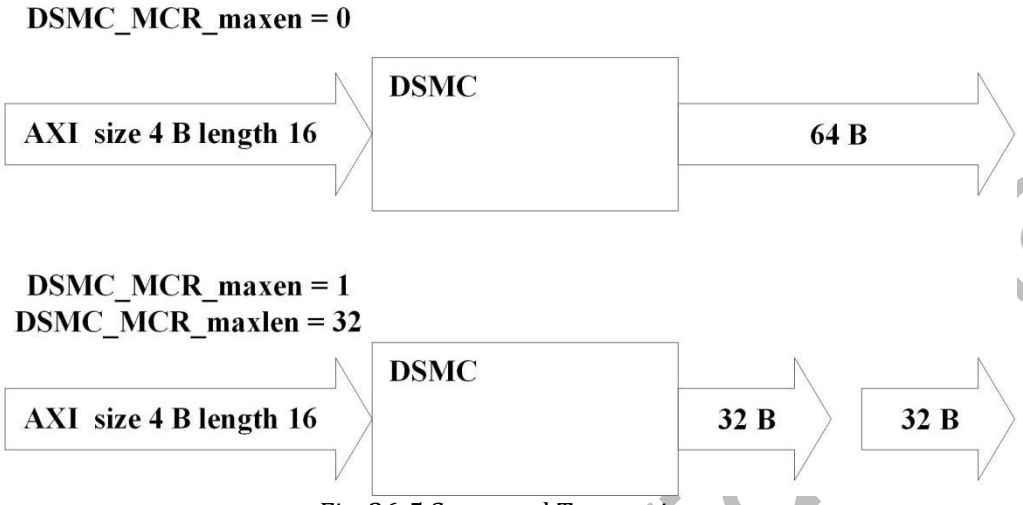

Fig. 36-5 Separated Transaction

36.6.5 Data Map

The data mapping relationship between memory and DSMC interface is shown as below.

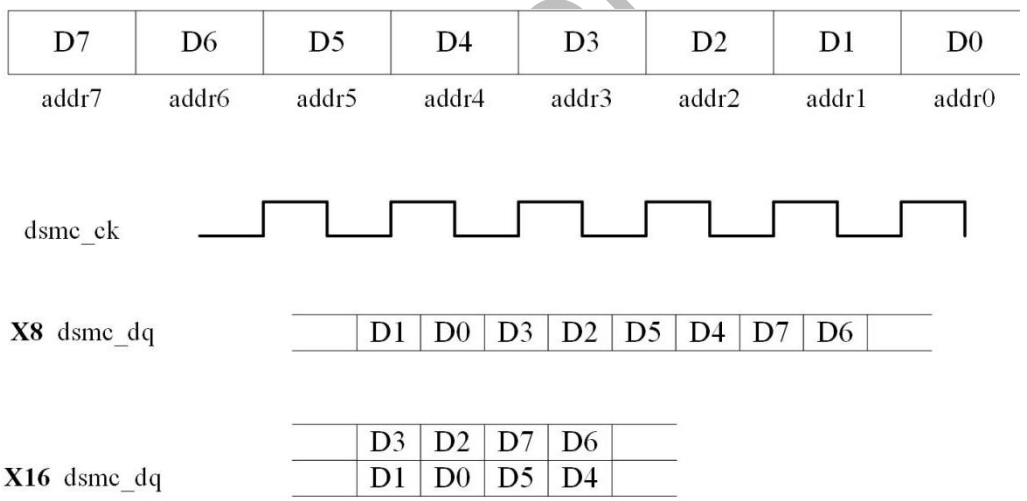

Fig. 36-6 Data mapping relationship between memory and DSMC interface

36.6.6 Merge Operation

The merge operation function supports Hyper device and Localbus device, and it is configured by the DSMC_MRGTCRx register.

- Merge operation removes address output period and latency cycles for subsequent transaction.
- When DSMC Memory Controller IP accepts subsequent read transaction with continuous address, it is merged to one CS# period on DSMC memory interface.

36.6.7 Timing Adjustment

This section describes the DSMC timing adjustment. DSMC core has timing adjustment circuit and timing adjustment is controlled by DSMC_MTRn. RCSHI, RCSS, and RCSH in DSMC_MTRn are used for the read timing adjustment, and WCSHI, WCSS, and WCSH in DSMC_MTRn are used for the write timing adjustment.

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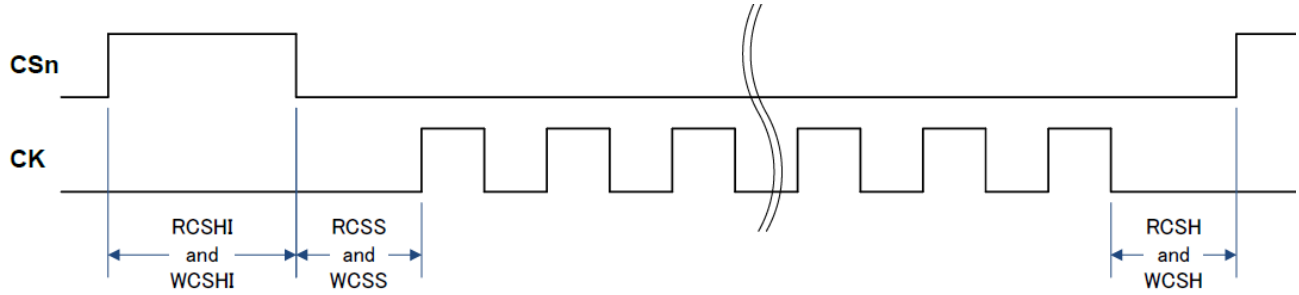

Fig. 36-7 Timing Adjustment

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Chapter 37 FlexBUS

37.1 Overview

FlexBUS is an AHB slave device. FlexBUS can achieve high-speed IO toggle and imitate some irregular or standards protocols. There are four possible combinations for the serial clock phase and polarity. The chip select signal (csn) is held high when the FlexBUS is idle or disabled. There are two channels which are transmission channel and receiving channel in FlexBUS. Therefore, FlexBUS can support both transmitting and receiving simultaneously. The flexbus0_clk, flexbus0_csn and flexbus0_data ports can be used for transmission channel and receiving channel. The flexbus1_clk, flexbus1_csn and flexbus1_data ports can only be used for receiving channel.

FlexBUS Controller supports the following features:

- Support for built-in DMA and ping-pong operation for allocating two address
- Support for filling in all 0 if the last DMA burst is less than 32Bytes or 64Bytes in receiving mode
- Support timeout interrupt of DMA response
- The direction of flexbus0_data port is I/O, flexbus0_data port can be used for transmission and receiving operation. The direction of flexbus1_data port is Input, flexbus1_data port can only be used for receiving operation
- Support for four working modes
    - Flexbus0_data port is used for transmission channel and receiving channel, flexbus0_clk port is used for transmission channel and receiving channel, supporting three mode: transmit only, receive only, transmission then receive
    - Flexbus0_data port is only used for transmission channel, flexbus0_clk port is used for transmission channel and receiving channel, supporting four mode: transmit only, receive only, transmission then receive, transmission and receive
    - Flexbus0_data port is only used for transmission channel, flexbus0_clk port is only used for transmission channel, supporting three mode: transmit only, receive only, transmission and receive
- Support software configuration and following data for csn port
- Support the image format of BT601 YUV422 and RGB565
- Support image cropping function
- Support clock port two modes, free running and following data mode
    - Free running mode
        - Txfifo is empty and supports the following two processing modes

    1) Stop transmission, pull up csn and send abnormal interruption
    2) Data, csn remain unchanged and clock hold toggle, send abnormal interruption

        - Rxfifo is pre-full

    1) Stop transmission, pull up csn and send abnormal interruption

    - Following data mode
        - Txfifo is empty and supports the following two processing modes

    1) Stop transmission, pull up csn and send abnormal interruption
    2) Data, csn and clock remain unchanged, send abnormal interruption

        - Rxfifo is pre-full and supports the following two processing modes

    1) Stop transmission, pull up csn and send abnormal interruption
    2) Data, csn and clock remain unchanged, send abnormal interruption
- Support single mode and continuous mode. Continuous mode can not support transmission then receive mode
- Support configurable four possible combinations for the clock port polarity and phase
- Support 2,4,8,16bits parallel data transfer
- Support clk port masking function
- Support the maximum of clock port up to 100MHz in transmission mode and receive mode
- Support software configuration modification of sampling points

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37.2 Block Diagram

The FlexBUS Controller comprises with:

- AHB_CFG
  The AHB_CFG contains control registers of transmitters and receiver.
- AXI Master Interface and DMA Controller
  The AXI Master Interface and DMA Controller implement for reading data from DDR and writing data to DDR.
- Engine
  The Engine implements control over all modules and monitor the generation of abnormal interrupts.
- IOBUF
  The IOBUF implements logic of data, csn and clock port.
- TX and RX FIFO

The TX FIFO is the buffer to store transmitted data. The TX FIFO is the buffer to store received data. The size of the TX and RX FIFO is 32bits x 512

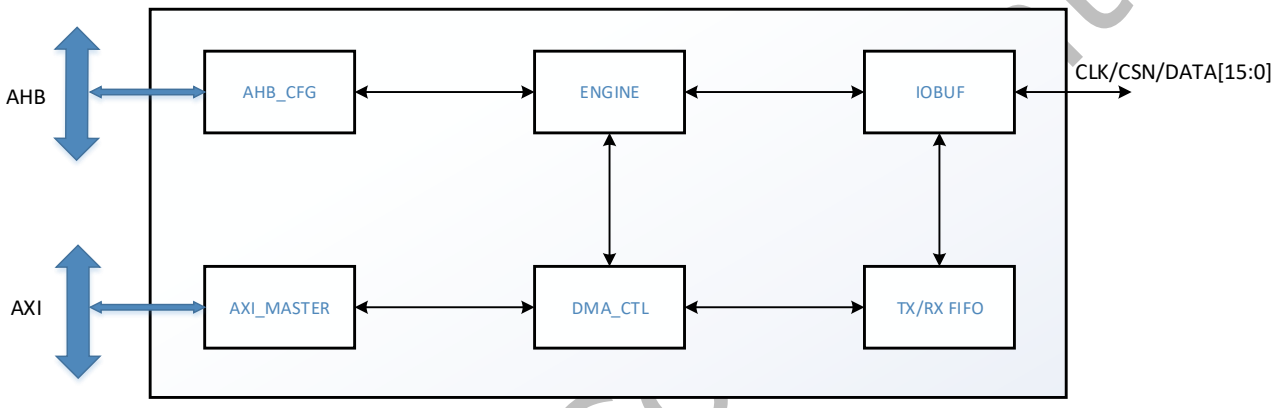

Fig. 37-1 FlexBUS Controller Block diagram

37.3 Function Description

37.3.1 Transfer Modes

According to multiplexed of flexbus0_data and flexbus0_clk ports, FlexBUS can be divided into different working modes. The following table shows the ports in different transfer modes.

Table 37-1 FlexBUS Tranfer Modes Port List

com_ctl[3:2]	tx only	rx only	tx and rx	tx then rx
2'b11	flexbus0_data/ flexbus0_clk/ flexbus0_csn/	flexbus0_data/ flexbus0_clk/ flexbus0_csn/	not support	flexbus0_data/ flexbus0_clk flexbus0_csn
2'b01		flexbus1_data/ flexbus0_clk/ flexbus0_csn	flexbus0_data/flexbus1_data flexbus0_clk/ flexbus0_csn/	flexbus0_data/flexbus1_data flexbus0_clk flexbus0_csn
2'b00		flexbus1_data/ flexbus1_clk1/ flexbus1_csn/	flexbus0_data/flexbus1_data flexbus0_clk/flexbus1_clk1 flexbus0_csn/flexbus1_csn	not support

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37.3.2 Free Running

flexbus0/1_clk can output earlier than csn begin active in free running mode. flexbus0/1_clk can output as soon as FLEXBUS_FREE_SCLK is configured to 1. When FLEXBUS_FREE_SCLK is configured to 0, flexbus0/1_clk will follow data after csn being active.

37.3.3 Single and Continuous Mode

37.3.3.1 Single Mode

In this mode, the amount of data transmitted or received is determined by FLEXBUS_TX_NUM/RX_NUM. FlexBUS will stop and send interrupt when the amount of data transmitted or received reaches the FLEXBUS_TX_NUM/RX_NUM. The address of transmission is FLEXBUS_DMA_SRC_ADDR0/DMA_DST_ADDR0. If the value of FLEXBUS_TX_NUM/RX_NUM is greater than FLEXBUS_DMA_SRC_LEN0/DMA_DST_LEN0, FlexBUS will automatically jump to FLEXBUS_DMA_SRC_ADDR1/DMA_DST_ADDR1 after FLEXBUS_DMA_SRC_ADDR0/ DMA_DST_ADDR0 is full. So it is recommended that the value of FLEXBUS_TX_NUM/RX_NUM is smaller than FLEXBUS_DMA_SRC_LEN0/DMA_DST_LEN0 in single mode.

37.3.3.2 Continuous Mode

In continuous mode, FlexBUS keeps working until the value of FLEXBUS_STOP is set and FLEXBUS_RX_NUM/TX_NUM will be ignored. FlexBUS will send interrupt when FLEXBUS_STOP is set. The user can configures two buffer which buffer0 is configured by FLEXBUS_DMA_SRC_ADDR0/DMA_DST_ADDR0 and FLEXBUS_DMA_SRC_LEN0/DMA_DST_LEN0, buffer1 is configured by FLEXBUS_DMA_SRC_ADDR1/DMA_DST_ADDR1 and FLEXBUS_DMA_SRC_LEN1/DMA_DST_LEN1. After the amount of data transmitted and received reaches the value of buffer0, FlexBUS will automatically jump to buffer1 and the user can configure new address of buffer0 and clear buffer0 interrupt status. Similarly, FlexBUS will automatically jump to buffer0 and the user can configure new address of buffer1 and clear buffer1 interrupt status after the amount of data transmitted and received reaches the value of buffer1.

37.3.4 CPOL and CPHA

The clock polarity (CPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. This is same as SPI. To transmit data, both FlexBUS and peripherals must have identical serial clock phase (CPHA) and clock polarity (CPOL) values. The data frame can be 2/4/8/16 bits in length.

When the configuration parameter CPHA = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the data lines prior to the first serial clock edge. The following two figures show a timing diagram for FlexBUS data transfer with CPHA = 0. The serial clock is shown for configuration parameters CPOL = 0 and CPOL = 1.

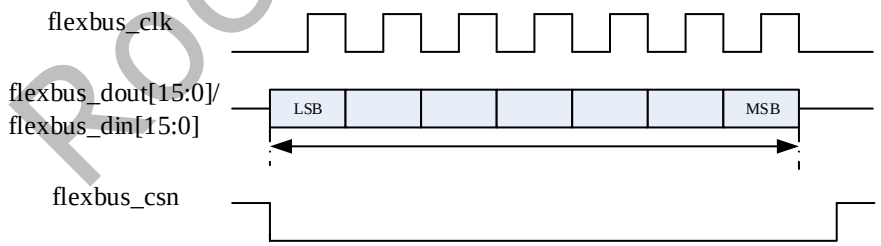

Fig. 37-2 FlexBUS Format (CPHA=0 CPOL=0)

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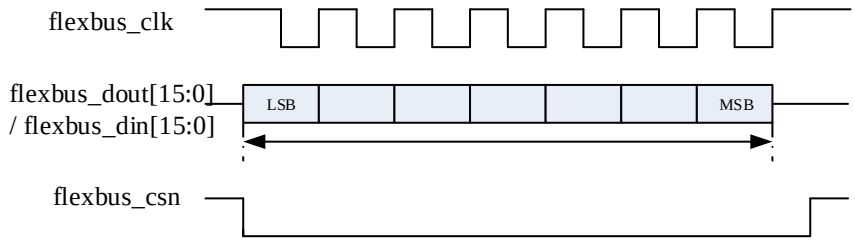

Fig. 37-3 FlexBUS Format (CPHA=0 CPOL=1)

When the configuration parameter CPHA = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the FlexBUS format when the configuration parameter CPHA = 1.

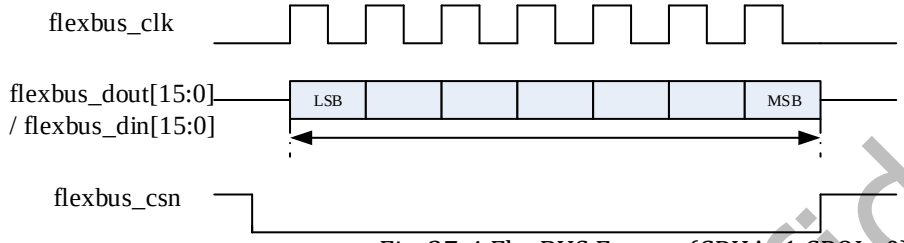

Fig. 37-4 FlexBUS Format (CPHA=1 CPOL=0)

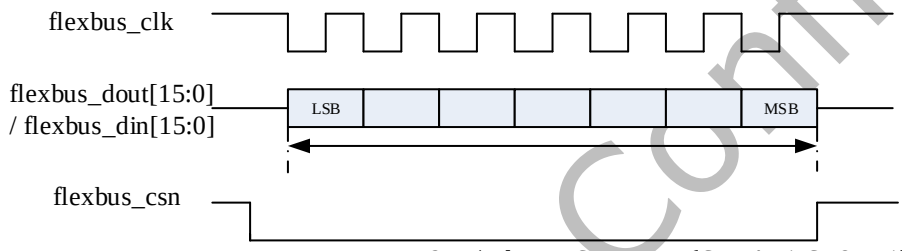

Fig. 37-5 FlexBUS Format (CPHA=1 CPOL=1)

37.3.5 TX Then RX Mode

CPHA=1, CPOL=0, transmit data at the posedge of CLKA and receive data at the negedge of CLKA. At T2, the last data is transmitted, and at T3, data pad would change to input. When FLEXBUS_RXCLK_DUMMY[4:0]=0, at T3 negedge of CLKA, rx logic would sample data; when FLEXBUS_RXCLK_DUMMY[4:0]=1, at T4 negedge of CLKA, rx logic would sample data.

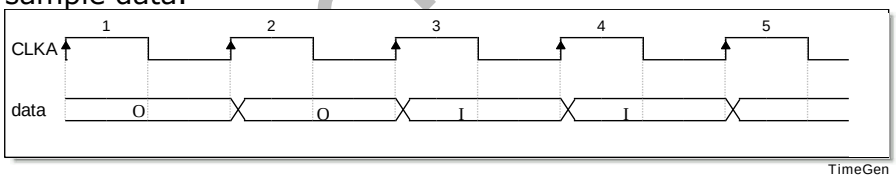

Fig. 37-6 FlexBUS TX Then RX Mode (CPHA=1 CPOL=0)

37.3.6 DVP Slave Mode

37.3.6.1 Support Vsync high active or low active

Vsync Low active

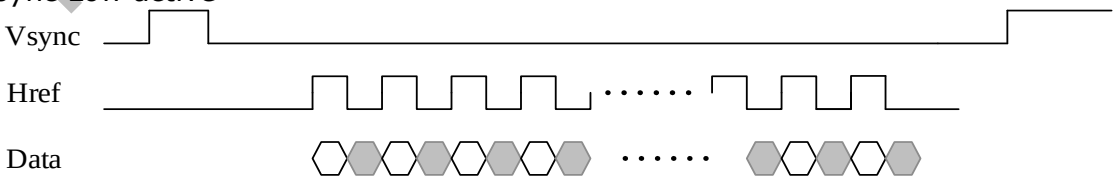

Fig. 37-7 Timing diagram when vsync low active

Vsync High active

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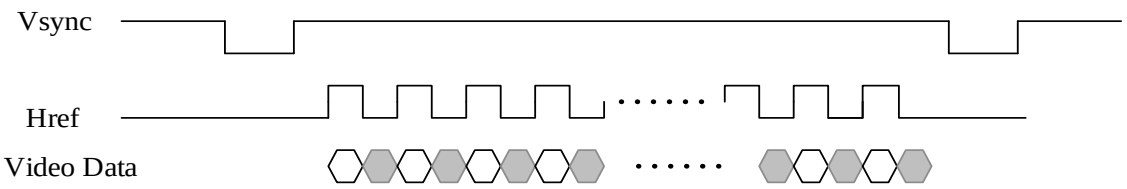

Fig. 37-8 Timing diagram when vsync high active

37.3.6.2 Support Href High Active or Low Active

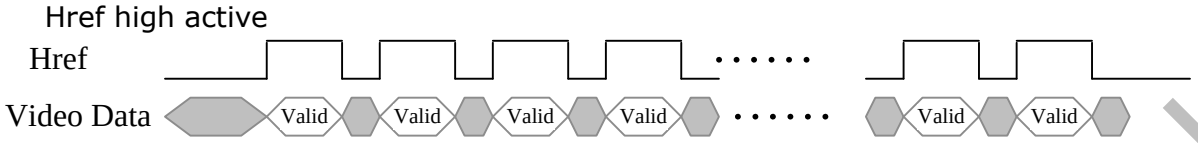

Fig. 37-9 Timing diagram when href high active

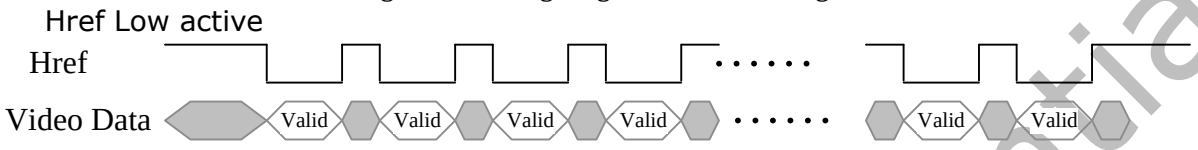

Fig. 37-10 Timing diagram when href low active

37.3.6.3 Data Format

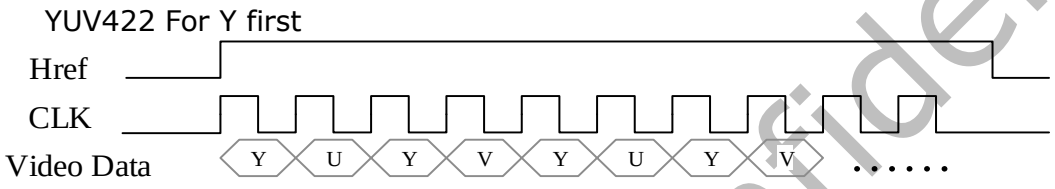

Fig. 37-11 Timing diagram when Y data first

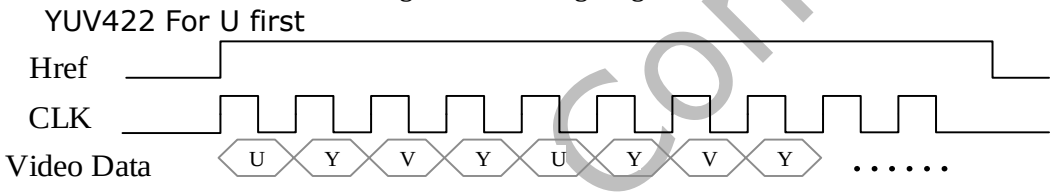

Fig. 37-12 Timing diagram when U data first

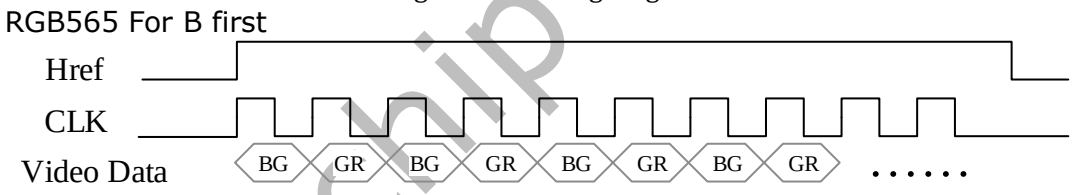

Fig. 37-13 Timing diagram when U data first

37.3.6.4 One Frame Stop Mode

In this mode, configure the register FLEXBUS_RX_CTL to one frame stop mode. After one frame captured, FlexBUS will automatic stop and send interrupt. FlexBUS will not capture the sensor data. The address of Y/UV is DMA_DST_ADDR0.

37.3.6.5 Frame Ping-Pong Mode

After one frame(F0) captured, FlexBUS will jump to buffer1 and start to capture the next frame(F1) automatically, and host must assign new address pointer of frame0 and clear the frame0 status, thus FlexBUS will capture the third frame automatically(by new F0 address) without any stop and so on for the following frames.

37.3.6.6 Storage

Y/UV data or R/G/B data will be storage in the same buffer. In addition, the amount of data in a row must be an integer multiple of 4Bytes.

37.3.6.7 Crop

The register FLEXBUS_DVP_CROP_START defines the coordinate of crop start point. And the frame size after cropping is following the value of FLEXBUS_DVP_CROP_SIZE.

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37.4 Register Description

37.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

37.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
FLEXBUS_ENR	0x0000	W	0x00000000	Enable Register
FLEXBUS_FREE_SCLK	0x0004	W	0x00000000	Sclk Free Register
FLEXBUS_CSN_CFG	0x0008	W	0x00000000	Csn Config Register
FLEXBUS_COM_CTL	0x000C	W	0x00000004	Common Control Register
FLEXBUS_REMAP	0x0010	W	0x00000000	Data Io Remap Register
FLEXBUS_STOP	0x0014	W	0x00000000	Continue Mode Stop Register
FLEXBUS_SLAVE_MODE	0x0018	W	0x00000001	Slave Mode Register
FLEXBUS_DVP_POL	0x001C	W	0x00000000	DVP Interface Register
FLEXBUS_DVP_CROP_SIZE	0x0020	W	0x00000000	The expected width and height of received image
FLEXBUS_DVP_CROP_START	0x0024	W	0x00000000	The start point of DVP path cropping
FLEXBUS_DVP_ORDER	0x0028	W	0x00000000	YVYU422 Mode Order
FLEXBUS_TX_CTL	0x0040	W	0x00000000	Tx Control Register
FLEXBUS_TX_DATA_NUM	0x0044	W	0x00000000	Tx Length Register
FLEXBUS_TXWAT_START	0x0048	W	0x00000000	Waterline To Start Transmission Register
FLEXBUS_TXFIFO_DNUM	0x004C	W	0x00000000	Transmit FIFO Level
FLEXBUS_TX_WIDTH	0x0050	W	0x00000000	The expected width of image
FLEXBUS_TX_CSN_DUMMY	0x0054	W	0x00000000	Csn Inactive Counter
FLEXBUS_TX_CMD_LEN	0x0058	W	0x00000000	Tx Command Width
FLEXBUS_TX_CMD0	0x005C	W	0x00000000	Tx Command0 Register
FLEXBUS_TX_CMD1	0x0060	W	0x00000000	Tx Command1 Register
FLEXBUS_RX_CTL	0x0080	W	0x00000000	Rx Control Register
FLEXBUS_RX_NUM	0x0084	W	0x00000000	Rx Length Register
FLEXBUS_RXFIFO_DNUM	0x0088	W	0x00000000	Receive FIFO Level
FLEXBUS_DLL_EN	0x008C	W	0x00000000	Delayline Enable Register
FLEXBUS_DLL_NUM	0x0090	W	0x00000000	Delayline Number Register
FLEXBUS_RXCLK_DUMMY	0x0094	W	0x00000000	RX CLK Dummy Register
FLEXBUS_RXCLK_CAP_CNT	0x0098	W	0x00000000	RX Capture Counter Register
FLEXBUS_DMA_RD_OUTSTD	0x0100	W	0x0000000F	DMA Read Outstanding Register
FLEXBUS_DMA_WR_OUTSTD	0x0104	W	0x0000000F	DMA Write Outstanding Register
FLEXBUS_DMA_SRC_ADDR0	0x0108	W	0x00000000	DMA Source Address0 Register
FLEXBUS_DMA_DST_ADDR0	0x010C	W	0x00000000	DMA Destination Address0 Register
FLEXBUS_DMA_SRC_ADDR1	0x0110	W	0x00000000	DMA Source Address1 Register
FLEXBUS_DMA_DST_ADDR1	0x0114	W	0x00000000	DMA Destination Address1 Register
FLEXBUS_DMA_SRC_LEN0	0x0118	W	0x00000000	DMA Source Address0 Size Register
FLEXBUS_DMA_DST_LEN0	0x011C	W	0x00000000	DMA Destination Address0 Size Register

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Name	Offset	Size	Reset Value	Description
FLEXBUS_DMA_SRC_LEN1	0x0120	W	0x00000000	DMA Source Address1 Size Register
FLEXBUS_DMA_DST_LEN1	0x0124	W	0x00000000	DMA Source Address0 Size Register
FLEXBUS_DMA_WAT_INT	0x0128	W	0x00000000	DMA Watermark Register
FLEXBUS_DMA_TIMEOUT	0x012C	W	0x00000000	DMA Timeout Register
FLEXBUS_DMA_RD_LEN	0x0130	W	0x00000000	DMA Read Burst Length
FLEXBUS_STATUS	0x0160	W	0x00000000	Status Register
FLEXBUS_IMR	0x0164	W	0x00000000	Interrupt Mask
FLEXBUS_RISR	0x0168	W	0x00000000	Raw Interrupt Status
FLEXBUS_ISR	0x016C	W	0x00000000	Interrupt Status
FLEXBUS_ICR	0x0170	W	0x00000000	Interrupt Clear
FLEXBUS_REVISION	0x01F0	W	0x000906F7	Svn Revision

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

37.4.3 Detail Registers Description

FLEXBUS_ENR

Address: Operational Base(0x2A2F0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	rx_enr Enables and disables all rx logic operations. Receive FIFO buffers are cleared when rx logic is disabled. 1'b1: Enable 1'b0: Disable
0	RW	0x0	tx_enr Enables and disables all tx logic operations. Transmit FIFO buffers are cleared when tx logic is disabled. 1'b1: Enable 1'b0: Disable

FLEXBUS_FREE_SCLK

Address: Operational Base(0x2A2F0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	rx_free_mode If set to 1, rx 1xclk output in advance, not following data.
0	RW	0x0	tx_free_mode If set to 1, tx 1xclk output in advance, not following data.

FLEXBUS_CSN_CFG

Address: Operational Base(0x2A2F0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:16	RW	0x0	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	rx_csn_cfg 1'b1: If set to 1, rx csn is active low in advance. 1'b0: Rx csn follows data.
0	RW	0x0	tx_csn_cfg 1'b1: If set to 1, tx csn is active low in advance. 1'b0: Tx csn follows data.

FLEXBUS_COM_CTL

Address: Operational Base(0x2A2F0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	rxfifo_expand If set to 1, txfifo would be used for rxfifo in rx only mode. The capacity of rxfifo would be doubled to the original.
4	RW	0x0	txfifo_expand If set to 1, rxfifo would be used for txfifo in tx only mode. The capacity of txfifo would be doubled to the original.
3	RW	0x0	tx_use_rx If set to 1, tx data channel will be used for rx data channel.
2	RW	0x1	sclk_share If set to 1, rx logic and tx logic use the same 2xclk and 1xclk.
1:0	RW	0x0	tx_rx_mode Transmit and receive mode select. 2'b00 : Transmit & Receive 2'b01 : Transmit Only 2'b10 : Receive Only 2'b11 : Transmit first, and then change to receive

FLEXBUS_REMAP

Address: Operational Base(0x2A2F0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	rx_data_remap When rx_dfs=0, 3'b000: Din[1:0] PAD input valid. 3'b001: Din[3:2] PAD input valid. 3'b010: Din[5:4] PAD input valid. 3'b011: Din[7:6] PAD input valid. 3'b100: Din[9:8] PAD input valid. 3'b101: Din[11:10] PAD input valid. 3'b110: Din[13:12] PAD input valid. 3'b111: Din[15:14] PAD input valid. When rx_dfs=1, 3'b000: Din[3:0] PAD input valid. 3'b001: Din[7:4] PAD input valid. 3'b010: Din[11:8] PAD input valid. 3'b011: Din[15:12] PAD input valid. Reserved. When rx_dfs=2, 3'b000: Din[7:0] PAD input valid. 3'b001: Din[15:8] PAD input valid. Reserved. When rx_dfs=3, 3'b000: Din[15:0] PAD input valid. Reserved.
3	RO	0x0	reserved
2:0	RW	0x0	tx_data_remap When tx_dfs=0, 3'b000: Dout[1:0] PAD output valid. 3'b001: Dout[3:2] PAD output valid. 3'b010: Dout[5:4] PAD output valid. 3'b011: Dout[7:6] PAD output valid. 3'b100: Dout[9:8] PAD output valid. 3'b101: Dout[11:10] PAD output valid. 3'b110: Dout[13:12] PAD output valid. 3'b111: Dout[15:14] PAD output valid. When tx_dfs=1, 3'b000: Dout[3:0] PAD output valid. 3'b001: Dout[7:4] PAD output valid. 3'b010: Dout[11:8] PAD output valid. 3'b011: Dout[15:12] PAD output valid. Reserved. When tx_dfs=2, 3'b000: Dout[7:0] PAD output valid. 3'b001: Dout[15:8] PAD output valid. Reserved. When tx_dfs=3, 3'b000: Dout[15:0] PAD output valid. Reserved.

FLEXBUS_STOP

Address: Operational Base(0x2A2F0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/W SC	0x0	rx_stop In rx continue mode, used to stop receive.
0	R/W SC	0x0	tx_stop If set to 1, it used to stop transmit in continue mode.

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FLEXBUS_SLAVE_MODE
Address: Operational Base(0x2A2F0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dvp_sel 1'b0: Work as adc 1'b1: Work as dvp interface
0	RW	0x1	clk1_in If set to 1, rx logic uses flexbus_clk1_in as the 2xclk.

FLEXBUS_DVP_POL
Address: Operational Base(0x2A2F0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	href_pol 1'b1: High active. 1'b0: Low active.
0	RW	0x0	vsync_pol 1'b1: High active. 1'b0: Low active.

FLEXBUS_DVP_CROP_SIZE
Address: Operational Base(0x2A2F0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_height The expected height of received image.
15:0	RW	0x0000	sw_width The expected width of received image. The value of the register is equal to the number of bytes. So if one pixel is equal to 2bytes, the value of the register is double to width of image.

FLEXBUS_DVP_CROP_START
Address: Operational Base(0x2A2F0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_start_y The vertical ordinate of the start point.
15:0	RW	0x0000	sw_start_x The horizontal ordinate of the start point. The value of the register is equal to the number of bytes. So if one pixel is equal to 2bytes, the value of the register is double to width of image.

FLEXBUS_DVP_ORDER
Address: Operational Base(0x2A2F0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	out_order 2'b00: YVYU 2'b01: VYUY 2'b10: YUYV 2'b11: UYVY
1:0	RW	0x0	in_order 2'b00: YVYU 2'b01: VYUY 2'b10: YUYV 2'b11: UYVY

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FLEXBUS_TX_CTL
Address: Operational Base(0x2A2F0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	cmd_width Command and address line width. 1'b0: x1 mode. 1'b1: x4 mode.
11	RW	0x0	multi_line 1'b1: Multi-line transmission and csn auto switching is enable. 1'b1: Multi-line transmission and csn auto switching is disable.
10:9	RW	0x0	csn_pos_cnt_cfg The register should be configured to define the number of the 2xclk cycles between csn inactive and data stop transmission. Unit is 2xclk. 2'b00: 2 cycles delay 2'b01: 3 cycles delay 2'b10: 4 cycles delay 2'b11: 5 cycles delay
8:7	RW	0x0	csn_neg_cnt_cfg The register should be configured to define the number of the 1xclk cycles between csn active and data active. Unit is 1xclk. 2'b00: Do not delay 2'b01: half cycle delay 2'b10: one cycles delay 2'b11: one and half cycles delay
6	RW	0x0	cutoff_cfg Cutoff function enable/disable. When txfifo is empty, tx logic will stop 1xclk until txfifo is not empty. 1'b1: Enable 1'b0: Disable
5	RW	0x0	1xclk_mask 1xclk mask enable/disable. 1'b1: Enable 1'b0: Disable
4	RW	0x0	continue_mode Continue mode enable/disable. 1'b1: Enable 1'b0: Disable
3	RW	0x0	cpol 1'b0: Inactive state of 1xclk is low. 1'b1: Inactive state of 1xclk is high.
2	RW	0x0	cpha 1'b0: 1xclk toggles in middle of first data bit. 1'b1: 1xclk toggles at start of first data bit.
1:0	RW	0x0	data_width Selects the data frame length. 2'b00: 2bit data 2'b01: 4bit data 2'b10: 8bit data 2'b11: 16bit data

FLEXBUS_TX_DATA_NUM
Address: Operational Base(0x2A2F0000) + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	num The register field sets the number of data frames to transmit. The Flexbus continues to transmit data until the number of data frames transmited is equal to this register value. Unit is data_width.

FLEXBUS_TXWAT_START

Address: Operational Base(0x2A2F0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	txfifo_wat_start When the number of words in transmit FIFO is more than or equal to this value, the transmit logic starts work. Unit is word.

FLEXBUS_TXFIFO_DNUM

Address: Operational Base(0x2A2F0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	dnum Contains the number of valid data entries in the transmit FIFO. Unit is word.

FLEXBUS_TX_WIDTH

Address: Operational Base(0x2A2F0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	width_size In tx multi-line mode, the number of data will be transmitted when cs is low at one time, excluding command length. Unit is data_width.

FLEXBUS_TX_CSN_DUMMY

Address: Operational Base(0x2A2F0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	csn_dummy The register should be configured to define the number of the 2xclk cycles between csn inactive and csn active. Unit is 2xclk.

FLEXBUS_TX_CMD_LEN

Address: Operational Base(0x2A2F0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	cmd_len The number of data will be transmitted in one wire mode. Unit is bit. The minimum configured value should be greater than 1.

FLEXBUS_TX_CMD0

Address: Operational Base(0x2A2F0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd0 Data used to transmit in one wire mode.

FLEXBUS_TX_CMD1

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Address: Operational Base(0x2A2F0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd1 Data used to transmit in one wire mode.

FLEXBUS_RX_CTL

Address: Operational Base(0x2A2F0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	shift 1'b0: First parallel bit is LSB in shift register. 1'b1: First parallel bit is MSB in shift register.
14	RW	0x0	auto_pad When the remaining number of data entries in rx fifo is less than one burst data of dma, the dma request will not be set high, but if this bit set to 1, the dma request will be raised, and 0 will be automatically added to make up for the data volume.
13:9	RW	0x00	csn_pos_cnt_cfg The register should be configured to define the number of the 2xclk cycles between csn inactive and data stop receiving. Unit is 2xclk. 5'b00: 1 cycle delay 5'b01: 2 cycles delay 5'b10: 3 cycles delay 5'b11: 4 cycles delay 5'h1f: Max 32 cycles delay
8:7	RW	0x0	csn_neg_cnt_cfg The register should be configured to define the number of the 1xclk cycles between csn active and data active. 2'b00: Do not delay 2'b01: half cycle delay 2'b10: one cycles delay 2'b11: one and half cycles delay
6	RW	0x0	cutoff_cfg Cutoff function enable/disable. When rxfifo is full, rx logic will stop 1xclk until rxfifo is not full. 1'b1: Enable 1'b0: Disable
5	RW	0x0	rxd_dy If the rxd data cannot be sampled by the sclk edge at the right time, this register should be configured to define the number of the 2xclk cycles after the active 1xclk edge to sample rxd data later when flexbus works at high frequency. Unit is 2xclk. 1'b0: Do not delay 1'b1: One cycle delay
4	RW	0x0	continue_mode Continue mode enable/disable. 1'b1: Enable 1'b0: Disable
3	RW	0x0	cpol 1'b0: Inactive state of 1xclk is low. 1'b1: Inactive state of 1xclk is high.
2	RW	0x0	cpha 1'b0: 1xclk toggles in middle of first data bit. 1'b1: 1xclkl clock toggles at start of first data bit.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	data_width Selects the data frame length. 2'b00: 2bit data 2'b01: 4bit data 2'b10: 8bit data 2'b11: 16bit data

FLEXBUS_RX_NUM

Address: Operational Base(0x2A2F0000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	num The register field sets the number of data frames to receive. The flexbus continues to receive data until the number of data frames transmited is equal to this register value. This value contains rx_clk_dummy. Unit is data_width.

FLEXBUS_RXFIFO_DNUM

Address: Operational Base(0x2A2F0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	dnum Contains the number of valid data entries in the receive FIFO. Unit is word.

FLEXBUS_DLL_EN

Address: Operational Base(0x2A2F0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	enable If set to 1, rx delayline clk is enable.

FLEXBUS_DLL_NUM

Address: Operational Base(0x2A2F0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
6:0	RW	0x00	num The number steps of delayline.

FLEXBUS_RXCLK_DUMMY

Address: Operational Base(0x2A2F0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	rx_clk_dummy In tramsmit then receive mode, this register should be configured to define the number of the 1xclk cycles after transmit operation finish to sample rx data. Unit is 1xclk.

FLEXBUS_RXCLK_CAP_CNT

Address: Operational Base(0x2A2F0000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	rx_cap_cnt Used to define the position of the first data being captured. Unit is 1xclk.

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FLEXBUS_DMA_RD_OUTSTD
Address: Operational Base(0x2A2F0000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x0f	read_outstanding Dma read outstanding is equal to (register + 1).

FLEXBUS_DMA_WR_OUTSTD
Address: Operational Base(0x2A2F0000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x0f	write_outstanding Dma write outstanding is equal to (register + 1).

FLEXBUS_DMA_SRC_ADDR0
Address: Operational Base(0x2A2F0000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_addr0 The first source address. The address is 4Byte alignment. Unit is 4Byte. So the register value is equal to 1, dma source address is equal to 30'h04.

FLEXBUS_DMA_DST_ADDR0
Address: Operational Base(0x2A2F0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_addr0 The first destination address. Unit is 4Byte.

FLEXBUS_DMA_SRC_ADDR1
Address: Operational Base(0x2A2F0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	src_addr1 The second source address. Unit is 4Byte.

FLEXBUS_DMA_DST_ADDR1
Address: Operational Base(0x2A2F0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dst_addr1 The second destination address. Unit is 4Byte.

FLEXBUS_DMA_SRC_LEN0
Address: Operational Base(0x2A2F0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:6	RW	0x000000	src_len0 The size of first source address. Unit is byte.
5:0	RO	0x00	reserved

FLEXBUS_DMA_DST_LEN0
Address: Operational Base(0x2A2F0000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:6	RW	0x000000	dst_len0 The size of first destination address. Unit is byte.
5:0	RO	0x00	reserved

FLEXBUS_DMA_SRC_LEN1
Address: Operational Base(0x2A2F0000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:6	RW	0x000000	src_len1 The size of second source address. Unit is byte.
5:0	RO	0x00	reserved

FLEXBUS_DMA_DST_LEN1
Address: Operational Base(0x2A2F0000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:6	RW	0x000000	dst_len1 The size of second destination address. Unit is byte.
5:0	RO	0x00	reserved

FLEXBUS_DMA_WAT_INT
Address: Operational Base(0x2A2F0000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	src_wat_lvl Used to config the watermark interrupt of read buffer0 and buffer1. 2'b00: The amount of data read from ddr is up to one-quarter of the size of source address. 2'b00: The amount of data read from ddr is up to half of the size of source address. 2'b10 or 2'b11: The amount of data read from ddr is up to the size of source address.
1:0	RW	0x0	dst_wat_lvl Used to config the watermark interrupt of write buffer0 and buffer1. 2'b00: The amount of data written to ddr is up to one-quarter of the size of destination address. 2'b00: The amount of data written to ddr is up to half of the size of destination address. 2'b10 or 2'b11: The amount of data written to ddr is up to the size of destination address.

FLEXBUS_DMA_TIMEOUT
Address: Operational Base(0x2A2F0000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:1	RW	0x000	counter Unit is x16.
0	RW	0x0	en 1'b1: Timeout function is enable. 1'b0: Timeout function is disable.

FLEXBUS_DMA_RD_LEN
Address: Operational Base(0x2A2F0000) + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	burst_len8 1'b1: DMA read burst length is equal to 8. 1'b0: DMA read burst length is equal to 16.

FLEXBUS_STATUS

Address: Operational Base(0x2A2F0000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	dst_dma_busy 1'b0: Dma write operation is in idle. 1'b1: Dma write operation is busy.
6	RO	0x0	src_dma_busy 1'b0: Dma read operation is in idle. 1'b1: Dma read operation is busy.
5	RO	0x0	rx_empty 1'b0: Receive FIFO is not empty. 1'b1: Receive FIFO is empty.
4	RO	0x0	rx_full 1'b0: Receive FIFO is not full. 1'b1: Receive FIFO is full.
3	RO	0x0	tx_empty 1'b0: Transmit FIFO is not empty. 1'b1: Transmit FIFO is empty.
2	RO	0x0	tx_full 1'b0: Transmit FIFO is not full. 1'b1: Transmit FIFO is full.
1	RO	0x0	rx_busy When set, indicates that receive transfer is in progress; when cleared, indicates that the receive is idle or disabled.
0	RO	0x0	tx_busy When set, indicates that transmission transfer is in progress; when cleared, indicates that the transmission is idle or disabled.

FLEXBUS_IMR

Address: Operational Base(0x2A2F0000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	dma_timeout_im 1'b0: Timeout interrupt is masked. 1'b1: Timeout interrupt is not masked.
12	RW	0x0	dma_err_im 1'b0: Dma error response interrupt is masked. 1'b1: Dma error response interrupt is not masked.
11	RW	0x0	dma_dst1_im 1'b0: Dma write buffer1 interrupt is masked. 1'b1: Dma write buffer1 interrupt is not masked.
10	RW	0x0	dma_dst0_im 1'b0: Dma write buffer0 interrupt is masked. 1'b1: Dma write buffer0 interrupt is not masked.
9	RW	0x0	dma_src1_im 1'b0: Dma read buffer1 interrupt is masked. 1'b1: Dma read buffer1 interrupt is not masked.

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Bit	Attr	Reset Value	Description
8	RW	0x0	dma_src0_im 1'b0: Dma read buffer0 interrupt is masked. 1'b1: Dma read buffer0 interrupt is not masked.
7	RW	0x0	dvp_frame_start_im 1'b0: Frame start interrupt is masked. 1'b1: Frame start interrupt is not masked.
6	RW	0x0	dvp_frame_ab 1'b0: Frame abnormal interrupt is masked. 1'b1: Frame abnormal interrupt is not masked.
5	RW	0x0	rx_done_im 1'b0: receive finish interrupt is masked. 1'b1: receive finish interrupt is not masked.
4	RW	0x0	rx_udf_im 1'b0: rxfifo underflow interrupt is masked. 1'b1: rxfifo underflow interrupt is not masked.
3	RW	0x0	rx_ovf_im 1'b0: rxfifo overflow interrupt is masked. 1'b1: rxfifo overflow interrupt is not masked.
2	RW	0x0	tx_done_im 1'b0: transmission finish interrupt is masked. 1'b1: transmission finish interrupt is not masked.
1	RW	0x0	tx_udf_im 1'b0: txfifo underflow interrupt is masked. 1'b1: txfifo underflow interrupt is not masked.
0	RW	0x0	tx_ovf_im 1'b0: txfifo overflow interrupt is masked. 1'b1: txfifo overflow interrupt is not masked.

FLEXBUS_RISR

Address: Operational Base(0x2A2F0000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	dma_timeout_ris 1'b0: Dma timeout interrupt is not active prior to masking. 1'b1: Dma timeout interrupt is active prior to masking.
12	RO	0x0	dma_err_ris 1'b0: Dma error response interrupt is not active prior to masking. 1'b1: Dma error response interrupt is active prior to masking.
11	RO	0x0	dma_dst1_ris 1'b0: Dma write buffer1 interrupt is not active prior to masking. 1'b1: Dma write buffer1 interrupt is active prior to masking.
10	RO	0x0	dma_dst0_ris 1'b0: Dma write buffer0 interrupt is not active prior to masking. 1'b1: Dma write buffer0 interrupt is active prior to masking.
9	RO	0x0	dma_src1_ris 1'b0: Dma read buffer1 interrupt is not active prior to masking. 1'b1: Dma read buffer1 interrupt is active prior to masking.
8	RO	0x0	dma_src0_ris 1'b0: Dma read buffer0 interrupt is not active prior to masking. 1'b1: Dma read buffer0 interrupt is active prior to masking.
7	RO	0x0	dvp_frame_start_ris 1'b0: Frame start interrupt is not active prior to masking. 1'b1: Frame start interrupt is active prior to masking.

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Bit	Attr	Reset Value	Description
6	RO	0x0	dvp_frame_ab_ris 1'b0: Frame abnormal interrupt is not active prior to masking. 1'b1: Frame abnormal interrupt is active prior to masking.
5	RO	0x0	rx_done_ris 1'b0: receive finish interrupt is not active prior to masking. 1'b1: receive finish interrupt is active prior to masking.
4	RO	0x0	rx_udf_ris 1'b0: rxfifo underflow interrupt is not active prior to masking. 1'b1: rxfifo underflow interrupt is active prior to masking.
3	RO	0x0	rx_ovf_ris 1'b0: rxfifo overflow interrupt is not active prior to masking. 1'b1: rxfifo overflow interrupt is active prior to masking.
2	RO	0x0	tx_done_ris 1'b0: transmission finish interrupt is not active prior to masking. 1'b1: transmission finish interrupt is active prior to masking.
1	RO	0x0	tx_udf_ris 1'b0: txfifo underflow interrupt is not active prior to masking. 1'b1: txfifo underflow interrupt is active prior to masking.
0	RO	0x0	tx_ovf_ris 1'b0: txfifo overflow interrupt is not active prior to masking. 1'b1: txfifo overflow interrupt is active prior to masking.

FLEXBUS_ISR

Address: Operational Base(0x2A2F0000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	dma_timeout_is 1'b0: Dma timeout interrupt is not active after masking. 1'b1: Dma timeout interrupt is active after masking.
12	RO	0x0	dma_err_is 1'b0: Dma error response interrupt is not active after masking. 1'b1: Dma error response interrupt is active after masking.
11	RO	0x0	dma_dst1_is 1'b0: Dma write buffer1 interrupt is not active after masking. 1'b1: Dma write buffer1 interrupt is active after masking.
10	RO	0x0	dma_dst0_is 1'b0: Dma write buffer0 interrupt is not active after masking. 1'b1: Dma write buffer0 interrupt is active after masking.
9	RO	0x0	dma_src1_is 1'b0: Dma read buffer1 interrupt is not active after masking. 1'b1: Dma read buffer1 interrupt is active after masking.
8	RO	0x0	dma_src0_is 1'b0: Dma read buffer0 interrupt is not active after masking. 1'b1: Dma read buffer0 interrupt is active after masking.
7	RO	0x0	dvp_frame_start_is 1'b0: Frame start interrupt is not active after masking. 1'b1: Frame start interrupt is active after masking.
6	RO	0x0	dvp_frame_ab_is 1'b0: Frame abnormal interrupt is not active after masking. 1'b1: Frame abnormal interrupt is active after masking.
5	RO	0x0	rx_done_is 1'b0: receive finish interrupt is not active after masking. 1'b1: receive finish interrupt is active after masking.

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Bit	Attr	Reset Value	Description
4	RO	0x0	rx_udf_is 1'b0: rxfifo underflow interrupt is not active after masking. 1'b1: rxfifo underflow interrupt is active after masking.
3	RO	0x0	rx_ovf_is 1'b0: rxfifo overflow interrupt is not active after masking. 1'b1: rxfifo overflow interrupt is active after masking.
2	RO	0x0	tx_done_is 1'b0: transmission finish interrupt is not active after masking. 1'b1: transmission finish interrupt active after masking.
1	RO	0x0	tx_udf_is 1'b0: txfifo underflow interrupt is not active after masking. 1'b1: txfifo underflow interrupt is active after masking.
0	RO	0x0	tx_ovf_is 1'b0: txfifo overflow interrupt is not active after masking. 1'b1: txfifo overflow interrupt is active after masking.

FLEXBUS_ICR

Address: Operational Base(0x2A2F0000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	cci Write 1 to Clear Combined Interrupt.
30:14	RO	0x00000	reserved
13	R/W SC	0x0	ctimeout Write 1 to clear dma timeout interrupt.
12	R/W SC	0x0	cdma_err Write 1 to clear dma error response interrupt.
11	R/W SC	0x0	cdst1 Write 1 to clear dma write buffer1 interrupt.
10	R/W SC	0x0	cdst0 Write 1 to clear dma write buffer0 interrupt.
9	R/W SC	0x0	csrc1 Write 1 to clear dma read buffer1 interrupt.
8	R/W SC	0x0	csrc0 Write 1 to clear dma read buffer0 interrupt.
7	R/W SC	0x0	cframe_start Write 1 to clear dvp frame start interrupt.
6	R/W SC	0x0	crx_dvp_frame_ab Write 1 to clear frame abnormal interrupt.
5	R/W SC	0x0	crx_done Write 1 to clear receive finish interrupt.
4	R/W SC	0x0	crx_udf Write 1 to clear rxfifo underflow Interrupt.
3	R/W SC	0x0	crx_ovf Write 1 to clear rxfifo overflow Interrupt.
2	R/W SC	0x0	ctx_done Write 1 to clear transmission finish interrupt.
1	R/W SC	0x0	ctx_udf Write 1 to clear txfifo underflow Interrupt.
0	R/W SC	0x0	ctx_ovf Write 1 to clear txfifo overflow Interrupt.

FLEXBUS_REVISION

Address: Operational Base(0x2A2F0000) + offset (0x01F0)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0009	revision Function revision.
15:0	RO	0x06f7	svn Svn revision.

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

37.5 Interface Description

Table 37-2 FlexBUS interface description

Module Pin	Direction	Pin Name	IOMUX Setting
flexbus0_clk	O	VO_LCDC_D13/VO_EBC_SDDO13/ETH0_TXCLK_M0/DSMC_DQS1/FLEXBUS0_CLK/SPI3_CSN0_M1/PWM0_CH1_M3/GPIO3_B6_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[11:8] = 4'h6
flexbus0_csn_m0	O	VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 4'h8
flexbus0_csn_m1	O	VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/DSMC_INT2/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[7:4] = 4'h8
flexbus0_csn_m2	O	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 4'h6
flexbus0_csn_m3	O	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'h8
flexbus0_csn_m4	O	SPDIF_RX0_M0/FLEXBUS0_CSN_M4/UART2_RX_M1/I2C3_SDA_M0/CAN1_RX_M2/GPIO4_B4_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[3:0] = 4'h4
flexbus0_d0	I/O	VO_LCDC_D14/VO_EBC_SDDO14/ETH0_TXD0_M0/SPDIF_TX1_M0/DSMC_DATA8/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4] = 4'h6

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Module Pin	Direction	Pin Name	IOMUX Setting
flexbus0_d1	I/O	VO_LCDC_D15/VO_EBC_SDDO15/ETH0_TXD1_M0/SPDIF_RX1_M0/DSMC_DATA9/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[3:0] = 4'h6
flexbus0_d2	I/O	VO_LCDC_D16/VO_EBC_SDCE0/ETH0_TXCTL_M0/PDM1_SDI0_M2/DSMC_DATA10/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[15:12] = 4'h6
flexbus0_d3	I/O	VO_LCDC_D17/VO_EBC_SDCE1/ETH0_RXD0_M0/PDM1_SDI1_M2/DSMC_DATA11/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[11:8] = 4'h6
flexbus0_d4	I/O	VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4] = 4'h6
flexbus0_d5	I/O	VO_LCDC_D20/VO_EBC_VCOM/ETH0_RXCTL_M0/PDM1_CLK1_M2/DSMC_DATA13/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[15:12] = 4'h6
flexbus0_d6	I/O	VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8] = 4'h6
flexbus0_d7	I/O	VO_LCDC_D22/VO_EBC_GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[7:4] = 4'h6
flexbus0_d8	I/O	VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0] = 4'h6
flexbus0_d9	I/O	VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 4'h6
flexbus0_d10	I/O	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 4'h6

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Module Pin	Direction	Pin Name	IOMUX Setting
		1_M3/GPIO3_C3_d	
flexbus0_d11	I/O	VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[7:4] = 4'h6
flexbus0_d12	I/O	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'h6
flexbus0_d13_m0	I/O	SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0] = 4'h6
flexbus0_d13_m1	I/O	SAI4_SCLK_M0/PDM1_SDI3_M1/FLEXBUS0_D13_M1/SPI3_MOSI_M2/UART6_TX_M0/I2C4_SCL_M1/CAN0_TX_M2/GPIO4_A4_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[3:0] = 4'h4
flexbus0_d14_m0	I/O	VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/DSMC_INT2/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[7:4] = 4'h6
flexbus0_d14_m1	I/O	SAI4_LRCK_M0/PDM1_CLK0_M1/FLEXBUS0_D14_M1/SPI3_MISO_M2/UART6_RX_M0/I2C4_SDA_M1/CAN0_RX_M2/GPIO4_A6_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[11:8] = 4'h4
flexbus0_d15_m0	I/O	VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12] = 4'h6
flexbus0_d15_m1	I/O	SPDIF_TX0_M0/FLEXBUS0_D15_M1/UART2_TX_M1/I2C3_SCL_M0/PCIE0_CLKREQN_M2/CAN1_TX_M2/GPIO4_B5_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[7:4] = 4'h4
flexbus1_clk	I/O	VO_LCDC_VSYNC/VO_EBC_SDCLK/SAI1_SDI3_M1/DSMC_CLKN/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:8] = 4'h6

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Module Pin	Direction	Pin Name	IOMUX Setting
flexbus1_csn_m0	O	VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12] = 4'h8
flexbus1_csn_m1	O	VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12] = 4'h8
flexbus1_csn_m2	O	VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[7:4] = 4'h8
flexbus1_csn_m3	O	SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0] = 4'h8
flexbus1_csn_m4	O	SAI1_SCLK_M0/FLEXBUS1_CSN_M4/SPI3_CSN0_M2/UART5_RTSN_M1/I2C2_SCL_M2/PWM2_CH4_M1/GPIO4_A3_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[15:12] =4'h4
flexbus1_d0	I	VO_LCDC_HSYNC/VO_EBC_GDCLK/SAI1_SDI2_M1/DSMC_CLKP/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 4'h6
flexbus1_d1	I	VO_LCDC_DEN/VO_EBC_SDLE/SAI1_SDI1_M1/DSMC_DATA0/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'h6
flexbus1_d2	I	VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[15:12] = 4'h6
flexbus1_d3	I	VO_LCDC_D3/VO_EBC_SDDO3/SAI1_MCLK_M1/DSMC_DATA1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[3:0] = 4'h6
flexbus1_d4	I	VO_LCDC_D4/VO_EBC_SDDO4/SAI1_SCLK_M1/DSMC_DATA2/FLEXBUS1_D4/UART8_RT	TOP_IOC_GPIO3C_IOMUX_SEL_H[15:12] = 4'h6

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Module Pin	Direction	Pin Name	IOMUX Setting
		SN_M0/SPI1_CLK_M2/GPIO3_C7_d	
flexbus1_d5	I	VO_LCDC_D5/VO_EBC_SDDO5/SAI1_LRCK_M1/DSMC_DATA3/FLEXBUS1_D5/UART8_TX_M0/SPI1_MOSI_M2/GPIO3_C6_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[11:8] = 4'h6
flexbus1_d6	I	VO_LCDC_D6/VO_EBC_SDDO6/SAI1_SDO0_M1/DSMC_DATA4/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[7:4] = 4'h6
flexbus1_d7	I	VO_LCDC_D7/VO_EBC_SDDO7/SAI1_SDO1_M1/DSMC_DATA5/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/CAN0_TX_M3/GPIO3_C4_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[3:0] = 4'h6
flexbus1_d8	I	VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 4'h6
flexbus1_d9	I	VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/DSMC_DATA7/FLEXBUS1_D9/UART2_TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0] = 4'h6
flexbus1_d10	I	VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12] = 4'h6
flexbus1_d11	I	VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 4'h6
flexbus1_d12_m0	I	VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12] = 4'h7
flexbus1_d12_m1	I	SAI1_LRCK_M0/FLEXBUS1_D12_M1/SPI4_CSN1_M2/UART5_CTSN_M1/I2C2_SDA_M2/P	TOP_IOC_GPIO4A_IOMUX_SEL_H[7:4] = 4'h4

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Module Pin	Direction	Pin Name	IOMUX Setting
		CIE1_CLKREQN_M2/GPIO4_A5_d	
flexbus1_d13_m0	I	VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/DSMC_INT2/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[7:4] = 4'h7
flexbus1_d13_m1	I	SAI1_SDO1_M0/SAI1_SDI3_M0/PDM1_CLK1_M1/FLEXBUS1_D13_M1/SPI4_CLK_M2/UART5_TX_M1/UART6_RTSN_M0/UART2_RTSN_M1/GPIO4_B0_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[3:0] = 4'h4
flexbus1_d14_m0	I	SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/DSMC_INT0/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	TOP_IOC_GPIO4A_IOMUX_SEL_L[3:0] = 4'h7
flexbus1_d14_m1	I	SAI1_SDO2_M0/SAI1_SDI2_M0/PDM1_SDI2_M1/FLEXBUS1_D14_M1/SPI4_MOSI_M2/UART5_RX_M1/UART6_CTSN_M0/UART2_CTSN_M1/GPIO4_B1_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[7:4] = 4'h4
flexbus1_d15-m0	I	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'h7
flexbus1_d15-m1	I	SAI1_SDO3_M0/SAI1_SDI1_M0/PDM1_SDI1_M1/FLEXBUS1_D15_M1/SPI4_MISO_M2/MIPI_TE_M0/GPIO4_B2_d	TOP_IOC_GPIO4B_IOMUX_SEL_L[11:8] = 4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional.

37.6 Application Notes

Clock Ratios

The frequency of PAD is half of FlexBUS operation clock.When FlexBUS operation clock is 200MHz, the frequency of flexbus0_clk and flexbus1_clk is 100MHz.

FSPI Transfer Flow

If want to support FSPI feature, the configuration is showing as below:

A. Set VCCIO_IOC_MISC_CON0[8]=0 to as master; set modes, transmit then receive, FLEXBUS_COM_CTL[3:0]=4'hf;
B. Set RX CLK dummy counter, FLEXBUS_RXCLK_DUMMY;
C. Set Interrupt mask, FLEXBUS_IMR;
D. Set format of transmit data, FLEXBUS_TX_CTL;
E. Set tx start water line, FLEXBUS_TXWAT_START;
F. Set tx length, FLEXBUS_TX_NUM;

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G. Set format of receive data, FLEXBUS_RX_CTL;
H. Set rx length, FLEXBUS_RX_NUM;
I. Set DMA,FLEXBUS_DMA_SRC_ADDR0/DST_ADDR0/SRC_LEN0/DST_LEN0;
J. Set FlexBUS enable, FLEXBUS_ENR[1:0]=2'b11;

Wait Interrupt and clear interrupt;
Final, disable FlexBUS.

ADC with Sync CLKIN Transfer Flow

A. Set VCCIO_IOC_MISC_CON0[7] based on ADC interface timing and set VCCIO_IOC_MISC_CON0[8]=1 to as slave;
B. Set modes, rx only mode, FLEXBUS_COM_CTL[3:0]=4'h2;
C. Set Interrupt mask, FLEXBUS_IMR;
D. Set format of receive data, FLEXBUS_RX_CTL[4]=1, data frame configuration according to actual usage;
E. Set FLEXBUS_SLAVE_MODE=2'b01;
F. Set DMA;
G. Set FlexBUS enable, FLEXBUS_ENR[1]=1'b1;
H. Wait interrupt, if dma_dst0 is active indicating that buffer0 has finished and clear interrupt, FlexBUS can set new buffer0 address. FlexBUS will automatically jump to buffer1 address and capture new data; If don't want to receive data, set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
I. Wait interrupt, if dma_dst1 is active indicating that buffer1 has finished and clear interrupt, FlexBUS can set new buffer1 address. FlexBUS will automatically jump to buffer0 address and capture new data; If don't want to receive new data, Set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
J. If want to stop receiving data , set FlexBUS.STOP[1]=1 at any time and wait rx_done interrupt; final disable FlexBUS;
K. If want to continue to receive data, repeat H-I.

ADC without CLKIN Transfer Flow

A. Set VCCIO_IOC_MISC_CON0[8]=0;
B. Set modes, rx only mode, FLEXBUS_COM_CTL[3:0]=4'h2;
C. Set Interrupt mask, FLEXBUS_IMR;
D. Set format of receive data, FLEXBUS_RX_CTL[4]=1, data frame configuration according to actual usage;
E. Set DMA;
F. Set FlexBUS enable, FLEXBUS_ENR[1]=1'b1;
G. Wait interrupt, if dma_dst0 is active indicating that buffer0 has finished and clear interrupt, FlexBUS can set new buffer0 address. FlexBUS will automatically jump to buffer1 address and capture new data; If don't want to receive data, set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
H. Wait interrupt, if dma_dst1 is active indicating that buffer1 has finished and clear interrupt, FlexBUS can set new buffer1 address. FlexBUS will automatically jump to buffer0 address and capture new data; If don't want to receive new data, Set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
I. If want to stop receiving data , set FlexBUS.STOP[1]=1 at any time and wait rx_done interrupt; final disable FlexBUS;
J. If want to continue to receive data, repeat G-H-I.

DAC Transfer Flow

If want to support DAC feature, the configuration is showing as below:

A. Set modes, tx only, FLEXBUS_COM_CTL[3:0]=4'h1;
B. Set Interrupt mask, FLEXBUS_IMR;
C. Set format of transmit data, FLEXBUS_TX_CTL and continue_mode =1;
D. Set tx start water line, FLEXBUS_TXWAT_START;
E. Set DMA;
F. Set FlexBUS enable, FLEXBUS_ENR[1:0]=2'b01;
G. Wait interrupt, if dma_src0 is active indicating that buffer0 has finished and clear

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interrupt, FlexBUS can set new buffer0 address. FlexBUS will automatically jump to buffer1 address and send new data; If don’t want to send data, set FLEXBUS_STOP[0]=1, and then disable FlexBUS;

H. Wait interrupt, if dma_src1 is active indicating that buffer1 has finished and clear interrupt, FlexBUS can set new buffer1 address. FlexBUS will automatically jump to buffer0 address and send new data; If don’t want to send new data, Set FLEXBUS_STOP[0]=1, and then disable FlexBUS;

I. If want to stop sending data , set FlexBUS.STOP[0]=1 at any time and wait tx_done interrupt; final disable FlexBUS;

J. If want to continue to receive data, repeat G-H-I.

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Chapter 38 EMMC Host Controller

38.1 Overview

The eMMC Host Controller is highly programmable, and provides high performance with AXI as the bus interface for data transfer (master interface) and AHB as its slave interface.
It supports following features:

- Supports SD-HCI Host version 4 mode or less
  - Supports same SD-HCI register set for eMMC transfers
  - Supports Command Queuing Engine (CQE) and compliant with eMMC CQ HCI
  - Supports the following data transfer types: CPU, SDMA, AMDM2, ADMA3
- Supports eMMC protocols including eMMC 5.1
  - Supports Auto-tuning
  - Supports 4-bit/8-bit interface
  - Supports legacy, High Speed SDR, High Speed DDR, HS200, and HS400 speed modes
  - Supports boot operation and alternative boot operation
- AHB Slave Interface:
  - Supports 32-bit data width and address width
- AXI Master Interface:
  - Supports 64-bit address width and 64-bit data width
- Phase adjustment:

Supports phase auto adjustment for transmit clock, sample clock and data strobe, command output.

38.2 Block Diagram

The Host Controller consists of the following main functional blocks.

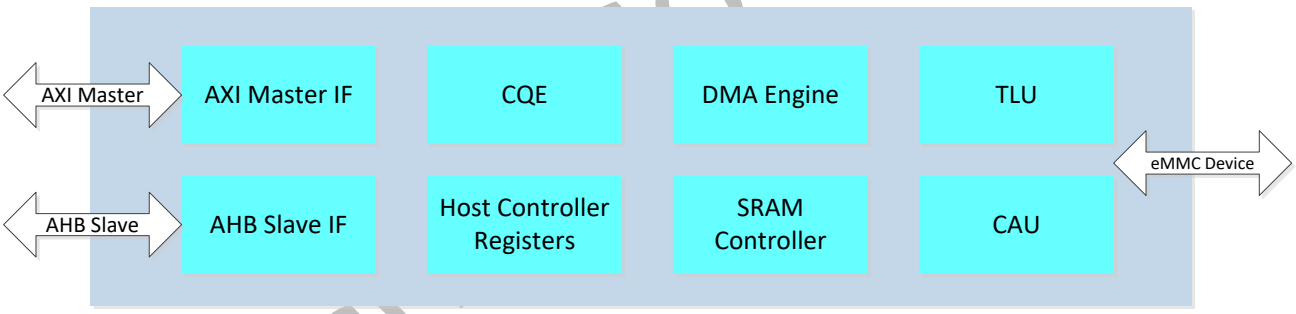

Fig. 38-1 EMMC Host Control Block Diagram

38.3 Function Description

38.3.1 The AXI Master Bus Interface Unit

This Master Bus Interface Unit implements the logic to transfer data on the AMBA Extensible Interface Bus (AXI) bus. The AXI interface transfers data to and from the system memory through the AXI master bus interface, respectively.

38.3.2 The AHB Slave Bus Interface Unit

The AHB slave bus interface module implements the logic to primarily access the host registers by using an external AMBA high-performance (AHB) bus.

38.3.3 Host Controller Registers

The host controller register unit comprises of the standard SD host controller registers as specified in the SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20a. It also includes Command Queuing registers compliance to JEDEC eMMC 5.1 HCI specification.

38.3.4 DMA Engine

The DMA Engine unit handles data transfer between the host and system memory.

- Support SDMA/ADMA2/ADMA3 modes
- Fetch the descriptor and data

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- The same DMA engine is used to interleave data transfer and descriptor fetch. This enables new task descriptor fetches (for CMD44 and CMD45) while DMA is moving data during task execution (for CMD46 and CMD47).
- The AXI transaction ID 0 is used for moving data and AXI transaction ID 1 is used to fetch task descriptors.
- Pre-fetch data for back-to-back eMMC write commands
- Write back the received data packets to the system memory

38.3.5 SRAM Controller

The SRAM controller interfaces the packet buffer of the host and the transaction controller units. The SRAM is a single clock single-port RAM synchronous to the core base clock. The width is 64-bit, the depth is 288-location.

38.3.6 Command Queuing Engine

This module implements command queuing and includes the following:

- Task scheduler with the ability to prioritize execution of tasks
- Control logic for descriptor fetch
- Control and sequence task submission and execution
- Status polling
- Timers and counter dedicated for CQE operation
- Interrupt coalescing logic

38.3.7 Transfer Level Unit

The TLU manages the command/response and data flow for communication with memory cards.

38.3.8 Clock Adjustment Unit

The clock adjustment unit (CAU) will detect the clock period and get the delay precision, adjust the clock phase base on the dedicate delay element. Also, you can program the register to set the delay precision. The flowing signals supports adjustment: transmit clock, sample clock and data strobe, command output.

38.4 Register Description

38.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

38.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
EMMC_SDMASA	0x0000	W	0x00000000	SDMA System Address Register
EMMC_BLOCKSIZE	0x0004	HW	0x00000000	Block Size Register
EMMC_ARGUMENT	0x0008	W	0x00000000	Argument Register
EMMC_BLOCKCOUNT	0x0006	HW	0x00000000	Block Count Register
EMMC_XFER_MODE	0x000C	HW	0x00000000	Transfer Mode Register
EMMC_CMD	0x000E	HW	0x00000000	Command Register
EMMC_RESP01	0x0010	W	0x00000000	Response Register 0/1
EMMC_RESP23	0x0014	W	0x00000000	Response Register 2/3
EMMC_RESP45	0x0018	W	0x00000000	Response Register 4/5
EMMC_RESP67	0x001C	W	0x00000000	Response Register 6/7
EMMC_BUF_DATA	0x0020	W	0x00000000	Buffer Data Port Register
EMMC_PSTATE	0x0024	W	0x19FF0000	Present State Register
EMMC_HOST_CTRL1	0x0028	B	0x00000000	Host Control 1 Register
EMMC_PWR_CTRL	0x0029	B	0x00000000	Power Control Register
EMMC_BGAP_CTRL	0x002A	B	0x00000000	Block Gap Control Register
EMMC_CLK_CTRL	0x002C	HW	0x00000000	Clock Control Register
EMMC_TOUT_CTRL	0x002E	B	0x00000000	Timeout Control Register
EMMC_SW_RST	0x002F	B	0x00000000	Software Reset Register
EMMC_NORMAL_INT_STAT	0x0030	HW	0x00000000	Normal Interrupt Status Register

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Name	Offset	Size	Reset Value	Description
EMMC_ERROR_INT_STAT	0x0032	HW	0x00000000	Error Interrupt Status Register
EMMC_NORMAL_INT_STAT_EN	0x0034	HW	0x00000000	Normal Interrupt Status Enable Register
EMMC_ERROR_INT_STAT_EN	0x0036	HW	0x00000000	Error Interrupt Status Enable Register
EMMC_NORMAL_INT_SIGNAL_EN	0x0038	HW	0x00000000	Normal Interrupt Signal Enable Register
EMMC_ERROR_INT_SIGNAL_EN	0x003A	HW	0x00000000	Error Interrupt Signal Enable Register
EMMC_AUTO_CMD_STAT	0x003C	HW	0x00000000	Auto CMD Error Status Register
EMMC_HOST_CTRL2	0x003E	HW	0x00000000	Host Control 2 Register
EMMC_CAPABILITIES1	0x0040	W	0x40EDC880	Capabilities Register 1
EMMC_CAPABILITIES2	0x0044	W	0x000A2077	Capabilities Register 2
EMMC_FORCE_AUTO_CMD_STAT	0x0050	HW	0x00000000	Force Event Register for Auto CMD Error Status Register
EMMC_FORC_ERR_INT_STAT	0x0052	HW	0x00000000	Force Event Register for Error Interrupt Status Register
EMMC_ADMA_ERR_STAT	0x0054	B	0x00000000	ADMA Error Status Register
EMMC_ADMA_SA_LOW	0x0058	W	0x00000000	ADMA System Address Register-Low
EMMC_ADMA_SA_HIGH	0x005C	W	0x00000000	ADMA System Address Register-High
EMMC_PRESET_INIT	0x0060	HW	0x00000000	Preset Value for Initialization Register
EMMC_PRESET_DS	0x0062	HW	0x00000000	Preset Value for Default Speed Register
EMMC_PRESET_HS	0x0064	HW	0x00000000	Preset Value for High Speed Register
EMMC_PRESET_SDR12	0x0066	HW	0x00000000	Preset Value for SDR12 Register
EMMC_PRESET_SDR25	0x0068	HW	0x00000000	Preset Value for SDR25 Register
EMMC_PRESET_SDR50	0x006A	HW	0x00000000	Preset Value for SDR50 Register
EMMC_PRESET_SDR104	0x006C	HW	0x00000000	Preset Value for SDR104 Register
EMMC_PRESET_DDR50	0x006E	HW	0x00000000	Preset Value for DDR50 Register
EMMC_ADMA_ID_LOW	0x0078	W	0x00000000	ADMA3 Integrated Descriptor Address Register-Low
EMMC_ADMA_ID_HIGH	0x007C	W	0x00000000	ADMA3 Integrated Descriptor Address Register-High
EMMC_SLOT_INTR_STATUS	0x00FC	HW	0x00000000	Slot Interrupt Status Register
EMMC_HOST_CNTRL_VERS	0x00FE	HW	0x00001005	Host Controller Version Register
EMMC_CQVER	0x0180	W	0x00000510	Command Queuing Version Register
EMMC_CQCAP	0x0184	W	0x00000000	Command Queuing Capabilities Register
EMMC_CQCFG	0x0188	W	0x00000000	Command Queuing Configuration Register
EMMC_CQCTRL	0x018C	W	0x00000000	Command Queuing Control Register
EMMC_CQIS	0x0190	W	0x00000000	Command Queuing Interrupt Status Register
EMMC_CQISE	0x0194	W	0x00000000	Command Queuing Interrupt Status Enable Register

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Name	Offset	Size	Reset Value	Description
EMMC_CQISGE	0x0198	W	0x00000000	Command Queuing Interrupt Signal Enable Register
EMMC_CQIC	0x019C	W	0x00000000	Command Queuing Interrupt Coalescing Register
EMMC_CQTDLBA	0x01A0	W	0x00000000	Command Queuing Task Descriptor List Base Address Register
EMMC_CQTDBR	0x01A8	W	0x00000000	Command Queuing Door Bell Register
EMMC_CQTCN	0x01AC	W	0x00000000	Command Queuing Task Clear Notification Register
EMMC_CQDQS	0x01B0	W	0x00000000	Command Queuing Device Queue Status Register
EMMC_CQDPT	0x01B4	W	0x00000000	Command Queuing Device Pending Tasks Register
EMMC_CQTCLR	0x01B8	W	0x00000000	Command Queuing Task Clear Register
EMMC_CQSSC1	0x01C0	W	0x00011000	Command Queuing Send Status Configuration 1 Register
EMMC_CQSSC2	0x01C4	W	0x00000000	Command Queuing Send Status Configuration 2 Register
EMMC_CQCRDCT	0x01C8	W	0x00000000	Command Queuing Command Response For Direct Command Register
EMMC_CQRMEM	0x01D0	W	0xFDF9A080	Command Queuing Command Response Mode Error Mask Register
EMMC_CQTERRI	0x01D4	W	0x00000000	Command Queuing Task Error Information Register
EMMC_CQCRI	0x01D8	W	0x00000000	Command Queuing Command Response Index Register
EMMC_CQCRA	0x01DC	W	0x00000000	Command Queuing Command Response Argument Register
EMMC_VER_ID	0x0500	W	0x00000000	Host Version ID Register
EMMC_VER_TYPE	0x0504	W	0x00000000	Host Version Type Register
EMMC_HOST_CTRL3	0x0508	B	0x00000000	Host Control 3 Register
EMMC_EMMC_CTRL	0x052C	HW	0x00000004	EMMC Control Register
EMMC_BOOT_CTRL	0x052E	HW	0x00000000	Boot Control Register
EMMC_AT_CTRL	0x0540	W	0x00000000	Tuning Control Register
EMMC_AT_STAT	0x0544	W	0x00000000	Tuning Status Register
EMMC_DLL_CTRL	0x0800	W	0x00000000	DLL Global Control Register
EMMC_DLL_RXCLK	0x0804	W	0x00000000	DLL Control Register For Receive Clock
EMMC_DLL_TXCLK	0x0808	W	0x00000000	DLL Control Register For Transmit Clock
EMMC_DLL_STRBIN	0x080C	W	0x00000000	DLL Control Register For Strobe Input
EMMC_DLL_CMDOUT	0x0810	W	0x00000000	DLL Control Register For Command Output
EMMC_MISC_CON	0x081C	W	0x00000001	Miscellaneous Control Register
EMMC_DLL_STATUS0	0x0840	W	0x00000000	DLL Status Register 0
EMMC_DLL_STATUS1	0x0844	W	0x00000000	DLL Status Register 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

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38.4.3 Detail Register Description

EMMC_SDMASA

Address: Operational Base(0x2A330000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	BLOCKCNT_SDMASA 32-bit Block Count (SDMA System Address). 1. SDMA System Address (Host Version 4 Enable = 0): This register contains the system memory address for an SDMA transfer in the 32-bit addressing mode. When the Host Controller stops an SDMA transfer, this register points to the system address of the next contiguous data position. It can be accessed only if no transaction is executing. Reading this register during data transfers may return an invalid value. 2. 32-bit Block Count (Host Version 4 Enable = 1): From the Host Controller Version 4.10 specification, this register is redefined as 32-bit Block Count. The Host Controller decrements the block count of this register for every block transfer and the data transfer stops when the count reaches zero. This register must be accessed when no transaction is executing. Reading this register during data transfers may return invalid value. Values: 32'hFFFFFFFF: 1 Block ..... 32'h00000002: 2 Blocks 32'h00000001: 1 Block 32'h00000000: Stop Count Note: a. For Host Version 4 Enable = 0, the Host driver does not program the system address in this register while operating in ADMA mode. The system address must be programmed in the ADMA System Address register. b. For Host Version 4 Enable = 0, the Host driver programs a non-zero 32-bit block count value in this register when Auto CMD23 is enabled for non-DMA and ADMA modes. Auto CMD23 cannot be used with SDMA. c. This register must be programmed with a non-zero value for data transfer if the 32-bit Block count register is used instead of the 16-bit Block count register.

EMMC_BLOCKSIZE

Address: Operational Base(0x2A330000) + offset (0x0004)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x0	SDMA_BUF_BDARY SDMA Buffer Boundary. These bits specify the size of contiguous buffer in system memory. The SDMA transfer waits at every boundary specified by these fields and the Host Controller generates the DMA interrupt to request the Host Driver to update the SDMA System Address register. Values: 3'h0: 4K bytes SDMA Buffer Boundary 3'h1: 8K bytes SDMA Buffer Boundary 3'h2: 16K bytes SDMA Buffer Boundary 3'h3: 32K bytes SDMA Buffer Boundary 3'h4: 64K bytes SDMA Buffer Boundary 3'h5: 128K bytes SDMA Buffer Boundary

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Bit	Attr	Reset Value	Description
			3'h6: 256K bytes SDMA Buffer Boundary 3'h7: 512K bytes SDMA Buffer Boundary
11:0	RW	0x000	XFER_BLOCK_SIZE Transfer Block Size. These bits specify the block size of data transfers. In case of memory, it is set to 512 bytes. It can be accessed only if no transaction is executing. Read operations during transfers may return an invalid value, and write operations are ignored. Values: 12'h1: 1 byte 12'h2: 2 bytes 12'h3: 3 bytes ..... 12'h1FF: 511 byte 12'h200: 512 bytes ..... 12'h800: 2048 bytes Note: This register must be programmed with a non-zero value for data transfer.

EMMC_ARGUMENT

Address: Operational Base(0x2A330000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARGUMENT Command Argument. These bits specify the SD/eMMC command argument that is specified in bits 39-8 of the Command format.

EMMC_BLOCKCOUNT

Address: Operational Base(0x2A330000) + offset (0x0006)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	BLOCK_CNT 16-bit Block Count. If the Host Version 4 Enable bit is set 0 or the 16-bit Block Count register is set to non-zero, the 16-bit Block Count register is selected. If the Host Version 4 Enable bit is set 1 and the 16-bit Block Count register is set to zero, the 32-bit Block Count register is selected. Values: 16'h0: Stop Count 16'h1: 1 Block 16'h2: 2 Blocks ..... 16'hFFFF: 65535 Blocks Note: For Host Version 4 Enable = 0, this register must be set to 0 before programming the 32-bit block count register when Auto CMD23 is enabled for non-DMA and ADMA modes.

EMMC_XFER_MODE

Address: Operational Base(0x2A330000) + offset (0x000C)

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	RESP_INT_DISABLE Response Interrupt Disable. The Host Controller supports response check function to avoid overhead of response error check by the Host driver. Response types of only R1 and R5 can be checked by the Controller. If Host Driver checks the response error, set this bit to 0 and wait for Command Complete Interrupt and then check the response register. If the Host Controller checks the response error, set this bit to 1 and set the Response Error Check Enable bit to 1. The Command Complete Interrupt is disabled by this bit regardless of the Command Complete Signal Enable. Note: During tuning (when the Execute Tuning bit in the Host Control2 register is set), the Command Complete Interrupt is not generated irrespective of the Response Interrupt Disable setting. Values: 1'b0: Response Interrupt is enabled 1'b1: Response Interrupt is disabled
7	RW	0x0	RESP_ERR_CHK_ENABLE Response Error Check Enable. The Host Controller supports response check function to avoid overhead of response error check by Host driver. Response types of only R1 and R5 can be checked by the Controller. If the Host Controller checks the response error, set this bit to 1 and set Response Interrupt Disable to 1. If an error is detected, the Response Error interrupt is generated in the Error Interrupt Status register. Note: a. Response error check must not be enabled for any response type other than R1 and R5. b. Response check must not be enabled for the tuning command. Values: 1'b0: Response Error Check is disabled 1'b1: Response Error Check is enabled
6	RW	0x0	RESP_TYPE Response Type R1/R5. This bit selects either R1 or R5 as a response type when the Response Error Check is selected. Values: 1'b0: R1 1'b1: R5
5	RW	0x0	MULTI_BLK_SEL Multi/Single Block Select. This bit is set when issuing multiple-block transfer commands using the DAT line. If this bit is set to 0, it is not necessary to set the Block Count register. Values: 1'b0: Single Block 1'b1: Multiple Block

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Bit	Attr	Reset Value	Description
4	RW	0x0	DATA_XFER_DIR Data Transfer Direction Select. This bit defines the direction of DAT line data transfers. This bit is set to 1 by the Host Driver to transfer data from the SD/eMMC card to the Host Controller and it is set to 0 for all other commands. Values: 1'b0: Write (Host to Card) 1'b1: Read (Card to Host)
3:2	RW	0x0	AUTO_CMD_ENABLE Auto Command Enable. This field determines use of Auto Command functions. Values: 2'h0: Auto Command Disabled 2'h1: Auto CMD12 Enable 2'h2: Auto CMD23 Enable 2'h3: Auto CMD Auto Select
1	RW	0x0	BLOCK_COUNT_ENABLE Block Count Enable. This bit is used to enable the Block Count register, which is relevant for multiple block transfers. If this bit is set to 0, the Block Count register is disabled, which is useful in executing an infinite transfer. The Host Driver must set this bit to 0 when ADMA is used. Values: 1'b0: Disable 1'b1: Enable
0	RW	0x0	DMA_ENABLE DMA Enable. This bit enables the DMA functionality. If this bit is set to 1, a DMA operation begins when the Host Driver writes to the Command register. You can select one of the DMA modes by using DMA Select in the Host Control 1 register. Values: 1'b0: No data transfer or Non-DMA data transfer 1'b1: DMA Data transfer

EMMC_CMD

Address: Operational Base(0x2A330000) + offset (0x000E)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:8	RW	0x00	CMD_INDEX Command Index. These bits are set to the command number that is specified in bits 45-40 of the command format.
7:6	RW	0x0	CMD_TYPE Command Type. These bits indicate the command type. Note: While issuing Abort CMD using CMD12/CMD52 or reset CMD using CMD0/CMD52, CMD_TYPE field shall be set to 0x3. Values: 2'h0: Normal 2'h1: Suspend 2'h2: Resume 2'h3: Abort

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Bit	Attr	Reset Value	Description
5	RW	0x0	DATA_PRESENT_SEL Data Present Select. This bit is set to 1 to indicate that data is present and that the data is transferred using the DAT line. This bit is set to 0 in the following instances: a. Command using the CMD line b. Command with no data transfer but using busy signal on the DAT[0] line c. Resume Command Values: 1'b0: No Data Present 1'b1: Data Present
4	RW	0x0	CMD_IDX_CHK_ENABLE Command Index Check Enable. This bit enables the Host Controller to check the index field in the response to verify if it has the same value as the command index. If the value is not the same, it is reported as a Command Index error. Note: a. Index check enable must be set to 0 for the command with no response, R2 response, R3 response and R4 response. b. For the tuning command, this bit must always be set to enable the index check. Values: 1'b0: Disable 1'b1: Enable
3	RW	0x0	CMD_CRC_CHK_ENABLE Command CRC Check Enable. This bit enables the Host Controller to check the CRC field in the response. If an error is detected, it is reported as a Command CRC error. Note: a. CRC check enable must be set to 0 for the command with no response, R3 response, and R4 response. b. For the tuning command, this bit must always be set to 1 to enable the CRC check. Values: 1'b0: Disable 1'b1: Enable
2	RW	0x0	SUB_CMD_FLAG Sub Command Flag. This bit distinguishes between a main command and a sub command. Values: 1'b0: Main Command 1'b1: Sub Command
1:0	RW	0x0	RESP_TYPE_SELECT Response Type Select. This bit indicates the type of response expected from the card. Values: 2'h0: No Response 2'h1: Response length 136 2'h2: Response length 48 2'h3: Response length 48, check Busy after response.

EMMC_RESP01

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Address: Operational Base(0x2A330000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP01 Command Response. These bits reflect 39-8 bits of SD/eMMC Response Field. Note: For Auto CMD, the 32-bit response (bits 39-8 of the Response Field) is updated in the RESP67 register.

EMMC_RESP23

Address: Operational Base(0x2A330000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP23 Command Response. These bits reflect 71-40 bits of the SD/eMMC Response Field.

EMMC_RESP45

Address: Operational Base(0x2A330000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	RESP45 Command Response. These bits reflect 103-72 bits of the Response Field.

EMMC_RESP67

Address: Operational Base(0x2A330000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP67 Command Response These bits reflect bits 135-104 of SD/EMMC Response Field. For Auto CMD, this register also reflects the 32-bit response (bits 39-8 of the Response Field).

EMMC_BUF_DATA

Address: Operational Base(0x2A330000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	BUF_DATA Buffer Data. These bits enable access to the Host Controller packet buffer.

EMMC_PSTATE

Address: Operational Base(0x2A330000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x1	SUB_CMD_STAT Sub Command Status. This bit is used to distinguish between a main command and a sub command status. Values: 1'b0: Main Command Status 1'b1: Sub Command Status

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Bit	Attr	Reset Value	Description
27	RO	0x1	CMD_ISSUE_ERR Command Not Issued by Error. This bit is set if a command cannot be issued after setting the command register due to an error except the Auto CMD12 error. Values: 1'b0: No error for issuing a command 1'b1: Command cannot be issued
26:25	RO	0x0	reserved
24	RO	0x1	CMD_LINE_LVL Command-Line Signal Level. This bit is used to check the CMD line level to recover from errors and for debugging.
23:20	RO	0xf	DAT_3_0 DAT[3:0] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging.
19	RO	0x1	WR_PROTECT_SW_LVL Write Protect Switch Pin Level. This bit is supported only for memory and combo cards. Values: 1'b0: Write protected 1'b1: Write enabled
18	RO	0x1	CARD_DETECT_PIN_LEVEL Card Detect Pin Level. Values: 1'b0: No card present 1'b1: Card Present
17	RO	0x1	CARD_STABLE Card Stable. This bit indicates the stability of the Card Detect Pin Level. A card is not detected if this bit is set to 1 and the value of the CARD_INSERTED bit is 0. Values: 1'b0: Reset or Debouncing 1'b1: No Card or Inserted
16	RO	0x1	CARD_INSERTED Card Inserted. This bit indicates whether a card has been inserted. The Host Controller debounces this signal so that Host Driver need not wait for it to stabilize. Values: 1'b0: Reset, Debouncing, or No card 1'b1: Card Inserted
15:12	RO	0x0	reserved
11	RO	0x0	BUF_RD_ENABLE Buffer Read Enable. This bit is used for non-DMA transfers. This bit is set if valid data exists in the Host buffer. Values: 1'b0: Read disable 1'b1: Read enable

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Bit	Attr	Reset Value	Description
10	RO	0x0	BUF_WR_ENABLE Buffer Write Enable. This bit is used for non-DMA transfers. This bit is set if space is available for writing data. Values: 1'b0: Write disable 1'b1: Write enable
9	RW	0x0	RD_XFER_ACTIVE Read Transfer Active. This bit indicates whether a read transfer is active for SD/eMMC mode. Values: 1'b0: No valid data 1'b1: Transferring data
8	RO	0x0	WR_XFER_ACTIVE Write Transfer Active. This status indicates whether a write transfer is active for SD/eMMC mode. Values: 1'b0: No valid data 1'b1: Transferring data
7:4	RO	0x0	DAT_7_4 DAT[7:4] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging.
3	RO	0x0	RE_TUNE_REQ Re-Tuning Request. Host Controller does not generate retuning request. The software must maintain the Retuning timer.
2	RO	0x0	DAT_LINE_ACTIVE DAT Line Active (SD/eMMC Mode only). This bit indicates whether one of the DAT lines on the SD/eMMC bus is in use. In the case of read transactions, this bit indicates whether a read transfer is executing on the SD/eMMC bus. In the case of write transactions, this bit indicates whether a write transfer is executing on the SD/eMMC bus. For a command with busy, this status indicates whether the command executing busy is executing on an SD/eMMC bus. Values: 1'b0: DAT Line Inactive 1'b1: DAT Line Active
1	RO	0x0	CMD_INHIBIT_DAT Command Inhibit (DAT). This bit is applicable for SD/eMMC mode and is generated if either DAT line active or Read transfer active is set to 1. If this bit is set to 0, it indicates that the Host Controller can issue subsequent SD/eMMC commands. Values: 1'b0: Can issue command which used DAT line 1'b1: Cannot issue command which used DAT line

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Bit	Attr	Reset Value	Description
0	RO	0x0	CMD_INHIBIT Command Inhibit (CMD). If this bit is set to 0, it indicates that the CMD line is not in use and the Host controller can issue an SD/eMMC command using the CMD line. This bit is set when the command register is written. This bit is cleared when the command response is received. This bit is not cleared by the response of auto CMD12/23 but cleared by the response of read/write command. Values: 1'b0: Host Controller is ready to issue a command 1'b1: Host Controller is not ready to issue a command

EMMC_HOST_CTRL1

Address: Operational Base(0x2A330000) + offset (0x0028)

Bit	Attr	Reset Value	Description
7	RW	0x0	CARD_DETECT_SIG_SEL Card Detect Signal Selection. This bit selects a source for card detection. When the source for the card detection is switched, the interrupt must be disabled during the switching period. Values: 1'b0: Card Detect Signal is selected (for normal use) 1'b1: Card Detect Test Level is selected (for test purpose)
6	RW	0x0	CARD_DETECT_TEST_LVL Card Detect Test Level. This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates whether a card inserted or not. Values: 1'b0: No Card 1'b1: Card Inserted
5	RW	0x0	EXT_DAT_XFER Extended Data Transfer Width. This bit controls 8-bit bus width mode of embedded device. Values: 1'b0: Bus Width is selected by the Data Transfer Width 1'b1: 8-bit Bus Width
4:3	RW	0x0	DMA_SEL DMA Select. This field is used to select the DMA type. When Host Version 4 Enable is 1 in Host Control 2 register: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: ADMA2 is selected 2'h3: ADMA2 or ADMA3 is selected When Host Version 4 Enable is 0 in Host Control 2 register: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: 32-bit Address ADMA2 is selected 2'h3: Reserved Values: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: ADMA2 is selected 2'h3: ADMA2 or ADMA3 is selected

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Bit	Attr	Reset Value	Description
2	RW	0x0	HIGH_SPEED_EN High Speed Enable. In SD/eMMC mode, this bit is used to determine the selection of pre-set value for High Speed mode. Before setting this bit, the Host Driver checks the High Speed Support in the Capabilities register. Values: 1'b0: Normal Speed mode 1'b1: High Speed mode
1	RW	0x0	DAT_XFER_WIDTH Data Transfer Width. For SD/eMMC mode, this bit selects the data transfer width of the Host Controller. The Host Driver sets it to match the data width of the SD/eMMC card. Values: 1'b0: 1-bit mode 1'b1: 4-bit mode
0	RO	0x0	reserved

EMMC_PWR_CTRL

Address: Operational Base(0x2A330000) + offset (0x0029)

Bit	Attr	Reset Value	Description
7:1	RO	0x00	reserved
0	RW	0x0	SD_BUS_PWR If this bit is cleared, the Host Controller stops the SD Clock by clearing the SD_CLK_IN bit in the EMMC_CLK_CTRL register. Values: 1'b0: Power off 1'b1: Power on

EMMC_BGAP_CTRL

Address: Operational Base(0x2A330000) + offset (0x002A)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3	RW	0x0	INT_AT_BGAP Interrupt At Block Gap. This bit is valid only in the 4-bit mode of an SDIO card and is used to select a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer.
2	RW	0x0	RD_WAIT_CTRL Read Wait Control. This bit is used to enable the read wait protocol to stop read data using DAT[2] line if the card supports read wait. Otherwise, the Host Controller has to stop the card clock to hold the read data. Values: 1'b0: Disable Read Wait Control 1'b1: Enable Read Wait Control

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Bit	Attr	Reset Value	Description
1	RW	0x0	CONTINUE_REQ Continue Request. This bit is used to restart the transaction, which was stopped using the Stop At Block Gap Request. The Host Controller automatically clears this bit when the transaction restarts. If stop at block gap request is set to 1, any write to this bit is ignored. Values: 1'b0: No Affect 1'b1: Restart
0	RW	0x0	STOP_BG_REQ Stop At Block Gap Request. This bit is used to stop executing read and write transactions at the next block gap for non-DMA, SDMA, and ADMA transfers. Values: 1'b0: Transfer 1'b1: Stop

EMMC_CLK_CTRL

Address: Operational Base(0x2A330000) + offset (0x002C)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	FREQ_SEL SDCLK Frequency Select. These bits specify the lower 8 bits of 10-bit SDCLK Frequency Select control. These bits are used to select the frequency of the SDCLK signal. These bits depend on setting of Preset Value Enable in the Host Control 2 register. If Preset Value Enable = 0, these bits are set by the Host Driver. If Preset Value Enable = 1, these bits are automatically set to a value specified in one of the Preset Value register. 1. 10-bit Divided Clock Mode: 10'h000: Base clock (10MHz - 255 MHz) 10'h001: 1/2 Divided Clock 10'h002: 1/4 Divided Clock ..... 10'h3ff: 1/2046 Divided clock 2. Programmable Clock Mode: 10'h000: Base clock * M 10'h001: Base clock * M /2 10'h002: Base clock * M /3 ..... 10'h3ff: Base clock * M /1024
7:6	RW	0x0	UPPER_FREQ_SEL These bits specify the upper 2 bits of 10-bit SDCLK Frequency Select control.
5	RW	0x0	CLK_GEN_SELECT Clock Generator Select. This bit is used to select the clock generator mode in SDCLK Frequency Select. If Preset Value Enable = 0, this bit is set by the Host Driver. If Preset Value Enable = 1, this bit is automatically set to a value specified in one of the Preset Value registers. Values: 1'b0: Divided Clock Mode 1'b1: Programmable Clock Mode
4:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	SD_CLK_EN SD/eMMC Clock Enable. This bit stops the SDCLK when set to 0. The SDCLK Frequency Select bit can be changed when this bit is set to 0. Values: 1'b0: Disable providing SDCLK 1'b1: Enable providing SDCLK
1	RO	0x0	INTERNAL_CLK_STABLE Internal Clock Stable. Values: 1'b0: Not Ready 1'b1: Ready
0	RW	0x0	INTERNAL_CLK_EN Internal Clock Enable. This bit is set to 0 when the Host Driver is not using the Host Controller. The Host Controller must stop its internal clock to enter a very low power state. However, registers can still be read and written to. Note: If this bit is not used to control the internal clock (base clock and master clock), it is recommended to set this bit to 1. Values: 1'b0: Stop 1'b1: Oscillate

EMMC_TOUT_CTRL

Address: Operational Base(0x2A330000) + offset (0x002E)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3:0	RW	0x0	TOUT_CNT Data Timeout Counter Value. This value determines the interval by which DAT line timeouts are detected. Timeout clock frequency will be generated by dividing the base clock TMCLK by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). Values: 4'h0: TMCLK * 2^13 4'h1: TMCLK * 2^14 ..... 4'he: TMCLK * 2^27 4'hf: Reserved

EMMC_SW_RST

Address: Operational Base(0x2A330000) + offset (0x002F)

Bit	Attr	Reset Value	Description
7:3	RO	0x00	reserved
2	RW	0x0	SW_RST_DAT Software Reset For DAT line. This bit is used in SD/eMMC mode and it resets only a part of the data circuit and the DMA circuit is also reset. The following registers and bits are cleared by this bit: a. Buffer Data Port register: Buffer is cleared and initialized.

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Bit	Attr	Reset Value	Description
			b. Present state register: Buffer Read Enable Buffer Write Enable Read Transfer Active Write Transfer Active DAT Line Active Command Inhibit (DAT) c. Block Gap Control register: Continue Request Stop At Block Gap Request d. Normal Interrupt status register: Buffer Read Ready Buffer Write Ready DMA Interrupt Block Gap Event Transfer Complete Values: 1'b0: Work 1'b1: Reset
1	RW	0x0	SW_RST_CMD Software Reset For CMD line. This bit resets only a part of the command circuit to be able to issue a command. This reset is effective only for a command issuing circuit (including response error statuses related to Command Inhibit (CMD) control) and does not affect the data transfer circuit. Host Controller can continue data transfer even after this reset is executed while handling subcommand-response errors. The following registers and bits are cleared by this bit: a. Present State register - Command Inhibit (CMD) bit b. Normal Interrupt Status register - Command Complete bit c. Error Interrupt Status - Response error statuses related to Command Inhibit (CMD) bit Values: 1'b0: Work 1'b1: Reset
0	RW	0x0	SW_RST_ALL Software Reset For All. This reset affects the entire Host Controller except for the card detection circuit. During its initialization, the Host Driver sets this bit to 1 to reset the Host Controller. All registers are reset except the capabilities register. If this bit is set to 1, the Host Driver must issue reset command and reinitialize the card. Values: 1'b0: Work 1'b1: Reset

EMMC_NORMAL_INT_STAT

Address: Operational Base(0x2A330000) + offset (0x0030)

Bit	Attr	Reset Value	Description
15	RO	0x0	ERROR_INT_STAT Error Interrupt. If any of the bits in the Error Interrupt Status register are set, then this bit is set. Values: 1'b0: No Error

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Bit	Attr	Reset Value	Description
			1'b1: Error
14	RC/W1C	0x0	CQE_EVENT Command Queuing Event. This status is set if Command Queuing/Crypto related event has occurred in eMMC/SD mode. Read CQHCI's CQIS/CRNQIS register for more details. Values: 1'b0: No Event 1'b1: Command Queuing Event is detected Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
13	RO	0x0	FX_EVENT FX Event. This status is set when R[14] of response register is set to 1 and Response Type R1/R5 is set to 0 in Transfer Mode register. This interrupt is used with response check function. Values: 1'b0: No Event 1'b1: FX Event is detected
12	RO	0x0	RE_TUNE_EVENT Re-tuning Event. This bit is set if the Re-Tuning Request changes from 0 to 1. Re-Tuning request is not supported.
11:9	RO	0x0	reserved
8	RO	0x0	CARD_INTERRUPT Card Interrupt. This bit reflects the synchronized value of DAT[1] Interrupt Input for SD Mode. Values: 1'b0: No Card Interrupt 1'b1: Generate Card Interrupt
7	RC/W1C	0x0	CARD_REMOVAL Card Removal. This bit is set if the Card Inserted in the Present State register changes from 1 to 0. Values: 1'b0: Card state stable or Debouncing 1'b1: Card Removed Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
6	RC/W1C	0x0	CARD_INSERTION Card Insertion. This bit is set if the Card Inserted in the Present State register changes from 0 to 1. Values: 1'b0: Card state stable or Debouncing 1'b1: Card Inserted Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.

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Bit	Attr	Reset Value	Description
5	RC/W1C	0x0	BUF_RD_READY Buffer Read Ready. This bit is set if the Buffer Read Enable changes from 0 to 1. Values: 1'b0: Not ready to read buffer 1'b1: Ready to read buffer Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
4	RC/W1C	0x0	BUF_WR_READY Buffer Write Ready. This bit is set if the Buffer Write Enable changes from 0 to 1. Values: 1'b0: Not ready to write buffer 1'b1: Ready to write buffer Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
3	RC/W1C	0x0	DMA_INTERRUPT DMA Interrupt. This bit is set if the Host Controller detects the SDMA Buffer Boundary during transfer. In case of ADMA, by setting the Int field in the descriptor table, the Host controller generates this interrupt. This interrupt is not generated after a Transfer Complete. Values: 1'b0: No DMA Interrupt 1'b1: DMA Interrupt is generated Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
2	RC/W1C	0x0	BGAP_EVENT Block Gap Event. This bit is set when both read/write transaction is stopped at block gap due to a Stop at Block Gap Request. Values: 1'b0: No Block Gap Event 1'b1: Transaction stopped at block gap Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
1	RC/W1C	0x0	XFER_COMPLETE Transfer Complete. This bit is set when a read/write transfer and a command with status busy is completed. Values: 1'b0: Not complete 1'b1: Command execution is completed Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
0	RC/W1C	0x0	CMD_COMPLETE Command Complete. In an SD/eMMC Mode, this bit is set when the end bit of a response except for Auto CMD12 and Auto CMD23. This interrupt is not generated when the Response Interrupt Disable in Transfer Mode Register is set to 1. Values: 1'b0: No Command Complete 1'b1: Command Complete Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit

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Bit	Attr	Reset Value	Description
			intact.

EMMC_ERROR_INT_STAT

Address: Operational Base(0x2A330000) + offset (0x0032)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RC/W1C	0x0	BOOT_ACK_ERR Boot Acknowledgement Error. This bit is set when there is a timeout for boot acknowledgement or when detecting boot acknowledgement status having a value other than 3'b010. This is applicable only when boot acknowledgement is expected in eMMC mode. Values: 1'b0: No Error 1'b1: Error
11	RC/W1C	0x0	RESP_ERR Response Error Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1. Values: 1'b0: No Error 1'b1: Error
10	RC/W1C	0x0	TUNING_ERR Tuning Error. This bit is set when an unrecoverable error is detected in a tuning circuit except during the tuning procedure (occurrence of an error during tuning procedure is indicated by Sampling Clock Select in the Host Control 2 register). By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock Select is set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Tuning Error, the Host Driver must discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from the tuning circuit error. Values: 1'b0: No Error 1'b1: Error
9	RC/W1C	0x0	ADMA_ERR ADMA Error. This bit is set when the Host Controller detects error during ADMA-based data transfer. The error could be due to following reasons: a. Error response received from System bus b. ADMA3,ADMA2 Descriptors invalid c. CQE Task or Transfer descriptors invalid When the error occurs, the state of the ADMA is saved in the ADMA Error Status register. In eMMC CQE mode: The Host Controller generates this Interrupt when it detects an invalid descriptor data at the Fetch Descriptor state. ADMA Error State in the ADMA Error Status indicates that an error has

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Bit	Attr	Reset Value	Description
			occurred in Fetch Descriptor state. The Host Driver may find that Valid bit is not set at the error descriptor. Values: 1'b0: No Error 1'b1: Error
8	RC/W1C	0x0	AUTO_CMD_ERR Auto CMD Error. This error status is used by Auto CMD12 and Auto CMD23 in SD/eMMC mode. This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared by clearing of this bit. Values: 1'b0: No Error 1'b0: Error
7	RO	0x0	reserved
6	RC/W1C	0x0	DATA_END_BIT_ERR Data End Bit Error. This error occurs in SD/eMMC mode either when detecting 0 at the end bit position of read data that uses the DAT line or at the end bit position of the CRC status. Values: 1'b0: No Error 1'b1: Error
5	RC/W1C	0x0	DATA_CRC_ERR Data CRC Error. This error occurs in SD/eMMC mode when detecting CRC error when transferring read data which uses the DAT line, when detecting the Write CRC status having a value of other than 010 or when write CRC status timeout. Values: 1'b0: No Error 1'b1: Error
4	RC/W1C	0x0	DATA_TOUT_ERR Data Timeout Error. This bit is set in SD/eMMC mode when detecting one of the following timeout conditions: a. Busy timeout for R1b, R5b type b. Busy timeout after Write CRC status c. Write CRC Status timeout d. Read Data timeout Values: 1'b0: No Error 1'b1: Time out
3	RC/W1C	0x0	CMD_IDX_ERR Command Index Error. This bit is set if a Command Index error occurs in the command response in SD/eMMC mode. Values: 1'b0: No Error 1'b1: Error

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Bit	Attr	Reset Value	Description
2	RC/W1C	0x0	CMD_END_BIT_ERR Command End Bit Error. This bit is set when detecting that the end bit of a command response is 0 in SD/eMMC mode. Values: 1'b0: No Error 1'b1: End Bit Error generated
1	RC/W1C	0x0	CMD_CRC_ERR Command CRC Error. Command CRC Error is generated in SD/eMMC mode for following two cases. a. If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. b. The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller aborts the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error is also set to 1 to distinguish a CMD line conflict. Values: 1'b0: No Error 1'b1: CRC Error generated
0	RC/W1C	0x0	CMD_TOUT_ERR Command Timeout Error. In SD/eMMC Mode, this bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, along with Command CRC Error bit, this bit is set to 1, without waiting for 64 SD/eMMC card clock cycles. Values: 1'b0: No Error 1'b1: Time out

EMMC_NORMAL_INT_STAT_EN

Address: Operational Base(0x2A330000) + offset (0x0034)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	CQE_EVENT_STAT_EN CQE Event Status Enable. Values: 1'b0: Masked 1'b1: Enabled
13:9	RO	0x00	reserved
8	RW	0x0	CARD_INTERRUPT_STAT_EN Card Interrupt Status Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RW	0x0	CARD_REMOVAL_STAT_EN Card Removal Status Enable. Values: 1'b0: Masked 1'b1: Enabled

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Bit	Attr	Reset Value	Description
6	RW	0x0	CARD_INSERTION_STAT_EN Card Insertion Status Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	BUF_RD_READY_STAT_EN Buffer Read Ready Status Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	BUF_WR_READY_STAT_EN Buffer Write Ready Status Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	DMA_INTERRUPT_STAT_EN DMA Interrupt Status Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	BGAP_EVENT_STAT_EN Block Gap Event Status Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	XFER_COMPLETE_STAT_EN Transfer Complete Status Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_COMPLETE_STAT_EN Command Complete Status Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_ERROR_INT_STAT_EN

Address: Operational Base(0x2A330000) + offset (0x0036)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	BOOT_ACK_ERR_STAT_EN Boot Acknowledgment Error Status Enable.. Values: 1'b0: Masked 1'b1: Enabled
11	RW	0x0	RESP_ERR_STAT_EN Response Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
10	RW	0x0	TUNING_ERR_STAT_EN Tuning Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled

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Bit	Attr	Reset Value	Description
9	RW	0x0	ADMA_ERR_STAT_EN ADMA Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
8	RW	0x0	AUTO_CMD_ERR_STAT_EN Auto CMD Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RO	0x0	reserved
6	RW	0x0	DATA_END_BIT_ERR_STAT_EN Data End Bit Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	DATA_CRC_ERR_STAT_EN Data CRC Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	DATA_TOUT_ERR_STAT_EN Data Timeout Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	CMD_IDX_ERR_STAT_EN Command Index Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	CMD_END_BIT_ERR_STAT_EN Command End Bit Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	CMD_CRC_ERR_STAT_EN Command CRC Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_TOUT_ERR_STAT_EN Command Timeout Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_NORMAL_INT_SIGNAL_EN

Address: Operational Base(0x2A330000) + offset (0x0038)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	CQE_EVENT_SIGNAL_EN CQE Event Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

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Bit	Attr	Reset Value	Description
13:9	RO	0x00	reserved
8	RW	0x0	CARD_INTERRUPT_SIGNAL_EN Card Interrupt Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RW	0x0	CARD_REMOVAL_SIGNAL_EN Card Removal Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
6	RW	0x0	CARD_INSERTION_SIGNAL_EN Card Insertion Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	BUF_RD_READY_SIGNAL_EN Buffer Read Ready Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	BUF_WR_READY_SIGNAL_EN Buffer Write Ready Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	DMA_INTERRUPT_SIGNAL_EN DMA Interrupt Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	BGAP_EVENT_SIGNAL_EN Block Gap Event Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	XFER_COMPLETE_SIGNAL_EN Transfer Complete Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_COMPLETE_SIGNAL_EN Command Complete Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_ERROR_INT_SIGNAL_EN

Address: Operational Base(0x2A330000) + offset (0x003A)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	BOOT_ACK_ERR_SIGNAL_EN Boot Acknowledgment Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

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Bit	Attr	Reset Value	Description
11	RW	0x0	RESP_ERR_SIGNAL_EN Response Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
10	RW	0x0	TUNING_ERR_SIGNAL_EN Tuning Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
9	RW	0x0	ADMA_ERR_SIGNAL_EN ADMA Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
8	RW	0x0	AUTO_CMD_ERR_SIGNAL_EN Auto CMD Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RO	0x0	reserved
6	RW	0x0	DATA_END_BIT_ERR_SIGNAL_EN Data End Bit Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	DATA_CRC_ERR_SIGNAL_EN Data CRC Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	DATA_TOUT_ERR_SIGNAL_EN Data Timeout Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	CMD_IDX_ERR_SIGNAL_EN Command Index Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	CMD_END_BIT_ERR_SIGNAL_EN Command End Bit Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	CMD_CRC_ERR_SIGNAL_EN Command CRC Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_TOUT_ERR_SIGNAL_EN Command Timeout Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

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EMMC_AUTO_CMD_STAT

Address: Operational Base(0x2A330000) + offset (0x003C)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RO	0x0	CMD_NOT_ISSUED_AUTO_CMD12 Command Not Issued By Auto CMD12 Error. If this bit is set to 1, CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 1'b0: No Error 1'b1: Not Issued
6	RO	0x0	reserved
5	RO	0x0	AUTO_CMD_RESP_ERR Auto CMD Response Error. This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or CMD13. This status is ignored if any bit between D00 to D04 is set to 1. Values: 1'b0: No Error 1'b1: Error
4	RO	0x0	AUTO_CMD_IDX_ERR Auto CMD Index Error. This bit is set if the command index error occurs in response to a command. Values: 1'b0: No Error 1'b1: Error
3	RO	0x0	AUTO_CMD_EBIT_ERR Auto CMD End Bit Error. This bit is set when detecting that the end bit of command response is 0. Values: 1'b0: No Error 1'b1: End Bit Error Generated
2	RO	0x0	AUTO_CMD_CRC_ERR Auto CMD CRC Error. This bit is set when detecting a CRC error in the command response. Values: 1'b0: No Error 1'b1: CRC Error Generated
1	RO	0x0	AUTO_CMD_TOUT_ERR Auto CMD Timeout Error. This bit is set if no response is returned with 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, error status bits (D04-D01) are meaningless. Values: 1'b0: No Error 1'b1: Time out

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Bit	Attr	Reset Value	Description
0	RO	0x0	AUTO_CMD12_NOT_EXEC Auto CMD12 Not Executed. If multiple memory block data transfer is not started due to a command error, this bit is not set because it is not necessary to issue an Auto CMD12. Setting this bit to 1 means that the Host Controller cannot issue Auto CMD12 to stop multiple memory block data transfer, due to some error. If this bit is set to 1, error status bits (D04-D01) is meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 1'b0: Executed 1'b1: Not Executed

EMMC_HOST_CTRL2

Address: Operational Base(0x2A330000) + offset (0x003E)

Bit	Attr	Reset Value	Description
15	RW	0x0	PRESET_VAL_ENABLE Preset Value Enable. This bit enables automatic selection of SDCLK frequency and Driver strength Preset Value registers. When Preset Value Enable is set, SDCLK frequency generation (Frequency Select and Clock Generator Select) and the driver strength selection are performed by the controller. These values are selected from set of Preset Value registers based on selected speed mode. Values: 1'b0: SDCLK and Driver Strength are controlled by Host Driver 1'b1: Automatic Selection by Preset Value are Enabled
14	RW	0x0	ASYNC_INT_ENABLE Asynchronous Interrupt Enable. This bit can be set if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Values: 1'b0: Disabled 1'b1: Enabled
13	RW	0x0	ADDRESSING 64-bit Addressing. This bit is effective when Host Version 4 Enable is set to 1. Values: 1'b0: 32 bits addressing 1'b1: 64 bits addressing
12	RW	0x0	HOST_VER4_ENABLE Host Version 4 Enable. This bit selects either Version 3.00 compatible mode or Version 4 mode. Values: 1'b0: Version 3.00 compatible mode 1'b1: Version 4 mode
11	RW	0x0	CMD23_ENABLE CMD23 Enable. If the card supports CMD23, this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 data transfer. Values: 1'b0: Auto CMD23 is disabled 1'b1: Auto CMD23 is enabled

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Bit	Attr	Reset Value	Description
10	RW	0x0	ADMA2_LEN_MODE ADMA2 Length Mode. This bit selects ADMA2 Length mode to be either 16-bit or 26-bit. Values: 1'b0: 16-bit Data Length Mode 1'b1: 26-bit Data Length Mode
9	RO	0x0	reserved
8	RW	0x0	UHS2_IF_ENABLE This bit should be set to 0 for SD/eMMC Interface.
7	RW	0x0	SAMPLE_CLK_SEL Sampling Clock Select. This bit is used by the Host Controller to select the sampling clock in SD/eMMC mode to receive CMD and DAT. This bit is set by the tuning procedure and is valid after the completion of tuning (when Execute Tuning is cleared). Setting this bit to 1 means that tuning is completed successfully and setting this bit to 0 means that tuning has failed. Values: 1'b0: Fixed clock is used to sample data 1'b1: Tuned clock is used to sample data
6	RW	0x0	EXEC_TUNING Execute Tuning. This bit is set to 1 to start the tuning procedure in SD/eMMC speed modes and this bit is automatically cleared when tuning procedure is completed. Values: 1'b0: Not Tuned or Tuning completed 1'b1: Execute Tuning
5:4	RO	0x0	reserved
3	RW	0x0	SIGNALING_EN 1.8V Signalling Enable. Values: 1'b0: 3.3V Signalling 1'b1: 1.8V Signalling
2:0	RW	0x0	UHS_MODE_SEL UHS Mode/eMMC Speed Mode Select. These bits are used to select UHS mode in the SD mode of operation. In eMMC mode, these bits are used to select eMMC Speed mode. Values: UHS Mode: 3'h0: SDR12 3'h1: SDR25 3'h2: SDR50 3'h3: SDR104 3'h4: DDR50 Others: Reserved eMMC Mode: 3'h0: Legacy 3'h1: High Speed SDR 3'h3: HS200 3'h4: High Speed DDR 3'h7: HS400 Others: Reserved

EMMC_CAPABILITIES1

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Address: Operational Base(0x2A330000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x1	SLOT_TYPE Slot Type. These bits indicate usage of a slot by a specific Host System. 2'h0: Removable Card Slot 2'h1: Embedded Slot for One Device 2'h2: Shared Bus Slot (SD mode) 2'h3: Reserved
29	RO	0x0	ASYNC_INT_SUPPORT Asynchronous Interrupt Support (SD Mode only). Values: 1'b0: Asynchronous Interrupt Not Supported 1'b1: Asynchronous Interrupt Supported
28	RO	0x0	SYS_ADDR_64_V3 64-bit System Address Support for V3. This bit sets the Host controller to support 64-bit System Addressing of V3 mode. SDMA cannot be used in 64-bit Addressing in Version 3 Mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor can be enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 0) and DMA select (DMA_SEL =11b). Values: 1'b0: 64-bit System Address for V3 is Not Supported 1'b1: 64-bit System Address for V3 is Supported
27	RO	0x0	SYS_ADDR_64_V4 64-bit System Address Support for V4. This bit sets the Host Controller to support 64-bit System Addressing of V4 mode. When this bit is set to 1, full or part of 64-bit address must be used to decode the Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller registers is effective regardless of setting to 64-bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Addressing for version 4 is enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 1) and by setting 64-bit Addressing (ADDRESSING =1) in the Host Control 2 register. SDMA can be used and ADMA2 uses 128-bit Descriptor. Values: 1'b0: 64-bit System Address for V4 is Not Supported 1'b1: 64-bit System Address for V4 is Supported
26:24	RO	0x0	reserved
23	RO	0x1	SUS_RES_SUPPORT Suspense/Resume Support. This bit indicates whether the Host Controller supports Suspend/Resume functionality. If this bit is 0, the Host Driver does not issue either Suspend or Resume commands because the Suspend and Resume mechanism is not supported. Values: 1'b0: Not Supported 1'b1: Supported

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Bit	Attr	Reset Value	Description
22	RO	0x1	SDMA_SUPPORT SDMA Support. This bit indicates whether the Host Controller is capable of using SDMA to transfer data between the system memory and the Host Controller directly. Values: 1'b0: SDMA not Supported 1'b1: SDMA Supported
21	RO	0x1	HIGH_SPEED_SUPPORT High Speed Support. This bit indicates whether the Host Controller and the Host System supports High Speed mode and they can supply the SD Clock frequency from 25 MHz to 50 MHz. Values: 1'b0: High Speed not Supported 1'b1: High Speed Supported
20	RO	0x0	reserved
19	RO	0x1	ADMA2_SUPPORT ADMA2 Support. This bit indicates whether the Host Controller is capable of using ADMA2. Values: 1'b0: ADMA2 not Supported 1'b1: ADMA2 Supported
18	RO	0x1	EMBEDDED_8_BIT 8-bit Support for Embedded Device. This bit indicates whether the Host Controller is capable of using an 8-bit bus width mode. Values: 1'b0: 8-bit Bus Width not Supported 1'b1: 8-bit Bus Width Supported
17:16	RO	0x1	MAX_BLK_LEN Maximum Block Length. This bit indicates the maximum block size that the Host driver can read and write to the buffer in the Host Controller. The buffer transfers this block size without wait cycles. The transfer block length is always 512 bytes for the SD Memory irrespective of this bit. Values: 2'h0: 512 Byte 2'h1: 1024 Byte 2'h2: 2048 Byte 2'h3: Reserved

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Bit	Attr	Reset Value	Description
15:8	RO	0xc8	BASE_CLK_FREQ Base Clock Frequency for SD clock. These bits indicate the base (maximum) clock frequency for the SD Clock. The definition of these bits depends on the Host Controller Version. (1) 6-Bit Base Clock Frequency: This mode is supported by the Host Controller version 1.00 and 2.00. The upper 2 bits are not effective and are always 0. The unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. 8'h0: Get information through another method 8'h0: 1 MHz 8'h1: 2 MHz ..... 8'h3f: 63 MHz Others: Reserved (2) 8-Bit Base Clock Frequency: This mode is supported by the Host Controller version 3.00. The unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. 8'h0: Get information through another method 8'h0: 1 MHz 8'h0: 2 MHz ..... 8'hff: 255 MHz
7	RO	0x1	TOUT_CLK_UNIT Timeout Clock Unit. This bit shows the unit of base clock frequency used to detect Data Timeout Error. Values: 1'b0: KHz 1'b1: MHz
6	RO	0x0	reserved
5:0	RO	0x00	TOUT_CLK_FREQ Timeout Clock Frequency. This bit shows the base clock frequency used to detect Data Timeout Error. The Timeout Clock unit defines the unit of timeout clock frequency. It can be KHz or MHz. 6'h0: Get information through another method 6'h1: 1KHz / 1MHz 6'h2: 2KHz / 2MHz 6'h3: 3KHz / 3MHz ..... 6'h3f: 63KHz / 63MHz

EMMC_CAPABILITIES2

Address: Operational Base(0x2A330000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	ADMA3_SUPPORT ADMA3 Support. This bit indicates whether the Host Controller is capable of using ADMA3. Values: 1'b0: ADMA3 not Supported 1'b1: ADMA3 Supported
24	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
23:16	RO	0x0a	CLK_MUL Clock Multiplier. These bits indicate the clock multiplier of the programmable clock generator. Setting these bits to 0 means that the Host Controller does not support a programmable clock generator. Values: 8'h0: Clock Multiplier is not Supported 8'h1: Clock Multiplier M = 2 8'h2: Clock Multiplier M = 3 ..... 8'hFF: Clock Multiplier M = 256
15:14	RO	0x0	RE_TUNING_MODES Re-Tuning Modes. Values: These bits select the re-tuning method and limit the maximum data length. Values: 2'h0: Timer 2'h1: Timer and Re-Tuning Request (Not supported) 2'h2: Auto Re-Tuning (for transfer) 2'h3: Reserved
13	RO	0x1	USE_TUNING_SDR50 Use Tuning for SDR50. Values: 1'b0: SDR50 does not require tuning 1'b1: SDR50 requires tuning
12	RO	0x0	reserved
11:8	RO	0x0	RETUNE_CNT Timer Count for Re-Tuning. Values: 4'h0: Re-Tuning Timer disabled 4'h1: 1 seconds 4'h2: 2 seconds 4'h3: 4 seconds ..... 4'hB: 1024 seconds 4'hC~4'hE: Reserved 4'hF: Get information from other source
7	RO	0x0	reserved
6	RO	0x1	DRV_TYPED This bit indicates support of Driver Type D for 1.8 Signaling. Values: 1'b0: Driver Type D is Not Supported 1'b1: Driver Type D is Supported
5	RO	0x1	DRV_TYPEC This bit indicates support of Driver Type C for 1.8 Signaling. Values: 1'b0: Driver Type C is Not Supported 1'b1: Driver Type C is Supported
4	RO	0x1	DRV_TYPEA This bit indicates support of Driver Type A for 1.8 Signaling. Values: 1'b0: Driver Type A is Not Supported 1'b1: Driver Type A is Supported

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Bit	Attr	Reset Value	Description
3	RO	0x0	UHS2_SUPPORT UHS-II Support. Values: 1'b0: UHS-II is Not Supported 1'b1: UHS-II is Supported
2	RO	0x1	DDR50_SUPPORT DDR50 Support. Values: 1'b0: DDR50 is Not Supported 1'b1: DDR50 is Supported
1	RO	0x1	SDR104_SUPPORT SDR104 Support. Values: 1'b0: SDR104 is Not Supported 1'b1: SDR104 is Supported
0	RO	0x1	SDR50_SUPPORT SDR50 Support. Values: 1'b0: SDR50 is Not Supported 1'b1: SDR50 is Supported

EMMC_FORCE_AUTO_CMD_STAT

Address: Operational Base(0x2A330000) + offset (0x0050)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	WO	0x0	FORCE_CMD_NOT_ISSUED_AUTO_CMD12 Force Event for Command Not Issued By Auto CMD12 Error. Values: 1'b0: Not Affected 1'b1: Command Not Issued By Auto CMD12 Error Status is set
6	RO	0x0	reserved
5	WO	0x0	FORCE_AUTO_CMD_RESP_ERR Force Event for Auto CMD Response Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Response Error Status is set
4	WO	0x0	FORCE_AUTO_CMD_IDX_ERR Force Event for Auto CMD Index Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Index Error Status is set
3	WO	0x0	FORCE_AUTO_CMD_EBIT_ERR Force Event for Auto CMD End Bit Error. Values: 1'b0: Not Affected 1'b1: Auto CMD End Bit Error Status is set
2	WO	0x0	FORCE_AUTO_CMD_CRC_ERR Force Event for Auto CMD CRC Error. Values: 1'b0: Not Affected 1'b1: Auto CMD CRC Error Status is set
1	WO	0x0	FORCE_AUTO_CMD12_TOUT_ERR Force Event for Auto CMD Timeout Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Timeout Error Status is set

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Bit	Attr	Reset Value	Description
0	WO	0x0	FORCE_AUTO_CMD12_NOT_EXEC Force Event for Auto CMD12 Not Executed. Values: 1'b0: Not Affected 1'b1: Auto CMD12 Not Executed Status is set

EMMC_FORC_ERR_INT_STAT

Address: Operational Base(0x2A330000) + offset (0x0052)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	WO	0x0	FORCE_BOOT_ACK_ERR Force Event for Boot Acknowledge error. Values: 1'b0: Not Affected 1'b1: Boot Acknowledge Error Status is set
11	WO	0x0	FORCE_RESP_ERR Force Event for Response Error. Values: 1'b0: Not Affected 1'b1: Response Error Status is set
10	WO	0x0	FORCE_TUNING_ERR Force Event for Tuning Error Values: 1'b0: Not Affected 1'b1: Tuning Error Status is set
9	WO	0x0	FORCE_ADMA_ERR Force Event for ADMA Error. Values: 1'b0: Not Affected 1'b1: ADMA Error Status is set
8	WO	0x0	FORCE_AUTO_CMD_ERR Force Event for Auto CMD Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Error Status is set
7	RO	0x0	reserved
6	WO	0x0	FORCE_DATA_END_BIT_ERR Force Event for Data End Bit Error. Values: 1'b0: Not Affected 1'b1: Data End Bit Error Status is set
5	WO	0x0	FORCE_DATA_CRC_ERR Force Event for Data CRC Error. Values: 1'b0: Not Affected 1'b1: Data CRC Error Status is set
4	WO	0x0	FORCE_DATA_TOUT_ERR Force Event for Data Timeout Error. Values: 1'b0: Not Affected 1'b1: Data Timeout Error Status is set
3	WO	0x0	FORCE_CMD_IDX_ERR Force Event for Command Index Error. Values: 1'b0: Not Affected 1'b1: Command Index Error Status is set

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Bit	Attr	Reset Value	Description
2	WO	0x0	FORCE_CMD_END_BIT_ERR Force Event for Command End Bit Error. Values: 1'b0: Not Affected 1'b1: Command End Bit Error Status is set
1	WO	0x0	FORCE_CMD_CRC_ERR Force Event for Command CRC Error. Values: 1'b0: Not Affected 1'b1: Command CRC Error Status is set
0	WO	0x0	FORCE_CMD_TOUT_ERR Force Event for Command Timeout Error. Values: 1'b0: Not Affected 1'b1: Command Timeout Error Status is set

EMMC_ADMA_ERR_STAT

Address: Operational Base(0x2A330000) + offset (0x0054)

Bit	Attr	Reset Value	Description
7:3	RO	0x00	reserved
2	RO	0x0	ADMA_LEN_ERR ADMA Length Mismatch Error States. This error occurs in the following instances: a. While the Block Count Enable is being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length; b. When the total data length cannot be divided by the block length Values: 1'b0: No Error 1'b1: Error
1:0	RO	0x0	ADMA_ERR_STATES ADMA Error States. These bits indicate the state of ADMA when an error occurs during ADMA data transfer. Values: 2'h0: Stop DMA - SYS_ADR register points to a location next to the error descriptor 2'h1: Fetch Descriptor - SYS_ADR register points to the error descriptor 2'h2: Never set this state 2'h3: Transfer Data - SYS_ADR register points to a location next to the error descriptor

EMMC_ADMA_SA_LOW

Address: Operational Base(0x2A330000) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_SA_LOW ADMA System Address. These bits indicate the lower 32 bits of the ADMA system address. a. SDMA: If Host Version 4 Enable is set to 1, this register stores the system address of the data location b. ADMA2: This register stores the byte address of the executing command of the descriptor table c. ADMA3: This register is set by ADMA3. ADMA2 increments the address of this register that points to the next line, every time a Descriptor line is fetched.

EMMC_ADMA_SA_HIGH

Address: Operational Base(0x2A330000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_SA_HIGH ADMA System Address. These bits indicate the higher 32 bits of the ADMA system address. a. SDMA: If Host Version 4 Enable is set to 1, this register stores the system address of the data location b. ADMA2: This register stores the byte address of the executing command of the descriptor table c. ADMA3: This register is set by ADMA3. ADMA2 increments the address of this register that points to the next line, every time a Descriptor line is fetched.

EMMC_PRESET_INIT

Address: Operational Base(0x2A330000) + offset (0x0060)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_DS

Address: Operational Base(0x2A330000) + offset (0x0062)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_HS

Address: Operational Base(0x2A330000) + offset (0x0064)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR12

Address: Operational Base(0x2A330000) + offset (0x0066)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR25

Address: Operational Base(0x2A330000) + offset (0x0068)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR50

Address: Operational Base(0x2A330000) + offset (0x006A)

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Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR104

Address: Operational Base(0x2A330000) + offset (0x006C)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_DDR50

Address: Operational Base(0x2A330000) + offset (0x006E)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_ADMA_ID_LOW

Address: Operational Base(0x2A330000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_ID_LOW ADMA Integrated Descriptor Address. These bits indicate the lower 32-bit of the ADMA Integrated Descriptor address. The start address of Integrated Descriptor is set to these register bits. The ADMA3 fetches one Descriptor Address and increments these bits to indicate the next Descriptor address.

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EMMC_ADMA_ID_HIGH

Address: Operational Base(0x2A330000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_ID_HIGH ADMA Integrated Descriptor Address. These bits indicate the higher 32-bit of the ADMA Integrated Descriptor address. The start address of Integrated Descriptor is set to these register bits. The ADMA3 fetches one Descriptor Address and increments these bits to indicate the next Descriptor address.

EMMC_SLOT_INTR_STATUS

Address: Operational Base(0x2A330000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:0	RO	0x00	INTR_SLOT Interrupt signal for each Slot. Host Controller support single card slot. This register shall always return 0.

EMMC_HOST_CNTRL_VERS

Address: Operational Base(0x2A330000) + offset (0x00FE)

Bit	Attr	Reset Value	Description
15:8	RO	0x10	VENDOR_VERSION_NUM Vendor Version Number.
7:0	RO	0x05	SPEC_VERSION_NUM Specification Version Number. Values: 8'h0: SD Host Controller Specification Version 1.00 8'h1: SD Host Controller Specification Version 2.00 8'h2: SD Host Controller Specification Version 3.00 8'h3: SD Host Controller Specification Version 4.00 8'h4: SD Host Controller Specification Version 4.10 8'h5: SD Host Controller Specification Version 4.20 Others: Reserved

EMMC_CQVER

Address: Operational Base(0x2A330000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x5	EMMC_VER_MAJOR eMMC Major Version Number (1st digit left of decimal point) in BCD format
7:4	RO	0x1	EMMC_VER_MINOR eMMC Minor Version Number(1st digit right of decimal point) in BCD format
3:0	RO	0x0	EMMC_VER_SUFFIX eMMC Version Suffix (2nd digit right of decimal point) in BCD format

EMMC_CQCAP

Address: Operational Base(0x2A330000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28	RO	0x0	CRYPTO_SUPPORT Crypto Support. This bit indicates whether the Host Controller supports cryptographic operations. Values: 1'b0: Crypto not Supported 1'b1: Crypto Supported
27:16	RO	0x000	reserved
15:12	RO	0x0	ITCFMUL Internal Timer Clock Frequency Multiplier. This field indicates the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details. 4'h0: 1 KHz clock 4'h1: 10 KHz clock 4'h2: 100 KHz clock 4'h3: 1 MHz clock 4'h4: 10 MHz clock Others: Reserved
11:10	RO	0x0	reserved
9:0	RO	0x000	ITCFVAL Internal Timer Clock Frequency Value. This field scales the frequency of the timer clock provided by ITCFMUL. The Final clock frequency of actual timer clock is calculated as ITCFVAL* ITCFMUL.

EMMC_CQCFG

Address: Operational Base(0x2A330000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	DCMD_EN Direct Command (DCMD) Enable. This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Values: 1'b0: Task descriptor in slot #31 is a Data Transfer Task Descriptor 1'b1: Task descriptor in slot #31 is a DCMD Task Descriptor
11:9	RO	0x0	reserved
8	RW	0x0	TASK_DESC_SIZE This bit indicates the size of task descriptor used in host memory. This bit can only be configured when Command Queueing Enable bit is 0 (command queueing is disabled) Values: 1'b0: Task descriptor size is 64 bits 1'b1: Task descriptor size is 128 bits
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	CR_GENERAL_EN Crypto General Enable. Enable/Disable bit for Crypto Engine. If cryptographic operations are not supported, this status bit is reserved. Values: 1'b0: Disable cryptographic operations for all transactions 1'b1: Enable cryptographic operations for transactions where TD.CE=1 or CRNQP.CE=1
0	RW	0x0	CQ_EN Command Queueing Enable. When CQE is disable, the software controls the eMMC bus using the registers between the addresses 0x000 to 0x1FF. Before the software writes to this bit, the software verifies that the eMMC host controller is in idle state and there are no ongoing commands or data transfers. When software wants to exit command queuing mode, it clears all previous tasks (if any) before setting this bit to 0. Values: 1'b0: Disable command queuing 1'b1: Enable command queuing

EMMC_CQCTRL

Address: Operational Base(0x2A330000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	CLR_ALL_TASKS Clear all tasks. This bit can only be written when the controller is halted. This bit does not clear tasks in the device. The software has to use the CMDQ_TASK_MGMT command to clear device's queue. Values: 1'b0: Programming 0 has no effect 1'b1: Clears all the tasks in the controller
7:1	RO	0x00	reserved
0	RW	0x0	HALT Halt request and resume. Values: 1'b0: RESUME_CQE. Software writes 0 to this bit to exit from the halt state and resume CQE activity. 1'b1: HALT_CQE. Software writes 1 to this bit when it wants to acquire software control over the eMMC bus and to disable CQE from issuing command on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT). When the software writes 1, CQE completes the ongoing task (if any in progress). After the task is completed and the CQE is in idle state, CQE does not issue new commands and indicates to the software by setting this bit to 1. The software can poll on this bit until it is set to 1 and only then send commands on the eMMC bus.

EMMC_CQIS

Address: Operational Base(0x2A330000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RC/W1C	0x0	TCL Task Cleared Interrupt. This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL). Values: 1'b0: TCL Interrupt is not set 1'b1: TCL Interrupt is set
2	RC/W1C	0x0	RED Response Error Detected Interrupt. This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked. Values: 1'b0: RED Interrupt is not set 1'b1: RED Interrupt is set
1	RC/W1C	0x0	TCC Task Complete Interrupt. This status bit is asserted(if CQISTE.TCC=1) when at least one of the following two conditions are met: a. A task is completed and the INT bit is set in its Task Descriptor b. Interrupt caused by Interrupt Coalescing logic Values: 1'b0: TCC Interrupt is not set 1'b1: TCC Interrupt is set
0	RC/W1C	0x0	HAC Halt Complete Interrupt. This status bit is asserted (if CQISTE.HAC=1) when halt bit in CQCTL register transitions from 0 to 1 indicating that Hhost Controller has completed its current ongoing task and has entered halt state. Values: 1'b0: HAC Interrupt is not set 1'b1: HAC Interrupt is set

EMMC_CQISE

Address: Operational Base(0x2A330000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TCL_STE Task Cleared Interrupt status enable. Values: 1'b0: CQIS.TCL is disabled 1'b1: CQIS.TCL is set when its interrupt condition is active
2	RW	0x0	RED_STE Response Error Detected Interrupt status enable. Values: 1'b0: CQIS.RED is disabled 1'b1: CQIS.RED is set when its interrupt condition is active
1	RW	0x0	TCC_STE Task Complete Interrupt status enable. Values: 1'b0: CQIS.TCC is disabled 1'b1: CQIS.TCC is set when its interrupt condition is active

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Bit	Attr	Reset Value	Description
0	RW	0x0	HAC_STE Halt Complete Interrupt status enable. Values: 1'b0: CQIS.HAC is disabled 1'b1: CQIS.HAC is set when its interrupt condition is active

EMMC_CQISGE

Address: Operational Base(0x2A330000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TCL_SGE Task Cleared Interrupt signal enable. Values: 1'b0: CQIS.TCL interrupt signal generation is disabled 1'b1: CQIS.TCL interrupt signal generation is active
2	RW	0x0	RED_SGE Response Error Detected Interrupt signal enable. Values: 1'b0: CQIS.RED interrupt signal generation is disabled 1'b1: CQIS.RED interrupt signal generation is active
1	RW	0x0	TCC_SGE Task Complete Interrupt signal enable. Values: 1'b0: CQIS.TCC interrupt signal generation is disabled 1'b1: CQIS.TCC interrupt signal generation is active
0	RW	0x0	HAC_SGE Halt Complete Interrupt signal enable. Values: 1'b0: CQIS.HAC interrupt signal generation is disabled 1'b1: CQIS.HAC interrupt signal generation is active

EMMC_CQIC

Address: Operational Base(0x2A330000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31	RW	0x0	INTC_EN Interrupt Coalescing Enable Bit. Values: 1'b0: Interrupt coalescing mechanism is disabled 1'b1: Interrupt coalescing mechanism is active. Interrupts are counted and timed, and coalesced interrupts are generated
30:21	RO	0x000	reserved
20	RO	0x0	INTC_STAT Interrupt Coalescing Status Bit. This bit indicates to the software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (that is, this is set if and only if INTC counter > 0). Values: 1'b0: INT0 Task completions have not occurred since last counter reset (INTC counter == 0) 1'b1: At least one INT0 task completion has been counted (INTC counter > 0)
19:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	WO	0x0	INTC_RST Counter and Timer Reset. When host driver writes 1, the interrupt coalescing timer and counter are reset. Values: 1'b0: No Effect 1'b1: Interrupt coalescing timer and counter are reset
15	WO	0x0	INTC_TH_WEN Interrupt Coalescing Counter Threshold Write Enable. When software writes 1 to this bit, the value INTC_TH is updated with the contents written on the same cycle. Values: 1'b0: Clears INTC_TH_WEN 1'b1: Sets INTC_TH_WEN
14:13	RO	0x0	reserved
12:8	WO	0x00	INTC_TH Interrupt Coalescing Counter Threshold filed. Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor), which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in INTC_TH, and generates interrupt. 5'h0: Interrupt coalescing feature disabled 5'h1: Interrupt coalescing interrupt generated after 1 task when INT=0 completes 5'h2: Interrupt coalescing interrupt generated after 2 tasks when INT=0 completes ..... 5'h1f: Interrupt coalescing interrupt generated after 31 tasks when INT=0 completes To write to this field, the INTC_TH_WEN bit must be set during the same write operation.
7	WO	0x0	TOUT_VAL_WEN When software writes 1 to this bit, the value TOUT_VAL is updated with the contents written on the same cycle. Values: 1'b0: clears TOUT_VAL_WEN 1'b1: Sets TOUT_VAL_WEN

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	TOUT_VAL Interrupt Coalescing Timeout Value. Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timer's unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. 7'h0: Timer is disabled. Timeout-based interrupt is not generated 7'h1: Timeout on 01x1024 cycles of timer clock frequency 7'h2: Timeout on 02x1024 cycles of timer clock frequency ..... 7'h7f: Timeout on 127x1024 cycles of timer clock frequency In order to write to this field, the TOUT_VAL_WEN bit must be set at the same write operation.

EMMC_CQTDLBA

Address: Operational Base(0x2A330000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDLBA Task Descriptor List Base Address. This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KB boundary. The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE.

EMMC_CQTDBR

Address: Operational Base(0x2A330000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DBR Command Queueing Task Doorbell. Software shall configure TDLBA, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. Writing 0 by the software does not have any impact on the hardware, and does not change the value of the register bit. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: a. When a task execution is completed (with success or error) b. The task is cleared using CQTCLR register

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Bit	Attr	Reset Value	Description
			c. All tasks are cleared using CQCTL register d. CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission, CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order.

EMMC_CQTCN

Address: Operational Base(0x2A330000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TCN Task Complete Notification. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Task-N has completed execution (with success or errors) Bit-N(0): Task-N has not completed, could be pending or not submitted. On task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

EMMC_CQDQS

Address: Operational Base(0x2A330000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DQS Device Queue Status. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Device has marked task N as ready for execution Bit-N(0): Task-N is not ready for execution. This task could be pending in device or not submitted. Host controller updates this register with response of the Device Queue Status command.

EMMC_CQDPT

Address: Operational Base(0x2A330000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DPT Device Pending Tasks. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Task-N has been successfully queued into the device and is awaiting execution. Bit-N(0): Task-N is not yet queued. Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task has not been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software reads this register in the task-discard procedure to determine if the task is queued in the device.

EMMC_CQTCLR

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Address: Operational Base(0x2A330000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TCLR Command Queueing Task Clear. Writing 1 to bit n of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once the clear operation is complete. Software must poll on the CQTCLR until it is cleared to verify that a clear operation was done.

EMMC_CQSSC1

Address: Operational Base(0x2A330000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x1	SQSCMD_BLK_CNT Send Status Command Block Counter. This field indicates when SQS CMD is sent while data transfer is in progress. A value of 'n' indicates that CQE sends status command on the CMD line, during the transfer of data block BLOCK_CNT-n, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. 4'h0: SEND_QUEUE_STATUS (CMD13) command is not sent during the transaction. Instead, it is sent only when the data lines are idle. 4'h1: SEND_QUEUE_STATUS command is to be sent during the last block of the transaction. 4'h2: SEND_QUEUE_STATUS command when last 2 blocks are pending. 4'h3: SEND_QUEUE_STATUS command when last 3 blocks are pending. ..... 4'hf: SEND_QUEUE_STATUS command when last 15 blocks are pending. Should be programmed only when CQCFG.CQ_EN is '0'.
15:0	RW	0x1000	SQSCMD_IDLE_TMR Send Status Command Idle Timer. This field configures the polling period to be used when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicates that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0x0001 (1 clock period) and the maximum value is 0xFFFF (65535 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 0x1000, the calculated polling period is 4096*52.08 ns= 213.33 ns. Should be programmed only when CQCFG.CQ_EN is '0'.

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EMMC_CQSSC2

Address: Operational Base(0x2A330000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	SQSCMD_RCA Send Queue RCA. This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE copies this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.

EMMC_CQCRDCT

Address: Operational Base(0x2A330000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DCMD_RESP Direct Command Last Response. This register contains the response of the command generated by the last direct command (DCMD) task that was sent. Contents of this register are valid only after bit 31 of CQTDBR register is cleared by the controller.

EMMC_CQRMEM

Address: Operational Base(0x2A330000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:0	RW	0xfdf9a080	RESP_ERR_MASK Response Mode Error Mask. The bits of this field are bit mapped to the device response. This bit is used as an interrupt mask on the device status filed that is received in R1/R1b responses. The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. 1'b0: When a R1/R1b response is received, bit i in the device status is ignored. 1'b1: When a R1/R1b response is received, with a bit i in the device status set, a RED interrupt is generated. Note: Responses to CMD13 (SQS) encode the QSR so that they are ignored by this logic.

EMMC_CQTERRI

Address: Operational Base(0x2A330000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31	RO	0x0	TRANS_ERR_FIELDS_VALID Data Transfer Error Field Valid. This bit is updated when an error is detected while a data transfer transaction was in progress. Values: 1'b0: Ignore contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX 1'b1: Data transfer related error detected. Check contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX fields
30:29	RO	0x0	reserved
28:24	RO	0x00	TRANS_ERR_TASKID Data Transfer Error Task ID. This field captures the ID of the task that was executed and whose data transfer has errors.
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RO	0x00	TRANS_ERR_CMD_INDX Data Transfer Error Command Index. This field captures the index of the command that was executed and whose data transfer has errors.
15	RO	0x0	RESP_ERR_FIELDS_VALID Response Mode Error Fields Valid. This bit is updated when an error is detected while a command transaction was in progress. Values: 1'b0: Ignore contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX 1'b1: Response-related error is detected. Check contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX fields
14:13	RO	0x0	reserved
12:8	RO	0x00	RESP_ERR_TASKID Response Mode Error Task ID. This field captures the ID of the task which was executed on the command line when the error occurred.
7:6	RO	0x0	reserved
5:0	RO	0x00	RESP_ERR_CMD_INDX Response Mode Error Command Index. This field captures the index of the command that was executed on the command line when the error occurred.

EMMC_CQCRI

Address: Operational Base(0x2A330000) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	CMD_RESP_INDX Last Command Response Index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

EMMC_CQCRA

Address: Operational Base(0x2A330000) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CMD_RESP_ARG Last Command Response Argument. This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

EMMC_VER_ID

Address: Operational Base(0x2A330000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VER_ID Current version number.

EMMC_VER_TYPE

Address: Operational Base(0x2A330000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VER_TYPE Version type.

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EMMC_HOST_CTRL3

Address: Operational Base(0x2A330000) + offset (0x0508)

Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4	RW	0x0	SW_CG_DIS Internal clock gating disable control. This bit must be used to disable IP's internal clock gating when required. When disabled clocks are not gated. Clocks to the core (except AHB bus clock) must be stopped when programming this bit. Values: 1'b0: Internal clock gating is disabled, clocks are not gated internally 1'b1: Internal clock gates are active and clock gating is controlled internally
3:1	RO	0x0	reserved
0	RW	0x0	CMD_CONFLICT_CHECK Command conflict check. This bit enables command conflict check. Host Controller monitors the CMD line whenever a command is issued and checks whether the value driven on command output line matches the value on command input line at next subsequent edge of transmit clock to determine command conflict error. This bit is cleared only if the feed back delay (including IO Pad delay) is more than (card clock period - flop setup time). Values: 1'b0: Disable command conflict check 1'b1: Check for command conflict after 1 card clock cycle

EMMC_EMMC_CTRL

Address: Operational Base(0x2A330000) + offset (0x052C)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RW	0x0	CQE_PREFETCH_DISABLE Enable or Disable CQE's PREFETCH feature. This field allows Software to disable CQE's data prefetch feature when set to 1. Values: 1'b0: CQE can prefetch data for successive WRITE transfers and pipeline successive READ transfers 1'b1: Prefetch for WRITE and Pipeline for READ are disabled
9	RW	0x0	CQE_ALGO_SEL Scheduler algorithm selected for execution. This bit selects the Algorithm used for selecting one of the many ready tasks for execution. Values: 1'b0: Priority based reordering with FCFS to resolve equal priority tasks 1'b1: First come First serve, in the order of DBR rings
8	RW	0x0	ENH_STROBE_ENABLE Enhanced Strobe Enable. This bit instructs Host to sample the CMD line using data strobe for HS400 mode. Values: 1'b0: CMD line is sampled using receive clock for HS400 mode 1'b1: CMD line is sampled using data strobe for HS400 mode
7:3	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x1	EMMC_RST_N EMMC Device Reset signal control. Values: 1'b0: Reset to eMMC device asserted 1'b1: Reset to eMMC device is de-asserted
1	RW	0x0	DISABLE_DATA_CRC_CHK Disable Data CRC Check. This bit controls masking of CRC16 error for Card Write in eMMC mode. This is useful in bus testing (CMD19) for an eMMC device. In bus testing, an eMMC card does not send CRC status for a block, which may generate CRC error. This CRC error can be masked using this bit during bus testing. Values: 1'b0: DATA CRC check is enabled 1'b1: DATA CRC check is disabled
0	RW	0x0	CARD_IS_EMMC eMMC Card present. This bit indicates the type of card connected. An application program this bit based on the card connected to Host Controller. Values: 1'b0: Card connected to Host Controller is a non-eMMC card 1'b1: Card connected to Host Controller is an eMMC card

EMMC_BOOT_CTRL

Address: Operational Base(0x2A330000) + offset (0x052E)

Bit	Attr	Reset Value	Description
15:12	RW	0x0	BOOT_TOUT_CNT Boot Acknowledge Timeout Counter Value. This value determines the interval by which boot acknowledge timeout (50 ms) is detected when boot acknowledge is expected during boot operation. Values: 4'h0: TMCLK x 2^13 4'h1: TMCLK x 2^14 ..... 4'hE: TMCLK x 2^27 4'hF: Reserved
11:9	RO	0x0	reserved
8	RW	0x0	BOOT_ACK_ENABLE Boot Acknowledge Enable. When this bit set, Host checks for boot acknowledge start pattern of 0-1-0 during boot operation. This bit is applicable for both mandatory and alternate boot mode. Values: 1'b1: Boot Acknowledge enable 1'b0: Boot Acknowledge disable
7	RW	0x0	VALIDATE_BOOT Validate Mandatory Boot Enable bit. This bit is used to validate the MAN_BOOT_EN bit. Values: 1'b1: Validate Mandatory boot enable bit 1'b0: Ignore Mandatory boot Enable bit
6:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	MAN_BOOT_EN Mandatory Boot Enable. This bit is used to initiate the mandatory boot operation. The application sets this bit along with VALIDATE_BOOT bit. Writing 0 is ignored. The Host Controller clears this bit after the boot transfer is completed or terminated. Values: 1'b1: Mandatory boot enable 1'b0: Mandatory boot disable

EMMC_AT_CTRL

Address: Operational Base(0x2A330000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:19	RW	0x0	POST_CHANGE_DLY Time taken for phase switching and stable clock output. Values: 2'h0: Less than 1-cycle latency 2'h1: Less than 2-cycle latency 2'h2: Less than 3-cycle latency 2'h3: Less than 4-cycle latency
18:17	RW	0x0	PRE_CHANGE_DLY Maximum Latency specification between transmit clock and receive clock. Values: 2'h0: Less than 1-cycle latency 2'h1: Less than 2-cycle latency 2'h2: Less than 3-cycle latency 2'h3: Less than 4-cycle latency
16	RW	0x0	TUNE_CLK_STOP_EN Clock stopping control for Tuning and auto-tuning circuit. When enabled, clock gate control output is pulled low before changing phase select codes. This effectively stops the receive clock. Changing phase code when clocks are stopped ensures glitch free phase switching. Values: 1'b0: Clocks not stopped 1'b1: Clocks stopped during phase code change
15:5	RO	0x000	reserved
4	RW	0x0	SW_TUNE_EN This fields enables software-managed tuning flow. Values: 1'b0: Software-managed tuning disabled 1'b1: Software-managed tuning enabled
3	RW	0x0	RPT_TUNE_ERR Framing errors are not generated when executing tuning. This debug bit allows users to report these errors. Values: 1'b0: Default mode where per host no errors are reported 1'b1: Debug mode for reporting framing errors

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Bit	Attr	Reset Value	Description
2	RW	0x0	SWIN_TH_EN Sampling window Threshold enable. Selects the tuning mode. Field should be programmed only when SAMPLE_CLK_SEL is '0'. Values: 1'b0: Tuning engine sweeps all taps and settles at the largest window. 1'b1: Tuning engine selects the first complete sampling window that meets the threshold set by SWIN_TH_VAL field.
1:0	RO	0x0	reserved

EMMC_AT_STAT

Address: Operational Base(0x2A330000) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	L_EDGE_PH_CODE Left Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Left edge of sampling window.
15:8	RO	0x00	R_EDGE_PH_CODE Right Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Right edge of sampling window.
7:0	RW	0x00	CENTER_PH_CODE Centered Phase code. Setting AT_CTRL.SW_TUNE_EN enables software to write to this field.

EMMC_DLL_CTRL

Address: Operational Base(0x2A330000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	DLL_ENCODER_SYNC_ENA DLL encoder value synchronization enable. 1'b0: Disable 1'b1: Enable. DLL encoder value can be synchronized to real-time value after DLL lock.
25	RW	0x0	DLL_ENCODER_SEL DLL encoder value selection. 1'b0: DLL encoder value update in real-time 1'b1: DLL encoder value update when DLL_ENCODER_SYNC_ENA changes from 0 to 1 and DLL has locked
24	RW	0x0	DLL_BYPASS_MODE DLL bypass mode enable. 1'b0: Normal 1'b1: Bypass. DLL doesn't execute phase detect to gain the DLL lock value.
23:16	RW	0x00	DLL_START_POINT DLL start point for phase detect.
15:8	RW	0x00	DLL_INCRMENT DLL increment value.
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	DLL_SRST DLL software reset indication. 1'b0: Normal work 1'b1: Reset
0	RW	0x0	DLL_START DLL working indication. 1'b0: DLL is not working 1'b1: DLL is working

EMMC_DLL_RXCLK

Address: Operational Base(0x2A330000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31	RW	0x0	RX_CLK_ORI_GATE Receive original clock source gating enable. 1'b0: Receive original clock source is not auto gating, active when card clock is stable and enable. 1'b1: Receive original clock source is auto gating, active when card is working.
30	RO	0x0	reserved
29	RW	0x0	RX_CLK_SRC_SEL Receive clock source selection. 1'b0: Receive clock source is transmit clock output 1'b1: Receive clock source is original clock input
28	RO	0x0	reserved
27	RW	0x0	RX_CLK_DLY_ENA Delay enable for receive clock output. 1'b0: Disable delay. Receive clock output comes from receive clock source, determined by RX_CLK_SRC_SEL. 1'b1: Enable delay. Receive clock output comes from delay line output of receive clock source.
26	RW	0x0	RX_DELAY_NUM_SEL Delay element number selection for receive clock. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (RX_DELAY_NUM)
25	RW	0x0	RX_TAP_VALUE_SEL Tap value selection for receive clock. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (RX_TAP_VALUE)
24	RW	0x0	RX_TAP_NUM_SEL Tap number selection for receive clock. 1'b0: Tap number comes from tuning result 1'b1: Tap number comes from software (RX_TAP_NUM)
23:16	RW	0x00	RX_DELAY_NUM Total delay element number of selected tap used for receive clock.
15:8	RW	0x00	RX_TAP_VALUE Tap value for receive clock. It denotes delay element number for receive clock cycle.
7:5	RO	0x0	reserved
4:0	RW	0x00	RX_TAP_NUM Tap number for receive clock. Every clock is divided into 32 taps equably. The selected tap number is RX_TAP_NUM+1. Use tap number to select tap used for receive clock.

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EMMC_DLL_TXCLK

Address: Operational Base(0x2A330000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	TX_CLK_SRC_SEL Transmit clock source selection. 1'b0: Transmit clock source is invertion of original clock input 1'b1: Transmit clock source is original clock input
28	RO	0x0	reserved
27	RW	0x0	TX_CLK_DLY_ENA Delay enable for transmit clock output. 1'b0: Disable delay. Transmit clock output comes from transmit clock source, determined by TX_CLK_SRC_SEL. 1'b1: Enable delay. Transmit clock output comes from delay line output of transmit clock source.
26	RW	0x0	TX_DELAY_NUM_SEL Delay element number selection for transmit clock. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (TX_DELAY_NUM)
25	RW	0x0	TX_TAP_VALUE_SEL Tap value selection for transmit clock. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (TX_TAP_VALUE)
24	RW	0x0	TX_TAP_NUM_SEL Tap number selection for transmit clock. 1'b0: Tap number is 8 1'b1: Tap number comes from software (TX_TAP_NUM)
23:16	RW	0x00	TX_DELAY_NUM Total delay element number of selected tap used for transmit clock.
15:8	RW	0x00	TX_TAP_VALUE Tap value for transmit clock. It denotes delay element number for transmit clock cycle.
7:5	RO	0x0	reserved
4:0	RW	0x00	TX_TAP_NUM Tap number for transmit clock. Every clock is divided into 32 taps equably. The selected tap number is TX_TAP_NUM+1. Use tap number to select tap used for transmit clock.

EMMC_DLL_STRBIN

Address: Operational Base(0x2A330000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	STRBIN_DELAY_ENA Delay enable for strobe input. 1'b0: Disable delay. Strobe input comes from original data strobe. 1'b1: Enable delay. Strobe input comes from delay line output of original data strobe.
26	RW	0x0	STRBIN_DELAY_NUM_SEL Delay element number selection for strobe input. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (STRBIN_DELAY_NUM)

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Bit	Attr	Reset Value	Description
25	RW	0x0	STRBIN_TAP_VALUE_SEL Tap value selection for strobe input. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (STRBIN_TAP_VALUE)
24	RW	0x0	STRBIN_TAP_NUM_SEL Tap number selection for strobe input. 1'b0: Tap number is 8 1'b1: Tap number comes from software (TAPNUM_TAP_NUM)
23	RO	0x0	reserved
22:16	RW	0x00	STRBIN_DELAY_NUM Total delay element number of selected tap used for strobe input.
15:8	RW	0x00	STRBIN_TAP_VALUE Tap value for strobe input. It denotes delay element number for strobe input cycle.
7:4	RO	0x0	reserved
3:0	RW	0x0	STRBIN_TAP_NUM Tap number for strobe input. Every clock is divided into 32 taps equably. The selected tap number is STRBIN_TAP_NUM+1. Use tap number to select tap used for strobe input.

EMMC_DLL_CMDOUT

Address: Operational Base(0x2A330000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RW	0x0	CMDOEN_SRC_SEL Command output enable selection. 2'b00: Command output enable is from register output triggered by clock rising edge 2'b01: Command output enable is from register output triggered by clock falling edge Others: Command output enable is from both register output triggered by clock rising edge and register output triggered by clock falling edge
28	RW	0x0	CMDOUT_SRC_SEL Command output source selection. 1'b0: Command output source is from register output triggered by clock rising edge 1'b1: Command output source is from register output triggered by clock falling edge
27	RW	0x0	CMDOUT_DELAY_ENA Delay enable for command output. 1'b0: Disable delay. Command output comes from command output source, determined by CMDOUT_SRC_SEL. 1'b1: Enable delay. Command output comes from delay line output of command output source.
26	RW	0x0	CMDOUT_DELAY_NUM_SEL Delay element number selection for command output. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (CMDOUT_DELAY_NUM)
25	RW	0x0	CMDOUT_TAP_VALUE_SEL Tap value selection for command output. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (CMDOUT_TAP_VALUE)

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Bit	Attr	Reset Value	Description
24	RW	0x0	CMDOUT_TAP_NUM_SEL Tap number selection for command output. 1'b0: Tap number is 0 1'b1: Tap number comes from software (CMDOUT_TAP_NUM)
23	RO	0x0	reserved
22:16	RW	0x00	CMDOUT_DELAY_NUM Total delay element number of selected tap used for command output.
15:8	RW	0x00	CMDOUT_TAP_VALUE Tap value for command output. It denotes delay element number for command output.
7:4	RO	0x0	reserved
3:0	RW	0x0	CMDOUT_TAP_NUM Tap number for command output. Every clock is divided into 32 taps equably. The selected tap number is CMDOUT_TAP_NUM+1. Use tap number to select tap used for command output.

EMMC_MISC_CON

Address: Operational Base(0x2A330000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:3	RO	0x000000	reserved
2	RW	0x0	MEM_CLKGAT_ENABLE Memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
1	RW	0x0	INTCLK_EN_SW Host clock enable by software. 1'b0: Clock is gated when INTERNAL_CLK_EN is 0 1'b1: Clock is active when INTERNAL_CLK_EN is 0
0	RW	0x1	CLK_STABLE Host clock stable enable. 1'b0: Not stable 1'b1: Stable

EMMC_DLL_STATUS0

Address: Operational Base(0x2A330000) + offset (0x0840)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RO	0x0	DLL_LOCK_OVERFLOW Delay line lock value overflow. 1'b0: Not overflow 1'b1: Overflow. If DLL_LOCK_VALUE is greater than 128, lock value is overflow. It is recommended that you calculate the delay element number by software to do clock adjustment.
9	RO	0x0	DLL_LOCK_TIMEOUT Delay line phase detection timeout status. 1'b0: Not timeout 1'b1: Timeout
8	RO	0x0	DLL_LOCK Delay line lock indication. 1'b0: Delay line is not locked 1'b1: Delay line is locked

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	DLL_LOCK_VALUE Delay line lock value for half card clock cycle. It denotes the delay element number needed for delay line locked. It is valid when DLL_LOCK is high.

EMMC_DLL_STATUS1

Address: Operational Base(0x2A330000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	DLL_CMDOUT_DELAY_VALUE Delay element number used for command output
23	RO	0x0	reserved
22:16	RO	0x00	DLL_STRBIN_DELAY_VALUE Delay element number used for strobe input
15:8	RO	0x00	DLL_RXCLK_DELAY_VALUE Delay element number used for receive clock
7:0	RO	0x00	DLL_TXCLK_DELAY_VALUE Delay element number used for transmit clock

38.5 Interface Description

Table 38-1 EMMC Interface Description

Module Pin	Dir	PAD Name	IOMUX Setting
emmc_cclk	O	EMMC_CLK/FSPI0_CLK/SAI0_SDO3_M2/SAI0_SDI1_M2/PDM0_CLK0_M1/PWM2_CH7_M1/GPIO1_B1_d	TOP_IOC_GPIO1B_IOMUX_SEL_L[7:4]=4'h1
emmc_ccmd	I/O	EMMC_CMD/FSPI0_RSTN/FSPI0_CSN1/UART6_TX_M2/I2C7_SCL_M0/GPIO1_B0_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[3:0]=4'h1
emmc_cdata0	I/O	EMMC_D0/FSPI0_D0/SAI0_SCLK_M2/UART7_RTSN_M1/I2C2_SCL_M1/GPIO1_A0_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[3:0]=4'h1
emmc_cdata1	I/O	EMMC_D1/FSPI0_D1/SAI0_LRCK_M2/UART7_CTSN_M1/I2C2_SDA_M1/GPIO1_A1_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[7:4]=4'h1
emmc_cdata2	I/O	EMMC_D2/FSPI0_D2/SAI0_SDO1_M2/SAI0_SDI3_M2/PDM0_SDI3_M1/UART7_TX_M1/UART6_RTSN_M2/GPIO1_A2_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4'h1
emmc_cdata3	I/O	EMMC_D3/FSPI0_D3/SAI0_SDO2_M2/SAI0_SDI2_M2/PDM0_SDI1_M1/UART7_RX_M1/UART6_CTSN_M2/GPIO1_A3_u	TOP_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4'h1
emmc_cdata4	I/O	EMMC_D4/SAI0_MCLK_M2/SAI3_MCLK_M0/SPI0_CSN0_M2/GPIO1_A4_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[3:0]=4'h1
emmc_cdata5	I/O	EMMC_D5/SAI3_SCLK_M0/PDM0_SDI2_M1/SPI0_MOSI_M2/I2C9_SCL_M0/GPIO1_A5_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[7:4]=4'h1
emmc_cdata6	I/O	EMMC_D6/SAI3_LRCK_M0/PDM0_CLK1_M1/SPI0_MISO_M2/I2C9_SDA_M0/GPIO1_A6_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[11:8]=4'h1
emmc_cdata7	I/O	EMMC_D7/SAI0_SDO0_M2/SAI3_SDI_M0/SPI0_CLK_M2/GPIO1_A7_u	TOP_IOC_GPIO1A_IOMUX_SEL_H[15:12]=4'h1
emmc_strbin	I	EMMC_STRB/SAI0_SDI0_M2/SAI3_SDO_M0/PDM0_SDI0_M1/SPI0_CSN1_M2/GPIO1_B2_d	EMMC_STRB/SAI0_SDI0_M2/SAI3_SDO_M0/PDM0_SDI0_M1/SPI0_CSN1_M2/GPIO1_B2_d
emmc_rstn	O	EMMC_RSTN/FSPI0_CSN0/UART6_RX_M2/I2C7_SDA_M0/MIPI_TE_M3/PWM2_CH1_M0/GPIO1_B3_u	TOP_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

38.6 Application Notes

38.6.1 Clock Adjustment

Phase detection is needed if you want to know the card clock's precision before clock adjustment. The detection flow is as below:

(1) Set EMMC_DLL_CTRL[1]=1 to reset the EMMC DLL; then set EMMC_DLL_CTRL[1]=0 to dis-reset EMMC DLL;

(2) Set DLL_START_POINT in EMMC_DLL_CTRL[23:16]; set DLL_INCREMENT in EMMC_DLL_CTRL[15:8], and set EMMC_DLL_CTRL[0] to start the DLL phase detection.

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(3) Wait for DLL lock until EMMC_DLL_STATUS0[8] equals to 1. Get the EMMC_DLL_STATUS0[7:0] as the locked value for the half card clock cycle time.
(4) If EMMC_DLL_STATUS0[9]=1 and EMMC_DLL_STATUS0[8]=0, the detection is timeout, you can adjust the DLL_START_POINT or DLL_INCREMENT to re-detection; or bypass the detection if the total delay line length is short than half clock cycle. You need to set EMMC_DLL_CTRL[0] to 0 before you restart phase detection as(1)~(3).

After phase detection, the clock's precision is shown in EMMC_DLL_STATUS0[7:0] (DLL_LOCK_VALUE) based on delay element.

We can calculate the delay element numbers requirement for transmit clock (TXCLK), receive clock (RXCLK), data strobe input (STRBIN), command output (CMDOUT), denoted as "XX" as follows:

(1) Get tap value: if XX_TAP_VALUE_SEL=0, tap value equals to (DLL_LOCK_VALUE*2)%256; else tap value is set by software, XX_TAP_VALUE;
(2) Get tap number: if XX_TAP_NUM_SEL=0, tap number comes from Host Controller; else tap number is set by software, XX_TAP_NUM;
(3) Get required delay element numbers: if XX_DELAY_NUM_SEL=0, delay element number equals to tap value* tap number; else delay element number is set by software, XX_DELAY_NUM.

The adjustment value for every cycle (XX) is equals to required delay element numbers*delay time of every element.

For STRBIN and CMDOUT, the max number of delay element is 128. The average delay for every delay element is 39ps~75ps, the total delay is 5ns~9.8ns, varies with VT.

For TXCLK and RXCLK, the max number of delay element is 256. The average delay for every delay element is 39ps~76ps, the total delay is 10ns~20ns, varies with VT.

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Chapter 39 Mobile Storage Host Controller (SDMMC&SDIO)

39.1 Overview

The Mobile Storage Host Controller is designed to support Secure Digital memory (SD-max version 3.01) with 1 bits or 4 bits data width, Multimedia Card(MMC-max version 4.51) with 1 bits or 4 bits or 8 bits data width.
The Host Controller is instantiated for SDMMC, SDIO. The interface difference between these instances is shown in "Interface Description".
The Host Controller supports following features:

- Bus Interface Features:
  - Support AMBA AHB interface for master and slave
  - Supports internal DMA interface(IDMAC)
    - Supports 16/32-bit data transfers
    - Single engine used for Transmit and Receive, which are mutually exclusive
    - Dual-buffer and chained descriptor linked list
    - Each descriptor can transfer up to 4KB of data in chained mode and 8KB of data in dual-buffer mode
    - Programmable burst size for optimal host bus utilization
  - Support combined single FIFO for both transmit and receive operations
  - Support FIFO size of 256x32
  - Support FIFO over-run and under-run prevention by stopping card clock
- Card Interface Features:
  - Support Secure Digital memory protocol commands
  - Support Secure Digital I/O protocol commands
  - Support Multimedia Card protocol commands
  - Support Command Completion Signal and interrupts to host
  - Support CRC generation and error detection
  - Support programmable baud rate
  - Support power management and power switch
  - Support card detection
  - Support write protection
  - Support hardware reset
  - Support SDIO interrupts in 1-bit and 4-bit modes
  - Support 4-bit mode in SDIO3.0
  - Support SDIO suspend and resume operation
  - Support SDIO read wait
  - Support block size of 1 to 65,535 bytes
  - Support 1-bit, 4-bit and 8-bit SDR modes
  - Supports 4-bit and 8-bit DDR
  - Support boot in 1-bit, 4-bit and 8-bit SDR modes
- Clock Interface Features:
  - Support 0/90/180/270-degree phase shift operation for sample clock (cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock(cclk_in) respectively
  - Support phase tuning using delay line for sample clock(cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock (cclk_in) respectively.
  - The max number of delay element is 128. The average delay for every delay element is 39ps~75ps, the total delay is 5ns~9ns, varies with VT.

39.2 Block Diagram

The Host Controller consists of the following main functional blocks.

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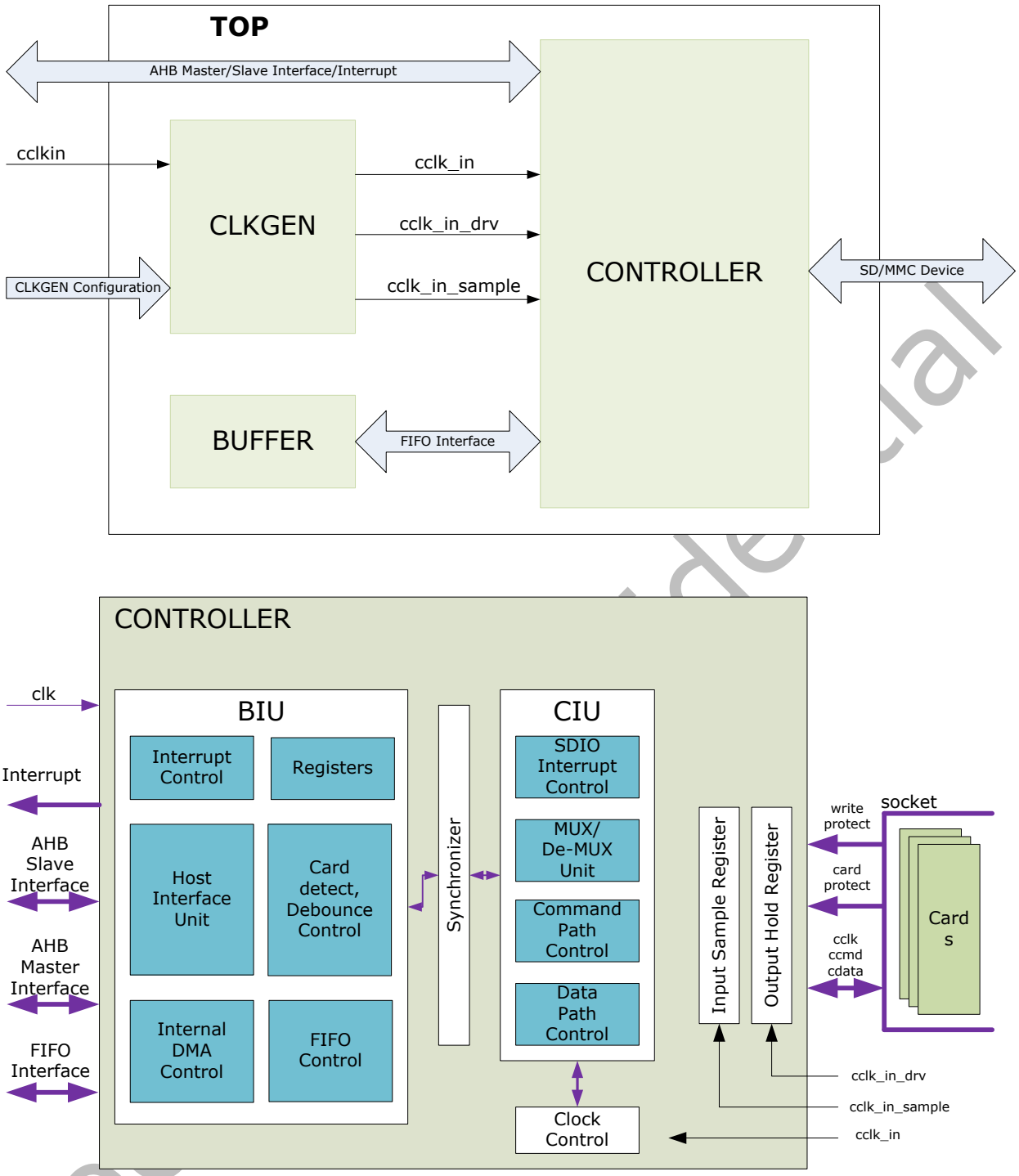

Fig. 39-1 Mobile Storage Host Control Block Diagram

- Clock Generate Unit (CLKGEN): Generates card interface clock cclk_in/ cclk_sample/cclk_drv based on cclkin and configuration information.
  - cclkin: original clock
  - cclk_in: functional clock
  - cclk_sample: sample clock
  - cclk_drv: driver clock
- Asynchronous dual-port memory (BUFFER): Use a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, and the other port is connected to the card clock.
- Bus Interface Unit (BIU): Provides AMBA AHB interfaces for register and data read/write.
- Card Interface Unit (CIU): Takes care of the SD/MMC protocols and provides clock management.

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39.3 Function Description

39.3.1 Bus Interface Unit

The Bus Interface Unit provides the following functions:

- Host interface
- Interrupt control
- Register access
- External FIFO access
- Card detection

39.3.1.1 Host Interface Unit

The Host Interface Unit is an AHB slave interface, which provides the interface between the SD/MMC card and the host bus.

39.3.1.2 Register Unit

The register unit is part of the bus interface unit; it provides read and write access to the registers.

All registers reside in the Bus Interface Unit clock domain. When a command is sent to a card by setting the start_bit, which is bit[31] of the SDMMC_CMD register, all relevant registers needed for the CIU operation are transferred to the CIU block. During this time, the registers that are transferred from the BIU to the CIU should not be written. The software should wait for the hardware to clear the start bit before writing to these registers again. The register unit has a hardware locking feature to prevent illegal writes to registers. The lock is necessary in order to avoid metastability violations, both because the host and card clock domains are different and to prevent illegal software operations.

Once a command start is issued by setting the start_bit of the SDMMC_CMD register, the following registers cannot be reprogrammed until the command is accepted by the card interface unit:

- SDMMC_CMD
- SDMMC_CMDARG
- SDMMC_BYTCNT
- SDMMC_BLKSIZ
- SDMMC_CLKDIV
- SDMMC_CLKENA
- SDMMC_CLKSRC
- SDMMC_TMOUT
- SDMMC_CTYPE

The hardware resets the start_bit once the CIU accepts the command. If a host write to any of these registers is attempted during this locked time, then the write is ignored and the hardware lock error bit is set in the raw interrupt status register. Additionally, if the interrupt is enabled and not masked for a hardware lock error, then an interrupt is sent to the host.

When the Card Interface Unit is in an idle state, it typically takes the following number of clocks for the command handshake, where clk is the BIU clock and cclk_in is the CIU clock:
3 (clk) + 3 (cclk_in)

Once a command is accepted, you can send another command to the CIU-which has a one-deep command queue-under the following conditions:

- If the previous command was not a data transfer command, the new command is sent to the SD/MMC card once the previous command completes.
- If the previous command is a data transfer command and if wait_prvdata_complete (bit[13]) of the SDMMC_CMD register is set for the new command, the new command is sent to the SD/MMC card only when the data transfer completes.

If the wait_prvdata_complete is 0, then the new command is sent to the SD/MMC card as soon as the previous command is sent. Typically, you should use this only to stop or abort a previous data transfer or query the card status in the middle of a data transfer.

39.3.1.3 Interrupt Controller Unit

The interrupt controller unit generates an interrupt that depends on the controller raw interrupt status, the interrupt-mask register, and the global interrupt-enable register bit.

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Once an interrupt condition is detected, it sets the corresponding interrupt bit in the raw interrupt status register SDMMC_RINTSTS. The raw interrupt status bit stays on until the software clears the bit by writing a 1 to the interrupt bit; a 0 leaves the bit untouched.
The interrupt port is an active-high, level-sensitive interrupt. The interrupt port is active only when any bit in the raw interrupt status register is active, the corresponding interrupt mask bit is 1, and the global interrupt enable bit is 1. The interrupt port is registered in order to avoid any combinational glitches.
The int_enable is reset to 0 on power-on, and the interrupt mask bits are set to 32'h0, which masks all the interrupts.

Notes:
Before enabling the interrupt, it is always recommended that you write 32'hffff_ffff to the raw interrupt status register in order to clear any pending unserviced interrupts. When clearing interrupts during normal operation, ensure that you clear only the interrupt bits that you serviced.
The SDIO Interrupts, Receive FIFO Data Request (RXDR), and Transmit FIFO Data Request (TXDR) are set by level-sensitive interrupt sources. Therefore, the interrupt source should be first cleared before you can clear the interrupt bit of the Raw Interrupt register. For example, on seeing the Receive FIFO Data Request (RXDR) interrupt, the FIFO should be emptied so that the "FIFO count greater than the RX-Watermark" condition, which triggers the interrupt, becomes inactive. The rest of the interrupts are triggered by a single clock-pulse-width source.

Table 39-1 Bits in Interrupt Status Register

Bits	Interrupt	Description
24	sdio_interrupt	Interrupt from SDIO card. In MMC-Ver3.3-only mode, these bits are always 0.
16	Card no-busy	If card exit busy status, the interrupt happened.
15	End Bit Error (read) / Write no CRC (EBE)	Error in end-bit during read operation, or no data CRC received during write operation. For MMC CMD19, there may be no CRC status returned by the card. Hence, EBE is set for CMD19. The application should not treat this as an error.
14	Auto Command Done (ACD)	Stop/abort commands automatically sent by card unit and not initiated by host; similar to Command Done (CD) interrupt. Recommendation: Software typically need not enable this for non CE-ATA accesses; Data Transfer Over (DTO) interrupt that comes after this interrupt determines whether data transfer has correctly competed.
13	Start Bit Error (SBE)	Error in data start bit when data is read from a card. In 4-bit mode, if DAT[0] line indicates start bit-that is, 0-and any of the other data bits do not have start bit, then this error is set. Busy Complete Interrupt when data is written to the card. This interrupt is generated after completion of busy driven by the card after the last data block is written into the card.
12	Hardware Locked write Error (HLE)	During hardware-lock period, write attempted to one of locked registers. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
11	FIFO Underrun/ Overrun Error (FRUN)	Host tried to push data when FIFO was full, or host tried to read data when FIFO was empty. Typically this should not happen, except due to error in software. Card unit never pushes data into FIFO when FIFO is full, and pop data when FIFO is empty. If IDMAC is enabled, FIFO under-run/over-run can

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Bits	Interrupt	Description
		occur due to a programming error on MSIZE and watermark values in SDMMC_FIFOTH register.
10	Data Starvation by Host Timeout (HTO)	To avoid data loss, card clock out is stopped if FIFO is empty when writing to card, or FIFO is full when reading from card. Whenever card clock is stopped to avoid data loss, data-starvation timeout counter is started with data-timeout value. This interrupt is set if host does not fill data into FIFO during write to card, or does not read from FIFO during read from card before timeout period. Even after timeout, card clock stays in stopped state, with CIU state machines waiting. It is responsibility of host to push or pop data into FIFO upon interrupt, which automatically restarts cclk_out and card state machines. Even if host wants to send stop/abort command, it still needs to ensure it has to push or pop FIFO so that clock starts in order for stop/abort command to send on command signal along with data that is sent or received on data line.
9	Data Read Timeout (DRTO)	In Normal functioning mode: Data read timeout (DRTO) Data timeout occurred. Data Transfer Over (DTO) also set if data timeout occurs. In Boot Mode: Boot Data Start (BDS) When set, indicates that Host Controller has started to receive boot data from the card. A write to this register with a value of 1 clears this interrupt.
8	Response Timeout (RTO)	In normal functioning mode: Response timeout (RTO) Response timeout occurred. Command Done (CD) also set if response timeout occurs. If command involves data transfer and when response times out, no data transfer is attempted by Host Controller. In Boot Mode: Boot Ack Received (BAR) When expect_boot_ack is set, on reception of a boot acknowledge pattern—0-1-0—this interrupt is asserted. A write to this register with a value of 1 clears this interrupt.
7	Data CRC Error (DCRC)	Received Data CRC does not match with locally-generated CRC in CIU. Can also occur if the Write CRC status is incorrectly sampled by the Host.
6	Response CRC Error (RCRC)	Response CRC does not match with locally-generated CRC in CIU.
5	Receive FIFO Data Request (RXDR)	Interrupt set during read operation from card when FIFO level is greater than Receive-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode: pop RX_WMark + 1 data from FIFO.
4	Transmit FIFO Data Request (TXDR)	Interrupt set during write operation to card when FIFO level reaches less than or equal to Transmit-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode:

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Bits	Interrupt	Description

		if (pending_bytes > (FIFO_DEPTH - TX_WMark))
		push (FIFO_DEPTH - TX_WMark) data into FIFO
		else
		push pending_bytes data into FIFO

3	Data Transfer Over (DTO)	Indicates Data transfer completed. Though on detection of errors-Start Bit Error, Data CRC error, and so on, DTO may or may not be set; the application must issue CMD12, which ensures that DTO is set. Recommendation: In non-DMA mode, when data is read from card, on seeing interrupt, host should read any pending data from FIFO. In DMA mode, DMA controllers guarantee FIFO is flushed before interrupt. DTO bit is set at the end of the last data block, even if the device asserts MMC busy after the last data block.
2	Command Done(CD)	Command sent to card and got response from card, even if Response Error or CRC error occurs.
1	Response Error (RE)	Error in received response set if one of following occurs: ● Transmission bit != 0 ● Command index mismatch ● End-bit != 1
0	Card-Detect (CDT)	When one or more cards inserted or removed, this interrupt occurs. Software should read card-detect register to determine current card status. Recommendation: After power-on and before enabling interrupts, software should read card detect register and store it in memory. When interrupt occurs, it should read card detect register and compare it with value stored in memory to determine which card(s) were removed/inserted. Before exiting ISR, software should update memory with new card-detect value.

39.3.1.4 FIFO Controller Unit

The FIFO controller interfaces the external FIFO to the host interface and the card controller unit. When FIFO overrun and under-run conditions occur, the card clock stops in order to avoid data loss.

The FIFO uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock(clk), and the second port is connected to the card clock(cclk_in).

39.3.1.5 Card Detection Unit

The register unit has registers that control the power. Power to each card can be selectively turned on or off.

The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounce associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value.

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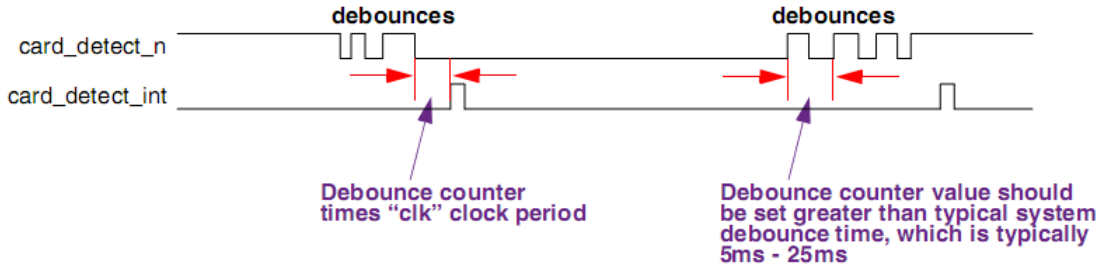

Fig. 39-2 SD/MMC Card-Detect Signal

39.3.2 Card Interface Unit

The Card Interface Unit (CIU) interfaces with the Bus Interface Unit (BIU) and the external devices. The host writes command parameters to the BIU control registers, and these parameters are then passed to the CIU. Depending on control register values, the CIU generates SD/MMC command and data traffic on a selected card bus according to SD/MMC protocol. The Host Controller accordingly controls the command and data path.

The following software restrictions should be met for proper CIU operation:

- Only one data transfer command can be issued at a time.
- During an open-ended card write operation, if the card clock is stopped because the FIFO is empty, the software must first fill the data into the FIFO and start the card clock. It can then issue only a stop/abort command to the card.
- When issuing card reset commands (CMD0, CMD15 or CMD52_reset) while a card data transfer is in progress, the software must set the stop_abort_cmd bit in the SDMMC_CMD register so that the Host Controller can stop the data transfer after issuing the card reset command.
- When the data end bit error is set in the SDMMC_RINTSTS register, the Host Controller does not guarantee SDIO interrupts. The software should ignore the SDIO interrupts and issue the stop/abort command to the card, so that the card stops sending the read data.
- If the card clock is stopped because the FIFO is full during a card read, the software should read at least two FIFO locations to start the card clock.

The CIU block consists of the following primary functional blocks:

- Command path
- Data path
- SDIO interrupt control
- Clock control
- Error detection

39.3.2.1 Command Path

The command path performs the following functions:

- Loads clock parameters
- Loads card command parameters
- Sends commands to card bus (ccmd_out line)
- Receives responses from card bus (ccmd_in line)
- Sends responses to BIU
- Drives the P-bit on command line

A new command is issued to the Host Controller by programming the BIU registers and setting the start_cmd bit in the SDMMC_CMD register. The BIU asserts start_cmd, which indicates that a new command is issued to the SD/MMC device. The command path loads this new command (command, command argument, timeout) and sends acknowledge to the BIU by asserting cmd_taken.

Once the new command is loaded, the command path state machine sends a command to the device bus-including the internally generated CRC7-and receives a response, if any. The state machine then sends the received response and signals to the BIU that the command is done, and then waits for eight clocks before loading a new command.

Load Command Parameters

One of the following commands or responses is loaded in the command path:

- New command from BIU – When start_cmd is asserted, then the start_cmd bit is set in the SDMMC_CMD register.

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- Internally generated auto-stop command – When the data path ends, the stop command request is loaded.
- IRQ response with RCA 0x000 – When the command path is waiting for an IRQ response from the MMC card and a "send irq response" request is signaled by the BIU, then the send_irq_response bit is set in the SDMMC_CTRL register.

Loading a new command from the BIU in the command path depends on the following SDMMC_CMD register bit settings:

- update_clock_registers_only – If this bit is set in the SDMMC_CMD register, the command path updates only the clock enable, clock divider, and clock source registers. If this bit is not set, the command path loads the command, command argument, and timeout registers; it then starts processing the new command.
- wait_prvdata_complete – If this bit is set, the command path loads the new command under one of the following conditions:
  - Immediately, if the data path is free (that is, there is no data transfer in progress), or if an open-ended data transfer is in progress (byte_count = 0).
  - After completion of the current data transfer, if a predefined data transfer is in progress.

Send Command and Receive Response

Once a new command is loaded in the command path, update_clock_registers_only bit is unset – the command path state machine sends out a command on the device bus; the command path state machine is illustrated in following figure.

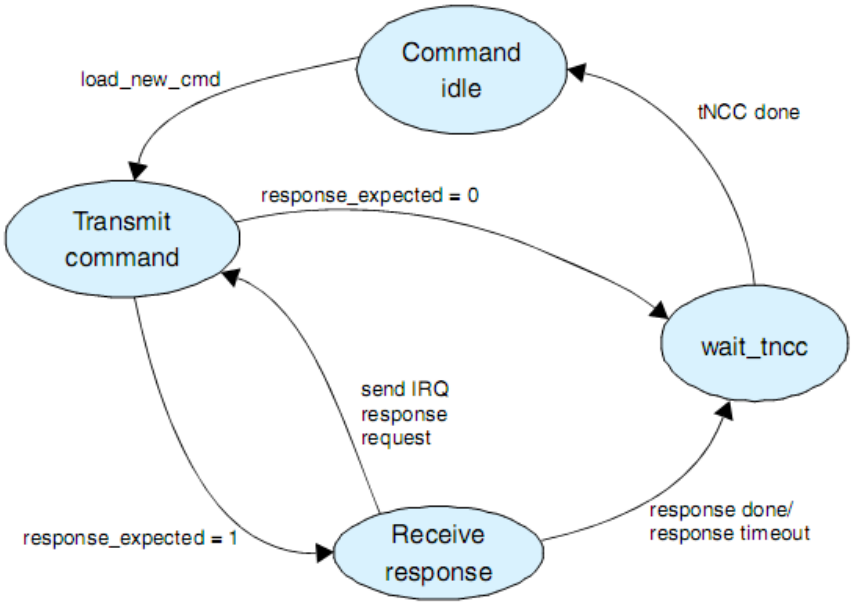

Fig. 38-3 Host Controller Command Path State Machine

The command path state machine performs the following functions, according to SDMMC_CMD register bit values:

- send_initialization – Initialization sequence of 80 clocks is sent before sending the command.
- response_expected – Response is expected for the command. After the command is sent out, the command path state machine receives a 48-bit or 136-bit response and sends it to the BIU. If the start bit of the card response is not received within the number of clocks programmed in the timeout register, then the response timeout and command done bit is set in the Raw Interrupt Status register as a signal to the BIU. If the response-expected bit is not set, the command path sends out a command and signals a response done to the BIU; that is, the command done bit is set in the Raw Interrupt Status register.
- response_length – If this bit is set, a 136-bit response is received; if it is not set, a 48-bit response is received.
- check_response_crc – If this bit is set, the command path compares CRC7 received in the response with the internally-generated CRC7. If the two do not match, the response CRC error is signaled to the BIU; that is, the response CRC error bit is set in

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the Raw Interrupt Status register SDMMC_RINTSTS.

Send Response to BIU

If the response_expected bit is set in the SDMMC_CMD register, the received response is sent to the BIU. The Response0 register is updated for a short response, and the Response3, Response2, Response1, and Response0 registers are updated on a long response, after which the Command Done bit is set. If the response is for an auto_stop command sent by the CIU, the response is saved in the Response1 register, after which the Auto Command Done bit is set.

Additionally, the command path checks for the following:

- Transmission bit = 0
- Command index matches command index of the sent command
- End bit = 1 in received card response

The command index is not checked for a 136-bit response or if the check_response_crc bit is unset. For a 136-bit response and reserved CRC 48-bit responses, the command index is reserved-that is, 111111.

Polling Command Completion Signal

The device generates the Command Completion Signal in order to notify the host controller of the normal command completion or command termination.

Command Completion Signal Detection and Interrupt to Host Processor

If the ccs_expected bit is set in the SDMMC_CMD register, the Command Completion Signal (CCS) from the device is indicated by setting the Data Transfer Over (DTO) bit in the SDMMC_RINTSTS register. The Host Controller generates a Data Transfer Over (DTO) interrupt if this interrupt is not masked.

Command Completion Signal Timeout

If the command expects a CCS from the device—if the ccs_expected bit is set in the SDMMC_CMD register—the command state machine waits for the CCS and remains in a wait_CCSS state. If the device fails to send out the CCS, the host software should implement a timeout mechanism to free the command and data path. The host controller does not implement a hardware timer; it is the responsibility of the host software to maintain a software timer.

In the event of a CCS timeout, the host should issue a CCSD by setting the send_ccsd bit in the CTRL register. The host controller command state machine sends the CCSD to the device and exits to an idle state. After sending the CCSD, the host should also send a CMD12 to the device in order to abort the outstanding command.

Send Command Completion Signal Disable

If the send_ccsd bit is set in the SDMMC_CTRL register, the host sends a Command Completion Signal Disable (CCSD) pattern on the CMD line. The host can send the CCSD while waiting for the CCS or after a CCS timeout happens.

After sending the CCSD pattern, the host sets the Command Done (CD) bit in SDMMC_RINTSTS and also generates an interrupt to the host if the Command Done interrupt is not masked.

39.3.2.2 Data Path

The data path block pops the data FIFO and transmits data on cdata_out during a write data transfer, or it receives data on cdata_in and pushes it into the FIFO during a read data transfer. The data path loads new data parameters—that is, data expected, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers—whenever a data transfer command is not in progress.

If the data_expected bit is set in the SDMMC_CMD register, the new command is a data transfer command and the data path starts one of the following:

- Transmit data if the read/write bit = 1
- Data receive if read/write bit = 0

Data Transmit

The data transmit state machine, illustrated in following figure, starts data transmission two clocks after a response for the data write command is received; this occurs even if the command path detects a response error or response CRC error. If a response is not received from the card because of a response timeout, data is not transmitted. Depending upon the value of the transfer_mode bit in the SDMMC_CMD register, the data transmit

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state machine puts data on the card data bus in a stream or in block(s).

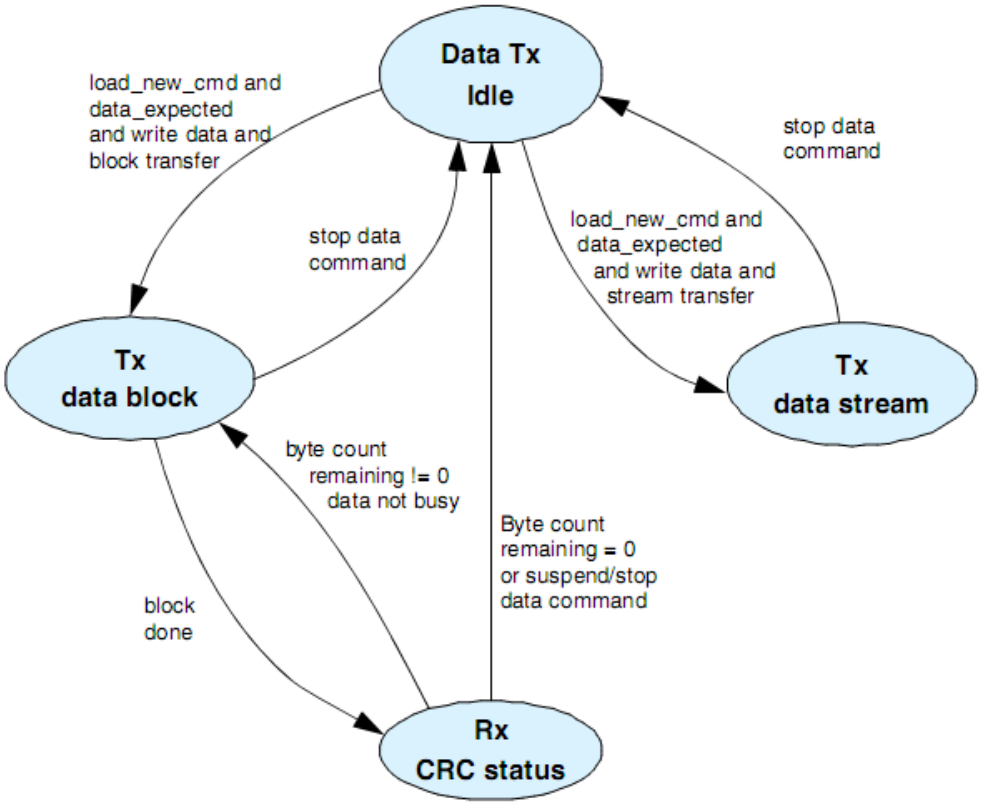

Fig. 39-4 Host Controller Data Transmit State Machine

Stream Data Transmit

If the transfer_mode bit in the SDMMC_CMD register is set to 1, it is a stream-write data transfer. The data path pops the FIFO from the BIU and transmits in a stream to the card data bus. If the FIFO becomes empty, the card clock is stopped and restarted once data is available in the FIFO.

If the byte_count register is programmed to 0, it is an open-ended stream-write data transfer. During this data transfer, the data path continuously transmits data in a stream until the host software issues a stop command. A stream data transfer is terminated when the end bit of the stop command and end bit of the data match over two clocks.

If the byte_count register is programmed with a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated and loaded in the command path when the end bit of the stop command occurs after the last byte of the stream write transfer matches.

This data transfer can also terminate if the host issues a stop command before all the data bytes are transferred to the card bus.

Single Block Data

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the byte_count register value is equal to the value of the block_size register, a single-block write-data transfer occurs. The data transmit state machine sends data in a single block, where the number of bytes equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set for a 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted for 1, 4, or 8 data lines, respectively.

After a single data block is transmitted, the data transmit state machine receives the CRC status from the card and signals a data transfer to the BIU; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register.

Additionally, if the start bit of the CRC status is not received by two clocks after the end of the data block, a CRC status start bit error is signaled to the BIU by setting the write-no-

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CRC bit in the SDMMC_RINTSTS register.

Multiple Block Data

A multiple-block write-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value in the byte_count register is not equal to the value of the block_size register. The data transmit state machine sends data in blocks, where the number of bytes in a block equals the block size, including the internally-generated CRC16. If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted on 1, 4, or 8 data lines, respectively.

After one data block is transmitted, the data transmit state machine receives the CRC status from the card. If the remaining byte_count becomes 0, the data path signals to the BIU that the data transfer is done; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If the remaining data bytes are greater than 0, the data path state machine starts to transmit another data block.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register, and continues further data transmission until all the bytes are transmitted.

Additionally, if the CRC status start bit is not received by two clocks after the end of a data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register; further data transfer is terminated.

If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated during the transfer of the last data block, where no extra bytes are transferred to the card. The end bit of the stop command may not exactly match the end bit of the CRC status in the last data block.

If the block size is less than 4, 16, or 32 for card data widths of 1 bit, 4 bits, or 8 bits, respectively, the data transmit state machine terminates the data transfer when all the data is transferred, at which time the internally generated stop command is loaded in the command path.

If the byte_count is 0 – the block size must be greater than 0 – it is an open-ended block transfer. The data transmit state machine for this type of data transfer continues the block-write data transfer until the host software issues a stop or abort command.

Data Receive

The data-receive state machine, illustrated in following figure, receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or response CRC error. If a response is not received from the card because a response timeout occurs, the BIU does not receive a signal that the data transfer is complete; this happens if the command sent by the Host Controller is an illegal operation for the card, which keeps the card from starting a read data transfer.

If data is not received before the data timeout, the data path signals a data timeout to the BIU and an end to the data transfer done. Based on the value of the transfer_mode bit in the SDMMC_CMD register, the data-receive state machine gets data from the card data bus in a stream or block(s).

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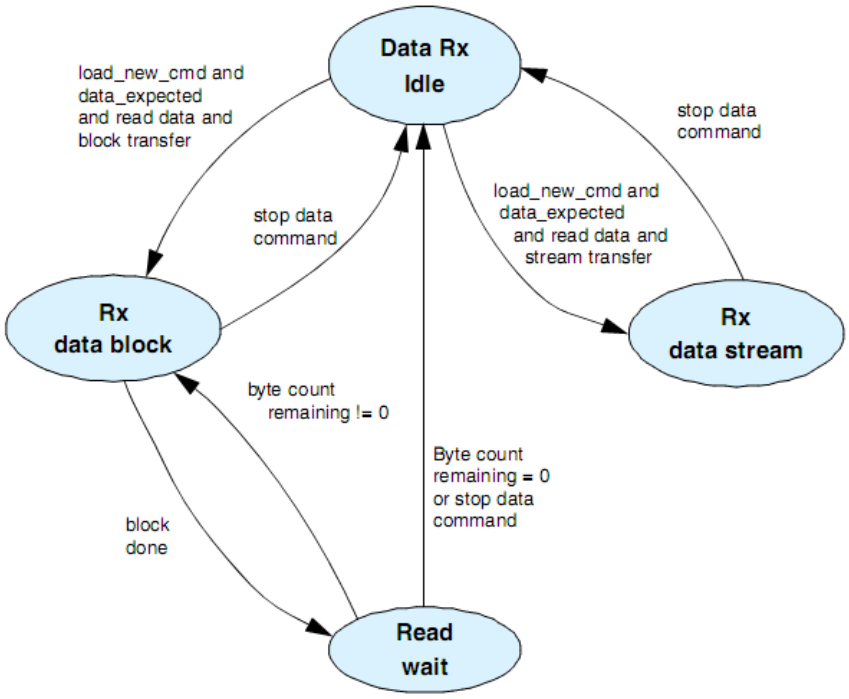

Fig. 39-5 Host Controller Data Receive State Machine

Stream Data Read

A stream-read data transfer occurs if the transfer_mode bit in the SDMMC_CMD register equals 1, at which time the data path receives data from the card and pushes it to the FIFO. If the FIFO becomes full, the card clock stops and restarts once the FIFO is no longer full.

An open-ended stream-read data transfer occurs if the byte_count register equals 0. During this type of data transfer, the data path continuously receives data in a stream until the host software issues a stop command. A stream data transfer terminates two clock cycles after the end bit of the stop command.

If the byte_count register contains a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, a stop command is internally generated and loaded into the command path, where the end bit of the stop command occurs after the last byte of the stream data transfer is received. This data transfer can terminate if the host issues a stop or abort command before all the data bytes are received from the card.

Single-Block Data Read

A single-block read-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is equal to the value of the block_size register. When a start bit is received before the data times out, data bytes equal to the block size and CRC16 are received and checked with the internally-generated CRC16. If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively. If there is a CRC16 mismatch, the data path signals a data CRC error to the BIU. If the received end bit is not 1, the BIU receives an end-bit error.

Multiple-Block Data Read

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is not equal to the value of the block_size register, it is a multiple-block read-data transfer. The data-receive state machine receives data in blocks, where the number of bytes in a block is equal to the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively.

After a data block is received, if the remaining byte_count becomes 0, the data path signals

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a data transfer to the BIU.
If the remaining data bytes are greater than 0, the data path state machine causes another data block to be received. If CRC16 of a received data block does not match the internally-generated CRC16, a data CRC error to the BIU and data reception continue further data transmission until all bytes are transmitted.
Additionally, if the end of a received data block is not 1, data on the data path signals terminate the bit error to the CIU and the data-receive state machine terminates data reception, waits for data timeout, and signals to the BIU that the data transfer is complete.
If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated when the last data block is transferred, where no extra bytes are transferred from the card; the end bit of the stop command may not exactly match the end bit of the last data block.
If the requested block size for data transfers to cards is less than 4, 16, or 32 bytes for 1-bit, 4-bit, or 8-bit data transfer modes, respectively, the data-transmit state machine terminates the data transfer when all data is transferred, at which point the internally-generated stop command is loaded in the command path. Data received from the card after that are then ignored by the data path.
If the byte_count is 0—the block size must be greater than 0—it is an open-ended block transfer. For this type of data transfer, the data-receive state machine continues the block-read data transfer until the host software issues a stop or abort command.

Auto-Stop

The Host Controller internally generates a stop command and is loaded in the command path when the send_auto_stop bit is set in the SDMMC_CMD register.
The software should set the send_auto_stop bit according to details listed in following table.

Table 39-2 Auto-Stop Generation

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count =0 is illegal
MMC	Single-block write	>0	No	Byte count =0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes①	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes①	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count =0 is illegal
SDMEM	Single-block write	>0	No	Byte count =0 illegal
SDMEM	Multiple-block read	0	No	Open-ended multiple block
SDMEM	Multiple-block read	>0	Yes	Auto-stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open-ended multiple block
SDMEM	Multiple-block write	>0	Yes	Auto-stop after all bytes transfer
SDIO	Single-block read	>0	No	Byte count =0 is illegal
SDIO	Single-block write	>0	No	Byte count =0 illegal
SDIO	Multiple-block	0	No	Open-ended multiple block

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Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
	read			
SDIO	Multiple-block read	>0	No	Pre-defined multiple block
SDIO	Multiple-block write	0	No	Open-ended multiple block
SDIO	Multiple-block write	>0	No	Pre-defined multiple block

*①:The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.*

The following list conditions for the auto-stop command.

- Stream read for MMC card with byte count greater than 0 – The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent out when the last byte of data is read from the card and no extra data byte is received. If the byte count is less than 6 (48 bits), a few extra data bytes are received from the card before the end bit of the stop command is sent.
- Stream write for MMC card with byte count greater than 0 - The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent when the last byte of data is transmitted on the card bus and no extra data byte is transmitted. If the byte count is less than 6 (48 bits), the data path transmits the data last in order to meet the above condition.
- Multiple-block read memory for SD card with byte count greater than 0 – If the block size is less than 4 (single-bit data bus), 16 (4-bit data bus), or 32 (8-bit data bus), the auto-stop command is loaded in the command path after all the bytes are read. Otherwise, the top command is loaded in the command path so that the end bit of the stop command is sent after the last data block is received.
- Multiple-block write memory for SD card with byte count greater than 0 – If the block size is less than 3 (single-bit data bus), 12 (4-bit data bus), or 24 (8-bit data bus), the auto-stop command is loaded in the command path after all data blocks are transmitted. Otherwise, the stop command is loaded in the command path so that the end bit of the stop command is sent after the end bit of the CRC status is received.

Precaution for host software during auto-stop – Whenever an auto-stop command is issued, the host software should not issue a new command to the SD/MMC device until the auto-stop is sent by the Host Controller and the data transfer is complete. If the host issues a new command during a data transfer with the auto-stop in progress, an auto-stop command may be sent after the new command is sent and its response is received; this can delay sending the stop command, which transfers extra data bytes. For a stream write, extra data bytes are erroneous data that can corrupt the card data. If the host wants to terminate the data transfer before the data transfer is complete, it can issue a stop or abort command, in which case the Host Controller does not generate an auto-stop command.

39.3.2.3 Non-Data Transfer Commands that Use Data Path

Some non-data transfer commands (non-read/write commands) also use the data path. Following table lists the commands and register programming requirements for them.

Table 39-5 Non-data Transfer Commands and Requirements

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
SDMMC_CMD register programming						
cmd_index	6'h1B	6'h1E	6'h2A	6'h0D	6'h16	6'h33
response_expect	1	1	1	1	1	1

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Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
rResponse_length	0	0	0	0	0	0
check_response_crc	1	1	1	1	1	1
data_expected	1	1	1	1	1	1
read/write	1	0	1	0	0	0
transfer_mode	0	0	0	0	0	0
send_auto_stop	0	0	0	0	0	0
wait_prevdata_complete	0	0	0	0	0	0
stop_abort_cmd	0	0	0	0	0	0
Command Argument register programming						
	stuff bits	32-bit write protect data address	stuff bits	stuff bits	stuff bits	stuff bits
Block Size register programming						
	16	4	Num_bytes①	64	4	8
Byte Count register programming						
	16	4	Num_bytes①	64	4	8

①: Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)

39.3.2.4 SDIO Interrupt Control

Interrupts for SD cards are reported to the BIU by asserting an interrupt signal for two clock cycles. SDIO cards signal an interrupt by asserting cdata_in low during the interrupt period; an interrupt period for the selected card is determined by the interrupt control state machine. An interrupt period is always valid for non-active or non-selected cards, and 1-bit data mode for the selected card. An interrupt period for a wide-bus active or selected card is valid for the following conditions:

- Card is idle
- Non-data transfer command in progress
- Third clock after end bit of data block between two data blocks
- From two clocks after end bit of last data until end bit of next data transfer command

Bear in mind that, in the following situations, the controller does not sample the SDIO interrupt of the selected card when the card data width is 4 bits. Since the SDIO interrupt is level-triggered, it is sampled in a further interrupt period and the host does not lose any SDIO interrupt from the card.

- Read/Write Resume – The CIU treats the resume command as a normal data transfer command. SDIO interrupts during the resume command are handled similarly to other data commands. According to the SDIO specification, for the normal data command the interrupt period ends after the command end bit of the data command; for the resume command, it ends after the response end bit. In the case of the resume command, the Controller stops the interrupt sampling period after the resume command end bit, instead of stopping after the response end bit of the resume command.

Suspend during read transfer – If the read data transfer is suspended by the host, the host sets the abort_read_data bit in the controller to reset the data state machine. In the CIU, the SDIO interrupts are handled such that the interrupt sampling starts after the abort_read_data bit is set by the host. In this case the controller does not sample SDIO interrupts between the period from response of the suspend command to setting the abort_read_data bit, and starts sampling after setting the abort_read_data bit.

39.3.2.5 Clock Control

The clock control block provides different clock frequencies required for SD/MMC cards. The cclk_in signal is the source clock (cclk_in >= card max operating frequency) for clock divider of the clock control block. This source clock (cclk_in) is used to generate different card clock frequencies (cclk_out). The card clock can have different clock frequencies, since the card can be a low-speed card or a full-speed card. The Host Controller provides one clock signal (cclk_out).

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The clock frequency of a card depends on the following clock control registers:

- Clock Divider register – Internal clock dividers are used to generate different clock frequencies required for card. The division factor for each clock divider can be programmed by writing to the Clock Divider register. A value of 0 represents a clock-divider bypass, a value of 1 represents a divide by 2.
- Clock Control register – cclk_out can be enabled or disabled for each card under the following conditions:
  - clk_enable – cclk_out for a card is enabled if the clk_enable bit for a card in the Clock Control register is programmed (set to 1) or disabled (set to 0).
  - Low-power mode – Low-power mode of a card can be enabled by setting the low-power mode bit of the Clock Control register to 1. If low-power mode is enabled to save card power, the cclk_out is disabled when the card is idle for at least 8 card clock cycles. It is enabled when a new command is loaded and the command path goes to a non-idle state.

Additionally, cclk_out is disabled when an internal FIFO is full – card read (no more data can be received from card) – or when the FIFO is empty – card write (no data is available for transmission). This helps to avoid FIFO overrun and underrun conditions. It is used by the command and data path to qualify cclk_in for driving outputs and sampling inputs at the programmed clock frequency for the selected card, according to the Clock Divider and Clock Source register values.

Under the following conditions, the card clock is stopped or disabled, along with the active clk_en, for the selected card:

- Clock can be disabled by writing to Clock Enable register (clk_en bit = 1).
- If low-power mode is selected and card is idle, or not selected for 8 clocks.
- FIFO is full and data path cannot accept more data from the card and data transfer is incomplete –to avoid FIFO overrun.

FIFO is empty and data path cannot transmit more data to the card and data transfer is incomplete – to avoid FIFO underrun.

39.3.2.6 Error Detection

- Response
  - Response timeout – Response expected with response start bit is not received within programmed number of clocks in timeout register.
  - Response CRC error – Response is expected and check response CRC requested; response CRC7 does not match with the internally-generated CRC7.
  - Response error – Response transmission bit is not 0, command index does not match with the command index of the send command, or response end bit is not 1.
- Data transmit
  - No CRC status – During a write data transfer, if the CRC status start bit is not received two clocks after the end bit of the data block is sent out, the data path does the following:
    - Signals no CRC status error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to the BIU
  - Negative CRC – If the CRC status received after the write data block is negative (that is, not 010), a data CRC error is signaled to the BIU and further data transfer is continued.
  - Data starvation due to empty FIFO – If the FIFO becomes empty during a write data transmission, or if the card clock is stopped and the FIFO remains empty for data timeout clocks, then a data-starvation error is signaled to the BIU and the data path continues to wait for data in the FIFO.
- Data receive
  - Data timeout – During a read-data transfer, if the data start bit is not received before the number of clocks that were programmed in the timeout register, the data path does the following:
    - Signals data-timeout error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to BIU

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- Data start bit error – During a 4-bit or 8-bit read-data transfer, if the all-bit data line does not have a start bit, the data path signals a data start bit error to the BIU and waits for a data timeout, after which it signals that the data transfer is done.
- Data CRC error – During a read-data-block transfer, if the CRC16 received does not match with the internally generated CRC16, the data path signals a data CRC error to the BIU and continues further data transfer.
- Data end-bit error – During a read-data transfer, if the end bit of the received data is not 1, the data path signals an end-bit error to the BIU, terminates further data transfer, and signals to the BIU that the data transfer is done.

Data starvation due to FIFO full – During a read data transmission and when the FIFO becomes full, the card clock is stopped. If the FIFO remains full for data timeout clocks, a data starvation error is signaled to the BIU (Data Starvation by Host Timeout bit is set in SDMMC_RINTSTS register) and the data path continues to wait for the FIFO to start to empty.

39.3.3 Internal Direct Memory Access Controller (IDMAC)

The Internal Direct Memory Access Controller (IDMAC) has a Control and Status Register (CSR) and a single Transmit/Receive engine, which transfers data from host memory to the device port and vice versa. The controller utilizes a descriptor to efficiently move data from source to destination with minimal Host CPU intervention. You can program the controller to interrupt the Host CPU in situations such as data Transmit and Receive transfer completion from the card, as well as other normal or error conditions.

The IDMAC and the Host driver communicate through a single data structure. CSR addresses 0x80 to 0x98 are reserved for host programming.

The IDMAC transfers the data received from the card to the Data Buffer in the Host memory, and it transfers Transmit data from the Data Buffer in the Host memory to the FIFO. Descriptors that reside in the Host memory act as pointers to these buffers.

A data buffer resides in physical memory space of the Host and consists of complete data or partial data. Buffers contain only data, while buffer status is maintained in the descriptor. Data chaining refers to data that spans multiple data buffers. However, a single descriptor cannot span multiple data.

A single descriptor is used for both reception and transmission. The base address of the list is written into Descriptor List Base Address Register (SDMMC_DBADDR @0x88). A descriptor list is forward linked. The Last Descriptor can point back to the first entry in order to create a ring structure. The descriptor list resides in the physical memory address space of the Host. Each descriptor can point to a maximum of two data buffers.

39.3.3.1 IDMAC CSR Access

When an IDMAC is introduced, an additional CSR space resides in the IDMAC that controls the IDMAC functionality. The host accesses the new CSR space in addition to the existing control register set in the BIU. The IDMAC CSR primarily contains descriptor information. For a write operation to the CSR, the respective CSR logic of the IDMAC and BIU decodes the address before accepting. For a read operation from the CSR, the appropriate CSR read path is enabled.

You can enable or disable the IDMAC operation by programming bit[25] in the SDMMC_CTRL register of the BIU. This allows the data transfer by accessing the slave interface on the AMBA bus if the IDMAC is present but disabled. When IDMAC is enabled, the FIFO cannot be accessed through the slave interface.

39.3.3.2 Descriptors

- Descriptor structures

The IDMAC uses these types of descriptor structures:

- Dual-Buffer Structure – The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (SDMMC_BMOD @0x80).

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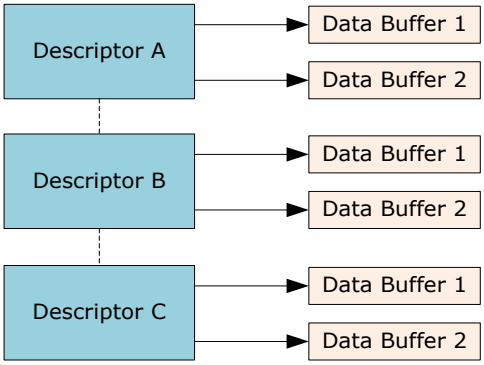

Fig. 39-6 Dual-Buffer Descriptor Structure

- Chain Structure – Each descriptor points to a unique buffer and the next descriptor.

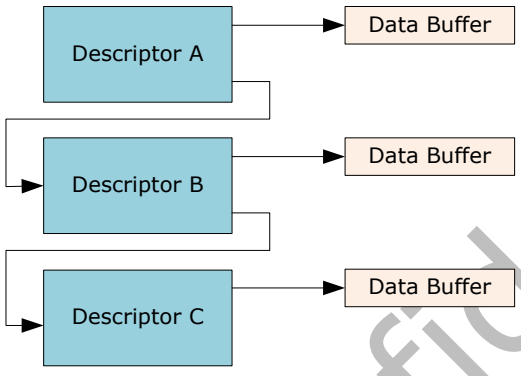

Fig. 39-7 Chain Descriptor Structure

- Descriptor formats

Following figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit AHB data buses. Each descriptor contains 16 bytes of control and status information. DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, DES3 to denote [127:96] bits.

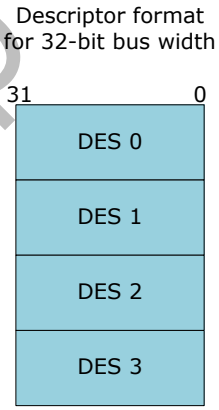

Fig. 39-8 Descriptor Formats for 32-bit AHB Address Bus Width

- The DES0 element in the IDMAC contains control and status information.

Table 39-4 Bits in IDMAC DES0 Element

Bit	Name	Description
31	OWN	When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the Host. The IDMAC clears this bit when it completes the data transfer.
30	Card Error Summary (CES)	These error bits indicate the status of the transaction to or from the card. These bits are also present in SDMMC_RINTSTS Indicates the logical OR of the following bits:

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Bit	Name	Description
		● EBE: End Bit Error ● RTO: Response Time out ● RCRC: Response CRC ● SBE: Start Bit Error ● DRTO: Data Read Timeout ● DCRC: Data CRC for Receive ● RE: Response Error
29:6	Reserved	-
5	End of Ring (ER)	When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.
4	Second Address Chained (CH)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.
3	First Descriptor (FS)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.
2	Last Descriptor (LD)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed to by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	Disable Interrupt on Completion (DIC)	When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in the buffer pointed to by this descriptor.
0	Reserved	-

■ The DES1 element contains the buffer size.

Table 39-5 Bits in IDMAC DES1 Element

Bit	Name	Description
31:26	Reserved	-
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

■ The DES2 element contains the address pointer to the data buffer.

Table 39-6 Bits in IDMAC DES2 Element

Bit	Name	Description
31:26	Reserved	
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the

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Bit	Name	Description
		buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 39-7 Bits in IDMAC DES3 Element

Bit	Name	Description
31:0	Buffer Address Pointer 2/ Next Descriptor Address (BAP2)	These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor address pointer must be bus-width aligned.

39.3.3.3 Initialization

IDMAC initialization occurs as follows:

1) Write to IDMAC Bus Mode Register—SDMMC_BMOD to set Host bus access parameters.
2) Write to IDMAC Interrupt Enable Register—SDMMC_IDINTEN to mask unnecessary interrupt causes.
3) The software driver creates either the Transmit or the Receive descriptor list. Then it writes to IDMAC Descriptor List Base Address Register (SDMMC_DBADDR), providing the IDMAC with the starting address of the list.
4) The IDMAC engine attempts to acquire descriptors from the descriptor lists.

- Host Bus Burst Access

The IDMAC attempts to execute fixed-length burst transfers on the AHB Master interface if configured using the FB bit of the IDMAC Bus Mode register. The maximum burst length is indicated and limited by the PBL field. The descriptors are always accessed in the maximum possible burst-size for the 16-bytes to be read— 16*8/bus-width.

The IDMAC initiates a data transfer only when sufficient space to accommodate the configured burst is available in the FIFO or the number of bytes to the end of data, when less than the configured burst-length.

The IDMAC indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length bursts, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise, in no fixed-length bursts, it transfers data using INCR (undefined length) and SINGLE transactions.

- Host Data Buffer Alignment

The Transmit and Receive data buffers in host memory must be aligned, depending on the data width.

- Buffer Size Calculations

The driver knows the amount of data to transmit or receive. For transmitting to the card, the IDMAC transfers the exact number of bytes to the FIFO, indicated by the buffer size field of DES1.

If a descriptor is not marked as last-LS bit of DES0-then the corresponding buffer(s) of the descriptor are full, and the amount of valid data in a buffer is accurately indicated by its buffer size field. If a descriptor is marked as last, then the buffer cannot be full, as

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indicated by the buffer size in DES1. The driver is aware of the number of locations that are valid in this case.

- Transmission

IDMAC transmission occurs as follows:

1) The Host sets up the elements (DES0-DES3) for transmission and sets the OWN bit (DES0[31]). The Host also prepares the data buffer.
2) The Host programs the write data command in the SDMMC_CMD register in BIU.
3) The Host will also program the required transmit threshold level (TX_WMark field in SDMMC_FIFOTH register).
4) The IDMAC determines that a write data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the IDMAC enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed transmit threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB Master Interface.
8) The IDMAC fetches the Transmit data from the data buffer in the Host memory and transfers to the FIFO for transmission to card.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data transmission is complete, status information is updated in SDMMC_IDSTS register by setting Transmit Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Reception

IDMAC reception occurs as follows:

1) The Host sets up the element (DES0-DES3) for reception, sets the OWN (DES0[31]).
2) The Host programs the read data command in the SDMMC_CMD register in BIU.
3) The Host will program the required receive threshold level (RX_WMark field in FIFOTH register).
4) The IDMAC determines that a read data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the DMA enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed receive threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB.
8) The IDMAC fetches the data from the FIFO and transfer to Host memory.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data reception is complete, status information is updated in SDMMC_IDSTS register by setting Receive Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Interrupts

Interrupts can be generated as a result of various events. SDMMC_IDSTS register contains

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all the bits that might cause an interrupt. SDMMC_IDINTEN register contains an Enable bit for each of the events that can cause an interrupt.
There are two groups of summary interrupts-Normal and Abnormal-as outlined in SDMMC_IDSTS register. Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal dmac_intr_o is de-asserted.
Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, Receive Interrupt—SDMMC_IDSTS[1] indicates that one or more data was transferred to the Host buffer.
An interrupt is generated only once for simultaneous, multiple events. The driver must scan SDMMC_IDSTS register for the interrupt cause.

39.3.3.4 Variable Delay/Clock Generation Unit

Variable delay mechanism for the cclk_in_drv is useful in order to meet a range of hold-time requirements across modes. Variable delay mechanism for the cclk_in_sample is mandatory and is required to achieve the correct sampling point for data.
The Clock Generation Unit (CLKGEN) includes Phase Shift Unit and Delay Line Unit.
The Phase Shift Unit can shift cclk_in_sample/cclk_in_drv by 0/90/180/270-degree relative to cclk_in. The Delay Line Unit can shift cclk_in_sample/cclk_in_drv step by step in the unit of delay element. The delay value range is 21ps~48ps for every delay element; the max delay element number is 128.
The architecture is as follows.

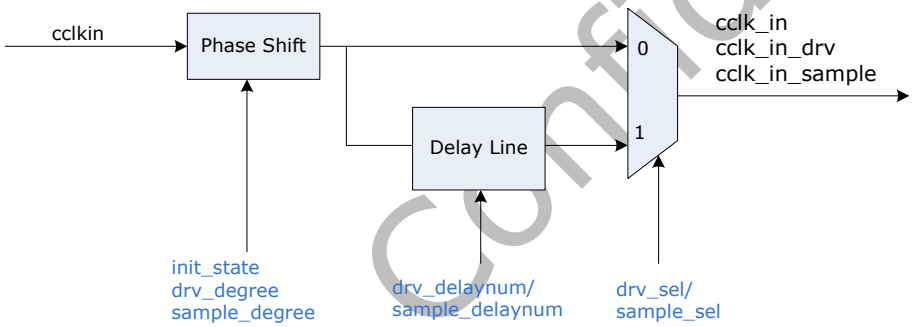

Fig. 39-9 Clock Generation Unit

39.4 Register Description

39.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SDMMC	0x2A310000
SDIO	0x2A320000

39.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SDMMC_CTRL	0x0000	W	0x00000000	Control register
SDMMC_PWREN	0x0004	W	0x00000000	Power enable register
SDMMC_CLKDIV	0x0008	W	0x00000000	Clock divider register
SDMMC_CLKSRC	0x000C	W	0x00000000	SD clock source register
SDMMC_CLKENA	0x0010	W	0x00000000	Clock enable register
SDMMC_TMOUT	0x0014	W	0xFFFFFF40	Timeout register
SDMMC_CTYPE	0x0018	W	0x00000000	Card type register
SDMMC_BLKSIZ	0x001C	W	0x00000200	Block size register
SDMMC_BYTCNT	0x0020	W	0x00000200	Byte count register
SDMMC_INTMASK	0x0024	W	0x00000000	Interrupt mask register

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Name	Offset	Size	Reset Value	Description
SDMMC_CMDARG	0x0028	W	0x00000000	Command argument register
SDMMC_CMD	0x002C	W	0x20000000	Command register
SDMMC_RESP0	0x0030	W	0x00000000	Response register 0
SDMMC_RESP1	0x0034	W	0x00000000	Response register 1
SDMMC_RESP2	0x0038	W	0x00000000	Response register 2
SDMMC_RESP3	0x003C	W	0x00000000	Response register 3
SDMMC_MINTSTS	0x0040	W	0x00000000	Masked interrupt status register
SDMMC_RINTSTS	0x0044	W	0x00000000	Raw interrupt status register
SDMMC_STATUS	0x0048	W	0x00000106	Status register
SDMMC_FIFOTH	0x004C	W	0x00FF0000	FIFO threshold register
SDMMC_CDETECT	0x0050	W	0x00000001	Card detect register
SDMMC_WRTPRT	0x0054	W	0x00000000	Write protect register
SDMMC_TCBCNT	0x005C	W	0x00000000	Transferred card byte count register
SDMMC_TBBCNT	0x0060	W	0x00000000	Transferred host to FIFO byte count register
SDMMC_DEBNCE	0x0064	W	0x00FFFFFF	Debounce count register
SDMMC_USRID	0x0068	W	0x20230001	User ID register
SDMMC_VERID	0x006C	W	0x5342270A	Version ID register
SDMMC_HCON	0x0070	W	0x04C434C1	Hardware configuration register
SDMMC_UHSREG	0x0074	W	0x00000000	UHS-1 control register
SDMMC_RSTN	0x0078	W	0x00000001	Hardware reset register
SDMMC_BMOD	0x0080	W	0x00000000	Bus mode register
SDMMC_PLDMND	0x0084	W	0x00000000	Poll demand register
SDMMC_DBADDR	0x0088	W	0x00000000	Descriptor list base address register
SDMMC_IDSTS	0x008C	W	0x00000000	Internal DMAC status register
SDMMC_IDINTEN	0x0090	W	0x00000000	Internal DMAC interrupt enable register
SDMMC_DSCADDR	0x0094	W	0x00000000	Current host descriptor address register
SDMMC_BUFADDR	0x0098	W	0x00000000	Current buffer descriptor address register
SDMMC_CARDTHRCTL	0x0100	W	0x00000000	Card threshold control register
SDMMC_BACKEND_POWER	0x0104	W	0x00000000	Back-end power register
SDMMC_EMMCDDR_REG	0x010C	W	0x00000000	eMMC4.5 DDR start bit detection control register
SDMMC_RDYINT_GEN	0x0120	W	0x00FF0000	Card ready interrupt generation control register
SDMMC_CLKGEN_CON0	0x0130	W	0x00000004	Clock generation control register 0
SDMMC_CLKGEN_CON1	0x0134	W	0x00000004	Clock generation control register 1
SDMMC_MISC_CON	0x0138	W	0x00000000	Miscellaneous control register
SDMMC_FIFO_BASE	0x0200	W	0x00000000	FIFO base address register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

39.4.3 Detail Register Description

SDMMC_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25	RW	0x0	use_internal_dmac Present only for the Internal DMAC configuration; else, it is reserved. 1'b0: The host performs data transfers through the slave interface 1'b1: Internal DMAC used for data transfer
24:12	RO	0x0000	reserved
11	RW	0x0	ceata_device_interrupt_status 1'b0: Interrupts not enabled in CE-ATA device 1'b1: Interrupts are enabled in CE-ATA device Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled. If the host enables CE-ATA device interrupt, then software should set this bit.
10	RW	0x0	send_auto_stop_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send internally generated STOP after sending CCSD to CE-ATA device NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together send_auto_stop_ccsd should not be set independent of send_ccsd. When set, the Host Controller automatically sends internally-generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in SDMMC_RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, the Host Controller automatically clears send_auto_stop_ccsd bit.
9	RW	0x0	send_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send Command Completion Signal Disable (CCSD) to CE-ATA device When set, the Host Controller sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, the Host Controller automatically clears send_ccsd bit. It also sets Command Done (CD) bit in SDMMC_RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS.
8	RW	0x0	abort_read_data 1'b0: No change 1'b1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.

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Bit	Attr	Reset Value	Description
7	RW	0x0	send_irq_response 1'b0: No change 1'b1: Send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, software issues CMD40, and the Host Controller waits for interrupt response from MMC card. In meantime, if software wants the Controller to exit waiting for interrupt state, it can set this bit, at which time the Host Controller command state-machine sends CMD40 response on bus and returns to idle state.
6	RW	0x0	read_wait 1'b0: Clear read wait 1'b1: Assert read wait For sending read-wait to SDIO cards.
5	RW	0x0	dma_enable 1'b0: Disable DMA transfer mode 1'b1: Enable DMA transfer mode Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside the controller to prioritize simultaneous host/DMA access.
4	RW	0x0	int_enable Global interrupt enable/disable bit 1'b0: Disable interrupts 1'b1: Enable interrupts The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.
3	RO	0x0	reserved
2	W1C	0x0	dma_reset 1'b0: No change 1'b1: Reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.
1	W1C	0x0	fifo_reset 1'b0: No change 1'b1: Reset to data FIFO to reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.
0	W1C	0x0	controller_reset 1'b0: No change 1'b1: Reset Host Controller To reset Host Controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: a. BIU/CIU interface b. CIU and state machines c. abort_read_data, send_irq_response, and read_wait bits of SDMMC_CTRL register d. start_cmd bit of SDMMC_CMD register Does not affect any registers or DMA interface, or FIFO or controller interrupts.

SDMMC_PWREN

Address: **Operational Base** + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	power_enable Power on/off switch for the card. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 1'b0: Power off 1'b1: Power on Bit values output to card_power_en port.

SDMMC_CLKDIV

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_divider0 Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, and so on. The recommended value is 0 or 1.

SDMMC_CLKSRC

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	clk_source Clock divider source. 2'b00: Clock divider 0 The cclk_out is always from clock divider 0, and this register is not implemented.

SDMMC_CLKENA

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	cclk_low_power Low-power control for SD card clock and MMC card clock supported. 1'b0: Non-low-power mode 1'b1: Low-power mode. Stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).
15:1	RO	0x0000	reserved
0	RW	0x0	cclk_enable Clock-enable control for SD card clock and MMC card clock supported. 1'b0: Clock disabled 1'b1: Clock enabled

SDMMC_TMOUT

Address: **Operational Base** + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:8	RW	0xffffff	data_timeout Value for card data read timeout; same value also used for data starvation by host timeout. Value is in number of card output clock. Note: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.
7:0	RW	0x40	response_timeout Response timeout value. Value is in number of card output clock cclk_out.

SDMMC_CTYPE

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	card_width_8 Indicates if card is 8-bit. 1'b0: Non 8-bit mode 1'b1: 8-bit mode
15:1	RO	0x0000	reserved
0	RW	0x0	card_width Indicates if card is 1-bit or 4-bit. 1'b0: 1-bit mode 1'b1: 4-bit mode

SDMMC_BLKSIZ

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0200	block_size Block size

SDMMC_BYTCNT

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	byte_count Number of bytes to be transferred; should be integer multiple of block size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.

SDMMC_INTMASK

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sdio_int_mask 1'b0: SDIO interrupt not masked 1'b1: SDIO interrupt masked
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_mask 1'b0: Data no busy interrupt not masked 1'b1: Data no busy interrupt masked

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_mask Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_CMDARG

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_arg Value indicates command argument to be passed to card

SDMMC_CMD

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	start_cmd Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD/MMC cards, Command Done bit is set in raw interrupt register.
30	RO	0x0	reserved
29	RW	0x1	use_hold_reg Use hold register. 1'b0: CMD and DATA sent to card bypassing hold register 1'b1: CMD and DATA sent to card through the hold register
28	RW	0x0	volt_switch Voltage switch bit. 1'b0: No voltage switching 1'b1: Voltage switching enabled; must be set for CMD11 only.
27	RW	0x0	boot_mode Boot mode selection. 1'b0: Mandatory boot operation 1'b1: Alternate boot operation
26	RW	0x0	disable_boot Disable boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do not set disable_boot and enable_boot together.

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Bit	Attr	Reset Value	Description
25	RW	0x0	expect_boot_ack Expect boot acknowledge. When software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.
24	RW	0x0	enable_boot Enable boot. This bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do not set disable_boot and enable_boot together.
23	RW	0x0	ccs_expected 1'b0: Interrupts are not enabled in CE-ATA device or command does not expect CCS from device 1'b1: Interrupts are enabled in CE-ATA device and RW_BLK command expects command completion signal from CE-ATA device If the command expects command completion signal (CCS) from the CE-ATA device, the software should set this control bit. The Host Controller sets data transfer over (DTO) bit in SDMMC_RINTSTS register and generates interrupt to host if data transfer over interrupt is not masked.
22	RW	0x0	read_ceata_device 1'b0: Host is not performing read access towards CE-ATA device 1'b1: Host is performing read access towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. The Host Controller should not indicate read data timeout while waiting for data from CE-ATA device.
21	RW	0x0	update_clock_regs_only 1'b0: Normal command sequence 1'b1: Do not send commands, just update clock register value into card clock domain. Following register values transferred into card clock domain: SDMMC_CLKDIV, SDMMC_CLRSRC, SDMMC_CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_regs_only = 0, following control registers are transferred from BIU to CIU: SDMMC_CMD, SDMMC_CMDARG, SDMMC_TMOUT, SDMMC_CTYPE, SDMMC_BLKSIZ, SDMMC_BYTCNT. CIU uses new register values for new command sequence to card. When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.
20:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15	RW	0x0	send_initialization 1'b0: Do not send initialization sequence (80 clocks of 1) before sending this command 1'b1: Send initialization sequence before sending this command After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).
14	RW	0x0	stop_abort_cmd 1'b0: Neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1'b1: Stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with SDMMC_CMD[26]=disable_boot.
13	RW	0x0	wait_prvdata_complete 1'b0: Send command at once, even if previous data transfer has not completed 1'b1: Wait for previous data transfer completion before sending command The wait_prvdata_complete=0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.
12	RW	0x0	send_auto_stop 1'b0: No stop command sent at end of data transfer 1'b1: Send stop command at end of data transfer When set, the Host Controller sends stop command to card at end of data transfer. a. When send_auto_stop bit should be set, since some data transfers do not need explicit stop commands b. Open-ended transfers that software should explicitly send to stop command Additionally, when "resume" is sent to resume-suspended memory access of SD-Combo card, bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.
11	RW	0x0	transfer_mode 1'b0: Block data transfer command 1'b1: Stream data transfer command Don't care if no data expected.
10	RW	0x0	wr 1'b0: Read from card 1'b1: Write to card Don't care if no data expected from card.
9	RW	0x0	data_expected 1'b0: No data transfer expected (read/write) 1'b1: Data transfer expected (read/write)

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Bit	Attr	Reset Value	Description
8	RW	0x0	check_response_crc 1'b0: Do not check response CRC 1'b1: Check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.
7	RW	0x0	response_length 1'b0: Short response expected from card 1'b1: Long response expected from card
6	RW	0x0	response_expect 1'b0: No response expected from card 1'b1: Response expected from card
5:0	RW	0x00	cmd_index Command index

SDMMC_RESP0

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response0 Bit[31:0] of response

SDMMC_RESP1

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response1 Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always "short" for them.

SDMMC_RESP2

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response2 Bit[95:64] of long response

SDMMC_RESP3

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response3 Bit[127:96] of long response

SDMMC_MINTSTS

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	sdio_interrupt SDIO interrupt status when sdio_int_mask is set
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_status Data no busy interrupt status when data_nobusy_int_mask is set

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	int_status Interrupt enabled only if corresponding bit in interrupt mask register is set. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_RINTSTS

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	R/WSC	0x0	sdio_interrupt Raw SDIO interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
23:17	RO	0x00	reserved
16	R/WSC	0x0	data_nobusy_int_status Raw data no busy interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
15:0	R/WSC	0x0000	int_status Raw interrupt status. Writes to bits clear status bit. Write value of 1 clears status bit, and value of 0 leaves bit intact. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_STATUS

Address: **Operational Base** + offset (0x0048)

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Bit	Attr	Reset Value	Description
31	RO	0x0	dma_req DMA request signal state
30	RO	0x0	dma_ack DMA acknowledge signal state
29:17	RO	0x0000	fifo_count Number of filled locations in FIFO
16:11	RO	0x00	response_index Index of previous response, including any auto-stop sent by core.
10	RO	0x0	data_state_mc_busy Data transmit or receive state-machine is busy
9	RO	0x0	data_busy Inverted version of raw selected card_data[0]. 1'b0: Card data not busy 1'b1: Card data busy
8	RO	0x1	data_3_status Raw selected card_data[3]; checks whether card is present. 1'b0: Card not present 1'b1: Card present
7:4	RO	0x0	command_fsm_states Command FSM states: 4'h0: Idle 4'h1: Send init sequence 4'h2: Tx cmd start bit 4'h3: Tx cmd tx bit 4'h4: Tx cmd index + arg 4'h5: Tx cmd crc7 4'h6: Tx cmd end bit 4'h7: Tx resp start bit 4'h8: Rx resp IRQ response 4'h9: Rx resp tx bit 4'ha: Rx resp cmd idx 4'hb: Rx resp data 4'hc: Rx resp crc7 4'hd: Rx resp end bit 4'he: Cmd path wait NCC 4'hf: Wait; CMD-to-response turnaround The command FSM state is represented using 19 bits. The SDMMC_STATUS register[7:4] has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the SDMMC_STATUS[7:4] register. The three states that are not represented in the SDMMC_STATUS register[7:4] are: Bit 16: Wait for CCS Bit 17: Send CCSD Bit 18: Boot Mode Due to this, while command FSM is in "Wait for CCS state" or "Send CCSD" or "Boot Mode", the SDMMC_STATUS register indicates status as 0 for the bit field [7:4].
3	RO	0x0	fifo_full FIFO is full status
2	RO	0x1	fifo_empty FIFO is empty status
1	RO	0x1	fifo_tx_watermark FIFO reached Transmit watermark level; not qualified with data transfer.

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Bit	Attr	Reset Value	Description
0	RO	0x0	fifo_rx_watermark FIFO reached Receive watermark level; not qualified with data transfer.

SDMMC_FIFOTH

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	dma_mutiple_transaction_size Burst size of multiple transaction; should be programmed same as DMA controller multiple-transaction-size SRC/DEST_MSIZE. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers The unit for transfer is 32bits.
27:16	RW	0x0ff	rx_wmark FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits-1 bit less than FIFO-count of status register, which is 13 bits. Limitation: rx_wmark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	tx_wmark FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits -1 bit less than FIFO-count of status register, which is 13 bits. Limitation: tx_wmark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)

SDMMC_CDETECT

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	card_detect_n Value on card_detect_n input port. 1'b0: Represents presence of card 1'b1: Represents absence of card

SDMMC_WRTPRT

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	write_protect Value on card_write_prt input port. 1 represents write protection.

SDMMC_TCBCNT

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_card_byte_count Number of bytes transferred by CIU unit to card

SDMMC_TBBCNT

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_fifo_byte_count Number of bytes transferred between host/DMA memory and BIU FIFO

SDMMC_DEBNCE

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:0	RW	0xffffff	debounce_count Number of host clock used by debounce filter logic; typical debounce time is 5-25 ms.

SDMMC_USRID

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x20230001	usrid User identification register

SDMMC_VERID

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x5342270a	verid Version identification register

SDMMC_HCON

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x1	area_optimized 1'b0: No area optimization 1'b1: Area optimization
25:24	RO	0x0	num_clk_div divider number-1.
23	RO	0x1	set_clk_false_path 1'b0: No false path 1'b1: False path set
22	RO	0x1	impl_hold_reg 1'b0: No hold register 1'b1: Hold register
21	RO	0x0	fifo_ram_inside 1'b0: Outside 1'b1: Inside
20:18	RO	0x1	ge_dma_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved
17:16	RO	0x0	dma_interface 2'b00: None 2'b01: INT_DMA 2'b10: GENERIC_DMA 2'b11: NON_INT_DMA
15:10	RO	0x0d	h_addr_width 6'h8: 9 bits 6'h9: 10 bits ..... 6'h1f: 32 bits Others: Reserved
9:7	RO	0x1	h_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved

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Bit	Attr	Reset Value	Description
6	RO	0x1	h_bus_type 1'b0: APB 1'b1: AHB
5:1	RO	0x00	card_num Card number -1.
0	RO	0x1	card_type Card type. 1'b0: MMC_ONLY 1'b1: SD_MMC

SDMMC_UHSREG

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	ddr_reg DDR mode. These bits indicate DDR mode of operation to the core for the data transfer. 1'b0: Non-DDR mode 1'b1: DDR mode
15:0	RO	0x0000	reserved

SDMMC_RSTN

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	card_reset Hardware reset. 1'b0: Active mode 1'b1: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

SDMMC_BMOD

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	pbl Programmable burst length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of SDMMC_FIFOTH register. In order to change this value, write the required value to SDMMC_FIFOTH register. This is an encode value as follows. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers Transfer unit is 32 bits. PBL is a read-only value and is applicable only for data access; it does not apply to descriptor accesses.
7	RW	0x0	de IDMAC enable. When set, the IDMAC is enabled.
6:2	RW	0x00	dsl Descriptor skip length. Specifies the number of word to skip between two unchained descriptors. This is applicable only for dual buffer structure.
1	RW	0x0	fb Fixed burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	RW	0x0	swr Software reset. When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle.

SDMMC_PLDMND

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	pd Poll demand. If the OWN bit of a descriptor is not set, the FSM goes to the suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation.

SDMMC_DBADDR

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sbl Start of descriptor list. Contains the base address of the first descriptor. The LSB bits[1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

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SDMMC_IDSTS

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:13	RO	0x0	fsm DMAC FSM present state. 4'h0: DMA_IDLE 4'h1: DMA_SUSPEND 4'h2: DESC_RD 4'h3: DESC_CHK 4'h4: DMA_RD_REQ_WAI 4'h5: DMA_WR_REQ_WAI 4'h6: DMA_RD 4'h7: DMA_WR 4'h8: DESC_CLOSE Others: Reserved
12:10	RO	0x0	eb Error bits. Indicates the type of error that caused a bus error. Valid only with fatal bus. 3'h1: Host abort received during transmission 3'h2: Host abort received during reception Others: Reserved
9	RW	0x0	ais Abnormal interrupt summary. Logical OR of the following: SDMMC_IDSTS[2] fatal bus interrupt SDMMC_IDSTS[4] du bit interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes ais to be set is cleared. Writing a 1 clears this bit.
8	RW	0x0	nis Normal interrupt summary. Logical OR of the following: SDMMC_IDSTS[0] transmit interrupt SDMMC_IDSTS[1] receive interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes nis to be set is cleared. Writing a 1 clears this bit.
7:6	RO	0x0	reserved
5	RW	0x0	ces Card error summary. Indicates the status of the transaction to/from the card; also present in SDMMC_RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot Ack Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a "response error"; however, it will not abort if the CES bit is cleared.

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Bit	Attr	Reset Value	Description
4	RW	0x0	dui Descriptor unavailable interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error interrupt. Indicates that a bus error occurred (SDMMC_IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	RW	0x0	ri Receive interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	RW	0x0	ti Transmit interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit.

SDMMC_IDINTEN

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ai Abnormal interrupt summary enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: SDMMC_IDINTEN[2] fatal bus error interrupt SDMMC_IDINTEN[4] du interrupt
8	RW	0x0	ni Normal interrupt summary enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: SDMMC_IDINTEN[0] transmit interrupt SDMMC_IDINTEN[1] receive interrupt
7:6	RO	0x0	reserved
5	RW	0x0	ces Card error summary interrupt enable. When set, it enables the card interrupt summary.
4	RW	0x0	du Descriptor unavailable interrupt. When set along with abnormal interrupt summary enable, the du interrupt is enabled.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error enable. When set with abnormal interrupt summary enable, the fatal bus error interrupt is enabled. When reset, fatal bus error enable interrupt is disabled.
1	RW	0x0	ri Receive interrupt enable. When set with normal interrupt summary enable, receive interrupt is enabled. When reset, receive interrupt is disabled.

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Bit	Attr	Reset Value	Description
0	RW	0x0	ti Transmit interrupt enable. When set with normal interrupt summary enable, transmit interrupt is enabled. When reset, transmit interrupt is disabled.

SDMMC_DSCADDR

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hda Host descriptor address pointer. This register points to the start address of the current descriptor read by the IDMAC. Cleared on reset. Pointer updated by IDMAC during operation.

SDMMC_BUFADDR

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hba Host buffer address pointer. This register points to the current data buffer address being accessed by the IDMAC. Cleared on Reset. Pointer updated by IDMAC during operation.

SDMMC_CARDTHRCTL

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	card_rd_thres Card read threshold size
15:2	RO	0x0000	reserved
1	RW	0x0	busy_clr_int_en Busy clear interrupt. 1'b0: Busy clear interrupt disabled 1'b1: Busy clear interrupt enabled Note: The application can disable this feature if it does not want to wait for a busy clear interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.
0	RW	0x0	card_rd_thres_en Card read threshold enable. 1'b0: Card read threshold disabled 1'b1: Card read threshold enabled. The host initiates read transfer only if card_rd_thres amount of space is available in receive FIFO.

SDMMC_BACKEND_POWER

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	back_end_power Back end power. 1'b0: Off; Reset 1'b1: Back-end power supplied to card application

SDMMC_EMMCDDR_REG

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	half_start_bit Control for start bit detection mechanism inside Host Controller based on duration of start bit. For eMMC 4.5, start bit can be: 1'b0: Full cycle (half_start_bit=0) 1'b1: Less than one full cycle (half_start_bit=1) Set half_start_bit=1 for eMMC 4.5 and above; set to 0 for SD applications.

SDMMC_RDYINT_GEN

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	rdyint_cnt_finish Counter finish indication. When high, it indicates that the rdyint counter is finished.
23:16	RO	0xff	rdyint_cnt_status Couner status, reflect internal counter value.
15:9	RO	0x00	reserved
8	RW	0x0	rdyint_gen_working Working indication for rdyint generator. When high, Host Controller start to count and generate one rdyint trigger. After the rdyint trigger is generated, this bit will be set to 0 by Host Controller. So software should set it to 1 before detecting next interrupt.
7:0	RW	0x00	rdyint_gen_maxval Max counter value to detect cdata_in0 high value for generating rdyint, based on internal clock frequency.

SDMMC_CLKGEN_CON0

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	drv_sel Selection for drive clock. 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:3	RW	0x00	drv_delaynum Delay element number configuration for drive clock. It can be modified when init_state=1 and should be stable when init_state=0.
2:1	RW	0x2	drv_degree Phase selection for drive clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
0	RW	0x0	init_state Enable initialization for clock source. 1'b0: Disable 1'b1: Enable When init_state=1, the host clocks including drive clock and sample clock are inactive.

SDMMC_CLKGEN_CON1

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	sample_sel Selection for sample clock. 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
10	RO	0x0	reserved
9:3	RW	0x00	sample_delaynum Delay element number configuration for sample clock. It can be modified when init_state=1 and should be stable when init_state=0.
2:1	RW	0x2	sample_degree Phase selection for sample clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
0	RO	0x0	reserved

SDMMC_MISC_CON

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
5	RW	0x0	mem_clkgat_enable Memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
4:0	RO	0x0	reserved

SDMMC_FIFO_BASE

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_base_addr FIFO base address

39.5 Interface Description

39.5.1 SDMMC Interface Description

Table 39-8 SDMMC Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc_cclk	O	SDMMC0_CLK/FSPI1_CLK_M0/SAI3_SCLK_M3/TEST_CLK_OUT/UART5_TX_M2/I2C5_SCL_M0/SPI0_CLK_M1/I3C1_SDA_PU_M1/GPIO2_A5_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[7:4]=4'h1
sdmmc_ccmd	I/O	SDMMC0_CMD/FSPI1_CSN0_M0/SAI3_SDO_M3/UART5_RX_M2/I2C5_SDA_M0/SPI0_CSN0_M1/PWM2_CH4_M0/GPIO2_A4_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[3:0]=4'h1
sdmmc_cdata0	I/O	SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/CAN0_RX_M0/PWM2_CH2_M0/GPIO2_A0_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'h1
sdmmc_cdata1	I/O	SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/CAN0_TX_M0/PWM2_CH3_M0/GPIO2_A1_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'h1
sdmmc_cdata2	I/O	SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/CAN1_RX_M0/I3C1_SCL_M1/GPIO2_A2_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[11:8]=4'h1
sdmmc_cdata3	I/O	SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/CAN1_TX_M0/I3C1_SDA_M1/GPIO2_A3_d	TOP_IOC_GPIO2A_IOMUX_SEL_L[15:12]=4'h1
sdmmc_cdetn	I	SDMMC0_DETN/SPI2_CSN1_M0/GPIO0_A7_u	PMU0_IOC_GPIO0A_IOMUX_SEL_H[15:12]=4'h1
sdmmc_pwren	O	SDMMC0_PWREN/SDMMC1_DETN_M2/HDMI_TX_HPDIN_M1/EDP_TX_HPDIN_M1/PWM1_CH2_M0/GPIO0_B6_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[11:8]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

39.5.2 SDIO Interface Description

Table 39-9 SDIO-m0 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdio_cclk	O	ETH1_TXCLK_M1/SDMMC1_CLK_M0/SAI3_MCLK_M1/PDM0_CLK0_M2/UART3_RX_M2/GPIO1_C1_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[7:4]=4'h2
sdio_ccmd	I/O	ETH1_TXD3_M1/SDMMC1_CMD_M0/PDM0_SDI2_M2/UART3_TX_M2/SPI1_CSN1_M0/PWM0_CH0_M1/GPIO1_C0_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[3:0]=4'h2
sdio_cdata0	I/O	ETH1_RXD2_M1/SDMMC1_D0_M0/SAI3_SCLK_M1/I2C9_SDA_M1/SPI1_CLK_M0/PCIE1_CLKREQN_M1/PWM1_CH0_M1/GPIO1_B4_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4'h2
sdio_cdata1	I/O	ETH1_RXD3_M1/SDMMC1_D1_M0/SAI3_LRCK_M1/I2C9_SCL_M1/SPI1_MOSI_M0/PWM1_CH1_M1/GPIO1_B5_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[7:4]=4'h2
sdio_cdata2	I/O	ETH1_RXCLK_M1/SDMMC1_D2_M0/SAI3_SDO_M1/UART3_CTSN_M2/SPI1_MISO_M0/PCIE0_CLKREQN_M1/GPIO1_B6_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4'h2
sdio_cdata3	I/O	ETH1_TXD2_M1/SDMMC1_D3_M0/SAI3_SDI_M1/UART3_RTSN_M2/SPI1_CSN0_M0/GPIO1_B7_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4'h2
sdio_cdetn	I	ETH1_PPSTRIG_M1/SDMMC1_DETN_M0/FSPI1_CSN0_M1/UART4_CTSN_M1/I2C6_SDA_M1/SPI2_CSN0_M1/GPIO1_C3_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[15:12]=4'h2

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Module Pin	Dir.	PAD Name	IOMUX Setting
sdio_pwren	O	ETH1_PPSCLK_M1/SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_CSN1_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[11:8]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 39-10 SDIO-m1 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdio_cclk	O	VI_CIF_D10/SDMMC1_CLK_M1/ETH0_TXCLK_M1/SAI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/PCIE1_CLKREQN_M0/GPIO2_B3_	TOP_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4'h2
sdio_ccmd	I/O	VI_CIF_D11/SDMMC1_CMD_M1/ETH0_TXD3_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCIE0_CLKREQN_M0/GPIO2_B2_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[11:8]=4'h2
sdio_cdata0	I/O	VI_CIF_D15/SDMMC1_D0_M1/ETH0_RXD0_M1/SAI0_SDO0_M0/UART8_TX_M1/SPI4_CSN1_M3/I2C4_SCL_M2/GPIO2_A6_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[11:8]=4'h2
sdio_cdata1	I/O	VI_CIF_D14/SDMMC1_D1_M1/ETH0_TXCTL_M1/SAI0_SDO1_M0/UART8_RX_M1/I2C4_SDA_M2/GPIO2_A7_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[15:12]=4'h2
sdio_cdata2	I/O	VI_CIF_D13/SDMMC1_D2_M1/ETH0_TXD1_M1/SAI0_SDI0_M0/PDM0_SDI3_M3/UART1_TX_M1/GPIO2_B0_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[3:0] =4'h2
sdio_cdata3	I/O	VI_CIF_D12/SDMMC1_D3_M1/ETH0_TXD0_M1/SAI0_SDI1_M0/PDM0_SDI2_M3/UART1_RX_M1/GPIO2_B1_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[7:4] =4'h2
sdio_cdetn	I	VI_CIF_D8/SDMMC1_DETN_M1/ETH0_RXCLK_M1/SAI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/SATA1_ACTLED_M0/GPIO2_B5_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[7:4] =4'h2
sdio_pwren	O	VI_CIF_D9/SDMMC1_PWREN_M1/ETH0_TXD2_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/SATA0_ACTLED_M0/GPIO2_B4_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[3:0] =4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 39-11 SDIO-m2 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdio_cdetn	I	SDMMC0_PWREN/SDMMC1_DETN_M2/HDMI_TX_HPDIN_M1/EDP_TX_HPDIN_M1/PWM1_CH2_M0/GPIO0_B6_d	PMU1_IOC_GPIO0B_IOMUX_SEL_H[11:8]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

39.6 Application Notes

39.6.1 Software/Hardware Restriction

Before issuing a new data transfer command, the software should ensure that the card is not busy due to any previous data transfer command. Before changing the card clock frequency, the software must ensure that there are no data or command transfers in progress.

To avoid glitches in the card clock outputs, the software should use the following steps when changing the card clock frequency:

1) Before disable the clocks, ensure that the card is not busy due to any previous data command. To determine this, check for 0 in bit9 of SDMMC_STATUS register.
2) Update the Clock Enable register to disable clock. To ensure completion of any previous command before this update, send a command to the CIU to update the clock registers by setting:

- start_cmd bit
- "update clock registers only" bits
- "wait_previous data complete" bit

   Wait for the CIU to take the command by polling for 0 on the start_cmd bit.

3) Set the start_cmd bit to update the Clock Divider and/or Clock Source register, and send a command to the CIU in order to update the clock registers; wait for the CIU to take the command.
4) Set start_cmd to update the Clock Enable register in order to enable the required clocks and send a command to the CIU to update the clock registers; wait for the CIU to take the command.

In non-DMA mode, while reading from a card, the Data Transfer Over (SDMMC_RINTSTS[3]) interrupt occurs as soon as the data transfer from the card is over. There still could be some data left in the FIFO, and the RX_WMark interrupt may or may not occur, depending on the remaining bytes in the FIFO. Software should read any

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remaining bytes upon seeing the Data Transfer Over (DTO) interrupt. While using the external DMA interface for reading from a card, the DTO interrupt occurs only after all the data is flushed to memory by the DMA interface unit.
While writing to a card in external DMA mode, if an undefined-length transfer is selected by setting the Byte Count Register to 0, the DMA logic will likely request more data than it will send to the card, since it has no way of knowing at which point the software will stop the transfer. The DMA request stops as soon as the DTO is set by the CIU.
If the software issues a controller_reset command by setting control register bit[0] to 1, all the CIU state machines are reset; the FIFO is not cleared. The DMA sends all remaining bytes to the host. In addition to a card-reset, if a FIFO reset is also issued, then:

- Any pending DMA transfer on the bus completes correctly
- DMA data read is ignored
- Write data is unknown(x)

Additionally, if dma_reset is also issued, any pending DMA transfer is abruptly terminated. When the DMA is used, the DMA controller channel should also be reset and reprogrammed.
If any of the previous data commands do not properly terminate, then the software should issue the FIFO reset in order to remove any residual data, if any, in the FIFO. After asserting the FIFO reset, you should wait until this bit is cleared.
One data-transfer requirement between the FIFO and host is that the number of transfers should be a multiple of the FIFO data width (32bits). For example, you want to write only 15 bytes to an SD/MMC card (SDMMC_BYTCNT), the host should write 16 bytes to the FIFO or program the DMA to do 16-byte transfers. The software can still program the Byte Count register to only 15, at which point only 15 bytes will be transferred to the card. Similarly, when 15 bytes are read from a card, the host should still read all 16 bytes from the FIFO. It is recommended that you not change the FIFO threshold register in the middle of data transfers.

39.6.2 Programming Sequence

39.6.2.1 Initialization

Following figure illustrates the initialization flow.

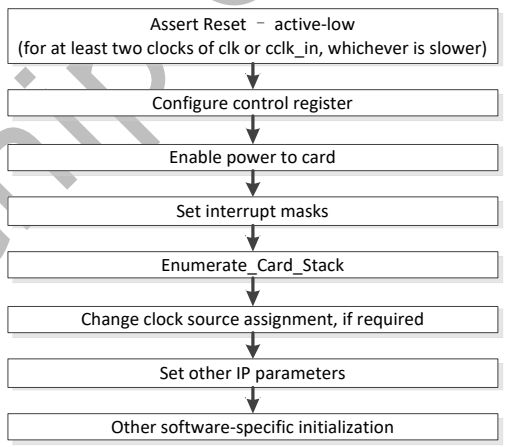

Fig. 39-10 Host Controller Initialization Sequence

Once the power and clocks are stable, reset_n should be asserted(active-low) for at least two cycles of clk or cclk_in, whichever is slower. The reset initializes the registers, ports, FIFO-pointers, DMA interface controls, and state-machines in the design. After power-on reset, the software should do the following:

1) Configure control register – For MMC mode, enable the open-drain pullup by setting enable_OD_pullup(bit24) in the SDMMC_CTRL register.
2) Enable power to cards – Before enabling the power, confirm that the voltage setting to the voltage regulators is correct. Enable power to the connected cards by setting the corresponding bit to 1 in the Power Enable register. Wait for the power ramp-up time.
3) Set masks for interrupts by clearing appropriate bits in the Interrupt Mask register. Set the global int_enable bit of the SDMMC_CTRL register. It is recommended that you write 0xffff_ffff to the Raw Interrupt register in order to clear any pending interrupts

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before setting the int_enable bit.

4) Enumerate card stack – Each card is enumerated according to card type; for details, refer to "Enumerated Card Stack". For enumeration, you should restrict the clock frequency to 400KHz.
5) Changing clock source assignment – set the card frequency using the clock-divider and clock-source registers; for details, refer to "Clock Programming". MMC cards operate at a maximum of 20MHz (at maximum of 52MHz in high-speed mode). SD mode operates at a maximum of 25MHz (at maximum of 50MHz in high-speed mode).
6) Set other parameters, which normally do not need to be changed with every command, with a typical value such as timeout values in cclk_out according to SD/MMC specifications.

- ResponseTimeOut = 0x64
- DataTimeOut = highest of one of the following:
  - (10*((TAAC*Fop)+(100*NSAC))
  - Host FIFO read/write latency from FIFO empty/full
- Set the debounce value to 25ms(default:0x0fffff) in host clock cycle units in the SDMMC_DEBNCE register.
- FIFO threshold value in bytes in the SDMMC_FIFOTH register. Typically, the threshold value can be set to half the FIFO depth; that is:
  - RX_WMark = (FIFO_DEPTH/2) - 1;
  - TX_WMark = FIFO_DEPTH/2.

39.6.2.2 Enumerated Card Stack

The card stack does the following:

- Enumerates all connected cards
- Sets the RCA for the connected cards
- Reads card-specific information
- Stores card-specific information locally

Enumeration depends on the operating mode of the SD/MMC card; the card type is first identified and the appropriate card enumeration routine is called.

1) Check if the card is connected.
2) Clear the card type register to set the card width as a single bit. For the given card number, clear the corresponding bits in the card_type register. Clear the register bit for a 1-bit, 4-bit bus width. For example, for card number=1, clear bit 0 and bit 16 of the card_type register.
3) Set clock frequency to FOD=400KHz, maximum – Program clock divider0 (bits 0-7 in the SDMMC_CLKDIV register) value to one-half of the cclk_in frequency divided by 400KHz. For example, if cclk_in is 20MHz, then the value is 20, 000/(2*400)=25.
4) Identify the card type; that is, SD, MMC, or SDIO.
   a. Send CMD5 first. If a response is received, then the card is SDIO
   b. If not, send CMD8 with the following Argument
      Bit[31:12] = 20'h0 //reserved bits
      Bit[11:8] = 4'b0001 //VHS value
      Bit[7:0] = 8'b10101010 //Preferred Check Pattern by SD2.0
   c. If Response is received the card supports High Capacity SD2.0 then send ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b1; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
   d. If Response is received for ACMD41 then the card is SD. Otherwise the card is MMC.
   e. If response is not received for initial CMD8 then card does not support High Capacity SD2.0, then issue CMD0 followed by ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b0; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range

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5) Enumerate the card according to the card type.
6) Use a clock source with a frequency = Fod (that is, 400KHz) and use the following enumeration command sequence:

- SD card – Send CMD0, CMD8, ACMD41, CMD2, CMD3.
- MMC – Send CMD0, CMD1, CMD2, CMD3.

39.6.2.3 Clock Programming

The Host Controller supports one clock source. The clock to an individual card can be enabled or disabled. Registers that support this are:

- SDMMC_CLKDIV – Programs individual clock source frequency. SDMMC_CLKDIV limited to 0 or 1 is recommended.
- SDMMC_CLKSRC – Assign clock source for each card.
- SDMMC_CLKENA – Enables or disables clock for individual card and enables low-power mode, which automatically stops the clock to a card when the card is idle for more than 8 clocks.

The Host Controller loads each of these registers only when the start_cmd bit and the update_clk_regs_only bit in the SDMMC_CMD register are set. When a command is successfully loaded, the Host Controller clears this bit, unless the Host Controller already has another command in the queue, at which point it gives an HLE(Hardware Locked Error). Software should look for the start_cmd and the update_clk_regs_only bits, and should also set the wait_prvdata_complete bit to ensure that clock parameters do not change during data transfer. Note that even though start_cmd is set for updating clock registers, the Host Controller does not raise a command_done signal upon command completion.
The following shows how to program these registers:

1) Confirm that no card is engaged in any transaction; if there is a transaction, wait until it finishes.
2) Stop all clocks by writing 0 to the SDMMC_CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.
3) Program the SDMMC_CLKDIV and SDMMC_CLKSRC registers, as required. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

Re-enable all clocks by programming the SDMMC_CLKENA register. Set the start_cmd, update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

39.6.2.4 No-Data Command With or Without Response Sequence

To send any non-data command, the software needs to program the SDMMC_CMD register @0x2C and the SDMMC_CMDARG register @0x28 with appropriate parameters. Using these two registers, the Host Controller forms the command and sends it to the command bus. The Host Controller reflects the errors in the command response through the error bits of the SDMMC_RINTSTS register.
When a response is received – either erroneous or valid – the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. A short response is copied in Response Register0, while along response is copied to all four response registers @0x30, 0x34, 0x38, and 0x3C. The Response3 register bit 31 represents the MSB, and the Response0 register bit 0 represents the LSB of a long response.
For basic commands or non-data commands, follow these steps:

1) Program the Command register @0x28 with the appropriate command argument parameter.
2) Program the Command register @0x2C with the settings in following table.

Table 39-12 Command Settings for No-Data Command

Parameter	Value	Description
Default		

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Parameter	Value	Description
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
data_expected	0	No data command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
cmd_index	command-index	-
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
wait_prvdata_complete	1	Before sending command on command line, host should wait for completion of any data command in process, if any (recommended to always set this bit, unless the current command is to query status or stop data transfer when transfer is in progress)
check_response_crc	1	If host should crosscheck CRC of response received

3) Wait for command acceptance by host. The following happens when the command is loaded into the Host Controller:

- Host Controller accepts the command for execution and clears the start_cmd bit in the SDMMC_CMD register, unless one command is in process, at which point the Host Controller can load and keep the second command in the buffer.
- If the Host Controller is unable to load the command – that is, a command is already in progress, a second command is in the buffer, and a third command is attempted – then it generates an HLE (hardware-locked error).

4) Check if there is an HLE.
5) Wait for command execution to complete. After receiving either a response from a card or response timeout, the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. Software can either poll for this bit or respond to a generated interrupt.
6) Check if response_timeout error, response_CRC error, or response error is set. This can be done either by responding to an interrupt raised by these errors or by polling bits 1, 6, and 8 from the SDMMC_RINTSTS register @0x44. If no response error is received, then the response is valid. If required, the software can copy the response from the response registers @0x30-0x3C.

Software should not modify clock parameters while a command is being executed.

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39.6.2.5 Data Transfer Commands

Data transfer commands transfer data between the memory card and the Host Controller. To send a data command, the Host Controller needs a command argument, total data size, and block size. Software can receive or send data through the FIFO.

Before a data transfer command, software should confirm that the card is not busy and is in a transfer state, which can be done using the CMD13 and CMD7 commands, respectively. For the data transfer commands, it is important that the same bus width that is programmed in the card should be set in the card type register @0x18.

The Host Controller generates an interrupt for different conditions during data transfer, which are reflected in the SDMMC_RINTSTS register @0x44 as:

1) Data_Transfer_Over (bit 3) – When data transfer is over or terminated. If there is a response timeout error, then the Host Controller does not attempt any data transfer and the "Data Transfer Over" bit is never set.
2) Transmit_FIFO_Data_request (bit 4) – FIFO threshold for transmitting data was reached; software is expected to write data, if available, in FIFO.
3) Receive_FIFO_Data_request (bit 5) – FIFO threshold for receiving data was reached; software is expected to read data from FIFO.
4) Data starvation by Host timeout (bit 10) – FIFO is empty during transmission or is full during reception. Unless software writes data for empty condition or reads data for full condition, the Host Controller cannot continue with data transfer. The clock to the card has been stopped.
5) Data read timeout error (bit 9) – Card has not sent data within the timeout period.
6) Data CRC error (bit 7) – CRC error occurred during data reception.
7) Start bit error (bit 13) – Start bit was not received during data reception.
8) End bit error (bit 15) – End bit was not received during data reception or for a write operation; a CRC error is indicated by the card.

Conditions 6), 7), and 8) indicate that the received data may have errors. If there was a response timeout, then no data transfer occurred.

39.6.2.6 Single-Block or Multiple-Block Read

Steps involved in a single-block or multiple-block read are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C. The Host Controller expects data from the card in blocks of size SDMMC_BLKSIZ each.
3) Program the SDMMC_CMDARG register @0x28 with the data address of the beginning of a data read.
4) Program the Command register with the parameters listed in following table. For SD and MMC cards, use CMD17 for a single-block read and CMD18 for a multiple-block read. For SDIO cards, use CMD53 for both single-block and multiple-block transfers.

Table 39-13 Command Setting for Single or Multiple-Block Read

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No.0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as

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Parameter	Value	Description
		CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	0	Read from card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, the Host Controller starts executing the command; when the command is sent to the bus, the command_done interrupt is generated.

- Software should look for data error interrupts; that is, bits 7, 9, 13, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending a STOP command.
- Software should look for Receive_FIFO_Data_request and/or data starvation by host timeout conditions. In both cases, the software should read data from the FIFO and make space in the FIFO for receiving more data.

When a Data_Transfer_Over interrupt is received, the software should read the remaining data from the FIFO.

39.6.2.7 Single-Block or Multiple-Block Write

Steps involved in a single-block or multiple-block write are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C; the Host Controller sends data in blocks of size SDMMC_BLKSIZ each.
3) Program SDMMC_CMDARG register @0x28 with the data address to which data should be written.
4) Write data in the FIFO; it is usually best to start filling data the full depth of the FIFO.
5) Program the Command register with the parameters listed in following table.

Table 39-14 Command Settings for Single or Multiple-Block Write

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
send_initialization	0	Can be 1, but only for card

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Parameter	Value	Description
		reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	1	Write to card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, Host Controller starts executing a command; when the command is sent to the bus, a command_done interrupt is generated.

- Software should look for data error interrupts; that is, for bits 7, 9, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending the STOP command.
- Software should look for Transmit_FIFO_Data_Request and/or timeout conditions from data starvation by the host. In both cases, the software should write data into the FIFO.

When a Data_Transfer_Over interrupt is received, the data command is over. For an open-ended block transfer, if the byte count is 0, the software must send the STOP command. If the byte count is not 0, then upon completion of a transfer of a given number of bytes, the Host Controller should send the STOP command, if necessary. Completion of the AUTO-STOP command is reflected by the Auto_command_done interrupt – bit 14 of the SDMMC_RINTSTS register. A response to AUTO_STOP is stored in SDMMC_RESP1 @0x34.

39.6.2.8 Sending Stop or Abort in Middle of Transfer

The STOP command can terminate a data transfer between a memory card and the Controller, while the ABORT command can terminate an I/O data transfer for only the SDIO_IOONLY and SDIO_COMBO cards.

- Send STOP command – Can be sent on the command line while a data transfer is in progress; this command can be sent at any time during a data transfer.

You can also use an additional setting for this command in order to set the Command register bits (5-0) to CMD12 and set bit 14 (stop_abort_cmd) to 1. If stop_abort_cmd is not set to 1, the Controller does not know that the user stopped a data transfer. Reset bit 13 of the Command register (wait_prvdata_complete) to 0 in order to make the Controller send the command at once, even though there is a data transfer in progress.
Send ABORT command – Can be used with only an SDIO_IOONLY or SDIO_COMBO card. To abort the function that is transferring data, program the function number in ASx bits (CCCR register of card, address 0x06, bits (0-2) using CMD52.

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39.6.2.9 Read_Wait Sequence

Read_wait is used with only the SDIO card and can temporarily stall the data transfer—either from function or memory—and allow the host to send commands to any function within the SDIO device. The host can stall this transfer for as long as required. The Host Controller provides the facility to signal this stall transfer to the card. The steps for doing this are:

1) Check if the card supports the read_wait facility; read SRW (bit 2) of the CCCR register @0x08. If this bit is 1, then all functions in the card support the read_wait facility. Use CMD52 to read this bit.
2) If the card supports the read_wait signal, then assert it by setting the read_wait (bit 6) in the SDMMC_CTRL register @0x00.

Clear the read_wait bit in the SDMMC_CTRL register.

39.6.2.10 Controller/DMA/FIFO Reset Usage

- Controller reset – Resets the controller by setting the controller_reset bit (bit 0) in the SDMMC_CTRL register; this resets the CIU and state machines, and also resets the BIU-to-CIU interface. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.
- FIFO reset - Resets the FIFO by setting the fifo_reset bit (bit 1) in the SDMMC_CTRL register; this resets the FIFO pointers and counters of the FIFO. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

In external DMA transfer mode, even when the FIFO pointers are reset, if there is a DMA transfer in progress, it could push or pop data to or from the FIFO; the DMA itself completes correctly. In order to clear the FIFO, the software should issue an additional FIFO reset and clear any FIFO under-run or overrun errors in the SDMMC_RAWINTS register caused by the DMA transfers after the FIFO was reset.

39.6.2.11 Card Read Threshold

When an application needs to perform a Single or Multiple Block Read command, the application must program the SDMMC_CARDTHRCTL register with the appropriate Card Read Threshold size (CardRdThreshold) and set the Card Read Threshold Enable (CardRdThrEnable) bit to 1'b1. This additional programming ensures that the Host controller sends a Read Command only if there is space equal to the Card Read Threshold available in the Rx FIFO. This in turn ensures that the card clock is not stopped in the middle a block of data being transmitted from the card. The Card Read Threshold can be set to the block size of the transfer, which guarantees that there is a minimum of one block size of space in the RxFIFO before the controller enables the card clock. The Card Read Threshold is required when the Round Trip Delay is greater than 0.5cclk_in period.

39.6.2.12 Error Handling

The Host Controller implements error checking; errors are reflected in the SDMMC_RAWINTS register@0x44 and can be communicated to the software through an interrupt, or the software can poll for these bits. Upon power-on, interrupts are disabled (int_enable in the SDMMC_CTRL register is 0), and all the interrupts are masked (bits 0-31 of the SDMMC_INTMASK register; default is 0).

Error handling:

- Response and data timeout errors – For response timeout, software can retry the command. For data timeout, the Host Controller has not received the data start bit – either for the first block or the intermediate block – within the timeout period, so software can either retry the whole data transfer again or retry from a specified block onwards. By reading the contents of the SDMMC_TCBCNT later, the software can decide how many bytes remain to be copied.
- Response errors – Set when an error is received during response reception. In this case, the response that copied in the response registers is invalid. Software can retry the command.
- Data errors – Set when error in data reception are observed; for example, data CRC, start bit not found, end bit not found, and so on. These errors could be set for any

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block-first block, intermediate block, or last block. On receipt of an error, the software can issue a STOP or ABORT command and retry the command for either whole data or partial data.

- Hardware locked error – Set when the Host Controller cannot load a command issued by software. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
- FIFO under-run/overrun error – If the FIFO is full and software tries to write data in the FIFO, then an overrun error is set. Conversely, if the FIFO is empty and the software tries to read data from the FIFO, an under-run error is set. Before reading or writing data in the FIFO, the software should read the fifo_empty or fifo_full bits in the Status register.
- Data starvation by host timeout – Raised when the Host Controller is waiting for software intervention to transfer the data to or from the FIFO, but the software does not transfer within the stipulated timeout period. Under this condition and when a read transfer is in process, the software should read data from the FIFO and create space for further data reception. When a transmit operation is in process, the software should fill data in the FIFO in order to start transferring data to the card.
- CRC Error on Command – If a CRC error is detected for a command, the CE-ATA device does not send a response, and a response timeout is expected from the Host Controller. The ATA layer is notified that an MMC transport layer error occurred.

Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register. It then continues further data transmission until all the bytes are transmitted.

39.6.2.13 Voltage Switching

The Host Controller supports SD 3.0 Ultra High Speed (UHS-1) and is capable of voltage switching in SD-mode, which can be applied to SD High-Capacity (SDHC) and SD Extended Capacity (SDXC) cards. UHS-1 supports only 4-bit mode.
However, whether the IO voltage of 1.8v supported or not is depended on the SoC design.
SD 3.0 UHS-1 supports the following transfer speed modes for UHS-50 and/or UHS-104 cards:

- DS – default-speed up to 25MHz, 3.3V signaling
- HS – high-speed up to 50MHz, 3.3V signaling
- SDR12 – SDR up to SDR 25MHz, 1.8V signaling
- SDR25 – SDR up to 50MHz, 1.8V signaling
- SDR50 – SDR up to 100MHz, 1.8V signaling
- DDR50 – DDR up to 50MHz, 1.8V signaling

Voltage selection can be done in only SD mode. The first CMD0 selects the bus mode-either SD mode or SPI mode. The card must be in SD mode in order for 1.8V signaling mode to apply, during which time the card cannot be switched to SPI mode or 3.3V signaling without a power cycle.
If the System BIOS in an embedded system already knows that it is connected to an SD 3.0 card, then the driver programs the Controller to initiate ACMD41. The software knows from the response of ACMD41 whether or not the card supports voltage switching to 1.8V.

- If bit 32 of ACMD41 response is 1'b1: card supports voltage switching and next command-CMD11-invokes voltage switching sequence. After CMD11 is started, the software must program the IO voltage selection register based on the soc architecture.
- If bit 32 of ACMD41 response is 1'b0: card does not support voltage switching and CMD11 should not be started.

If the card and host controller accept voltage switching, then they support UHS-1 modes of data transfer. After the voltage switch to 1.8V, SDR12 is the default speed.
Since the UHS-1 can be used in only 4-bit mode, the software must start ACMD6 and change the card data width to 4-bit mode; ACMD6 is driven in any of the UHS-1 speeds. If the host wants to select the DDR mode of data transfer, then the software must program the SDMMC_DDR_REG register in the CSR space with the appropriate card number.
To choose from any of the SDR or DDR modes, appropriate values should be programmed in the SDMMC_CLKDIV register.

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39.6.2.14 Voltage Switch Operation

The Voltage Switch operation must be performed in SD mode only.

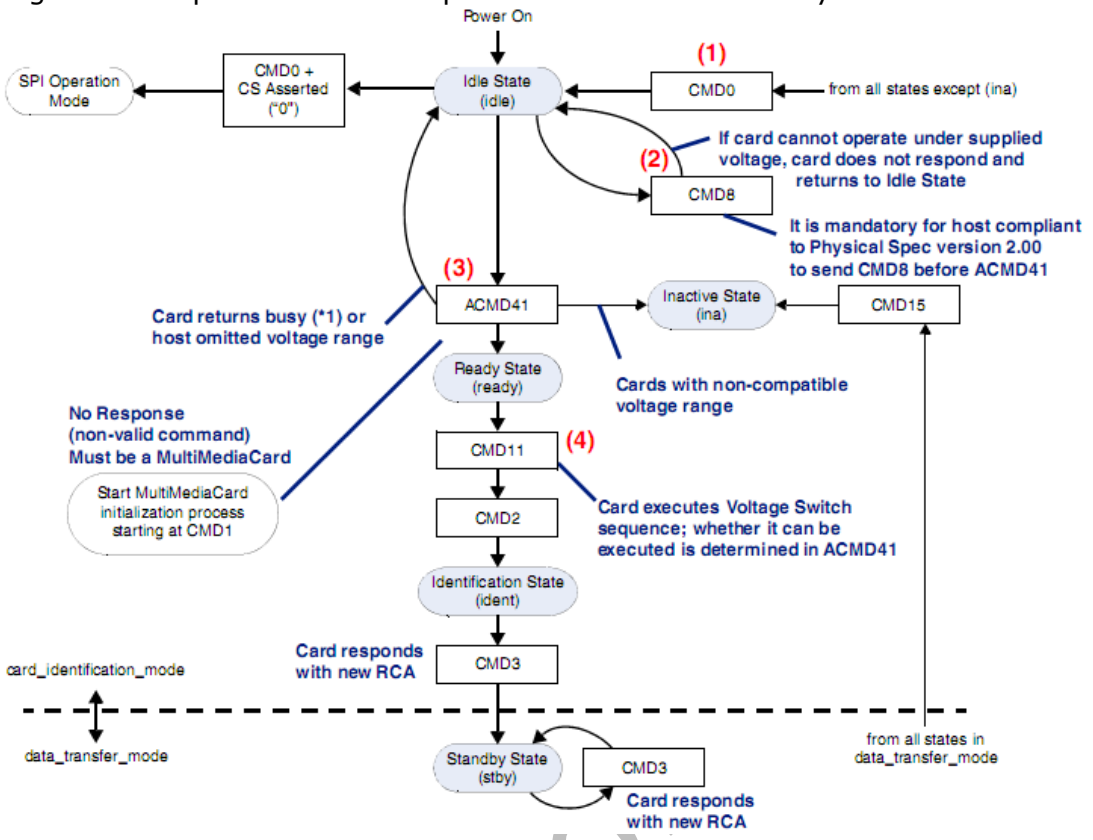

Fig. 39-11 Voltage Switching Command Flow Diagram

The following outlines the steps for the voltage switch programming sequence

1) Software Driver starts CMD0, which selects the bus mode as SD.
2) After the bus is in SD card mode, CMD8 is started in order to verify if the card is compatible with the SD Memory Card Specification, Version 2. 00. CMD8 determines if the card is capable of working within the host supply voltage specified in the VHS (19:16) field of the CMD; the card supports the current host voltage if a response to CMD8 is received.
3) ACMD 41 is started. The response to this command informs the software if the card supports voltage switching; bits 38, 36, and 32 are checked by the card argument of ACMD41; refer to following figure.

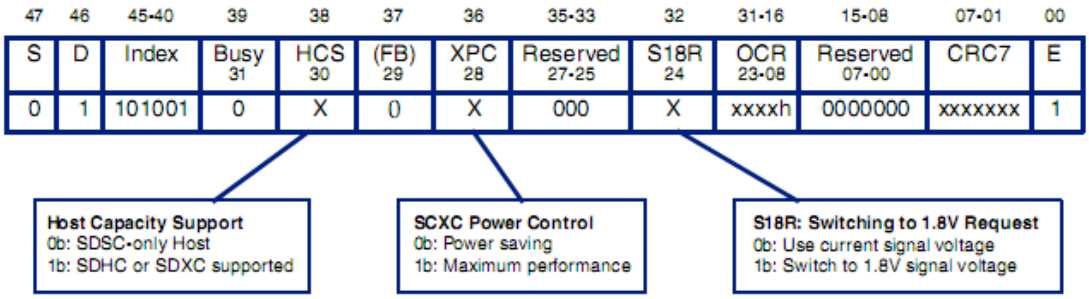

Fig. 39-12 ACMD41 Argument

- Bit 30 informs the card if host supports SDHC/SDXC or not; this bit should be set to 1'b1.
- Bit 28 can be either 1 or 0.
- Bit 24 should be set to 1'b1, indicating that the host is capable of voltage switching; refer to following figure.

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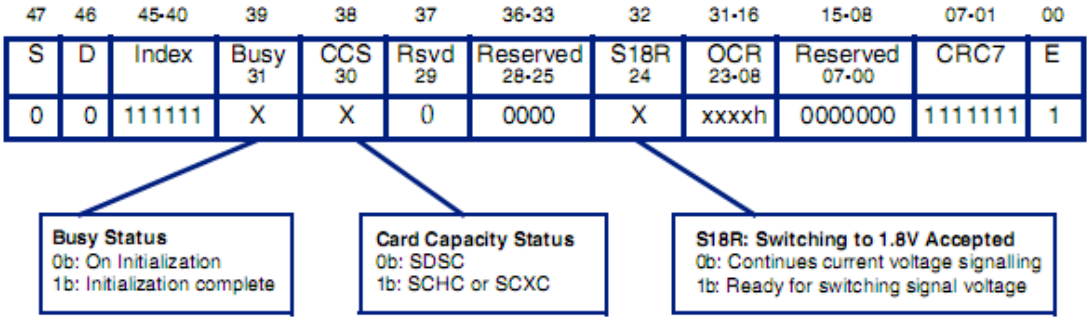

Fig. 39-13 ACMD41 Response(R3)

- Bit 30 – If set to 1'b1, card supports SDHC/SDXC; if set to 1'b0, card supports only SDSC
- Bit 24 – If set to 1'b1, card supports voltage switching and is ready for the switch
- Bit 31 – If set to 1'b1, initialization is over; if set to 1'b0, means initialization in process

If the card supports voltage switching, then the software must perform the steps discussed for either the "Voltage Switch Normal Scenario" or the "Voltage Switch Error Scenario".

39.6.2.15 Voltage Switch Normal Scenario

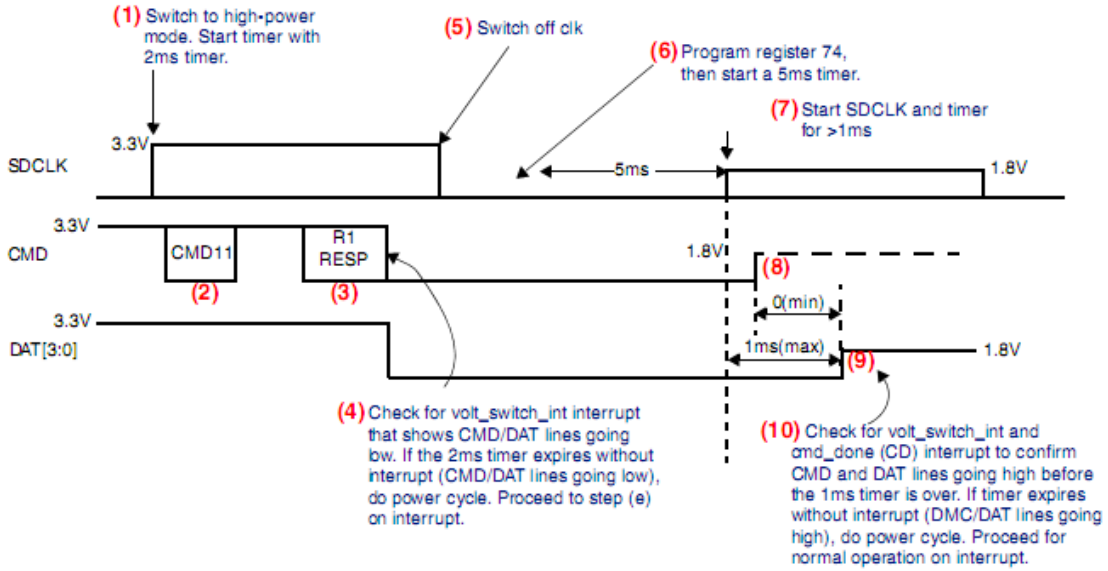

Fig. 3938-14 Voltage Switch Normal Scenario

1) The host programs SDMMC_CLKENA—cclk_low_power register—with zero (0) for the corresponding card, which makes the host controller move to high-power mode. The application should start a timer with a recommended value of 2ms; this value of 2 ms is determined as below: Total cycles required for CMD11 = 48 cycles
   Total cycles required for RESP R1 = 48 cycles
   Maximum clock delay between MCD11 end to start of RESP1 = 60 cycles
   Total = 48+48 + 60 = 160
   Minimum frequency during enumeration is 100 KHz; that is, 10us
   Total time = 160 * 10us = 1600us = 1. 6ms ~ 2ms
2) The host issues CMD11 to start the voltage switch sequence. Set bit 28 to 1'b1 in CMD when setting CMD11; for more information on setting bits, refer to "Boot Operation".
3) The card returns R1 response; the host controller does not generate cmd_done interrupt on receiving R1 response.
4) The card drives CMD and DAT [3:0] to low immediately after the response. The host controller generates interrupt (VOLT_SWITCH_INT) once the CMD or DAT [3:0] line goes low. The application should wait for this interrupt. If the 2ms timer expires without an interrupt (CMD/DAT lines going low), do a power cycle.

Note: Before doing a power cycle, switch off the card clock by programming SDMMC_CLKENA register

Proceed to step (5) on getting an interrupt (VOLT_SWITCH_INT).

Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be masked during the voltage switch sequence.

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If the timer expires without interrupt (CMD/DAT lines going low), perform a power cycle. Proceed to step (5) on interrupt.

1) Program the SDMMC_CLKENA register, with 0 for the corresponding card; the host stops supplying SDCLK.
2) Program Voltage register to the required values for the corresponding card. The application should start a timer > 5ms.
3) After the 5ms timer expires, the host voltage regulator is stable. Program SDMMC_CLKENA register, with 1 for the corresponding card; the host starts providing SDCLK at 1. 8V; this can be at zero time after Voltage register has been programmed. When the SDMMC_CLKENA register is programmed, the application should start another timer > 1ms.
4) By detecting SDCLK, the card drives CMD to high at 1. 8V for at least one clock and then stops driving (tri-state); CMD is triggered by the rising edge of SDCLK (SDR timing).
5) If switching to 1. 8V signaling is completed successfully, the card drives DAT [3:0] to high at 1. 8V for at least one clock and then stops driving (tri-state); DAT [3:0] is triggered by the rising edge of SDCLK (SDR timing). DAT[3:0] must be high within 1ms from the start of SDCLK.
6) The host controller generates a voltage switch interrupt (VOLT_SWITCH_INT) and a command done (CD) interrupt once the CMD and DAT[3:0] lines go high. The application should wait for this interrupt to confirm CMD and DAT lines going high before the 1ms timer is done.

If the timer expires without the voltage switch interrupt (VOLT_SWITCH_INT), a power cycle should be performed. Program the SDMMC_CLKENA register to stop the clock for the corresponding card number. Wait for the cmd_done (CD) interrupt. Proceed for normal operation on interrupt. After the sequence is completed, the host and the card start communication in SDR12 timing.

39.6.2.16 Voltage Switch Error Scenario

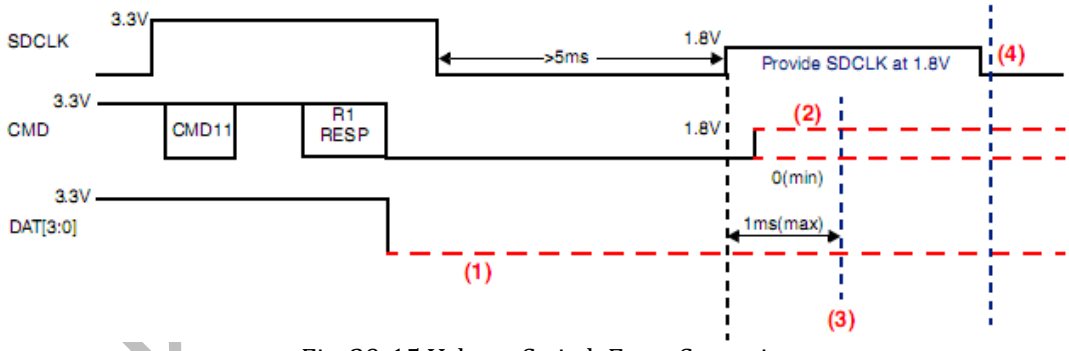

Fig. 39-15 Voltage Switch Error Scenario

1) If the interrupt (VOLT_SWITCH_INT) does not come, then the 2 ms timer should time out and a power cycle should be initiated.

Note: Before performing a power cycle, switch off the card clock by programming SDMMC_CLKENA register; no cmd_done (CD) interrupt is generated.

Additionally, if the card detects a voltage error at any point in between steps (5) and (7) in the card keeps driving DAT[3:0] to low until card power off.

2) CMD can be low or tri-state.
3) The host controller generates a voltage switch interrupt once the CMD and DAT[3:0] lines go high. The application should check for an interrupt to confirm CMD and DAT lines going high before the 1 ms timer is done.

If the 1 ms timer expires without interrupt (VOLT_SWITCH_INT) and cmd_done (CD), a power cycle should be performed. Program the SDMMC_CLKENA register to stop SDCLK of the corresponding card. Wait for the cmd_done interrupt. Proceed for normal operation on interrupt.

4) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2. 5V. Errors are indicated by (1) and (2).

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- If voltage switching is accepted by the card, the default speed is SDR12.
- Command Done is given:
  - If voltage switching is properly done, CMD and DAT line goes high.
  - If switching is not complete, the 1ms timer expires, and the card clock is switched off.

Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

- The application should use CMD6 to check and select the particular function; the function appropriate-speed should be selected.

After the function switches, the application should program the correct value in the CLKDIV register, depending on the function chosen. Additionally, if Function 0x4 of the Access mode is chosen—that is, DDR50, then the application should also program 1'b1 in DDR_REG for the card number that has been selected for DDR50 mode.

39.6.3 DDR Operation

39.6.3.1 4-bit DDR Programming Sequence

DDR programming should be done only after the voltage switch operation has completed. The following outlines the steps for the DDR programming sequence:

1) Once the voltage switch operation is complete, the user must program voltage selection register to the required values for the corresponding card.

- To start a card to work in DDR mode, the application must program a bit of the newly defined SDMMC_UHSREG[16] register with a value of 1'b1.
- The bit that the user programs depends on which card is to be accessed in DDR mode.

To move back to SDR mode, a power cycle should be run on the card—putting the card in SDR12 mode—and only then should SDMMC_UHSREG[16]be set back to 1'b0 for the appropriate card.

39.6.3.2 8-bit DDR Programming Sequence

The following outlines the steps for the 8-bit DDR programming sequence:

1) The cclk_in signal should be twice the speed of the required cclk_out. Thus, if the cclk_out signal is required to be 50 MHz, the cclk_in signal should be 100 MHz.
2) The SDMMC_CLKDIV register should always be programmed with a value higher than zero (0); that is, a clock divider should always be used for 8-bit DDR mode.
3) The application must program the SDMMC_UHSREG[16] register (ddr_reg bits) by assigning it with a value of 1 for the bit corresponding to the card number; this causes the selected card to start working in DDR mode.

Depending on the card number, the SDMMC_CTYPE [16] bits should be set in order to make the host work in the 8-bit mode.

39.6.3.3 eMMC4.5 DDR START Bit

The eMMC4.5 changes the START bit definition in the following manner:

1) Receiver samples the START bit on the rising edge.
2) On the next rising edge after sampling the START bit, the receiver must sample the data.
3) Removes requirement of the START bit and END bit to be high for one full cycle.

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the EMMC_DDR_REG register.

39.6.3.4 Reset Command/Moving From DDR50 to SDR12

To reset the mode of operation from DDR50 to SDR12, the following sequence of operations has to be done by the application:

1) Issue CMD0.
2) When CMD0 is received, the card changes from DDR50 to SDR12.
3) Program the SDMMC_CLKDIV register with an appropriate value.
4) Set ddr_reg to 0.

Note: The Voltage register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

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39.6.4 H/W Reset Operation

When the RST_n signal goes low, the card enters a pre-idle state from any state other than the inactive state.

The following outlines the steps for the H/W reset programming sequence:

1) Program CMD12 to end any transfer in process.
2) Wait for DTO, even if no response is sent back by the card.
3) Set the following resets:

- DMA reset–SDMMC_CTRL [2] bit
- FIFO reset–SDMMC_CTRL [1] bit

Note: The above steps are required only if a transfer is in process.

4) Program the SDMMC_RSTN register with a value of 0; this can be done at any time when the card is connected to the controller. This programming asserts the RST_n signal and resets the card.
5) Wait for minimum of 1 µs or cclk_in period, whichever is greater
6) After a minimum of 1 µs, the application should program a value of 0 into the SDMMC_RSTN register. This de-asserts the RST_n signal and takes the card out of reset.
7) The application can program a new CMD only after a minimum of 200 µs after the de-assertion of the RST_n signal, as per the MMC 4.41 standard.

Note: For backward compatibility, the RST_n signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

39.6.5 FBE Scenarios

An FBE occurs due to an AHB error response on the AHB bus. This is a system error, so the software driver should not perform any further programming to the Host. The only recovery mechanism from such scenarios is to do one of the following:

- Issue a hard reset by asserting the reset_n signal
- Do a program controller reset by writing to the SDMMC_CTRL[0] bit

39.6.5.1 FIFO Overflow and Underflow

During normal data transfer conditions, FIFO overflow and underflow will not occur. However if there is a programming error, then FIFO overflow/underflow can result. For example, consider the following scenarios.

- For transmit: PBL=4, Tx watermark = 1. For the above programming values, if the FIFO has only one location empty, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pushes into the FIFO. This will result in a FIFO overflow interrupt.
- For receive: PBL=4, Rx watermark = 1. For the above programming values, if the FIFO has only one location filled, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pops to the FIFO. This will result in a FIFO underflow interrupt.

The driver should ensure that the number of bytes to be transferred as indicated in the descriptor should be a multiple of 4bytes with respect to H_DATA_WIDTH=32. For example, if the SDMMC_BYTCNT=13, the number of bytes indicated in the descriptor should be 16 for H_DATA_WIDTH=32.

39.6.5.2 Programming of PBL and Watermark Levels

The DMAC performs data transfers depending on the programmed PBL and threshold values.

Table 39-15 PBL and Watermark Levels

PBL (Number of transfers)	Tx/Rx Watermark Value
1	Greater than or equal to 1
4	Greater than or equal to 4
8	Greater than or equal to 8
16	Greater than or equal to 16
32	Greater than or equal to 32
64	Greater than or equal to 64

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PBL (Number of transfers)	Tx/Rx Watermark Value
128	Greater than or equal to 128
256	Greater than or equal to 256

39.6.6 Variable Delay Usage

The control signals for variable delay element usage are described in SDMMC_CLKGEN_CON0 and SDMMC_CLKGEN_CON1.
The following outlines the steps for clock generation sequence:
1) Assert init_state to soft reset the CLKGEN.
2) Configure drv_degree/sample_degree.
3) If fine adjustment required, delay line can be used by configuring drv_delaynum/sample_delaynum and drv_sel/sample_sel.
4) Dis-assert init_state to start CLKGEN.

39.6.7 Variable Delay Tuning

Tuning is defined by SD and MMC cards to determine the correct sampling point required for the host, especially for the speed modes SDR104 and HS200 where the output delays from the cards can be up to 2 UI. Tuning is required for other speed modes-such as DDR50-even though the output delay from the card is less than one cycle.
Command for tuning is different for different cards.
- SD Memory Card:
  - CMD19 – SD card for SDR50 and SDR104 speed modes. Tuning data is defined by card specifications.
  - CMD6 – SD card for speed modes not supporting CMD19. Tuning data is the 64byte SD status.
- Multimedia Card:
  - CMD21 – MMC card for HS200 speed mode. Tuning data is defined by card specifications.
  - CMD8 – MMC card for speed modes not supporting CMD21. Tuning data is 512 byte ExtCSD data.

The following is the procedure for variable delay tuning:
1) Set a phase shift of 0-degree on cclk_in_sample.
2) Send the Tuning command to the card; the card in turn sends an R1 response on the CMD line and tuning data on the DAT line.
3) If the host sees any of the errors—start bit error, data crc error, end bit error, data read time-out, response CRC error, response error—then the sampling point is incorrect.
4) Send CMD12 to bring the host controller state machines to idle.
   - The card may treat CMD12 as an invalid command because the card has successfully sent the tuning data, and it cannot send a response.
   - The host controller may generate a response time-out interrupt that must be cleared by software.
5) Repeat steps 2) to 4) by increasing the phase shift value or delay element number on cclk_in_sample until the correct sampling point is received such that the host does not see any of the errors.
6) Mark this phase shift value as the starting point of the sampling window.
7) Repeat steps 2 to 4 by increasing the phase shift value or delay element number on cclk_in_sample until the host sees the errors starting to come again or the phase shift value reaches 360-degree.
8) Mark the last successful phase shift value as the ending point of the sampling window.

A window is established where the tuning block is matched. For example, for a scenario where the tuning block is received correctly for a phase shift window of 90-degree and 180-degree, then an appropriate sampling point is established as 135-degree. Once a sampling point is established, no errors should be visible in the tuning block.

39.6.8 Card Detection Method

There are many methods for SDMMC/SDIO device detection.
- Method1: Using SDMMC_CDETECT register, which is value on card_detect_n input port.

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0 represents presence of card. This method is available only for SDMMC/SDIO.

- Method2: Using card detection unit in Host Controller, outputting host interrupt. The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounce associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value in SDMMC_DEBNCE [23:0]. Following figure illustrates the timing for card-detect signals. This method is available only for SDMMC/SDIO.

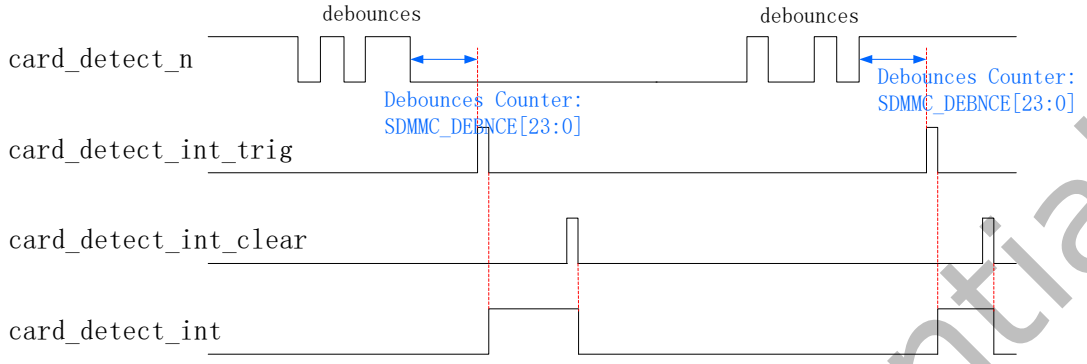

Fig. 39-16 Card Detection Method 2

- Method3: Using general card detection unit, outputting detect_dual_edge_int connecting to IRQ[288]. Similar to Method2, except that the debounce time is configurable by PMU1_GRF_SD_DETECT_CNT; and the insertion/removal detection interrupt can be enabled or cleared respectively.

The detailed register information is:

Table 39-16 Register for SDMMC Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rising_edge_irq_en	PMU1_GRF_SD_DETECT_CON[0]	0	Enable SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_falling_edge_detect_en	PMU1_GRF_SD_DETECT_CON[1]	0	Enable SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_rising_edge_dectect_status	PMU1_GRF_SD_DETECT_STS[0]	0	SDMMC detect pin rising edge status. 1'b0: Inactive 1'b1: Active
sd_detect_falling_edge_detect_status	PMU1_GRF_SD_DETECT_STS[1]	0	SDMMC detect pin falling edge status. 1'b0: Inactive 1'b1: Active
sd_detect_rising_edge_dectect_clr	PMU1_GRF_SD_DETECT_CLR[0]	0	Enable clear for SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_falling_edge_detect_clr	PMU1_GRF_SD_DETECT_CLR[1]	0	Enable clear for SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable

39.6.9 SDMMC IOMUX With JTAG

The GPIO2a2/GPIO2a3 for sdmmc_cdata2/sdmmc_cdata3 is shared with jtag_tck/jtag_tms. The condition of usage for SDMMC or JTAG usage is as follows.

- If TOP_IOC_MISC_CON0[1] is equal to 1 and SD/MMC card is not detected within detection time(defined in TOP_IOC_ SDMMC_DETN_FLT, in the unit of XIN24M clock), the GPIOs are used for JTAG.
- Otherwise, the GPIOs' usage is defined by IOMUX configuration.

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