Rockchip
RK3562
Technical Reference Manual
(Part 2)

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Revision History

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Chapter 1 Video Capture (VICAP)

1.1 Overview

The Video Capture, receives the data from Camera via MIPI, and transfers the data into system main memory by AXI bus or transfers the data into ISP.

- Support receiving four interfaces of MIPI CSI/DSI, up to four IDs for each interface
- Support VC/DT configurable for each ID
- Support five CSI data formats: RAW8/10/12/14, YUV422
- Support YUYV input sequence configurable and YUYV sequence reorder
- Support three modes of MIPI CSI HDR: virtual channel mode, identification code mode, line counter mode
- Support one DSI data formats: RGB888, support video mode/command mode
- Support reducing frame rate
- Support window cropping
- Support sending RAW data directly to ISP
- Support 8/16/32 times down-sampling for RAW data
- Support virtual stride when write to DDR
- Support NV16/NV12/YUV400/YUYV output format for YUV data
- Support compact/non-compact output format for RAW data
- Support DMA burst gather 2/4/8
- Support soft reset, auto-reset when DMA error
- Support MMU
- Support QOS(hurry/press)

1.2 Block Diagram

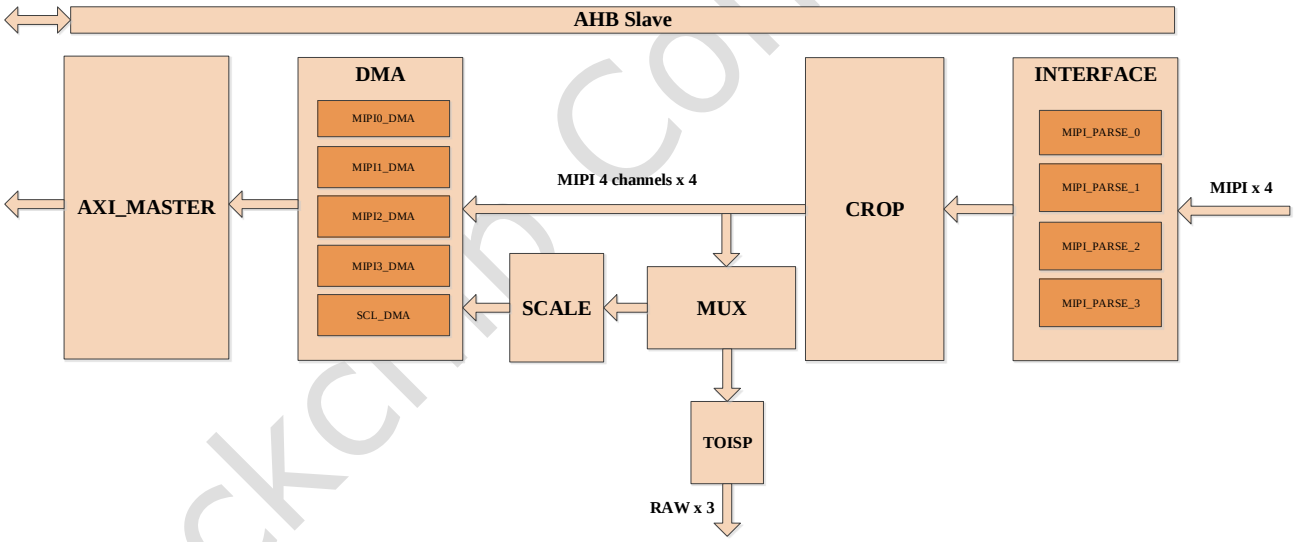

Fig.1-1 VICAP Block Diagram

VICAP is comprised of:

- AHB Slave
- AXI Master
- INTERFACE
- CROP
- SCALE
- TOISP
- DMA

1.3 Function Description

1.3.1 Interface

Translate the input video data into the requisite data format

- MIPI CSI RAW8 format

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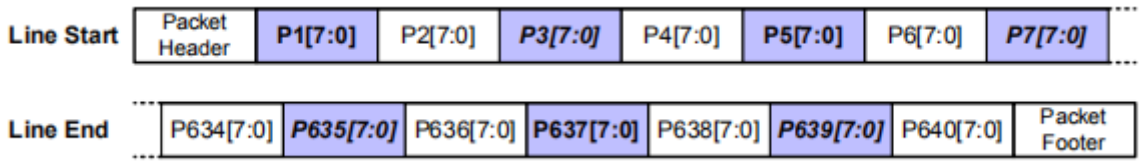

Fig.1-2 MIPI CSI RAW8 format

- MIPI CSI RAW10 format

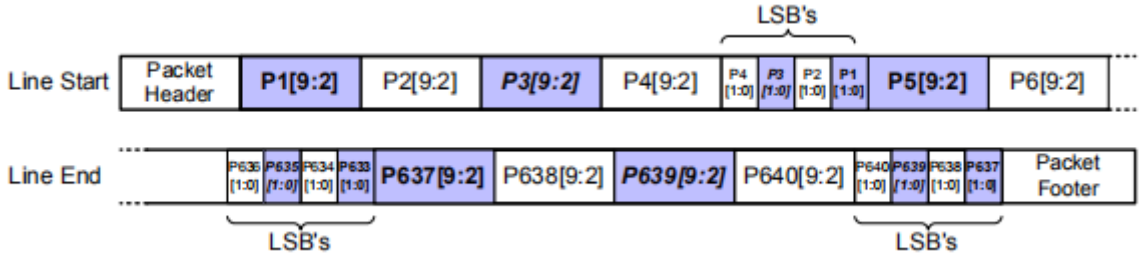

Fig.1-3 MIPI CSI RAW10 format

- MIPI CSI RAW12 format

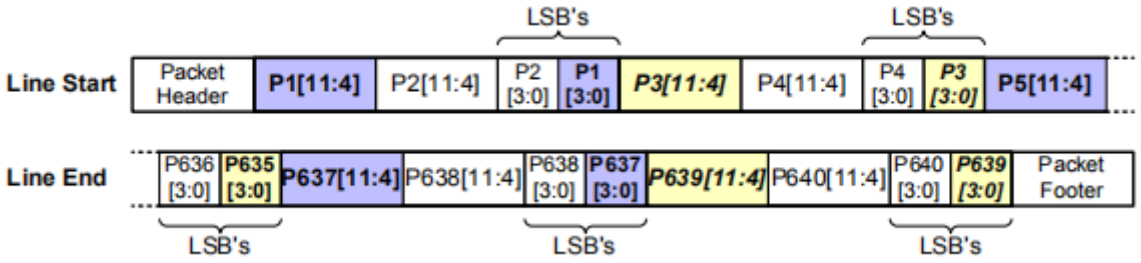

Fig.1-4 MIPI CSI RAW12 format

- MIPI CSI RAW14 format

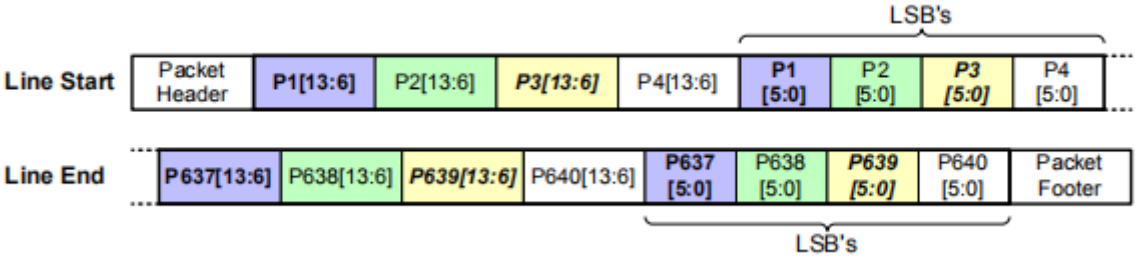

Fig.1-5 MIPI CSI RAW14 format

- MIPI CSI YUV422 format

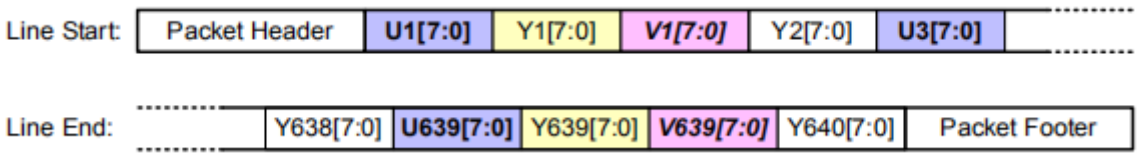

Fig.1-6 MIPI CSI YUV422 format

1.3.2 Crop

Bypass or crop the source video data to a smaller size destination.

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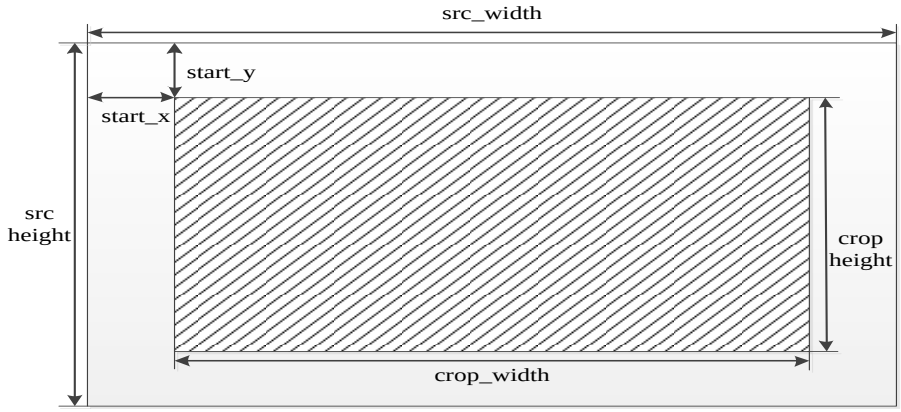

Fig.1-7 Crop

1.3.3 Scale

Scale down for RAW data.

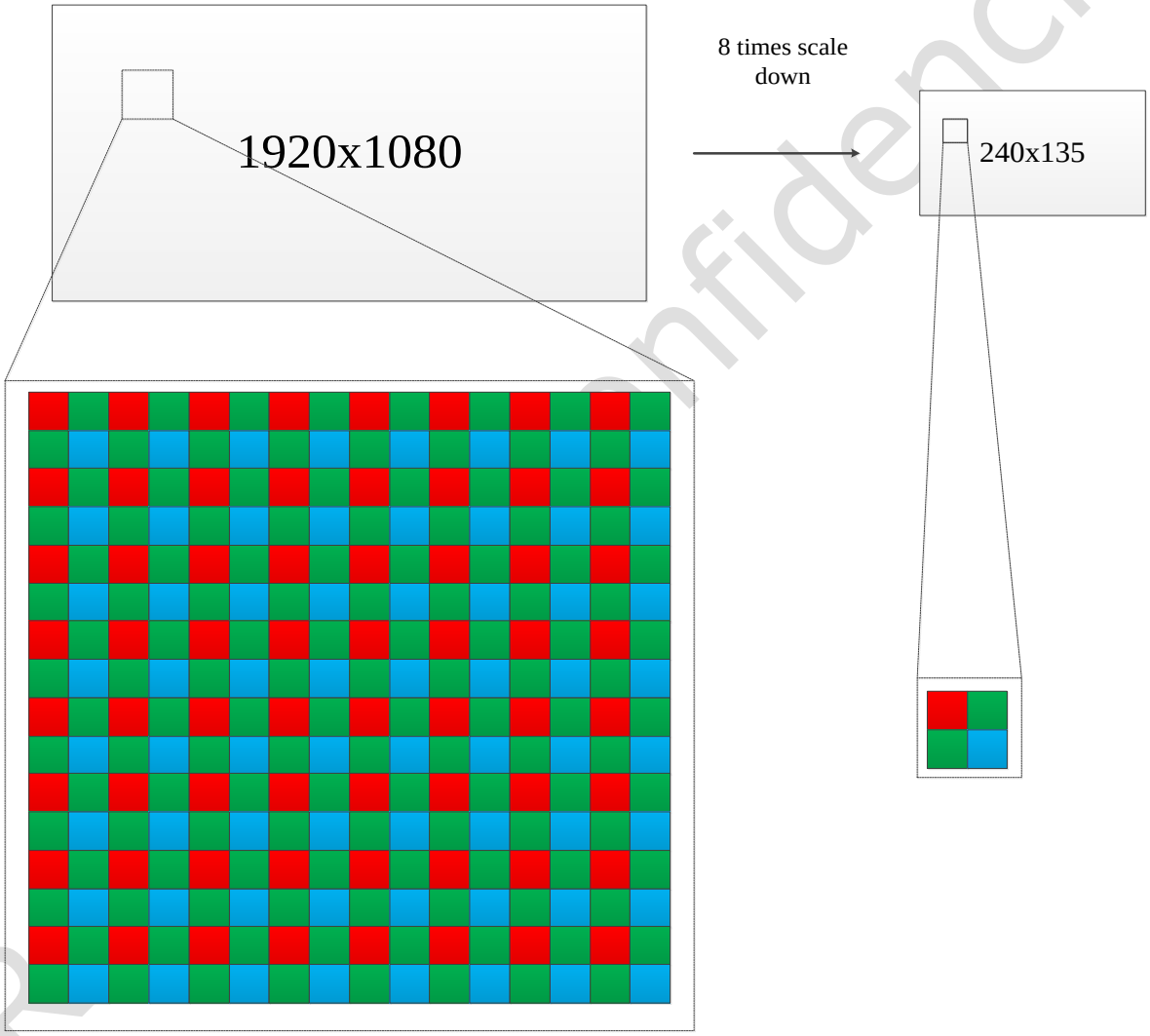

Fig.1-8 8 Times Scale down

1.3.4 Toisp

The parsed video data can go straight to ISP for real-time processing.

1.3.5 DMA

The DMA is used to transfer the data from crop module to the AXI master block which will send the data to the AXI bus.

- NV16

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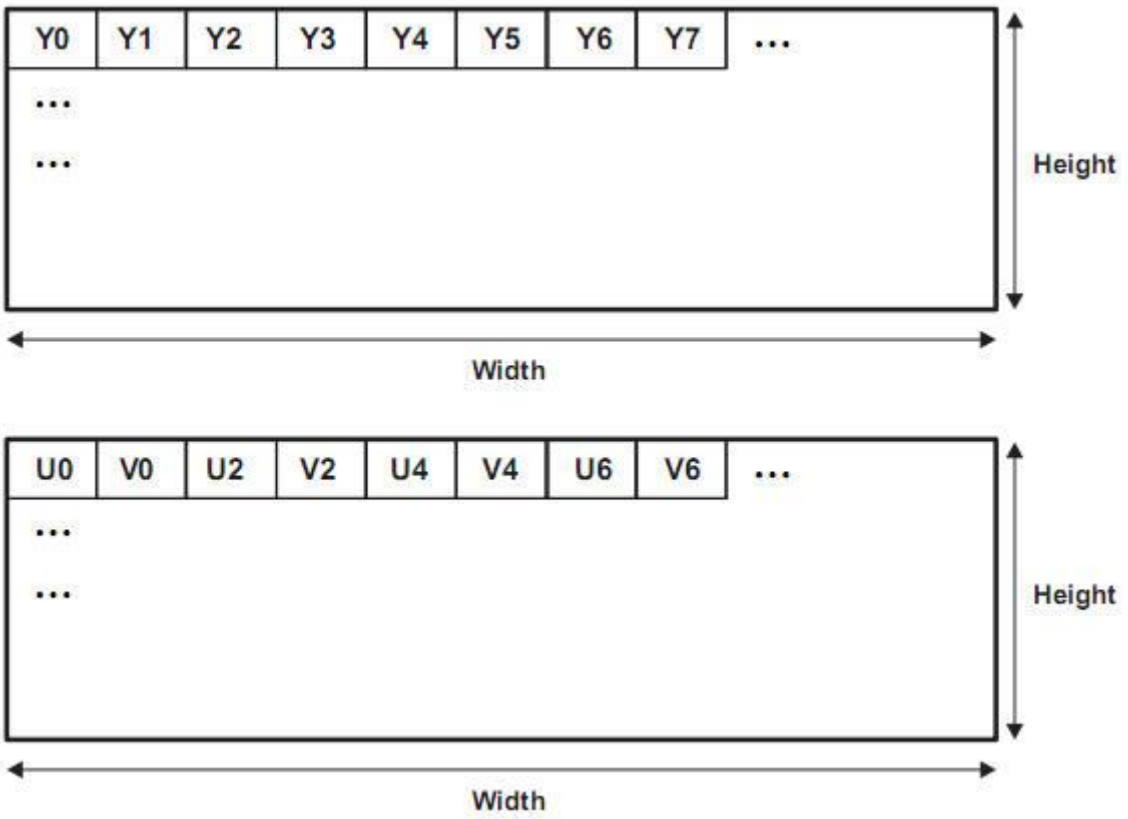

Fig. 1-9 NV16

- NV12

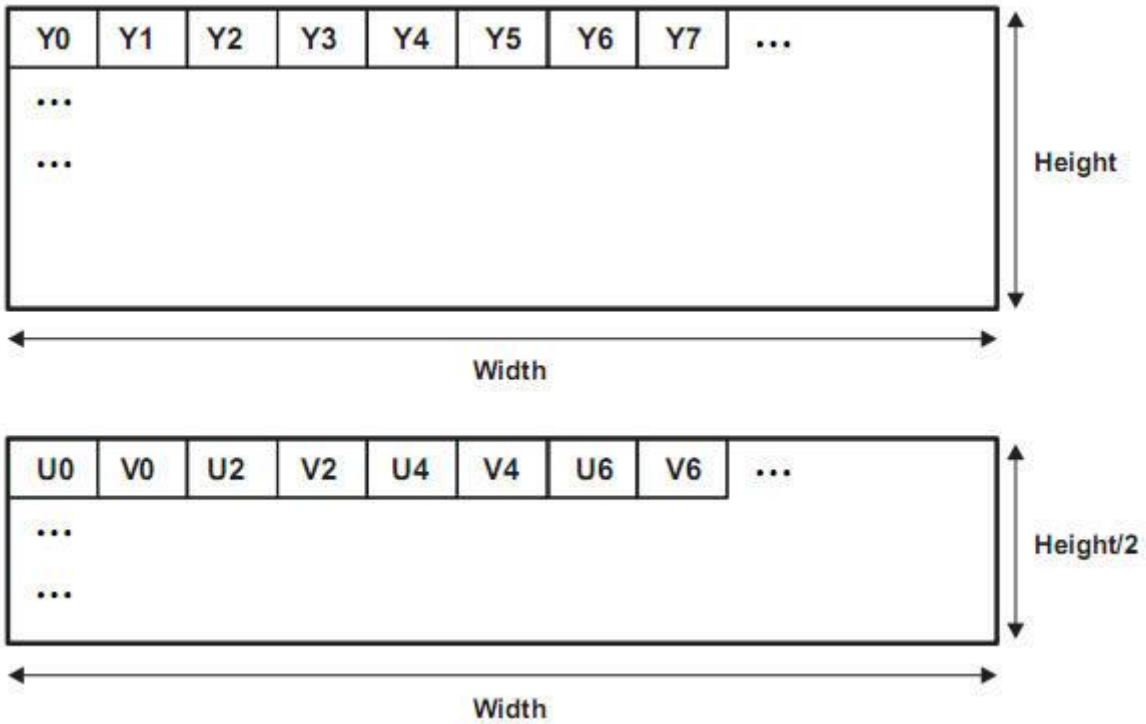

Fig.1-10 NV12

- YUV400

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Fig.1-11 YUV400

- YUYV

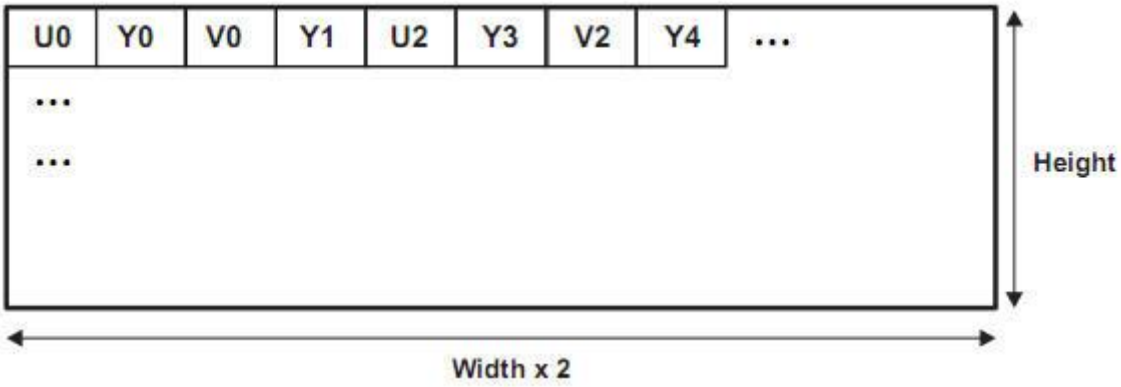

Fig.1-12 YUYV

- Compact RAW

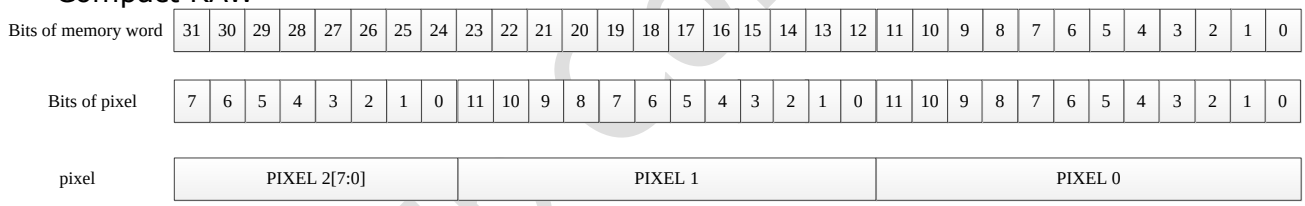

Fig.1-13 Compact RAW12

- Noncompact RAW

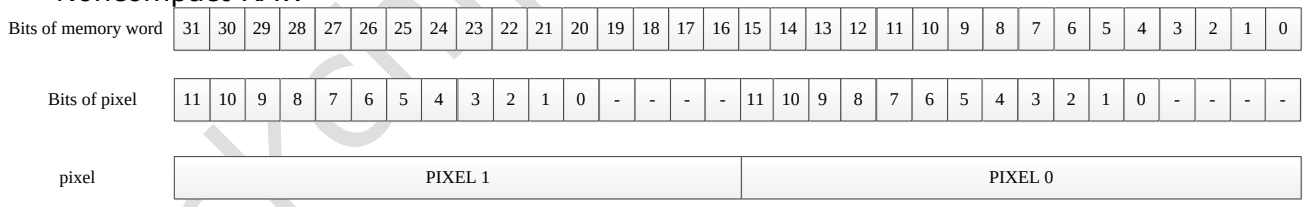

Fig.1-14 Noncompact RAW12(high align)

1.3.6 AXI Master

Transmit the data to chip memory via the AXI Master.

1.3.7 AHB Slave

Host configure the registers via the AHB Slave.

1.4 Register Description

1.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 1-1 VICAP Address Mapping

Base Address[11:8]	Device	Address Length	Offset Address Range
4'b0000	Global	256 BYTE	0x0000 ~ 0x00ff
4'b0001	MIPI0	512 BYTE	0x0100 ~ 0x02ff

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Base Address[11:8]	Device	Address Length	Offset Address Range
4'b0011	MIPI1	512 BYTE	0x0300 ~ 0x04ff
4'b0101	MIPI2	256 BYTE	0x0500 ~ 0x05ff
4'b0110	MIPI3	256 BYTE	0x0600 ~ 0x06ff
4'b0111	Scale/TOISP	256 BYTE	0x0700 ~ 0x07ff
4'b1000	MMU	256 BYTE	0x0800 ~ 0x08ff

1.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VICAP_GLB_CTRL	0x0000	W	0x00011C01	VICAP global control
VICAP_GLB_INTEN	0x0004	W	0x00000000	VICAP global interrupt enable.
VICAP_GLB_INTST	0x0008	W	0x00000000	VICAP global interrupt status.
VICAP_MIPI0_ID0_CTRL0	0x0100	W	0x00000000	MIPI0 path id0 control0
VICAP_MIPI0_ID0_CTRL1	0x0104	W	0x00000000	MIPI0 path id0 control1
VICAP_MIPI0_ID1_CTRL0	0x0108	W	0x00000000	MIPI0 path id1 control0
VICAP_MIPI0_ID1_CTRL1	0x010C	W	0x00000000	MIPI0 path id1 control1
VICAP_MIPI0_ID2_CTRL0	0x0110	W	0x00000000	MIPI0 path id2 control0
VICAP_MIPI0_ID2_CTRL1	0x0114	W	0x00000000	MIPI0 path id2 control1
VICAP_MIPI0_ID3_CTRL0	0x0118	W	0x00000000	MIPI0 path id3 control0
VICAP_MIPI0_ID3_CTRL1	0x011C	W	0x00000000	MIPI0 path id3 control1
VICAP_MIPI0_CTRL	0x0120	W	0x00000000	MIPI0 path control
VICAP_MIPI0_FRAME0_ADDR_Y_ID0	0x0124	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI0_FRAME1_ADDR_Y_ID0	0x0128	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI0_FRAME0_ADDR_UV_ID0	0x012C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI0_FRAME1_ADDR_UV_ID0	0x0130	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI0_VLW_ID0	0x0134	W	0x00000000	Virtual line width for ID0
VICAP_MIPI0_FRAME0_ADDR_Y_ID1	0x0138	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI0_FRAME1_ADDR_Y_ID1	0x013C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI0_FRAME0_ADDR_UV_ID1	0x0140	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI0_FRAME1_ADDR_UV_ID1	0x0144	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI0_VLW_ID1	0x0148	W	0x00000000	Virtual line width for ID1 path
VICAP_MIPI0_FRAME0_ADDR_Y_ID2	0x014C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI0_FRAME1_ADDR_Y_ID2	0x0150	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI0_FRAME0_ADDR_UV_ID2	0x0154	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI0_FRAME1_ADDR_UV_ID2	0x0158	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI0_VLW_ID2	0x015C	W	0x00000000	Virtual line width for ID2 path
VICAP_MIPI0_FRAME0_ADDR_Y_ID3	0x0160	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI0_FRAME1_ADDR_Y_ID3	0x0164	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI0_FRAME0_ADDR_UV_ID3	0x0168	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI0_FRAME1_ADDR_UV_ID3	0x016C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI0_VLW_ID3	0x0170	W	0x00000000	Virtual line width for ID3 path
VICAP_MIPI0_INTEN	0x0174	W	0x00000000	MIPI0 path interrupt enable
VICAP_MIPI0_INTSTAT	0x0178	W	0x00000000	MIPI0 path interrupt status
VICAP_MIPI0_LINE_INT_NUM_ID0_1	0x017C	W	0x00400040	Line number of the MIPI0 path ID0/1 line interrupt
VICAP_MIPI0_LINE_INT_NUM_ID2_3	0x0180	W	0x00400040	Line number of the MIPI0 path ID2/3 line interrupt
VICAP_MIPI0_LINE_CNT_ID0_1	0x0184	W	0x00000000	Line count of the MIPI0 path ID0/1
VICAP_MIPI0_LINE_CNT_ID2_3	0x0188	W	0x00000000	Line count of the MIPI0 path ID2/3
VICAP_MIPI0_ID0_CROP_START	0x018C	W	0x00000000	The start point of MIPI0 ID0 cropping
VICAP_MIPI0_ID1_CROP_START	0x0190	W	0x00000000	The start point of MIPI0 ID1 cropping
VICAP_MIPI0_ID2_CROP_START	0x0194	W	0x00000000	The start point of MIPI0 ID2 cropping
VICAP_MIPI0_ID3_CROP_START	0x0198	W	0x00000000	The start point of MIPI0 ID3 cropping
VICAP_MIPI0_FRAME_NUM_VC0	0x019C	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI0_FRAME_NUM_VC1	0x01A0	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI0_FRAME_NUM_VC2	0x01A4	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI0_FRAME_NUM_VC3	0x01A8	W	0x00000000	The frame number of virtual channel 3
VICAP_MIPI0_ID0_EFFECT_CODE	0x01AC	W	0x00000000	The effect code of MIPI0 ID0
VICAP_MIPI0_ID1_EFFECT_CODE	0x01B0	W	0x00000000	The effect code of MIPI0 ID1
VICAP_MIPI0_ID2_EFFECT_CODE	0x01B4	W	0x00000000	The effect code of MIPI0 ID2
VICAP_MIPI0_ID3_EFFECT_CODE	0x01B8	W	0x00000000	The effect code of MIPI0 ID3
VICAP_MIPI0_ON_PAD_VALUE	0x01BC	W	0x00000000	The ON padding value of MIPI0
VICAP_MIPI0_SIZE_NUM_ID0	0x01C0	W	0x00000000	MIPI0 path ID0 SIZE NUMBER
VICAP_MIPI0_SIZE_NUM_ID1	0x01C4	W	0x00000000	MIPI0 path ID1 SIZE NUMBER
VICAP_MIPI0_SIZE_NUM_ID2	0x01C8	W	0x00000000	MIPI0 path ID2 SIZE NUMBER
VICAP_MIPI0_SIZE_NUM_ID3	0x01CC	W	0x00000000	MIPI0 path ID3 SIZE NUMBER
VICAP_MIPI1_ID0_CTRL0	0x0300	W	0x00000000	MIPI1 path id0 control0
VICAP_MIPI1_ID0_CTRL1	0x0304	W	0x00000000	MIPI1 path id0 control1
VICAP_MIPI1_ID1_CTRL0	0x0308	W	0x00000000	MIPI1 path id1 control0
VICAP_MIPI1_ID1_CTRL1	0x030C	W	0x00000000	MIPI1 path id1 control1
VICAP_MIPI1_ID2_CTRL0	0x0310	W	0x00000000	MIPI1 path id2 control0

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI1_ID2_CTRL1	0x0314	W	0x00000000	MIPI1 path id2 control1
VICAP_MIPI1_ID3_CTRL0	0x0318	W	0x00000000	MIPI1 path id3 control0
VICAP_MIPI1_ID3_CTRL1	0x031C	W	0x00000000	MIPI1 path id3 control1
VICAP_MIPI1_CTRL	0x0320	W	0x00000000	MIPI1 path control
VICAP_MIPI1_FRAME0_ADDR_Y_ID0	0x0324	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI1_FRAME1_ADDR_Y_ID0	0x0328	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI1_FRAME0_ADDR_UV_ID0	0x032C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI1_FRAME1_ADDR_UV_ID0	0x0330	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI1_VLW_ID0	0x0334	W	0x00000000	Virtual line width for ID0
VICAP_MIPI1_FRAME0_ADDR_Y_ID1	0x0338	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI1_FRAME1_ADDR_Y_ID1	0x033C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI1_FRAME0_ADDR_UV_ID1	0x0340	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI1_FRAME1_ADDR_UV_ID1	0x0344	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI1_VLW_ID1	0x0348	W	0x00000000	Virtual line width for ID1 path
VICAP_MIPI1_FRAME0_ADDR_Y_ID2	0x034C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI1_FRAME1_ADDR_Y_ID2	0x0350	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI1_FRAME0_ADDR_UV_ID2	0x0354	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI1_FRAME1_ADDR_UV_ID2	0x0358	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI1_VLW_ID2	0x035C	W	0x00000000	Virtual line width for ID2 path
VICAP_MIPI1_FRAME0_ADDR_Y_ID3	0x0360	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI1_FRAME1_ADDR_Y_ID3	0x0364	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI1_FRAME0_ADDR_UV_ID3	0x0368	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI1_FRAME1_ADDR_UV_ID3	0x036C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI1_VLW_ID3	0x0370	W	0x00000000	Virtual line width for ID3 path
VICAP_MIPI1_INTEN	0x0374	W	0x00000000	MIPI1 path interrupt enable
VICAP_MIPI1_INTSTAT	0x0378	W	0x00000000	MIPI1 path interrupt status
VICAP_MIPI1_LINE_INT_NUM_ID0_1	0x037C	W	0x00400040	Line number of the MIPI1 path ID0/1 line interrupt
VICAP_MIPI1_LINE_INT_NUM_ID2_3	0x0380	W	0x00400040	Line number of the MIPI1 path ID2/3 line interrupt
VICAP_MIPI1_LINE_CNT_ID0_1	0x0384	W	0x00000000	Line count of the MIPI1 path ID0/1
VICAP_MIPI1_LINE_CNT_ID2_3	0x0388	W	0x00000000	Line count of the MIPI1 path ID2/3
VICAP_MIPI1_ID0_CROP_START	0x038C	W	0x00000000	The start point of MIPI1 ID0 cropping

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI1_ID1_CROP_START	0x0390	W	0x00000000	The start point of MIPI1 ID1 cropping
VICAP_MIPI1_ID2_CROP_START	0x0394	W	0x00000000	The start point of MIPI1 ID2 cropping
VICAP_MIPI1_ID3_CROP_START	0x0398	W	0x00000000	The start point of MIPI1 ID3 cropping
VICAP_MIPI1_FRAME_NUM_VC0	0x039C	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI1_FRAME_NUM_VC1	0x03A0	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI1_FRAME_NUM_VC2	0x03A4	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI1_FRAME_NUM_VC3	0x03A8	W	0x00000000	The frame number of virtual channel 3
VICAP_MIPI1_ID0_EFFECT_CODE	0x03AC	W	0x00000000	The effect code of MIPI1 ID0
VICAP_MIPI1_ID1_EFFECT_CODE	0x03B0	W	0x00000000	The effect code of MIPI1 ID1
VICAP_MIPI1_ID2_EFFECT_CODE	0x03B4	W	0x00000000	The effect code of MIPI2 ID2
VICAP_MIPI1_ID3_EFFECT_CODE	0x03B8	W	0x00000000	The effect code of MIPI1 ID3
VICAP_MIPI1_ON_PAD_VALUE	0x03BC	W	0x00000000	The ON padding value of MIPI1
VICAP_MIPI1_SIZE_NUM_ID0	0x03C0	W	0x00000000	MIPI1 path ID0 SIZE NUMBER
VICAP_MIPI1_SIZE_NUM_ID1	0x03C4	W	0x00000000	MIPI1 path ID1 SIZE NUMBER
VICAP_MIPI1_SIZE_NUM_ID2	0x03C8	W	0x00000000	MIPI1 path ID2 SIZE NUMBER
VICAP_MIPI1_SIZE_NUM_ID3	0x03CC	W	0x00000000	MIPI1 path ID3 SIZE NUMBER
VICAP_MIPI2_ID0_CTRL0	0x0500	W	0x00000000	MIPI2 path id0 control0
VICAP_MIPI2_ID0_CTRL1	0x0504	W	0x00000000	MIPI2 path id0 control1
VICAP_MIPI2_ID1_CTRL0	0x0508	W	0x00000000	MIPI2 path id1 control0
VICAP_MIPI2_ID1_CTRL1	0x050C	W	0x00000000	MIPI2 path id1 control1
VICAP_MIPI2_ID2_CTRL0	0x0510	W	0x00000000	MIPI2 path id2 control0
VICAP_MIPI2_ID2_CTRL1	0x0514	W	0x00000000	MIPI2 path id2 control1
VICAP_MIPI2_ID3_CTRL0	0x0518	W	0x00000000	MIPI2 path id3 control0
VICAP_MIPI2_ID3_CTRL1	0x051C	W	0x00000000	MIPI2 path id3 control1
VICAP_MIPI2_CTRL	0x0520	W	0x00000000	MIPI2 path control
VICAP_MIPI2_FRAME0_ADDR_Y_ID0	0x0524	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI2_FRAME1_ADDR_Y_ID0	0x0528	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI2_FRAME0_ADDR_UV_ID0	0x052C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI2_FRAME1_ADDR_UV_ID0	0x0530	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI2_VLW_ID0	0x0534	W	0x00000000	Virtual line width for ID0
VICAP_MIPI2_FRAME0_ADDR_Y_ID1	0x0538	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI2_FRAME1_ADDR_Y_ID1	0x053C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI2_FRAME0_ADDR_UV_ID1	0x0540	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI2_FRAME1_ADDR_UV_ID1	0x0544	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI2_VLW_ID1	0x0548	W	0x00000000	Virtual line width for ID1 path
VICAP_MIPI2_FRAME0_ADDR_Y_ID2	0x054C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI2_FRAME1_ADDR_Y_ID2	0x0550	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI2_FRAME0_ADDR_UV_ID2	0x0554	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI2_FRAME1_ADDR_UV_ID2	0x0558	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI2_VLW_ID2	0x055C	W	0x00000000	Virtual line width for ID2 path
VICAP_MIPI2_FRAME0_ADDR_Y_ID3	0x0560	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI2_FRAME1_ADDR_Y_ID3	0x0564	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI2_FRAME0_ADDR_UV_ID3	0x0568	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI2_FRAME1_ADDR_UV_ID3	0x056C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI2_VLW_ID3	0x0570	W	0x00000000	Virtual line width for ID3 path
VICAP_MIPI2_INTEN	0x0574	W	0x00000000	MIPI2 path interrupt enable
VICAP_MIPI2_INTSTAT	0x0578	W	0x00000000	MIPI2 path interrupt status
VICAP_MIPI2_LINE_INT_NUM_ID0_1	0x057C	W	0x00400040	Line number of the MIPI2 path ID0/1 line interrupt
VICAP_MIPI2_LINE_INT_NUM_ID2_3	0x0580	W	0x00400040	Line number of the MIPI2 path ID2/3 line interrupt
VICAP_MIPI2_LINE_CNT_ID0_1	0x0584	W	0x00000000	Line count of the MIPI2 path ID0/1
VICAP_MIPI2_LINE_CNT_ID2_3	0x0588	W	0x00000000	Line count of the MIPI2 path ID2/3
VICAP_MIPI2_ID0_CROP_START	0x058C	W	0x00000000	The start point of MIPI2 ID0 cropping
VICAP_MIPI2_ID1_CROP_START	0x0590	W	0x00000000	The start point of MIPI2 ID1 cropping
VICAP_MIPI2_ID2_CROP_START	0x0594	W	0x00000000	The start point of MIPI2 ID2 cropping
VICAP_MIPI2_ID3_CROP_START	0x0598	W	0x00000000	The start point of MIPI2 ID3 cropping
VICAP_MIPI2_FRAME_NUM_VC0	0x059C	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI2_FRAME_NUM_VC1	0x05A0	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI2_FRAME_NUM_VC2	0x05A4	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI2_FRAME_NUM_VC3	0x05A8	W	0x00000000	The frame number of virtual channel 3
VICAP_MIPI2_ID0_EFFECT_CODE	0x05AC	W	0x00000000	The effect code of MIPI2 ID0

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI2_ID1_EFFECT_CODE	0x05B0	W	0x00000000	The effect code of MIPI2 ID1
VICAP_MIPI2_ID2_EFFECT_CODE	0x05B4	W	0x00000000	The effect code of MIPI2 ID2
VICAP_MIPI2_ID3_EFFECT_CODE	0x05B8	W	0x00000000	The effect code of MIPI2 ID3
VICAP_MIPI2_ON_PAD_VALUE	0x05BC	W	0x00000000	The ON padding value of MIPI2
VICAP_MIPI2_SIZE_NUM_ID0	0x05C0	W	0x00000000	MIPI2 path ID0 SIZE NUMBER
VICAP_MIPI2_SIZE_NUM_ID1	0x05C4	W	0x00000000	MIPI2 path ID1 SIZE NUMBER
VICAP_MIPI2_SIZE_NUM_ID2	0x05C8	W	0x00000000	MIPI2 path ID2 SIZE NUMBER
VICAP_MIPI2_SIZE_NUM_ID3	0x05CC	W	0x00000000	MIPI2 path ID3 SIZE NUMBER
VICAP_MIPI3_ID0_CTRL0	0x0600	W	0x00000000	MIPI3 path id0 control0
VICAP_MIPI3_ID0_CTRL1	0x0604	W	0x00000000	MIPI3 path id0 control1
VICAP_MIPI3_ID1_CTRL0	0x0608	W	0x00000000	MIPI3 path id1 control0
VICAP_MIPI3_ID1_CTRL1	0x060C	W	0x00000000	MIPI3 path id1 control1
VICAP_MIPI3_ID2_CTRL0	0x0610	W	0x00000000	MIPI3 path id2 control0
VICAP_MIPI3_ID2_CTRL1	0x0614	W	0x00000000	MIPI3 path id2 control1
VICAP_MIPI3_ID3_CTRL0	0x0618	W	0x00000000	MIPI3 path id3 control0
VICAP_MIPI3_ID3_CTRL1	0x061C	W	0x00000000	MIPI3 path id3 control1
VICAP_MIPI3_CTRL	0x0620	W	0x00000000	MIPI3 path control
VICAP_MIPI3_FRAME0_ADDR_Y_ID0	0x0624	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI3_FRAME1_ADDR_Y_ID0	0x0628	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI3_FRAME0_ADDR_UV_ID0	0x062C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI3_FRAME1_ADDR_UV_ID0	0x0630	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI3_VLW_ID0	0x0634	W	0x00000000	Virtual line width for ID0
VICAP_MIPI3_FRAME0_ADDR_Y_ID1	0x0638	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI3_FRAME1_ADDR_Y_ID1	0x063C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI3_FRAME0_ADDR_UV_ID1	0x0640	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI3_FRAME1_ADDR_UV_ID1	0x0644	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI3_VLW_ID1	0x0648	W	0x00000000	Virtual line width for ID1 path
VICAP_MIPI3_FRAME0_ADDR_Y_ID2	0x064C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI3_FRAME1_ADDR_Y_ID2	0x0650	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI3_FRAME0_ADDR_UV_ID2	0x0654	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI3_FRAME1_ADDR_UV_ID2	0x0658	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI3_VLW_ID2	0x065C	W	0x00000000	Virtual line width for ID2 path

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI3_FRAME0_ADDR_Y_ID3	0x0660	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI3_FRAME1_ADDR_Y_ID3	0x0664	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI3_FRAME0_ADDR_UV_ID3	0x0668	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI3_FRAME1_ADDR_UV_ID3	0x066C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI3_VLW_ID3	0x0670	W	0x00000000	Virtual line width for ID3 path
VICAP_MIPI3_INTEN	0x0674	W	0x00000000	MIPI3 path interrupt enable
VICAP_MIPI3_INTSTAT	0x0678	W	0x00000000	MIPI3 path interrupt status
VICAP_MIPI3_LINE_INT_NUM_ID0_1	0x067C	W	0x00400040	Line number of the MIPI3 path ID0/1 line interrupt
VICAP_MIPI3_LINE_INT_NUM_ID2_3	0x0680	W	0x00400040	Line number of the MIPI3 path ID2/3 line interrupt
VICAP_MIPI3_LINE_CNT_ID0_1	0x0684	W	0x00000000	Line count of the MIPI3 path ID0/1
VICAP_MIPI3_LINE_CNT_ID2_3	0x0688	W	0x00000000	Line count of the MIPI3 path ID2/3
VICAP_MIPI3_ID0_CROP_START	0x068C	W	0x00000000	The start point of MIPI3 ID0 cropping
VICAP_MIPI3_ID1_CROP_START	0x0690	W	0x00000000	The start point of MIPI3 ID1 cropping
VICAP_MIPI3_ID2_CROP_START	0x0694	W	0x00000000	The start point of MIPI3 ID2 cropping
VICAP_MIPI3_ID3_CROP_START	0x0698	W	0x00000000	The start point of MIPI3 ID3 cropping
VICAP_MIPI3_FRAME_NUM_VC0	0x069C	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI3_FRAME_NUM_VC1	0x06A0	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI3_FRAME_NUM_VC2	0x06A4	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI3_FRAME_NUM_VC3	0x06A8	W	0x00000000	The frame number of virtual channel 3
VICAP_MIPI3_ID0_EFFECT_CODE	0x06AC	W	0x00000000	The effect code of MIPI3 ID0
VICAP_MIPI3_ID1_EFFECT_CODE	0x06B0	W	0x00000000	The effect code of MIPI3 ID1
VICAP_MIPI3_ID2_EFFECT_CODE	0x06B4	W	0x00000000	The effect code of MIPI3 ID2
VICAP_MIPI3_ID3_EFFECT_CODE	0x06B8	W	0x00000000	The effect code of MIPI3 ID3
VICAP_MIPI3_ON_PAD_VALUE	0x06BC	W	0x00000000	The ON padding value of MIPI3
VICAP_MIPI3_SIZE_NUM_ID0	0x06C0	W	0x00000000	MIPI3 path ID0 SIZE NUMBER
VICAP_MIPI3_SIZE_NUM_ID1	0x06C4	W	0x00000000	MIPI3 path ID1 SIZE NUMBER
VICAP_MIPI3_SIZE_NUM_ID2	0x06C8	W	0x00000000	MIPI3 path ID2 SIZE NUMBER
VICAP_MIPI3_SIZE_NUM_ID3	0x06CC	W	0x00000000	MIPI3 path ID3 SIZE NUMBER
VICAP_SCL_CH_CTRL	0x0700	W	0x00000000	Scale channel0 path control

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Name	Offset	Size	Reset Value	Description
VICAP_SCL_CTRL	0x0704	W	0x00000000	MIPI3 path control
VICAP_SCL_FRAME0_ADDR_CH0	0x0708	W	0x00000000	First address of even frame for CH0 path
VICAP_SCL_FRAME1_ADDR_CH0	0x070C	W	0x00000000	First address of odd frame for CH0 path
VICAP_SCL_VLW_CH0	0x0710	W	0x00000000	Virtual line width for CH0
VICAP_SCL_CH0_BLACK_LEVEL	0x0738	W	0x00000000	Scale channel0 black level
VICAP_TOISP0_CH_CTRL	0x0780	W	0x00000000	TOISP0 path control
VICAP_TOISP0_CROP_SIZE	0x0784	W	0x00000000	The expected width and height of received image
VICAP_TOISP0_CROP_START	0x0788	W	0x00000000	The start point of toisp0 path cropping
VICAP_MMU0_DTE_ADDR	0x0800	W	0x00000000	MMU0 current page table address
VICAP_MMU0_STATUS	0x0804	W	0x00000000	MMU0 status register
VICAP_MMU0_COMMAND	0x0808	W	0x00000000	MMU0 command register
VICAP_MMU0_PAGE_FAULT_ADDR	0x080C	W	0x00000000	MMU0 logical address of last page fault
VICAP_MMU0_ZAP_ONE_LINE	0x0810	W	0x00000000	MMU0 Zap cache line register
VICAP_MMU0_INT_RAWSTAT	0x0814	W	0x00000000	MMU0 raw interrupt status register
VICAP_MMU0_INT_CLEAR	0x0818	W	0x00000000	MMU0 interrupt status clear
VICAP_MMU0_INT_MASK	0x081C	W	0x00000000	MMU0 interrupt mask
VICAP_MMU0_INT_STATUS	0x0820	W	0x00000000	MMU0 interrupt status
VICAP_MMU0_AUTO_GATING	0x0824	W	0x00000000	MMU0 auto gating

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.3 Detail Registers Description

VICAP_GLB_CTRL

Address: Operational Base(0xFF3E0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x1	ro_axi_idle 1'b0: AXI is working 1'b1: AXI is idle.
15:14	RO	0x0	reserved
13:12	RW	0x1	sw_dma_group_mode 2'b00: Group 2 (2 bursts gather) 2'b01: Group 4 (4 bursts gather) 2'b10: Group 8 (8 bursts gather) 2'b11: Group 8 (8 bursts gather) This register is valid when sw_dma_group_en=1.
11	RW	0x1	sw_dma_adapt_en 1'b0: Disable dma self-adapt(dma will transport data according the configured height) 1'b1: Enable dma self-adapt(dma will transport data according the actual height).
10	RW	0x1	sw_dma_group_en 1'b0: Disable dma burst group 1'b1: Enable dma burst group.

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Bit	Attr	Reset Value	Description
9	RW	0x0	sw_infrst_en 1'b0: Disable pre-interface reset 1'b1: Enable pre-interface reset.
8	RW	0x0	sw_clk_gating_dis 1'b0: Enable the auto clk gating 1'b1: Disable the auto clk gating
7	RO	0x0	reserved
6:5	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
4	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP(except MMU/AXI MASTER/REG FILE)
3:1	RO	0x0	reserved
0	RW	0x1	sw_cap_en 1'b0: Disable all interface capture 1'b1: Enable capture(still depends on sw_xxx_cap_en).

VICAP_GLB_INTEN

Address: Operational Base(0xFF3E0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	toisp0_fifo_overflow_inten Enable the interrupt of fifo overflow of TOISP0 path. 1'b0: Disable 1'b1: Enable
25:23	RO	0x0	reserved
22	RW	0x0	frame_end_toisp0_ch2_inten Enable the interrupt of frame end for TOISP0 channel2. 1'b0: Disable 1'b1: Enable
21	RW	0x0	frame_end_toisp0_ch1_inten Enable the interrupt of frame end for TOISP0 channel1. 1'b0: Disable 1'b1: Enable
20	RW	0x0	frame_end_toisp0_ch0_inten Enable the interrupt of frame end for TOISP0 channel0. 1'b0: Disable 1'b1: Enable
19:17	RO	0x0	reserved
16	RW	0x0	frame_start_toisp0_ch2_inten Enable the interrupt of frame start for TOISP0 channel2. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame_start_toisp0_ch1_inten Enable the interrupt of frame start for TOISP0 channel1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame_start_toisp0_ch0_inten Enable the interrupt of frame start for TOISP0 channel0. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
13:11	RO	0x0	reserved
10	RW	0x0	dma_fifo_overflow_scl_ch0_inten Enable the interrupt of dma fifo overflow of scale path CH0. 1'b0: Disable 1'b1: Enable
9:4	RO	0x00	reserved
3	RW	0x0	frame1_dma_end_scl_ch0_inten Enable the interrupt of end of odd frame for scale CH0. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame0_dma_end_scl_ch0_inten Enable the interrupt of end of even frame for scale CH0. 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	axi0_bus_err_inten Enable the interrupt of axi0 bus error. 1'b0: Disable 1'b1: Enable

VICAP_GLB_INTST

Address: Operational Base(0xFF3E0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	W1C	0x0	toisp0_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
25:23	RO	0x0	reserved
22	W1C	0x0	frame_end_toisp0_ch2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	frame_end_toisp0_ch1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	frame_end_toisp0_ch0_intst 1'b0: No interrupt 1'b1: Interrupt
19:17	RO	0x0	reserved
16	W1C	0x0	frame_start_toisp0_ch2_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame_start_toisp0_ch1_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame_start_toisp0_ch0_intst 1'b0: No interrupt 1'b1: Interrupt
13:11	RO	0x0	reserved
10	W1C	0x0	dma_fifo_overflow_scl_ch0_intst 1'b0: No interrupt 1'b1: Interrupt
9:4	RO	0x00	reserved
3	W1C	0x0	frame1_dma_end_scl_ch0_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
2	W1C	0x0	frame0_dma_end_scl_ch0_intst 1'b0: No interrupt 1'b1: Interrupt
1	RO	0x0	reserved
0	W1C	0x0	axi0_bus_err_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI0_ID0_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id0 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id0 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi0_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id0 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU

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Bit	Attr	Reset Value	Description
17:16	RW	0x0	sw_yuyv_in_order_id0 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id0 Data type for id0.
9:8	RW	0x0	sw_vc_id0 Virtual channel for id0.
7:5	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id0 The parse type of id0. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_ID0_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI0_ID1_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id1 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id1 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id1 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id1 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id1 Data type for id1.
9:8	RW	0x0	sw_vc_id1 Virtual channel for id1.

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_wrddr_type_id1 The write ddr type of id1. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id1 The parse type of id1. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_ID1_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI0_ID2_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id2 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id2 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).

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Bit	Attr	Reset Value	Description
28	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4 pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id2 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id2 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id2 Data type for id2.
9:8	RW	0x0	sw_vc_id2 Virtual channel for id2.
7:5	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:1	RW	0x0	sw_parse_type_id2 The parse type of id2. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_ID2_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI0_ID3_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id3 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id3 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode

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Bit	Attr	Reset Value	Description
25:24	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id3 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id3 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id3 Data type for id3.
9:8	RW	0x0	sw_vc_id3 Virtual channel for id3.
7:5	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id3 The parse type of id3. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

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VICAP_MIPI0_ID3_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI0_CTRL

Address: Operational Base(0xFF3E0000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
29:24	RW	0x00	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
23:21	RW	0x0	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
20	RW	0x0	sw_drop_frame_en_all 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI0 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI0 path dma. When this bit change to 0,dma is reseted completely.
15:13	RW	0x0	sw_press_value Press value.
12	RW	0x0	sw_press_en 1'b0: Disable press 1'b1: Enable press
11	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.
10	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.
9	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
8	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_hurry_value Hurry value.
4	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry
3	RO	0x0	reserved
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

VICAP_MIPI0_FRAME0_ADDR_Y_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_Y_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_UV_ID0

Address: Operational Base(0xFF3E0000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_UV_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI0_VLW_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_Y_ID1

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Address: Operational Base(0xFF3E0000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_Y_ID1

Address: Operational Base(0xFF3E0000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_UV_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_UV_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI0_VLW_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_Y_ID2

Address: Operational Base(0xFF3E0000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_Y_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_UV_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0154)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_UV_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI0_VLW_ID2

Address: Operational Base(0xFF3E0000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_Y_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_Y_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_UV_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_UV_ID3

Address: Operational Base(0xFF3E0000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI0_VLW_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0170)

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Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI0_INTEN

Address: Operational Base(0xFF3E0000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame1_start_id3_inten Enable the interrupt of start of odd frame for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame0_start_id3_inten Enable the interrupt of start of even frame for ID3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame1_start_id2_inten Enable the interrupt of start of odd frame for ID2. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame0_start_id2_inten Enable the interrupt of start of even frame for ID2. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame1_start_id1_inten Enable the interrupt of start of odd frame for ID1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame0_start_id1_inten Enable the interrupt of start of even frame for ID1. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	frame1_start_id0_inten Enable the interrupt of start of odd frame for ID0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame0_start_id0_inten Enable the interrupt of start of even frame for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_INTSTAT

Address: Operational Base(0xFF3E0000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame1_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame0_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame1_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame0_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame1_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame0_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame1_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame0_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI0_LINE_INT_NUM_ID0_1

Address: Operational Base(0xFF3E0000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0040	line_int_num_id1 For one-time mode, if line_int_num_id1=100,then channel 1 receive 100th line, the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode, if line_int_num_id0=100,then channel 0 receive 100th line, the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

VICAP_MIPI0_LINE_INT_NUM_ID2_3

Address: Operational Base(0xFF3E0000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 For one-time mode, if line_int_num_id3=100,then channel 3 receive 100th line, the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode, if line_int_num_id2=100,then channel 2 receive 100th line, the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI0_LINE_CNT_ID0_1

Address: Operational Base(0xFF3E0000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI0_LINE_CNT_ID2_3

Address: Operational Base(0xFF3E0000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RO	0x0000	ro_line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id2 Current line count for id2.

VICAP_MIPI0_ID0_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI0_ID1_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI0_ID2_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI0_ID3_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI0_FRAME_NUM_VC0

Address: Operational Base(0xFF3E0000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI0_FRAME_NUM_VC1

Address: Operational Base(0xFF3E0000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI0_FRAME_NUM_VC2

Address: Operational Base(0xFF3E0000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI0_FRAME_NUM_VC3

Address: Operational Base(0xFF3E0000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_MIPI0_ID0_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI0_ID1_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x01B0)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI0_ID2_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI0_ID3_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

VICAP_MIPI0_ON_PAD_VALUE

Address: Operational Base(0xFF3E0000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI0_SIZE_NUM_ID0

Address: Operational Base(0xFF3E0000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI0_SIZE_NUM_ID1

Address: Operational Base(0xFF3E0000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

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VICAP_MIPI0_SIZE_NUM_ID2

Address: Operational Base(0xFF3E0000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI0_SIZE_NUM_ID3

Address: Operational Base(0xFF3E0000) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_MIPI1_ID0_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id0 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id0 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi0_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved

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Bit	Attr	Reset Value	Description
21:20	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id0 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id0 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id0 Data type for id0.
9:8	RW	0x0	sw_vc_id0 Virtual channel for id0.
7:5	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id0 The parse type of id0. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_ID0_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_width_id0 Width for id0. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI1_ID1_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id1 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id1 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id1 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU

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Bit	Attr	Reset Value	Description
17:16	RW	0x0	sw_yuyv_in_order_id1 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id1 Data type for id1.
9:8	RW	0x0	sw_vc_id1 Virtual channel for id1.
7:5	RW	0x0	sw_wrddr_type_id1 The write ddr type of id1. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id1 The parse type of id1. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_ID1_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI1_ID2_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0310)

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id2 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id2 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id2 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id2 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id2 Data type for id2.
9:8	RW	0x0	sw_vc_id2 Virtual channel for id2.

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id2 The parse type of id2. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_ID2_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI1_ID3_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id3 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id3 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).

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Bit	Attr	Reset Value	Description
28	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id3 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id3 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id3 Data type for id3.
9:8	RW	0x0	sw_vc_id3 Virtual channel for id3.
7:5	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:1	RW	0x0	sw_parse_type_id3 The parse type of id3. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_ID3_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI1_CTRL

Address: Operational Base(0xFF3E0000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
29:24	RW	0x00	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
23:21	RW	0x0	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
20	RW	0x0	sw_drop_frame_en_all 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI1 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI1 path dma. When this bit change to 0,dma is reseted completely.
15:13	RW	0x0	sw_press_value Press value.

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Bit	Attr	Reset Value	Description
12	RW	0x0	sw_press_en 1'b0: Disable press 1'b1: Enable press
11	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.
10	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.
9	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
8	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.
7:5	RW	0x0	sw_hurry_value Hurry value.
4	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry
3	RO	0x0	reserved
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

VICAP_MIPI1_FRAME0_ADDR_Y_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_Y_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_UV_ID0

Address: Operational Base(0xFF3E0000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_UV_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0330)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI1_VLW_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_Y_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_Y_ID1

Address: Operational Base(0xFF3E0000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_UV_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_UV_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI1_VLW_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_Y_ID2

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Address: Operational Base(0xFF3E0000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_Y_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_UV_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_UV_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0358)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI1_VLW_ID2

Address: Operational Base(0xFF3E0000) + offset (0x035C)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_Y_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0360)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_Y_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0364)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_UV_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0368)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_UV_ID3

Address: Operational Base(0xFF3E0000) + offset (0x036C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI1_VLW_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI1_INTEN

Address: Operational Base(0xFF3E0000) + offset (0x0374)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame1_start_id3_inten Enable the interrupt of start of odd frame for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame0_start_id3_inten Enable the interrupt of start of even frame for ID3. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	frame1_start_id2_inten Enable the interrupt of start of odd frame for ID2. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame0_start_id2_inten Enable the interrupt of start of even frame for ID2. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame1_start_id1_inten Enable the interrupt of start of odd frame for ID1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame0_start_id1_inten Enable the interrupt of start of even frame for ID1. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame1_start_id0_inten Enable the interrupt of start of odd frame for ID0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame0_start_id0_inten Enable the interrupt of start of even frame for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_INTSTAT

Address: Operational Base(0xFF3E0000) + offset (0x0378)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame1_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame0_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame1_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame0_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame1_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame0_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
1	W1C	0x0	frame1_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame0_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI1_LINE_INT_NUM_ID0_1

Address: Operational Base(0xFF3E0000) + offset (0x037C)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 For one-time mode, if line_int_num_id1=100,then channel 1 receive 100th line, the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode, if line_int_num_id0=100,then channel 0 receive 100th line, the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

VICAP_MIPI1_LINE_INT_NUM_ID2_3

Address: Operational Base(0xFF3E0000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 For one-time mode, if line_int_num_id3=100,then channel 3 receive 100th line, the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode, if line_int_num_id2=100,then channel 2 receive 100th line, the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

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VICAP_MIPI1_LINE_CNT_ID0_1

Address: Operational Base(0xFF3E0000) + offset (0x0384)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI1_LINE_CNT_ID2_3

Address: Operational Base(0xFF3E0000) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	line_cnt_id2 Current line count for id2.

VICAP_MIPI1_ID0_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x038C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI1_ID1_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0390)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI1_ID2_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0394)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI1_ID3_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0398)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI1_FRAME_NUM_VC0

Address: Operational Base(0xFF3E0000) + offset (0x039C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI1_FRAME_NUM_VC1

Address: Operational Base(0xFF3E0000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI1_FRAME_NUM_VC2

Address: Operational Base(0xFF3E0000) + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI1_FRAME_NUM_VC3

Address: Operational Base(0xFF3E0000) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

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VICAP_MIPI1_ID0_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI1_ID1_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI1_ID2_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI1_ID3_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

VICAP_MIPI1_ON_PAD_VALUE

Address: Operational Base(0xFF3E0000) + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI1_SIZE_NUM_ID0

Address: Operational Base(0xFF3E0000) + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI1_SIZE_NUM_ID1

Address: Operational Base(0xFF3E0000) + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

VICAP_MIPI1_SIZE_NUM_ID2

Address: Operational Base(0xFF3E0000) + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI1_SIZE_NUM_ID3

Address: Operational Base(0xFF3E0000) + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_MIPI2_ID0_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id0 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id0 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.

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Bit	Attr	Reset Value	Description
26	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi0_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id0 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id0 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id0 Data type for id0.
9:8	RW	0x0	sw_vc_id0 Virtual channel for id0.
7:5	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id0 The parse type of id0. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_ID0_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI2_ID1_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id1 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id1 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved

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Bit	Attr	Reset Value	Description
21:20	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id1 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id1 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id1 Data type for id1.
9:8	RW	0x0	sw_vc_id1 Virtual channel for id1.
7:5	RW	0x0	sw_wrddr_type_id1 The write ddr type of id1. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id1 The parse type of id1. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_ID1_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_width_id1 Width for id1. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI2_ID2_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id2 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id2 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id2 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU

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Bit	Attr	Reset Value	Description
17:16	RW	0x0	sw_yuyv_in_order_id2 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id2 Data type for id2.
9:8	RW	0x0	sw_vc_id2 Virtual channel for id2.
7:5	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id2 The parse type of id2. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_ID2_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x0514)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI2_ID3_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0518)

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id3 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id3 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id3 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id3 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id3 Data type for id3.
9:8	RW	0x0	sw_vc_id3 Virtual channel for id3.

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id3 The parse type of id3. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_ID3_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x051C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI2_CTRL

Address: Operational Base(0xFF3E0000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
29:24	RW	0x00	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
23:21	RW	0x0	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
20	RW	0x0	sw_drop_frame_en_all 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.

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Bit	Attr	Reset Value	Description
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI1 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI1 path dma. When this bit change to 0,dma is reseted completely.
15:13	RW	0x0	sw_press_value Press value.
12	RW	0x0	sw_press_en 1'b0: Disable press 1'b1: Enable press
11	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.
10	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.
9	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
8	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.
7:5	RW	0x0	sw_hurry_value Hurry value.
4	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry
3	RO	0x0	reserved
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

VICAP_MIPI2_FRAME0_ADDR_Y_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0524)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_Y_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0528)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_UV_ID0

Address: Operational Base(0xFF3E0000) + offset (0x052C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_UV_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI2_VLW_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0534)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_Y_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0538)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_Y_ID1

Address: Operational Base(0xFF3E0000) + offset (0x053C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_UV_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_UV_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0544)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI2_VLW_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0548)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_Y_ID2

Address: Operational Base(0xFF3E0000) + offset (0x054C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_Y_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0550)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_UV_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0554)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_UV_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0558)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI2_VLW_ID2

Address: Operational Base(0xFF3E0000) + offset (0x055C)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_Y_ID3

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Address: Operational Base(0xFF3E0000) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_Y_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0564)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_UV_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0568)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_UV_ID3

Address: Operational Base(0xFF3E0000) + offset (0x056C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI2_VLW_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0570)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI2_INTEN

Address: Operational Base(0xFF3E0000) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame1_start_id3_inten Enable the interrupt of start of odd frame for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame0_start_id3_inten Enable the interrupt of start of even frame for ID3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame1_start_id2_inten Enable the interrupt of start of odd frame for ID2. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame0_start_id2_inten Enable the interrupt of start of even frame for ID2. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame1_start_id1_inten Enable the interrupt of start of odd frame for ID1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame0_start_id1_inten Enable the interrupt of start of even frame for ID1. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame1_start_id0_inten Enable the interrupt of start of odd frame for ID0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame0_start_id0_inten Enable the interrupt of start of even frame for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_INTSTAT

Address: Operational Base(0xFF3E0000) + offset (0x0578)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame1_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
6	W1C	0x0	frame0_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame1_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame0_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame1_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame0_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame1_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame0_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI2_LINE_INT_NUM_ID0_1

Address: Operational Base(0xFF3E0000) + offset (0x057C)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 For one-time mode, if line_int_num_id1=100,then channel 1 receive 100th line, the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode, if line_int_num_id0=100,then channel 0 receive 100th line, the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

VICAP_MIPI2_LINE_INT_NUM_ID2_3

Address: Operational Base(0xFF3E0000) + offset (0x0580)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0040	line_int_num_id3 For one-time mode, if line_int_num_id3=100,then channel 3 receive 100th line, the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode, if line_int_num_id2=100,then channel 2 receive 100th line, the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI2_LINE_CNT_ID0_1

Address: Operational Base(0xFF3E0000) + offset (0x0584)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI2_LINE_CNT_ID2_3

Address: Operational Base(0xFF3E0000) + offset (0x0588)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	line_cnt_id2 Current line count for id2.

VICAP_MIPI2_ID0_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x058C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI2_ID1_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0590)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI2_ID2_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0594)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI2_ID3_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0598)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI2_FRAME_NUM_VC0

Address: Operational Base(0xFF3E0000) + offset (0x059C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI2_FRAME_NUM_VC1

Address: Operational Base(0xFF3E0000) + offset (0x05A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI2_FRAME_NUM_VC2

Address: Operational Base(0xFF3E0000) + offset (0x05A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI2_FRAME_NUM_VC3

Address: Operational Base(0xFF3E0000) + offset (0x05A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_MIPI2_ID0_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x05AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI2_ID1_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x05B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI2_ID2_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x05B4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI2_ID3_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x05B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

VICAP_MIPI2_ON_PAD_VALUE

Address: Operational Base(0xFF3E0000) + offset (0x05BC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI2_SIZE_NUM_ID0

Address: Operational Base(0xFF3E0000) + offset (0x05C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI2_SIZE_NUM_ID1

Address: Operational Base(0xFF3E0000) + offset (0x05C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

VICAP_MIPI2_SIZE_NUM_ID2

Address: Operational Base(0xFF3E0000) + offset (0x05C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI2_SIZE_NUM_ID3

Address: Operational Base(0xFF3E0000) + offset (0x05CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_MIPI3_ID0_CTRL0

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Address: Operational Base(0xFF3E0000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id0 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id0 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi0_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id0 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id0 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id0 Data type for id0.
9:8	RW	0x0	sw_vc_id0 Virtual channel for id0.

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id0 The parse type of id0. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_ID0_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI3_ID1_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id1 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id1 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).

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Bit	Attr	Reset Value	Description
28	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id1 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id1 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id1 Data type for id1.
9:8	RW	0x0	sw_vc_id1 Virtual channel for id1.
7:5	RW	0x0	sw_wrddr_type_id1 The write ddr type of id1. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:1	RW	0x0	sw_parse_type_id1 The parse type of id1. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_ID1_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI3_ID2_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id2 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id2 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode

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Bit	Attr	Reset Value	Description
25:24	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
19:18	RW	0x0	sw_yuyv_out_order_id2 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id2 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id2 Data type for id2.
9:8	RW	0x0	sw_vc_id2 Virtual channel for id2.
7:5	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id2 The parse type of id2. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

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VICAP_MIPI3_ID2_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

VICAP_MIPI3_ID3_CTRL0

Address: Operational Base(0xFF3E0000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_vc_hdr_id_main_id3 The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
29	RW	0x0	sw_vc_hdr_protect_id3 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
28	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
27	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
26	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
25:24	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.
23:22	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
21:20	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved

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Bit	Attr	Reset Value	Description
19:18	RW	0x0	sw_yuyv_out_order_id3 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuyv_in_order_id3 2'b00: UYVY(CSI-2 standard) 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15:10	RW	0x00	sw_dt_id3 Data type for id3.
9:8	RW	0x0	sw_vc_id3 Virtual channel for id3.
7:5	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
4	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
3:1	RW	0x0	sw_parse_type_id3 The parse type of id3. 3'b000: For raw8/rgb888 3'b001: For raw10 3'b010: For raw12 3'b011: For raw14(data will be clipped to 12bit) 3'b100: For yuv422 8bit progress 3'b101: For yuv422 8bit interlace Others: Reserved
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_ID3_CTRL1

Address: Operational Base(0xFF3E0000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. If data format is rgb888, then the width is equal to the number of bytes(not pixel). The width value must be 4 aligned when data format is raw8/raw10/raw12/raw14/yuv422 8bit, and must be 12 aligned when data format is rgb888.

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VICAP_MIPI3_CTRL

Address: Operational Base(0xFF3E0000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
29:24	RW	0x00	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
23:21	RW	0x0	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
20	RW	0x0	sw_drop_frame_en_all 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI0 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI0 path dma. When this bit change to 0,dma is reseted completely.
15:13	RW	0x0	sw_press_value Press value.
12	RW	0x0	sw_press_en 1'b0: Disable press 1'b1: Enable press
11	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.
10	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.
9	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
8	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.
7:5	RW	0x0	sw_hurry_value Hurry value.
4	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry
3	RO	0x0	reserved
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

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VICAP_MIPI3_FRAME0_ADDR_Y_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0624)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_Y_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0628)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_UV_ID0

Address: Operational Base(0xFF3E0000) + offset (0x062C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_UV_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI3_VLW_ID0

Address: Operational Base(0xFF3E0000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_Y_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0638)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_Y_ID1

Address: Operational Base(0xFF3E0000) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_UV_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0640)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_UV_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI3_VLW_ID1

Address: Operational Base(0xFF3E0000) + offset (0x0648)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_Y_ID2

Address: Operational Base(0xFF3E0000) + offset (0x064C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_Y_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0650)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_UV_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_UV_ID2

Address: Operational Base(0xFF3E0000) + offset (0x0658)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI3_VLW_ID2

Address: Operational Base(0xFF3E0000) + offset (0x065C)

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Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_Y_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_Y_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_UV_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0668)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_UV_ID3

Address: Operational Base(0xFF3E0000) + offset (0x066C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI3_VLW_ID3

Address: Operational Base(0xFF3E0000) + offset (0x0670)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI3_INTEN

Address: Operational Base(0xFF3E0000) + offset (0x0674)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame1_start_id3_inten Enable the interrupt of start of odd frame for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame0_start_id3_inten Enable the interrupt of start of even frame for ID3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame1_start_id2_inten Enable the interrupt of start of odd frame for ID2. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame0_start_id2_inten Enable the interrupt of start of even frame for ID2. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame1_start_id1_inten Enable the interrupt of start of odd frame for ID1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame0_start_id1_inten Enable the interrupt of start of even frame for ID1. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame1_start_id0_inten Enable the interrupt of start of odd frame for ID0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame0_start_id0_inten Enable the interrupt of start of even frame for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_INTSTAT

Address: Operational Base(0xFF3E0000) + offset (0x0678)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame1_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame0_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame1_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame0_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame1_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame0_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame1_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame0_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI3_LINE_INT_NUM_ID0_1

Address: Operational Base(0xFF3E0000) + offset (0x067C)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 For one-time mode,if line_int_num_id1=100,then channel 1 receive 100th line,the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode,if line_int_num_id0=100,then channel 0 receive 100th line,the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

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VICAP_MIPI3_LINE_INT_NUM_ID2_3

Address: Operational Base(0xFF3E0000) + offset (0x0680)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 For one-time mode, if line_int_num_id3=100,then channel 3 receive 100th line, the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode, if line_int_num_id2=100,then channel 2 receive 100th line, the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI3_LINE_CNT_ID0_1

Address: Operational Base(0xFF3E0000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI3_LINE_CNT_ID2_3

Address: Operational Base(0xFF3E0000) + offset (0x0688)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id2 Current line count for id2.

VICAP_MIPI3_ID0_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x068C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI3_ID1_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0690)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI3_ID2_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0694)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI3_ID3_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0698)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI3_FRAME_NUM_VC0

Address: Operational Base(0xFF3E0000) + offset (0x069C)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI3_FRAME_NUM_VC1

Address: Operational Base(0xFF3E0000) + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI3_FRAME_NUM_VC2

Address: Operational Base(0xFF3E0000) + offset (0x06A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI3_FRAME_NUM_VC3

Address: Operational Base(0xFF3E0000) + offset (0x06A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_MIPI3_ID0_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x06AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI3_ID1_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x06B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI3_ID2_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x06B4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI3_ID3_EFFECT_CODE

Address: Operational Base(0xFF3E0000) + offset (0x06B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

VICAP_MIPI3_ON_PAD_VALUE

Address: Operational Base(0xFF3E0000) + offset (0x06BC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI3_SIZE_NUM_ID0

Address: Operational Base(0xFF3E0000) + offset (0x06C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI3_SIZE_NUM_ID1

Address: Operational Base(0xFF3E0000) + offset (0x06C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

VICAP_MIPI3_SIZE_NUM_ID2

Address: Operational Base(0xFF3E0000) + offset (0x06C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI3_SIZE_NUM_ID3

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Address: Operational Base(0xFF3E0000) + offset (0x06CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_SCL_CH_CTRL

Address: Operational Base(0xFF3E0000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x00	sw_scl_mux_ch0 5'd0: Select MIPI0 ID0 5'd1: Select MIPI0 ID1 5'd2: Select MIPI0 ID2 5'd3: Select MIPI0 ID3 5'd4: Select MIPI1 ID0 5'd5: Select MIPI1 ID1 5'd6: Select MIPI1 ID2 5'd7: Select MIPI1 ID3 5'd8: Select MIPI2 ID0 5'd9: Select MIPI2 ID1 5'd10: Select MIPI2 ID2 5'd11: Select MIPI2 ID3 5'd12: Select MIPI3 ID0 5'd13: Select MIPI3 ID1 5'd14: Select MIPI3 ID2 5'd15: Select MIPI3 ID3 Others: Reserved
2:1	RW	0x0	sw_scl_mode_ch0 Scale mode for channel 0. 2'b00: 8 times scale 2'b01: 16 times scale 2'b10: 32 times scale Others: Reserved
0	RW	0x0	sw_scl_en_ch0 Enable scale channel0. 1'b0: Disable 1'b1: Enable

VICAP_SCL_CTRL

Address: Operational Base(0xFF3E0000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	sw_soft_rst_ch0 Write 1 will reset VICAP SCALE channel 0 path. When this bit change to 0,scale is reseted completely.
15:13	RW	0x0	sw_press_value Press value.
12	RW	0x0	sw_press_en 1'b0: Disable press 1'b1: Enable press
11:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_hurry_value Hurry value.
4	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry
3	RO	0x0	reserved
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
0	RO	0x0	reserved

VICAP_SCL_FRAME0_ADDR_CH0

Address: Operational Base(0xFF3E0000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_ch0 First address of even frame for CH0 path(must be aligned to double word).

VICAP_SCL_FRAME1_ADDR_CH0

Address: Operational Base(0xFF3E0000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_ch0 First address of odd frame for CH0 path(must be aligned to double word).

VICAP_SCL_VLW_CH0

Address: Operational Base(0xFF3E0000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_ch0 Address force update for ch0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_ch0 Virtual line width of even frame for CH0 path(must be aligned to double word).

VICAP_SCL_CH0_BLACK_LEVEL

Address: Operational Base(0xFF3E0000) + offset (0x0738)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_scl_ch0_black_11 The black level for scale channel0 bayer pattern 11 position.
23:16	RW	0x00	sw_scl_ch0_black_10 The black level for scale channel0 bayer pattern 10 position.
15:8	RW	0x00	sw_scl_ch0_black_01 The black level for scale channel0 bayer pattern 01 position.
7:0	RW	0x00	sw_scl_ch0_black_00 The black level for scale channel0 bayer pattern 00 position.

VICAP_TOISP0_CH_CTRL

Address: Operational Base(0xFF3E0000) + offset (0x0780)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:25	RW	0x0	sw_toisp0_vc_hdr_ch_main Toisp0 vc hdr main channel.
24	RW	0x0	sw_toisp0_vc_hdr_protect Enable toisp0 vc hdr protect. 1'b0: Disable 1'b1: Enable
23:19	RW	0x00	sw_toisp0_mux_ch2 5'd0: Select MIPI0 ID0 5'd1: Select MIPI0 ID1 5'd2: Select MIPI0 ID2 5'd3: Select MIPI0 ID3 5'd4: Select MIPI1 ID0 5'd5: Select MIPI1 ID1 5'd6: Select MIPI1 ID2 5'd7: Select MIPI1 ID3 5'd8: Select MIPI2 ID0 5'd9: Select MIPI2 ID1 5'd10: Select MIPI2 ID2 5'd11: Select MIPI2 ID3 5'd12: Select MIPI3 ID0 5'd13: Select MIPI3 ID1 5'd14: Select MIPI3 ID2 5'd15: Select MIPI3 ID3 Others: Reserved
18:17	RO	0x0	reserved
16	RW	0x0	sw_toisp0_en_ch2 Enable toisp0 channel2. 1'b0: Disable 1'b1: Enable
15:11	RW	0x00	sw_toisp0_mux_ch1 5'd0: Select MIPI0 ID0 5'd1: Select MIPI0 ID1 5'd2: Select MIPI0 ID2 5'd3: Select MIPI0 ID3 5'd4: Select MIPI1 ID0 5'd5: Select MIPI1 ID1 5'd6: Select MIPI1 ID2 5'd7: Select MIPI1 ID3 5'd8: Select MIPI2 ID0 5'd9: Select MIPI2 ID1 5'd10: Select MIPI2 ID2 5'd11: Select MIPI2 ID3 5'd12: Select MIPI3 ID0 5'd13: Select MIPI3 ID1 5'd14: Select MIPI3 ID2 5'd15: Select MIPI3 ID3 Others: Reserved
10:9	RO	0x0	reserved
8	RW	0x0	sw_toisp0_en_ch1 Enable toisp0 channel1. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
7:3	RW	0x00	sw_toisp0_mux_ch0 5'd0: Select MIPI0 ID0 5'd1: Select MIPI0 ID1 5'd2: Select MIPI0 ID2 5'd3: Select MIPI0 ID3 5'd4: Select MIPI1 ID0 5'd5: Select MIPI1 ID1 5'd6: Select MIPI1 ID2 5'd7: Select MIPI1 ID3 5'd8: Select MIPI2 ID0 5'd9: Select MIPI2 ID1 5'd10: Select MIPI2 ID2 5'd11: Select MIPI2 ID3 5'd12: Select MIPI3 ID0 5'd13: Select MIPI3 ID1 5'd14: Select MIPI3 ID2 5'd15: Select MIPI3 ID3 Others: Reserved
2:1	RO	0x0	reserved
0	RW	0x0	sw_toisp0_en_ch0 Enable toisp0 channel0. 1'b0: Disable 1'b1: Enable

VICAP_TOISP0_CROP_SIZE

Address: Operational Base(0xFF3E0000) + offset (0x0784)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height The expected height of received image.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width The expected width of received image.

VICAP_TOISP0_CROP_START

Address: Operational Base(0xFF3E0000) + offset (0x0788)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y The vertical ordinate of the start point.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x The horizontal ordinate of the start point.

VICAP_MMU0_DTE_ADDR

Address: Operational Base(0xFF3E0000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page table address.

VICAP_MMU0_STATUS

Address: Operational Base(0xFF3E0000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:6	RW	0x00	page_fault_bus_id Index of master reponsible for last page fault.
5	RW	0x0	page_fault_is_write The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RW	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RW	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command.
0	RW	0x0	paging_enabled Paging is enabled.

VICAP_MMU0_COMMAND

Address: Operational Base(0xFF3E0000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE

VICAP_MMU0_PAGE_FAULT_ADDR

Address: Operational Base(0xFF3E0000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

VICAP_MMU0_ZAP_ONE_LINE

Address: Operational Base(0xFF3E0000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

VICAP_MMU0_INT_RAWSTAT

Address: Operational Base(0xFF3E0000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

VICAP_MMU0_INT_CLEAR

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Address: Operational Base(0xFF3E0000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

VICAP_MMU0_INT_MASK

Address: Operational Base(0xFF3E0000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

VICAP_MMU0_INT_STATUS

Address: Operational Base(0xFF3E0000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

VICAP_MMU0_AUTO_GATING

Address: Operational Base(0xFF3E0000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self

1.5 Application Notes

1.5.1 MIPI Interface

- The register sw_crop_en is suggested to be set to 1. The register sw_width/sw_start_x should be aligned to 4.
- In the sony identification code hdr mode, the register sw_sony_effect_code0/1 should be configured correctly according to the camera manual.
- In the line counter hdr mode, the register sw_on_pad_value should be configured correctly according to the camera manual.
- In the VC hdr mode, the register sw_vc_hdr_protect is suggested to be set to 1, and the register sw_vc_hdr_id_main should be configured as the first coming id that is the long exposure frame id.
- The register sw_cap_en_idx is recommended for static configuration, and the register sw_cap_en is recommended for dynamic configuration.
- The MIPI interface can receive DSI data, but there are following restrictions on DSI TX: (1) one row of data could not be split into multiple long packets; (2) multiple packets could not be concatenated within a single HS transmission.

1.5.2 Scale down

- The register sw_scl_chx_black_00/01/10/11 is the black level value for bayer pattern 00/01/10/11 position.
- The bit width of scale down output data is 16. When the max bit width of the scale down output data exceed 16, output data will be clipped. For example, 8 times scale down for RAW12, the bit width is 18, then the result will be clipped to 16 bits.

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- When the width is not a multiple of double scale down times, then the result will be rounded up to an integer. For example, the image width is 4656 and 32 times scaling down is performed, the result width equals to (ceil(4656/64)*64)/32.
- When the height is not a multiple of double scale down times, then the result will be rounded down to an integer. For example, the image height is 1080 and 8 times scaling down is performed, the result height equals to (floor(1080/16)*16)/8.

1.5.3 TOISP

- The register sw_width/sw_start_x should be aligned to 4.
- Although there are three channels to ISP, user just need enable channel 0 and select the short exposure frame id.

1.5.4 DMA

- The start address/virtual stride should be aligned to 8 at least. And being aligned to 64 is good for DDR.
- User could shut down DMA transferring by setting the register sw_dma_en to 0.
- User could set sw_hurry_en/sw_press_en to 1 for dynamic adjusting the priority of VICAP. And the register sw_water_line is the triggering condition of pulling up hurry/press signal.
- The register sw_yuyv_out_order is effective when the register sw_wrddr_type is NV16/NV12/YUYV. And in the NV16/NV12 case, 2'h0/2'h2 are the same for UV sequence and 2'h1/2'h3 are the same for VU sequence.
- There are two modes for line counter interrupt.In one-time mode, if line_int_num =100, the line_intst will be 1 when receive 100th line. In circular mode, if line_int_num =100, the line_intst will be 1 when receive 100th line200th line300th line.....
- The DMA has two transfer strategies :1. transfer image according to the actual height of reception. 2. transfer image according to the configured height. Which strategy you choose depends the register sw_dma_adapt_en.

1.5.5 Reset

- DMA will be auto-reset when DMA goes wrong, for example fifo overflow. And DMA will transfer data from the next frame.
- DMA also could be soft-reset by the register sw_dma_rst.
- User could reset the entire data path (interface/dma) by setting the register sw_soft_rst to 1. And the scale/toisp module will be reset if the sw_scl_mux/sw_toisp_mux is setted to choose the path.

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Chapter 2 IMAGE SIGNAL PROCESSING (ISP)

2.1 Introduction

2.1.1 Overview

The Image Signal Processing (ISP) is a complete video and still picture input unit which contains standard sensor picture data processing functions, such as image processing, scaling. This unit supports image sensors with integrated YCbCr processing and also simple CMOS sensors delivering RGB Bayer pattern without any integrated image processing. Image processing contains many functions, such as HDR_MGE, HDR_DRC, BAY3DNR, DEBAYER and so on. Scaling is used for downsizing the sensor data for displaying them on the screen, and also can be used for digital zoom effects, because scaling is capable of up-scaling as well. The camera interface provides parallel data and MIPI support, so that ISP can be connected to PHY devices or IP blocks directly. All data is transmitted via the memory interface (MI) to a AXI bus system using a bus master interface. Programming is done by register read/write transactions using an AHB slave interface.

ISP supports the following features:

- VICAP input: RX raw8/raw10/raw12
- Maximum input: 4224x3136 (width no more than 4224), throughput 13M @30fps
- Minimum input: 256x256
- 3A: Include Auto Enhance (AE)/Histogram, Auto Focus (AF), and Auto White Balance (AWB) statistics output
- BLC: Black Level Correction
- DPCC: Static/Dynamic Defect Pixel Cluster Correction
- PDAF: Phase Detection Auto Focus
- LSC: Lens Shading Correction
- Bayer-3DNR: Temporal Bayer-raw Noise Reduction
- HDR-MGE: 2-Frame Merge into High-Dynamic Range
- HDR-DRC: HDR Dynamic Range Compression, Tone mapping
- DeBayer: Advanced Adaptive Demosaic
- CCM/CSM: Color Correction Matrix, RGB2YUV, etc.
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and effect enhancement
- 3DLUT: 3D-LUT Color Palette for Customer
- LDCH: Lens Distortion Correction only in the Horizontal direction
- YUV-2DNR: Spatial YUV Noise Reduction
- Sharp: Image sharpening and boundary filtering
- Gain: Image local gain
- Multi-sensor reuse ISP, 4 sensors for maximum
- Bus interface: 32bit AHB configuration, 128bit AXI R/W
- Low power, auto-gating for each block
- MI R/W burst group to improve memory utilization
- MI 2 paths output, MP stepless scaling, SP 1080p (width no more than 1920) scaling

2.1.2 Using constrains

1. Sensor's hblank time is not less than 1% of each row time, or not less than 16 cycles (working clock). The vblank time does not exceed 40% of one frame time. And the vblank time is recommended to be no less than 136 rows time.
2. The YNR, CNR and SHARP should be on or off at the same time. YNR and SHARP has its own bypass control. If you want to bypass a module, you can turn on its bypass of the module. The bypass signal of YNR includes sw_ynr_bft3x3_bypass, sw_ynr_lbft5x5_bypass, sw_ynr_lgft3x3_bypass, sw_ynr_flt1x1_bypass, sw_ynr_sft5x5_bypass, and sw_ynr_flt1x1_bypass_sel. The bypass control of SHARP includes sw_sharp_bypass. CNR does NOT support bypass, which is the critical path in ISP. When CNR is disabled, all the data of these modules are bypass.
3. The enable of gain and the enable of module must be switched on and off together in normal mode. If sw_gain_module_free_mode (address offset 0x3f00[6]) is enabled,

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the enable of gain and the enable of module can be controlled separately, which is not recommend.

4. The input image width of BAY3D must be 16pixel aligned. BAY3D has a bandwidth saving control in no-HDR mode, corresponding register is sw_bay3d_bwsaving_en (address offset 0x2c00[13], defaults to 0), which is not available in HDR mode. Bandwidth saving is disable by default, which is recommended for developers to enable it. More application notes of BAY3D module are shown in Session 1.5 in detail.
5. MI burst group is the new upgraded features, supports 1~2 burst available which is more friendly to DDR.
6. The address offset of MMU configuration is 0x7f00.
7. For HDR on-the-fly mode, sw_ibuf_hold_watermark (address offset 0x1c0c[15:0]) is used to hold DDR read to control read rate.
8. LDCH module will adaptively consider that the table consists of an integer of 13 bits and a decimal of 3 bits when the width of table is bigger than 4080. If developers still want to use the table composed of integer of 12 bits and decimal of 4 bits, sw_ldch_force_map_en (address offset 0x3b00[6]) must be configured to 1 and sw_ldch_map13p3_en (address offset 0x3b00[7]) must be configured to 0, and ensure that the right boundary of table cannot exceed an integer of 12 bits (i.e., 4095).
9. Support the image resolution with width 4pixel alignment and height 4pixel alignment. The minimum input image resolution is 256x256.
10. After all configurations of ISP are completed, configure MI force update, and finally start MI readback.
11. It is recommended that GAIN module is always on to improve the image effect. It is not recommended to switch GAIN dynamically, unless the ISP data stream is transmitted completely.
12. ISP MI write supports output image vertical flip. Vertical flip operation is configured to each path independently. When vertical flip is enabled, the corresponding write virtual width register and write size register should NOT be configured to 0.
13. ISP self path (SP) supports ARGB8888/RGB888/RGB565 output format. When SP vertical flip is enabled with RGB output format, the output image width must be 4pixel aligned for ARGB8888 and 8pixel aligned for RGB565.
14. MI wrap and ISP2ENC refer to Session 1.5 in detail.
15. CNR module must be enabled when frame buffer to DDR is enabled, and the start signal of frame buffer DDR read is reused with AXI configuration, which means that when frame buffer DDR read is enabled, the AXI configuration must be enabled too. If developer only need frame buffer to DDR function, just configure some unimportant registers (such as address register) by AXI.

2.2 Block Diagram

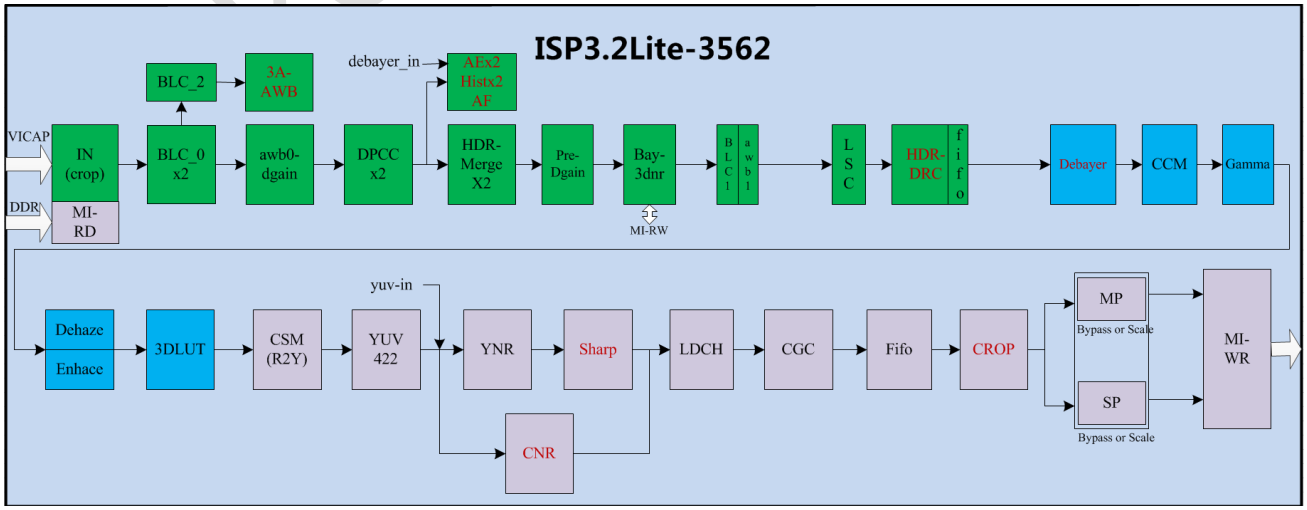

Fig.2-1 ISP Block Diagram

ISP is comprised of:

- VICAP Direct Interface

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- RAW Processing
- RGB Processing
- YUV Processing
- Memory Interface (MI)

4 channels of data of RXPHY input to VICAP and one channel can directly input to ISP to make a direct connection between HDR on the fly and no-HDR.

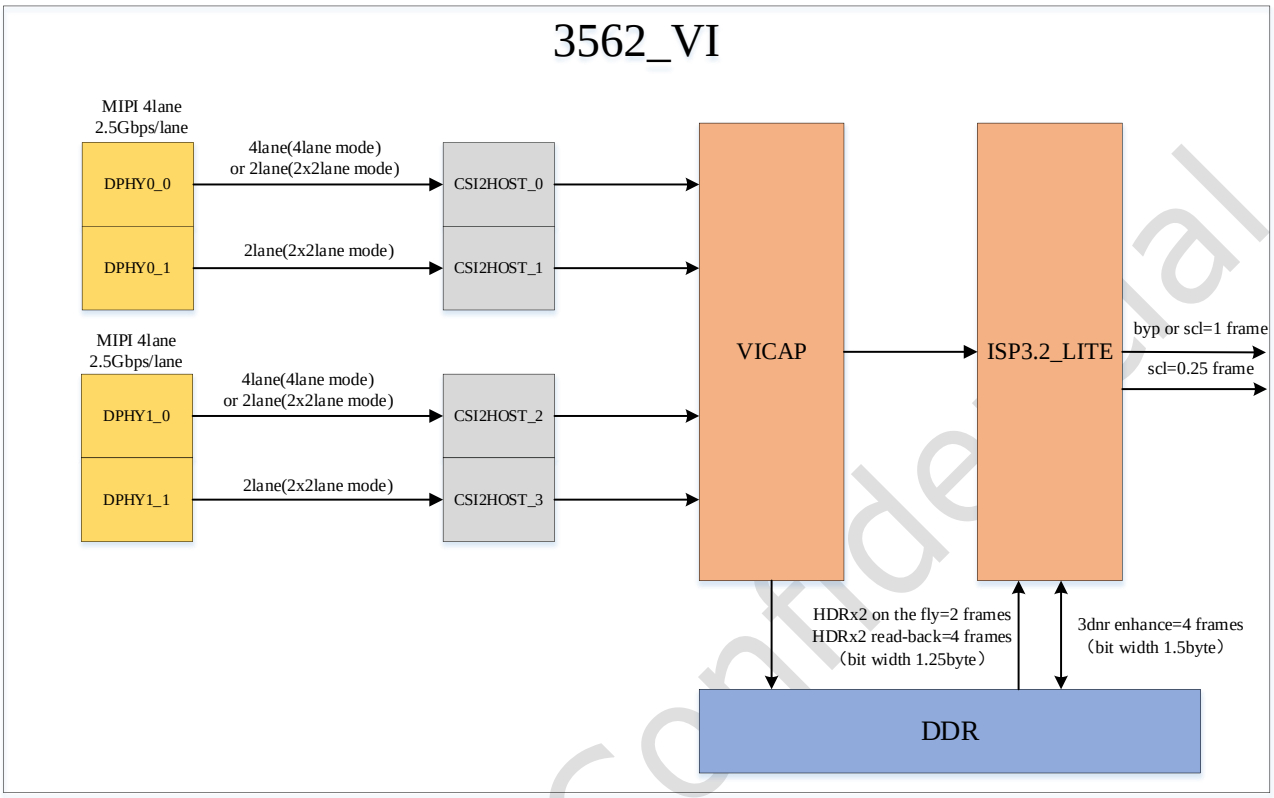

Fig.2-2 ISP data flow

2.3 Function Description

2.3.1 CSI2RX (MIPI)

1. Overview

The raw data come from VICAP or MI.

2. Features

- Support HDR stream: frame mode, line mode
- Support MIPI raw read back framex1, framex2

2.3.1.1 Block Descriptions

Raw-picture into DDR support un-compact and compact (including swap) mode:

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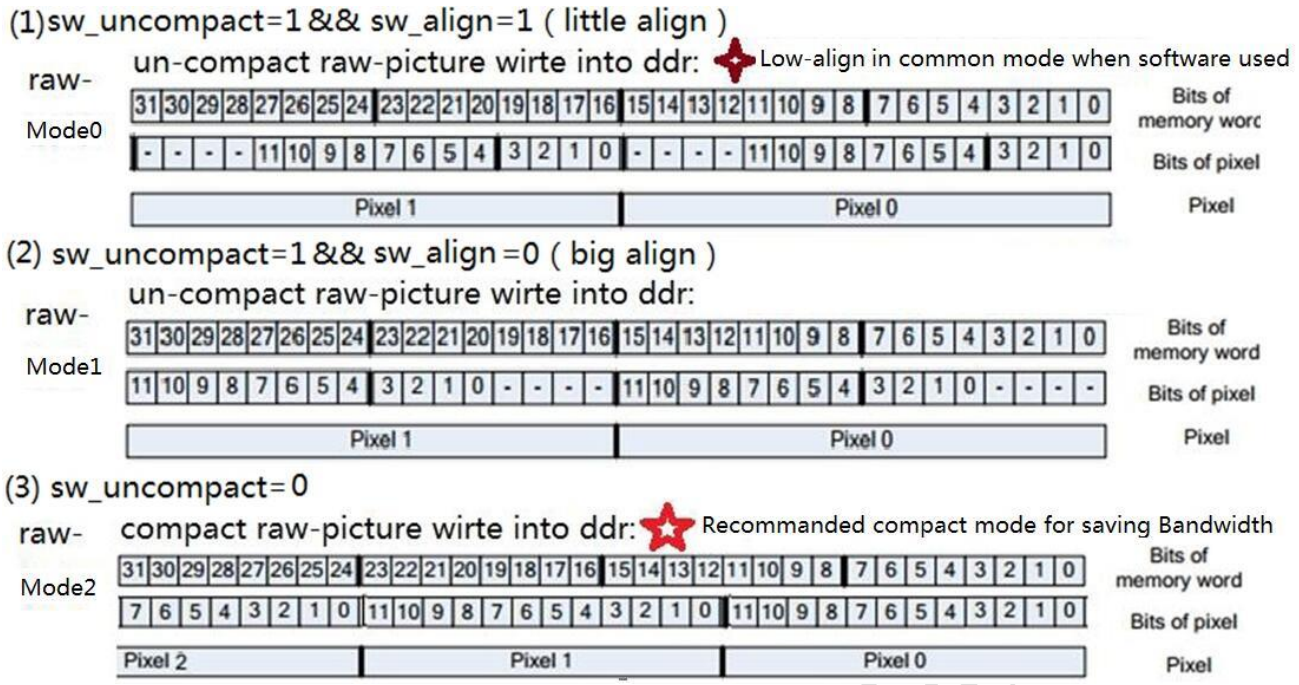

Fig.2-3 Un-compact and Compact (including swap) Mode

The function mode of CSI2RX depend on the configuration of sw_ibuf_op_mode, which are shown in the following table.

Table 2-1 CSI2RX Function Mode

Sw_ibuf_op_mode	Function	Interval mode	HDR mode	Need DDR
0	normal	NA	N	N
4	raw_rdback_framex1	NA	N	Y
5	raw_rdback_framex2	frame/line	Y	Y
8	frame_line_x2_ddr	frame/line	Y	Y

(1) frame_line_x2_ddr mode (2IDs--HDR mode)

The 2IDs inter frame mode or inter line mode has L-data and S-data. VICAP will transfer L-data to DDR and output S-data to ISP. Then ISP will read back L-data when S-data arrives ISP.

(2) raw_rdback_framex2 mode (2IDs--HDR mode)

The difference between frame_line_x2_ddr mode and raw_rdback_framex2 mode is that S-data also needs to go in and out of DDR. S-data is output from VICAP to DDR. Then S-data is read back through channel DMARX2 (DMARXS). The time to start read back is up to the user. Start once, read back one frame of L-data, M-data.

(3) raw_rdback_framex1 mode

Under raw_rdback_framex1 mode, S-data is processed by VICAP and output from VICAP to DDR. Then S-data is read back through channel DMARX2 (DMARXS). The time to start DMARXS is up to the user. Start once, read back one frame of S-data.

(4) normal mode (Single ID--linear mode)

The single ID mode is the normal sensor mode. The single ID data is input to CSI2HOST through D-PHY interface. CSI2HOST decodes the PPI stream data of D-PHY, then output to VICAP. VICAP parse the CSI2HOST output data to pixel and output to ISP.

2.3.2 Memory Interface (MI)

The memory interface unit (MI) is responsible for reading/writing image data from/to the system memory (DDR). The MI has six main tasks, which can operate independently:

- Take image data from the main path, either in YCbCr or RAW format, and write it into DDR.
- Take image data from MIPI module, and take it back from the DDR to MIPI module.
- Take image data from DBR module, and take it back from the DDR to DBR module.
- Take image data of LUT data from the DDR to 3D_LUT/LDCH/LSC module.

Memory Interface is as following:

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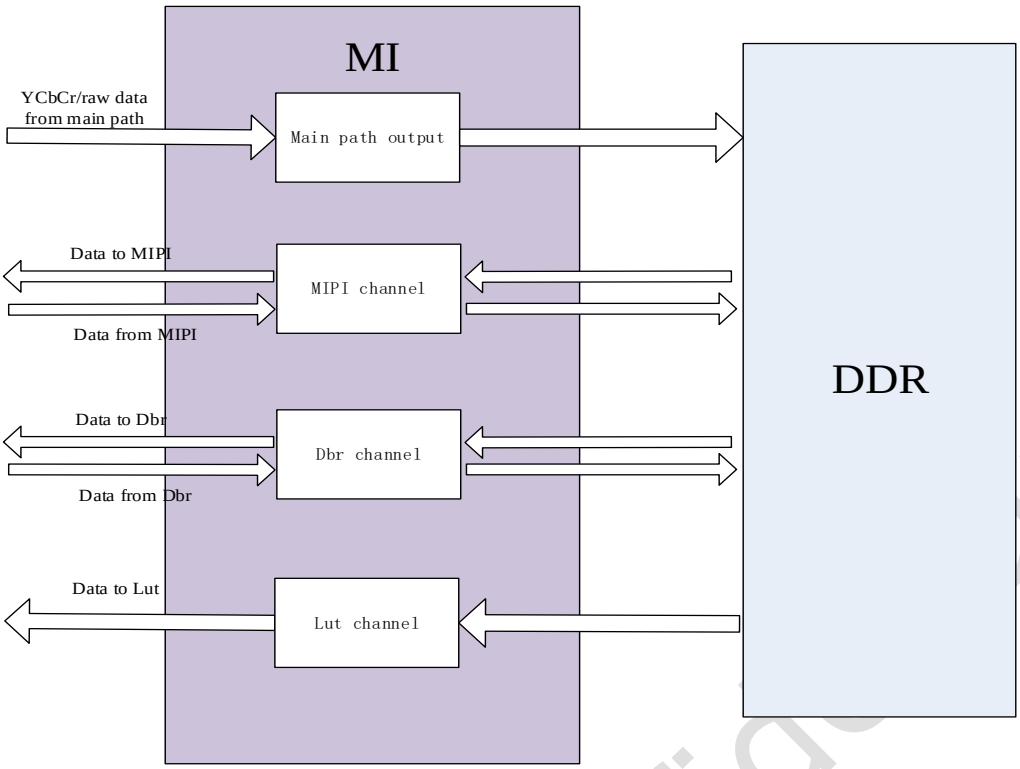

Fig.2-4 Memory Interface

The following registers need to be configured to use different channels:

(1) Main path

The registers need to be configured are as follows (xx means Y, CB and CR):

- MI_MP_WR_xx_BASE

This is the base address of the memory area to use for that buffer.

This register protects from non-aligned access. The bits 0 to 2 are hard wired to 3'b000. As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64bit aligned address: *write(MI_MP_WR_xx_BASE, address_value)* is equivalent to *write(MI_MP_WR_xx_BASE, address_value & 0xFFFFFFF8)*.

Anyhow, in order to avoid confusion, it is not recommended to use non-aligned address values for access. It is also not recommended to actively consider the register slice for register access in order to avoid unnecessary mask and shift operations.

In addition, the programmed base address shall be burst aligned with respect to the burst length configured in MI_WR_CTRL.

Set control bit init_base_en before updating so that a forced or automatic update can take effect.

- MI_MP_WR_xx_SIZE

Size of main picture ring buffer or raw data ring buffer.

Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configure update.

Set control bit init_base_en before updating so that a forced or automatic update can take effect.

Note: This register protects from non-aligned access.

- MI_MP_xx_OFFS_CNT_INIT

This is the initial offset (in bytes) for writing to the buffer after e.g., a soft reset. Usually, to write to the buffer from the very beginning, an offset of zero is to be programmed into this register.

- MI_MP_xx_OFFS_CNT_START

This is a read-only register, which holds the offset at which the MI had written the last processed frame. This register is updated at frame end, so at any given time, it contains always the starting offset of the last completely processed frame.

- MI_WR_CTRL

This register is a global write control register of main path, include path_enable, wr_format and so on. Refer to MI_WR_CTRL register description for details.

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(2) MIPI/DBR/LUT channel

The registers need to be configured are as follows (xx include RAW0~RAW1, LUT and DBR):

- xx_WR_BASE

DDR write base address, similar to MI_SP_WR_xx_BASE. Refer to register description for details.

- xx_WR_SIZE

DDR write size, similar to MI_SP_WR_xx_SIZE. Refer to register description for details.

- xx_WR_LENGHT

Line length of DDR write in pixel, also known as line stride. If no line stride is used, line length must match image width. For example, raw8 mode must be a multiple of 8.

- xx_RD_BASE

Image read start address.

- xx_RD_LENGTH

Line length of DDR read in pixel, also known as line stride.

- MI_WR_CTRL2

This register is a global write control register of MIPI/DBR/LUT channel. Refer to register description for details.

- MI_RD_CTRL2

This register is a control register of MIPI/DBR/LUT channel, refer to MI_WR_CTRL register description for details.

2.3.3 ISP_CORE

2.3.3.1 INFORM

The input formatter module is responsible for sampling data from the sensor device and providing it to the other blocks in the processing pipelines.

2.3.3.2 OUTFORM

At the output of the ISP sub-module the image data may be cropped a third time.
The following figure illustrates the different possible regions which can be defined by register settings. Some of these regions may have the same size and offset (settings), if a differentiation is not needed.

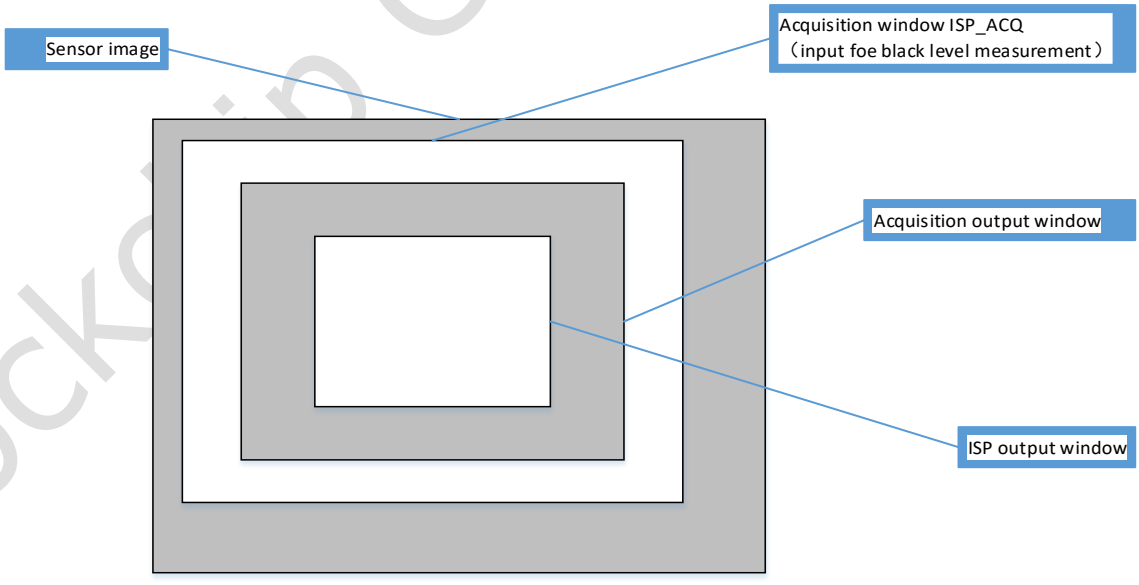

Fig.2-5 Possible cropping regions of ISP

2.3.3.3 BLC

Black Level Correction (BLC) module is a function to subtract a DC offset from picture data. A CMOS sensor always has a so-called black level shift. So that pixels with no light on them will not read out the value zero. This value varies with different setting for the exposure. This black level can easily be detected by special pixels on the sensor that are permanently covered, i.e., they are always black.
BLC module reads out the values of these pixels, calculates their mean value and then subtracts these values from all pixels that represent the picture frame (in automatic mode).

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2.3.3.4 GAMMA_IN

GAMMA_IN module is used to adapt the image signal processing to the characteristics of the attached sensor device.

There are three gamma curves can be defined, one for each color component red, green and blue.

2.3.3.5 DPCC

Static/Dynamic Defect Pixel Cluster Correction (DPCC) module is used to correct the defect pixels of the sensor, and supports both static and dynamic DPCC. DPCC module supports detection and correction of single pixels and small cluster defects (up to 3x3 pixels). It detects and corrects single pixels and small cluster defects on raw Bayer image data. An integrated defect pixel table allows the correction of up to 2048 fix positions independently from the on-the-fly detection.

2.3.3.6 HDR

High Dynamic Range (HDR) refers to the high ratio of brightest value and darkest value contained in an image, that is, the number of levels of gray scale division between brightest and darkest is big. The larger the dynamic range, the richer the level of representation and the wider the color space.

Dynamic range calculation formula: dynamic_range = 20log(MaxIntensity / MinIntensity), where MaxIntensity means maximum brightness value, MinIntensity means minimum brightness value. 3562 HDR*2 support 20bit, the dynamic range is 120dB.

HDR unit is composed of both HDR-MGE module and HDR-DRC. HDR-MGE realizes the function of two frames synthesizing one frame. HDR-DRC realizes wide dynamic compression.

2.3.3.7 BAY3D

Bayer-3DNR (BAY3D for short) module mainly realizes advanced temporal noise reduction of image in raw format. Motion detection in high and low frequency domain, Kalman filter is applied to reduce high frequency and low frequency noise, image edges and details are preserved at the same time.

2.3.3.8 LSC

Lens Shade Correction (LSC) is designed to deal the problems of lens shading and vignette. It is done during input data processing: If the lens shading correction is enabled, each pixel is processed and corrected according to the stored settings. LSC is done by multiplying each input pixel with its respective correction value. Only the correction factors at predefined sector corners as well as the sector positions are stored. The pixel position specific correction values are calculated using bilinear interpolation. The correction factors at the sector corners are calculated during a calibration process which uses one or more reference frames which have to be captured under dedicated light conditions and at a dedicated position of the sensor. The captured frames are evaluated by software and the calculated parameters for LSC are stored in multiple illumination specific tables e.g., in external memory or on a flash device. The software controls LSC process by loading or updating the correct tables into the hardware module.

It is also possible to use different LSC parameters for different environment conditions, e.g., lightness, light direction or sensor position.

2.3.3.9 DEBAYER

The DEBAYER module outputs RGB data after interpolation and filtering operation of the input Bayer data. The filtering operation can be bypassed by software configuration, and DEBAYER module can also output three RGB components of the same value in black-and-white mode.

2.3.3.10 CCM

Color Correct Matrix (CCM) is used to correct the color crosstalk because of three channels response of sensor when only one channel color input. For example, when the sensor input is red, the other two channels GB not only R is also response too. CCM is working to reduce this crosstalk to make color brighter in color. The adjustment factor is added to adjust CCM working strength. The factor is works at dark range and bright range, which are symmetry.

2.3.3.11 GAMMA_OUT

Because the human eye's perception of natural brightness is non-linear, the dynamic range

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and gray-scale budget of the medium we use to record and display the picture are limited. In this premise, gamma is produced which is the mapping relationship between the natural brightness and the subjective gray-scale experience.

2.3.3.12 DEHAZE_ENHANCE

Dehaze: The process of dehaze is that the input pixel first goes through the dark channel defogging treatment, then goes through a histogram equalization module, and finally outputs the defogging results. In addition, a dehaze gain is also output to guide the noise reduction module. The module supports two modes of parameter adaptation and parameter external configuration. The parameters of the adaptive mode are calculated by the module itself, without external intervention, and the adaptive parameters are conservative.
Enhance: Dehaze algorithm can't enhance the image effect at night, so an enhance enable is added. When the enable is turned on, it can enhance the image at night.

2.3.3.13 3DLUT

3D Look up Table (3DLUT) is a technical means of color calibration. Because the 3DLUT has RGB channels for each coordinate direction, the biggest advantage of 3DLUT in color calibration can affect both gamut, color temperature and gamma, which 1DLUT, 2DLUT or matrix can't be achieved, and more accurate than traditional matrix calibration methods. In addition, the 3DLUT can map and process all color information, whether it is a color that exists or does not exist, or a color gamut that cannot be reached by film.

2.3.3.14 LDCH

LDCH module achieves distortion correction in horizontal direction under fisheye lens.
LDCH module needs to take table from DDR through MI unit. When the resolution is small, it is recommended that the MI burst length configuration of images should be greater than the width of table, otherwise, the fetching will hang.
https://fanyi.baidu.com/?aldtype=16047 - zh/en/javascript:void(0);

2.3.3.15 YUV-2DNR

YUV-2DNR consists of two modules, YNR and CNR. YNR is used to reduce the noise of Y component, and CNR is used to reduce the color noise.
YUV-2DNR supports the following features:
Support the independent configuration of Y component and UV component denoising intensity.
Support the independent configuration of high-frequency and low-frequency noise suppression.

2.3.3.16 SHARP

SHARP includes two functions: image sharpening and boundary filtering. sharpening can sharpen the intermediate frequency and high frequency respectively. Boundary filtering is to do another level of filtering on the sharpening results, remove the boundary burrs, and finally add a level of general sharpening to supplement the image details.
SHARP supports the following features:
Support image sharpening and boundary filtering
Support sharpening of medium-low frequency and high frequency respectively
Support adaptive filtering and specified coefficient filtering
Support detail enhancement

2.3.3.17 GAIN

GAIN is used to adjust the local gain of image, and guide the noise reduction of YNR and CNR.

2.3.3.18 CSM

CSM module realizes data conversion from RGB to YUV format.

2.3.3.19 CONV422

CONV422 module change YUV444 format data to YUV422 format.

2.3.3.20 SCL-RESIZE

The resize modules get pictures in YCbCr 4:2:2 format, and scale them by an arbitrary factor up or down to a new format. See following figure for a module overview:

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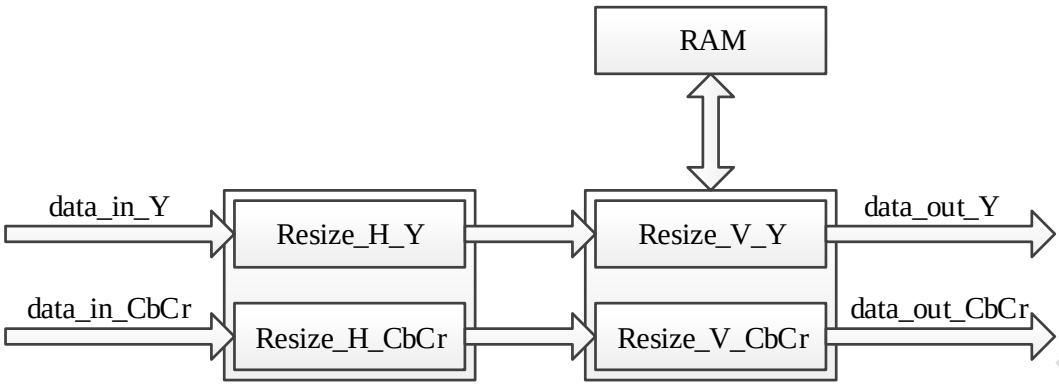


Fig.2-6 Block Diagram of the Resize Module

The resize module is configurable for horizontal and vertical up- or down-scaling. Discrete values for the scaling factors of the luminance and the two chrominance components allow conversion between YUV4:2:2 and YUV4:2:0 color format and support of uneven line width.

Phase shift registers are provided to shift the output pixel positions with respect to the input pixel positions. For example, this allows format conversion between cosited and non-cosited color schemes.

In sensor mode this module supports only down-scaling because of the sensor cannot be stopped from delivering data during one frame.

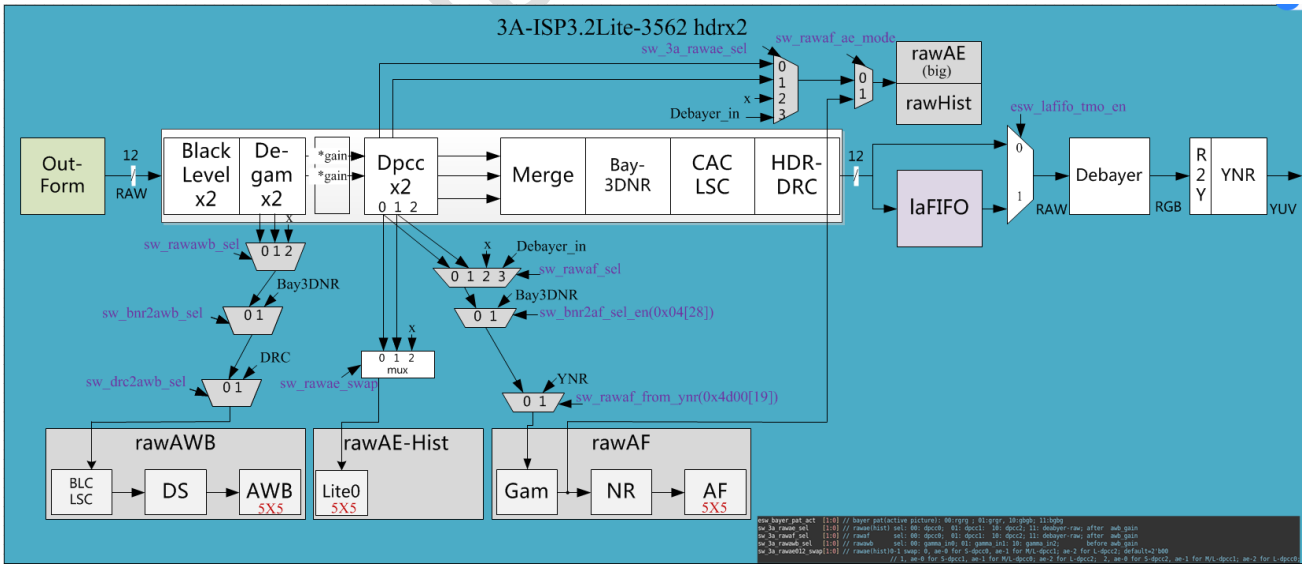
The resize module is able to process luminance and chrominance data independently, i.e., there are separate pipelines for luminance and chrominance processing using dedicated scale factors and phase offsets. This allows format conversion to be done (YCbCr 4:2:2 to 4:2:0, 4:1:1, 4:1:0).

2.3.3.21 FLASH_LIGHT

The sensor interface supports triggering of a LED or tube flash light. To control a flash light device, the flash light output and the prelight output can be used. A trigger event could active both the flash light and the prelight. This event may either be a positive or negative edge from the camera or a positive edge from any other trigger source at the input port 'vds_vsync'.

Programming respective configuration register can determine the signal polarity, flash delay time and flash light time.

2.3.4 3A



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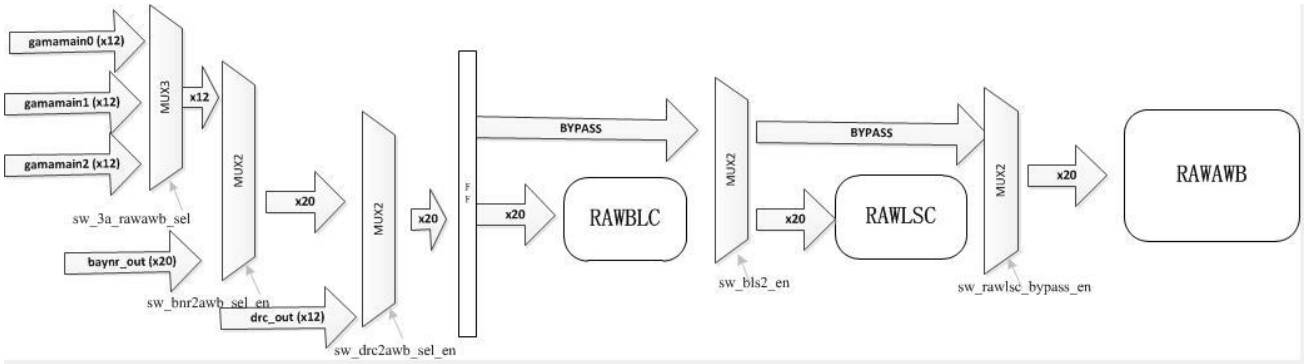

Fig.2-7 3A-ISP3.2 lite

2.3.4.1 AF

AF realizes the function of Auto Focus. The main part of AF control will be completed in the software: the search algorithm for the maximum definition in the image will be realized in the software, and the motion of the lens will be controlled by the software. The hardware AF module mainly realizes the measurement of image definition by configuring the configuration register. Filtering and gamma are added to facilitate the dark field processing. It supports a 5x5 size window and a separate window. Because its input data format is raw, AF here is named RAWAF.

2.3.4.2 AE

AE realizes the function of Auto Exposure. The input source is raw format. Two versions of AE are used here named RAWAE_BIG and RAWAE_LITE here. There are two AE modules here, one is RAWAE_BIG and the other is RAWAE_LITE. The difference between RAWAE_BIG and RAWAE_LITE is that RAWAE_BIG supports 15x15 statistics window while RAWAE_LITE supports 5x5 statistics window.

2.3.4.3 AWB

AWB module provides Auto White Balance function, and configures the gains of the R, Gr, Gb and B components. Because its input data format is raw, AWB here is named RAWAWB. RAWAWB has 3 engines for finding valid white points (XY UV and 3DYUV domain).
It supports a 5x5 size window for white points or all points. It accumulates R, G, B channel data of all white points in XY domain for small normal and big window and for 7 source lights.

2.3.4.4 HIST

Histogram (HIST) counts the number of pixels with the same or similar values. In general, a histogram is a graphical representation of the pattern of change that exists in the intensity value of a color or luminance plane. It is often shown as a vertical bar chart to indicate the frequency level of data collected over a specific range. The measurement can be used in different applications. The common application is to display the information of the end user, or to improve the exposure control and so on.
Two versions of HIST are named RAWHIST_BIG and RAWHIST_LITE here. Each AE follows a HIST, RAWAE_BIG follows RAWHIST_BIG (256bin), RAWAE_LITE follows RAWHIST_LITE (64bin). The difference between RAWHIST_BIG and RAWHIST_LITE is same with AE.

2.3.4.5 PDAF

Phase Detection Auto Focus (PDAF) module here replaces the PDAF points inside the raw input data with corresponding 3x3 median data.

2.4 Register Description

The ISP uses a distributed configuration register scheme, so there is no central unit containing all programming registers, but all sub-modules contain their own programming registers. An address space is reserved for each sub-module inside the total ISP controller.

Table 2-2 ISP module base address

Module	Description	Offset Address
BLS	Black level subtraction	0X3000
DPCC	Defect pixel cluster correction	0X3400
HDRMGE	High dynamic range merge	0X3800

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Module	Description	Offset Address
BAY3D	Temporal noise reduction in raw space	0X2C00
LSC	Lens shade correction	0X2200
HDRTMO	High dynamic range tone mapping	0X3900
DEBAYER	DeBayer	0X2500
CCM	Color correct matrix	0X0700
GAMMA_OUT	Gamma out	0X0900
2DNR-YNR	Filter the noise of Y component	0X2700
2DNR-CNR	Filter the noise of C component	0X2800
SHARP	Image sharpening and boundary filtering	0X2900
LDCH	Lens distortion correction in horizontal	0X3B00
DHAZ	Dehaze	0X3C00
3DLUT	3D look up table	0X3E00
GAIN	Image local gain	0X3F00
SELF_RESIZE	Main resize	0X0C00
	Scale self-resize	0X1000
ISP_CORE	ISP top module	0X0400
FLASH	ISP flash light	0X0660
SHUTTER	ISP mechanical shutter	0X0680
CTRL	Marvin top control	0X0000
RAWAF	Auto focus measurement	0X4D00
RAWAE_LITE	Auto exposure lite version	0X4500
RAWAE_BIG	Auto exposure big version	0X4400,0X4600,0X4700
RAWAWB	Auto white balancing	0X5000
RAWHIST_LITE	Histogram calculation lite	0X4900
RAWHIST_BIG	Histogram calculation big	0X4800,0X4A00,0X4B00

2.4.1 Registers Summary

2.4.1.1 MIPI

Name	Offset	Size	Reset Value	Description
CSI2RX_1C00_CTRL0	0x0000	W	0x20820000	Version of the CSI-2 host controller 0
CSI2RX_1C00_CTRL1	0x0004	W	0x00032103	Version of the CSI-2 host controller 1
CSI2RX_1C00_CTRL2	0x0008	W	0x00000000	Version of the CSI-2 host controller 2
CSI2RX_1C00_CTRL3	0x000C	W	0x00000000	Version of the CSI-2 host controller 3
CSI2RX_1C00_CSI2_RESETN	0x0010	W	0x00000003	CSI-2 controller reset
CSI2RX_1C00_DATA_IDS_1	0x0018	W	0x0000002B	List of Data Ids for which IDI reports line boundary matching errors (CSI2_HOST_N_DATA_IDS > 0). Data IDs for which IDI reports line boundary matching errors
CSI2RX_1C00_ERR_OVERFLOW	0x0028	W	0x00000000	Error state overflow register

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Name	Offset	Size	Reset Value	Description
CSI2RX_1C00_ERR_STAT	0x002C	W	0x00000000	Error state
CSI2RX_1C00_MASK_OVERFLOW	0x0038	W	0x00000000	Error state overflow register
CSI2RX_1C00_MASK_STAT	0x003C	W	0x00000000	Error state register 3
CSI2RX_1C00_RAW_RD_CTRL	0x0080	W	0x00000000	RAW_RD control register, the channel that read picture data from DDR
CSI2RX_1C00_RAW_RD_LINECNT_RO	0x0084	W	0x00000000	RAW_RD line counter
CSI2RX_1C00_RAW_RD_PIC_SIZE	0x0088	W	0x00000000	RAW_RD picture size
CSI2RX_1C00_RAW2_RD_LINECNT_RO	0x008C	W	0x00000000	RAW2_RD line counter
CSI2RX_1C00_ISP_LINECNT_RO	0x00B4	W	0x00000000	Current line counter
CSI2RX_1C00_RAW_WR_IBUF_STATUS_RO	0x00B8	W	0x00000000	HDR ibuf status
CSI2RX_1C00_FPN_CTRL	0x00D0	W	0x00000000	FPN control register
CSI2RX_1C00_FPN_TABLE_CTRL	0x00D4	W	0x00000001	FPN data write control register. The memory write address clear when finish
CSI2RX_1C00_FPN_TABLE_DATA0	0x00D8	W	0x00000000	FPN data register to memory. FPN data to memory, the memory write address add 1 after write
CSI2RX_1C00_FPN_TABLE_DATA1	0x00DC	W	0x00000000	FPN data register to memory. FPN data to memory, the memory write address add 1 after write
CSI2RX_1C00_VERSION	0x00FC	W	0x02013323	Version of the CSI-2 host controller

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.2 MMU

Name	Offset	Size	Reset Value	Description
MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address
MMU_STATUS	0x0004	W	0x00000000	MMU status register
MMU_COMMAND	0x0008	W	0x00000000	MMU command register
MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault
MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
MMU_INT_MASK	0x001C	W	0x00000000	MMU raw interrupt status register
MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
MMU_AUTO_GATING	0x0024	W	0x80000000	mmu auto gating

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.3 MI

Name	Offset	Size	Reset Value	Description
MI_1400_MI_WR_CTRL	0x0000	W	0x200A0000	Global write control register
MI_1400_MI_WR_INIT	0x0004	W	0x00000020	Control register for address initialization and skip function

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_MP_WR_Y_BASE	0x0008	W	0x00000000	Base address for main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_SIZE	0x000C	W	0x00000000	Size of main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT	0x0010	W	0x00000000	Offset counter initial value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT_START	0x0014	W	0x00000000	Offset counter start value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_IRQ_OFFS	0x0018	W	0x00000000	Fill level interrupt offset value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_CB_BASE	0x001C	W	0x00000000	Base address for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_SIZE	0x0020	W	0x00000000	Size of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT	0x0024	W	0x00000000	Offset counter initial value for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT_START	0x0028	W	0x00000000	Offset counter start value for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CR_BASE	0x002C	W	0x00000000	Base address for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_SIZE	0x0030	W	0x00000000	Size of main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT	0x0034	W	0x00000000	Offset counter initial value for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT_START	0x0038	W	0x00000000	Offset counter start value for main picture Cr component ring buffer
MI_1400_MI_SP_WR_Y_BASE	0x003C	W	0x00000000	Base address for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_SIZE	0x0040	W	0x00000000	Size of self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT	0x0044	W	0x00000000	Offset counter initial value for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT_START	0x0048	W	0x00000000	Offset counter start value for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_LLENGTH	0x004C	W	0x00000000	Line length of self picture Y component
MI_1400_MI_SP_WR_CB_BASE	0x0050	W	0x00000000	Base address for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_SIZE	0x0054	W	0x00000000	Size of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT	0x0058	W	0x00000000	Offset counter initial value for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT_START	0x005C	W	0x00000000	Offset counter start value for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CR_BASE	0x0060	W	0x00000000	Base address for self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_SIZE	0x0064	W	0x00000000	Size of self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_OFFS_CNT	0x0068	W	0x00000000	Offset counter initial value for self picture Cr component ring buffer

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_SP_WR_CR_OFFS_CNT_START	0x006C	W	0x00000000	Offset counter start value for self picture Cr component ring buffer
MI_1400_MI_WR_BYTE_CNT	0x0070	W	0x00000000	Counter value of JPEG or RAW data bytes
MI_1400_MI_WR_CTRL_SHD	0x0074	W	0x00000000	Global control internal shadow register
MI_1400_MI_MP_WR_Y_BASE_SHD	0x0078	W	0x00000000	Base address shadow register for main picture Y component, JPEG or raw data ring buffer
MI_1400_MI_MP_WR_Y_SIZE_SHD	0x007C	W	0x00000000	Size shadow register of main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT_SHD	0x0080	W	0x00000000	Current offset counter of main picture Y component, JPEG or raw data ring buffer
MI_1400_MI_MP_WR_Y_IRQ_OFFS_SHD	0x0084	W	0x00000000	Shadow register of fill level interrupt offset value for main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_CB_BASE_SHD	0x0088	W	0x00000000	Base address shadow register for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_SIZE_SHD	0x008C	W	0x00000000	Size shadow register of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT_SHD	0x0090	W	0x00000000	Current offset counter of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CR_BASE_SHD	0x0094	W	0x00000000	Base address shadow register for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_SIZE_SHD	0x0098	W	0x00000000	Size shadow register of main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT_SHD	0x009C	W	0x00000000	Current offset counter of main picture Cr component ring buffer
MI_1400_MI_SP_WR_Y_BASE_SHD	0x00A0	W	0x00000000	Base address shadow register for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_SIZE_SHD	0x00A4	W	0x00000000	Size shadow register of self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT_SHD	0x00A8	W	0x00000000	Current offset counter of self picture Y component ring buffer
MI_1400_MI_SP_WR_CB_BASE_AD_SHD	0x00B0	W	0x00000000	Base address shadow register for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_SIZE_SHD	0x00B4	W	0x00000000	Size shadow register of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT_SHD	0x00B8	W	0x00000000	Current offset counter of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CR_BASE_AD_SHD	0x00BC	W	0x00000000	Base address shadow register for self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_SIZE_SHD	0x00C0	W	0x00000000	Size shadow register of self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_OFFS_CNT_SHD	0x00C4	W	0x00000000	Current offset counter of self picture Cr component ring buffer

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_IMSC	0x00F8	W	0x00000000	Interrupt Mask1'b1: Interrupt active1'b0: Interrupt masked
MI_1400_MI_RIS	0x00FC	W	0x00000000	Raw Interrupt Status
MI_1400_MI_MIS	0x0100	W	0x00000000	Masked Interrupt Status
MI_1400_MI_ICR	0x0104	W	0x00000000	Interrupt Clear Register
MI_1400_MI_ISR	0x0108	W	0x00000000	Interrupt Set Register
MI_1400_MI_STATUS	0x010C	W	0x00000000	MI Status Register
MI_1400_MI_STATUS_CLR	0x0110	W	0x00000000	MI Status Clear Register
MI_1400_MI_SP_WR_Y_PIC_WIDTH	0x0114	W	0x00000000	Y component image width for self picture
MI_1400_MI_SP_WR_Y_PIC_HEIGHT	0x0118	W	0x00000000	Y component image height for self picture
MI_1400_MI_SP_WR_Y_PIC_SIZE	0x011C	W	0x00000000	Y component image size for self picture
MI_1400_MI_WR_PIXEL_CNT	0x012C	W	0x00000000	Counter value for defect pixel list
MI_1400_MI_MP_WR_Y_BASE2	0x0130	W	0x00000000	Base address 2 (ping pong) for main picture Y component
MI_1400_MI_MP_WR_CB_BASE2	0x0134	W	0x00000000	Base address 2 (ping pong) for main picture CB component
MI_1400_MI_MP_WR_CR_BASE2	0x0138	W	0x00000000	Base address 2 (ping pong) for main picture CR component
MI_1400_MI_SP_WR_Y_BASE2	0x013C	W	0x00000000	Base address 2 (ping pong) for self picture Y component
MI_1400_MI_SP_WR_CB_BASE2	0x0140	W	0x00000000	Base address 2 (ping pong) for self picture CB component
MI_1400_MI_SP_WR_CR_BASE2	0x0144	W	0x00000000	Base address 2 (ping pong) for self picture CR component
MI_1400_MI_WR_XTD_FORMAT_CTRL	0x0148	W	0x00000000	Extended Storage Format Control for main, self and dma read path
MI_1400_MI_WR_ID	0x0154	W	0x65432100	AXI write id group1
MI_1400_MI_MP_WR_Y_IRQ_OFFS2	0x01E0	W	0x00000000	Fill level interrupt2 offset value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_IRQ_OFFS2_SHD	0x01E4	W	0x00000000	Shadow register of fill level interrupt2 offset value for main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_LLENGTH	0x01E8	W	0x00000000	Line length of main picture Y component
MI_1400_MI_MP_WR_Y_PIC_WIDTH	0x01EC	W	0x00000000	Y component image width for main picture
MI_1400_MI_MP_WR_Y_PIC_HEIGHT	0x01F0	W	0x00000000	Y component image height for main picture
MI_1400_MI_MP_WR_Y_PIC_SIZE	0x01F4	W	0x00000000	Y component image size
MI_1400_MI_MP_WR_CTRL	0x01F8	W	0x00000200	Main path write control register
MI_1400_MI_SP_WR_Y_END_ADDR	0x0268	W	0x00000000	SP y frame end address
MI_1400_MI_SP_WR_CB_END_ADDR	0x026C	W	0x00000000	SP uv frame end address
MI_1400_MI_WR_CTRL2	0x0400	W	0x00000000	New path control register
MI_1400_MI_WR_ID2	0x0404	W	0x00000000	AXI write id group2

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_RD_CTRL2	0x0408	W	0x00A50000	DMA path control register
MI_1400_MI_RD_ID	0x040C	W	0x00000000	AXI read id group
MI_1400_MI_WR_CTRL2_SHD	0x0410	W	0x00000000	New path control register
MI_1400_MI_WR_WRAP_CTRL	0x0414	W	0x00000037	MI write wrap control
MI_1400_MI_WR_VFLIP_CTRL	0x0418	W	0x00000000	MI write wrap control
MI_1400_RAW0_RD_BASE	0x0470	W	0x00000000	Base address for mipi raw0 rx. Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_LENGTH	0x0474	W	0x00000000	Line length of raw0 rx (virtual width). Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_BASE_SHD	0x0478	W	0x00000000	Base shadow address for mipi raw0 rx. Update mode include hdr_dbg read pulse.Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_SIZE	0x047C	W	0x00000000	Frame size of raw0 read
MI_1400_RAW1_RD_BASE	0x0480	W	0x00000000	Base address for mipi raw1 rx. Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_LENGTH	0x0484	W	0x00000000	Line length of raw1 rx (virtual width). Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_BASE_SHD	0x0488	W	0x00000000	Base shadow address for mipi raw1 rx. Update mode include hdr_dbg read pulse.Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_SIZE	0x048C	W	0x00000000	Frame size of raw1 read
MI_1400_RAWS_RD_BASE	0x0490	W	0x00000000	Base address for mipi raws rx. Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_LENGTH	0x0494	W	0x00000000	Line length of raws rx (virtual width). Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_BASE_SHD	0x0498	W	0x00000000	Base shadow address for mipi rawsrx. Update mode include hdr_dbg read pulse.Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_SIZE	0x049C	W	0x00000000	Frame size of raws read
MI_1400_LUT_CAC_RD_BASE	0x0530	W	0x00000000	Base address for cac read
MI_1400_LUT_CAC_RD_H_WSIZE	0x0534	W	0x00000000	Cac word size
MI_1400_LUT_CAC_RD_V_SIZE	0x0538	W	0x00000000	Cac lut v_size
MI_1400_LUT_3D_RD_BASE	0x0540	W	0x00000000	Base address for 3d lut read
MI_1400_LUT_LSC_RD_BASE	0x0544	W	0x00000000	Base address for lsc lut read

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Name	Offset	Size	Reset Value	Description
MI_1400_LUT_LDCH_RD_BASE	0x0548	W	0x00000000	Base address for ldch lut read
MI_1400_LUT_3D_RD_WSIZE	0x0550	W	0x000002D9	3d lut word size
MI_1400_LUT_LSC_RD_WSIZE	0x0554	W	0x00000000	3d lut word size
MI_1400_LUT_LDCH_RD_H_WSIZE	0x0558	W	0x00000000	Ldch lut word size
MI_1400_LUT_LDCH_RD_V_SIZE	0x055C	W	0x00000000	Ldch lut vertical size
MI_1400_DBR_WR_BASE	0x0560	W	0x00000000	Base address for debayer-in write, sws reuse
MI_1400_DBR_WR_SIZE	0x0564	W	0x00000000	Size of debayer-in write data
MI_1400_DBR_WR_LENGTH	0x0568	W	0x00000000	Line length of debayer-in write (virtual width)
MI_1400_DBR_WR_BASE_SHD	0x056C	W	0x00000000	Base address shadow register for debayer-in write data ring buffer
MI_1400_DBR_RD_BASE	0x0570	W	0x00000000	Base address for debayer-in read
MI_1400_DBR_RD_LENGTH	0x0574	W	0x00000000	Line length of debayer-in read (virtual width)
MI_1400_DBR_RD_BASE_SHD	0x0578	W	0x00000000	Base shadow address for debayer-in read
MI_1400_SWS_3A_WR_BASE	0x057C	W	0x00000000	AXI write 3A stats data to DDR address
MI_1400_GAIN_WR_BASE	0x0580	W	0x00000000	Base address for gain data write
MI_1400_GAIN_WR_SIZE	0x0584	W	0x00000000	Size of gain write data
MI_1400_GAIN_WR_LENGTH	0x0588	W	0x00000000	Line length of gain data write (virtual width)
MI_1400_GAIN_WR_BASE2	0x058C	W	0x00000000	Base address 2 for gain data write
MI_1400_GAIN_WR_BASE_SHD	0x0590	W	0x00000000	Base address shadow register for gain write data ring buffer
MI_1400_BAY3D_IIR_WR_BASE	0x05A0	W	0x00000000	Base address for bayer 3dnr iir write
MI_1400_BAY3D_IIR_WR_SIZE	0x05A4	W	0x00000000	Size of bayer 3dnr iir write data
MI_1400_BAY3D_IIR_WR_LENGTH	0x05A8	W	0x00000000	Line length of bayer 3dnr iir write (virtual width)
MI_1400_BAY3D_IIR_WR_BASE_SHD	0x05AC	W	0x00000000	Base address shadow register for bayer 3dnr iir write data ring buffer
MI_1400_BAY3D_IIR_RD_BASE	0x05B0	W	0x00000000	Base address for bayer 3dnr read
MI_1400_BAY3D_IIR_RD_LENGTH	0x05B4	W	0x00000000	Line length of bayer 3dnr read (virtual width)
MI_1400_BAY3D_IIR_RD_BASE_SHD	0x05B8	W	0x00000000	Base shadow address for bayer 3dnr read
MI_1400_BAY3D_CUR_WR_BASE	0x05C0	W	0x00000000	Base address for bayer 3dnr current write
MI_1400_BAY3D_CUR_WR_SIZE	0x05C4	W	0x00000000	Size of bayer 3dnr current write data
MI_1400_BAY3D_CUR_WR_LENGTH	0x05C8	W	0x00000000	Line length of bayer 3dnr current write (virtual width)

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Name	Offset	Size	Reset Value	Description
MI_1400_BAY3D_CUR_WR_BASE_SHD	0x05CC	W	0x00000000	Base address shadow register for bayer 3dnr current write data ring buffer
MI_1400_BAY3D_CUR_RD_BASE	0x05D0	W	0x00000000	Base address for bayer 3dnr read
MI_1400_BAY3D_CUR_RD_LENGTH	0x05D4	W	0x00000000	Line length of bayer 3dnr read (virtual width)
MI_1400_BAY3D_CUR_RD_BASE_SHD	0x05D8	W	0x00000000	Base shadow address for bayer 3dnr read
MI_1400_BAY3D_CUR_RD_SIZE	0x05DC	W	0x00000000	Frame size of bayer 3dnr read
MI_1400_BAY3D_DS_WR_BASE	0x05E0	W	0x00000000	Base address for bayer 3dnr down scale write
MI_1400_BAY3D_DS_WR_SIZE	0x05E4	W	0x00000000	Size of bayer 3dnr down scale write data
MI_1400_BAY3D_DS_WR_LENGTH	0x05E8	W	0x00000000	Line length of bayer 3dnr down scale write (virtual width)
MI_1400_BAY3D_DS_WR_BASE_SHD	0x05EC	W	0x00000000	Base address shadow register for bayer 3dnr down scale write data ring buffer
MI_1400_BAY3D_DS_RD_BASE	0x05F0	W	0x00000000	Base address for bayer 3dnr read
MI_1400_BAY3D_DS_RD_LENGTH	0x05F4	W	0x00000000	Line length of bayer 3dnr read (virtual width)
MI_1400_BAY3D_DS_RD_BASE_SHD	0x05F8	W	0x00000000	Base shadow address for bayer 3dnr read
MI_1400_AXI_CONF_RD_CTRL	0x0640	W	0x80000000	AXI configure read control for module registers, except MMU.
MI_1400_AXI_CONF_RD_BASE	0x0644	W	0x00000000	Base address for axi configure read
MI_1400_AXI_CONF_RD_H_WSIZE	0x0648	W	0x00000000	AXI configure read word size of horizontal direction
MI_1400_AXI_CONF_RD_V_SIZE	0x064C	W	0x00000000	AXI configure size of vertical direction
MI_1400_FRM_BUF_WR_BASE	0x0650	W	0x00000000	Base address for frame buffer write
MI_1400_FRM_BUF_WR_SIZE	0x0654	W	0x00000000	Size of frame buffer write data
MI_1400_FRM_BUF_RD_BASE	0x0658	W	0x00000000	Base address for frame buff read

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.4 ISP_TOP

Name	Offset	Size	Reset Value	Description
ISP_0400_CTRL0	0x0000	W	0x00006000	Global control register
ISP_0400_CTRL1	0x0004	W	0x0F800060	ISP acquisition properties
ISP_0400_ACQ_H_OFFS	0x0008	W	0x00000000	Horizontal input offset
ISP_0400_ACQ_V_OFFS	0x000C	W	0x00000000	Vertical input offset
ISP_0400_ACQ_H_SIZE	0x0010	W	0x10001000	Horizontal input size
ISP_0400_ACQ_V_SIZE	0x0014	W	0x00000C00	Vertical input size
ISP_0400_ACQ_NR_FRAMES	0x0018	W	0x00000000	Number of frames to be captured

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Name	Offset	Size	Reset Value	Description
ISP_0400_GAMMA_DX_LO	0x001C	W	0x44444444	De-Gamma Curve definition lower x increments (sampling points)
ISP_0400_GAMMA_DX_HI	0x0020	W	0x44444444	De-Gamma Curve definition higher x increments (sampling points)
ISP_0400_GAMMA_R_Y_0	0x0024	W	0x00000000	De-Gamma Curve definition y red 0
ISP_0400_GAMMA_R_Y_1	0x0028	W	0x00000100	De-Gamma Curve definition y red 1
ISP_0400_GAMMA_R_Y_2	0x002C	W	0x00000200	De-Gamma Curve definition y red 2
ISP_0400_GAMMA_R_Y_3	0x0030	W	0x00000300	De-Gamma Curve definition y red 3
ISP_0400_GAMMA_R_Y_4	0x0034	W	0x00000400	De-Gamma Curve definition y red 4
ISP_0400_GAMMA_R_Y_5	0x0038	W	0x00000500	De-Gamma Curve definition y red 5
ISP_0400_GAMMA_R_Y_6	0x003C	W	0x00000600	De-Gamma Curve definition y red 6
ISP_0400_GAMMA_R_Y_7	0x0040	W	0x00000700	De-Gamma Curve definition y red 7
ISP_0400_GAMMA_R_Y_8	0x0044	W	0x00000800	De-Gamma Curve definition y red 8
ISP_0400_GAMMA_R_Y_9	0x0048	W	0x00000900	De-Gamma Curve definition y red 9
ISP_0400_GAMMA_R_Y_10	0x004C	W	0x00000A00	De-Gamma Curve definition y red 10
ISP_0400_GAMMA_R_Y_11	0x0050	W	0x00000B00	De-Gamma Curve definition y red 11
ISP_0400_GAMMA_R_Y_12	0x0054	W	0x00000C00	De-Gamma Curve definition y red 12
ISP_0400_GAMMA_R_Y_13	0x0058	W	0x00000D00	De-Gamma Curve definition y red 13
ISP_0400_GAMMA_R_Y_14	0x005C	W	0x00000E00	De-Gamma Curve definition y red 14
ISP_0400_GAMMA_R_Y_15	0x0060	W	0x00000F00	De-Gamma Curve definition y red 15
ISP_0400_GAMMA_R_Y_16	0x0064	W	0x00000FFF	De-Gamma Curve definition y red 16
ISP_0400_GAMMA_G_Y_0	0x0068	W	0x00000000	De-Gamma Curve definition y green 0
ISP_0400_GAMMA_G_Y_1	0x006C	W	0x00000100	De-Gamma Curve definition y green 1
ISP_0400_GAMMA_G_Y_2	0x0070	W	0x00000200	De-Gamma Curve definition y green 2
ISP_0400_GAMMA_G_Y_3	0x0074	W	0x00000300	De-Gamma Curve definition y green 3
ISP_0400_GAMMA_G_Y_4	0x0078	W	0x00000400	De-Gamma Curve definition y green 4
ISP_0400_GAMMA_G_Y_5	0x007C	W	0x00000500	De-Gamma Curve definition y green 5
ISP_0400_GAMMA_G_Y_6	0x0080	W	0x00000600	De-Gamma Curve definition y green 6

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Name	Offset	Size	Reset Value	Description
ISP_0400_GAMMA_G_Y_7	0x0084	W	0x00000700	De-Gamma Curve definition y green 7
ISP_0400_GAMMA_G_Y_8	0x0088	W	0x00000800	De-Gamma Curve definition y green 8
ISP_0400_GAMMA_G_Y_9	0x008C	W	0x00000900	De-Gamma Curve definition y green 9
ISP_0400_GAMMA_G_Y_10	0x0090	W	0x00000A00	De-Gamma Curve definition y green 10
ISP_0400_GAMMA_G_Y_11	0x0094	W	0x00000B00	ISP_GAMMA_G_Y_11
ISP_0400_GAMMA_G_Y_12	0x0098	W	0x00000C00	De-Gamma Curve definition y green 12
ISP_0400_GAMMA_G_Y_13	0x009C	W	0x00000D00	De-Gamma Curve definition y green 13
ISP_0400_GAMMA_G_Y_14	0x00A0	W	0x00000E00	De-Gamma Curve definition y green 14
ISP_0400_GAMMA_G_Y_15	0x00A4	W	0x00000F00	De-Gamma Curve definition y green 15
ISP_0400_GAMMA_G_Y_16	0x00A8	W	0x00000FFF	De-Gamma Curve definition y green 16
ISP_0400_GAMMA_B_Y_0	0x00AC	W	0x00000000	De-Gamma Curve definition y blue 0
ISP_0400_GAMMA_B_Y_1	0x00B0	W	0x00000100	De-Gamma Curve definition y blue 1
ISP_0400_GAMMA_B_Y_2	0x00B4	W	0x00000200	De-Gamma Curve definition y blue 2
ISP_0400_GAMMA_B_Y_3	0x00B8	W	0x00000300	De-Gamma Curve definition y blue 3
ISP_0400_GAMMA_B_Y_4	0x00BC	W	0x00000400	De-Gamma Curve definition y blue 4
ISP_0400_GAMMA_B_Y_5	0x00C0	W	0x00000500	De-Gamma Curve definition y blue 5
ISP_0400_GAMMA_B_Y_6	0x00C4	W	0x00000600	De-Gamma Curve definition y blue 6
ISP_0400_GAMMA_B_Y_7	0x00C8	W	0x00000700	De-Gamma Curve definition y blue 7
ISP_0400_GAMMA_B_Y_8	0x00CC	W	0x00000800	De-Gamma Curve definition y blue 8
ISP_0400_GAMMA_B_Y_9	0x00D0	W	0x00000900	De-Gamma Curve definition y blue 9
ISP_0400_GAMMA_B_Y_10	0x00D4	W	0x00000A00	De-Gamma Curve definition y blue 10
ISP_0400_GAMMA_B_Y_11	0x00D8	W	0x00000B00	De-Gamma Curve definition y blue 11
ISP_0400_GAMMA_B_Y_12	0x00DC	W	0x00000C00	De-Gamma Curve definition y blue 12
ISP_0400_GAMMA_B_Y_13	0x00E0	W	0x00000D00	De-Gamma Curve definition y blue 13
ISP_0400_GAMMA_B_Y_14	0x00E4	W	0x00000E00	De-Gamma Curve definition y blue 14
ISP_0400_GAMMA_B_Y_15	0x00E8	W	0x00000F00	De-Gamma Curve definition y blue 15
ISP_0400_GAMMA_B_Y_16	0x00EC	W	0x00000FFF	De-Gamma Curve definition y blue 16

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Name	Offset	Size	Reset Value	Description
ISP_0400_AWB1_GAIN_G	0x0130	W	0x01000100	Auto white balance gain green after bayer-3dnr
ISP_0400_AWB1_GAIN_RB	0x0134	W	0x01000100	Auto white balance gain red and blue after bayer-3dnr
ISP_0400_AWB0_GAIN0_G	0x0138	W	0x01000100	Auto white balance gain green for normal channel and short-expose frame
ISP_0400_AWB0_GAIN0_RB	0x013C	W	0x01000100	Auto white balance gain red and blue for normal channel and short-expose frame
ISP_0400_AWB0_GAIN1_G	0x0140	W	0x00000000	Auto white balance gain green for Long-Expose frame(HDRx2) or Middle-Expose frame(HDRx3)
ISP_0400_AWB0_GAIN1_RB	0x0144	W	0x00000000	Auto white balance gain red and blue for Long-Expose frame(HDRx2) or Middle-Expose frame(HDRx3)
ISP_0400_AWB0_GAIN2_G	0x0148	W	0x00000000	Auto white balance gain green for Long-Expose frame(HDRx3)
ISP_0400_AWB0_GAIN2_RB	0x014C	W	0x00000000	Auto white balance gain red and blue for Long-Expose frame(HDRx3)
ISP_0400_HURRY_CTRL	0x0158	W	0x00006583	Isp interconnect hurry control
ISP_0400_AWQOS_CTRL	0x015C	W	0x00123121	AXI write qos to interconnect control
ISP_0400_ARQOS_CTRL	0x0160	W	0x01212131	AXI read qos to interconnect control
ISP_0400_IRQ_CFG0	0x0164	W	0x00000000	ISP out irq configure register0
ISP_0400_IRQ_CFG1	0x0168	W	0x00000000	ISP out irq configure register1
ISP_0400_CC_COEFF_0	0x0170	W	0x00000021	Color conversion coefficient 0
ISP_0400_CC_COEFF_1	0x0174	W	0x00000040	Color conversion coefficient 1
ISP_0400_CC_COEFF_2	0x0178	W	0x0000000D	Color conversion coefficient 2
ISP_0400_CC_COEFF_3	0x017C	W	0x000001ED	Color conversion coefficient 3
ISP_0400_CC_COEFF_4	0x0180	W	0x000001DB	Color conversion coefficient 4
ISP_0400_CC_COEFF_5	0x0184	W	0x00000038	Color conversion coefficient 5
ISP_0400_CC_COEFF_6	0x0188	W	0x00000038	Color conversion coefficient 6
ISP_0400_CC_COEFF_7	0x018C	W	0x000001D1	Color conversion coefficient 7
ISP_0400_CC_COEFF_8	0x0190	W	0x000001F7	Color conversion coefficient 8
ISP_0400_OUT_H_OFFS	0x0194	W	0x00000000	Horizontal offset of output window
ISP_0400_OUT_V_OFFS	0x0198	W	0x00000000	Vertical offset of output window
ISP_0400_OUT_H_SIZE	0x019C	W	0x00001000	Output horizontal picture size
ISP_0400_OUT_V_SIZE	0x01A0	W	0x00000C00	Output vertical picture size
ISP_0400_FLAGS_SHD	0x01A8	W	0x00000000	Flags (current status) of certain signals and Shadow registers for enable signals
ISP_0400_OUT_H_OFFS_SHD	0x01AC	W	0x00000000	Current horizontal offset of output window (shadow register)
ISP_0400_OUT_V_OFFS_SHD	0x01B0	W	0x00000000	Current vertical offset of output window (shadow register)
ISP_0400_OUT_H_SIZE_SHD	0x01B4	W	0x00000000	Current output horizontal picture size (shadow register)
ISP_0400_OUT_V_SIZE_SHD	0x01B8	W	0x00000000	Current output vertical picture size (shadow register)

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Name	Offset	Size	Reset Value	Description
ISP_0400_ISP_IMSC	0x01BC	W	0x00000000	Interrupt mask
ISP_0400_ISP_RIS	0x01C0	W	0x00000000	Raw interrupt status
ISP_0400_ISP_MIS	0x01C4	W	0x00000000	Masked interrupt status
ISP_0400_ISP_ICR	0x01C8	W	0x00000000	Interrupt clear register, high clear
ISP_0400_ISP_ISR	0x01CC	W	0x00000000	Interrupt set register, high set
ISP_0400_ISP3A_IMSC	0x01D0	W	0x00000000	Interrupt mask
ISP_0400_ISP3A_RIS	0x01D4	W	0x00000000	Raw interrupt status
ISP_0400_ISP3A_MIS	0x01D8	W	0x00000000	Masked interrupt status
ISP_0400_ISP3A_ICR	0x01DC	W	0x00000000	Interrupt clear register
ISP_0400_ERR	0x023C	W	0x00000000	ISP error register
ISP_0400_ERR_CLR	0x0240	W	0x00000000	ISP error clear register
ISP_0400_FRAME_COUNT	0x0244	W	0x00000000	Frame counter
ISP_0400_DEBUG1	0x0248	W	0x00000000	RKISP_DEBUG1
ISP_0400_DEBUG2	0x024C	W	0x00000000	RKISP_DEBUG2
ISP_0400_DEBUG3	0x0250	W	0x00000000	RKISP_DEBUG3
ISP_0400_DEBUG4	0x0254	W	0x00000000	RKISP_DEBUG4
ISP_0400_YNR_LUMA_RCTRL	0x0290	W	0x00000000	YNR luma ahb readback control register
ISP_0400_YNR_LUMA_RDATA	0x0294	W	0x00000000	YNR luma ahb readback data.
ISP_0400_STITCH_CTRL0	0x0298	W	0x00000000	Multi-sensor stitch control0
ISP_0400_STITCH_CTRL1	0x029C	W	0x00000000	Multi-sensor stitch control1
ISP_0400_STITCH_CTRL2	0x02A0	W	0x00000000	Multi-sensor stitch control2
ISP_0400_SLICE_ST_CTRL	0x02A4	W	0x00000000	ISP slice start control

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.5 CTRL

Name	Offset	Size	Reset Value	Description
CTRL_0000_VI_ISP_EN	0x0000	W	0x00000000	Isp_top_en control
CTRL_0000_VI_ISP_PATH	0x0004	W	0x00000000	3A path select
CTRL_0000_VI_ID	0x0008	W	0x03012106	Revision identification register
CTRL_0000_VI_ISP_CLK_CTRL	0x000C	W	0x00000000	Internal clock control register
CTRL_0000_VI_ICCL	0x0010	W	0x00006F7B	Internal clock control register
CTRL_0000_VI_IRCL	0x0014	W	0x00000000	Internal reset control register
CTRL_0000_VI_DPCL	0x0018	W	0x00000000	Data path control register
CTRL_0000_SWS_CFG	0x001C	W	0x00000000	Isp2enc handshake signals and 3A write

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.6 BLS

Name	Offset	Size	Reset Value	Description
ISP_BLS_3000_CTRL	0x0000	W	0x00000000	Global control register
ISP_BLS_3000_SAMPLES	0x0004	W	0x00000000	Samples register
ISP_BLS_3000_H1_START	0x0008	W	0x00000000	Window 1 horizontal start
ISP_BLS_3000_H1_STOP	0x000C	W	0x00000000	Window 1 horizontal stop
ISP_BLS_3000_V1_START	0x0010	W	0x00000000	Window 1 vertical start
ISP_BLS_3000_V1_STOP	0x0014	W	0x00000000	Window 1 vertical stop
ISP_BLS_3000_H2_START	0x0018	W	0x00000000	Window 2 horizontal start
ISP_BLS_3000_H2_STOP	0x001C	W	0x00000000	Window 2 horizontal stop

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Name	Offset	Size	Reset Value	Description
ISP_BLS_3000_V2_START	0x0020	W	0x00000000	Window 2 vertical start
ISP_BLS_3000_V2_STOP	0x0024	W	0x00000000	Window 2 vertical stop
ISP_BLS_3000_BLC0_A_FIXED	0x0028	W	0x00000000	Fixed black level A of main-path
ISP_BLS_3000_BLC0_B_FIXED	0x002C	W	0x00000000	Fixed black level B of main-path
ISP_BLS_3000_BLC0_C_FIXED	0x0030	W	0x00000000	Fixed black level C of main-path
ISP_BLS_3000_BLC0_D_FIXED	0x0034	W	0x00000000	Fixed black level D of main-path
ISP_BLS_3000_A_MEASURED	0x0038	W	0x00000000	Measured black level A
ISP_BLS_3000_B_MEASURED	0x003C	W	0x00000000	Measured black level B
ISP_BLS_3000_C_MEASURED	0x0040	W	0x00000000	Measured black level C
ISP_BLS_3000_D_MEASURED	0x0044	W	0x00000000	Measured black level D
ISP_BLS_3000_BLS1_A_FIXED	0x0048	W	0x00000000	Fixed black level A of bay3dnr-blc
ISP_BLS_3000_BLS1_B_FIXED	0x004C	W	0x00000000	Fixed black level B of bay3dnr-blc
ISP_BLS_3000_BLS1_C_FIXED	0x0050	W	0x00000000	Fixed black level C of bay3dnr-blc
ISP_BLS_3000_BLS1_D_FIXED	0x0054	W	0x00000000	Fixed black level D of bay3dnr-blc
ISP_BLS_3000_BLS2_A_FIXED	0x0058	W	0x00000000	Fixed black level A of 3a-awb
ISP_BLS_3000_BLS2_B_FIXED	0x005C	W	0x00000000	Fixed black level B of 3a-awb
ISP_BLS_3000_BLS2_C_FIXED	0x0060	W	0x00000000	Fixed black level C of 3a-awb
ISP_BLS_3000_BLS2_D_FIXED	0x0064	W	0x00000000	Fixed black level D of 3a-awb
ISP_BLS_3000_ISP_OB_OFFSET	0x0068	W	0x00000000	OB value for protecting dark texture, if not equal to zero then bls1 will auto-enable
ISP_BLS_3000_ISP_OB_PREDGAIN	0x006C	W	0x00000100	OB pre-dgain8,8 for replacing adrc-gain, in linear mode
ISP_BLS_3000_ISP_OB_MAX	0x0070	W	0x000FFFFF	AWB1 max value clip, value equal to predgain*0xfff.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.7 DPCC

Name	Offset	Size	Reset Value	Description
ISP_DPCC_3400_MODE	0x0000	W	0x00000004	Mode control for DPCC detection unit
ISP_DPCC_3400_OUTPUT_MODE	0x0004	W	0x00000003	Interpolation mode for correction unit
ISP_DPCC_3400_SET_USE	0x0008	W	0x00000007	DPCC methods set usage for detection
ISP_DPCC_3400_METHODS_SET_1	0x000C	W	0x00001D1D	Methods enable bits for SET_1

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Name	Offset	Size	Reset Value	Description
ISP_DPCC_3400_METHODS_SET_2	0x0010	W	0x00000707	Methods enable bits for SET_2
ISP_DPCC_3400_METHODS_SET_3	0x0014	W	0x00001F1F	Methods enable bits for SET_3
ISP_DPCC_3400_LINE_THRESH_1	0x0018	W	0x00000808	Line threshold SET_1
ISP_DPCC_3400_LINE_MAD_FAC_1	0x001C	W	0x00000404	Mean Absolute Difference (MAD) factor for Line check set 1
ISP_DPCC_3400_PG_FAC_1	0x0020	W	0x00000403	Peak gradient factor for set 1
ISP_DPCC_3400_RND_THRESH_1	0x0024	W	0x00000A0A	Rank Neighbor Difference(RND) threshold for set 1
ISP_DPCC_3400_RG_FAC_1	0x0028	W	0x00002020	Rank gradient factor for set 1
ISP_DPCC_3400_LINE_THRESH_2	0x002C	W	0x0000100C	Line threshold set 2
ISP_DPCC_3400_LINE_MAD_FAC_2	0x0030	W	0x00001810	Mean Absolute Difference (MAD) factor for Line check set 2
ISP_DPCC_3400_PG_FAC_2	0x0034	W	0x00000403	Peak gradient factor for set 2
ISP_DPCC_3400_RND_THRESH_2	0x0038	W	0x00000808	Rank Neighbor Difference threshold for set 2
ISP_DPCC_3400_RG_FAC_2	0x003C	W	0x00000808	Rank gradient factor for set 2
ISP_DPCC_3400_LINE_THRESH_3	0x0040	W	0x00002020	Line threshold set 3
ISP_DPCC_3400_LINE_MAD_FAC_3	0x0044	W	0x00000404	Mean Absolute Difference (MAD) factor for Line check set 3
ISP_DPCC_3400_PG_FAC_3	0x0048	W	0x00000403	Peak gradient factor for set 3
ISP_DPCC_3400_RND_THRESH_3	0x004C	W	0x00000806	Rank Neighbor Difference threshold for set 3
ISP_DPCC_3400_RG_FAC_3	0x0050	W	0x00000404	Rank gradient factor for set 3
ISP_DPCC_3400_RO_LIMITS	0x0054	W	0x00000A0A	Rank Order Limits
ISP_DPCC_3400_RND_OFFS	0x0058	W	0x00000FFF	Differential Rank Offsets for Rank Neighbor Difference
ISP_DPCC_3400_BPT_CTRL	0x005C	W	0x00000000	Bad pixel table settings
ISP_DPCC_3400_BPT_NUMBER	0x0060	W	0x00000000	Number of entries for bad pixel table (table based correction)
ISP_DPCC_3400_BPT_ADDR	0x0064	W	0x00000000	TABLE Start Address for table-based correction algorithm
ISP_DPCC_3400_BPT_DATA	0x0068	W	0x00000000	TABLE DATA register for read and write access of table RAM
ISP_DPCC_3400_BP_CNT	0x006C	W	0x00000000	Number of entries for bad pixel table (table based correction)
ISP_DPCC_3400_PDAF_EN	0x0070	W	0x00000000	Pdaf enable
ISP_DPCC_3400_PDAF_POINT_EN	0x0074	W	0x00000000	Enable for each pdaf point
ISP_DPCC_3400_PDAF_OFFSET	0x0078	W	0x00000000	Pdaf point offset position in wrapper

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Name	Offset	Size	Reset Value	Description
ISP_DPCC_3400_PDAF_WRAP	0x007C	W	0x00000000	Pdaf pattern size
ISP_DPCC_3400_PDAF_SCOPE	0x0080	W	0x00000000	The number of DPCC pattern
ISP_DPCC_3400_PDAF_POINT_0	0x0084	W	0x00000000	Point0 & point1 coordinate
ISP_DPCC_3400_PDAF_POINT_1	0x0088	W	0x00000000	Point2 & point3 coordinate
ISP_DPCC_3400_PDAF_POINT_2	0x008C	W	0x00000000	Point4 & point5 coordinate
ISP_DPCC_3400_PDAF_POINT_3	0x0090	W	0x00000000	Point6 & point7 coordinate
ISP_DPCC_3400_PDAF_POINT_4	0x0094	W	0x00000000	Point8 & point9 coordinate
ISP_DPCC_3400_PDAF_POINT_5	0x0098	W	0x00000000	Point10 & point11 coordinate
ISP_DPCC_3400_PDAF_POINT_6	0x009C	W	0x00000000	Point12 & point13 coordinate
ISP_DPCC_3400_PDAF_POINT_7	0x00A0	W	0x00000000	Point14 & point15 coordinate
ISP_DPCC_3400_PDAF_FORWARD_MED	0x00A4	W	0x00000000	Median value = center point = pdaf point , select forward median value or backwrad median value to replace pdaf point

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.8 HDRMGE

Name	Offset	Size	Reset Value	Description
ISP_HDRMGE_3800_CTRL	0x0000	W	0x00000000	Global control
ISP_HDRMGE_3800_GAIN0	0x0008	W	0x01000400	Gain0 configuration of S-frame
ISP_HDRMGE_3800_GAIN1	0x000C	W	0x04000100	Gain1 configuration of M-frame
ISP_HDRMGE_3800_GAIN2	0x0010	W	0x00000040	Gain2 configuration of L-frame (1106 no use)
ISP_HDRMGE_3800_LIGHTZ	0x0014	W	0x00FF00FF	Light zone configuration
ISP_HDRMGE_3800_MS_DIFF	0x0018	W	0x80000080	Ms_diff configuration
ISP_HDRMGE_3800_LM_DIFF	0x001C	W	0x80000080	Lm_diff configuration (1106 no use)
ISP_HDRMGE_3800_DIFF_Y0	0x0020	W	0x00000000	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y1	0x0024	W	0x00C900C9	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y2	0x0028	W	0x01FA01FA	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y3	0x002C	W	0x02C002C0	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y4	0x0030	W	0x032F032F	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y5	0x0034	W	0x03700370	Y value of L-curve0,1 configuration

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Name	Offset	Size	Reset Value	Description
ISP_HDRMGE_3800_DIFF_Y6	0x0038	W	0x03970397	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y7	0x003C	W	0x03B103B1	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y8	0x0040	W	0x03C203C2	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y9	0x0044	W	0x03CF03CF	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y10	0x0048	W	0x03D803D8	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y11	0x004C	W	0x03DE03DE	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y12	0x0050	W	0x03E403E4	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y13	0x0054	W	0x03E803E8	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y14	0x0058	W	0x03EB03EB	Y value of L-curve0,1
ISP_HDRMGE_3800_DIFF_Y15	0x005C	W	0x03EE03EE	Y value of L-curve0,1
ISP_HDRMGE_3800_DIFF_Y16	0x0060	W	0x03F003F0	Y value of L-curve0,1
ISP_HDRMGE_3800_OVER_Y0	0x0070	W	0x0310C400	Y value of ES-curve
ISP_HDRMGE_3800_OVER_Y1	0x0074	W	0x05715C01	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y2	0x0078	W	0x09826004	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y3	0x007C	W	0x0FB3EC0E	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y4	0x0080	W	0x18360C31	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y5	0x0084	W	0x22088098	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y6	0x0088	W	0x2B7ADD83	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y7	0x008C	W	0x331CC6B7	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y8	0x0090	W	0x386E1B86	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y9	0x0094	W	0x3BBEEFDA	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y10	0x0098	W	0x3DAF6BF5	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y11	0x009C	W	0x3EBFAFFD	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y12	0x00A0	W	0x3F5FD7FF	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y13	0x00A4	W	0x3FAFEBFF	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y14	0x00A8	W	0x3FDFF7FF	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y15	0x00AC	W	0x3FEFFBFF	Y value of ES-curve configuration

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Name	Offset	Size	Reset Value	Description
ISP_HDRMGE_3800_OVER_Y16	0x00B0	W	0x3FFFFFFF	Y value of ES-curve configuration
ISP_HDRMGE_3800_EACH_GAIN	0x00B4	W	0x01000400	Gain configuration of each-raw

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.9 BAY3D

Name	Offset	Size	Reset Value	Description
BAY3D_2C00_BAY3D_CTRL	0x0000	W	0x00000040	Bayer 3DNR control
BAY3D_2C00_BAY3D_KALRATIO	0x0004	W	0xFFFF0100	Soft threshold weight
BAY3D_2C00_BAY3D_GLBPK2	0x0008	W	0x00000800	Global pk gain
BAY3D_2C00_BAY3D_CTRL1	0x000C	W	0x00000001	Bayer 3DNR control 1
BAY3D_2C00_BAY3D_WGTLMT	0x0010	W	0x00000380	Weight limit
BAY3D_2C00_BAY3D_SIG0_X0	0x0014	W	0x102D002D	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG0_X1	0x0018	W	0x10331031	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG0_X2	0x001C	W	0x10571053	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG0_X3	0x0020	W	0x30D73057	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG0_X4	0x0024	W	0x715770D7	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG0_X5	0x0028	W	0x715D715B	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG0_X6	0x002C	W	0x72DD725D	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG0_X7	0x0030	W	0x771D76DD	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG0_Y0	0x0034	W	0x0C000C00	Sigma curve coordinate y, [integer, fraction] = [4, 10]
BAY3D_2C00_BAY3D_SIG0_Y1	0x0038	W	0x0C000C00	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG0_Y2	0x003C	W	0x0A000A00	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG0_Y3	0x0040	W	0x0A000A00	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG0_Y4	0x0044	W	0x08000800	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG0_Y5	0x0048	W	0x08000800	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG0_Y6	0x004C	W	0x06000600	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG0_Y7	0x0050	W	0x04000600	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG1_X0	0x0054	W	0x102D002D	Sigma curve coordinate x

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Name	Offset	Size	Reset Value	Description
BAY3D_2C00_BAY3D_SIG1_X1	0x0058	W	0x10331031	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG1_X2	0x005C	W	0x10571053	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG1_X3	0x0060	W	0x30D73057	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG1_X4	0x0064	W	0x715770D7	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG1_X5	0x0068	W	0x715D715B	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG1_X6	0x006C	W	0x72DD725D	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG1_X7	0x0070	W	0x771D76DD	Sigma curve coordinate x
BAY3D_2C00_BAY3D_SIG1_Y0	0x0074	W	0x096C096C	Sigma curve coordinate y, [integer, fraction] = [4, 10]
BAY3D_2C00_BAY3D_SIG1_Y1	0x0078	W	0x096C096C	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG1_Y2	0x007C	W	0x04B604B6	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG1_Y3	0x0080	W	0x04B604B6	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG1_Y4	0x0084	W	0x04B604B6	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG1_Y5	0x0088	W	0x04B604B6	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG1_Y6	0x008C	W	0x04B604B6	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG1_Y7	0x0090	W	0x04B604B6	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG2_Y0	0x0094	W	0x007E007E	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG2_Y1	0x0098	W	0x007E007E	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG2_Y2	0x009C	W	0x003F003F	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG2_Y3	0x00A0	W	0x003F003F	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG2_Y4	0x00A4	W	0x003F003F	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG2_Y5	0x00A8	W	0x003F003F	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG2_Y6	0x00AC	W	0x003F003F	Sigma curve coordinate y
BAY3D_2C00_BAY3D_SIG2_Y7	0x00B0	W	0x003F003F	Sigma curve coordinate y
BAY3D_2C00_BAY3D_LODIF_STAT0	0x00B4	W	0x00000000	BAY3D low difference sum
BAY3D_2C00_BAY3D_LODIF_STAT1	0x00B8	W	0x00000000	BAY3D low difference sum
BAY3D_2C00_BAY3D_HIDIF_STAT0	0x00BC	W	0x00000000	BAY3D high difference sum
BAY3D_2C00_BAY3D_HIDIF_STAT1	0x00C0	W	0x00000000	BAY3D high difference sum

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Name	Offset	Size	Reset Value	Description
BAY3D_2C00_BAY3D_MI_ST	0x00C8	W	0x0000001C	BAY3D MI auto/manual start
BAY3D_2C00_BAY3D_RO_CNT	0x00CC	W	0x00000000	BAY3D running state: col/row counter
BAY3D_2C00_BAY3D_RO_FIFO_CUR	0x00D0	W	0x00000000	BAY3D running state: current MI FIFO space2empty
BAY3D_2C00_BAY3D_RO_FIFO_IIR	0x00D4	W	0x00000000	BAY3D running state: IIR MI FIFO space2empty
BAY3D_2C00_BAY3D_RO_FIFO_DS	0x00D8	W	0x00000000	BAY3D running state: downscale MI FIFO space2empty
BAY3D_2C00_BAY3D_RO_FIFO_STATE	0x00DC	W	0x00000000	BAY3D FIFO state
BAY3D_2C00_BAY3D_IN_IRQ_LINECNT	0x00E0	W	0x0000004E	BAY3D input interrupt line_cnt
BAY3D_2C00_BAY3D_HISIGRAT	0x00E4	W	0x00000000	BAY3D high weight optimise parameters sigma ratio
BAY3D_2C00_BAY3D_HISIGOFF	0x00E8	W	0x04000100	BAY3D high weight optimise parameters sigma offset
BAY3D_2C00_BAY3D_LOSIG	0x00EC	W	0x00000000	BAY3D low weight optimise parameters sigma offset
BAY3D_2C00_BAY3D_SIGPK	0x00F0	W	0x00000000	BAY3D pk weight optimise parameters sigma offset
BAY3D_2C00_BAY3D_SIGGAUS	0x00F4	W	0x08100810	BAY3D sigma index filter kernel
BAY3D_2C00_BAY3D_WRMI	0x00F8	W	0x00000000	BAY3D current MI write counter
BAY3D_2C00_BAY3D_RDMI	0x00FC	W	0x00000000	BAY3D current MI read counter

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.10 LSC

Name	Offset	Size	Reset Value	Description
ISP_LSC_2200_CTRL	0x0000	W	0x00000000	Lens shade control
ISP_LSC_2200_R_TABLE_ADDR	0x0004	W	0x00000000	Table RAM Address for red component
ISP_LSC_2200_GR_TABLE_ADDR	0x0008	W	0x00000000	Table RAM Address for green (red) component
ISP_LSC_2200_B_TABLE_ADDR	0x000C	W	0x00000000	Table RAM Address for blue component
ISP_LSC_2200_GB_TABLE_ADDR	0x0010	W	0x00000000	Table RAM Address for green (blue) component
ISP_LSC_2200_R_TABLE_DATA	0x0014	W	0x00000000	Sample table red
ISP_LSC_2200_GR_TABLE_DATA	0x0018	W	0x00000000	Sample table green (red)
ISP_LSC_2200_B_TABLE_DATA	0x001C	W	0x00000000	Sample table blue
ISP_LSC_2200_GB_TABLE_DATA	0x0020	W	0x00000000	Sample table green (blue)
ISP_LSC_2200_XGRAD_01	0x0024	W	0x00000000	Gradient table x
ISP_LSC_2200_XGRAD_23	0x0028	W	0x00000000	Gradient table x

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Name	Offset	Size	Reset Value	Description
ISP_LSC_2200_XGRAD_45	0x002C	W	0x00000000	Gradient table x
ISP_LSC_2200_XGRAD_67	0x0030	W	0x00000000	Gradient table x
ISP_LSC_2200_YGRAD_01	0x0034	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_23	0x0038	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_45	0x003C	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_67	0x0040	W	0x00000000	Gradient table y
ISP_LSC_2200_XSIZE_01	0x0044	W	0x00000000	Size table
ISP_LSC_2200_XSIZE_23	0x0048	W	0x00000000	Size table
ISP_LSC_2200_XSIZE_45	0x004C	W	0x00000000	Size table
ISP_LSC_2200_XSIZE_67	0x0050	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_01	0x0054	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_23	0x0058	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_45	0x005C	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_67	0x0060	W	0x00000000	Size table
ISP_LSC_2200_TABLE_SEL	0x0064	W	0x00000000	Lens shade table set selection
ISP_LSC_2200_ISP_LSC_STATUS	0x0068	W	0x00000000	Lens shade status
ISP_LSC_2200_XGRAD_89	0x0070	W	0x00000000	Gradient table x
ISP_LSC_2200_XGRAD_AB	0x0074	W	0x00000000	Gradient table x
ISP_LSC_2200_XGRAD_CD	0x0078	W	0x00000000	Gradient table x
ISP_LSC_2200_XGRAD_EF	0x007C	W	0x00000000	Gradient table x
ISP_LSC_2200_YGRAD_89	0x0080	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_AB	0x0084	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_CD	0x0088	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_EF	0x008C	W	0x00000000	Gradient table y
ISP_LSC_2200_XSIZE_89	0x0090	W	0x00000000	Size table
ISP_LSC_2200_XSIZE_AB	0x0094	W	0x00000000	Size table
ISP_LSC_2200_XSIZE_CD	0x0098	W	0x00000000	Size table
ISP_LSC_2200_XSIZE_EF	0x009C	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_89	0x00A0	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_AB	0x00A4	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_CD	0x00A8	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_EF	0x00AC	W	0x00000000	Size table

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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2.4.1.11 HDR_DRC

Name	Offset	Size	Reset Value	Description
ISP_DRC_3900_CTRL0	0x0000	W	0x00000000	Global hdr-control-0
ISP_DRC_3900_CTRL1	0x0004	W	0x83904100	Drc control1
ISP_DRC_3900_LPRATIO	0x0008	W	0x40000000	lp-ratio
ISP_DRC_3900_EXPLRATIO	0x000C	W	0x60000000	Exp-ratio
ISP_DRC_3900_SIGMA	0x0010	W	0x00000000	Edge, motion control signals
ISP_DRC_3900_SPACESGM	0x0014	W	0x0FE40F80	Space sigma
ISP_DRC_3900_RANESGM	0x0018	W	0x04000400	Range sigma
ISP_DRC_3900_BILAT	0x001C	W	0x00000010	Bilateral configuration
ISP_DRC_3900_GAIN_Y0	0x0020	W	0x04000400	Curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y1	0x0024	W	0x04000400	Curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y2	0x0028	W	0x04000400	Curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y3	0x002C	W	0x04000400	Curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y4	0x0030	W	0x04000400	Curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y5	0x0034	W	0x04000400	Curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y6	0x0038	W	0x04000400	Curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y7	0x003C	W	0x04000400	Curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y8	0x0040	W	0x00000400	Curve gain Y0~Y16
ISP_DRC_3900_COMPRES_Y0	0x0044	W	0x022E0000	Curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y1	0x0048	W	0x0634043F	Curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y2	0x004C	W	0x09D3080F	Curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y3	0x0050	W	0x0D190B80	Curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y4	0x0054	W	0x11790EA0	Curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y5	0x0058	W	0x16771413	Curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y6	0x005C	W	0x1AB618AC	Curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y7	0x0060	W	0x1E5C1C9A	Curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y8	0x0064	W	0x00002000	Curve compress Y0~Y16
ISP_DRC_3900_SCALE_Y0	0x0068	W	0x00020000	Curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y1	0x006C	W	0x004C0014	Curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y2	0x0070	W	0x017D00C1	Curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y3	0x0074	W	0x03040277	Curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y4	0x0078	W	0x042A0397	Curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y5	0x007C	W	0x05C704BB	Curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y6	0x0080	W	0x074706A4	Curve scale Y0~Y16

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Name	Offset	Size	Reset Value	Description
ISP_DRC_3900_SCALE_Y7	0x0084	W	0x07E807B0	Curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y8	0x0088	W	0x00000800	Curve scale Y0~Y16
ISP_DRC_3900_IIRWG_GAIN	0x008C	W	0x00000000	Drc_min_ogain, drc_iir_weight
ISP_DRC_3900_LUM3X2_CTRL	0x0090	W	0x00000000	Adrc luma3x2 control
ISP_DRC_3900_LUM3X2_GAS	0x0094	W	0x00000040	Luma3x2 gaussian factor

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.12 DEBAYER

Name	Offset	Size	Reset Value	Description
ISP_DEBAYER_2500_CONTROL	0x0000	W	0x00000110	DEBAYER CONTROL
ISP_DEBAYER_2500_G_INTERP	0x0004	W	0x040D6381	G INTERPOLATION REGISTER
ISP_DEBAYER_2500_G_INTERP_FILTER1	0x0008	W	0x041C021E	THIS FILTER IS FOR GETTING THE EDGE OF LOW FREQUENCY
ISP_DEBAYER_2500_G_INTERP_FILTER2	0x000C	W	0x041E021F	THIS FILTER IS FOR GETTING THE DETAIL OF HIGH FREQUENCY
ISP_DEBAYER_2500_G_INTERP_OFFSET	0x0010	W	0x00800004	G INTERPOLATION OFFSET REGISTER
ISP_DEBAYER_2500_G_FILTER_OFFSET	0x0014	W	0x00000001	G FILTER OFFSET REGISTER

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.13 CCM

Name	Offset	Size	Reset Value	Description
ISP_CCM_0700_CTRL	0x0000	W	0x00000000	ISP CCM Enable
ISP_CCM_0700_COEFF0_R	0x0004	W	0x07B70065	CCM matrix R coefficient 0 & 1
ISP_CCM_0700_COEFF1_R	0x0008	W	0x000007E4	CCM matrix R coefficient 2 & offset
ISP_CCM_0700_COEFF0_G	0x000C	W	0x005807D9	CCM matrix G coefficient 0 & 1
ISP_CCM_0700_COEFF1_G	0x0010	W	0x000007CF	CCM matrix G coefficient 2 & offset
ISP_CCM_0700_COEFF0_B	0x0014	W	0x07B70002	CCM matrix B coefficient 0&1
ISP_CCM_0700_COEFF1_B	0x0018	W	0x00000046	CCM matrix B coefficient 2 & offset
ISP_CCM_0700_COEFF0_Y	0x001C	W	0x004B0026	The R&G coefficient of RGB2Y calculation
ISP_CCM_0700_COEFF1_Y	0x0020	W	0x0000000F	The B coefficient of RGB2Y calculation
ISP_CCM_0700_ALP_Y0	0x0024	W	0x04000400	CCM curve definition y0 & y1
ISP_CCM_0700_ALP_Y1	0x0028	W	0x04000400	CCM curve definition y2 & y3
ISP_CCM_0700_ALP_Y2	0x002C	W	0x04000400	CCM curve definition y4 & y5
ISP_CCM_0700_ALP_Y3	0x0030	W	0x04000400	CCM curve definition y6 & y7
ISP_CCM_0700_ALP_Y4	0x0034	W	0x04000400	CCM curve definition y8 & y9

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Name	Offset	Size	Reset Value	Description
ISP_CCM_0700_ALP_Y5	0x0038	W	0x04000400	CCM curve definition y10 & y11
ISP_CCM_0700_ALP_Y6	0x003C	W	0x04000400	CCM curve definition y12 & y13
ISP_CCM_0700_ALP_Y7	0x0040	W	0x04000400	CCM curve definition y14 & y15
ISP_CCM_0700_ALP_Y8	0x0044	W	0x04000400	CCM curve definition y16
ISP_CCM_0700_BOUND_BIT	0x0048	W	0x000000AA	Curve inflection point, the value is 2^bound_bit.
ISP_CCM_0700_ENHANCE0	0x004C	W	0x004B0026	CCM color enhance0
ISP_CCM_0700_ENHANCE1	0x0050	W	0x0000000F	CCM color enhance1

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.14 GAMMA_OUT

Name	Offset	Size	Reset Value	Description
ISP_GAMMA_OUT_0900_CTRL	0x0000	W	0x00000000	Global control register
ISP_GAMMA_OUT_0900_OFFSET	0x0004	W	0x00000000	Offset configuration register
ISP_GAMMA_OUT_0900_Y0	0x0010	W	0x00010000	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y1	0x0014	W	0x00030002	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y2	0x0018	W	0x00050004	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y3	0x001C	W	0x00070006	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y4	0x0020	W	0x000A0008	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y5	0x0024	W	0x000E000C	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y6	0x0028	W	0x00140010	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y7	0x002C	W	0x001C0018	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y8	0x0030	W	0x00280020	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y9	0x0034	W	0x00380030	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y10	0x0038	W	0x00500040	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y11	0x003C	W	0x00700060	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y12	0x0040	W	0x00A00080	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y13	0x0044	W	0x00E000C0	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y14	0x0048	W	0x01400100	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y15	0x004C	W	0x01C00180	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y16	0x0050	W	0x02800200	Y value of gamma_out curve configuration register

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Name	Offset	Size	Reset Value	Description
ISP_GAMMA_OUT_0900_Y17	0x0054	W	0x03800300	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y18	0x0058	W	0x05000400	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y19	0x005C	W	0x07000600	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y20	0x0060	W	0x0A000800	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y21	0x0064	W	0x0E000C00	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y22	0x0068	W	0x0FFF0FFF	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y23	0x006C	W	0x0FFF0FFF	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y24	0x0070	W	0x00000FFF	Y value of gamma_out curve configuration register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.15 DEHAZE_ENHANCE

Name	Offset	Size	Reset Value	Description
ISP_DHAZ_3C00_CTRL	0x0000	W	0x00000110	Dehaze Control
ISP_DHAZ_3C00_ADP0	0x0004	W	0x1BF9C040	Dehaze Self-adaption Coefficient 0
ISP_DHAZ_3C00_ADP1	0x0008	W	0x00E6F0B4	Dehaze Self-adaption Coefficient 1
ISP_DHAZ_3C00_ADP2	0x000C	W	0x7DFAFAE6	Dehaze Self-adaption Coefficient 2
ISP_DHAZ_3C00_ADP_TMAX	0x0010	W	0x02000066	Dehaze Self-adaption Tmax
ISP_DHAZ_3C00_ADP_HIST0	0x0014	W	0x00044008	Dehaze Self-adaption Hist 0
ISP_DHAZ_3C00_ADP_HIST1	0x0018	W	0x001000E6	Dehaze Self-adaption Hist 1
ISP_DHAZ_3C00_ENHANCE	0x001C	W	0x060004CC	Enhance Value
ISP_DHAZ_3C00_IIR0	0x0020	W	0x000F0108	Dehaze Iir Control 0
ISP_DHAZ_3C00_IIR1	0x0024	W	0x07005F08	Dehaze Iir Control 1
ISP_DHAZ_3C00_SOFT_CFG0	0x0028	W	0x00CCD200	Dehaze User Configuration Register 0
ISP_DHAZ_3C00_SOFT_CFG1	0x002C	W	0x020000CC	Dehaze User Configuration Register 1
ISP_DHAZ_3C00_BF_SIGMA	0x0030	W	0x00804D99	Bilateral Filter Sigma
ISP_DHAZ_3C00_BF_WET	0x0034	W	0x01000080	Bilateral Filter Weight
ISP_DHAZ_3C00_ENH_CURVE0	0x0038	W	0x00400000	Enhance Curve Register 0
ISP_DHAZ_3C00_ENH_CURVE1	0x003C	W	0x00C00080	Enhance Curve Register 1
ISP_DHAZ_3C00_ENH_CURVE2	0x0040	W	0x01400100	Enhance Curve Register 2
ISP_DHAZ_3C00_ENH_CURVE3	0x0044	W	0x01C00180	Enhance Curve Register 3
ISP_DHAZ_3C00_ENH_CURVE4	0x0048	W	0x02400200	Enhance Curve Register 4
ISP_DHAZ_3C00_ENH_CURVE5	0x004C	W	0x02C00280	Enhance Curve Register 5

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Name	Offset	Size	Reset Value	Description
ISP_DHAZ_3C00_ENH_CURVE6	0x0050	W	0x03400300	Enhance Curve Register 6
ISP_DHAZ_3C00_ENH_CURVE7	0x0054	W	0x03C00380	Enhance Curve Register 7
ISP_DHAZ_3C00_ENH_CURVE8	0x0058	W	0x000003FF	Enhance Curve Register 8
ISP_DHAZ_3C00_GAUS	0x005C	W	0x00020408	Gauss Kernel
ISP_DHAZ_3C00_GAIN_IDX0	0x0060	W	0x40302010	Dehaze Gain Index
ISP_DHAZ_3C00_GAIN_IDX1	0x0064	W	0x80706050	Dehaze Gain Index
ISP_DHAZ_3C00_GAIN_IDX2	0x0068	W	0xC0B0A090	Dehaze Gain Index
ISP_DHAZ_3C00_GAIN_IDX3	0x006C	W	0x00F0E0D0	Dehaze Gain Index
ISP_DHAZ_3C00_GAIN_LUT0	0x0070	W	0x02000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_GAIN_LUT1	0x0074	W	0x02000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_GAIN_LUT2	0x0078	W	0x02000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_GAIN_LUT3	0x007C	W	0x02000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_GAIN_LUT4	0x0080	W	0x02000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_GAIN_LUT5	0x0084	W	0x02000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_GAIN_LUT6	0x0088	W	0x02000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_GAIN_LUT7	0x008C	W	0x02000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_GAIN_LUT8	0x0090	W	0x00000200	Dehaze Gain Look Up Table
ISP_DHAZ_3C00_SUMH_RD	0x009C	W	0x00000000	Read Hist Sum Register
ISP_DHAZ_3C00_HIST_WR0	0x00A8	W	0x02004000	Soft Write Hist RGB Register 0
ISP_DHAZ_3C00_HIST_WR1	0x00AC	W	0x05010030	Soft Write Hist RGB Register 1
ISP_DHAZ_3C00_HIST_WR2	0x00B0	W	0x0801C060	Soft Write Hist RGB Register 2
ISP_DHAZ_3C00_HIST_WR3	0x00B4	W	0x0B028090	Soft Write Hist RGB Register 3
ISP_DHAZ_3C00_HIST_WR4	0x00B8	W	0x0E0340C0	Soft Write Hist RGB Register 4
ISP_DHAZ_3C00_HIST_WR5	0x00BC	W	0x110400F0	Soft Write Hist RGB Register 5
ISP_DHAZ_3C00_HIST_WR6	0x00C0	W	0x1404C120	Soft Write Hist RGB Register 6
ISP_DHAZ_3C00_HIST_WR7	0x00C4	W	0x17058150	Soft Write Hist RGB Register 7
ISP_DHAZ_3C00_HIST_WR8	0x00C8	W	0x1A064180	Soft Write Hist RGB Register 8

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Name	Offset	Size	Reset Value	Description
ISP_DHAZ_3C00_HIST_WR9	0x00CC	W	0x1D0701B0	Soft Write Hist RGB Register 9
ISP_DHAZ_3C00_HIST_WR10	0x00D0	W	0x2007C1E0	Soft Write Hist RGB Register 10
ISP_DHAZ_3C00_HIST_WR11	0x00D4	W	0x23088210	Soft Write Hist RGB Register 11
ISP_DHAZ_3C00_HIST_WR12	0x00D8	W	0x26094240	Soft Write Hist RGB Register 12
ISP_DHAZ_3C00_HIST_WR13	0x00DC	W	0x290A0270	Soft Write Hist RGB Register 13
ISP_DHAZ_3C00_HIST_WR14	0x00E0	W	0x2C0AC2A0	Soft Write Hist RGB Register 14
ISP_DHAZ_3C00_HIST_WR15	0x00E4	W	0x2F0B82D0	Soft Write Hist RGB Register 15
ISP_DHAZ_3C00_HIST_WR16	0x00E8	W	0x320C4300	Soft Write Hist RGB Register 16
ISP_DHAZ_3C00_HIST_WR17	0x00EC	W	0x350D0330	Soft Write Hist RGB Register 17
ISP_DHAZ_3C00_HIST_WR18	0x00F0	W	0x380DC360	Soft Write Hist RGB Register 18
ISP_DHAZ_3C00_HIST_WR19	0x00F4	W	0x3B0E8390	Soft Write Hist RGB Register 19
ISP_DHAZ_3C00_HIST_WR20	0x00F8	W	0x3E0F43C0	Soft Write Hist RGB Register 20
ISP_DHAZ_3C00_HIST_WR21	0x00FC	W	0x000003F0	Soft Write Hist RGB Register 21
ISP_DHAZ_3C00_CTRL_SHD	0x0100	W	0x00000000	Dehaze Enable Shadow Register
ISP_DHAZ_3C00_ADP_RD0	0x0104	W	0x00C80003	Self_adaption Register 0
ISP_DHAZ_3C00_ADP_RD1	0x0108	W	0x000900CD	Self_adaption Register 1
ISP_DHAZ_3C00_HIST_REG0	0x0110	W	0x00100000	Histogram Equalization Register 0
ISP_DHAZ_3C00_HIST_REG1	0x0114	W	0x00300020	Histogram Equalization Register 1
ISP_DHAZ_3C00_HIST_REG2	0x0118	W	0x00500040	Histogram Equalization Register 2
ISP_DHAZ_3C00_HIST_REG3	0x011C	W	0x00700060	Histogram Equalization Register 3
ISP_DHAZ_3C00_HIST_REG4	0x0120	W	0x00900080	Histogram Equalization Register 4
ISP_DHAZ_3C00_HIST_REG5	0x0124	W	0x00B000A0	Histogram Equalization Register 5
ISP_DHAZ_3C00_HIST_REG6	0x0128	W	0x00D000C0	Histogram Equalization Register 6
ISP_DHAZ_3C00_HIST_REG7	0x012C	W	0x00F000E0	Histogram Equalization Register 7
ISP_DHAZ_3C00_HIST_REG8	0x0130	W	0x01100100	Histogram Equalization Register 8
ISP_DHAZ_3C00_HIST_REG9	0x0134	W	0x01300120	Histogram Equalization Register 9
ISP_DHAZ_3C00_HIST_REG10	0x0138	W	0x01500140	Histogram Equalization Register 10

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Name	Offset	Size	Reset Value	Description
ISP_DHAZ_3C00_HIST_REG11	0x013C	W	0x01700160	Histogram Equalization Register 11
ISP_DHAZ_3C00_HIST_REG12	0x0140	W	0x01900180	Histogram Equalization Register 12
ISP_DHAZ_3C00_HIST_REG13	0x0144	W	0x01B001A0	Histogram Equalization Register 13
ISP_DHAZ_3C00_HIST_REG14	0x0148	W	0x01D001C0	Histogram Equalization Register 14
ISP_DHAZ_3C00_HIST_REG15	0x014C	W	0x01F001E0	Histogram Equalization Register 15
ISP_DHAZ_3C00_HIST_REG16	0x0150	W	0x02100200	Histogram Equalization Register 16
ISP_DHAZ_3C00_HIST_REG17	0x0154	W	0x02300220	Histogram Equalization Register 17
ISP_DHAZ_3C00_HIST_REG18	0x0158	W	0x02500240	Histogram Equalization Register 18
ISP_DHAZ_3C00_HIST_REG19	0x015C	W	0x02700260	Histogram Equalization Register 19
ISP_DHAZ_3C00_HIST_REG20	0x0160	W	0x02900280	Histogram Equalization Register 20
ISP_DHAZ_3C00_HIST_REG21	0x0164	W	0x02B002A0	Histogram Equalization Register 21
ISP_DHAZ_3C00_HIST_REG22	0x0168	W	0x02D002C0	Histogram Equalization Register 22
ISP_DHAZ_3C00_HIST_REG23	0x016C	W	0x02F002E0	Histogram Equalization Register 23
ISP_DHAZ_3C00_HIST_REG24	0x0170	W	0x03100300	Histogram Equalization Register 24
ISP_DHAZ_3C00_HIST_REG25	0x0174	W	0x03300320	Histogram Equalization Register 25
ISP_DHAZ_3C00_HIST_REG26	0x0178	W	0x03500340	Histogram Equalization Register 26
ISP_DHAZ_3C00_HIST_REG27	0x017C	W	0x03700360	Histogram Equalization Register 27
ISP_DHAZ_3C00_HIST_REG28	0x0180	W	0x03900380	Histogram Equalization Register 28
ISP_DHAZ_3C00_HIST_REG29	0x0184	W	0x03B003A0	Histogram Equalization Register 29
ISP_DHAZ_3C00_HIST_REG30	0x0188	W	0x03D003C0	Histogram Equalization Register 30
ISP_DHAZ_3C00_HIST_REG31	0x018C	W	0x03F003E0	Histogram Equalization Register 31
ISP_DHAZ_3C00_ENH_LUMA0	0x0190	W	0x04010040	Enhance Luma Curve0
ISP_DHAZ_3C00_ENH_LUMA1	0x0194	W	0x04010040	Enhance Luma Curve1
ISP_DHAZ_3C00_ENH_LUMA2	0x0198	W	0x0C020040	Enhance Luma Curve2
ISP_DHAZ_3C00_ENH_LUMA3	0x019C	W	0x100400C0	Enhance Luma Curve3
ISP_DHAZ_3C00_ENH_LUMA4	0x01A0	W	0x10040100	Enhance Luma Curve4
ISP_DHAZ_3C00_ENH_LUMA5	0x01A4	W	0x00040100	Enhance Luma Curve5

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Name	Offset	Size	Reset Value	Description
ISP_DHAZ_3C00_STAB_FRAME	0x01F8	W	0x00000000	STABLE FRAME COUNT
ISP_DHAZ_3C00_PRE_FRAME	0x01FC	W	0x00000000	PREVIOUS THUMB FRAME COUNT

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.16 3DLUT

Name	Offset	Size	Reset Value	Description
ISP_3DLUT_3E00_CTRL	0x0000	W	0x00000000	3DLUT control register
ISP_3DLUT_3E00_UPDATE	0x0004	W	0x00000000	3DLUT lut update register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.17 YNR

Name	Offset	Size	Reset Value	Description
YNR_2700_GLOBAL_CTRL	0x0000	W	0x00801000	Control register
YNR_2700_RNR_MAX_R	0x0004	W	0x00803754	Control register
YNR_2700_RNR_CENTER_COOR	0x0008	W	0x00000001	Control register
YNR_2700_LOCAL_GAIN_CTRL	0x000C	W	0x00100010	Control register
YNR_2700_LOWNR_CTRL_0	0x0010	W	0x01000100	Control register
YNR_2700_LOWNR_CTRL_1	0x0014	W	0x00000080	Control register
YNR_2700_LOWNR_CTRL_2	0x0018	W	0x00100007	Control register
YNR_2700_LOWNR_CTRL_3	0x001C	W	0x40640133	Control register
YNR_2700_LOWNR_CTRL_4	0x002C	W	0x00000000	Control register
YNR_2700_GAUSS1_COEFF	0x0030	W	0x0054200B	Gauss coefficient for BFT3X3
YNR_2700_GAUSS2_COEFF	0x0034	W	0x00402010	Gauss coefficient for LGFT3X3
YNR_2700_SGM_DX_0_1	0x0040	W	0x00400000	X increments of noise intensity curve
YNR_2700_SGM_DX_2_3	0x0044	W	0x00C00080	X increments of noise intensity curve
YNR_2700_SGM_DX_4_5	0x0048	W	0x01400100	X increments of noise intensity curve
YNR_2700_SGM_DX_6_7	0x004C	W	0x01C00180	X increments of noise intensity curve
YNR_2700_SGM_DX_8_9	0x0050	W	0x02400200	X increments of noise intensity curve
YNR_2700_SGM_DX_10_11	0x0054	W	0x02C00280	X increments of noise intensity curve
YNR_2700_SGM_DX_12_13	0x0058	W	0x03400300	X increments of noise intensity curve
YNR_2700_SGM_DX_14_15	0x005C	W	0x03C00380	X increments of noise intensity curve

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Name	Offset	Size	Reset Value	Description
YNR_2700_SGM_DX_16	0x0060	W	0x00000400	X increments of noise intensity curve
YNR_2700_LSGM_Y_0_1	0x0070	W	0x00A0004C	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_2_3	0x0074	W	0x00E400D0	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_4_5	0x0078	W	0x00E400E8	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_6_7	0x007C	W	0x00CC00D8	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_8_9	0x0080	W	0x00C000C4	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_10_11	0x0084	W	0x00B800BC	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_12_13	0x0088	W	0x00A400B4	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_14_15	0x008C	W	0x00540088	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_16	0x0090	W	0x00000028	Noise intensity of low frequency coefficient
YNR_2700_RNR_STRENGTH03	0x00D0	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH47	0x00D4	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH8b	0x00D8	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTHcf	0x00DC	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH16	0x00E0	W	0x00000010	RNR strength adjust curve
YNR_2700_NLM_SIGMA_GAIN	0x00F0	W	0x0020800E	NLM SIGMA GAIN
YNR_2700_NLM_COE	0x00F4	W	0x00356367	NLM COEFFICIENT
YNR_2700_NLM_WEIGHT	0x00F8	W	0x00100005	NLM WEIGHT
YNR_2700_NLM_NR_WEIGHT	0x00FC	W	0x00000400	NLM NR WEIGHT

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.18 CNR

Name	Offset	Size	Reset Value	Description
ISP_CNR_2800_CTRL	0x0000	W	0x00000002	Global control
ISP_CNR_2800_EXGAIN	0x0004	W	0x00008080	External gain value
ISP_CNR_2800_THUMB1	0x0008	W	0x00C000A0	The parameter1 used in lbf1x7 module
ISP_CNR_2800_THUMB_BF_RATIO	0x000C	W	0x00000400	The parameter2 used in lbf1x7 module
ISP_CNR_2800_LBF_WEITD	0x0010	W	0x80808080	The distance weight in lbf1x7 module
ISP_CNR_2800_IIR_PARA1	0x0014	W	0x05A04D85	The parameter1 of IIR filter module
ISP_CNR_2800_IIR_PARA2	0x0018	W	0x00003A02	The parameter2 of IIR filter module

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Name	Offset	Size	Reset Value	Description
ISP_CNR_2800_GAUS_COE1	0x001C	W	0x061C1104	Gaussian filter coefficient parameter1
ISP_CNR_2800_GAUS_COE2	0x0020	W	0x0000301C	Gaussian filter coefficient parameter2
ISP_CNR_2800_GAUS_RATIO	0x0024	W	0x40000400	Gaussian and bf3x3 module parameter
ISP_CNR_2800_BF_PARA1	0x0028	W	0x0801B340	Bilateral filter 3x3 parameter1
ISP_CNR_2800_BF_PARA2	0x002C	W	0x00000014	Bilateral filter 3x3 parameter2
ISP_CNR_2800_SIGMA0	0x0030	W	0x405580FF	Sigma curve y0~y3
ISP_CNR_2800_SIGMA1	0x0034	W	0x1015202B	Sigma curve y4~y7
ISP_CNR_2800_SIGMA2	0x0038	W	0x01020408	Sigma curve y8~y11
ISP_CNR_2800_SIGMA3	0x003C	W	0x00000001	Sigma curve y12
ISP_CNR_2800_IIR_GLOBAL_GAIN	0x0040	W	0x00000040	The parameters for IIR gain control

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.19 SHARP

Name	Offset	Size	Reset Value	Description
ISP_SHARP_2900_EN	0x0000	W	0x00000000	Sharp Enable Ctrl
ISP_SHARP_2900_RATIO	0x0004	W	0x28800033	Sharp Ratio
ISP_SHARP_2900_LUMA_DX	0x0008	W	0x07887766	Sharp Luma Index
ISP_SHARP_2900_PBF_SIGMA_INV_0	0x000C	W	0x09430515	Sharp Pre Bilateral Filter Sigma Inverse Register 0
ISP_SHARP_2900_PBF_SIGMA_INV_1	0x0010	W	0x07819494	Sharp Pre Bilateral Filter Sigma Inverse Register 1
ISP_SHARP_2900_PBF_SIGMA_INV_2	0x0014	W	0x00025094	Sharp Pre Bilateral Filter Sigma Inverse Register 2
ISP_SHARP_2900_BF_SIGMA_INV_0	0x0018	W	0x0F14EDC7	Sharp Bilateral Filter Sigma Inverse Register 0
ISP_SHARP_2900_BF_SIGMA_INV_1	0x001C	W	0x0C3290F1	Sharp Bilateral Filter Sigma Inverse Register 1
ISP_SHARP_2900_BF_SIGMA_INV_2	0x0020	W	0x0003C4F1	Sharp Bilateral Filter Sigma Inverse Register 2
ISP_SHARP_2900_SIGMA_SHIFT	0x0024	W	0x00000076	Sharp PBF/BF Sigma Inverse Shift Bits
ISP_SHARP_2900_EHF_TH_0	0x0028	W	0x08020080	Sharp EHF Threshold Register 0
ISP_SHARP_2900_EHF_TH_1	0x002C	W	0x08020080	Sharp EHF Threshold Register 1
ISP_SHARP_2900_EHF_TH_2	0x0030	W	0x00000440	Sharp EHF Threshold Register 2
ISP_SHARP_2900_CLIP_HF_0	0x0034	W	0x08816040	Sharp High Frequency Clip Register 0
ISP_SHARP_2900_CLIP_HF_1	0x0038	W	0x0E03E0B4	Sharp High Frequency Clip Register 1
ISP_SHARP_2900_CLIP_HF_2	0x003C	W	0x00000048	Sharp High Frequency Clip Register 2
ISP_SHARP_2900_PBF_COEF	0x0040	W	0x000A1018	Sharp Pre Bilateral Filter Coefficient

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Name	Offset	Size	Reset Value	Description
ISP_SHARP_2900_BF_COEF	0x0044	W	0x000A1018	Sharp Bilateral Filter Coefficient
ISP_SHARP_2900_GAUS_COEF_0	0x0048	W	0x0006070C	Sharp Gauss Coefficient Register 0
ISP_SHARP_2900_GAUS_COEF_1	0x004C	W	0x00030405	Sharp Gauss Coefficient Register 1
ISP_SHARP_2900_GAIN	0x0050	W	0x80000010	Sharp Gain
ISP_SHARP_2900_GAIN_ADJUST0	0x0054	W	0x20004000	Sharp Gain Adjust Curve 0
ISP_SHARP_2900_GAIN_ADJUST1	0x0058	W	0x08001000	Sharp Gain Adjust Curve 1
ISP_SHARP_2900_GAIN_ADJUST2	0x005C	W	0x04000550	Sharp Gain Adjust Curve 2
ISP_SHARP_2900_GAIN_ADJUST3	0x0060	W	0x04000400	Sharp Gain Adjust Curve 3
ISP_SHARP_2900_GAIN_ADJUST4	0x0064	W	0x04000400	Sharp Gain Adjust Curve 4
ISP_SHARP_2900_GAIN_ADJUST5	0x0068	W	0x01000200	Sharp Gain Adjust Curve 5
ISP_SHARP_2900_GAIN_ADJUST6	0x006C	W	0x00010080	Sharp Gain Adjust Curve 6
ISP_SHARP_2900_CENTER	0x0070	W	0x01000080	Sharp Center
ISP_SHARP_2900_GAIN_DIS_STRENGTH0	0x0074	W	0x80808080	Sharp Gain Distance Strength Register 0
ISP_SHARP_2900_GAIN_DIS_STRENGTH1	0x0078	W	0x80808080	Sharp Gain Distance Strength Register 1
ISP_SHARP_2900_GAIN_DIS_STRENGTH2	0x007C	W	0x80808080	Sharp Gain Distance Strength Register 2
ISP_SHARP_2900_GAIN_DIS_STRENGTH3	0x0080	W	0x01010101	Sharp Gain Distance Strength Register 3
ISP_SHARP_2900_GAIN_DIS_STRENGTH4	0x0084	W	0x01010101	Sharp Gain Distance Strength Register 4
ISP_SHARP_2900_GAIN_DIS_STRENGTH5	0x0088	W	0x00000101	Sharp Gain Distance Strength Register 5
ISP_SHARP_2900_CLIP_NEG_0	0x0090	W	0x00000000	Sharp High Frequency Negative Clip Register 0
ISP_SHARP_2900_CLIP_NEG_1	0x0094	W	0x00000000	Sharp High Frequency Negative Clip Register 1
ISP_SHARP_2900_CLIP_NEG_2	0x0098	W	0x00000000	Sharp High Frequency Negative Clip Register 2

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.20 LDCH

Name	Offset	Size	Reset Value	Description
ISP_LDCH_3B00_LDCH_ADR_STS	0x0000	W	0x00000001	LDCH control register
ISP_LDCH_3B00_LDCH_BIC_TABLE0	0x0004	W	0x00000000	LDCH bicubic mode table0
ISP_LDCH_3B00_LDCH_BIC_TABLE1	0x0008	W	0x00000000	LDCH bicubic mode table1
ISP_LDCH_3B00_LDCH_BIC_TABLE2	0x000C	W	0x00000000	LDCH bicubic mode table2

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Name	Offset	Size	Reset Value	Description
ISP_LDCH_3B00_LDCH_BIC_TABLE3	0x0010	W	0x00000000	LDCH bicubic mode table3
ISP_LDCH_3B00_LDCH_BIC_TABLE4	0x0014	W	0x00000000	LDCH bicubic mode table4
ISP_LDCH_3B00_LDCH_BIC_TABLE5	0x0018	W	0x00000000	LDCH bicubic mode table5
ISP_LDCH_3B00_LDCH_BIC_TABLE6	0x001C	W	0x00000000	LDCH bicubic mode table6
ISP_LDCH_3B00_LDCH_BIC_TABLE7	0x0020	W	0x00000000	LDCH bicubic mode table7
ISP_LDCH_3B00_LDCH_BIC_TABLE8	0x0024	W	0x00000000	LDCH bicubic mode table8

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.21 GAIN

Name	Offset	Size	Reset Value	Description
ISP_GAIN_3F00_CTRL	0x0000	W	0x00000000	Gain control
ISP_GAIN_3F00_GAIN_G0	0x0004	W	0x00000040	HDR merge gain0 or initial gain when HDR disable
ISP_GAIN_3F00_GAIN_G1_G2	0x0008	W	0x00400040	Gain1 & gain2 for HDR_MERGE
ISP_GAIN_3F00_FIFO_STATUS	0x000C	W	0x00000000	All FIFO status

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.22 SELF_RESIZE

Name	Offset	Size	Reset Value	Description
SELF_RESIZE_0C00_1000_0E00_CTRL	0x0000	W	0x00000000	Global control register
SELF_RESIZE_0C00_1000_0E00_SCALE_HY	0x0004	W	0x00000000	Horizontal luminance scale factor register
SELF_RESIZE_0C00_1000_0E00_SCALE_HCB	0x0008	W	0x00000000	Horizontal chrominance scale factor register
SELF_RESIZE_0C00_1000_0E00_SCALE_HCR	0x000C	W	0x00000000	Horizontal chrominance scale factor register
SELF_RESIZE_0C00_1000_0E00_SCALE_VY	0x0010	W	0x00000000	Vertical luminance scale factor register
SELF_RESIZE_0C00_1000_0E00_SCALE_VC	0x0014	W	0x00000000	Vertical chrominance scale factor register The size of the output picture is calculated as follows:(size_out - 1) / (size_in - 1)) = scale,where size_in/out is the width or height of the in/output picture. The values of the MRSZ_SCALE registers then have to be int(scale x 2^16)+1
SELF_RESIZE_0C00_1000_0E00_PHASE_HY	0x0018	W	0x00000000	Horizontal luminance phase register
SELF_RESIZE_0C00_1000_0E00_PHASE_HC	0x001C	W	0x00000000	Horizontal chrominance phase register
SELF_RESIZE_0C00_1000_0E00_PHASE_VY	0x0020	W	0x00000000	Vertical luminance phase register

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Name	Offset	Size	Reset Value	Description
SELF_RESIZE_0C00_1000_0E00_PHASE_VC	0x0024	W	0x00000000	Vertical chrominance phase register
SELF_RESIZE_0C00_1000_0E00_SCALE_LUT_ADDR	0x0028	W	0x00000000	Address pointer of up-scaling look up table
SELF_RESIZE_0C00_1000_0E00_SCALE_LUT	0x002C	W	0x00000000	Entry of up-scaling look up table
SELF_RESIZE_0C00_1000_0E00_CTRL_SHD	0x0030	W	0x00000000	Global control shadow register
SELF_RESIZE_0C00_1000_0E00_SCALE_HY_SHD	0x0034	W	0x00000000	Horizontal luminance scale factor shadow register
SELF_RESIZE_0C00_1000_0E00_SCALE_HCB_SHD	0x0038	W	0x00000000	Horizontal Cb scale factor shadow register
SELF_RESIZE_0C00_1000_0E00_SCALE_HCR_SHD	0x003C	W	0x00000000	Horizontal Cr scale factor shadow register
SELF_RESIZE_0C00_1000_0E00_SCALE_VY_SHD	0x0040	W	0x00000000	Vertical luminance scale factor shadow register.
SELF_RESIZE_0C00_1000_0E00_SCALE_VC_SHD	0x0044	W	0x00000000	Vertical chrominance scale factor shadow register
SELF_RESIZE_0C00_1000_0E00_PHASE_HY_SHD	0x0048	W	0x00000000	Horizontal luminance phase shadow register
SELF_RESIZE_0C00_1000_0E00_PHASE_HC_SHD	0x004C	W	0x00000000	Horizontal chrominance phase shadow register.
SELF_RESIZE_0C00_1000_0E00_PHASE_VY_SHD	0x0050	W	0x00000000	Vertical luminance phase shadow register
SELF_RESIZE_0C00_1000_0E00_PHASE_VC_SHD	0x0054	W	0x00000000	Vertical chrominance phase shadow register
SELF_RESIZE_0C00_1000_0E00_HY_SIZE	0x0058	W	0x00000000	Scl out y size
SELF_RESIZE_0C00_1000_0E00_HC_SIZE	0x005C	W	0x00000000	Scl out uv size
SELF_RESIZE_0C00_1000_0E00_HY_OFFS_MI	0x0060	W	0x00000000	DDR data width is 128bit but Y data width is 8bit. This register configure the offset of first Y pix in 128bit, which rang from 0~15.
SELF_RESIZE_0C00_1000_0E00_HC_OFFS_MI	0x0064	W	0x00000000	DDR data width is 128bit but UV data width is 8bit. This register configure the offset of first UV pix in 128bit, which rang from 0~15.
SELF_RESIZE_0C00_1000_0E00_HY_SIZE_SHD	0x0068	W	0x00000000	Scl out y size shadow signal
SELF_RESIZE_0C00_1000_0E00_HC_SIZE_SHD	0x006C	W	0x00000000	Scl out uv size shadow signal
SELF_RESIZE_0C00_1000_0E00_HY_OFFS_MI_SHD	0x0070	W	0x00000000	Shadow signal of sw_scl_hy_offs_mi
SELF_RESIZE_0C00_1000_0E00_HC_OFFS_MI_SHD	0x0074	W	0x00000000	Shadow signal of sw_scl_hc_offs_mi
SELF_RESIZE_0C00_1000_0E00_IN_CROP_OFFSET	0x0078	W	0x00000000	Scl in data cut first some pixels if needed.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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2.4.1.23 BILINEAR_SCALE

Name	Offset	Size	Reset Value	Description
BILINEAR_SCALE_1000_SCALE_CTRL	0x0000	W	0x00000000	Global control register
BILINEAR_SCALE_1000_SCALE_UPDATE	0x0004	W	0x00000000	Shadow update register
BILINEAR_SCALE_1000_SCALE_SRC_SIZE	0x0008	W	0x00000000	Scale size of source (input)
BILINEAR_SCALE_1000_SCALE_DST_SIZE	0x000C	W	0x00000000	Scale size of destination (output)
BILINEAR_SCALE_1000_SCALE_HY_FAC	0x0010	W	0x00000000	Horizontal luminance scale factor register
BILINEAR_SCALE_1000_SCALE_HC_FAC	0x0014	W	0x00000000	Horizontal chrominance scale factor register
BILINEAR_SCALE_1000_SCALE_VY_FAC	0x0018	W	0x00000000	Vertical luminance scale factor register
BILINEAR_SCALE_1000_SCALE_VC_FAC	0x001C	W	0x00000000	Vertical chrominance scale factor register
BILINEAR_SCALE_1000_SCALE_HY_OFFS	0x0020	W	0x00000000	Horizontal luminance scale coordinate offset register for bilinear
BILINEAR_SCALE_1000_SCALE_HC_OFFS	0x0024	W	0x00000000	Horizontal chrominance scale coordinate offset register for bilinear
BILINEAR_SCALE_1000_SCALE_PHASE_HY	0x0030	W	0x00000000	Horizontal luminance phase register for average
BILINEAR_SCALE_1000_SCALE_PHASE_HC	0x0034	W	0x00000000	Horizontal chrominance phase register for average
BILINEAR_SCALE_1000_SCALE_PHASE_VY	0x0038	W	0x00000000	Vertical luminance phase register for average
BILINEAR_SCALE_1000_SCALE_PHASE_VC	0x003C	W	0x00000000	Vertical chrominance phase register for average
BILINEAR_SCALE_1000_SCALE_HY_SIZE	0x0040	W	0x00000000	Scale out Y size
BILINEAR_SCALE_1000_SCALE_HC_SIZE	0x0044	W	0x00000000	Scale out UV size for average
BILINEAR_SCALE_1000_SCALE_HY_OFFS_MI	0x0048	W	0x00000000	DDR data width is 128bit but Y data width is 8bit. This register configure the offset of first Y pixel in 128bit, which range from 0~15.
BILINEAR_SCALE_1000_SCALE_HC_OFFS_MI	0x004C	W	0x00000000	DDR data width is 128bit but UV data width is 8bit. This register configure the offset of first UV pixel in 128bit, which range from 0~15.
BILINEAR_SCALE_1000_SCALE_IN_CROP_OFFSET	0x0050	W	0x00000000	Scale in data cut first some pixels if needed.
BILINEAR_SCALE_1000_SCALE_CTRL_SHD	0x0080	W	0x00000000	Global control shadow register
BILINEAR_SCALE_1000_SCALE_SRC_SIZE_SHD	0x0088	W	0x00000000	Scale size of source (input), shadow register
BILINEAR_SCALE_1000_SCALE_DST_SIZE_SHD	0x008C	W	0x00000000	Scale size of destination (output), shadow register
BILINEAR_SCALE_1000_SCALE_HY_FAC_SHD	0x0090	W	0x00000000	Horizontal luminance scale factor shadow register

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Name	Offset	Size	Reset Value	Description
BILINEAR_SCALE_1000_SCALE_HC_FAC_SHD	0x0094	W	0x00000000	Horizontal chrominance scale factor shadow register
BILINEAR_SCALE_1000_SCALE_VY_FAC_SHD	0x0098	W	0x00000000	Vertical luminance scale factor shadow register
BILINEAR_SCALE_1000_SCALE_VC_FAC_SHD	0x009C	W	0x00000000	Vertical chrominance scale factor shadow register
BILINEAR_SCALE_1000_SCALE_HY_OFFS_SHD	0x00A0	W	0x00000000	Horizontal luminance scale coordinate offset shadow register for bilinear
BILINEAR_SCALE_1000_SCALE_HC_OFFS_SHD	0x00A4	W	0x00000000	Horizontal chrominance scale coordinate offset shadow register for bilinear
BILINEAR_SCALE_1000_SCALE_PHASE_HY_SHD	0x00B0	W	0x00000000	Horizontal luminance phase shadow register.
BILINEAR_SCALE_1000_SCALE_PHASE_HC_SHD	0x00B4	W	0x00000000	Horizontal chrominance phase shadow register.
BILINEAR_SCALE_1000_SCALE_PHASE_VY_SHD	0x00B8	W	0x00000000	Vertical luminance phase shadow register
BILINEAR_SCALE_1000_SCALE_PHASE_VC_SHD	0x00BC	W	0x00000000	Vertical chrominance phase shadow register
BILINEAR_SCALE_1000_SCALE_HY_SIZE_SHD	0x00C0	W	0x00000000	Scale out Y size shadow signal
BILINEAR_SCALE_1000_SCALE_HC_SIZE_SHD	0x00C4	W	0x00000000	Scale out UV size shadow signal
BILINEAR_SCALE_1000_SCALE_HY_OFFS_MI_SHD	0x00C8	W	0x00000000	Shadow signal of sw_scl_hy_offs_mi
BILINEAR_SCALE_1000_SCALE_HC_OFFS_MI_SHD	0x00CC	W	0x00000000	Shadow signal of sw_scl_hc_offs_mi
BILINEAR_SCALE_1000_SCALE_IN_CROP_OFFSET_SHD	0x00D0	W	0x00000000	Scale in data cut first some pixels if needed, shadow register.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.24 DUAL_CROP

Name	Offset	Size	Reset Value	Description
DUAL_CROP_0880_CTRL	0x0000	W	0x00000000	Global control register
DUAL_CROP_0880_M_H_OFFS	0x0004	W	0x00000080	MP path h offset
DUAL_CROP_0880_M_V_OFFS	0x0008	W	0x00000080	MP path v offset
DUAL_CROP_0880_M_H_SIZE	0x000C	W	0x00000080	MP path h size
DUAL_CROP_0880_M_V_SIZE	0x0010	W	0x00000C00	MP path v size
DUAL_CROP_0880_S_H_OFFS	0x0014	W	0x00000080	SP path h offset
DUAL_CROP_0880_S_V_OFFS	0x0018	W	0x00000080	SP path v offset
DUAL_CROP_0880_S_H_SIZE	0x001C	W	0x00000080	SP path h size
DUAL_CROP_0880_S_V_SIZE	0x0020	W	0x00000C00	SP path v size

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Name	Offset	Size	Reset Value	Description
DUAL_CROP_0880_M_H_OFFS_SHD	0x0024	W	0x00000080	MP path h offset shadow signal
DUAL_CROP_0880_M_V_OFFS_SHD	0x0028	W	0x00000080	MP path v offset shadow signal
DUAL_CROP_0880_M_H_SIZE_SHD	0x002C	W	0x00000080	MP path h size shadow signal
DUAL_CROP_0880_M_V_SIZE_SHD	0x0030	W	0x00000000	MP path v size shadow signal
DUAL_CROP_0880_S_H_OFFS_SHD	0x0034	W	0x00000080	SP path h offset
DUAL_CROP_0880_S_V_OFFS_SHD	0x0038	W	0x00000080	SP path v offset shadow signal
DUAL_CROP_0880_S_H_SIZE_SHD	0x003C	W	0x00000080	SP path h size shadow signal
DUAL_CROP_0880_S_V_SIZE_SHD	0x0040	W	0x00000080	SP path v size shadow signal
DUAL_CROP_0880_FBC_H_OFFS	0x0044	W	0x00000080	FBC path h offset
DUAL_CROP_0880_FBC_V_OFFS	0x0048	W	0x00000080	FBC path v offset
DUAL_CROP_0880_FBC_H_SIZE	0x004C	W	0x00000080	FBC path h size
DUAL_CROP_0880_FBC_V_SIZE	0x0050	W	0x00000080	FBC path v size
DUAL_CROP_0880_FBC_H_OFFS_SHD	0x0054	W	0x00000080	FBC path h offset
DUAL_CROP_0880_FBC_V_OFF_SHD	0x0058	W	0x00000080	FBC path v offset
DUAL_CROP_0880_FBC_H_SIZE_SHD	0x005C	W	0x00000080	FBC path h size
DUAL_CROP_0880_FBC_V_SIZE_SHD	0x0060	W	0x00000080	FBC path v size

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.25 FLASH

Name	Offset	Size	Reset Value	Description
ISP_FLASH_0660_CMD	0x0000	W	0x00000000	Flash command
ISP_FLASH_0660_CONFIG	0x0004	W	0x00000000	Flash configure
ISP_FLASH_0660_PREDIV	0x0008	W	0x00000000	Flash Counter Pre-Divider
ISP_FLASH_0660_DELAY	0x000C	W	0x00000000	Flash Delay
ISP_FLASH_0660_TIME	0x0010	W	0x00000000	Flash time
ISP_FLASH_0660_MAXP	0x0014	W	0x00000000	Maximum value for flash or preflash

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.26 SHUTTER

Name	Offset	Size	Reset Value	Description
ISP_SHUTTER_0680_CTRL	0x0000	W	0x00000000	Mechanical shutter control
ISP_SHUTTER_0680_PREDIV	0x0004	W	0x00000000	Mech. Shutter Counter Pre-Divider

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Name	Offset	Size	Reset Value	Description
ISP_SHUTTER_0680_DELAY	0x0008	W	0x00000000	Delay register
ISP_SHUTTER_0680_TIME	0x000C	W	0x00000000	Time register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.27 RAWAF

Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_CTRL	0x0000	W	0x00C100B6	This is the control register for RAWAF measurement unit
ISP_RAWAF_4D00_OFFSET_WINA	0x0004	W	0x00030003	Top Left corner of measure window A
ISP_RAWAF_4D00_SIZE_WINA	0x0008	W	0x00000000	Size of measure window A
ISP_RAWAF_4D00_OFFSET_WINB	0x000C	W	0x00000000	Top Left corner of measure window B
ISP_RAWAF_4D00_SIZE_WINB	0x0010	W	0x00000000	Size of measure window B
ISP_RAWAF_4D00_INT_LINE	0x0014	W	0x000FC963	Line of window 15x15 that need to produce int signal
ISP_RAWAF_4D00_CTRL1	0x0018	W	0x00000000	Size of measure window A
ISP_RAWAF_4D00_THRES	0x001C	W	0x00000000	Threshold and ram_star_addr register
ISP_RAWAF_4D00_VAR_SHIFT	0x0020	W	0x00000000	Variable shift register
ISP_RAWAF_4D00_HVIIR_VAR_SHIFT	0x0024	W	0x00000000	Variable shift register
ISP_RAWAF_4D00_SUM_B	0x0028	W	0x00000000	Sharpness Value Status Register of Window B
ISP_RAWAF_4D00_LUM_B	0x0030	W	0x00000000	Luminance Value Status Register of Window B
ISP_RAWAF_4D00_GAMMA_Y0	0x0034	W	0x002D0000	Include y0 and y1 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y1	0x0038	W	0x00B3006C	Include y2 and y3 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y2	0x003C	W	0x015800F5	Include y4 and y5 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y3	0x0040	W	0x01CB0199	Include y6 and y7 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y4	0x0044	W	0x023701F4	Include y8 and y9 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y5	0x0048	W	0x02A4026E	Include y10 and y11 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y6	0x004C	W	0x034102F7	Include y12 and y13 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y7	0x0050	W	0x03C20380	Include y14 and y15 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y8	0x0054	W	0x000003FF	Include y16 value of gamma table
ISP_RAWAF_4D00_INT_STATE	0x0058	W	0x00000000	Int state of five line interrupt
ISP_RAWAF_4D00_HIIR_THRESH	0x005C	W	0x00200020	AF measurement threshold

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Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_H1_IIR1_COE01	0x0060	W	0x02BB0200	H1IIR1 filter coefficient
ISP_RAWAF_4D00_H1_IIR1_COE23	0x0064	W	0x003F0F19	H1IIR1 filter coefficient
ISP_RAWAF_4D00_H1_IIR1_COE45	0x0068	W	0x0EB10000	H1IIR1 filter coefficient
ISP_RAWAF_4D00_H_CURVEL	0x006C	W	0x05061C40	LDG curve for H1 H2
ISP_RAWAF_4D00_H1_IIR2_COE01	0x0070	W	0x01BF0200	H1IIR2 filter coefficient
ISP_RAWAF_4D00_H1_IIR2_COE23	0x0074	W	0x00AC0E7E	H1IIR2 filter coefficient
ISP_RAWAF_4D00_H1_IIR2_COE45	0x0078	W	0x0FC10000	H1IIR2 filter coefficient
ISP_RAWAF_4D00_H_CURVEH	0x007C	W	0x057808B9	LDG curve for H1 H2
ISP_RAWAF_4D00_H2_IIR1_COE01	0x0080	W	0x02720200	H2IIR1 filter coefficient
ISP_RAWAF_4D00_H2_IIR1_COE23	0x0084	W	0x00670ECB	H2IIR1 filter coefficient
ISP_RAWAF_4D00_H2_IIR1_COE45	0x0088	W	0x0F990000	H2IIR1 filter coefficient
ISP_RAWAF_4D00_V_CURVEL	0x008C	W	0x05061C40	LDG curve for V1 V2
ISP_RAWAF_4D00_H2_IIR2_COE01	0x0090	W	0x01BF0200	H2IIR2 filter coefficient
ISP_RAWAF_4D00_H2_IIR2_COE23	0x0094	W	0x00AC0E9F	H2IIR2 filter coefficient
ISP_RAWAF_4D00_H2_IIR2_COE45	0x0098	W	0x0F540000	H2IIR2 filter coefficient
ISP_RAWAF_4D00_V_CURVEH	0x009C	W	0x057808B9	LDG curve for V1 V2
ISP_RAWAF_4D00_V_IIR_COE0	0x00A0	W	0x00AB00AB	VIIR filter coefficient
ISP_RAWAF_4D00_V_IIR_COE1	0x00A4	W	0x00330033	VIIR filter coefficient
ISP_RAWAF_4D00_V_IIR_COE2	0x00A8	W	0x00E700E7	VIIR filter coefficient
ISP_RAWAF_4D00_CORING_H	0x00AC	W	0x00E700E7	CORING for H direction input = (max(input - fv_thresh, 0) * fv_slope) >> AF_CORE_SLOP_FIX_BITS; ret = min(input, fv_limit);
ISP_RAWAF_4D00_V_FIR_COE0	0x00B0	W	0x02000200	1x3 VFIR filter coefficient
ISP_RAWAF_4D00_V_FIR_COE1	0x00B4	W	0x00000000	1x3 VFIR filter coefficient
ISP_RAWAF_4D00_V_FIR_COE2	0x00B8	W	0x0E000E00	1x3 VFIR filter coefficient
ISP_RAWAF_4D00_CORING_V	0x00BC	W	0x00E700E7	CORING for V direction
ISP_RAWAF_4D00_GAUS_COE_03	0x00C0	W	0x10081008	GAUS filter coefficient

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Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_GAUS_COE_47	0x00C4	W	0x10081020	GAUS filter coefficient
ISP_RAWAF_4D00_GAUS_COE_8	0x00C8	W	0x00000008	GAUS filter coefficient
ISP_RAWAF_4D00_HIGHLIT_THRESH	0x00D0	W	0x000003CC	Threshold and ram_star_addr register
ISP_RAWAF_4D00_HIGHLIT_CNT_WINB	0x00D8	W	0x00000000	Sharpness Value Status Register of Window B
ISP_RAWAF_4D00_RAM_DATA	0x00E0	W	0x00000000	Read 5x5 sum data in reg should choose this address, then data will be read out by AHB bus.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.28 RAWAE

Name	Offset	Size	Reset Value	Description
RAWAE_BIG_4400_4600_4700_CTRL	0x0000	W	0x00000000	Exposure control
RAWAE_BIG_4400_4600_4700_WND0_BLK_SIZE	0x0004	W	0x00000000	Size of one block for window0
RAWAE_BIG_4400_4600_4700_WND0_OFFSET	0x0008	W	0x00000000	Offset of one block for window0
RAWAE_BIG_4400_4600_4700_RAM_CTRL	0x000C	W	0x00000000	RAM address offset
RAWAE_BIG_4400_4600_4700_WND1_SIZE	0x0010	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4600_4700_WND1_OFFSET	0x0014	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4600_4700_WND2_SIZE	0x0018	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4600_4700_WND2_OFFSET	0x001C	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4600_4700_WND3_SIZE	0x0020	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4600_4700_WND3_OFFSET	0x0024	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4600_4700_WND4_SIZE	0x0028	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4600_4700_WND4_OFFSET	0x002C	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4600_4700_WND1_SUMR	0x0030	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND2_SUMR	0x0034	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND3_SUMR	0x0038	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND4_SUMR	0x003C	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND1_SUMG	0x0040	W	0x00000000	Sum G channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND2_SUMG	0x0044	W	0x00000000	Sum G channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND3_SUMG	0x0048	W	0x00000000	Sum G channel data for this single separated window

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Name	Offset	Size	Reset Value	Description
RAWAE_BIG_4400_4600_4700_WND4_SUMG	0x004C	W	0x00000000	Sum G channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND1_SUMB	0x0050	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND2_SUMB	0x0054	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND3_SUMB	0x0058	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND4_SUMB	0x005C	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4600_4700_RO_MEAN_BASE_ADDR	0x0080	W	0x00000000	Mean luminance value of block 00 ~ee(total 225) Read data from RAM, support burst16

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

Name	Offset	Size	Reset Value	Description
ISP_RAWAE_LITE_4500_CTRL	0x0000	W	0x00000000	Exposure control
ISP_RAWAE_LITE_4500_BLK_SIZE	0x0004	W	0x00000000	Horizontal size of one block
ISP_RAWAE_LITE_4500_OFFSET	0x0008	W	0x00000000	Horizontal offset for first block
ISP_RAWAE_LITE_4500_RO_MEAN_XX	0x0010	W	0x00000000	Reg name from EXP_MEAN_00 EXP_MEAN_24

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.29 RAWAWB

Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_CTRL	0x0000	W	0x00000000	Global control register
ISP_RAWAWB_5000_BLK_CTRL	0x0004	W	0xFFFF0000	Block control register
ISP_RAWAWB_5000_WIN_OFFS	0x0008	W	0x00000000	Awb vertical and horizontal offset of measure window
ISP_RAWAWB_5000_WIN_SIZE	0x000C	W	0x00000000	Awb vertical and horizontal window size
ISP_RAWAWB_5000_LIMIT_RG_MAX	0x0010	W	0x00000000	Max red and green value in white point detection
ISP_RAWAWB_5000_LIMIT_BY_MAX	0x0014	W	0x00000000	Max blue and luminance value in white point detection
ISP_RAWAWB_5000_LIMIT_RG_MIN	0x0018	W	0x00000000	Min red and green value in white point detection
ISP_RAWAWB_5000_LIMIT_BY_MIN	0x001C	W	0x00000000	Min blue and luminance value in white point detection
ISP_RAWAWB_5000_WEIGHT_CURVE_CTRL	0x0020	W	0x00000000	Weight curve control
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR03	0x0024	W	0x60402000	The X coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR47	0x0028	W	0xE0C0A080	The X coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR8	0x002C	W	0x000000FF	The X coordinate of Y weight curve

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR03	0x0030	W	0x20202020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR47	0x0034	W	0x20202020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR8	0x0038	W	0x01000020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_PREWBGAIN_INV	0x003C	W	0x01000100	This is a white balance gain invert operation
ISP_RAWAWB_5000_UVDETC_VERTEX0_0	0x0040	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX1_0	0x0044	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX2_0	0x0048	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX3_0	0x004C	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_ISLOPE01_0	0x0050	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_ISLOPE12_0	0x0054	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_ISLOPE23_0	0x0058	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_ISLOPE30_0	0x005C	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_VERTEX0_1	0x0060	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX1_1	0x0064	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX2_1	0x0068	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX3_1	0x006C	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_ISLOPE01_1	0x0070	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_ISLOPE12_1	0x0074	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_ISLOPE23_1	0x0078	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_ISLOPE30_1	0x007C	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_VERTEX0_2	0x0080	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX1_2	0x0084	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX2_2	0x0088	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_VERTEX3_2	0x008C	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UVDETC_ISLOPE01_2	0x0090	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_ISLOPE12_2	0x0094	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UVDETC_ISLOPE23_2	0x0098	W	0x00000000	UV detect, slope inversion

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_2	0x009C	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_VERTEX0_3	0x00A0	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX1_3	0x00A4	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX2_3	0x00A8	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX3_3	0x00AC	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_3	0x00B0	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_3	0x00B4	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_3	0x00B8	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_3	0x00BC	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_YUV_RGB2ROTY_0	0x0120	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTY_1	0x0124	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTU_0	0x0128	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTU_1	0x012C	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTV_0	0x0130	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTV_1	0x0134	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_X_COOR_Y_0	0x0140	W	0x00000000	The Y coordinate of point1 and vector point21 for light 0
ISP_RAWAWB_5000_YUV_X_COOR_U_0	0x0144	W	0x00000000	The U coordinate of point1 and vector point21 for light 0
ISP_RAWAWB_5000_YUV_X_COOR_V_0	0x0148	W	0x00000000	The V coordinate of point1 and vector point21 for light 0
ISP_RAWAWB_5000_YUV_X1X2_DIS_0	0x014C	W	0x00000000	The distance between point1 and point2 for light 0
ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_0	0x0150	W	0x00000000	The 3DYUV U interpolation curve of X coordinate for light 0
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_0	0x0154	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 0
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_0	0x0158	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 0
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_0	0x015C	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 0
ISP_RAWAWB_5000_YUV_X_COOR_Y_1	0x0160	W	0x00000000	The Y coordinate of point1 and vector point21 for light 1
ISP_RAWAWB_5000_YUV_X_COOR_U_1	0x0164	W	0x00000000	The U coordinate of point1 and vector point21 for light 1
ISP_RAWAWB_5000_YUV_X_COOR_V_1	0x0168	W	0x00000000	The V coordinate of point1 and vector point21 for light 1

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_YUV_X1X2_DIS_1	0x016C	W	0x00000000	The distance between point1 and point2 for light 1
ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_1	0x0170	W	0x00000000	The 3DYUV U interpolation curve of X coordinate for light 1
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_1	0x0174	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 1
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_1	0x0178	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 1
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_1	0x017C	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 1
ISP_RAWAWB_5000_YUV_X_COOR_Y_2	0x0180	W	0x00000000	The Y coordinate of point1 and vector point21 for light 2
ISP_RAWAWB_5000_YUV_X_COOR_U_2	0x0184	W	0x00000000	The U coordinate of point1 and vector point21 for light 2
ISP_RAWAWB_5000_YUV_X_COOR_V_2	0x0188	W	0x00000000	The V coordinate of point1 and vector point21 for light 2
ISP_RAWAWB_5000_YUV_X1X2_DIS_2	0x018C	W	0x00000000	The distance between point1 and point2 for light 2
ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_2	0x0190	W	0x00000000	The 3DYUV U interpolation curve of X coordinate for light 2
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_2	0x0194	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 2
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_2	0x0198	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 2
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_2	0x019C	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 2
ISP_RAWAWB_5000_YUV_X_COOR_Y_3	0x01A0	W	0x00000000	The Y coordinate of point1 and vector point21 for light 3
ISP_RAWAWB_5000_YUV_X_COOR_U_3	0x01A4	W	0x00000000	The U coordinate of point1 and vector point21 for light 3
ISP_RAWAWB_5000_YUV_X_COOR_V_3	0x01A8	W	0x00000000	The V coordinate of point1 and vector point21 for light 3
ISP_RAWAWB_5000_YUV_X1X2_DIS_3	0x01AC	W	0x00000000	The distance between point1 and point2 for light 3
ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_3	0x01B0	W	0x00000000	The 3DYUV U interpolation curve of X coordinate for light 3
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_3	0x01B4	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 3
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_3	0x01B8	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 3
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_3	0x01BC	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 3
ISP_RAWAWB_5000_RGB2XY_WT01	0x01FC	W	0x00000000	RGB2XY weight matrix, coefficient 01
ISP_RAWAWB_5000_RGB2XY_WT2	0x0200	W	0x00000000	RGB2XY weight matrix, coefficient 2
ISP_RAWAWB_5000_RGB2XY_MAT0_XY	0x0204	W	0x00000000	RGB2XY, rotation matrix, first column XY
ISP_RAWAWB_5000_RGB2XY_MAT1_XY	0x0208	W	0x00000000	RGB2XY, rotation matrix, second column XY

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_RGB2XY_MAT2_XY	0x020C	W	0x00000000	RGB2XY, rotation matrix, third column XY
ISP_RAWAWB_5000_XY_DETC_NOR_X_0	0x0210	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_0	0x0214	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_0	0x0218	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_0	0x021C	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_1	0x0228	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_1	0x022C	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_1	0x0230	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_1	0x0234	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_2	0x0240	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_2	0x0244	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_2	0x0248	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_2	0x024C	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_3	0x0258	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_3	0x025C	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_3	0x0260	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_3	0x0264	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_MULTIWINDOW_EXC_CTRL	0x02B8	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW0_OFFS	0x02BC	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW0_SIZE	0x02C0	W	0x00000000	The horizontal and vertical size of multi-window
ISP_RAWAWB_5000_MULTIWINDOW1_OFFS	0x02C4	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW1_SIZE	0x02C8	W	0x00000000	The horizontal and vertical size of multi-window
ISP_RAWAWB_5000_MULTIWINDOW2_OFFS	0x02CC	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW2_SIZE	0x02D0	W	0x00000000	The horizontal and vertical size of multi-window
ISP_RAWAWB_5000_MULTIWINDOW3_OFFS	0x02D4	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW3_SIZE	0x02D8	W	0x00000000	The horizontal and vertical size of multi-window
ISP_RAWAWB_5000_EXC_WP_REGION0_XU	0x02FC	W	0x00000000	The left and right boundary of exclude region in UV or XY range

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_EXC_WP_REGION0_YV	0x0300	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION1_XU	0x0304	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION1_YV	0x0308	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION2_XU	0x030C	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION2_YV	0x0310	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION3_XU	0x0314	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION3_YV	0x0318	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION4_XU	0x031C	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION4_YV	0x0320	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION5_XU	0x0324	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION5_YV	0x0328	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION6_XU	0x032C	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION6_YV	0x0330	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_WEIGHT0_3	0x0334	W	0x3F3F3F3F	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_WEIGHT4_6	0x0338	W	0x003F3F3F	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_SUM_RGAIN_NOR_0	0x0340	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_0	0x0348	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_NOR_0	0x034C	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_0	0x0350	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_0	0x0358	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_BIG_0	0x035C	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_1	0x0370	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_1	0x0378	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_NOR_1	0x037C	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_1	0x0380	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_1	0x0388	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_BIG_1	0x038C	W	0x00000000	White point sum number with Y-weight and block weight

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_SUM_RGAIN_NOR_2	0x03A0	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_2	0x03A8	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_NOR_2	0x03AC	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_2	0x03B0	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_2	0x03B8	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_BIG_2	0x03BC	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_3	0x03D0	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_3	0x03D8	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_NOR_3	0x03DC	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_3	0x03E0	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_3	0x03E8	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_BIG_3	0x03EC	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_R_EXC_0	0x05E0	W	0x00000000	R-gain sum in the exclude range
ISP_RAWAWB_5000_SUM_B_EXC_0	0x05E8	W	0x00000000	B-gain sum in the exclude range
ISP_RAWAWB_5000_WP_NM_EXC_0	0x05EC	W	0x00000000	White point in the exclude range
ISP_RAWAWB_5000_SUM_R_EXC_1	0x05F0	W	0x00000000	R-gain sum in the exclude range
ISP_RAWAWB_5000_SUM_B_EXC_1	0x05F8	W	0x00000000	B-gain sum in the exclude range
ISP_RAWAWB_5000_WP_NM_EXC_1	0x05FC	W	0x00000000	White point in the exclude range
ISP_RAWAWB_5000_SUM_R_EXC_2	0x0600	W	0x00000000	R-gain sum in the exclude range
ISP_RAWAWB_5000_SUM_B_EXC_2	0x0608	W	0x00000000	B-gain sum in the exclude range
ISP_RAWAWB_5000_WP_NM_EXC_2	0x060C	W	0x00000000	White point in the exclude range
ISP_RAWAWB_5000_SUM_R_EXC_3	0x0610	W	0x00000000	R-gain sum in the exclude range
ISP_RAWAWB_5000_SUM_B_EXC_3	0x0618	W	0x00000000	B-gain sum in the exclude range
ISP_RAWAWB_5000_WP_NM_EXC_3	0x061C	W	0x00000000	White point in the exclude range
ISP_RAWAWB_5000_Y_HIST01	0x0620	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_Y_HIST23	0x0624	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_Y_HIST45	0x0628	W	0x00000000	Y HIST bin

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_Y_HIST67	0x062C	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_WPNUM2_0	0x0630	W	0x00000000	White pixel num2
ISP_RAWAWB_5000_WPNUM2_1	0x0634	W	0x00000000	White pixel num2
ISP_RAWAWB_5000_WPNUM2_2	0x0638	W	0x00000000	White pixel num2
ISP_RAWAWB_5000_WPNUM2_3	0x063C	W	0x00000000	White pixel num2
ISP_RAWAWB_5000_RAM_CTRL	0x0650	W	0x00000000	Control of reading ram
ISP_RAWAWB_5000_WRAM_CTRL	0x0654	W	0x00000000	Control of BLK weight ram
ISP_RAWAWB_5000_WIN_WEIGHT_0	0x0660	W	0x00000000	The Weight of BLK00-BLK04 system.
ISP_RAWAWB_5000_WIN_WEIGHT_1	0x0664	W	0x00000000	The Weight of BLK10-BLK14 system.
ISP_RAWAWB_5000_WIN_WEIGHT_2	0x0668	W	0x00000000	The Weight of BLK20-BLK24 system.
ISP_RAWAWB_5000_WIN_WEIGHT_3	0x066C	W	0x00000000	The Weight of BLK30-BLK34 system.
ISP_RAWAWB_5000_WIN_WEIGHT_4	0x0670	W	0x00000000	The Weight of BLK40-BLK44 system.
ISP_RAWAWB_5000_REG_DATA_BASE	0x0700	W	0x00000000	Data read from reg

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.30 RAWHIST

Name	Offset	Size	Reset Value	Description
ISP_RAWHIST_BIG_4800_4A00_4B00_CTRL	0x0000	W	0x20000000	Histogram properties
ISP_RAWHIST_BIG_4800_4A00_4B00_SIZE	0x0004	W	0x00000000	Horizontal (sub-)window size
ISP_RAWHIST_BIG_4800_4A00_4B00_OFFS	0x0008	W	0x00000000	Histogram window horizontal offset
ISP_RAWHIST_BIG_4800_4A00_4B00_HRAM_CTRL	0x000C	W	0x00000000	HRAM address offset
ISP_RAWHIST_BIG_4800_4A00_4B00_RAW2Y_CC	0x0010	W	0x000D2021	The offset of RAW2Y formula
ISP_RAWHIST_BIG_4800_4A00_4B00_WRAM_CTRL	0x0014	W	0x00000000	RAM offset for write or read
ISP_RAWHIST_BIG_4800_4A00_4B00_WEIGHT_BASE	0x0040	W	0x20820820	Weighting factor for sub-windows total 25 factor
ISP_RAWHIST_BIG_4800_4A00_4B00_RO_BASE_BIN	0x0080	W	0x00000000	Histogram measurement result bin 0..255(total 256)

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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Name	Offset	Size	Reset Value	Description
ISP_RAWHIST_LITE_4900_CTRL	0x0000	W	0x00000000	Histogram properties
ISP_RAWHIST_LITE_4900_SIZE	0x0004	W	0x00000000	Horizontal (sub-)window size
ISP_RAWHIST_LITE_4900_OFFS	0x0008	W	0x00000000	Histogram window horizontal offset
ISP_RAWHIST_LITE_4900_RAM_CTRL	0x000C	W	0x00000000	RAM address offset
ISP_RAWHIST_LITE_4900_RAW2Y_CC	0x0010	W	0x000D2021	The offset of RAW2Y formula
ISP_RAWHIST_LITE_4900_WEIGHT_0	0x0040	W	0x20202020	Weighting factor for sub-windows total 25 factor
ISP_RAWHIST_LITE_4900_RO_BASE_BIN	0x0080	W	0x00000000	Histogram measurement result bin 0..63(total 64)

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.1.31 IMG_EFF

Name	Offset	Size	Reset Value	Description
IMG_EFF_0200_IMG_EFF_CTRL	0x0000	W	0x00000000	Img_eff_ctrl
IMG_EFF_0200_IMG_EFF_COLOR_SEL	0x0004	W	0x00000000	Img_eff_color_sel
IMG_EFF_0200_IMG_EFF_TINT	0x001C	W	0x0000880C	Img_eff_tint
IMG_EFF_0200_IMG_EFF_CTRL_SHD	0x0020	W	0x00000000	Img_eff_ctrl_shd

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.2 Detail Registers Description

2.4.2.1 MIPI

CSI2RX_1C00_CTRL0

Address: Operational Base(0xFF3F1C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	sw_dma_2frm_mode Raw read back two/three frames mode, only the last frame valid 2'b00: Normal one frame mode 2'b01: Two frame mode 2'b10: Three frame mode 2'b11: Reserved
11:8	RW	0x0	sw_ibuf_op_mode 4'h0: Normal_mode (no hdr). 4'h4: Raw_rdback_frame1(start use sw_dma_rdback_p) 4'h5: Hdr_rdback_frame2 (start use sw_dma_rdback_p) 4'h6: Hdr_rdback_frame3 (start use sw_dma_rdback_p) 4'h8: Hdr_frame_linex2_ddr_mode 4'h12: Hdr_frame_linex3_ddr_mode Others: Reserved
7	RW	0x0	sw_ibuf_op_frame_stmode Op_mode=8,12 framex2/x3 start mode 1'b0: RawS frame_st then start 1'b1: RawM/L frame_end then start
6:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_csi_2pix_dis Ibuf in and out pixel mode 1'b1: One pixel mode 1'b0: Two pixel mode
0	RW	0x0	sw_csi2rx_en_p Csi rx read enable under hdr debug mode, auto-clear Note: CTRL0[0] read back is mipi readback working

CSI2RX_1C00_CTRL1

Address: Operational Base(0xFF3F1C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	ro_csi2rx_enable Mipi mode enable (~sw_dvp_mode)
29:28	RW	0x0	sw_ibuf_lvl1_sel2 Ibuf2_m select 2'b00: Ibuf2_m_i 2'b01: Ibuf1_l_i 2'b10: Ibuf0_s_i
27:26	RW	0x0	sw_ibuf_lvl1_sel1 Ibuf1_l select 2'b00: Ibuf1_l_i 2'b01: Ibuf0_s_i 2'b10: Ibuf2_m_i
25:24	RW	0x0	sw_ibuf_lvl1_sel0 Ibuf0_s select 2'b00: Ibuf0_s_i 2'b01: Ibuf1_l_i 2'b10: Ibuf2_m_i
23	RW	0x0	sw_ibuf_lvl0_sel3 Ibuf3_r_i select 1'b0: Csi0_mipi[chan3_sel] 1'b1: Raw2_mipi(from DDR)
22	RW	0x0	sw_ibuf_lvl0_sel2 Ibuf2_l_i select 1'b0: Csi0_mipi[chan2_sel] 1'b1: Raw1_mipi(from DDR)
21	RW	0x0	sw_ibuf_lvl0_sel1 Ibuf1_l_i select 1'b0: Csi0_mipi[chan1_sel] 1'b1: Raw0_mipi(from DDR)
20	RW	0x0	sw_ibuf_lvl0_sel0 Ibuf0_s_i select 1'b0: Csi0_mipi[chan0_sel] 1'b1: Csi1_mipi[chan0_sel]
19	RO	0x0	reserved
18:16	RW	0x3	sw_csi_chan3_sel Csi0_mipi[7:0] chan3 select
15	RO	0x0	reserved
14:12	RW	0x2	sw_csi_chan2_sel Csi0_mipi[7:0] chan2 select
11	RO	0x0	reserved
10:8	RW	0x1	sw_csi_chan1_sel Csi0_mipi[7:0] chan1 select
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	sw_csi_chan0_sel Csi0_mipi[7:0] + csi1_mipi[7:0] chan0 select
3:2	RO	0x0	reserved
1:0	RW	0x3	sw_csi_lane Number of active data lanes 2'b00: 1 data lane (lane 0) 2'b01: 2 data lanes (lanes 0 and 1) 2'b10: 3 data lanes (lanes 0, 1, and 2) 2'b11: 4 data lanes (All) Can only be updated when the D-PHY lane is in Stop state. Value after Reset: CSI2_HOST_NUMBER_OF_LANES-1 = 0x3

CSI2RX_1C00_CTRL2

Address: Operational Base(0xFF3F1C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_ibuf_hblank_count Mipi in buffer horizontal blank counter
23:20	RW	0x0	sw_rdbak_hold_diff Raw readback hold diff value for pipeline full
19:14	RO	0x00	reserved
13:0	RW	0x0000	sw_csi_isp_linecnt Isp line counter reach interrupt for ro_err3[15]

CSI2RX_1C00_CTRL3

Address: Operational Base(0xFF3F1C00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_ibuf_hold_watermark HDR input buffer hold watermark. For ddr read hold, to control read rate. For example, image resolution 1920x1080, configure sw_ibuf_hold_watermark = 1920 / 2 = 960. Note: sw_ibuf_hold_watermark Only used in hdr line mode, otherwise default sw_ibuf_hold_watermark = 0.

CSI2RX_1C00_CSI2_RESETN

Address: Operational Base(0xFF3F1C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_csi_delete_2pix_dis Disable delete mipi_hsync for invalid 2pixel at line end
30:2	RO	0x00000000	reserved
1	R/WSC	0x1	sw_csi_fifo_clr_n Fifo clear. Active Low. Auto-clear Write then clear
0	R/WSC	0x1	sw_csi_rxbyte_rst_n Reset output. Active Low. Auto-clear Write then clear

CSI2RX_1C00_DATA_IDS_1

Address: Operational Base(0xFF3F1C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x2b	sw_csi_id0 Data ID 0 [dt0_vc[1:0], dt0_dt[5:0]] Channel 0

CSI2RX_1C00_ERR_OVERFLOW

Address: Operational Base(0xFF3F1C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RC	0x0	ibuf3r_overflow Ibuf_r_fifo overflow
18:16	RC	0x0	ibufx3_overflow Ibufx3 overflow [0]: ibuf_s_fifo overflow [1]: ibuf_l_fifo overflow [2]: ibuf_m_fifo overflow
15	RO	0x0	reserved
14	RC	0x0	afifo22_overflow Afifo22 overflow
13	RC	0x0	afifo21_overflow Afifo21 overflow
12	RC	0x0	afifo20_overflow Afifo20 overflow
11:0	RO	0x000	reserved

CSI2RX_1C00_ERR_STAT

Address: Operational Base(0xFF3F1C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	mipi_drop_frm Mipi drop frame state
30:17	RO	0x0000	reserved
16	RC	0x0	mipi_linecnt Line counter number reach the sw_csi_isp_linecnt
15:7	RO	0x000	reserved
6	RC	0x0	raw2_rd_frame_end Raw2 read data frame end
5	RC	0x0	raw1_rd_frame_end Raw1 read data frame end
4	RC	0x0	raw0_rd_frame_end Raw0 read data frame end
3:0	RO	0x0	reserved

CSI2RX_1C00_MASK_OVERFLOW

Address: Operational Base(0xFF3F1C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	sw_imsk_ibuf3r_overflow Mask for ibuf_r_fifo overflow
18:16	RW	0x0	sw_imsk_ibufx3_overflow Mask for ibufx3 overflow [0]: ibuf_s_fifo overflow [1]: ibuf_l_fifo overflow [2]: ibuf_m_fifo overflow
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	sw_imsk_afifo22_overflow Mask for afifo22 overflow
13	RW	0x0	sw_imsk_afifo21_overflow Mask for afifo21 overflow
12	RW	0x0	sw_imsk_afifo20_overflow Mask for afifo20 overflow
11:0	RO	0x000	reserved

CSI2RX_1C00_MASK_STAT

Address: Operational Base(0xFF3F1C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_imsk_mipi_drop_frm Mask for mipi drop frame state
30:17	RO	0x0000	reserved
16	RW	0x0	sw_imsk_csi_isp_linecnt Mask for line counter number reach the sw_csi_isp_linecnt
15:7	RO	0x000	reserved
6	RW	0x0	sw_imsk_raw2_rd_frame_end Mask for raw2_rd data frame_end
5	RW	0x0	sw_imsk_raw1_rd_frame_end Mask for raw_rd1 data frame_end
4	RW	0x0	sw_imsk_raw0_rd_frame_end Mask for raw_rd0 data frame_end
3:0	RO	0x0	reserved

CSI2RX_1C00_RAW_RD_CTRL

Address: Operational Base(0xFF3F1C00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_rxself_force_upd All mipi rx self force update Note: If readback this register, it's mipi working.
30:8	RO	0x000000	reserved
7:5	RW	0x0	sw_csi_raw_rd_chan_sel Raw_rd sw_csi_id_7to0 id input id select, default id0
4	RW	0x0	sw_csi_raw_rd_align Raw_rd pix-out align mode 1'b0: big-endian 1'b1: little-endian
3	RW	0x0	sw_csi_raw_rd_uncompact Raw_rd pix-out simg_mod enable
2	RW	0x0	sw_csi_raw2_rd_en_org Raw_rd1 enable Auto clear when finish
1	RW	0x0	sw_csi_raw1_rd_en_org Raw_rd1 enable Auto clear when finish
0	RW	0x0	sw_csi_raw0_rd_en_org Raw_rd0 enable Auto clear when finish

CSI2RX_1C00_RAW_RD_LINECNT_RO

Address: Operational Base(0xFF3F1C00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RO	0x0000	ro_raw1_rd_isp_line_cnt Current raw_rd1 to isp line counter
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_raw0_rd_isp_line_cnt Current raw_rd0 to isp line counter

CSI2RX_1C00_RAW_RD_PIC_SIZE

Address: Operational Base(0xFF3F1C00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw_rd_v_size_org If (sw_csi_raw_rd_v_size_org equal 0), use regs_acq_v_size value.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw_rd_h_size_org If (sw_csi_raw_rd_h_size_org equal 0), use regs_acq_h_size value.

CSI2RX_1C00_RAW2_RD_LINECNT_RO

Address: Operational Base(0xFF3F1C00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	ro_raw2_rd_isp_line_cnt Current raw2_rd to isp line counter

CSI2RX_1C00_ISP_LINECNT_RO

Address: Operational Base(0xFF3F1C00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	ro_csi_isp_line_cnt Current csi to isp line counter

CSI2RX_1C00_RAW_WR_IBUF_STATUS_RO

Address: Operational Base(0xFF3F1C00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	ro_ibuf3_debug_status ibuf working debug status, mipi_clk

CSI2RX_1C00_FPN_CTRL

Address: Operational Base(0xFF3F1C00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	sw_fpn_bits Calculate data bits selection 2'b00: [3'b000, x] 2'b01: [2'b00, x, 1'b0] 2'b10: [1'b0, x, 2'b00] 2'b11: [x, 3'b000] Note: "x" is 4 bits data, frame FPN_TABLE_DATA
1	RW	0x0	sw_cfpn_n Column fpn enable, active low 1'b0: Col fpn 1'b1: Row fpn

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_fpn_en FPN enable 1'b0: Disable 1'b1: Enable

CSI2RX_1C00_FPN_TABLE_CTRL

Address: Operational Base(0xFF3F1C00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	sw_fpn_cfg_ing Write fpn data to memory, active high 1'b0: Disable/finish configuration 1'b1: Write table data to memory enable

CSI2RX_1C00_FPN_TABLE_DATA0

Address: Operational Base(0xFF3F1C00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_fpn0_table_data FPN data register to memory

CSI2RX_1C00_FPN_TABLE_DATA1

Address: Operational Base(0xFF3F1C00) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_fpn1_table_data FPN data register to memory

CSI2RX_1C00_VERSION

Address: Operational Base(0xFF3F1C00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x02013323	version_id Version of the DWC_mipi_csi2_host Value after Reset: 32'h02013323 Integrated in ISP (max: 02, min: 01, svn: 23323)

2.4.2.2 MMU

MMU_DTE_ADDR

Address: Operational Base(0xFF3F7F00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page Table address

MMU_STATUS

Address: Operational Base(0xFF3F7F00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	page_fault_bus_id Index of master reponsible for last page fault.
5	RO	0x0	page_fault_is_write The direction of access for last page fault 1'b0: Read 1'b1: Write
4	RO	0x0	replay_buffer_empty The MMU replay buffer is empty

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Bit	Attr	Reset Value	Description
3	RO	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses
2	RO	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command
0	RO	0x0	paging_enabled Paging is enabled

MMU_COMMAND

Address: Operational Base(0xFF3F7F00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	mmu_cmd MMU_CMD. This can be 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

MMU_PAGE_FAULT_ADDR

Address: Operational Base(0xFF3F7F00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	page_fault_addr Address of last page fault.

MMU_ZAP_ONE_LINE

Address: Operational Base(0xFF3F7F00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

MMU_INT_RAWSTAT

Address: Operational Base(0xFF3F7F00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

MMU_INT_CLEAR

Address: Operational Base(0xFF3F7F00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	read_bus_error Read bus error
0	WO	0x0	page_fault Page fault

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MMU_INT_MASK

Address: Operational Base(0xFF3F7F00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

MMU_INT_STATUS

Address: Operational Base(0xFF3F7F00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	read_bus_error Read bus error
0	RO	0x0	page_fault Page fault

MMU_AUTO_GATING

Address: Operational Base(0xFF3F7F00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RW	0x1	sw_mmu_old_en mmu old version enable, need set 1.
30:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self.

2.4.2.3 MI

MI_1400_MI_WR_CTRL

Address: Operational Base(0xFF3F1400) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x2	sw_sp_wr_output_format Selects output format of self picture. For possible restrictions see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". 3'b111: RGB 888 3'b110: ARGB 888 3'b101: RGB 666 3'b100: RGB 565 3'b011: YCbCr 4:4:4 3'b010: YCbCr 4:2:2 3'b001: YCbCr 4:2:0 3'b000: YCbCr 4:0:0 Note: - Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path. - For RGB output format the SP input format must be YCbCr 4:2:2 -For ARGB888 format, Alpha is configurable (15f8[23:16]). - If sw_sp_wr_v_flip = 1 and yuv420 format, need to configure sw_sp_wr_output_format = 1.

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Bit	Attr	Reset Value	Description
27:26	RW	0x0	sw_sp_wr_input_format Selects input format of self picture. For possible restrictions see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". 2'b11: YCbCr 4:4:4 2'b10: YCbCr 4:2:2 2'b01: YCbCr 4:2:0 2'b00: YCbCr 4:0:0 Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
25:24	RW	0x0	sw_sp_wr_format Defines how YCbCr self picture data is written to memory. Must be set to 00 if RGB conversion is active. Note that with RGB conversion active the output format is always interleaved. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
23:22	RW	0x0	sw_mp_wr_format Defines how YCbCr main picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.
21	RW	0x0	sw_mi_wr_init_offset_en Enables updating of the offset counters shadow registers for raw path to the programmed register initial values. The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into raw picture. So only the corresponding raw shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
20	RW	0x0	sw_mi_wr_init_base_en Enables updating of the base address and buffer size shadow registers for main and self picture to the programmed register initial values. MI_MP/SP_Y/CB/CR_BASE_AD_INIT -> MI_MP/SP_Y/CB/CR_BASE_AD_SHD MI_MP/SP_Y/CB/CR_SIZE_INIT -> MI_MP/SP_Y/CB/CR_SIZE_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into main and self picture. So only the corresponding main/self shadow registers are affected.

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Bit	Attr	Reset Value	Description
19:18	RW	0x2	sw_mi_wr_burst_len_chrom_org Burst length for Cb or Cr data affecting write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported. If rotation is active, then only 4-beat bursts will be generated in self path, regardless of the setting here. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
17:16	RW	0x2	sw_mi_wr_burst_len_lum_org Burst length for Y data affecting write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
15	RW	0x0	sw_mi_wr_last_pixel_sig_en Enables the last pixel signalization 1'b1: Enabled 1'b0: Disabled
14	RW	0x0	sw_sp_wr_auto_upd Automatic update of configuration registers for self path at frame end. 1'b1: Enabled 1'b0: Disabled
13	RW	0x0	sw_mp_wr_auto_upd Automatic update of configuration registers for main path at frame end. 1'b1: Enabled 1'b0: Disabled Note: If mp pingpong enable, it needs to be set "1".
12	RW	0x0	sw_sp_wr_pingpong_en Pingpong mode of configuration registers for self path at frame end. 1'b1: Enabled 1'b0: Disabled
11	RW	0x0	sw_mp_wr_pingpong_en Pingpong mode of configuration registers for main path at frame end. 1'b1: Enabled 1'b0: Disabled

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Bit	Attr	Reset Value	Description
10	RW	0x0	sw_mi_wr_422noncosited Enables self path YCbCr422non-co-sited -> YCbCr444 interpolation (M5_v6, M5_v7 only) 1'b1: YCbCr422 data are non_co-sited (Cb and Cr samples are centered between Y samples) so modified interpolation is activated 1'b0: YCbCr422 data are co-sited (Y0 Cb0 and Cr0 are sampled at the same position) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
9	RW	0x0	sw_mi_wr_cbcr_full_range Enables CbCr full range for self path YCbCr -> RGB conversion (M5_v6, M5_v7 only) 1'b1: CbCr have full range (0..255) 1'b0: CbCr have compressed range range (16..240) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
8	RW	0x0	sw_mi_wr_y_full_range Enables Y full range for self path YCbCr -> RGB conversion (M5_v6, M5_v7 only) 1'b1: Y has full range (0..255) 1'b0: Y has compressed range (16..235) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
7	RW	0x0	sw_mi_wr_byte_swap Enable uv swap function YVYU mode: 1'b0: YVYU (U,LSB) 1'b1: YUYV (V,LSB) YUV-SP mode: 1'b0: VU (U,LSB) 1'b1: UV (V,LSB)
6:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_mi_wr_path_enable Enable data paths of MI according to the following table: 4'h0: Disabled, no data is transferred 4'h1: YUV data output, main-path only (mp_enable only) 4'h2: Self-path only, output data format depending on other settings (sp_enable only) 4'h3: YUV data output in main-path and self-path image data active 4'h4: JPEG data output, main-path only (jpeg_enable only) 4'h5: Not allowed 4'h6: JPEG data output in main-path and self-path image data active 4'h7: Not allowed 4'h8: RAW data output, main-path only (raw_enable only) 4'h9: Defect pixel data on self-path, image data on main-path 4'h10: Defect pixel data on main-path, image data on self-path 4'h11: Not allowed 4'h12: Defect pixel data on self-path, JPEG data on main-path 4'h13: Defect pixel data on main-path only 4'h14: Defect pixel data on self-path only 4'h15: Defect pixel data on self-path, RAW data on main-path Programmed value becomes effective (visible in shadow register) after a soft reset, a forced software update or an automatic configuration update. Affects MI_IN and MI_OUT module.

MI_1400_MI_WR_INIT

Address: Operational Base(0xFF3F1400) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sw_mi_update_last_pixel_en If this bit set 1, MI IN and MI OUT module will update at the time of dual crop module sent out the last pixel
5	RW	0x1	sw_mi_update_mode 1'b0: Old mode 1'b1: New mode, all path will update when frame_end In new mode, all path registers of MI will be updated at right time; (Not support input RAW/JEPG mode)
4	W1C	0x0	sys_mi_cfg_upd Forced configuration update. Leads to an immediate update of the shadow registers. Depending on the two initial enable bits in the MI_CTRL register (init_offset_en and init_base_en) the offset counter, base address and buffer size shadow registers are also updated.
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	W1C	0x0	sw_mi_skip Skip of current or next starting main picture: Aborts writing of main picture image data of the current frame to RAM (after the current burst transmission has been completed). Further main picture data up to the end of the current frame are discarded. No further macro block line interrupt (mblk_line), no wrap around interrupt for main picture (wrap_mp_y/cb/cr) and no fill level interrupt (fill_mp_y) are generated. Skip does not affect the generation of the main path frame end interrupt (mp_frame_end). Skip does not affect the processing of self picture and its corresponding interrupts namely the self path frame end interrupt (sp_frame_end). The byte counter (register MI_WR_BYTE_CNT) is not affected. It produces the correct number of JPEG or RAW data bytes at the end of the current (skipped) frame. After a skip has been performed the offset counter for the main picture at the start of the following frame are set depending on the bit init_offset_en in register MI_WR_CTRL: - Skip restart mode (init_offset_en = 0) The offset counters of the main picture are restarted at the old start values of the previous skipped frame. - Skip initial mode (init_offset_en = 1) The offset counters of the main picture are initialized with the register contents of the offset counter initial registers without any additional forced software update or automatic configuration update.
1:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_Y_BASE_AD_INIT --- Note: This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write (MI_MP_Y_BASE_AD_INIT, address_value) is equivalent to write(MI_MP_Y_BASE_AD_INIT, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is NOT recommended to use non-aligned address values for access. It is also NOT recommended to actively consider the register slice for register access in order to avoid unnecessary mask and shift operations. In addition, if camera IC provides AXI interfaces the programmed base address shall be burst aligned with respect to the burst length configured in MI_WR_CTRL. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

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MI_1400_MI_MP_WR_Y_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_size Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_Y_SIZE_INIT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT

Address: Operational Base(0xFF3F1400) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_offs_cnt Offset counter initial value of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_WR_Y_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT_START

Address: Operational Base(0xFF3F1400) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Y component, JPEG or raw data). Updated at frame end. Note: A soft reset resets the contents to the reset value. --- MI_MP_WR_Y_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS

Address: Operational Base(0xFF3F1400) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:4	RW	0x0000000	sw_mp_wr_y_irq_offs Reaching this programmed value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_WR_Y_IRQ_OFFS --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE

Address: Operational Base(0xFF3F1400) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base Base address of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cb_size Size of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT

Address: Operational Base(0xFF3F1400) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RW	0x000000	sw_mp_wr_cb_offs_cnt Offset counter initial value of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes. --- MI_MP_WR_CB_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT_START

Address: Operational Base(0xFF3F1400) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Cb component). Updated at frame end. --- MI_MP_WR_CB_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE

Address: Operational Base(0xFF3F1400) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base Base address of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RW	0x000000	sw_mp_wr_cr_size Size of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT

Address: Operational Base(0xFF3F1400) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cr_offs_cnt Offset counter initial value of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes. --- MI_MP_WR_CR_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT_START

Address: Operational Base(0xFF3F1400) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Cr component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CR_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE

Address: Operational Base(0xFF3F1400) + offset (0x003C)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_y_base Base address of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_sp_wr_y_size Size of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT

Address: Operational Base(0xFF3F1400) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_sp_wr_y_offs_cnt Offset counter initial value of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT_START

Address: Operational Base(0xFF3F1400) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:4	RO	0x0000000	sw_sp_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Y component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_LLENGTH

Address: Operational Base(0xFF3F1400) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_sp_wr_y_llength_tmp Line length of self picture Y component or RGB picture in pixel, also known as line stride. If no line stride is used, line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 16, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the line length of the Cb and Cr component is assumed the same size. Note: Line length always refers to the line length of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path. If ARGB888 vflip, you need to configure sw_sp_wr_y_llength_tmp to be the self picture width, which will be multiplied by 4 inside the hardware (argb storage format).

MI_1400_MI_SP_WR_CB_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_cb_base Base address of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RW	0x000000	sw_sp_wr_cb_size Size of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT

Address: Operational Base(0xFF3F1400) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_cb_offs_cnt_init Offset counter initial value of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT_START

Address: Operational Base(0xFF3F1400) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Cb component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0060)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_cr_base Base address of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_wr_cr_size Size of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT

Address: Operational Base(0xFF3F1400) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_wr_cr_offs_cnt Offset counter initial value of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT_START

Address: Operational Base(0xFF3F1400) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RO	0x000000	sw_sp_wr_cr_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Cr component). Updated at frame end. --- MI_SP_WR_CR_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_WR_BYTE_CNT

Address: Operational Base(0xFF3F1400) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	byte_cnt Counter value specifies the number of JPEG or RAW data bytes of the last transmitted frame. Updated at frame end. A soft reset will set the byte counter to zero.

MI_1400_MI_WR_CTRL_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	path_enable_out Path_enable shadow register for module MI_OUT (former raw_enable_out, jpeg_enable_out, sp_enable_out, mp_enable_out)
15:4	RO	0x000	reserved
3:0	RO	0x0	path_enable_in Path_enable shadow register for module MI_IN (former raw_enable_in, jpeg_enable_in, sp_enable_in, mp_enable_in)

MI_1400_MI_MP_WR_Y_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_y_base_shd Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_SIZE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_size_shd Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT_SHD

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Address: Operational Base(0xFF3F1400) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_offs_cnt_shd Current offset counter of main picture Y component, JPEG or raw data ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_irq_offs_shd Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_cb_base_shd Base address of main picture Cb component ring buffer. --- MI_MP_WR_CB_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_SIZE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cb_size_shd Size of main picture Cb component ring buffer. --- MI_MP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RO	0x000000	sw_mp_wr_cb_offs_cnt_shd Current offset counter of main picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_cr_base_shd Base address of main picture Cr component ring buffer. --- MI_MP_CR_BASE_AD_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_SIZE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_size_shd Size of main picture Cr component ring buffer. --- MI_MP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT_SHD

Address: Operational Base(0xFF3F1400) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_offs_cnt_shd Current offset counter of main picture Cr component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_y_base_shd Base address of self picture Y component ring buffer. --- MI_SP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_SIZE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00A4)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_wr_y_size_shd Size of self picture Y component ring buffer. --- MI_SP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_wr_y_offs_cnt_shd Current offset counter of self picture Y component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_BASE_AD_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_cb_base_shd Base address of self picture Cb component ring buffer. --- MI_SP_WR_CB_BASE_AD_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_SIZE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_size_shd Size of self picture Cb component ring buffer. --- MI_SP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_offs_cnt_shd Current offset counter of self picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

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MI_1400_MI_SP_WR_CR_BASE_AD_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_cr_base_shd Base address of self picture Cr component ring buffer. --- MI_SP_WR_CR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_SIZE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cr_size_shd Size of self picture Cr component ring buffer. --- MI_SP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT_SHD

Address: Operational Base(0xFF3F1400) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cr_offs_cnt_shd Current offset counter of self picture Cr component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_IMSC

Address: Operational Base(0xFF3F1400) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31	RW	0x0	mpfbc_wr_frame_end Mask mpfbc write end of frame interrupt
30	RW	0x0	isp_bus_err Mask bit for isp bus error interrupt
29	RW	0x0	bpds_frame_end Mask bypass down-sampling picture end of frame interrupt
28	RW	0x0	mpds_frame_end Mask main down-sampling picture end of frame interrupt
27	RW	0x0	wrap_bp_cb Mask bit for bypass picture Cb address wrap interrupt
26	RW	0x0	wrap_bp_y Mask bit for bypass picture Y address wrap interrupt
25	RW	0x0	bp_frame_end Mask bypass path write end of frame interrupt
24	RW	0x0	bay3d_ds_frame_end Mask bay3d down scale write end of frame interrupt
23	RW	0x0	bay3d_cur_frame_end Mask bay3d current write end of frame interrupt

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Bit	Attr	Reset Value	Description
22	RW	0x0	bay3d_iir_frame_end Mask bay3d iir write end of frame interrupt
21	RW	0x0	gain_wr_frame_end Mask gain write end of frame interrupt
20	RW	0x0	dbr_wr_frame_end Mask debayer-in write end of frame interrupt
19	RW	0x0	raw3_wr_frame_end Mask raw1 tx end of frame interrupt
18	RW	0x0	raw2_wr_frame_end Mask raw2 tx end of frame interrupt
17	RW	0x0	raw1_wr_frame_end Mask raw1 tx end of frame interrupt
16	RW	0x0	raw0_wr_frame_end Mask raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RW	0x0	sw_all_frame_end_en Mask all picture end of frame interrupt
13	RW	0x0	sw_y12c_frame_end_en Mask of Y12 C COMPENT picture end of frame interrupt
12	RW	0x0	sw_y12y_frame_end_en Mask of Y12 Y COMPENT picture end of frame interrupt
11	RW	0x0	dma_ready Mask bit for dma ready interrupt
10	RW	0x0	fill_mp_y2 Mask bit for fill level interrupt 2 of main picture Y, JPEG or raw data
9	RW	0x0	wrap_sp_cr Mask bit for self picture Cr address wrap interrupt
8	RW	0x0	wrap_sp_cb Mask bit for self picture Cb address wrap interrupt
7	RW	0x0	wrap_sp_y Mask bit for self picture Y address wrap interrupt
6	RW	0x0	wrap_mp_cr Mask bit for main picture Cr address wrap interrupt
5	RW	0x0	wrap_mp_cb Mask bit for main picture Cb address wrap interrupt
4	RW	0x0	wrap_mp_y Mask bit for main picture Y address wrap interrupt
3	RW	0x0	fill_mp_y Mask bit for fill level interrupt of main picture Y, JPEG or raw data
2	RW	0x0	mblk_line Mask bit for macro block line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM)
1	RW	0x0	sp_frame_end Mask self picture end of frame interrupt
0	RW	0x0	mp_frame_end Mask main picture end of frame interrupt

MI_1400_MI_RIS

Address: Operational Base(0xFF3F1400) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31	RO	0x0	mpfbc_wr_frame_end Raw status of mpfbc write end of frame interrupt
30	RO	0x0	isp_bus_err Raw status of isp bus error interrupt

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Bit	Attr	Reset Value	Description
29	RO	0x0	bpds_frame_end Raw status of bypass down-sampling picture end of frame interrupt
28	RO	0x0	mpds_frame_end Raw status of main down-sampling picture end of frame interrupt
27	RO	0x0	wrap_bp_cb Raw status of bypass picture Cb address wrap interrupt
26	RO	0x0	wrap_bp_y Raw status of bypass picture Y address wrap interrupt
25	RO	0x0	bp_frame_end Raw status of bypass path write end of frame interrupt
24	RO	0x0	bay3d_ds_frame_end Raw status of bay3d down scale write end of frame interrupt
23	RO	0x0	bay3d_cur_frame_end Raw status of bay3d current write end of frame interrupt
22	RO	0x0	bay3d_iir_frame_end Raw status of bay3d iir write end of frame interrupt
21	RO	0x0	gain_wr_frame_end Raw status of gain write end of frame interrupt
20	RO	0x0	dbr_wr_frame_end Raw status of debayer-in write end of frame interrupt
19	RO	0x0	raw3_wr_frame_end Raw status of raw0 tx end of frame interrupt
18	RO	0x0	raw2_wr_frame_end Raw status of raw2 tx end of frame interrupt
17	RO	0x0	raw1_wr_frame_end Raw status of raw1 tx end of frame interrupt
16	RO	0x0	raw0_wr_frame_end Raw status of raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RO	0x0	ro_all_frame_end_rawsts Raw status of all picture end of frame interrupt
13	RO	0x0	ro_y12c_frame_end_rawsts Raw status of Y12 C picture end of frame interrupt
12	RO	0x0	ro_y12y_frame_end_rawsts Raw status of Y12 Y picture end of frame interrupt
11	RO	0x0	dma_ready Raw status of dma ready interrupt
10	RO	0x0	fill_mp_y2 Raw status of fill level interrupt 2 of main picture Y, JPEG or raw data
9	RO	0x0	wrap_sp_cr Raw status of self picture Cr address wrap interrupt
8	RO	0x0	wrap_sp_cb Raw status of self picture Cb address wrap interrupt
7	RO	0x0	wrap_sp_y Raw status of self picture Y address wrap interrupt
6	RO	0x0	wrap_mp_cr Raw status of main picture Cr address wrap interrupt
5	RO	0x0	wrap_mp_cb Raw status of main picture Cb address wrap interrupt
4	RO	0x0	wrap_mp_y Raw status of main picture Y address wrap interrupt

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Bit	Attr	Reset Value	Description
3	RO	0x0	fill_mp_y Raw status of fill level interrupt of main picture Y, JPEG or raw data
2	RO	0x0	mblk_line Raw status of macro block line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM, valid only for planar and semi-planar mode)
1	RO	0x0	sp_frame_end Raw status of self picture end of frame interrupt
0	RO	0x0	mp_frame_end Raw status of main picture end of frame interrupt

MI_1400_MI_MIS

Address: Operational Base(0xFF3F1400) + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	mpfbc_wr_frame_end Masked status of mpfbc write end of frame interrupt
30	RO	0x0	isp_bus_err Masked status of isp bus error interrupt
29	RO	0x0	bpds_frame_end Masked status of bypass down-sampling picture end of frame interrupt
28	RO	0x0	mpds_frame_end Masked status of main down-sampling picture end of frame interrupt
27	RO	0x0	wrap_bp_cb Masked status of bypass picture Cb address wrap interrupt
26	RO	0x0	wrap_bp_y Masked status of bypass picture Y address wrap interrupt
25	RO	0x0	bp_frame_end Masked status of bypass path write end of frame interrupt
24	RO	0x0	bay3d_ds_frame_end Masked status of bay3d down scale write end of frame interrupt
23	RO	0x0	bay3d_cur_frame_end Masked status of bay3d current write end of frame interrupt
22	RO	0x0	bay3d_iir_frame_end Masked status of bay3d iir write end of frame interrupt
21	RO	0x0	gain_wr_frame_end Masked status of gain write end of frame interrupt
20	RO	0x0	dbr_wr_frame_end Masked status of debayer-in write end of frame interrupt
19	RO	0x0	raw3_wr_frame_end Masked status of raw3 tx end of frame interrupt
18	RO	0x0	raw2_wr_frame_end Masked status of raw2 tx end of frame interrupt
17	RO	0x0	raw1_wr_frame_end Masked status of raw1 tx end of frame interrupt
16	RO	0x0	raw0_wr_frame_end Masked status of raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RO	0x0	ro_all_frame_end_sts Masked status of all picture end of frame interrupt
13	RO	0x0	ro_y12c_frame_end_sts Masked status of Y12 C picture end of frame interrupt

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Bit	Attr	Reset Value	Description
12	RO	0x0	ro_y12y_frame_end_sts Masked status of Y12 Y picture end of frame interrupt
11	RO	0x0	dma_ready Masked status of dma ready interrupt
10	RO	0x0	fill_mp_y2 Masked status of fill level interrupt 2 of main picture Y, JPEG or raw data
9	RO	0x0	wrap_sp_cr Masked status of self picture Cr address wrap interrupt
8	RO	0x0	wrap_sp_cb Masked status of self picture Cb address wrap interrupt
7	RO	0x0	wrap_sp_y Masked status of self picture Y address wrap interrupt
6	RO	0x0	wrap_mp_cr Masked status of main picture Cr address wrap interrupt
5	RO	0x0	wrap_mp_cb Masked status of main picture Cb address wrap interrupt
4	RO	0x0	wrap_mp_y Masked status of main picture Y address wrap interrupt
3	RO	0x0	fill_mp_y Masked status of fill level interrupt of main picture Y, JPEG or raw data
2	RO	0x0	mblk_line Masked status of macro block line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM, valid only for planar and semi-planar mode)
1	RO	0x0	sp_frame_end Masked status of self picture end of frame interrupt
0	RO	0x0	mp_frame_end Masked status of main picture end of frame interrupt

MI_1400_MI_ICR

Address: Operational Base(0xFF3F1400) + offset (0x0104)

Bit	Attr	Reset Value	Description
31	WO	0x0	mpfbc_wr_frame_end Clear mpfbc write end of frame interrupt
30	WO	0x0	isp_bus_err Clear isp bus error interrupt
29	WO	0x0	bpds_frame_end Clear bypass down-sampling picture end of frame interrupt
28	WO	0x0	mpds_frame_end Clear main down-sampling picture end of frame interrupt
27	WO	0x0	wrap_bp_cb Clear bypass picture Cb address wrap interrupt
26	WO	0x0	wrap_bp_y Clear bypass picture Y address wrap interrupt
25	WO	0x0	bp_frame_end Clear bypass path write end of frame interrupt
24	WO	0x0	bay3d_ds_frame_end Clear bay3d down scale write end of frame interrupt
23	WO	0x0	bay3d_cur_frame_end Clear bay3d current write end of frame interrupt
22	WO	0x0	bay3d_iir_frame_end Clear bay3d iir write end of frame interrupt

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Bit	Attr	Reset Value	Description
21	WO	0x0	gain_wr_frame_end Clear gain write end of frame interrupt
20	WO	0x0	dbr_wr_frame_end Clear debayer-in write end of frame interrupt
19	WO	0x0	raw3_wr_frame_end Clear raw3 tx end of frame interrupt
18	WO	0x0	raw2_wr_frame_end Clear raw2 tx end of frame interrupt
17	WO	0x0	raw1_wr_frame_end Clear raw1 tx end of frame interrupt
16	WO	0x0	raw0_wr_frame_end Clear raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	WO	0x0	sw_all_frame_end_clr Clear all picture end of frame interrupt
13	WO	0x0	sw_y12c_frame_end_clr Clear Y12 C picture end of frame interrupt
12	WO	0x0	sw_y12y_frame_end_clr Clear Y12 Y picture end of frame interrupt
11	WO	0x0	dma_ready Clear dma ready interrupt
10	WO	0x0	fill_mp_y2 Clear fill level interrupt 2
9	WO	0x0	wrap_sp_cr Clear self picture Cr address wrap interrupt
8	WO	0x0	wrap_sp_cb Clear self picture Cb address wrap interrupt
7	WO	0x0	wrap_sp_y Clear self picture Y address wrap interrupt
6	WO	0x0	wrap_mp_cr Clear main picture Cr address wrap interrupt
5	WO	0x0	wrap_mp_cb Clear main picture Cb address wrap interrupt
4	WO	0x0	wrap_mp_y Clear main picture Y address wrap interrupt
3	WO	0x0	fill_mp_y Clear fill level interrupt
2	WO	0x0	mblk_line Clear macro block line interrupt
1	WO	0x0	sp_frame_end Clear self picture end of frame interrupt
0	WO	0x0	mp_frame_end Clear main picture end of frame interrupt

MI_1400_MI_ISR

Address: Operational Base(0xFF3F1400) + offset (0x0108)

Bit	Attr	Reset Value	Description
31	WO	0x0	mpfbc_wr_frame_end Set mpfbc write end of frame interrupt
30	WO	0x0	isp_bus_err Set isp bus error interrupt
29	WO	0x0	bpds_frame_end Set bypass down-sampling picture end of frame interrupt
28	WO	0x0	mpds_frame_end Set main down-sampling picture end of frame interrupt

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Bit	Attr	Reset Value	Description
27	WO	0x0	wrap_bp_cb Set bypass picture Cb address wrap interrupt
26	WO	0x0	wrap_bp_y Set bypass picture Y address wrap interrupt
25	WO	0x0	bp_frame_end Set bypass path write end of frame interrupt
24	WO	0x0	bay3d_ds_frame_end Set bay3d down scale write end of frame interrupt
23	WO	0x0	bay3d_cur_frame_end Set bay3d current write end of frame interrupt
22	WO	0x0	bay3d_iir_frame_end Set bay3d iir write end of frame interrupt
21	WO	0x0	gain_wr_frame_end Set gain write end of frame interrupt
20	WO	0x0	dbr_wr_frame_end Set debayer-in write end of frame interrupt
19	WO	0x0	raw3_wr_frame_end Set raw3 tx end of frame interrupt
18	WO	0x0	raw2_wr_frame_end Set raw2 tx end of frame interrupt
17	WO	0x0	raw1_wr_frame_end Set raw1 tx end of frame interrupt
16	WO	0x0	raw0_wr_frame_end Set raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RW	0x0	sw_all_frame_end_set Set all picture end of frame interrupt
13	RW	0x0	sw_y12c_frame_end_set Set Y12 C picture end of frame interrupt
12	RW	0x0	sw_y12y_frame_end_set Set Y12 Y picture end of frame interrupt
11	WO	0x0	dma_ready Set dma ready interrupt
10	WO	0x0	fill_mp_y2 Set fill level interrupt 2
9	WO	0x0	wrap_sp_cr Set self picture Cr address wrap interrupt
8	WO	0x0	wrap_sp_cb Set self picture Cb address wrap interrupt
7	WO	0x0	wrap_sp_y Set self picture Y address wrap interrupt
6	WO	0x0	wrap_mp_cr Set main picture Cr address wrap interrupt
5	WO	0x0	wrap_mp_cb Set main picture Cb address wrap interrupt
4	WO	0x0	wrap_mp_y Set main picture Y address wrap interrupt
3	WO	0x0	fill_mp_y Set fill level interrupt
2	WO	0x0	mblk_line Set macro block line interrupt
1	WO	0x0	sp_frame_end Set self picture end of frame interrupt
0	WO	0x0	mp_frame_end Set main picture end of frame interrupt

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MI_1400_MI_STATUS

Address: Operational Base(0xFF3F1400) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RO	0x0	bpds_cb_full FIFO full flag of Cb FIFO in main path down sampling asserted since last clear
21	RO	0x0	bpds_y_full FIFO full flag of Y FIFO in bypass path down sampling asserted since last clear
20	RO	0x0	mpds_cb_full FIFO full flag of Cb FIFO in main path down sampling asserted since last clear
19	RO	0x0	mpds_y_full FIFO full flag of Y FIFO in main path down sampling asserted since last clear
18	RO	0x0	bp_cb_fifo_full FIFO full flag of Cb FIFO in bypass path asserted since last clear
17	RO	0x0	bp_y_fifo_full FIFO full flag of Y FIFO in bypass path asserted since last clear
16	RO	0x0	bay3d_ds_fifo_full FIFO full flag of bay3d down scale FIFO asserted since last clear
15	RO	0x0	bay3d_cur_fifo_full FIFO full flag of bay3d current FIFO asserted since last clear
14	RO	0x0	bay3d_iir_fifo_full FIFO full flag of bay3d iir FIFO asserted since last clear
13	RO	0x0	gain_fifo_full FIFO full flag of gain FIFO asserted since last clear
12	RO	0x0	dbr_wr_y_fifo_full FIFO full flag of Y FIFO in debayer-in write path asserted since last clear
11	RO	0x0	raw3_wr_y_fifo_full FIFO full flag of Y FIFO in raw3 tx path asserted since last clear
10	RO	0x0	raw2_wr_y_fifo_full FIFO full flag of Y FIFO in raw2 tx path asserted since last clear
9	RO	0x0	raw1_wr_y_fifo_full FIFO full flag of Y FIFO in raw1 tx path asserted since last clear
8	RO	0x0	raw0_wr_y_fifo_full FIFO full flag of Y FIFO in raw0 tx path asserted since last clear
7	RO	0x0	reserved
6	RO	0x0	sp_cr_fifo_full FIFO full flag of Cr FIFO in self path asserted since last clear
5	RO	0x0	sp_cb_fifo_full FIFO full flag of Cb FIFO in self path asserted since last clear
4	RO	0x0	sp_y_fifo_full FIFO full flag of Y FIFO in self path asserted since last clear
3	RO	0x0	reserved
2	RO	0x0	mp_cr_fifo_full FIFO full flag of Cr FIFO in main path asserted since last clear
1	RO	0x0	mp_cb_fifo_full FIFO full flag of Cb FIFO in main path asserted since last clear
0	RO	0x0	mp_y_fifo_full FIFO full flag of Y FIFO in main path asserted since last clear

MI_1400_MI_STATUS_CLR

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Address: Operational Base(0xFF3F1400) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	WO	0x0	bp_cb_fifo_full Clear status of Cb FIFO full flag in bypass path
17	WO	0x0	bp_y_fifo_full Clear status of Y FIFO full flag in bypass path
16	WO	0x0	bay3d_ds_fifo_full Clear status of bay3d down scale FIFO full flag
15	WO	0x0	bay3d_cur_fifo_full Clear status of bay3d current FIFO full flag
14	WO	0x0	bay3d_iir_fifo_full Clear status of bay3d iir FIFO full flag
13	WO	0x0	gain_fifo_full Clear status of gain FIFO full flag
12	WO	0x0	dbr_wr_y_fifo_full Clear status of Y FIFO full flag in debayer-in write path
11	WO	0x0	raw3_wr_y_fifo_full Clear status of Y FIFO full flag in raw3 tx path
10	WO	0x0	raw2_wr_y_fifo_full Clear status of Y FIFO full flag in raw2 tx path
9	WO	0x0	raw1_wr_y_fifo_full Clear status of Y FIFO full flag in raw1 tx path
8	WO	0x0	raw0_wr_y_fifo_full Clear status of Y FIFO full flag in raw0 tx path
7	RO	0x0	reserved
6	WO	0x0	sp_cr_fifo_full Clear status of Cr FIFO full flag in self path
5	WO	0x0	sp_cb_fifo_full Clear status of Cb FIFO full flag in self path
4	WO	0x0	sp_y_fifo_full Clear status of Y FIFO full flag in self path
3	RO	0x0	reserved
2	WO	0x0	mp_cr_fifo_full Clear status of Cr FIFO full flag in main path
1	WO	0x0	mp_cb_fifo_full Clear status of Cb FIFO full flag in main path
0	WO	0x0	mp_y_fifo_full Clear status of Y FIFO full flag in main path

MI_1400_MI_SP_WR_Y_PIC_WIDTH

Address: Operational Base(0xFF3F1400) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:0	RW	0x0000	sw_sp_wr_y_pic_width Image width of the self picture Y component or RGB picture in pixel. For YCbCr 4:2:x and RGB 565 the image width must be a multiple of 2. If no line stride is used but flipping required, the image width must be a multiple of 8 for 4:2:x planar or 4 for 4:4:4 planar/4:2:x semi planar. There are no restrictions for RGB 888/666. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used. Note: Image width always refers to the picture width of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_SP_WR_Y_PIC_HEIGHT

Address: Operational Base(0xFF3F1400) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_sp_wr_y_pic_height Image height of the y component or RGB picture in pixel. In planar and semi planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:0 and the same for 4:2:2 and 4:4:4. Note: Image height always refers to the picture height of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_SP_WR_Y_PIC_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_sp_wr_y_pic_size Image size of the Y component or RGB picture in pixel which has to be the Y line length multiplied by the Y image height (sp_y_llength * sp_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb and Cr component is assumed half for 4:2:0 and the same size for 4:2:2. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_WR_PIXEL_CNT

Address: Operational Base(0xFF3F1400) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:0	RO	0x0000000	pix_cnt Counter value specifies the number of pixels of the defect pixel list generated by DPCC of the last transmitted frame. Updated at frame end. A soft reset will set the counter to zero.

MI_1400_MI_MP_WR_Y_BASE2

Address: Operational Base(0xFF3F1400) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base2 2nd ping pong base address of main picture Y component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_Y_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE2

Address: Operational Base(0xFF3F1400) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base2 2nd ping pong base address of main picture CB component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details. Refer also to MI_MP_WR_CB_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE2

Address: Operational Base(0xFF3F1400) + offset (0x0138)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base2 2nd ping pong base address of main picture CR component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CR_BASE register description for details. Refer also to MI_MP_WR_CR_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE2

Address: Operational Base(0xFF3F1400) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base2 2nd ping pong base address of main picture Y component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_Y_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_BASE2

Address: Operational Base(0xFF3F1400) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base2 2nd ping pong base address of main picture CB component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details. Refer also to MI_MP_WR_CB_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_BASE2

Address: Operational Base(0xFF3F1400) + offset (0x0144)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base2 2nd ping pong base address of main picture CR component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CR_BASE register description for details. Refer also to MI_MP_WR_CR_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_WR_XTD_FORMAT_CTRL

Address: Operational Base(0xFF3F1400) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	sw_mi_wr_nv21_dma_read 1'b0: DMA read path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: DMA read path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses.
1	RW	0x0	sw_mi_wr_nv21_self 1'b0: Self path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: Self path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses. Note: If RGB888, do RB swap.
0	RW	0x0	sw_mi_wr_nv21_main 1'b0: Main path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: Main path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses.

MI_1400_MI_WR_ID

Address: Operational Base(0xFF3F1400) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x6	sw_spcr_wr_axi_id Spcr write id
27:24	RO	0x5	sw_spcb_wr_axi_id Spcb write id
23:20	RO	0x4	sw_spy_wr_axi_id Spy write id
19:16	RO	0x3	sw_mpcr_wr_axi_id Mpcr write id
15:12	RO	0x2	sw_mpcb_wr_axi_id Mpcb write id
11:8	RO	0x1	sw_mpy_wr_axi_id Mpy write id
7:0	RO	0x00	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS2

Address: Operational Base(0xFF3F1400) + offset (0x01E0)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_irq_offs2 Reaching this programmed value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_WR_Y_IRQ_OFFS --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS2_SHD

Address: Operational Base(0xFF3F1400) + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_irq_offs2_shd Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_LLENGTH

Address: Operational Base(0xFF3F1400) + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mp_wr_y_llegnth Line length of main picture Y component in pixel, also known as line stride. If no line stride is used, line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 16. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr. In semi planar 4:2:x mode the line length of the Cb and Cr component is assumed the same size. Note: Line length always refers to the line length of the output image. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_MP_WR_Y_PIC_WIDTH

Address: Operational Base(0xFF3F1400) + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:0	RW	0x0000	sw_mp_wr_y_pic_width Image width of the main picture Y component or RGB picture in pixel. For YCbCr 4:2:x and RGB 565 the image width must be a multiple of 2. If no line stride is used but flipping required, the image width must be a multiple of 8 for 4:2:x planar or 4 for 4:4:4 planar/4:2:x semi planar. There are no restrictions for RGB 888/666. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used. Note: Image width always refers to the picture width of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_MP_WR_Y_PIC_HEIGHT

Address: Operational Base(0xFF3F1400) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mp_wr_y_pic_height Image height of the y component or RGB picture in pixel. In planar and semi planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:0 and the same for 4:2:2 and 4:4:4. Note: Image height always refers to the picture height of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_MP_WR_Y_PIC_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_mp_wr_y_pic_size Image size of the Y component or RGB picture in pixel which has to be the Y line length multiplied by the Y image height (sp_y_llength * sp_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb and Cr component is assumed half for 4:2:0 and the same size for 4:2:2. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_MP_WR_CTRL

Address: Operational Base(0xFF3F1400) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mp_wr_align_dis 1'b0: Mp+sp burst align 1'b1: Disable mi_mp+mi_sp write burst align
30:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	sw_sp_wr_rgb888_alpha The RGB888 format of the self path supports filling with configurable alpha bits.
15:11	RO	0x00	reserved
10:8	RW	0x2	sw_mp_wr_output_format Selects output format of main picture. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 Others: Reserved Note: - Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path. - If sw_mp_wr_v_flip = 1 and yuv420 format, need to configure sw_mp_wr_output_format = 1.
7:0	RO	0x00	reserved

MI_1400_MI_SP_WR_Y_END_ADDR

Address: Operational Base(0xFF3F1400) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_sp_wr_y_end_addr SP y frame end address readback, used for SP wrap debug.

MI_1400_MI_SP_WR_CB_END_ADDR

Address: Operational Base(0xFF3F1400) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_sp_wr_cb_end_addr SP uv frame end address readback, used for SP wrap debug.

MI_1400_MI_WR_CTRL2

Address: Operational Base(0xFF3F1400) + offset (0x0400)

Bit	Attr	Reset Value	Description
31	WO	0x0	sys_dbr_st Soft start debayer
30	RW	0x0	sw_dbr_st_mode Start mode of debayer 1'b0: Frame_end auto start debayer 1'b1: Soft start debayer
29	RW	0x0	sw_path_sel_fix_dis MI path select fix disable 1'b0: enable 1'b1: disable If sw_path_sel_fix_dis is 1, maybe MI path enable input shadow update fail when When auto-update and self-update are used together.
28:25	RO	0x0	reserved
24	W1C	0x0	sys_bay3d_dsself_force_upd Force update of configuration registers for bay3dnr down scale frame DMA write.
23	W1C	0x0	sys_bay3d_curself_force_upd Force update of configuration registers for bay3dnr current frame DMA write.
22	W1C	0x0	sys_bay3d_iirself_force_upd Force update of configuration registers for bay3dnr iir frame DMA write.

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Bit	Attr	Reset Value	Description
21	W1C	0x0	sys_gainself_force_upd Force update of configuration registers for gain DMA write.
20	W1C	0x0	sys_dbr_3a_self_force_upd Force update of configuration registers for debayer or 3a DMA write.
19	RO	0x0	reserved
18	RW	0x0	sw_bay3d_ds_wr_auto_upd Automatic update of configuration registers for bay3d down scale write at frame end. 1'b1: Enabled 1'b0: Disabled
17	RW	0x0	sw_bay3d_cur_wr_auto_upd Automatic update of configuration registers for bay3d current write at frame end. 1'b1: Enabled 1'b0: Disabled
16	RW	0x0	sw_bay3d_iir_wr_auto_upd Automatic update of configuration registers for bay3d iir write at frame end. 1'b1: Enabled 1'b0: Disabled
15:14	RO	0x0	reserved
13	RW	0x0	sw_gain_wr_auto_upd Automatic update of configuration registers for gain write at frame end. 1'b1: Enabled 1'b0: Disabled
12	RW	0x0	sw_gain_wr_pingpong_en Pingpong mode of configuration registers for gain write at frame end. 1'b1: Enabled 1'b0: Disabled
11	WO	0x0	sys_rxdbr_force_upd Debayer read update
10	RW	0x0	sw_dbr_wr_auto_upd Automatic update of configuration registers for debayer-in write at frame end. 1'b1: Enabled 1'b0: Disabled
9	RW	0x0	sw_mimux_raw_align Debayer-in write align mode, 32bit including two data 1'b0: big-endian 1'b1: little-endian
8	RW	0x0	sw_dbr_enable_org Debayer-in enable for isp_hdrtmo data mux to DDR and read back to isp_debayer
7	WO	0x0	sys_rxb3d_force_upd Force update of configuration registers for bay3d DMA write.
6	RO	0x0	reserved
5	WO	0x0	sys_spself_force_upd Force update of configuration registers for self path DMA write.
4	WO	0x0	sys_mpself_force_upd Force update of configuration registers for main path DMA write.
3:0	RO	0x0	reserved

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MI_1400_MI_WR_ID2

Address: Operational Base(0xFF3F1400) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	sw_bay3d_iir_wr_axi_id Bay3d iir write id, read only
27:24	RO	0x0	sw_gain_wr_axi_id Gain write id, read only
23:20	RO	0x0	sw_dbr_wr_axi_id Debayer-in write id, read only
19:0	RO	0x00000	reserved

MI_1400_MI_RD_CTRL2

Address: Operational Base(0xFF3F1400) + offset (0x0408)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mi_new_rw_burst_dis 1'b0: Self-adaption enable 1'b1: Self-adaption disable
30	RW	0x0	sw_raw_rd_old Old-mi read. 1'b0: Disable 1'b1: Enable
29	RO	0x0	reserved
28	RW	0x0	sw_rw_mi_group_fix Fix group mode, backdoor
27	RW	0x0	sw_lut_raddr_shd_dis lut read address shadow disable 1'b1: disable 1'b0: enable
26:24	RO	0x0	reserved
23:22	RW	0x2	sw_rawx_rd_burst_len Burst length for raw data affecting DMA read port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: 2-beat bursts Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So read to the register only if no picture data is sent to the main and self path.
21:20	RW	0x2	sw_rawx_wr_burst_len Burst length for raw data affecting DMA write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: 2-beat bursts Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.

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Bit	Attr	Reset Value	Description
19:18	RW	0x1	sw_rd_rawx_group_mode Group mode for raw data affecting DMA read port. 2'b00: BurstN*4 2'b01: BurstN*3 2'b10: BurstN*2 2'b11: BurstN*1 Note: Programmed value becomes effective immediately. So read to the register only if no picture data is sent to the main and self path.
17:16	RW	0x1	sw_wr_rawx_group_mode Group mode for raw data affecting DMA write port. 2'b00: BurstN*4 2'b01: BurstN*3 2'b10: BurstN*2 2'b11: BurstN*1 Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
15:7	RO	0x000	reserved
6	RW	0x0	sw_bay3d_ds_rw_one_addr_en DDR address of debayer-in read is the same to bay3d down scale write
5	RW	0x0	sw_bay3d_cur_rw_one_addr_en DDR address of debayer-in read is the same to bay3d current write
4	RW	0x0	sw_bay3d_iir_rw_one_addr_en DDR address of debayer-in read is the same to bay3d iir write
3	RW	0x0	sw_dbr_rw_one_addr_en DDR address of debayer-in read is the same to debayer-in write
2	RW	0x0	sw_raws_rw_one_addr_en DDR address of raw2 rx is the same to raw2 tx
1	RW	0x0	sw_raw1_rw_one_addr_en DDR address of raw1 rx is the same to raw1 tx
0	RW	0x0	sw_raw0_rw_one_addr_en DDR address of raw0 rx is the same to raw0 tx

MI_1400_MI_RD_ID

Address: Operational Base(0xFF3F1400) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	sw_bay3d_ds_rd_axi_id Bay3d down scale read id, read only
27:24	RO	0x0	sw_bay3d_cur_rd_axi_id Bay3d current read id, read only
23:20	RO	0x0	sw_bay3d_iir_rd_axi_id Bay3d iir read id, read only
19:16	RO	0x0	sw_lut_rd_axi_id Mipi lut read id, read only
15:12	RO	0x0	sw_dbr_rd_axi_id Mipi debayer-in read id, read only
11:8	RO	0x0	sw_raws_rd_axi_id Mipi raw2 rx id, read only
7:4	RO	0x0	sw_raw1_rd_axi_id Mipi raw1 rx id, read only
3:0	RO	0x0	sw_raw0_rd_axi_id Mipi raw0 rx id, read only

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MI_1400_MI_WR_CTRL2_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	stat_bay3d_ds_wr_en_out_shd Bay3dnr down-sampling path output enable shadow in isp_mi.
25	RO	0x0	stat_bay3d_iir_wr_en_out_shd Bay3dnr iir path output enable shadow in isp_mi.
24	RO	0x0	stat_bay3d_cur_wr_en_out_shd Bay3dnr current path output enable shadow in isp_mi.
23	RO	0x0	reserved
22	RO	0x0	stat_gain_wr_en_out_shd Gain path output enable shadow in isp_mi.
21	RO	0x0	stat_dbr_wr_en_out_shd Debayer mi-mux path output enable shadow in isp_mi.
20:11	RO	0x000	reserved
10	RO	0x0	stat_bay3d_ds_wr_en_in_shd Bay3dnr down-sampling path input enable shadow in isp_mi.
9	RO	0x0	stat_bay3d_iir_wr_en_in_shd Bay3dnr iir path input enable shadow in isp_mi.
8	RO	0x0	stat_bay3d_cur_wr_en_in_shd Bay3dnr current path input enable shadow in isp_mi.
7	RO	0x0	reserved
6	RO	0x0	stat_gain_wr_en_in_shd Gain path input enable shadow in isp_mi.
5	RO	0x0	stat_dbr_wr_en_in_shd Debayer mi-mux path input enable shadow in isp_mi.
4:0	RO	0x00	reserved

MI_1400_MI_WR_WRAP_CTRL

Address: Operational Base(0xFF3F1400) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	sw_sp_wr_frmend_upd_dis Frame end address shadow update disable of self path.
24	RW	0x0	sw_mp_wr_frmend_upd_dis Frame end address shadow update disable of main path.
23:10	RO	0x0000	reserved
9	RW	0x0	sw_sp_dynamic_upd_addr Wrap dynamic address update enable of self path.
8	RW	0x0	sw_mp_dynamic_upd_addr Wrap dynamic address update enable of main path.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x1	sw_bpds_wr_init_offset_en Enables updating of the offset counters shadow registers for bypass path down sampling to the programmed register initial values. MI_MPDS_Y/CB/CR_OFFS_CNT_INIT -> MI_MPDS_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into bypass path down sampling picture. So only the corresponding bypass path down sampling shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
4	RW	0x1	sw_mpds_wr_init_offset_en Enables updating of the offset counters shadow registers for main path down sampling to the programmed register initial values. MI_MPDS_Y/CB/CR_OFFS_CNT_INIT -> MI_MPDS_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into main path down sampling picture. So only the corresponding main path down sampling shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
3	RO	0x0	reserved
2	RW	0x1	sw_bp_wr_init_offset_en Enables updating of the offset counters shadow registers for bypass path to the programmed register initial values. MI_BP_Y/CB/CR_OFFS_CNT_INIT -> MI_BP_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into bypass path picture. So only the corresponding bypass path shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
1	RW	0x1	sw_sp_wr_init_offset_en Enables updating of the offset counters shadow registers for self path to the programmed register initial values. MI_SP_Y/CB/CR_OFFS_CNT_INIT -> MI_SP_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into self path picture. So only the corresponding self path shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).

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Bit	Attr	Reset Value	Description
0	RW	0x1	sw_mp_wr_init_offset_en Enables updating of the offset counters shadow registers for main path to the programmed register initial values. MI_MP_Y/CB/CR_OFFS_CNT_INIT -> MI_MP_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into main path picture. So only the corresponding main path shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).

MI_1400_MI_WR_VFLIP_CTRL

Address: Operational Base(0xFF3F1400) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	sw_sp_wr_v_flip Vertical flipping of mainself picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_sp_wr_v_flip = 1, need to configure sw_sp_wr_y_pic_size.
0	RW	0x0	sw_mp_wr_v_flip Vertical flipping of main picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_mp_wr_v_flip = 1, need to configure sw_mp_wr_y_pic_size.

MI_1400_RAW0_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0470)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw0_rd_base Base address of raw0 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW0_RD_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_raw0_rd_length Line length of raw0 rx in pixel, also known as line stride.

MI_1400_RAW0_RD_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0478)

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Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_raw0_rd_base_shd Base shadow address of raw0 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW0_RD_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x047C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_raw0_rd_frmsize Frame size of raw0 read, only used in wrap mode.

MI_1400_RAW1_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0480)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw1_rd_base Base address of raw1 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW1_RD_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x0484)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_raw1_rd_length Line length of raw1 rx in pixel, also known as line stride.

MI_1400_RAW1_RD_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0488)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_raw1_rd_base_shd Base shadow address of raw1 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW1_RD_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x048C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_raw1_rd_frmsize Frame size of raw1 read, only used in wrap mode.

MI_1400_RAWS_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raws_rd_base Base address of raws rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAWS_RD_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x0494)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_raws_rd_length Line length of raws rx in pixel, also known as line stride.

MI_1400_RAWS_RD_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0498)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raws_rd_base_shd Base shadow address of raws rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAWS_RD_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x049C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_raws_rd_frmsize Frame size of raws read, only used in wrap mode.

MI_1400_LUT_CAC_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_caclut_rd_base Base address of cac lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_CAC_RD_H_WSIZE

Address: Operational Base(0xFF3F1400) + offset (0x0534)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_cac_lut_h_wsize Cac lut horizontal size, word unit cac_wsize = bigmode_en ? (pic_width+126)>>7 : (pic_width+62)>>6, lut_h_wsize = cac_wsize*9

MI_1400_LUT_CAC_RD_V_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0538)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_cac_lut_v_size Cac lut vertical size cac_hsize = bigmode_en ? (pic_height+126)>>7 : (pic_height+62)>>6, lut_v_size = cac_hsize*2

MI_1400_LUT_3D_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_3dlut_rd_base Base address of 3d lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_LSC_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_lsclut_rd_base Base address of lsc lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_LDCH_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0548)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_ldch_rd_base Base address of ldch lut read data ring buffer.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

MI_1400_LUT_3D_RD_WSIZE

Address: Operational Base(0xFF3F1400) + offset (0x0550)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x2d9	sw_3d_lut_wsize 3d lut actual size, word unit

MI_1400_LUT_LSC_RD_WSIZE

Address: Operational Base(0xFF3F1400) + offset (0x0554)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_lsc_lut_wsize Lsc lut actual size, word unit

MI_1400_LUT_LDCH_RD_H_WSIZE

Address: Operational Base(0xFF3F1400) + offset (0x0558)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_ldch_lut_h_wsize Ldch lut horizontal size, word unit (((pic_width+15)/16+1)+1)/2

MI_1400_LUT_LDCH_RD_V_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x055C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_ldch_lut_v_size Ldch lut vertical size (pic_height+7)/8+1

MI_1400_DBR_WR_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_dbr_wr_base Base address of debayer-in write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_DBR_WR_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0564)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_dbr_wr_size Size of debayer-in write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_DBR_WR_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x0568)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_dbr_wr_length Line length of debayer-in write in pixel, also known as line stride. If no line stride is used, line length must match image width.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

MI_1400_DBR_WR_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x056C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	dbr_wr_base_shd Base address of debayer-in write data ring buffer. --- DBR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to DBR_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_DBR_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0570)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_dbr_rd_base Base address of debayer-in read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_DBR_RD_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_dbr_rd_length Line length of debayer-in read in pixel, also known as line stride.

MI_1400_DBR_RD_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0578)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	dbr_rd_base_shd Base shadow address of debayer-in read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_SWS_3A_WR_BASE

Address: Operational Base(0xFF3F1400) + offset (0x057C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sws_3a_wr_base Base shadow address of debayer-in read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0580)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_gain_wr_base Base address of gain write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0584)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_gain_wr_size Size of gain write data ring buffer.
3:0	RO	0x0	reserved

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MI_1400_GAIN_WR_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x0588)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_gain_wr_length Line length of gain write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_BASE2

Address: Operational Base(0xFF3F1400) + offset (0x058C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_gain_wr_base2 Base address of gain write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x0590)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	gain_wr_base_shd Base address of gain write data ring buffer. --- GAIN_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to GAIN_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_WR_BASE

Address: Operational Base(0xFF3F1400) + offset (0x05A0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_iir_wr_base Base address of bayer 3dnr iir write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_WR_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x05A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bay3d_iir_wr_size Size of bayer 3dnr iir write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_WR_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x05A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_bay3d_iir_wr_length Line length of bayer 3dnr iir write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_WR_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x05AC)

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Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_wr_iir_base_shd Base address of bayer 3dnr iir write data ring buffer. --- BAY3D_IIR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_IIR_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x05B0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_iir_rd_base Base address of bayer 3dnr iir read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_RD_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x05B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_bay3d_iir_rd_length Line length of bayer 3dnr iir read in pixel, also known as line stride.

MI_1400_BAY3D_IIR_RD_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x05B8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_iir_rd_base_shd Base shadow address of bayer 3dnr iir read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_WR_BASE

Address: Operational Base(0xFF3F1400) + offset (0x05C0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_cur_wr_base Base address of bayer 3dnr current write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_WR_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x05C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bay3d_cur_wr_size Size of bayer 3dnr current write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_WR_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x05C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_bay3d_cur_wr_length Line length of bayer 3dnr current write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

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MI_1400_BAY3D_CUR_WR_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x05CC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_cur_wr_base_shd Base address of bayer 3dnr current write data ring buffer. --- BAY3D_CUR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_CUR_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x05D0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_cur_rd_base Base address of bayer 3dnr current read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_RD_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x05D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_bay3d_cur_rd_length Line length of bayer 3dnr current read in pixel, also known as line stride.

MI_1400_BAY3D_CUR_RD_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x05D8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_cur_rd_base_shd Base shadow address of bayer 3dnr current read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_RD_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x05DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_bay3d_cur_rd_frmsize Frame size of bayer 3dnr read, only used in wrap mode.

MI_1400_BAY3D_DS_WR_BASE

Address: Operational Base(0xFF3F1400) + offset (0x05E0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_ds_wr_base Base address of bayer 3dnr down scale write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_WR_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x05E4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bay3d_ds_wr_size Size of bayer 3dnr down scale write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_WR_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x05E8)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_bay3d_ds_wr_length Line length of bayer 3dnr down scale write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_WR_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x05EC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_ds_wr_base_shd Base address of bayer 3dnr iir write data ring buffer. --- BAY3D_IIR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_IIR_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x05F0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_ds_rd_base Base address of bayer 3dnr down scale read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_RD_LENGTH

Address: Operational Base(0xFF3F1400) + offset (0x05F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_bay3d_ds_rd_length Line length of bayer 3dnr down scale read in pixel, also known as line stride.

MI_1400_BAY3D_DS_RD_BASE_SHD

Address: Operational Base(0xFF3F1400) + offset (0x05F8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_ds_rd_base_shd Base shadow address of bayer 3dnr down scale read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_AXI_CONF_RD_CTRL

Address: Operational Base(0xFF3F1400) + offset (0x0640)

Bit	Attr	Reset Value	Description
31	RO	0x1	axi_conf_rd_status AXI configure read status. 1'b1: axi configure done. 1'b0: auto-start axi configure at mi all_frame_end
30	RO	0x0	ro_axi_conf_might_fail AXI configure might fail. 1'b1: isp_in_vsync is valid in the period of axi configure, maybe configure fail.
29	RO	0x0	ro_frm_buf_rw_conflict This status just detect whether write and read of frame buffer occur at the same time. It may not cause errors.

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Bit	Attr	Reset Value	Description
28	RO	0x0	ro_wr_frm_buf_error Error occurs when bay3d_ds and frame buffer write DDR at the same time.
27:17	RO	0x000	reserved
16	RW	0x0	sys_frm_buf_self_force_upd Write and read frame buffer data enable shadow force update. Note: - Readback is shadow register.
15:12	RO	0x0	reserved
11	RO	0x0	sw_rd_frm_buf_en_shd Read frame buffer data enable shadow. Shadow is updated by mi_all_frame_end.
10	RO	0x0	sw_wr_frm_buf_en_shd Write frame buffer data enable shadow. Shadow is updated by mi_all_frame_end.
9	RW	0x0	sw_rd_frm_buf_en Read frame buffer data enable.
8	RW	0x0	sw_wr_frm_buf_en Write frame buffer data enable. Bay3d_ds write path is reused by write frame buffer.
7:5	RO	0x0	reserved
4	W1C	0x0	sys_axi_conf_rd_clear AXI configure read clear to pull down axi_conf_rd_status for next frame auto axi configure.
3:2	RO	0x0	reserved
1	RW	0x0	sw_axi_conf_rd_st_mode AXI configure read start mode. 1'b0: aoto-start axi configure at mi all_frame_end when axi_conf_rd_status is 0. 1'b1: start axi configure at sys_axi_conf_rd_st is 1.
0	W1C	0x0	sys_axi_conf_rd_st AXI configure read start.

MI_1400_AXI_CONF_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_axi_conf_rd_base Base address of axi configure read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_AXI_CONF_RD_H_WSIZE

Address: Operational Base(0xFF3F1400) + offset (0x0648)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_axi_conf_wsize AXI configure size of horizontal direction, word unit

MI_1400_AXI_CONF_RD_V_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x064C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_axi_conf_vsize AXI configure size of vertical direction

MI_1400_FRM_BUF_WR_BASE

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Address: Operational Base(0xFF3F1400) + offset (0x0650)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_frm_buf_wr_base Base address of frame buffer write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_FRM_BUF_WR_SIZE

Address: Operational Base(0xFF3F1400) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_frm_buf_wr_size Size of frame buffer write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_FRM_BUF_RD_BASE

Address: Operational Base(0xFF3F1400) + offset (0x0658)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_frm_buf_rd_base Base address of frame buffer read data ring buffer.
3:0	RO	0x0	reserved

2.4.2.4 ISP_TOP

ISP_0400_CTRL0

Address: Operational Base(0xFF3F0400) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_cgc_ratio_en Cgc ratio mode 1'b1: Ration use 219/224 1'b0: Ration use
28	RW	0x0	sw_cgc_yuv_limit Yuv cgc enable 1'b1: Limit range 1'b0: Full range(bypass)
27:17	RO	0x000	reserved
16	RW	0x0	sw_en_12bit_unpack Isp_dma: Raw16to12->isp(unpack csi-raw12, 8-8-4/4)
15	RW	0x0	sw_en_12bit_packed Isp_dma: Raw16to12->isp(pack csi-raw12, 8-8-4/4)
14	RW	0x1	sw_csm_c_range Color Space Matrix chrominance clipping range for ISP output 1'b0: CbCr range 64..960 (16..240) according to ITU-R BT.601 standard 1'b1: Full UV range 0..1023 (0..255) Numbers in brackets are for 8 bit resolution. This bit also configures the YCbCr sequence align block accordingly
13	RW	0x1	sw_csm_y_range Color Space Matrix luminance clipping range for ISP output 1'b0: Y range 64..940 (16..235) according to ITU-R BT.601 standard 1'b1: Full Y range 0..1023 (0..255) Numbers in brackets are for 8 bit resolution. This bit also configures the YCbCr sequence align block accordingly

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Bit	Attr	Reset Value	Description
12	RW	0x0	sw_flash_mode 1'b0: Sensor interface works independently from flash control unit 1'b1: One frame is captured when signaled by flash control unit
11	RO	0x0	reserved
10	WO	0x0	sys_cfg_gen_upd 1'b1: Generate frame synchronous configuration signal at the output of ISP for shadow registers of the following processing modules, write only
9	WO	0x0	sys_cfg_force_upd 1'b1: Immediately configure (update) shadow registers, write only
8	RW	0x0	sys_cfg_gen_upd_fix 1'b1: Permanent configure (update) shadow registers on frame end
7	RW	0x0	isp_awb_enable Auto white balance ON/OFF
6	RW	0x0	sw_gamma_in_enable Sensor De-gamma ON/OFF
5	RW	0x0	sw_mir_enable 1'b1: ISP out yuv mirror enabled 1'b0: ISP out yuv mirror disabled There is a line delay from input to output. Note: Readback is shadow register.
4	RW	0x0	sw_inform_enable 1'b1: Input formatter enabled 1'b0: Input formatter disabled The ISP input formatter is enabled or disabled by this bit immediately, but always starts or stops acquisition frame synchronously
3:1	RW	0x0	sw_isp_mode 3'b000: RAW picture with BT.601 sync (ISP bypass) 3'b001: ITU-R BT.656 (YUV with embedded sync) 3'b010: ITU-R BT.601 (YUV input with H and Vsync signals) 3'b011: Bayer RGB processing with H and Vsync signals 3'b100: Data mode (ISP bypass, sync signals interpreted as data enable) 3'b101: Bayer RGB processing with BT.656 synchronization 3'b110: RAW picture with ITU-R BT.656 synchronization (ISP bypass) 3'b111: Reserved Side effect: If RAW, BT.601, BT.656, or data mode is selected, the clock of the ISP SRAMs (ISP line buffer, Lens Shading, Bad Pixel) is switched off. Only in Bayer RGB mode the clock to the SRAMs is enabled. This further reduces power consumption
0	RW	0x0	sw_isp_enable 1'b1: ISP data output enabled 1'b0: ISP data output disabled Controls output formatter frame synchronously, if isp_gen_cfg_upd is used to activate this bit. For immediate update isp_cfg_upd must be used. --- ISP_CTRL --- Note: Partly write-only

ISP_0400_CTRL1

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Address: Operational Base(0xFF3F0400) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_bigmode_mode Bigmode_mode 1'b1: Use bigmode force_en 1'b0: Bigmode auto(ynr fix non-bigmode, cnr>2688 auto use bigmode, others > half of picture-max-width); Note: cnr need to use bigmode_force_en to set bigmode when picture size > 2688x1536.
28	RW	0x0	sw_bigmode_force_en Bigmode force enable
27	W1C	0x1	sys_raw3d_fst_frame 3drawnr 1st_frame pulse signal
26	W1C	0x1	sys_cnr_fst_frame Cnr 1st_frame pulse signal
25	W1C	0x1	sys_dhaz_fst_frame Dhaz 1st_frame pulse signal
24	W1C	0x1	sys_adrc_fst_frame Adrc 1st_frame pulse signal
23	W1C	0x1	sys_ynr_fst_frame Ynr 1st_frame pulse signal
22	RW	0x0	sw_bt_1120_yc_swap Old dvp for ccir656, not use now It has been deleted in isp-lite version.
21	RW	0x0	sw_dualedge_en Old dvp for ccir656, not use now It has been deleted in isp-lite version.
20	RW	0x0	sw_bt1120_en 1'b0: Disable bt1120 mode 1'b1: Enable bt1120 mode Old dvp for ccir656, not use now It has been deleted in isp-lite version.
19	W1C	0x0	sys_shp_fst_frame Sharp 1st_frame pulse signal
18:17	RO	0x0	reserved
16	RW	0x0	sw_yuv_dma_sel 1'b0: Use align or conversion data for isp_is input 1'b1: Use dma yuv read data for isp_is input
15	RW	0x0	sw_rgb_dma_sel 1'b0: Use input formatter data for latency fifo 1'b1: Use dma rgb read data for latency fifo
14:12	RW	0x0	sw_input_selection 3'b000: 12Bit external Interface 3'b001: 10Bit Interface, append 2 zeroes as LSBs 3'b010: 10Bit Interface, append 2 MSBs as LSBs 3'b011: 8Bit Interface, append 4 zeroes as LSBs 3'b100: 8Bit Interface, append 4 MSBs as LSBs Others: Reserved It has been deleted in isp-lite version.
11	RW	0x0	sw_field_inv 1'b1: Swap odd and even fields 1'b0: Do not swap fields Old dvp for ccir656, not use now It has been deleted in isp-lite version.

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Bit	Attr	Reset Value	Description
10:9	RW	0x0	sw_field_selection 2'b00: Sample all fields (do not care about fields) 2'b01: Sample only even fields 2'b10: Sample only odd fields 2'b11: Reserved Old dvp for ccir656, not use now It has been deleted in isp-lite version.
8:7	RW	0x0	sw_ccir_seq 2'b00: YCbYCr 2'b01: YCrYCb 2'b10: CbYCrY 2'b11: CrYCbY Old dvp for ccir656, not use now
6:5	RW	0x3	sw_conv_422 2'b00 - Co-sited color sub-sampling Y0Cb0Cr0 C Y1 2'b01 - Interleaved color sub-sampling Y0Cb0 C Y1Cr1 (not recommended) 2'b10 - Non-cosited color sub-sampling Y0Cb(0+1)/2 C Y1Cr(0+1)/2 2'b11 - UV 1/2 sample (drop mode)
4:3	RW	0x0	sw_bayer_pat Color components from sensor, starting with top left position in sampled frame (reprogram with ISP_ACQ_H_OFFS, ISP_ACQ_V_OFFS) 2'b00 - First line: RGRG..., second line: GBGB..., etc. 2'b01 - First line: GRGR..., second line: BGBG..., etc. 2'b10 - First line: GBGB..., second line: RGRG..., etc. 2'b11 - First line: BGBG..., second line: GRGR..., etc. This configuration applies for the black level area after cropping by the input formatter
2	RW	0x0	sw_vsync_pol Vertical sync polarity 1'b0: High active 1'b1: Low active Old dvp for ccir656, not use now It has been deleted in isp-lite version.
1	RW	0x0	sw_hsync_pol Horizontal sync polarity 1'b0: High active 1'b1: Low active Old dvp for ccir656, not use now It has been deleted in isp-lite version.
0	RO	0x0	reserved

ISP_0400_ACQ_H_OFFS

Address: Operational Base(0xFF3F0400) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_sensor_index Multi-sensor index used 2'b00: Sensor0 index 2'b01: Sensor1 index 2'b10: Sensor2 index 2'b11: Sensor3 index Then same as sensor_id in old version

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Bit	Attr	Reset Value	Description
27:24	RW	0x0	sw_sensor_force_index Frame buffer is divided to 16 equal parts. If sw_sensor_mode is not meeting demand, you can use this reg to generate the desire shape of frame buffer. For example, when sensor_id=0, configure the register value to 0; when sensor_id=0, configure the register value to 8. Then this configure is equal to configure sw_sensor_mode to 1(two sensor of same size).
23	RO	0x0	reserved
22:20	RW	0x0	sw_sensor_mode Multi-sensor mode (outside sensor numbers): 3'b00: One sensor 3'b01: Two sensor of same size 3'b10: Four sensor of same size 3'b100: Three sensor of one big and two small(8M+4M+4M) 3'b101: Two sensor of one big and one small(13M+2M) Others: Reserved eg:8M=3840x2160;4M=2688x1536;13M=4224x3136
19:15	RO	0x00	reserved
14:0	RW	0x0000	sw_acq_h_offs Horizontal sample offset in 8-bit samples (yuv: 4 samples=2pix)

ISP_0400_ACQ_V_OFFS

Address: Operational Base(0xFF3F0400) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_acq_v_offs Vertical sample offset in lines

ISP_0400_ACQ_H_SIZE

Address: Operational Base(0xFF3F0400) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	sw_acq_h_size_bay3dmi sw_acq_h_size_bay3dmi for bay3d size configure, when not configure, hardware will auto-calculate
15	RO	0x0	reserved
14:0	RW	0x1000	sw_acq_h_size Horizontal sample size in 12-bit samples YUV input: 2 samples = 1 pixel, else 1 sample = 1 pixel. So in YUV mode ACQ_H_SIZE must be twice as large as horizontal image size Horizontal image size must always be even except in raw picture mode. If an odd size is programmed the value will be truncated to even size

ISP_0400_ACQ_V_SIZE

Address: Operational Base(0xFF3F0400) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0c00	sw_acq_v_size Vertical sample size in lines

ISP_0400_ACQ_NR_FRAMES

Address: Operational Base(0xFF3F0400) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_acq_nr_frames Number of input frames to be sampled (0 = continuous)

ISP_0400_GAMMA_DX_LO

Address: Operational Base(0xFF3F0400) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x4	sw_gamma_dx8 Gamma curve sample point definition x-axis (input)
27	RO	0x0	reserved
26:24	RW	0x4	sw_gamma_dx7 Gamma curve sample point definition x-axis (input)
23	RO	0x0	reserved
22:20	RW	0x4	sw_gamma_dx6 Gamma curve sample point definition x-axis (input)
19	RO	0x0	reserved
18:16	RW	0x4	sw_gamma_dx5 Gamma curve sample point definition x-axis (input)
15	RO	0x0	reserved
14:12	RW	0x4	sw_gamma_dx4 Gamma curve sample point definition x-axis (input)
11	RO	0x0	reserved
10:8	RW	0x4	sw_gamma_dx3 Gamma curve sample point definition x-axis (input)
7	RO	0x0	reserved
6:4	RW	0x4	sw_gamma_dx2 Gamma curve sample point definition x-axis (input)
3	RO	0x0	reserved
2:0	RW	0x4	sw_gamma_dx1 Gamma curve sample point definition x-axis (input)

ISP_0400_GAMMA_DX_HI

Address: Operational Base(0xFF3F0400) + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x4	sw_gamma_dx16 Gamma curve sample point definition x-axis (input)
27	RO	0x0	reserved
26:24	RW	0x4	sw_gamma_dx15 Gamma curve sample point definition x-axis (input)
23	RO	0x0	reserved
22:20	RW	0x4	sw_gamma_dx14 Gamma curve sample point definition x-axis (input)
19	RO	0x0	reserved
18:16	RW	0x4	sw_gamma_dx13 Gamma curve sample point definition x-axis (input)
15	RO	0x0	reserved
14:12	RW	0x4	sw_gamma_dx12 Gamma curve sample point definition x-axis (input)
11	RO	0x0	reserved
10:8	RW	0x4	sw_gamma_dx11 Gamma curve sample point definition x-axis (input)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x4	sw_gamma_dx10 Gamma curve sample point definition x-axis (input)
3	RO	0x0	reserved
2:0	RW	0x4	sw_gamma_dx9 Gamma curve sample point definition x-axis (input)

ISP_0400_GAMMA_R_Y_0

Address: Operational Base(0xFF3F0400) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_gamma_r_y0 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_1

Address: Operational Base(0xFF3F0400) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x100	sw_gamma_r_y1 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_2

Address: Operational Base(0xFF3F0400) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x200	sw_gamma_r_y2 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_3

Address: Operational Base(0xFF3F0400) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x300	sw_gamma_r_y3 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_4

Address: Operational Base(0xFF3F0400) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x400	sw_gamma_r_y4 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

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ISP_0400_GAMMA_R_Y_5

Address: Operational Base(0xFF3F0400) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x500	sw_gamma_r_y5 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_6

Address: Operational Base(0xFF3F0400) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x600	sw_gamma_r_y6 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_7

Address: Operational Base(0xFF3F0400) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x700	sw_gamma_r_y7 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_8

Address: Operational Base(0xFF3F0400) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x800	sw_gamma_r_y8 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_9

Address: Operational Base(0xFF3F0400) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x900	sw_gamma_r_y9 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_10

Address: Operational Base(0xFF3F0400) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0xa00	sw_gamma_r_y10 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_11

Address: Operational Base(0xFF3F0400) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xb00	sw_gamma_r_y11 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_12

Address: Operational Base(0xFF3F0400) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xc00	sw_gamma_r_y12 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_13

Address: Operational Base(0xFF3F0400) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xd00	sw_gamma_r_y13 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_14

Address: Operational Base(0xFF3F0400) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xe00	sw_gamma_r_y14 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_15

Address: Operational Base(0xFF3F0400) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xf00	sw_gamma_r_y15 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

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ISP_0400_GAMMA_R_Y_16

Address: Operational Base(0xFF3F0400) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xfff	sw_gamma_r_y16 Gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_0

Address: Operational Base(0xFF3F0400) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_gamma_g_y0 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_1

Address: Operational Base(0xFF3F0400) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x100	sw_gamma_g_y1 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_2

Address: Operational Base(0xFF3F0400) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x200	sw_gamma_g_y2 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_3

Address: Operational Base(0xFF3F0400) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x300	sw_gamma_g_y3 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_4

Address: Operational Base(0xFF3F0400) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x400	sw_gamma_g_y4 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_5

Address: Operational Base(0xFF3F0400) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x500	sw_gamma_g_y5 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_6

Address: Operational Base(0xFF3F0400) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x600	sw_gamma_g_y6 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_7

Address: Operational Base(0xFF3F0400) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x700	sw_gamma_g_y7 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_8

Address: Operational Base(0xFF3F0400) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x800	sw_gamma_g_y8 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_9

Address: Operational Base(0xFF3F0400) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x900	sw_gamma_g_y9 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

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ISP_0400_GAMMA_G_Y_10

Address: Operational Base(0xFF3F0400) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xa00	sw_gamma_g_y10 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_11

Address: Operational Base(0xFF3F0400) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xb00	sw_gamma_g_y11 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_12

Address: Operational Base(0xFF3F0400) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xc00	sw_gamma_g_y12 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_13

Address: Operational Base(0xFF3F0400) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xd00	sw_gamma_g_y13 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_14

Address: Operational Base(0xFF3F0400) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xe00	sw_gamma_g_y14 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_15

Address: Operational Base(0xFF3F0400) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0xf00	sw_gamma_g_y15 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_16

Address: Operational Base(0xFF3F0400) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xfff	sw_gamma_g_y16 Gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_0

Address: Operational Base(0xFF3F0400) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_gamma_b_y0 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_1

Address: Operational Base(0xFF3F0400) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x100	sw_gamma_b_y1 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_2

Address: Operational Base(0xFF3F0400) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x200	sw_gamma_b_y2 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_3

Address: Operational Base(0xFF3F0400) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x300	sw_gamma_b_y3 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

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ISP_0400_GAMMA_B_Y_4

Address: Operational Base(0xFF3F0400) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x400	sw_gamma_b_y4 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_5

Address: Operational Base(0xFF3F0400) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x500	sw_gamma_b_y5 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_6

Address: Operational Base(0xFF3F0400) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x600	sw_gamma_b_y6 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_7

Address: Operational Base(0xFF3F0400) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x700	sw_gamma_b_y7 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_8

Address: Operational Base(0xFF3F0400) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x800	sw_gamma_b_y8 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_9

Address: Operational Base(0xFF3F0400) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x900	sw_gamma_b_y9 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_10

Address: Operational Base(0xFF3F0400) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xa00	sw_gamma_b_y10 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_11

Address: Operational Base(0xFF3F0400) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xb00	sw_gamma_b_y11 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_12

Address: Operational Base(0xFF3F0400) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xc00	sw_gamma_b_y12 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_13

Address: Operational Base(0xFF3F0400) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xd00	sw_gamma_b_y13 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_14

Address: Operational Base(0xFF3F0400) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xe00	sw_gamma_b_y14 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

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ISP_0400_GAMMA_B_Y_15

Address: Operational Base(0xFF3F0400) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xf00	sw_gamma_b_y15 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_16

Address: Operational Base(0xFF3F0400) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xfff	sw_gamma_b_y16 Gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_AWB1_GAIN_G

Address: Operational Base(0xFF3F0400) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x100	sw_awb1_gain_gr Gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 15 with 8 bit fractional part.
15:12	RO	0x0	reserved
11:0	RW	0x100	sw_awb1_gain_gb Gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 15 with 8 bit fractional part.

ISP_0400_AWB1_GAIN_RB

Address: Operational Base(0xFF3F0400) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x100	sw_awb1_gain_r Gain value for red component 100h = 1, unsigned integer value, range 0 to 15 with 8 bit fractional part.
15:12	RO	0x0	reserved
11:0	RW	0x100	sw_awb1_gain_b Gain value for blue component 100h = 1, unsigned integer value, range 0 to 15 with 8 bit fractional part.

ISP_0400_AWB0_GAIN0_G

Address: Operational Base(0xFF3F0400) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RW	0x0100	sw_awb_gain0_gr Gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.
15:0	RW	0x0100	sw_awb_gain0_gb Gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.

ISP_0400_AWB0_GAIN0_RB

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Address: Operational Base(0xFF3F0400) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0100	sw_awb_gain0_r Gain value for red component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.
15:0	RW	0x0100	sw_awb_gain0_b Gain value for blue component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.

ISP_0400_AWB0_GAIN1_G

Address: Operational Base(0xFF3F0400) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_awb_gain1_gr Gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.
15:0	RW	0x0000	sw_awb_gain1_gb Gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.

ISP_0400_AWB0_GAIN1_RB

Address: Operational Base(0xFF3F0400) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_awb_gain1_r Gain value for red component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.
15:0	RW	0x0000	sw_awb_gain1_b Gain value for blue component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.

ISP_0400_AWB0_GAIN2_G

Address: Operational Base(0xFF3F0400) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_awb_gain2_gr Gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part. (3562 no use)
15:0	RW	0x0000	sw_awb_gain2_gb Gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part. (3562 no use)

ISP_0400_AWB0_GAIN2_RB

Address: Operational Base(0xFF3F0400) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_awb_gain2_r Gain value for red component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part. (3562 no use)
15:0	RW	0x0000	sw_awb_gain2_b Gain value for blue component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part. (3562 no use)

ISP_0400_HURRY_CTRL

Address: Operational Base(0xFF3F0400) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:12	RW	0x6	sw_noc_hurry_r_mode Lafifo wr-channel, 3bit: hurry_req assert high when left water level<(hurry_w1_mode/8) fifo empty, recommended value=0x6;
11:8	RW	0x5	sw_noc_hurry_w1_mode Ibuf0-S rw-channel, 3bit: hurry_req assert high when left water level<(hurry_w1_mode/16) fifo empty, recommended value=0x5;
7:4	RW	0x8	sw_noc_hurry_w0_mode Lafifo wr-channel, 3bit: hurry_req assert high when left water level<(hurry_w1_mode/8) fifo empty, recommended value=0x8
3	RO	0x0	reserved
2:0	RW	0x3	sw_noc_hurry_value 3'b000: The Low priority to interconnect ..... 3'b111: The first High priority to interconnect

ISP_0400_AWQOS_CTRL

Address: Operational Base(0xFF3F0400) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x1	sw_aw_allwr_qos1 Register1 of other channel (except bay3d) write qos to interconnect, configure 0 to 7, default 1
19	RO	0x0	reserved
18:16	RW	0x2	sw_aw_allwr_qos2 Register2 of other channel (except bay3d) write qos to interconnect, configure 0 to 7, default 2
15	RO	0x0	reserved
14:12	RW	0x3	sw_aw_allwr_qos3 Register3 of other channel (except bay3d) write qos to interconnect, configure 0 to 7, default 3
11	RO	0x0	reserved
10:8	RW	0x1	sw_aw_bay3d_qos1 Register1 of bay3d write qos to interconnect, configure 0 to 7, default 1
7	RO	0x0	reserved
6:4	RW	0x2	sw_aw_bay3d_qos2 Register2 of bay3d write qos to interconnect, configure 0 to 7, default 2
3:1	RO	0x0	reserved
0	RW	0x1	sw_aw_qos_en All bus channel AXI write qos to interconnect, enable

ISP_0400_ARQOS_CTRL

Address: Operational Base(0xFF3F0400) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x1	sw_ar_rawx3_qos1 Register1 of rawx3 read qos to interconnect, configure 0 to 7, default 1
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x2	sw_ar_rawx3_qos2 Register2 of rawx3 read qos to interconnect, configure 0 to 7, default 2
19	RO	0x0	reserved
18:16	RW	0x1	sw_ar_bay3d_qos1 Register1 of bay3d read qos to interconnect, configure 0 to 7, default 1
15	RO	0x0	reserved
14:12	RW	0x2	sw_ar_bay3d_qos2 Register2 of bay3d read qos to interconnect, configure 0 to 7, default 2
11	RO	0x0	reserved
10:8	RW	0x1	sw_ar_others_qos1 Other channel (except bay3d and mmu) write qos to interconnect, configure 0 to 7, default 1
7	RO	0x0	reserved
6:4	RW	0x3	sw_ar_mmu_qos3 MMU write qos to interconnect, configure 0 to 7, default 3
3:1	RO	0x0	reserved
0	RW	0x1	sw_ar_qos_en All bus channel AXI read qos to interconnect, enable

ISP_0400_IRQ_CFG0

Address: Operational Base(0xFF3F0400) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_isp_irq_line1 ISP out irq line1 configuration for half frame interrupt of image height. And ISP_IRQ is generated by interrupt bit[24].
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_isp_irq_line0 ISP out irq line0 configuration for quarter frame interrupt of image height. And ISP_IRQ is generated by interrupt bit[25]. Note: sw_isp_irq_line0 is reused by ISP slice done.

ISP_0400_IRQ_CFG1

Address: Operational Base(0xFF3F0400) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_isp_irq_line2 ISP out irq line2 configuration for three quarters frame interrupt of image height. And ISP_IRQ is generated by interrupt bit[23].

ISP_0400_CC_COEFF_0

Address: Operational Base(0xFF3F0400) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_csm_y_offset If this signal is 0, will use old function(Y = f(coe_x) + 0 or 16). If this signal is not 0, Y = f(coe_x) + sw_csm_y_offset
23:16	RW	0x00	sw_csm_c_offset If this signal is 0, will use old function(Cb/r = f(coe_x) + 128). If this signal is not 0, Cb/r = f(coe_x) + sw_csm_c_offset
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x021	sw_csm_coeff0 Coefficient 0 for color space conversion --- ISP_CC_COEFF_0 --- Note: All color conversion coefficients are signed integer values with 7 bit fractional part, range -2 to 1.992

ISP_0400_CC_COEFF_1

Address: Operational Base(0xFF3F0400) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x040	sw_csm_coeff1 Coefficient 1 for color space conversion

ISP_0400_CC_COEFF_2

Address: Operational Base(0xFF3F0400) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x00d	sw_csm_coeff2 Coefficient 2 for color space conversion

ISP_0400_CC_COEFF_3

Address: Operational Base(0xFF3F0400) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x1ed	sw_csm_coeff3 Coefficient 3 for color space conversion

ISP_0400_CC_COEFF_4

Address: Operational Base(0xFF3F0400) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x1db	sw_csm_coeff4 Coefficient 4 for color space conversion

ISP_0400_CC_COEFF_5

Address: Operational Base(0xFF3F0400) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x038	sw_csm_coeff5 Coefficient 5 for color space conversion

ISP_0400_CC_COEFF_6

Address: Operational Base(0xFF3F0400) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x038	sw_csm_coeff6 Coefficient 6 for color space conversion

ISP_0400_CC_COEFF_7

Address: Operational Base(0xFF3F0400) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x1d1	sw_csm_coeff7 Coefficient 7 for color space conversion

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ISP_0400_CC_COEFF_8

Address: Operational Base(0xFF3F0400) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x1f7	sw_csm_coeff8 Coefficient 8 for color space conversion

ISP_0400_OUT_H_OFFS

Address: Operational Base(0xFF3F0400) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_out_h_offs Vertical picture offset in lines

ISP_0400_OUT_V_OFFS

Address: Operational Base(0xFF3F0400) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_out_v_offs Vertical picture offset in lines

ISP_0400_OUT_H_SIZE

Address: Operational Base(0xFF3F0400) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x1000	sw_out_h_size Horizontal picture size in pixel if ISP_MODE is set to 3'b001: ITU-R BT.656 YUV 3'b010: ITU-R BT.601 YUV 3'b011: ITU-R BT.601 Bayer RGB 3'b101: ITU-R BT.656 Bayer RGB Only even numbers are accepted, because complete quadruples of YUYV(YCbYCr) are needed for the 422 output. (If an odd size is programmed the value will be truncated to even size)

ISP_0400_OUT_V_SIZE

Address: Operational Base(0xFF3F0400) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0c00	sw_out_v_size Vertical picture size in lines

ISP_0400_FLAGS_SHD

Address: Operational Base(0xFF3F0400) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31	RO	0x0	s_hsync State of ISP input port s_hsync, for test purposes
30	RO	0x0	s_vsync State of ISP input port s_vsync, for test purposes
29:28	RO	0x0	reserved
27:16	RO	0x000	s_data State of ISP input port s_data, for test purposes
15:3	RO	0x0000	reserved
2	RO	0x0	inform_field Current field information (0=odd, 1=even)

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Bit	Attr	Reset Value	Description
1	RO	0x0	isp_inform_enable_shd Input formatter enable shadow register
0	RO	0x0	isp_enable_shd ISP enable shadow register shows, if ISP currently outputs data (1) or not (0)

ISP_0400_OUT_H_OFFS_SHD

Address: Operational Base(0xFF3F0400) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	isp_out_h_offs_shd Current vertical picture offset in lines

ISP_0400_OUT_V_OFFS_SHD

Address: Operational Base(0xFF3F0400) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	isp_out_v_offs_shd Current vertical picture offset in lines

ISP_0400_OUT_H_SIZE_SHD

Address: Operational Base(0xFF3F0400) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	isp_out_h_size_shd Current horizontal picture size in pixel

ISP_0400_OUT_V_SIZE_SHD

Address: Operational Base(0xFF3F0400) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	isp_out_v_size_shd Vertical picture size in lines

ISP_0400_ISP_IMSC

Address: Operational Base(0xFF3F0400) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_imsc_fetch_lut_end 1'b1: Enable interrupt 1'b0: Mask out
29	RW	0x0	sw_imsc_baynr_frame_end 1'b1: Enable interrupt 1'b0: Mask out
28	RW	0x0	sw_imsc_bay3d_post_st 1'b1: Enable interrupt 1'b0: Mask out
27	RW	0x0	sw_imsc_bay3d_in_linecnt_done 1'b1: Enable interrupt 1'b0: Mask out
26	RW	0x0	sw_imsc_bay3d_in_done 1'b1: Enable interrupt 1'b0: Mask out

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Bit	Attr	Reset Value	Description
25	RW	0x0	sw_imsc_out_quarter 1'b1: Enable interrupt 1'b0: Mask out
24	RW	0x0	sw_imsc_out_half 1'b1: Enable interrupt 1'b0: Mask out
23	RW	0x0	sw_imsc_out_frm_end 1'b1: Enable interrupt 1'b0: Mask out
22	RW	0x0	sw_imsc_gain_err 1'b1: Enable interrupt 1'b0: Mask out
21	RW	0x0	sw_imsc_dhaz_done 1'b1: Enable interrupt 1'b0: Mask out
20	RW	0x0	sw_imsc_hdr_done 1'b1: Enable interrupt 1'b0: Mask out
19	RO	0x0	reserved
18	RW	0x0	sw_imsc_exp_end 1'b1: Enable interrupt 1'b0: Mask out
17	RW	0x0	sw_imsc_flash_cap 1'b1: Enable interrupt 1'b0: Mask out
16	RW	0x0	sw_imsc_lsc_lut_err 1'b1: Enable interrupt 1'b0: Mask out
15	RW	0x0	sw_imsc_hist_measure_rdy 1'b1: Enable interrupt 1'b0: Mask out
14	RW	0x0	sw_imsc_afm_fin 1'b1: Enable interrupt 1'b0: Mask out
13	RW	0x0	sw_imsc_afm_lum_of 1'b1: Enable interrupt 1'b0: Mask out
12	RW	0x0	sw_imsc_afm_sum_of 1'b1: Enable interrupt 1'b0: Mask out
11	RW	0x0	sw_imsc_shutter_off 1'b1: Enable interrupt 1'b0: Mask out
10	RW	0x0	sw_imsc_shutter_on 1'b1: Enable interrupt 1'b0: Mask out
9	RW	0x0	sw_imsc_flash_off 1'b1: Enable interrupt 1'b0: Mask out
8	RW	0x0	sw_imsc_flash_on 1'b1: Enable interrupt 1'b0: Mask out
7	RW	0x0	sw_imsc_h_start 1'b1: Enable interrupt 1'b0: Mask out

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Bit	Attr	Reset Value	Description
6	RW	0x0	sw_imsc_v_start 1'b1: Enable interrupt 1'b0: Mask out
5	RW	0x0	sw_imsc_frame_in 1'b1: Enable interrupt 1'b0: Mask out
4	RW	0x0	sw_imsc_awb_done 1'b1: Enable interrupt 1'b0: Mask out
3	RW	0x0	sw_imsc_pic_size_err 1'b1: Enable interrupt 1'b0: Mask out
2	RW	0x0	sw_imsc_data_loss 1'b1: Enable interrupt 1'b0: Mask out
1	RW	0x0	sw_imsc_frame 1'b1: Enable interrupt 1'b0: Mask out
0	RW	0x0	sw_imsc_isp_off 1'b1: Enable interrupt 1'b0: Mask out

ISP_0400_ISP_RIS

Address: Operational Base(0xFF3F0400) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	ris_fetch_lut_end LUT readback DDR complete, high valid
29	RO	0x0	ris_baynr_frame_end BAYBR module complete, high valid
28	RO	0x0	ris_bay3d_post_st BAY3D module next frame start signal generate before current frame_end, high valid
27	RO	0x0	ris_bay3d_in_linecnt_done BAY3D module current line counter done, high valid
26	RO	0x0	ris_bay3d_in_done BAY3D module current write buffer empty, high valid
25	RO	0x0	ris_out_quarter ISP output frame transmit quarter, high valid
24	RO	0x0	ris_out_half ISP output frame transmit half, high valid
23	RO	0x0	ris_out_frm_end ISP output frame complete, high valid
22	RO	0x0	ris_gain_err GAIN module error flag, high valid
21	RO	0x0	ris_dhaz_done DHAZ module complete, high valid
20	RO	0x0	ris_hdr_done HDR module complete, high valid
19	RO	0x0	reserved
18	RO	0x0	ris_exp_end Exposure measurement complete, high valid
17	RO	0x0	ris_flash_cap Signaling captured frame, high valid

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Bit	Attr	Reset Value	Description
16	RO	0x0	ris_lsc_lut_err LSC and RAWLSC LUT update error, high valid
15	RO	0x0	ris_hist_measure_rdy Histogram measurement ready. (Old or new histogram measurement), high valid
14	RO	0x0	ris_afm_fin AF measurement finished: This interrupt is set when the first complete frame is calculated after enabling the AF measurement, high valid
13	RO	0x0	ris_afm_lum_of Auto focus luminance overflow, high valid
12	RO	0x0	ris_afm_sum_of Auto focus sum overflow, high valid
11	RO	0x0	ris_shutter_off Mechanical shutter is switched off, high valid
10	RO	0x0	ris_shutter_on Mechanical shutter is switched on, high valid
9	RO	0x0	ris_flash_off Flash light is switched off, high valid
8	RO	0x0	ris_flash_on Flash light is switched on, high valid
7	RO	0x0	ris_h_start Start edge of h_sync, high valid
6	RO	0x0	ris_v_start Start edge of v_sync, high valid
5	RO	0x0	ris_frame_in Sampled input frame is complete, high valid
4	RO	0x0	ris_awb_done White balancing measurement cycle is complete, results can be read out, high valid
3	RO	0x0	ris_pic_size_err Picture size violation occurred, programming seems wrong, high valid
2	RO	0x0	ris_data_loss Loss of data occurred within a line, processing failure, high valid
1	RO	0x0	ris_frame Frame was completely put out, high valid
0	RO	0x0	ris_isp_off Isp output was disabled (vsynced) due to f_cnt reached or manual, high valid

ISP_0400_ISP_MIS

Address: Operational Base(0xFF3F0400) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	mis_fetch_lut_end LUT readback DDR complete, high valid
29	RO	0x0	mis_baynr_frame_end BAYBR module complete, high valid
28	RO	0x0	mis_bay3d_post_st BAY3D module next frame start signal generate before current frame_end, high valid
27	RO	0x0	mis_bay3d_in_linecnt_done BAY3D module current line counter done, high valid

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Bit	Attr	Reset Value	Description
26	RO	0x0	mis_bay3d_in_done BAY3D module current write buffer empty, high valid
25	RO	0x0	mis_out_quarter ISP output frame transmit quarter, high valid
24	RO	0x0	mis_out_half ISP output frame transmit half, high valid
23	RO	0x0	mis_out_frm_end ISP output frame complete, high valid
22	RO	0x0	mis_gain_err GAIN module error flag, high valid
21	RO	0x0	mis_dhaz_done DHAZ module complete, high valid
20	RO	0x0	mis_hdr_done HDR module complete, high valid
19	RO	0x0	reserved
18	RO	0x0	mis_exp_end Exposure measurement complete, high valid
17	RO	0x0	mis_flash_cap Captured is frame is detected, high valid
16	RO	0x0	mis_lsc_lut_err LSC and RAWLSC LUT update error, high valid
15	RO	0x0	mis_hist_measure_rdy Histogram measurement ready. (Old or new histogram measurement), high valid
14	RO	0x0	mis_afm_fin AF measurement finished: This interrupt is set when the first complete frame is calculated after enabling the AF measurement, high valid
13	RO	0x0	mis_afm_lum_of Luminance overflow, high valid
12	RO	0x0	mis_afm_sum_of Sum overflow, high valid
11	RO	0x0	mis_shutter_off Mechanical shutter is switched off, high valid
10	RO	0x0	mis_shutter_on Mechanical shutter is switched on, high valid
9	RO	0x0	mis_flash_off Flash light is switched off, high valid
8	RO	0x0	mis_flash_on Flash light is switched on, high valid
7	RO	0x0	mis_h_start Start edge of h_sync, high valid
6	RO	0x0	mis_v_start Start edge of v_sync, high valid
5	RO	0x0	mis_frame_in Sampled input frame is complete, high valid
4	RO	0x0	mis_awb_done White balancing measurement cycle is complete, results can be read out, high valid
3	RO	0x0	mis_pic_size_err Picture size violation occurred, programming seems wrong, high valid
2	RO	0x0	mis_data_loss Loss of data occurred within a line, processing failure, high valid

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Bit	Attr	Reset Value	Description
1	RO	0x0	mis_frame Frame was completely put out, high valid each MIS[31:0] signals high, set IRQ.
0	RO	0x0	mis_isp_off Isp was turned off (vsync) due to f_cnt reached or manual, high valid each MIS[31:0] signals high, set IRQ.

ISP_0400_ISP_ICR

Address: Operational Base(0xFF3F0400) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	WO	0x0	sys_icr_fetch_lut_end Clear interrupt
29	WO	0x0	sys_icr_baynr_frame_end Clear interrupt
28	WO	0x0	sys_icr_bay3d_post_st Clear interrupt
27	WO	0x0	sys_icr_bay3d_in_linecnt_done Clear interrupt
26	WO	0x0	sys_icr_bay3d_in_done Clear interrupt
25	WO	0x0	sys_icr_out_quarter Clear interrupt
24	WO	0x0	sys_icr_out_half Clear interrupt
23	WO	0x0	sys_icr_out_frm_end Clear interrupt
22	WO	0x0	sys_icr_gain_err Clear interrupt
21	WO	0x0	sys_icr_dhaz_done Clear interrupt
20	WO	0x0	sys_icr_hdr_done Clear interrupt
19	RO	0x0	reserved
18	WO	0x0	sys_icr_exp_end Clear interrupt
17	WO	0x0	sys_icr_flash_cap Clear interrupt
16	WO	0x0	sys_icr_lsc_lut_err Clear interrupt
15	WO	0x0	sys_icr_hist_measure_rdy Clear interrupt
14	WO	0x0	sys_icr_afm_fin Clear interrupt
13	WO	0x0	sys_icr_afm_lum_of Clear interrupt
12	WO	0x0	sys_icr_afm_sum_of Clear interrupt
11	WO	0x0	sys_icr_shutter_off Clear interrupt
10	WO	0x0	sys_icr_shutter_on Clear interrupt
9	WO	0x0	sys_icr_flash_off Clear interrupt

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Bit	Attr	Reset Value	Description
8	WO	0x0	sys_icr_flash_on Clear interrupt
7	WO	0x0	sys_icr_h_start Clear interrupt
6	WO	0x0	sys_icr_v_start Clear interrupt
5	WO	0x0	sys_icr_frame_in Clear interrupt
4	WO	0x0	sys_icr_awb_done Clear interrupt
3	WO	0x0	sys_icr_pic_size_err Clear interrupt
2	WO	0x0	sys_icr_data_loss Clear interrupt
1	WO	0x0	sys_icr_frame Clear interrupt
0	WO	0x0	sys_icr_isp_off Clear interrupt

ISP_0400_ISP_ISR

Address: Operational Base(0xFF3F0400) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	WO	0x0	sys_isr_fetch_lut_end Set interrupt
29	WO	0x0	sys_isr_baynr_frame_end Set interrupt
28	WO	0x0	sys_isr_bay3d_post_st Set interrupt
27	WO	0x0	sys_isr_bay3d_in_linecnt_done Set interrupt
26	WO	0x0	sys_isr_bay3d_in_done Set interrupt
25	WO	0x0	sys_isr_out_quarter Set interrupt
24	WO	0x0	sys_isr_out_half Set interrupt
23	WO	0x0	sys_isr_out_frm_end Set interrupt
22	WO	0x0	sys_isr_gain_err Set interrupt
21	WO	0x0	sys_isr_dhaz_done Set interrupt
20	WO	0x0	sys_isr_hdr_done Set interrupt
19	RO	0x0	reserved
18	WO	0x0	sys_isr_exp_end Set interrupt
17	WO	0x0	sys_isr_flash_cap Set interrupt
16	WO	0x0	sys_isr_lsc_lut_err Set interrupt
15	WO	0x0	sys_isr_hist_measure_rdy Set interrupt

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Bit	Attr	Reset Value	Description
14	WO	0x0	sys_isr_afm_fin Set interrupt
13	WO	0x0	sys_isr_afm_lum_of Set interrupt
12	WO	0x0	sys_isr_afm_sum_of Set interrupt
11	WO	0x0	sys_isr_shutter_off Set interrupt
10	WO	0x0	sys_isr_shutter_on Set interrupt
9	WO	0x0	sys_isr_flash_off Set interrupt
8	WO	0x0	sys_isr_flash_on Set interrupt
7	WO	0x0	sys_isr_h_start Set interrupt
6	WO	0x0	sys_isr_v_start Set interrupt
5	WO	0x0	sys_isr_frame_in Set interrupt
4	WO	0x0	sys_isr_awb_done Set interrupt
3	WO	0x0	sys_isr_pic_size_err Set interrupt
2	WO	0x0	sys_isr_data_loss Set interrupt
1	WO	0x0	sys_isr_frame Set interrupt
0	WO	0x0	sys_isr_isp_off Set interrupt

ISP_0400_ISP3A_IMSC

Address: Operational Base(0xFF3F0400) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	sw_imsc_sws_3a_ddr_done 1'b1: Enable interrupt 1'b0: Mask out
11	RW	0x0	sw_imsc_rawawb_done 1'b1: Enable interrupt 1'b0: Mask out
10	RW	0x0	sw_imsc_rawaf_done 1'b1: Enable interrupt 1'b0: Mask out
9	RW	0x0	sw_imsc_rawaf_lum_of 1'b1: Enable interrupt 1'b0: Mask out
8	RW	0x0	sw_imsc_rawaf_sum_of 1'b1: Enable interrupt 1'b0: Mask out
7	RW	0x0	sw_imsc_rawhist_ch2_done 1'b1: Enable interrupt 1'b0: Mask out

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Bit	Attr	Reset Value	Description
6	RW	0x0	sw_imsc_rawhist_ch1_done 1'b1: Enable interrupt 1'b0: Mask out
5	RW	0x0	sw_imsc_rawhist_ch0_done 1'b1: Enable interrupt 1'b0: Mask out
4	RW	0x0	sw_imsc_rawhist_big_done 1'b1: Enable interrupt 1'b0: Mask out
3	RW	0x0	sw_imsc_rawae_ch2_done 1'b1: Enable interrupt 1'b0: Mask out
2	RW	0x0	sw_imsc_rawae_ch1_done 1'b1: Enable interrupt 1'b0: Mask out
1	RW	0x0	sw_imsc_rawae_ch0_done 1'b1: Enable interrupt 1'b0: Mask out
0	RW	0x0	sw_imsc_rawae_big_done 1'b1: Enable interrupt 1'b0: Mask out

ISP_0400_ISP3A_RIS

Address: Operational Base(0xFF3F0400) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	ris_sws_3a_ddr_done 3a result write to DDR done flag
11	RO	0x0	ris_rawawb_done RAWAWB module complete
10	RO	0x0	ris_rawaf_done RAWAF module complete
9	RO	0x0	ris_rawaf_lum_of Auto focus luminance overflow
8	RO	0x0	ris_rawaf_sum_of Auto focus sum overflow
7	RO	0x0	ris_rawhist_ch2_done RAWHIST 2channel complete
6	RO	0x0	ris_rawhist_ch1_done RAWHIST 1channel complete
5	RO	0x0	ris_rawhist_ch0_done RAWHIST 0channel complete
4	RO	0x0	ris_rawhist_big_mode RAWHIST BIG module complete
3	RO	0x0	ris_rawae_ch2_done RAWAE 2channel complete
2	RO	0x0	ris_rawae_ch1_done RAWAE 1channel complete
1	RO	0x0	ris_rawae_ch0_done RAWAE 0channel complete
0	RO	0x0	ris_rawae_big_done RAWAE BIG module complete

ISP_0400_ISP3A_MIS

Address: Operational Base(0xFF3F0400) + offset (0x01D8)

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Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	mis_sws_3a_ddr_done 3a result write to DDR done flag
11	RO	0x0	mis_rawawb_done RAWAWB module complete
10	RO	0x0	mis_rawaf_done RAWAF module complete
9	RO	0x0	mis_rawaf_lum_of Auto focus luminance overflow
8	RO	0x0	mis_rawaf_sum_of Auto focus sum overflow
7	RO	0x0	mis_rawhist_ch2_done RAWHIST 2channel complete
6	RO	0x0	mis_rawhist_ch1_done RAWHIST 1channel complete
5	RO	0x0	mis_rawhist_ch0_done RAWHIST 0channel complete
4	RO	0x0	mis_rawhist_big_done RAWHIST BIG module complete
3	RO	0x0	mis_rawae_ch2_done RAWAE 2channel complete
2	RO	0x0	mis_rawae_ch1_done RAWAE 1channel complete
1	RO	0x0	mis_rawae_ch0_done RAWAE 0channel complete
0	RO	0x0	mis_rawae_big_done RAWAE BIG module complete

ISP_0400_ISP3A_ICR

Address: Operational Base(0xFF3F0400) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	WO	0x0	sys_icr_sws_3a_ddr_done Clear interrupt
11	WO	0x0	sys_icr_rawawb_done Clear interrupt
10	WO	0x0	sys_icr_rawaf_done Clear interrupt
9	WO	0x0	sys_icr_rawaf_lum_of Clear interrupt
8	WO	0x0	sys_icr_rawaf_sum_of Clear interrupt
7	WO	0x0	sys_icr_rawhist_ch2_done Clear interrupt
6	WO	0x0	sys_icr_rawhist_ch1_done Clear interrupt
5	WO	0x0	sys_icr_rawhist_ch0_done Clear interrupt
4	WO	0x0	sys_icr_rawhist_big_done Clear interrupt
3	WO	0x0	sys_icr_rawae_ch2_done Clear interrupt
2	WO	0x0	sys_icr_rawae_ch1_done Clear interrupt

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Bit	Attr	Reset Value	Description
1	WO	0x0	sys_icr_rawae_ch0_done Clear interrupt
0	WO	0x0	sys_icr_rawae_big_done Clear interrupt

ISP_0400_ERR

Address: Operational Base(0xFF3F0400) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	rawlsc_lut_err This error is generated by RAWLSC LUT configure error
3	RO	0x0	lsc_lut_err This error is generated by LSC LUT configure error. (This bit will assert high when update this LUT select from DDR mode and can not finish update at vsync period)
2	RO	0x0	outform_size_err Size error is generated in out mux sub-module
1	RO	0x0	is_size_err Size error is generated in image stabilization sub-module
0	RO	0x0	inform_size_err size error is generated in inform sub-module --- ISP_ERR --- Note: For debug purposes the ISP_ERR and ISP_ERR_CLR are implemented. For the case when a PIC_SIZE_ERR interrupt is signaled the SW is able to see in which sub-module this error is generated. Writing to the ISP_ERR_CLR register clears this bit

ISP_0400_ERR_CLR

Address: Operational Base(0xFF3F0400) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	WO	0x0	rawlsc_lut_err_clr This error is cleared
3	WO	0x0	lsc_lut_err_clr This error is cleared
2	WO	0x0	outform_size_err_clr Size error is cleared
1	WO	0x0	is_size_err_clr Size error is cleared
0	WO	0x0	inform_size_err_clr Size error is cleared

ISP_0400_FRAME_COUNT

Address: Operational Base(0xFF3F0400) + offset (0x0244)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RO	0x0	ro_lut_state Fetch lut: 3'b000: Idle 3'b001: Lsc 3'b010: 3dlut 3'b011: Cac 3'b100: Ldch
27:10	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	frame_counter Current frame count of processing --- ISP_FRAME_COUNT --- Note: In the ISP_FRAME_COUNT register the number of processed frames are displayed. For example: If a 8 is programmed into the ISP_ACQ_NR_FRAMES register, a read access to the ISP_FRAME_COUNT register during processing of the first picture shows a 7. After the entire frames are processed the ISP_OFF interrupt is generated and the ISP_FRAME_COUNT has the count zero. In case a "0" is programmed into the ISP_ACQ_NR_FRAMES register (continues mode) the ISP_FRAME_COUNT register keeps the value "0".

ISP_0400_DEBUG1

Address: Operational Base(0xFF3F0400) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_fifo_space2full Space2full status group: [ro_ibuf2_space2full, ro_ibuf1_space2full, ro_ibuf0_space2full, mpfbc_infifo_space2full, ro_r1fifo_space2full, ro_r0fifo_space2full, ro_outfifo_space2full, ro_lafifo_space2full]

ISP_0400_DEBUG2

Address: Operational Base(0xFF3F0400) + offset (0x024C)

Bit	Attr	Reset Value	Description
31	RO	0x0	bay3d_fifo_iir_full Bay3d fifo iir full
30	RO	0x0	bay3d_fifo_cur_full Bay3d fifo current full
29:16	RO	0x0000	outform_vcnt Module outform vertical counter
15:14	RO	0x0	ro_isp2enc_frm_cnt ISP to encoder frame counter Frame counter from mp or isp out. MUX register 0x001c[0].
13:0	RO	0x0000	ro_isp2enc_line_cnt ISP to encoder line counter. Line counter from mp or isp out. MUX register 0x001c[0].

ISP_0400_DEBUG3

Address: Operational Base(0xFF3F0400) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	isp_pipe_ack ISP pipeline group: [mge_val, mge_ack, rawnr_val, rawnr_ack, bay3d_val, bay3d_ack, tmo_val, tmo_ack, gic_val, gic_ack, dbr_val, dbr_ack, debayer_val, debayer_ack, ccm_val, ccm_ack, gamma_out_val, gamma_out_ack, dhaz_val, dhaz_ack, lut3d_val, lut3d_ack, ldch_val, ldch_ack, conv422_val, conv422_ack, ynr_val, ynr_ack, shp_val, shp_ack, cgc_val, cgc_ack, 2'b0, cac_val, cac_ack, isp_out_val, isp_out_ack, isp_in_val, isp_in_ack]

ISP_0400_DEBUG4

Address: Operational Base(0xFF3F0400) + offset (0x0254)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	isp_pipe_ack1 ISP pipeline group1: [28'b0, expd_val, expd_ack, ynr_in_val, ynr_in_ack]

ISP_0400_YNR_LUMA_RCTRL

Address: Operational Base(0xFF3F0400) + offset (0x0290)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_ynr_luma_rdback_rdy YNR luma ahb readback ready flag. Configure sys_ynr_luma_rdback_st, then wait ro_ynr_luma_rdback_rdy = 1.
30	RO	0x0	reserved
29:16	RW	0x0000	sys_ynr_luma_rdback_offs YNR luma ahb readback offset in ram.
15:1	RO	0x0000	reserved
0	W1C	0x0	sys_ynr_luma_rdback_st YNR luma ahb readback start. And sys_ynr_luma_rdback_st is used for internal counter and cross-asynchronous fifo clearing.

ISP_0400_YNR_LUMA_RDATA

Address: Operational Base(0xFF3F0400) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cfg_ynr_luma_rdata YNR luma pixel value. Each pixel occupies 8 bits in cfg_ynr_luma_rdata.

ISP_0400_STITCH_CTRL0

Address: Operational Base(0xFF3F0400) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_stitch_off0 Sensor1 strat offset It has been deleted in isp-lite version.
15:5	RO	0x000	reserved
4:3	RW	0x0	sw_stitch_sen_id Sensor index of current read register. 2'b00: Current read is sensor 0 2'b01: Current read is sensor 1 2'b10: Current read is sensor 2 2'b11: Current read is sensor 3 It has been deleted in isp-lite version.
2:1	RW	0x0	sw_stitch_mode Multi-sensor stitch mode. 2'b00: Two sensor 2'b01: Three sensor 2'b10: Four sensor 2'b11: Reserved It has been deleted in isp-lite version.
0	RW	0x0	sw_stitch_en Multi-sensor stitch enable. 1'b1: Enable 1'b0: Disable It has been deleted in isp-lite version.

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ISP_0400_STITCH_CTRL1

Address: Operational Base(0xFF3F0400) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_stitch_off2 Sensor3 strat offset It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_stitch_off1 Sensor2 strat offset It has been deleted in isp-lite version.

ISP_0400_STITCH_CTRL2

Address: Operational Base(0xFF3F0400) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_lsc_stitch_lut_off2 Lsc sensor3 start lut offset It has been deleted in isp-lite version.
7:4	RW	0x0	sw_lsc_stitch_lut_off1 Lsc sensor2 start lut offset It has been deleted in isp-lite version.
3:0	RW	0x0	sw_lsc_stitch_lut_off0 Lsc sensor1 start lut offset It has been deleted in isp-lite version.

ISP_0400_SLICE_ST_CTRL

Address: Operational Base(0xFF3F0400) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31	RO	0x0	isp_slice_done ISP slice done, stop working. It is pulled up when ro_isp_out_line_cnt is equal to sw_isp_irq_line0.
30	RO	0x0	reserved
29:16	RO	0x0000	ro_isp_out_line_cnt ISP out line counter
15:1	RO	0x0000	reserved
0	W1C	0x0	sys_isp_slice_st ISP slice start. It is used to continue ISP when isp_line_done is pulled up.

2.4.2.5 CTRL

CTRL_0000_VI_ISP_EN

Address: Operational Base(0xFF3F0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	vi_ccl_dis Isp_top enable for all marvin sub_module 1'b0: Isp is disable 1'b1: Isp is enable

CTRL_0000_VI_ISP_PATH

Address: Operational Base(0xFF3F0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28	RW	0x0	sw_bnr2af_sel_en RAWAF data from BAYNR out select bit.
27	RW	0x0	sw_drc2awb_sel_en RAWAWB data from ADRC out select bit.
26	RW	0x0	sw_bnr2awb_sel_en RAWAWB data from BAYNR out select bit.
25:24	RW	0x0	sw_lsc_cfg_path_sel MAIN-LSC and RAW-LSC share the same configuration address space 2'b00: Both MAIN LSC and RAWLSC will be configured and selected MAIN LSC configuration readback data 2'b01: Only MAIN LSC will be configured and selected MAIN LSC configuration readback data 2'b10: Only RAWLSC will be configured and selected RAWLSC configuration readback data
23:22	RW	0x0	sw_3a_rawae012_swap 3A-rawae(hist)0-1 swap: 2'b00: RAWAE0 for StrmCh0, RAWAE1 for StrmCh1, RAWAE2 for StrmCh2; 2'b01: RAWAE0 for StrmCh1, RAWAE1 for StrmCh0, RAWAE2 for StrmCh2; 2'b10: RAWAE0 for StrmCh2, RAWAE1 for StrmCh1, RAWAE2 for StrmCh0;
21:20	RW	0x0	sw_3a_rawawb_sel 2'b00: Gamma-in0 with awb 2'b01: Gamma-in1 with awb 2'b10: Gamma-in2 with awb
19:18	RW	0x0	sw_3a_rawaf_sel 2'b00: Awb0 out path 2'b01: Awb1 out path 2'b10: Awb2 out path 2'b11: Debayer in path
17:16	RW	0x0	sw_3a_rawae_sel 2'b00: Awb0 out path 2'b01: Awb1 out path 2'b10: Awb2 out path 2'b11: Debayer in path
15:0	RO	0x0000	reserved

CTRL_0000_VI_ID

Address: Operational Base(0xFF3F0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x03	ro_isp_version_major Major version
23:16	RO	0x01	ro_isp_version_minor Minor version
15:0	RO	0x2106	ro_isp_version_date Year, Month

CTRL_0000_VI_ISP_CLK_CTRL

Address: Operational Base(0xFF3F0000) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	marvinmi_clk_alwayson Marvin_mi processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
30	RW	0x0	mipi_clk_alwayson Simipi & mipi0 & mipi1 processing clock control, not used now 1'b1: Clock always on 1'b0: Clock auto-gate
29	RW	0x0	rszs_clk_alwayson Rszs processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
28	RW	0x0	jpeg_clk_alwayson Jpeg processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
27	RW	0x0	dpmux_clk_alwayson Dpmux processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
26	RW	0x0	rszm_clk_alwayson Rszm processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
25	RW	0x0	si_clk_alwayson Si processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
24	RW	0x0	ie_clk_alwayson Iemux & ie processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
23	RW	0x0	cp_clk_alwayson Cp processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
22	RW	0x0	mi_raw_rd_clk_on Isp_mi raw read path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
21	RW	0x0	mi_read_clk_on Isp_mi dma read clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
20	RW	0x0	mi_raw1_clk_on Isp_mi raw1 write path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
19	RW	0x0	mi_raw0_clk_on Isp_mi raw0 write path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
18	RW	0x0	mi_sp_clk_on Isp_mi self path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate

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Bit	Attr	Reset Value	Description
17	RW	0x0	mi_y12_clk_on Isp_mi y12 path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
16	RW	0x0	mi_dp_clk_on Isp_mi dpcc path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
15	RW	0x0	mi_jpeg_clk_on Isp_mi jpeg path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
14	RW	0x0	mi_mp_clk_on Isp_mi main path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
13	RW	0x0	mi_ldc_clk_on Isp_mi ldc path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
12	RW	0x0	ldc_ram_clk_on Ldc_ram clock control, for ram 1'b1: Clock always on 1'b0: Clock auto-gate
11	RW	0x0	aclk_isp_clk_on Aclk_isp clock control, for ram 1'b1: Clock always on 1'b0: Clock auto-gate
10	RW	0x0	jpeg_ram_clk_on Jpeg ram clock control, not used now 1'b1: Clock always on 1'b0: Clock auto-gate
9	RW	0x0	rsz_ram_clk_on Rsz ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
8	RW	0x0	isp_ie_ram_clk_on Isp_ie_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
7	RW	0x0	isp_dpcc_ram_clk_on Isp_dpcc_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
6	RW	0x0	isp_dem_ram_clk_on Isp_dem_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
5	RW	0x0	isp_fifo_ram_clk_on Isp_fifo_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
4	RW	0x0	mipi_ram_clk_on Mipi_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate

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Bit	Attr	Reset Value	Description
3	RW	0x0	isp_3a_clk_on 3A processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
2	RW	0x0	isp_yuv_clk_on Yuv path clock control 1'b1: Clock always on 1'b0: Clock auto-gate
1	RW	0x0	isp_rgb_clk_on Rgb path clock control 1'b1: Clock always on 1'b0: Clock auto-gate
0	RW	0x0	isp_raw_clk_on Raw path clock control 1'b1: Clock always on 1'b0: Clock auto-gate

CTRL_0000_VI_ICCL

Address: Operational Base(0xFF3F0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	vi_mpfbc_clk_enable Mpfbc clock enable 1'b1: Processing mode 1'b0: Power safe
13	RW	0x1	vi_brsz_clk_enable Bypass picture resize clock enable 1'b1: Processing mode 1'b0: Power safe
12	RO	0x0	reserved
11	RW	0x1	vi_mipi_clk_enable MIPI interface clock enable 1'b1: Processing mode 1'b0: Power safe
10	RW	0x1	vi_smia_clk_enable SMIA interface clock enable 1'b1: Processing mode 1'b0: Power safe
9	RW	0x1	vi_simp_clk_enable Superimpose clock enable 1'b1: Processing mode 1'b0: Power safe
8	RW	0x1	vi_ie_clk_enable Image effect clock enable 1'b1: Processing mode 1'b0: Power safe
7	RO	0x0	reserved
6	RW	0x1	vi_mi_clk_enable Memory interface clock enable 1'b1: Processing mode 1'b0: Power safe
5	RW	0x1	vi_jpeg_clk_enable JPEG encoder clock enable 1'b1: Processing mode 1'b0: Power safe

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x1	vi_srsz_clk_enable Self picture resize clock enable 1'b1: Processing mode 1'b0: Power safe
3	RW	0x1	vi_mrsz_clk_enable Main picture resize clock enable 1'b1: Processing mode 1'b0: Power safe
2	RO	0x0	reserved
1	RW	0x1	vi_cp_clk_enable Color processing clock enable 1'b1: Processing mode 1'b0: Power safe
0	RW	0x1	vi_isp_clk_enable Isp processing clock enable 1'b1: Processing mode 1'b0: Power safe

CTRL_0000_VI_IRCL

Address: Operational Base(0xFF3F0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	W1C	0x0	arst_safety_isp_done Safety reset isp done.
30	RW	0x0	sw_rst_protect_dis Safety protect reset disable
29:14	RO	0x0000	reserved
13	RW	0x0	vi_3a_soft_rst 3A software reset 1'b0: Processing mode 1'b1: Reset state 3a can be reset by vi_isp_soft_rst too.
12	RO	0x0	reserved
11	RW	0x0	vi_mipi_soft_rst MIPI Interface software reset 1'b0: Processing mode 1'b1: Reset state
10	RW	0x0	vi_smia_soft_rst SMIA Interface software reset, not used now
9	RW	0x0	vi_simp_soft_rst Superimpose software reset 1'b0: Processing mode 1'b1: Reset state
8	RW	0x0	vi_ie_soft_rst Image effect software reset 1'b0: Processing mode 1'b1: Reset state
7	W1C	0x0	vi_marvin_rst Hardware reset of entire marvin, global reset when high valid 1'b0: Processing mode 1'b1: Reset state
6	RW	0x0	vi_mi_soft_rst Memory interface software reset 1'b0: Processing mode 1'b1: Reset state

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	vi_jpeg_soft_rst JPEG encoder software reset 1'b0: Processing mode 1'b1: Reset state
4	RW	0x0	vi_srsz_soft_rst Self-picture resize software reset 1'b0: Processing mode 1'b1: Reset state
3	RW	0x0	vi_mrsz_soft_rst Main-picture resize software reset 1'b0: Processing mode 1'b1: Reset state
2	RW	0x0	vi_ycs_soft_rst Y/C splitter software reset 1'b0: Processing mode 1'b1: Reset state
1	RW	0x0	vi_cp_soft_rst Color processing software reset 1'b0: Processing mode 1'b1: Reset state
0	RW	0x0	vi_isp_soft_rst Isp software reset 1'b0: Processing mode 1'b1: Reset state

CTRL_0000_VI_DPCL

Address: Operational Base(0xFF3F0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	vi_mi_debug_mode Vi_mi_debug_mode, open clock-gating used
13	RW	0x0	vi_old_mi_sel_rd Vi_old_mi_sel_rd, open clock-gating used
12	RW	0x0	vi_old_mi_sel_wr Vi_old_mi_sel_wr, open clock-gating used
11	RW	0x0	vi_dma_spmux 1'b0: Data from camera interface to self resize 1'b1: Data from DMA read port to self resize
10	RW	0x0	vi_dma_iemux 1'b0: Data from camera interface to image effects 1'b1: Data from DMA read port to image effects
9:8	RW	0x0	if_select selects input interface 2'd0: Parallel interface 2'd1: LVDS interface 2'd2: MIPI interface 2'd3: Reserved
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	vi_dma_switch DMA read data path selector 0: Path to SPMUX 1: Path to Superimpose 2: Path to Image Effects 3: Reserved 4: Path to ISP Bayer RGB 5: Path to ISP YCNR 6~7: Reserved
3:2	RW	0x0	vi_chan_mode Y/C splitter channel mode 2'd0: Disabled 2'd1: Main path and raw data mode 2'd2: Self path mode 2'd3: Main and self path mode
1:0	RW	0x0	vi_mp_mux Data path selector for main path 2'b00: Data from DMA read port to JPEG encoder 2'b01: Data from main resize to MI, uncompressed 2'b10: Data from main resize to JPEG encoder 2'b11: Reserved

CTRL_0000_SWS_CFG

Address: Operational Base(0xFF3F0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RO	0x0	isp2pp_hold Enc2isp pipeline hold, read only
30	RO	0x0	reserved
29	RO	0x0	sws_working Sws_working for 3a writing status
28	RO	0x0	reserved
27	RW	0x0	sw_clk_dsu_gate_en 1'b0: Clock off during reset 1'b1: Clock on during reset Note: No cross asynchronization for different clock domain
26	RW	0x0	sw_3d_dbr_start_mode 3A begin to write DDR mode 1'b0: After debayer end and all module end 1'b1: Just after debayer end
25	RW	0x0	sw_mipi2isp_fifo_dis V_blank hold fifo disable, backdoor
24	RW	0x0	sw_3a_ddr_write_en 3A result load to DDR enable
23:4	RO	0x00000	reserved
3	RW	0x0	sw_ack_frm_pro_dis Vblank optimize disable
2	RW	0x0	sw_mipi_drop_frm_dis Mipi drop frame disable 1'b0: Enable, default 1'b1: Disable Note: only mipi on-the-fly mode needs to use drop frame
1	RW	0x0	sw_isp2pp_pipe_en Isp2pp or isp2enc pipeline handshake, would hold isp pipe when enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_isp2enc_cnt_mux Isp2enc line counter mux. 1'b0: line counter from mp out 1'b1: line counter from isp out

2.4.2.6 BLS

ISP_BLS_3000_CTRL

Address: Operational Base(0xFF3F3000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	bls_working BLS working signal
29:6	RO	0x000000	reserved
5	RW	0x0	sw_bls2_en BLS2 module before rawlsc only used for RAWAWB.
4	RW	0x0	sw_bls1_en BLS1 module after baynr 1'b1: Black level subtraction is enabled 1'b0: Bypass the black level processing
3:2	RW	0x0	sw_bls_win_en 2'b00: No measuring is performed 2'b01: Only window 1 is measured 2'b10: Only window 2 is measured 2'b11: Both windows are measured
1	RW	0x0	sw_bls_mode 1'b1: Subtract measured values 1'b0: Subtract fixed values
0	RW	0x0	sw_bls_en 1'b1: Black level subtraction is enabled 1'b0: Bypass the black level processing

ISP_BLS_3000_SAMPLES

Address: Operational Base(0xFF3F3000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	sw_bls_samples This number to the power of two gives the number of measure samples for each Bayer position. Range 0x00: 2^0=1 to 0x12: 2^18=262144. This number is also the divider for the accumulator for each Bayer position. The accumulation will be stopped, if the number of measured pixels for the current Bayer position is equal to the number of samples. The measure windows must be positioned that way that the number of included pixels of each Bayer position included by both windows is equal or greater than the number of measure samples calculated by 2^BLS_SAMPLES. NOTE: The number of pixels of one Bayer position is 1/4 of the number of all Pixels included by the measure windows.

ISP_BLS_3000_H1_START

Address: Operational Base(0xFF3F3000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_bls_h1_start Black pixel window 1 horizontal start position

ISP_BLS_3000_H1_STOP

Address: Operational Base(0xFF3F3000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_h1_stop Black pixel window 1 horizontal stop position

ISP_BLS_3000_V1_START

Address: Operational Base(0xFF3F3000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_v1_start Black pixel window 1 vertical start position

ISP_BLS_3000_V1_STOP

Address: Operational Base(0xFF3F3000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_v1_stop Black pixel window 1 vertical stop position

ISP_BLS_3000_H2_START

Address: Operational Base(0xFF3F3000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_h2_start Black pixel window 2 horizontal start position

ISP_BLS_3000_H2_STOP

Address: Operational Base(0xFF3F3000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_h2_stop Black pixel window 2 horizontal stop position

ISP_BLS_3000_V2_START

Address: Operational Base(0xFF3F3000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_v2_start Black pixel window 2 vertical start position

ISP_BLS_3000_V2_STOP

Address: Operational Base(0xFF3F3000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_v2_stop Black pixel window 2 vertical stop position

ISP_BLS_3000_BLC0_A_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls_a_fixed Fixed black level for A pixels. Signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values.

ISP_BLS_3000_BLC0_B_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls_b_fixed Fixed black level for B pixels. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLC0_C_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls_c_fixed Fixed black level for C pixels. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLC0_D_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls_d_fixed Fixed black level for D pixels. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_A_MEASURED

Address: Operational Base(0xFF3F3000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_bls_a_measured Measured black level for A pixels

ISP_BLS_3000_B_MEASURED

Address: Operational Base(0xFF3F3000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_bls_b_measured Measured black level for B pixels

ISP_BLS_3000_C_MEASURED

Address: Operational Base(0xFF3F3000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_bls_c_measured Measured black level for C pixels

ISP_BLS_3000_D_MEASURED

Address: Operational Base(0xFF3F3000) + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_bls_d_measured Measured black level for D pixels

ISP_BLS_3000_BLS1_A_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls1_a_fixed Fixed black level for A pixels of bay3dnr-blc ; Signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values.

ISP_BLS_3000_BLS1_B_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls1_b_fixed Fixed black level for B pixels of bay3dnr-blc. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLS1_C_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:1	RW	0x0000	sw_bls1_c_fixed Fixed black level for C pixels of bay3dnr-blc. Signed two's complement, value range from -4096 to +4095.
0	RO	0x0	reserved

ISP_BLS_3000_BLS1_D_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls1_d_fixed Fixed black level for D pixels of bay3dnr-blc. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLS2_A_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls2_a_fixed Fixed black level for A pixels of 3a-awb. Signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values.

ISP_BLS_3000_BLS2_B_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls2_b_fixed Fixed black level for B pixels of 3a-awb. Signed two's complement, value range from -4096 to +4095.

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ISP_BLS_3000_BLS2_C_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:1	RW	0x0000	sw_bls2_c_fixed Fixed black level for C pixels of 3a-awb. Signed two's complement, value range from -4096 to +4095.
0	RO	0x0	reserved

ISP_BLS_3000_BLS2_D_FIXED

Address: Operational Base(0xFF3F3000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls2_d_fixed Fixed black level for D pixels of 3a-awb. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_ISP_OB_OFFSET

Address: Operational Base(0xFF3F3000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	sw_isp_ob_offset Add OB_offset for protecting dark texture(low 9bit in 12bit), if not equal to zero then bls1 will auto-enable

ISP_BLS_3000_ISP_OB_PREDGAIN

Address: Operational Base(0xFF3F3000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0100	sw_isp_ob_predgain OB pre-dgain{8,8} for replacing adrc-gain, in linear mode

ISP_BLS_3000_ISP_OB_MAX

Address: Operational Base(0xFF3F3000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_isp_ob_max AWB1 max value clip, value equal to predgain*0xfff

2.4.2.7 DPCC

ISP_DPCC_3400_MODE

Address: Operational Base(0xFF3F3400) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	dpcc_working DPCC working signal
29:3	RO	0x0000000	reserved
2	RW	0x1	stage1_enable 1'b0: Bypass stage1 1'b1: Enable stage1

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Bit	Attr	Reset Value	Description
1	RW	0x0	grayscale_mode 1'b0: BAYER DATA INPUT 1'b1: Enable gray scale data input from black and white sensors (without color filter array)
0	RW	0x0	isp_dpcc_enable 1'b0: Bypass DPCC 1'b1: Enable DPCC

ISP_DPCC_3400_OUTPUT_MODE

Address: Operational Base(0xFF3F3400) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	sw_dpcc_border_bypss_mode 1'b0: Border do DPCC 1'b1: Border(left and right two colum) output bypass
7	RO	0x0	reserved
6:5	RW	0x0	sw_roc_out_sel 2'b00: ROC(Rank Order Check) method1 2'b01: ROC method2 2'b10: ROC method3 2'b11: Reserved
4	RW	0x0	sw_dpcc_output_sel 1'b0: Select median mode 1'b1: Select ROC output mode
3	RW	0x0	stage1_rb_3x3 1'b0: Stage1 red/blue 4 or 5 pixel output median 1'b1: Stage1 red/blue 9 pixel (3x3) output median
2	RW	0x0	stage1_g_3x3 1'b0: Stage1 green 4 or 5 pixel output median 1'b1: Stage1 green 9 pixel (3x3) output median
1	RW	0x1	stage1_incl_rb_center 1'b0: Stage1 do not include center pixel for red/blue output median 2x2 1'b1: Stage1 include center pixel for red/blue output median 2x2+1
0	RW	0x1	stage1_incl_green_center 1'b0: Stage1 do not include center pixel for green output median 2x2 1'b1: Stage1 include center pixel for green output median 2x2+1

ISP_DPCC_3400_SET_USE

Address: Operational Base(0xFF3F3400) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	stage1_use_fix_set 1'b0: Stage1 do not use hard coded methods set 1'b1: Stage1 use hard coded methods set
2	RW	0x1	stage1_use_set_3 1'b0: Stage1 do not use methods set 3 1'b1: Stage1 use methods set 3
1	RW	0x1	stage1_use_set_2 1'b0: Stage1 do not use methods set 2 1'b1: Stage1 use methods set 2

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Bit	Attr	Reset Value	Description
0	RW	0x1	stage1_use_set_1 1'b0: Stage1 do not use methods set 1 1'b1: Stage1 use methods set 1 --- ISP_DPCC_SET_USE --- Note: methods sets can be used in parallel for each stage and the result is the logical OR of all selected sets

ISP_DPCC_3400_METHODS_SET_1

Address: Operational Base(0xFF3F3400) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	sw_roc_red_blue1_en 1'b0: Bypass ROC method check for green 1'b1: Enable ROC method check for green
12	RW	0x1	rg_red_blue1_enable 1'b0: Bypass rank gradient check for red_blue 1'b1: Enable rank gradient check for red_blue
11	RW	0x1	rnd_red_blue1_enable 1'b0: Bypass rank neighbor difference check for red_blue 1'b1: Enable rank neighbor difference check for red_blue
10	RW	0x1	ro_red_blue1_enable 1'b0: Bypass rank order check for red_blue 1'b1: Enable rank order check for red_blue
9	RW	0x0	lc_red_blue1_enable 1'b0: Bypass line check for red_blue 1'b1: Enable line check for red_blue
8	RW	0x1	pg_red_blue1_enable 1'b0: Bypass peak gradient check for red_blue 1'b1: Enable peak gradient check for red_blue
7:6	RO	0x0	reserved
5	RW	0x0	sw_roc_green1_en 1'b0: Bypass ROC method check for green 1'b1: Enable ROC method check for green
4	RW	0x1	rg_green1_enable 1'b0: Bypass rank gradient check for green 1'b1: Enable rank gradient check for green
3	RW	0x1	rnd_green1_enable 1'b0: Bypass rank neighbor difference check for green 1'b1: Enable rank neighbor difference check for green
2	RW	0x1	ro_green1_enable 1'b0: Bypass rank order check for green 1'b1: Enable rank order check for green
1	RW	0x0	lc_green1_enable 1'b0: Bypass line check for green 1'b1: Enable line check for green
0	RW	0x1	pg_green1_enable 1'b0: Bypass peak gradient check for green 1'b1: Enable peak gradient check for green --- ISP_DPCC_METHODS_SET_1 --- Note: Different methods can be used in parallel, the result is the logical AND of all selected methods

ISP_DPCC_3400_METHODS_SET_2

Address: Operational Base(0xFF3F3400) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	sw_roc_red_blue2_en 1'b0: Bypass ROC method check for green 1'b1: Enable ROC method check for green
12	RW	0x0	rg_red_blue2_enable 1'b0: Bypass rank gradient check for red_blue 1'b1: Enable rank gradient check for red_blue
11	RW	0x0	rnd_red_blue2_enable 1'b0: Bypass rank neighbor difference check for red_blue 1'b1: Enable rank neighbor difference check for red_blue
10	RW	0x1	ro_red_blue2_enable 1'b0: Bypass rank order check for red_blue 1'b1: Enable rank order check for red_blue
9	RW	0x1	lc_red_blue2_enable 1'b0: Bypass line check for red_blue 1'b1: Enable line check for red_blue
8	RW	0x1	pg_red_blue2_enable 1'b0: Bypass peak gradient check for red_blue 1'b1: Enable peak gradient check for red_blue
7:6	RO	0x0	reserved
5	RW	0x0	sw_roc_green2_en 1'b0: Bypass ROC method check for green 1'b1: Enable ROC method check for green
4	RW	0x0	rg_green2_enable 1'b0: Bypass rank gradient check for green 1'b1: Enable rank gradient check for green
3	RW	0x0	rnd_green2_enable 1'b0: Bypass rank neighbor difference check for green 1'b1: Enable rank neighbor difference check for green
2	RW	0x1	ro_green2_enable 1'b0: Bypass rank order check for green 1'b1: Enable rank order check for green
1	RW	0x1	lc_green2_enable 1'b0: Bypass line check for green 1'b1: Enable line check for green
0	RW	0x1	pg_green2_enable 1'b0: Bypass peak gradient check for green 1'b1: Enable peak gradient check for green --- ISP_DPCC_METHODS_SET_2 --- Note: Different methods can be used in parallel, the result is the logical AND of all selected methods

ISP_DPCC_3400_METHODS_SET_3

Address: Operational Base(0xFF3F3400) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	sw_roc_red_blue3_en 1'b0: Bypass ROC method check for green 1'b1: Enable ROC method check for green
12	RW	0x1	rg_red_blue3_enable 1'b0: Bypass rank gradient check for red_blue 1'b1: Enable rank gradient check for red_blue
11	RW	0x1	rnd_red_blue3_enable 1'b0: Bypass rank neighbor difference check for red_blue 1'b1: Enable rank neighbor difference check for red_blue

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Bit	Attr	Reset Value	Description
10	RW	0x1	ro_red_blue3_enable 1'b0: Bypass rank order check for red_blue 1'b1: Enable rank order check for red_blue
9	RW	0x1	lc_red_blue3_enable 1'b0: Bypass line check for red_blue 1'b1: Enable line check for red_blue
8	RW	0x1	pg_red_blue3_enable 1'b0: Bypass peak gradient check for red_blue 1'b1: Enable peak gradient check for red_blue
7:6	RO	0x0	reserved
5	RW	0x0	sw_roc_green3_en 1'b0: Bypass ROC method check for green 1'b1: Enable ROC method check for green
4	RW	0x1	rg_green3_enable 1'b0: Bypass rank gradient check for green 1'b1: Enable rank gradient check for green
3	RW	0x1	rnd_green3_enable 1'b0: Bypass rank neighbor difference check for green 1'b1: Enable rank neighbor difference check for green
2	RW	0x1	ro_green3_enable 1'b0: Bypass rank order check for green 1'b1: Enable rank order check for green
1	RW	0x1	lc_green3_enable 1'b0: Bypass line check for green 1'b1: Enable line check for green
0	RW	0x1	pg_green3_enable 1'b0: Bypass peak gradient check for green 1'b1: Enable peak gradient check for green --- ISP_DPCC_METHODS_SET_3 --- Note: Different methods can be used in parallel, the result is the logical AND of all selected methods

ISP_DPCC_3400_LINE_THRESH_1

Address: Operational Base(0xFF3F3400) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_mindis1_rb Min distance for set 1 red /blue
23:16	RW	0x00	sw_mindis1_g Min distance for set 1 green
15:8	RW	0x08	line_thr_1_rb Line threshold for set 1 red/blue
7:0	RW	0x08	line_thr_1_g Line threshold for set 1 green --- ISP_DPCC_LINE_THRESH_1 --- Note: All values are unsigned integer

ISP_DPCC_3400_LINE_MAD_FAC_1

Address: Operational Base(0xFF3F3400) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dis_scale_min1 Distance scale for min channel
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dis_scale_max1 Distance scale for max channel

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:8	RW	0x04	line_mad_fac_1_rb Line MAD factor for set 1 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x04	line_mad_fac_1_g Line MAD factor for set 1 green --- ISP_DPCC_LINE_MAD_FAC_1 --- Note: All values are unsigned integer

ISP_DPCC_3400_PG_FAC_1

Address: Operational Base(0xFF3F3400) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	pg_fac_1_rb Peak gradient factor for set 1 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x03	pg_fac_1_g Peak gradient factor for set 1 green --- ISP_DPCC_PG_FAC_1 --- Note: All values are unsigned integer

ISP_DPCC_3400_RND_THRESH_1

Address: Operational Base(0xFF3F3400) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0a	rnd_thr_1_rb Rank Neighbor Difference threshold for set 1 red/blue
7:0	RW	0x0a	rnd_thr_1_g Rank Neighbor Difference threshold for set 1 green --- ISP_DPCC_RND_THRESH_1 --- Note: All values are unsigned integer

ISP_DPCC_3400_RG_FAC_1

Address: Operational Base(0xFF3F3400) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x20	rg_fac_1_rb Rank gradient factor for set 1 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x20	rg_fac_1_g Rank gradient factor for set 1 green --- ISP_DPCC_RG_FAC_1 --- Note: All values are unsigned integer

ISP_DPCC_3400_LINE_THRESH_2

Address: Operational Base(0xFF3F3400) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_mindis2_rb Min distance for set 2 red /blue
23:16	RW	0x00	sw_mindis2_g Min distance for set 2 green
15:8	RW	0x10	line_thr_2_rb Line threshold for set 2 red/blue

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Bit	Attr	Reset Value	Description
7:0	RW	0x0c	line_thr_2_g Line threshold for set 2 green --- ISP_DPCC_LINE_THRESH_2 --- Note: All values are unsigned integer

ISP_DPCC_3400_LINE_MAD_FAC_2

Address: Operational Base(0xFF3F3400) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dis_scale_min2 Distance scale for min channel
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dis_scale_max2 Distance scale for max channel
15:14	RO	0x0	reserved
13:8	RW	0x18	line_mad_fac_2_rb Line MAD factor for set 2 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x10	line_mad_fac_2_g Line MAD factor for set 2 green --- ISP_DPCC_LINE_MAD_FAC_2 --- Note: All values are unsigned integer

ISP_DPCC_3400_PG_FAC_2

Address: Operational Base(0xFF3F3400) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	pg_fac_2_rb Peak gradient factor for set 2 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x03	pg_fac_2_g Peak gradient factor for set 2 green --- ISP_DPCC_PG_FAC_2 --- Note: All values are unsigned integer

ISP_DPCC_3400_RND_THRESH_2

Address: Operational Base(0xFF3F3400) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x08	rnd_thr_2_rb Rank Neighbor Difference threshold for set 2 red/blue
7:0	RW	0x08	rnd_thr_2_g Rank Neighbor Difference threshold for set 2 green --- ISP_DPCC_RND_THRESH_2 --- Note: All values are unsigned integer

ISP_DPCC_3400_RG_FAC_2

Address: Operational Base(0xFF3F3400) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x08	rg_fac_2_rb Rank gradient factor for set 2 red/blue
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x08	rg_fac_2_g Rank gradient factor for set 2 green --- ISP_DPCC_RG_FAC_2 --- Note: All values are unsigned integer

ISP_DPCC_3400_LINE_THRESH_3

Address: Operational Base(0xFF3F3400) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_mindis3_rb Min distance for set 3 red /blue
23:16	RW	0x00	sw_mindis3_g Min distance for set 3 green
15:8	RW	0x20	line_thr_3_rb Line threshold for set 3 red/blue
7:0	RW	0x20	line_thr_3_g Line threshold for set 3 green --- ISP_DPCC_LINE_THRESH_3 --- Note: All values are unsigned integer

ISP_DPCC_3400_LINE_MAD_FAC_3

Address: Operational Base(0xFF3F3400) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dis_scale_min3 Distance scale for min channel
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dis_scale_max3 Distance scale for max channel
15:14	RO	0x0	reserved
13:8	RW	0x04	line_mad_fac_3_rb Line MAD factor for set 3 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x04	line_mad_fac_3_g Line MAD factor for set 3 green --- ISP_DPCC_LINE_MAD_FAC_3 --- Note: All values are unsigned integer

ISP_DPCC_3400_PG_FAC_3

Address: Operational Base(0xFF3F3400) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	pg_fac_3_rb Peak gradient factor for set 3 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x03	pg_fac_3_g Peak gradient factor for set 3 green --- ISP_DPCC_PG_FAC_3 --- Note: All values are unsigned integer

ISP_DPCC_3400_RND_THRESH_3

Address: Operational Base(0xFF3F3400) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x08	rnd_thr_3_rb Rank Neighbor Difference threshold for set 3 red/blue

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Bit	Attr	Reset Value	Description
7:0	RW	0x06	rnd_thr_3_g Rank Neighbor Difference threshold for set 3 green --- ISP_DPCC_RND_THRESH_3 --- Note: All values are unsigned integer

ISP_DPCC_3400_RG_FAC_3

Address: Operational Base(0xFF3F3400) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	rg_fac_3_rb Rank gradient factor for set 3 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x04	rg_fac_3_g Rank gradient factor for set 3 green --- ISP_DPCC_RG_FAC_3 --- Note: All values are unsigned integer

ISP_DPCC_3400_RO_LIMITS

Address: Operational Base(0xFF3F3400) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:10	RW	0x2	ro_lim_3_rb Rank order limit for set 3 red/blue
9:8	RW	0x2	ro_lim_3_g Rank order limit for set 3 green
7:6	RW	0x0	ro_lim_2_rb Rank order limit for set 2 red/blue
5:4	RW	0x0	ro_lim_2_g Rank order limit for set 2 green
3:2	RW	0x2	ro_lim_1_rb Rank order limit for set 1 red/blue
1:0	RW	0x2	ro_lim_1_g Rank order limit for set 1 green --- ISP_DPCC_RO_LIMITS --- Note: All values are unsigned integer

ISP_DPCC_3400_RND_OFFS

Address: Operational Base(0xFF3F3400) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:10	RW	0x3	rnd_offs_3_rb Rank Offset to Neighbor for set 3 red/blue
9:8	RW	0x3	rnd_offs_3_g Rank Offset to Neighbor for set 3 green
7:6	RW	0x3	rnd_offs_2_rb Rank Offset to Neighbor for set 2 red/blue
5:4	RW	0x3	rnd_offs_2_g Rank Offset to Neighbor for set 2 green
3:2	RW	0x3	rnd_offs_1_rb Rank Offset to Neighbor for set 1 red/blue
1:0	RW	0x3	rnd_offs_1_g Rank Offset to Neighbor for set 1 green --- ISP_DPCC_RND_OFFS --- Note: All values are unsigned integer

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ISP_DPCC_3400_BPT_CTRL

Address: Operational Base(0xFF3F3400) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	bpt_rb_3x3 1'b0: If BPT active red/blue 4 or 5 pixel output median 1'b1: If BPT active red/blue 9 pixel (3x3) output median
10	RW	0x0	bpt_g_3x3 1'b0: If BPT active green 4 or 5 pixel output median 1'b1: If BPT active green 9 pixel (3x3) output median
9	RW	0x0	bpt_incl_rb_center 1'b0: If BPT active do not include center pixel for red/blue output median 2x2 1'b1: If BPT active include center pixel for red/blue output median 2x2+1
8	RW	0x0	bpt_incl_green_center 1'b0: If BPT active do not include center pixel for green output median 2x2 1'b1: If BPT active include center pixel for green output median 2x2+1
7	RW	0x0	bpt_use_fix_set 1'b0: For BPT write do not use hard coded methods set 1'b1: For BPT write use hard coded methods set
6	RW	0x0	bpt_use_set_3 1'b0: For BPT write do not use methods set 3 1'b1: For BPT write use methods set 3
5	RW	0x0	bpt_use_set_2 1'b0: For BPT write do not use methods set 2 1'b1: For BPT write use methods set 2
4	RW	0x0	bpt_use_set_1 1'b0: For BPT write do not use methods set 1 1'b1: For BPT write use methods set 1
3:2	RO	0x0	reserved
1	RW	0x0	bpt_cor_en table based correction enable 1'b1: Table based correction is enabled 1'b0: Table based correction is disabled
0	RW	0x0	bpt_det_en Bad pixel detection write enable 1'b1: Bad pixel detection write to memory is enabled 1'b0: Bad pixel detection write to memory is disabled --- ISP_DPCC_BPT_CTRL --- Note: This register controls the behaviour of the table based bad pixel correction module. It can be switched on and off independently of the DPCC detection and correction block. Different correction algorithms for the table based correction are available and are defined by this register. The default setting after reset enables a correction algorithm with most accurate correlation to surrounding pixels. Detection for the table based correction can be configured independently from the on-the-fly DPCC detection scheme

ISP_DPCC_3400_BPT_NUMBER

Address: Operational Base(0xFF3F3400) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	bp_number Number of current Bad Pixel entries in bad pixel table (BPT) --- ISP_DPCC_BPT_NUMBER --- Note: Bit width of bp_number depends on size of BP RAM which is defined during chip synthesis

ISP_DPCC_3400_BPT_ADDR

Address: Operational Base(0xFF3F3400) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	bp_table_addr Table RAM start address for read or write operations. The address counter is incremented at each read or write access to the data register (auto-increment mechanism)

ISP_DPCC_3400_BPT_DATA

Address: Operational Base(0xFF3F3400) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	bpt_v_addr Bad Pixel vertical address (pixel position)
15:13	RO	0x0	reserved
12:0	RO	0x0000	bpt_h_addr Bad Pixel horizontal address (pixel position) --- ISP_DPCC_BPT_DATA --- The programmed table value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits)

ISP_DPCC_3400_BP_CNT

Address: Operational Base(0xFF3F3400) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	bp_cnt Number of current bad pixel counter

ISP_DPCC_3400_PDAF_EN

Address: Operational Base(0xFF3F3400) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_pdaf_en PDAF point replace enable bit

ISP_DPCC_3400_PDAF_POINT_EN

Address: Operational Base(0xFF3F3400) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sw_pdaf_point15_en Point15 replace enable bit
14	RW	0x0	sw_pdaf_point14_en Point14 replace enable bit
13	RW	0x0	sw_pdaf_point13_en Point13 replace enable bit

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Bit	Attr	Reset Value	Description
12	RW	0x0	sw_pdaf_point12_en Point12 replace enable bit
11	RW	0x0	sw_pdaf_point11_en Point11 replace enable bit
10	RW	0x0	sw_pdaf_point10_en Point10 replace enable bit
9	RW	0x0	sw_pdaf_point9_en Point9 replace enable bit
8	RW	0x0	sw_pdaf_point8_en Point8 replace enable bit
7	RW	0x0	sw_pdaf_point7_en Point7 replace enable bit
6	RW	0x0	sw_pdaf_point6_en Point6 replace enable bit
5	RW	0x0	sw_pdaf_point5_en Point5 replace enable bit
4	RW	0x0	sw_pdaf_point4_en Point4 replace enable bit
3	RW	0x0	sw_pdaf_point3_en Point3 replace enable bit
2	RW	0x0	sw_pdaf_point2_en Point2 replace enable bit
1	RW	0x0	sw_pdaf_point1_en Point1 replace enable bit
0	RW	0x0	sw_pdaf_point0_en Point0 replace enable bit

ISP_DPCC_3400_PDAF_OFFSET

Address: Operational Base(0xFF3F3400) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_pdaf_offsety The beginning y coordinate of pdaf pattern
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_pdaf_offsetx The beginning x coordinate of pdaf pattern

ISP_DPCC_3400_PDAF_WRAP

Address: Operational Base(0xFF3F3400) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_pdaf_wrapy The height of pattren , 0x00 is 1, 0x0f is 16
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_pdaf_wrapx The width of pattren , 0x00 is 1, 0x0f is 16

ISP_DPCC_3400_PDAF_SCOPE

Address: Operational Base(0xFF3F3400) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_pdaf_wrapy_num The num of wrapy
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_pdaf_wrapx_num The num of wrapx

ISP_DPCC_3400_PDAF_POINT_0

Address: Operational Base(0xFF3F3400) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point1_y Point1 y coordinate
23:16	RW	0x00	sw_pdaf_point1_x Point1 x coordinate
15:8	RW	0x00	sw_pdaf_point0_y Point0 y coordinate
7:0	RW	0x00	sw_pdaf_point0_x Point0 x coordinate

ISP_DPCC_3400_PDAF_POINT_1

Address: Operational Base(0xFF3F3400) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point3_y Point3 y coordinate
23:16	RW	0x00	sw_pdaf_point3_x Point3 x coordinate
15:8	RW	0x00	sw_pdaf_point2_y Point2 y coordinate
7:0	RW	0x00	sw_pdaf_point2_x Point2 x coordinate

ISP_DPCC_3400_PDAF_POINT_2

Address: Operational Base(0xFF3F3400) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point5_y Point5 y coordinate
23:16	RW	0x00	sw_pdaf_point5_x Point5 x coordinate
15:8	RW	0x00	sw_pdaf_point4_y Point4 y coordinate
7:0	RW	0x00	sw_pdaf_point4_x Point4 x coordinate

ISP_DPCC_3400_PDAF_POINT_3

Address: Operational Base(0xFF3F3400) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point7_y Point7 y coordinate
23:16	RW	0x00	sw_pdaf_point7_x Point7 x coordinate
15:8	RW	0x00	sw_pdaf_point6_y Point6 y coordinate
7:0	RW	0x00	sw_pdaf_point6_x Point6 x coordinate

ISP_DPCC_3400_PDAF_POINT_4

Address: Operational Base(0xFF3F3400) + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point9_y Point9 y coordinate
23:16	RW	0x00	sw_pdaf_point9_x Point9 x coordinate
15:8	RW	0x00	sw_pdaf_point8_y Point8 y coordinate
7:0	RW	0x00	sw_pdaf_point8_x Point8 x coordinate

ISP_DPCC_3400_PDAF_POINT_5

Address: Operational Base(0xFF3F3400) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point11_y Point11 y coordinate
23:16	RW	0x00	sw_pdaf_point11_x Point11 x coordinate
15:8	RW	0x00	sw_pdaf_point10_y Point10 y coordinate
7:0	RW	0x00	sw_pdaf_point10_x Point10 x coordinate

ISP_DPCC_3400_PDAF_POINT_6

Address: Operational Base(0xFF3F3400) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point13_y Point13 y coordinate
23:16	RW	0x00	sw_pdaf_point13_x Point13 x coordinate
15:8	RW	0x00	sw_pdaf_point12_y Point12 y coordinate
7:0	RW	0x00	sw_pdaf_point12_x Point12 x coordinate

ISP_DPCC_3400_PDAF_POINT_7

Address: Operational Base(0xFF3F3400) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point15_y Point15 y coordinate
23:16	RW	0x00	sw_pdaf_point15_x Point15 x coordinate
15:8	RW	0x00	sw_pdaf_point14_y Point14 y coordinate
7:0	RW	0x00	sw_pdaf_point14_x Point14 x coordinate

ISP_DPCC_3400_PDAF_FORWARD_MED

Address: Operational Base(0xFF3F3400) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_pdaf_forward_med 1'b0: Select backward median value to replace pdaf point 1'b1: Select forward median value to replace pdaf point

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2.4.2.8 HDRMGE

ISP_HDRMGE_3800_CTRL

Address: Operational Base(0xFF3F3800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_hdrmge_en_shd HDR-Merge enable shadow
30	RO	0x0	ro_hdrmge_working Hdrmge working status
29:7	RO	0x000000	reserved
6	RW	0x0	sw_hdrmge_each_raw_en Enable each_raw merge for noise reduce
5:4	RW	0x0	sw_hdrmge_dbg_mode Merge debug mode 2'b00: Channel0 of S 2'b01: Channel1 of M 2'b10: Channel2 of L
3:2	RW	0x0	sw_hdrmge_mode HDR-Merge mode 2'b00: Normal 2'b01: Framex2 2'b10: Framex3
1	RW	0x0	sw_hdrmge_s_base HDR-Merge hugemsk enable, shadow reg 1'b0: Long base method 1'b1: Short base method
0	RW	0x0	sw_hdrmge_en_i HDR-Merge function enable, shadow reg

ISP_HDRMGE_3800_GAIN0

Address: Operational Base(0xFF3F3800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x100	sw_hdrmge_gain0_inv 1/Short -gain=[0,12}, shadow reg
15:14	RO	0x0	reserved
13:0	RW	0x0400	sw_hdrmge_gain0 Short -gain=[8,6], shadow reg

ISP_HDRMGE_3800_GAIN1

Address: Operational Base(0xFF3F3800) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x400	sw_hdrmge_gain1_inv 1/Middle-gain=[0,12], shadow reg (1106 no use)
15:11	RO	0x00	reserved
10:0	RW	0x100	sw_hdrmge_gain1 Middle-gain=[5,6], shadow reg

ISP_HDRMGE_3800_GAIN2

Address: Operational Base(0xFF3F3800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x40	sw_hdrmge_gain2 Long -gain=[1,6], shadow reg (1106 no use)

ISP_HDRMGE_3800_LIGHTZ

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Address: Operational Base(0xFF3F3800) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_hdrmge_lm_dif_0p15 Merge lm_dif_0p15 for diff-offset of (M_frame*gain1 - L_frame*gain2*0p9)/gain1 + 0p15.
23:16	RW	0xff	sw_hdrmge_lm_dif_0p9 Merge lm_dif_0p9 for diff-scale of (M_frame*gain1 - L_frame*gain2*0p9)/gain1 + 0p15.
15:8	RW	0x00	sw_hdrmge_ms_diff_0p15 Merge ms_0p15 for diff-offset of (S_frame*gain0 - M_frame*gain1*0p8)/gain0 + 0p15.
7:0	RW	0xff	sw_hdrmge_ms_dif_0p8 Merge ms_dif_0p8 for diff-scale of (S_frame*gain0 - M_frame*gain1*0p8)/gain0 + 0p15.

ISP_HDRMGE_3800_MS_DIFF

Address: Operational Base(0xFF3F3800) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:22	RW	0x200	sw_hdrmge_ms_thd1 Threshold-high of ms for clipping diff, [0,10]
21:12	RW	0x000	sw_hdrmge_ms_thd0 Threshold-low of ms for clipping diff, [0,10]
11	RO	0x0	reserved
10:0	RW	0x080	sw_hdrmge_ms_scl Ms-diff*scale[3,8] into range 0-255, {3,8}

ISP_HDRMGE_3800_LM_DIFF

Address: Operational Base(0xFF3F3800) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:22	RW	0x200	sw_hdrmge_lm_thd1 Merge threshold-high of lm for clipping diff, [0,10] (1106 no use)
21:12	RW	0x000	sw_hdrmge_lm_thd0 Merge threshold-low of lm for clipping diff, [0,10] (1106 no use)
11	RO	0x0	reserved
10:0	RW	0x080	sw_hdrmge_lm_scl Merge lm-diff*scale[3,8] into range 0-255, [3,8] (1106 no use)

ISP_HDRMGE_3800_DIFF_Y0

Address: Operational Base(0xFF3F3800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hdrmge_l1_y0 L-curve1 maskUseCur=D of Y0
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_hdrmge_l0_y0 L-curve0 maskUseCur=D of Y0

ISP_HDRMGE_3800_DIFF_Y1

Address: Operational Base(0xFF3F3800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x0c9	sw_hdrmge_l1_y1 L-curve1 maskUseCur=D of Y1
15:10	RO	0x00	reserved
9:0	RW	0x0c9	sw_hdrmge_l0_y1 L-curve0 maskUseCur=D of Y1

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ISP_HDRMGE_3800_DIFF_Y2

Address: Operational Base(0xFF3F3800) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x1fa	sw_hdrmge_l1_y2 L-curve1 maskUseCur=D of Y2
15:10	RO	0x00	reserved
9:0	RW	0x1fa	sw_hdrmge_l0_y2 L-curve0 maskUseCur=D of Y2

ISP_HDRMGE_3800_DIFF_Y3

Address: Operational Base(0xFF3F3800) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x2c0	sw_hdrmge_l1_y3 L-curve1 maskUseCur=D of Y3
15:10	RO	0x00	reserved
9:0	RW	0x2c0	sw_hdrmge_l0_y3 L-curve0 maskUseCur=D of Y3

ISP_HDRMGE_3800_DIFF_Y4

Address: Operational Base(0xFF3F3800) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x32f	sw_hdrmge_l1_y4 L-curve1 maskUseCur=D of Y4
15:10	RO	0x00	reserved
9:0	RW	0x32f	sw_hdrmge_l0_y4 L-curve0 maskUseCur=D of Y4

ISP_HDRMGE_3800_DIFF_Y5

Address: Operational Base(0xFF3F3800) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x370	sw_hdrmge_l1_y5 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x370	sw_hdrmge_l0_y5 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y6

Address: Operational Base(0xFF3F3800) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x397	sw_hdrmge_l1_y6 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x397	sw_hdrmge_l0_y6 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y7

Address: Operational Base(0xFF3F3800) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x3b1	sw_hdrmge_l1_y7 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3b1	sw_hdrmge_l0_y7 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y8

Address: Operational Base(0xFF3F3800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3c2	sw_hdrmge_l1_y8 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3c2	sw_hdrmge_l0_y8 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y9

Address: Operational Base(0xFF3F3800) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3cf	sw_hdrmge_l1_y9 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3cf	sw_hdrmge_l0_y9 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y10

Address: Operational Base(0xFF3F3800) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3d8	sw_hdrmge_l1_y10 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3d8	sw_hdrmge_l0_y10 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y11

Address: Operational Base(0xFF3F3800) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3de	sw_hdrmge_l1_y11 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3de	sw_hdrmge_l0_y11 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y12

Address: Operational Base(0xFF3F3800) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3e4	sw_hdrmge_l1_y12 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x3e4	sw_hdrmge_l0_y12 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y13

Address: Operational Base(0xFF3F3800) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3e8	sw_hdrmge_l1_y13 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3e8	sw_hdrmge_l0_y13 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y14

Address: Operational Base(0xFF3F3800) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3eb	sw_hdrmge_l1_y14 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3eb	sw_hdrmge_l0_y14 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y15

Address: Operational Base(0xFF3F3800) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3ee	sw_hdrmge_l1_y15 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3ee	sw_hdrmge_l0_y15 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y16

Address: Operational Base(0xFF3F3800) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3f0	sw_hdrmge_l1_y16 L-curve1 maskUseCur=D of Y16
15:10	RO	0x00	reserved
9:0	RW	0x3f0	sw_hdrmge_l0_y16 L-curve0 maskUseCur=D of Y16

ISP_HDRMGE_3800_OVER_Y0

Address: Operational Base(0xFF3F3800) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x031	sw_hdrmge_l_raw1_0 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x031	sw_hdrmge_l_raw0_0 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x000	sw_hdrmge_e_y0 E-curve over_exp_normal of Y-0

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ISP_HDRMGE_3800_OVER_Y1

Address: Operational Base(0xFF3F3800) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x057	sw_hdrmge_l_raw1_1 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x057	sw_hdrmge_l_raw0_1 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x001	sw_hdrmge_e_y1 E-curve over_exp_normal of Y-1

ISP_HDRMGE_3800_OVER_Y2

Address: Operational Base(0xFF3F3800) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x098	sw_hdrmge_l_raw1_2 sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x098	sw_hdrmge_l_raw0_2 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x004	sw_hdrmge_e_y2 E-curve over_exp_normal of Y-2

ISP_HDRMGE_3800_OVER_Y3

Address: Operational Base(0xFF3F3800) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0fb	sw_hdrmge_l_raw1_3 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x0fb	sw_hdrmge_l_raw0_3 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x00e	sw_hdrmge_e_y3 E-curve over_exp_normal of Y-3

ISP_HDRMGE_3800_OVER_Y4

Address: Operational Base(0xFF3F3800) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x183	sw_hdrmge_l_raw1_4 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x183	sw_hdrmge_l_raw0_4 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x031	sw_hdrmge_e_y4 E-curve over_exp_normal of Y-4

ISP_HDRMGE_3800_OVER_Y5

Address: Operational Base(0xFF3F3800) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x220	sw_hdrmge_l_raw1_5 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x220	sw_hdrmge_l_raw0_5 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x098	sw_hdrmge_e_y5 E-curve over_exp_normal of Y-5

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ISP_HDRMGE_3800_OVER_Y6

Address: Operational Base(0xFF3F3800) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x2b7	sw_hdrmge_l_raw1_6 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x2b7	sw_hdrmge_l_raw0_6 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x183	sw_hdrmge_e_y6 E-curve over_exp_normal of Y-6

ISP_HDRMGE_3800_OVER_Y7

Address: Operational Base(0xFF3F3800) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x331	sw_hdrmge_l_raw1_7 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x331	sw_hdrmge_l_raw0_7 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x2b7	sw_hdrmge_e_y7 E-curve over_exp_normal of Y-7

ISP_HDRMGE_3800_OVER_Y8

Address: Operational Base(0xFF3F3800) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x386	sw_hdrmge_l_raw1_8 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x386	sw_hdrmge_l_raw0_8 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x386	sw_hdrmge_e_y8 E-curve over_exp_normal of Y-8

ISP_HDRMGE_3800_OVER_Y9

Address: Operational Base(0xFF3F3800) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3bb	sw_hdrmge_l_raw1_9 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3bb	sw_hdrmge_l_raw0_9 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3da	sw_hdrmge_e_y9 E-curve over_exp_normal of Y-9

ISP_HDRMGE_3800_OVER_Y10

Address: Operational Base(0xFF3F3800) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3da	sw_hdrmge_l_raw1_10 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3da	sw_hdrmge_l_raw0_10 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3f5	sw_hdrmge_e_y10 E-curve over_exp_normal of Y-10

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ISP_HDRMGE_3800_OVER_Y11

Address: Operational Base(0xFF3F3800) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3eb	sw_hdrmge_l_raw11_1 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3eb	sw_hdrmge_l_raw11_0 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3fd	sw_hdrmge_e_y11 E-curve over_exp_normal of Y-11

ISP_HDRMGE_3800_OVER_Y12

Address: Operational Base(0xFF3F3800) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3f5	sw_hdrmge_l_raw12_1 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3f5	sw_hdrmge_l_raw12_0 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	sw_hdrmge_e_y12 E-curve over_exp_normal of Y-12

ISP_HDRMGE_3800_OVER_Y13

Address: Operational Base(0xFF3F3800) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3fa	sw_hdrmge_l_raw13_1 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3fa	sw_hdrmge_l_raw13_0 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	sw_hdrmge_e_y13 E-curve over_exp_normal of Y-13

ISP_HDRMGE_3800_OVER_Y14

Address: Operational Base(0xFF3F3800) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3fd	sw_hdrmge_l_raw1_14 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3fd	sw_hdrmge_l_raw0_14 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	sw_hdrmge_e_y14 E-curve over_exp_normal of Y-14

ISP_HDRMGE_3800_OVER_Y15

Address: Operational Base(0xFF3F3800) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3fe	sw_hdrmge_l_raw1_15 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3fe	sw_hdrmge_l_raw0_15 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	sw_hdrmge_e_y15 E-curve over_exp_normal of Y-15

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ISP_HDRMGE_3800_OVER_Y16

Address: Operational Base(0xFF3F3800) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3ff	sw_hdrmge_l_raw1_16 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3ff	sw_hdrmge_l_raw0_16 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	sw_hdrmge_e_y16 E-curve over_exp_normal of Y-16

ISP_HDRMGE_3800_EACH_GAIN

Address: Operational Base(0xFF3F3800) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x100	sw_hdrmge_each_raw_gain1 Raw_gain1[5,6] for raw_each_diff1 = M*raw_gain1 - L, only for HDRx3
15:14	RO	0x0	reserved
13:0	RW	0x0400	sw_hdrmge_each_raw_gain0 Raw_gain0[8,6] for raw_each_diff0 = S*raw_gain0 - M, for HDRx2 and HDRx3

2.4.2.9 BAY3D

BAY3D_2C00_BAY3D_CTRL

Address: Operational Base(0xFF3F2C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sys_itself_force_upd_bay3d_working Sys_itself_force_upd, write only Bay3d_working, read only
30	RO	0x0	sw_bay3d_soft_mode_shd Software calculate low weight shadow 1'b1: Backdoor enable for software calculate low weight 1'b0: Hardware calculate low weight It has been deleted in isp-lite version.
29	RO	0x0	sw_bay3d_bwsaving_en_shd Bandwidth saving optimise shadow 1'b1: Optimise 1'b0: No optimise
28	RW	0x0	sw_bay3d_ack_frm_pro_en_shd Small v_blank protect enable 1'b1: Enable 1'b0: Disable Read shadow
27	RO	0x0	sw_bay3d_glbpk_en_shd Global pk enable shadow 1'b1: Global pk from sw_bay3d_glbpk2 1'b0: Local pk from DDR
26	RO	0x0	sw_bay3d_logaus3_bypass_en_shd Low weight calculate 3x3 Gaussian filter bypass shadow 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
25	RO	0x0	sw_bay3d_logaus5_bypass_en_shd Low weight calculate Bayer Gaussian filter bypass shadow 1'b1: Enable 1'b0: Disable
24	RO	0x0	sw_bay3d_lomed_bypass_en_shd Low weight calculate median filter bypass shadow 1'b1: Enable 1'b0: Disable
23	RO	0x0	sw_bay3d_hichnsplit_en_shd High weight calculate Gaussian filter GRBG 4 channel split enable shadow 1'b1: 4 channels 3x3 Gaussian 1'b0: 1 channel 5x7 Gaussian It has been deleted in isp-lite version.
22	RO	0x0	sw_bay3d_hiabs_possel_shd High weight calculate abs position select shadow 1'b0: Difference->median->Gaussian->abs 1'b1: Difference->median->abs->Gaussian
21	RO	0x0	sw_bay3d_higaus_bypass_en_shd High weight calculate Gaussian filter bypass shadow 1'b1: Enable 1'b0: Disable
20	RO	0x0	sw_bay3d_himed_bypass_en_shd High weight calculate median filter bypass shadow 1'b1: Enable 1'b0: Disable It has been deleted in isp-lite version.
19	RO	0x0	sw_bay3d_lobypass_en_shd BAY3D low weight data path bypass shadow 1'b1: Enable 1'b0: Disable
18	RO	0x0	sw_bay3d_hibypass_en_shd BAY3D high weight data path bypass shadow 1'b1: Enable 1'b0: Disable
17	RO	0x0	sw_bay3d_bypass_en_shd BAY3D data path bypass shadow 1'b1: Enable 1'b0: Disable
16	RO	0x0	sw_bay3d_en_shd BAY3D enable shadow 1'b1: Enable 1'b0: Disable
15	W1C	0x0	sw_bay3d_soft_st In soft mode, software start BAY3D MI, auto clear. It has been deleted in isp-lite version.
14	RW	0x0	sw_bay3d_soft_mode Software calculate low weight 1'b1: Backdoor enable for software calculate low weight 1'b0: Hardware calculate low weight It has been deleted in isp-lite version.
13	RW	0x0	sw_bay3d_bwsaving_en Bandwidth saving optimise 1'b1: Optimise 1'b0: No optimise

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Bit	Attr	Reset Value	Description
12	RW	0x0	sw_bay3d_loswitch_protect First frame protect for low bypass When switch low bypass to NOT low bypass (low bypass switch from 1 to 0), sw_bay3d_loswitch_protect set to 1.
11	RW	0x0	sw_bay3d_glbpk_en Global pk enable 1'b1: Global pk from sw_bay3d_glbpk2 1'b0: Local pk from DDR
10	RW	0x0	sw_bay3d_logaus3_bypass_en Low weight calculate 3x3 Gaussian filter bypass 1'b1: Enable 1'b0: Disable
9	RW	0x0	sw_bay3d_logaus5_bypass_en Low weight calculate Bayer Gaussian filter bypass 1'b1: Enable 1'b0: Disable
8	RW	0x0	sw_bay3d_lomed_bypass_en Low weight calculate median filter bypass 1'b1: Enable 1'b0: Disable
7	RW	0x0	sw_bay3d_hichnsplit_en High weight calculate Gaussian filter Bayer 4 channel split enable 1'b1: 4 channels 3x3 Gaussian 1'b0: 1 channel 5x7 Gaussian It has been deleted in isp-lite version.
6	RW	0x1	sw_bay3d_hiabs_possel High weight calculate abs position select 1'b0: Difference->median->Gaussian->abs 1'b1: Difference->median->abs->Gaussian
5	RW	0x0	sw_bay3d_higaus_bypass_en High weight calculate Gaussian filter bypass 1'b1: Enable 1'b0: Disable
4	RW	0x0	sw_bay3d_himed_bypass_en High weight calculate median filter bypass 1'b1: Enable 1'b0: Disable It has been deleted in isp-lite version.
3	RW	0x0	sw_bay3d_lobypass_en BAY3D low weight data path bypass 1'b1: Enable 1'b0: Disable Low bypass has a higher priority than high bypass. When set low bypass=1 & high bypass=1, actually means low bypass=1 & high bypass=0.
2	RW	0x0	sw_bay3d_hibypass_en BAY3D high weight data path bypass 1'b1: Enable 1'b0: Disable Low bypass has a higher priority than high bypass. When set low bypass=1 & high bypass=1, actually means low bypass=1 & high bypass=0.
1	RW	0x0	sw_bay3d_bypass_en BAY3D data path bypass 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_bay3d_en_i BAY3D enable 1'b1: Enable 1'b0: Disable

BAY3D_2C00_BAY3D_KALRATIO

Address: Operational Base(0xFF3F2C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0xffff	sw_bay3d_hidif_th High difference statistic threshold dif_sel = dif <= sw_bay3d_hidif_th ? dif : sw_bay3d_hidif_th [integer, fraction] = [4, 12]
15:10	RO	0x00	reserved
9:0	RW	0x100	sw_bay3d_softwgt Soft threshold weight, [integer, fraction] = [0, 10]

BAY3D_2C00_BAY3D_GLBPK2

Address: Operational Base(0xFF3F2C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000800	sw_bay3d_glbpk2 Global pk square

BAY3D_2C00_BAY3D_CTRL1

Address: Operational Base(0xFF3F2C00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_bay3d_higaus5x5_en_shd BAY3D high weight 5x5 Gaussian filter enable shadow 1'b0: Disable 1'b1: Enable It has been deleted in isp-lite version.
26:25	RW	0x0	sw_bay3d_higaus3_mode_shd BAY3D high weight 3x3 Gaussian filter select shadow 2'b00: Disable 2'b01: Enable kernel 1 2'b10: Enable kernel 2 2'b11: Enable kernel 2 It has been deleted in isp-lite version.
24	RW	0x0	sw_bay3d_curds_high_en_shd BAY3D current downscale high precision enable shadow 1'b1: Enable 1'b0: Disable
23	RO	0x0	reserved
22	RW	0x0	sw_bay3d_pksig_ind_sel_shd BAY3D pk sigma index select shadow 1'b1: Filtered data 1'b0: Original data It has been deleted in isp-lite version.
21	RW	0x0	sw_bay3d_hisig_ind_sel_shd BAY3D high sigma index select shadow 1'b1: Filtered data 1'b0: Original data It has been deleted in isp-lite version.

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Bit	Attr	Reset Value	Description
20	RW	0x0	sw_bay3d_lo4x4_en_shd BAY3D low weight 4x4 filter enable shadow 1'b1: Enable 1'b0: Disable
19	RW	0x0	sw_bay3d_lo4x8_en_shd BAY3D low weight 4x8 filter enable shadow 1'b1: Enable 1'b0: Disable
18	RW	0x0	sw_bay3d_bwopt_gain_dis_shd Bandwidth saving optimise2 shadow 1'b1: No optimise 1'b0: Optimise
17	RW	0x0	sw_bay3d_hichncor_en_shd BAY3D high weight 5x5 filter with correction enable shadow 1'b1: Enable 1'b0: Disable It has been deleted in isp-lite version.
16	RO	0x0	sw_bay3d_hiwgt_opt_en_shd BAY3D high weight optimise enable shadow 1'b1: Enable 1'b0: Disable
15	RO	0x0	reserved
14	RW	0x0	sw_bay3d_wgtmm_sel_en BAY3D weight min or max mixture optimise select 1'b0: Min 1'b1: Max It has been added in isp-lite version.
13	RW	0x0	sw_bay3d_wgtmm_opt_en BAY3D weight min or max mixture optimise enable 1'b0: Disable 1'b1: Enable It has been added in isp-lite version.
12	RW	0x0	sw_bay3d_wgtmix_opt_en BAY3D weight mixture optimise enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	sw_bay3d_higaus5x5_en BAY3D high weight 5x5 Gaussian filter enable 1'b0: Disable 1'b1: Enable It has been deleted in isp-lite version.
10:9	RW	0x0	sw_bay3d_higaus3_mode BAY3D high weight 3x3 Gaussian filter select 2'b00: Disable 2'b01: Enable kernel 1 2'b10: Enable kernel 2 2'b11: Enable kernel 2 It has been deleted in isp-lite version.
8	RW	0x0	sw_bay3d_curds_high_en BAY3D current downscale high precision enable 1'b1: Enable 1'b0: Disable
7	RW	0x0	sw_bay3d_iirwr_rnd_en BAY3D IIR data rounding enable 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
6	RW	0x0	sw_bay3d_pksig_ind_sel BAY3D pk sigma index select 1'b1: Filtered data 1'b0: Original data It has been deleted in isp-lite version.
5	RW	0x0	sw_bay3d_hisig_ind_sel BAY3D high sigma index select 1'b1: Filtered data 1'b0: Original data It has been deleted in isp-lite version.
4	RW	0x0	sw_bay3d_lo4x4_en Bay3d low weight 4x4 filter enable 1'b1: Enable 1'b0: Disable
3	RW	0x0	sw_bay3d_lo4x8_en BAY3D low weight 4x8 filter enable 1'b1: Enable 1'b0: Disable
2	RW	0x0	sw_bay3d_bwopt_gain_dis Bandwidth saving optimise2 for gain data 1'b1: No optimise 1'b0: Optimise
1	RW	0x0	sw_bay3d_hichncor_en BAY3D high weight 5x5 filter with correction enable 1'b1: Enable 1'b0: Disable It has been deleted in isp-lite version;.
0	RW	0x1	sw_bay3d_hiwgt_opt_en BAY3D high weight optimise enable 1'b1: Enable 1'b0: Disable

BAY3D_2C00_BAY3D_WGTLMT

Address: Operational Base(0xFF3F2C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_bay3d_wgtratio Weight high and low mix ratio, [integer, fraction] = [0, 10]
15:10	RO	0x00	reserved
9:0	RW	0x380	sw_bay3d_wgtlmt High weight limit, [integer, fraction] = [0, 10]

BAY3D_2C00_BAY3D_SIG0_X0

Address: Operational Base(0xFF3F2C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x102d	sw_bay3d_sig0_x1 Sigma curve coordinate x1
15:0	RW	0x002d	sw_bay3d_sig0_x0 Sigma curve coordinate x0

BAY3D_2C00_BAY3D_SIG0_X1

Address: Operational Base(0xFF3F2C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x1033	sw_bay3d_sig0_x3 Sigma curve coordinate x3

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Bit	Attr	Reset Value	Description
15:0	RW	0x1031	sw_bay3d_sig0_x2 Sigma curve coordinate x2

BAY3D_2C00_BAY3D_SIG0_X2

Address: Operational Base(0xFF3F2C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x1057	sw_bay3d_sig0_x5 Sigma curve coordinate x5
15:0	RW	0x1053	sw_bay3d_sig0_x4 Sigma curve coordinate x4

BAY3D_2C00_BAY3D_SIG0_X3

Address: Operational Base(0xFF3F2C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x30d7	sw_bay3d_sig0_x7 Sigma curve coordinate x7
15:0	RW	0x3057	sw_bay3d_sig0_x6 Sigma curve coordinate x6

BAY3D_2C00_BAY3D_SIG0_X4

Address: Operational Base(0xFF3F2C00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x7157	sw_bay3d_sig0_x9 Sigma curve coordinate x9
15:0	RW	0x70d7	sw_bay3d_sig0_x8 Sigma curve coordinate x8

BAY3D_2C00_BAY3D_SIG0_X5

Address: Operational Base(0xFF3F2C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x715d	sw_bay3d_sig0_x11 Sigma curve coordinate x11
15:0	RW	0x715b	sw_bay3d_sig0_x10 Sigma curve coordinate x10

BAY3D_2C00_BAY3D_SIG0_X6

Address: Operational Base(0xFF3F2C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x72dd	sw_bay3d_sig0_x13 Sigma curve coordinate x13
15:0	RW	0x725d	sw_bay3d_sig0_x12 Sigma curve coordinate x12

BAY3D_2C00_BAY3D_SIG0_X7

Address: Operational Base(0xFF3F2C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x771d	sw_bay3d_sig0_x15 Sigma curve coordinate x15
15:0	RW	0x76dd	sw_bay3d_sig0_x14 Sigma curve coordinate x14

BAY3D_2C00_BAY3D_SIG0_Y0

Address: Operational Base(0xFF3F2C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0c00	sw_bay3d_sig0_y1 Sigma curve coordinate y1
15:14	RO	0x0	reserved
13:0	RW	0x0c00	sw_bay3d_sig0_y0 Sigma curve coordinate y0

BAY3D_2C00_BAY3D_SIG0_Y1

Address: Operational Base(0xFF3F2C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0c00	sw_bay3d_sig0_y3 Sigma curve coordinate y3
15:14	RO	0x0	reserved
13:0	RW	0x0c00	sw_bay3d_sig0_y2 Sigma curve coordinate y2

BAY3D_2C00_BAY3D_SIG0_Y2

Address: Operational Base(0xFF3F2C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0a00	sw_bay3d_sig0_y5 Sigma curve coordinate y5
15:14	RO	0x0	reserved
13:0	RW	0x0a00	sw_bay3d_sig0_y4 Sigma curve coordinate y4

BAY3D_2C00_BAY3D_SIG0_Y3

Address: Operational Base(0xFF3F2C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0a00	sw_bay3d_sig0_y7 Sigma curve coordinate y7
15:14	RO	0x0	reserved
13:0	RW	0x0a00	sw_bay3d_sig0_y6 Sigma curve coordinate y6

BAY3D_2C00_BAY3D_SIG0_Y4

Address: Operational Base(0xFF3F2C00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0800	sw_bay3d_sig0_y9 Sigma curve coordinate y9
15:14	RO	0x0	reserved
13:0	RW	0x0800	sw_bay3d_sig0_y8 Sigma curve coordinate y8

BAY3D_2C00_BAY3D_SIG0_Y5

Address: Operational Base(0xFF3F2C00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0800	sw_bay3d_sig0_y11 Sigma curve coordinate y11
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0800	sw_bay3d_sig0_y10 Sigma curve coordinate y10

BAY3D_2C00_BAY3D_SIG0_Y6

Address: Operational Base(0xFF3F2C00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0600	sw_bay3d_sig0_y13 Sigma curve coordinate y13
15:14	RO	0x0	reserved
13:0	RW	0x0600	sw_bay3d_sig0_y12 Sigma curve coordinate y12

BAY3D_2C00_BAY3D_SIG0_Y7

Address: Operational Base(0xFF3F2C00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0400	sw_bay3d_sig0_y15 Sigma curve coordinate y15
15:14	RO	0x0	reserved
13:0	RW	0x0600	sw_bay3d_sig0_y14 Sigma curve coordinate y14

BAY3D_2C00_BAY3D_SIG1_X0

Address: Operational Base(0xFF3F2C00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x102d	sw_bay3d_sig1_x1 Sigma curve coordinate x1
15:0	RW	0x002d	sw_bay3d_sig1_x0 Sigma curve coordinate x0

BAY3D_2C00_BAY3D_SIG1_X1

Address: Operational Base(0xFF3F2C00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x1033	sw_bay3d_sig1_x3 Sigma curve coordinate x3
15:0	RW	0x1031	sw_bay3d_sig1_x2 Sigma curve coordinate x2

BAY3D_2C00_BAY3D_SIG1_X2

Address: Operational Base(0xFF3F2C00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x1057	sw_bay3d_sig1_x5 Sigma curve coordinate x5
15:0	RW	0x1053	sw_bay3d_sig1_x4 Sigma curve coordinate x4

BAY3D_2C00_BAY3D_SIG1_X3

Address: Operational Base(0xFF3F2C00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x30d7	sw_bay3d_sig1_x7 Sigma curve coordinate x7
15:0	RW	0x3057	sw_bay3d_sig1_x6 Sigma curve coordinate x6

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BAY3D_2C00_BAY3D_SIG1_X4

Address: Operational Base(0xFF3F2C00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x7157	sw_bay3d_sig1_x9 Sigma curve coordinate x9
15:0	RW	0x70d7	sw_bay3d_sig1_x8 Sigma curve coordinate x8

BAY3D_2C00_BAY3D_SIG1_X5

Address: Operational Base(0xFF3F2C00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x715d	sw_bay3d_sig1_x11 Sigma curve coordinate x11
15:0	RW	0x715b	sw_bay3d_sig1_x10 Sigma curve coordinate x10

BAY3D_2C00_BAY3D_SIG1_X6

Address: Operational Base(0xFF3F2C00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x72dd	sw_bay3d_sig1_x13 Sigma curve coordinate x13
15:0	RW	0x725d	sw_bay3d_sig1_x12 Sigma curve coordinate x12

BAY3D_2C00_BAY3D_SIG1_X7

Address: Operational Base(0xFF3F2C00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x771d	sw_bay3d_sig1_x15 Sigma curve coordinate x15
15:0	RW	0x76dd	sw_bay3d_sig1_x14 Sigma curve coordinate x14

BAY3D_2C00_BAY3D_SIG1_Y0

Address: Operational Base(0xFF3F2C00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x096c	sw_bay3d_sig1_y1 Sigma curve coordinate y1
15:14	RO	0x0	reserved
13:0	RW	0x096c	sw_bay3d_sig1_y0 Sigma curve coordinate y0

BAY3D_2C00_BAY3D_SIG1_Y1

Address: Operational Base(0xFF3F2C00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x096c	sw_bay3d_sig1_y3 Sigma curve coordinate y3
15:14	RO	0x0	reserved
13:0	RW	0x096c	sw_bay3d_sig1_y2 Sigma curve coordinate y2

BAY3D_2C00_BAY3D_SIG1_Y2

Address: Operational Base(0xFF3F2C00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x04b6	sw_bay3d_sig1_y5 Sigma curve coordinate y5
15:14	RO	0x0	reserved
13:0	RW	0x04b6	sw_bay3d_sig1_y4 Sigma curve coordinate y4

BAY3D_2C00_BAY3D_SIG1_Y3

Address: Operational Base(0xFF3F2C00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x04b6	sw_bay3d_sig1_y7 Sigma curve coordinate y7
15:14	RO	0x0	reserved
13:0	RW	0x04b6	sw_bay3d_sig1_y6 Sigma curve coordinate y6

BAY3D_2C00_BAY3D_SIG1_Y4

Address: Operational Base(0xFF3F2C00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x04b6	sw_bay3d_sig1_y9 Sigma curve coordinate y9
15:14	RO	0x0	reserved
13:0	RW	0x04b6	sw_bay3d_sig1_y8 Sigma curve coordinate y8

BAY3D_2C00_BAY3D_SIG1_Y5

Address: Operational Base(0xFF3F2C00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x04b6	sw_bay3d_sig1_y11 Sigma curve coordinate y11
15:14	RO	0x0	reserved
13:0	RW	0x04b6	sw_bay3d_sig1_y10 Sigma curve coordinate y10

BAY3D_2C00_BAY3D_SIG1_Y6

Address: Operational Base(0xFF3F2C00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x04b6	sw_bay3d_sig1_y13 Sigma curve coordinate y13
15:14	RO	0x0	reserved
13:0	RW	0x04b6	sw_bay3d_sig1_y12 Sigma curve coordinate y12

BAY3D_2C00_BAY3D_SIG1_Y7

Address: Operational Base(0xFF3F2C00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x04b6	sw_bay3d_sig1_y15 Sigma curve coordinate y15
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x04b6	sw_bay3d_sig1_y14 Sigma curve coordinate y14

BAY3D_2C00_BAY3D_SIG2_Y0

Address: Operational Base(0xFF3F2C00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x07e	sw_bay3d_sig2_y1 Sigma curve coordinate y1
15:10	RO	0x00	reserved
9:0	RW	0x07e	sw_bay3d_sig2_y0 Sigma curve coordinate y0, [integer, fraction] = [0, 10]

BAY3D_2C00_BAY3D_SIG2_Y1

Address: Operational Base(0xFF3F2C00) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x07e	sw_bay3d_sig2_y3 Sigma curve coordinate y3
15:10	RO	0x00	reserved
9:0	RW	0x07e	sw_bay3d_sig2_y2 Sigma curve coordinate y2

BAY3D_2C00_BAY3D_SIG2_Y2

Address: Operational Base(0xFF3F2C00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x03f	sw_bay3d_sig2_y5 Sigma curve coordinate y5
15:10	RO	0x00	reserved
9:0	RW	0x03f	sw_bay3d_sig2_y4 Sigma curve coordinate y4

BAY3D_2C00_BAY3D_SIG2_Y3

Address: Operational Base(0xFF3F2C00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x03f	sw_bay3d_sig2_y7 Sigma curve coordinate y7
15:10	RO	0x00	reserved
9:0	RW	0x03f	sw_bay3d_sig2_y6 Sigma curve coordinate y6

BAY3D_2C00_BAY3D_SIG2_Y4

Address: Operational Base(0xFF3F2C00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x03f	sw_bay3d_sig2_y9 Sigma curve coordinate y9
15:10	RO	0x00	reserved
9:0	RW	0x03f	sw_bay3d_sig2_y8 Sigma curve coordinate y8

BAY3D_2C00_BAY3D_SIG2_Y5

Address: Operational Base(0xFF3F2C00) + offset (0x00A8)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x03f	sw_bay3d_sig2_y11 Sigma curve coordinate y11
15:10	RO	0x00	reserved
9:0	RW	0x03f	sw_bay3d_sig2_y10 Sigma curve coordinate y10

BAY3D_2C00_BAY3D_SIG2_Y6

Address: Operational Base(0xFF3F2C00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x03f	sw_bay3d_sig2_y13 Sigma curve coordinate y13
15:10	RO	0x00	reserved
9:0	RW	0x03f	sw_bay3d_sig2_y12 Sigma curve coordinate y12

BAY3D_2C00_BAY3D_SIG2_Y7

Address: Operational Base(0xFF3F2C00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x03f	sw_bay3d_sig2_y15 Sigma curve coordinate y15
15:10	RO	0x00	reserved
9:0	RW	0x03f	sw_bay3d_sig2_y14 Sigma curve coordinate y14

BAY3D_2C00_BAY3D_LODIF_STAT0

Address: Operational Base(0xFF3F2C00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_sum_lodif Sum of low difference [31:0]

BAY3D_2C00_BAY3D_LODIF_STAT1

Address: Operational Base(0xFF3F2C00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_bay3d_wgtmin Weight minimum, [integer, fraction] = [0, 10]
15:2	RO	0x0000	reserved
1:0	RO	0x0	ro_sum_lodif Sum of low difference [33:32]

BAY3D_2C00_BAY3D_HIDIF_STAT0

Address: Operational Base(0xFF3F2C00) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_sum_hidif0 Sum of high difference [31:0]

BAY3D_2C00_BAY3D_HIDIF_STAT1

Address: Operational Base(0xFF3F2C00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	ro_sum_hidif0 Sum of high difference [39:32]

BAY3D_2C00_BAY3D_MI_ST

Address: Operational Base(0xFF3F2C00) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x00	sw_bay3d_mi_safe_cnt MI WR and RD pixel clamp line counter
15:7	RO	0x000	reserved
6:0	RW	0x1c	sw_bay3d_mi2cur_linecnt When in_pix_row_cnt count to sw_bay3d_mi2cur_linecnt, start MI read Manually.

BAY3D_2C00_BAY3D_RO_CNT

Address: Operational Base(0xFF3F2C00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	ro_pix_col_cnt Column counter
15:13	RO	0x0	reserved
12:0	RO	0x0000	ro_pix_row_cnt Row counter

BAY3D_2C00_BAY3D_RO_FIFO_CUR

Address: Operational Base(0xFF3F2C00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	space2empty_wr_cur Current FIFO write space2empty It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RO	0x0000	space2empty_rd_cur Current FIFO read space2empty It has been deleted in isp-lite version.

BAY3D_2C00_BAY3D_RO_FIFO_IIR

Address: Operational Base(0xFF3F2C00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	space2empty_wr_iir IIR FIFO write space2empty It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RO	0x0000	space2empty_rd_iir IIR FIFO read space2empty It has been deleted in isp-lite version.

BAY3D_2C00_BAY3D_RO_FIFO_DS

Address: Operational Base(0xFF3F2C00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	space2empty_wr_ds Downscale FIFO write space2empty It has been deleted in isp-lite version.

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RO	0x000	space2empty_rd_ds Downscale FIFO read space2empty It has been deleted in isp-lite version.

BAY3D_2C00_BAY3D_RO_FIFO_STATE

Address: Operational Base(0xFF3F2C00) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	ro_lo_fifo_empty Low weight FIFO for merge
24	RO	0x0	fifo_curds_full MI FIFO state current downscale
23:18	RO	0x00	reserved
17	RO	0x0	fifo_ds_empty MI FIFO state IIR downscale
16	RO	0x0	fifo_ds_full MI FIFO state IIR downscale
15:10	RO	0x00	reserved
9	RO	0x0	fifo_iir_empty MI FIFO state IIR
8	RO	0x0	fifo_iir_full MI FIFO state IIR
7:5	RO	0x0	reserved
4	RO	0x0	sys_bay3d_fst_frame_shd BAY3D first frame flag shadow from 0x0404[27] sys_raw3d_fst_frame
3:2	RO	0x0	reserved
1	RO	0x0	fifo_cur_empty MI FIFO state current
0	RO	0x0	fifo_cur_full MI FIFO state current

BAY3D_2C00_BAY3D_IN_IRQ_LINECNT

Address: Operational Base(0xFF3F2C00) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_bay3d_mibuf_size BAY3D current MI buffer size constraint It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x004e	sw_bay3d_linecnt2done When in_row_cnt count to sw_bay3d_linecnt2done, generate done signal for interrupt.

BAY3D_2C00_BAY3D_HISIGRAT

Address: Operational Base(0xFF3F2C00) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_bay3d_hisigrat1 BAY3D high weight optimise parameters sigma ratio1, [integer, fraction] = [4, 8]
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_bay3d_hisigrat0 BAY3D high weight optimise parameters sigma ratio0, [integer, fraction] = [4, 8]

BAY3D_2C00_BAY3D_HISIGOFF

Address: Operational Base(0xFF3F2C00) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x400	sw_bay3d_hisigoff1 BAY3D high weight optimise parameters sigma offset1, [integer, fraction] = [2, 10]
15:12	RO	0x0	reserved
11:0	RW	0x100	sw_bay3d_hisigoff0 BAY3D high weight optimise parameters sigma offset0, [integer, fraction] = [2, 10]

BAY3D_2C00_BAY3D_LOSIG

Address: Operational Base(0xFF3F2C00) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_bay3d_losigrat BAY3D low weight optimise parameters sigma ratio, [integer, fraction] = [2, 10]
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_bay3d_losigoff BAY3D low weight optimise parameters sigma offset0, [integer, fraction] = [2, 10]

BAY3D_2C00_BAY3D_SIGPK

Address: Operational Base(0xFF3F2C00) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_bay3d_bgain_off BAY3D pk sigma B gain offset, [integer, fraction] = [4, 10]
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_bay3d_rgain_off BAY3D pk sigma R gain offset, [integer, fraction] = [4, 10]

BAY3D_2C00_BAY3D_SIGGAUS

Address: Operational Base(0xFF3F2C00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x08	sw_bay3d_siggaus3 BAY3D sigma index filter kernel coef3 It has been deleted in isp-lite version.
23:22	RO	0x0	reserved
21:16	RW	0x10	sw_bay3d_siggaus2 BAY3D sigma index filter kernel coef2
15:14	RO	0x0	reserved
13:8	RW	0x08	sw_bay3d_siggaus1 BAY3D sigma index filter kernel coef1
7:6	RO	0x0	reserved
5:0	RW	0x10	sw_bay3d_siggaus0 BAY3D sigma index filter kernel coef0

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BAY3D_2C00_BAY3D_WRMI

Address: Operational Base(0xFF3F2C00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RO	0x0000000	ro_wr_pix_cnt_a BAY3D current MI write pixel counter

BAY3D_2C00_BAY3D_RDMI

Address: Operational Base(0xFF3F2C00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	ro_bay3d_ack BAY3D ack state, composed of lo_ack, micur_wr_ack, hi_ack, bay3d_ack from high to low.
27:26	RO	0x0	reserved
25:0	RO	0x0000000	ro_rd_pix_cnt_a BAY3D current MI read pixel counter

2.4.2.10 LSC

ISP_LSC_2200_CTRL

Address: Operational Base(0xFF3F2200) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd For force update this module configuration
30	RO	0x0	ro_lsc_lut_loading Lsc lut loading flag
29:26	RO	0x0	reserved
25:24	RW	0x0	sys_itself_lut_mode LSC update mode 2'b00: Open frame_end and force update load lut mode 2'b11: soft control force update load lut mode; Suggest use force-upd load lut mode
23:5	RO	0x00000	reserved
4	RW	0x0	sws_pre_rd_st_mode LSC will read the table at the time of BLS frame start if this bit set to 1.
3	RO	0x0	reserved
2	RW	0x0	sw_lsc_sector_config16x16_en 1'b0: The sector will configure 8x8 and map to right and down(Old mode) 1'b1: All the 16x16 sector will be configured(New mode)
1	WO	0x0	lsc_lut_en Load correction factor from DDR, and will be cleared when begin to load DDR
0	RW	0x0	lsc_en 1'b0: Activation request for lens shading correction 1'b1: Deactivation request for lens shading correction Activation/Deactivation is object of a shadowing mechanism. The current status is visible at ISP_LSC_STATUS: lsc_enable_status

ISP_LSC_2200_R_TABLE_ADDR

Address: Operational Base(0xFF3F2200) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	r_ram_addr Table address in RAM for samples of the R color component. Will be automatically incremented by each read or write access to the table. Valid addresses are in the range 0 to 152. --- ISP_LSC_R_TABLE_ADDR --- Note: The table values are written into an internal RAM. The RAM Address is generated per auto- increment. The tables values will be read back by a continuous read access to the corresponding register. The read address is auto-incremented for each read access to that register and is reset to a specific value by a write access to the ISP_LSC_TABLE_ADDR register. Table access by SW at table address 0...152

ISP_LSC_2200_GR_TABLE_ADDR

Address: Operational Base(0xFF3F2200) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	gr_ram_addr Table address in RAM for samples of the G_R color component. Will be automatically incremented by each read or write access to the table.

ISP_LSC_2200_B_TABLE_ADDR

Address: Operational Base(0xFF3F2200) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	b_ram_addr Table address in RAM for samples of the B color component. Will be automatically incremented by each read or write access to the table.

ISP_LSC_2200_GB_TABLE_ADDR

Address: Operational Base(0xFF3F2200) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	gb_ram_addr Table address in RAM for samples of the G_B color component. Will be automatically incremented by each read or write access to the table. Table access by SW at table address 0...152

ISP_LSC_2200_R_TABLE_DATA

Address: Operational Base(0xFF3F2200) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	r_sample_1 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1..7.999)
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	r_sample_0 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1..7.999) --- ISP_LSC_R_TABLE_DATA --- Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table access by SW at table address 0...152

ISP_LSC_2200_GR_TABLE_DATA

Address: Operational Base(0xFF3F2200) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	gr_sample_1 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1..7.999)
15:13	RO	0x0	reserved
12:0	RW	0x0000	gr_sample_0 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1..7.999) --- ISP_LSC_GR_TABLE_DATA --- Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table access by SW at table address 0...152

ISP_LSC_2200_B_TABLE_DATA

Address: Operational Base(0xFF3F2200) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	b_sample_1 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1..7.999)
15:13	RO	0x0	reserved
12:0	RW	0x0000	b_sample_0 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1..7.999) --- ISP_LSC_B_TABLE_DATA --- Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table access by SW at table address 0...152

ISP_LSC_2200_GB_TABLE_DATA

Address: Operational Base(0xFF3F2200) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	gb_sample_1 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1..7.999)
15:13	RO	0x0	reserved
12:0	RW	0x0000	gb_sample_0 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1..7.999) --- ISP_LSC_GB_TABLE_DATA --- Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table access by SW at table address 0...152

ISP_LSC_2200_XGRAD_01

Address: Operational Base(0xFF3F2200) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_1 Factor for x-gradient calculation of sector 1
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_0 Factor for x-gradient calculation of sector 0

ISP_LSC_2200_XGRAD_23

Address: Operational Base(0xFF3F2200) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_3 Factor for x-gradient calculation of sector 3
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_2 Factor for x-gradient calculation of sector 2

ISP_LSC_2200_XGRAD_45

Address: Operational Base(0xFF3F2200) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_5 Factor for x-gradient calculation of sector 5
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_4 Factor for x-gradient calculation of sector 4

ISP_LSC_2200_XGRAD_67

Address: Operational Base(0xFF3F2200) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_7 Factor for x-gradient calculation of sector 7
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_6 Factor for x-gradient calculation of sector 6

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ISP_LSC_2200_YGRAD_01

Address: Operational Base(0xFF3F2200) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_1 Factor for y-gradient calculation of sector 1
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_0 Factor for y-gradient calculation of sector 0

ISP_LSC_2200_YGRAD_23

Address: Operational Base(0xFF3F2200) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_3 Factor for y-gradient calculation of sector 3
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_2 Factor for y-gradient calculation of sector 2

ISP_LSC_2200_YGRAD_45

Address: Operational Base(0xFF3F2200) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_5 Factor for y-gradient calculation of sector 5
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_4 Factor for y-gradient calculation of sector 4

ISP_LSC_2200_YGRAD_67

Address: Operational Base(0xFF3F2200) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_7 Factor for y-gradient calculation of sector 7
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_6 Factor for y-gradient calculation of sector 6

ISP_LSC_2200_XSIZE_01

Address: Operational Base(0xFF3F2200) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_1 Sector size 1 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_0 Sector size 0 in x-direction --- ISP_LSC_XSIZE_01 --- Note: The sector size in x-direction must be greater than 12 pixels. The sum of the sector sizes in x-direction must be "picture width / 2". The sum of the sector sizes in y-direction must be "picture height / 2". No interrupt is generated if above requirements are not fulfilled and the behaviour of the hardware cannot be predicted

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ISP_LSC_2200_XSIZE_23

Address: Operational Base(0xFF3F2200) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_3 Sector size 3 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_2 Sector size 2 in x-direction --- ISP_LSC_XSIZE_23 --- Note: Minimum sector size is 10 in x direction

ISP_LSC_2200_XSIZE_45

Address: Operational Base(0xFF3F2200) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_5 Sector size 5 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_4 Sector size 4in x-direction --- ISP_LSC_XSIZE_45 --- Note: Minimum sector size is 10 in x direction

ISP_LSC_2200_XSIZE_67

Address: Operational Base(0xFF3F2200) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_7 Sector size 7 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_6 Sector size 6 in x-direction --- ISP_LSC_XSIZE_67 --- Note: Minimum sector size is 10 in x direction

ISP_LSC_2200_YSIZE_01

Address: Operational Base(0xFF3F2200) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_1 Sector size 1 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_0 Sector size 0 in y-direction --- ISP_LSC_YSIZE_01 --- Note: Minimum sector size is 8 in y direction. The sector size in y-direction was defined to be 9 bits for preliminary Marvin versions

ISP_LSC_2200_YSIZE_23

Address: Operational Base(0xFF3F2200) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	y_sect_size_3 Sector size 3 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_2 Sector size 2 in y-direction --- ISP_LSC_YSIZE_23 --- Note: Minimum sector size is 8 in y direction

ISP_LSC_2200_YSIZE_45

Address: Operational Base(0xFF3F2200) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_5 Sector size 5 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_4 Sector size 4 in y-direction --- ISP_LSC_YSIZE_45 --- Note: Minimum sector size is 8 in y direction

ISP_LSC_2200_YSIZE_67

Address: Operational Base(0xFF3F2200) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_7 Sector size 7 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_6 Sector size 6 in y-direction --- ISP_LSC_YSIZE_67 --- Note: Minimum sector size is 8 in y direction

ISP_LSC_2200_TABLE_SEL

Address: Operational Base(0xFF3F2200) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	table_sel 1'b0: Next active tables set is table set 0. 1'b1: Next active tables set is table set 1. Table selection is object of a shadowing mechanism. The current status is visible at ISP_LSC_STATUS::active_table. --- ISP_LSC_TABLE_SEL --- Note: Table set 0 access by SW at table address 0...153. Table set 1 access at table address 154...307.

ISP_LSC_2200_ISP_LSC_STATUS

Address: Operational Base(0xFF3F2200) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	active_table 1'b0: Currently active tables set is table set 0 1'b1: Currently active tables set is table set 1
0	RO	0x0	lsc_en_status 1'b0: Lens shading correction is currently off 1'b1: Lens shading correction is currently on

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ISP_LSC_2200_XGRAD_89

Address: Operational Base(0xFF3F2200) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_9 Factor for x-gradient calculation of sector 9
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_8 Factor for x-gradient calculation of sector 8

ISP_LSC_2200_XGRAD_AB

Address: Operational Base(0xFF3F2200) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_b Factor for x-gradient calculation of sector b
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_a Factor for x-gradient calculation of sector a

ISP_LSC_2200_XGRAD_CD

Address: Operational Base(0xFF3F2200) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_d Factor for x-gradient calculation of sector d
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_c Factor for x-gradient calculation of sector c

ISP_LSC_2200_XGRAD_EF

Address: Operational Base(0xFF3F2200) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_f Factor for x-gradient calculation of sector f
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_e Factor for x-gradient calculation of sector e

ISP_LSC_2200_YGRAD_89

Address: Operational Base(0xFF3F2200) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_9 Factor for y-gradient calculation of sector 9
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_8 Factor for y-gradient calculation of sector 8

ISP_LSC_2200_YGRAD_AB

Address: Operational Base(0xFF3F2200) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	ygrad_b Factor for y-gradient calculation of sector b
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_a Factor for y-gradient calculation of sector a

ISP_LSC_2200_YGRAD_CD

Address: Operational Base(0xFF3F2200) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_d Factor for y-gradient calculation of sector d
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_c Factor for y-gradient calculation of sector c

ISP_LSC_2200_YGRAD_EF

Address: Operational Base(0xFF3F2200) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_f Factor for y-gradient calculation of sector f
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_e Factor for y-gradient calculation of sector e

ISP_LSC_2200_XSIZE_89

Address: Operational Base(0xFF3F2200) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_9 Sector size 9 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_8 Sector size 8 in x-direction --- ISP_LSC_XSIZE_89 --- Note: The sector size in x-direction must be greater than 12 pixels

ISP_LSC_2200_XSIZE_AB

Address: Operational Base(0xFF3F2200) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_b Sector size b in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_a Sector size a in x-direction --- ISP_LSC_XSIZE_AB --- Note: Minimum sector size is 10 in x direction

ISP_LSC_2200_XSIZE_CD

Address: Operational Base(0xFF3F2200) + offset (0x0098)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_d Sector size d in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_c Sector size c in x-direction --- ISP_LSC_XSIZE_CD --- Note: Minimum sector size is 10 in x direction

ISP_LSC_2200_XSIZE_EF

Address: Operational Base(0xFF3F2200) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_f Sector size f in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_e Sector size e in x-direction --- ISP_LSC_XSIZE_EF --- Note: Minimum sector size is 10 in x direction

ISP_LSC_2200_YSIZE_89

Address: Operational Base(0xFF3F2200) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_9 Sector size 9 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_8 Sector size 8 in y-direction --- ISP_LSC_YSIZE_89 --- Note: Minimum sector size is 8 in y direction

ISP_LSC_2200_YSIZE_AB

Address: Operational Base(0xFF3F2200) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_b Sector size b in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_a Sector size a in y-direction --- ISP_LSC_YSIZE_AB --- Note: Minimum sector size is 8 in y direction

ISP_LSC_2200_YSIZE_CD

Address: Operational Base(0xFF3F2200) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_d Sector size d in y-direction
15:10	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9:0	RW	0x000	y_sect_size_c Sector size c in y-direction --- ISP_LSC_YSIZE_CD --- Note: Minimum sector size is 8 in y direction

ISP_LSC_2200_YSIZE_EF

Address: Operational Base(0xFF3F2200) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_f Sector size f in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_e Sector size e in y-direction --- ISP_LSC_YSIZE_EF --- Note: Minimum sector size is 8 in y direction

2.4.2.11 HDR_DRC

ISP_DRC_3900_CTRL0

Address: Operational Base(0xFF3F3900) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd When write 1, it will force_upd drc module; auto-clear.
30	RO	0x0	ro_drc_working Drc working, high valid.
29:28	RW	0x0	sw_drc_bil_ack_mode Backdoor to bilateral interpolation acknowledge low 1-4 cycle.
27:7	RO	0x000000	reserved
6	RO	0x0	sw_pre_mem_ddr_wr_en_shd Last frame previous memory data write to DDR enable shadow.
5	RO	0x0	reserved
4	RW	0x0	sw_pre_mem_ddr_wr_en Last frame previous memory data write to DDR enable, shadow reg.
3:2	RO	0x0	reserved
1	RW	0x0	sw_drc_bypass_en Drc bypass enable.
0	RW	0x0	sw_drc_en Drc function enable, shadow reg.

ISP_DRC_3900_CTRL1

Address: Operational Base(0xFF3F3900) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RW	0x8	sw_drc_offset_pow2 Log offset: indata+(1<<offset_pow2), then log2data-offset_pow2.
27	RO	0x0	reserved
26:14	RW	0x0e41	sw_drc_compres_scl Integer, fraction=[2,11], scale plgmax range(0~24576) for trans compress, shadow reg.
13:0	RW	0x0100	sw_drc_position Integer, fraction=[6,8], pluma scale for table index of gain2raw.

ISP_DRC_3900_LPRATIO

Rockchip Confidencial

Address: Operational Base(0xFF3F3900) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	sw_drc_delta_scalein Integer, fraction=[0,8], for plgt*delta_scalein into scale table.
23:12	RW	0x000	sw_drc_hpdetail_ratio Integer, fraction=[1,11], for delt=delt + gain_scl*hpdetail_ratio used.
11:0	RW	0x000	sw_drc_lpdetail_ratio Integer, fraction=[1,11], for delt=(lgt-nglt) + (lgt-maxl)*lpdetail_ratio used.

ISP_DRC_3900_EXPLRATIO

Address: Operational Base(0xFF3F3900) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x60	sw_drc_weicur_pix Integer, fraction=[4,4]<<7, bilateral weight of current pix.
23:16	RW	0x00	sw_drc_weipre_frame Integer, fraction=[0,8], bilateral weight of previous frame. Fix this register value equal to zero, cannot be configured. It has been deleted in isp-lite version.
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_drc_bilat_wt_off The low 8bit of value={1,11}, bilateral weight offset for array_wt(bilateral weight){1,15}.

ISP_DRC_3900_SIGMA

Address: Operational Base(0xFF3F3900) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_drc_force_sgm_inv0 Integer, fraction=[5,11], force bilat-5x5 sigma(edge+motion) value = force_sgm_inv0 if force_sgm_inv0!=0.
15:8	RW	0x00	sw_drc_motion_scl Integer, fraction=[4,4], scale motion data for bilateral difference, use when edge/motion writing into ram.
7:0	RW	0x00	sw_drc_edge_scl Integer, fraction=[4,4], scale edge data for bilateral difference, use when edge/motion writing into ram.

ISP_DRC_3900_SPACESGM

Address: Operational Base(0xFF3F3900) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfe4	sw_drc_space_sgm_inv1 Integer, fraction=[4,8], bil3x3 space sigma invert weight: high-4b exponent, low-8b mantissa.
15:12	RO	0x0	reserved
11:0	RW	0xf80	sw_drc_space_sgm_inv0 Integer, fraction=[4,8], bil5x5 space sigma invert weight: high-4b exponent, low-8b mantissa, (x^2+y^2)*sigma_inv.

ISP_DRC_3900_RANESGM

Address: Operational Base(0xFF3F3900) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0400	sw_drc_range_sgm_inv1 Integer, fraction=[2,11], bil3x3 range sigma invert weight; (diff*range_sigma_inv)^2.
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_range_sgm_inv0 Integer, fraction=[2,11], bil5x5 range sigma invert weight; (diff*range_sigma_inv)^2.

ISP_DRC_3900_BILAT

Address: Operational Base(0xFF3F3900) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_drc_enable_soft_thd High valid, enable soft_thd constrain bilateral luminance for clip(org_luma-soft_thd,org_luma+soft_thd), shadow reg.
30	RO	0x0	reserved
29:16	RW	0x0000	sw_drc_bilat_soft_thd {3,11}, Soft_thd constrain bilateral luminance for clip(org_luma-soft_thd,org_luma+soft_thd), shadow reg.
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_drc_weig_maxl [1,4], Weight for (max3x3*W + (16-W)*gas3x3) when bilateral filter in.
7:5	RO	0x0	reserved
4:0	RW	0x10	sw_drc_weig_bilat Integer, fraction=[1,4], weight for (bilat*W + (16-W)*luma) when bilateral filter out.

ISP_DRC_3900_GAIN_Y0

Address: Operational Base(0xFF3F3900) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y1 [3,10], Curve_gain2raw y1, shadow reg.
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y0 [3,10], Curve_gain2raw y0, shadow reg.

ISP_DRC_3900_GAIN_Y1

Address: Operational Base(0xFF3F3900) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y3 [3,10], Curve_gain2raw y3, shadow reg.
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y2 [3,10], Curve_gain2raw y2, shadow reg.

ISP_DRC_3900_GAIN_Y2

Address: Operational Base(0xFF3F3900) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y5 [3,10], Curve_gain2raw y5, shadow reg.
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0400	sw_drc_gain_y4 [3,10], Curve_gain2raw y4, shadow reg.

ISP_DRC_3900_GAIN_Y3

Address: Operational Base(0xFF3F3900) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y7 [3,10], Curve_gain2raw y7, shadow reg.
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y6 [3,10], Curve_gain2raw y6, shadow reg.

ISP_DRC_3900_GAIN_Y4

Address: Operational Base(0xFF3F3900) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y9 [3,10], Curve_gain2raw y9, shadow reg.
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y8 [3,10], Curve_gain2raw y8, shadow reg.

ISP_DRC_3900_GAIN_Y5

Address: Operational Base(0xFF3F3900) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y11 [3,10], Curve_gain2raw y11, shadow reg.
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y10 [3,10], Curve_gain2raw y10, shadow reg.

ISP_DRC_3900_GAIN_Y6

Address: Operational Base(0xFF3F3900) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y13 [3,10], Curve_gain2raw y13, shadow reg.
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y12 [3,10], Curve_gain2raw y12, shadow reg.

ISP_DRC_3900_GAIN_Y7

Address: Operational Base(0xFF3F3900) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y15 [3,10], Curve_gain2raw y15, shadow reg.
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y14 [3,10], Curve_gain2raw y14, shadow reg.

ISP_DRC_3900_GAIN_Y8

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Address: Operational Base(0xFF3F3900) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0400	sw_drc_gain_y16 [3,10], Curve_gain2raw y16, shadow reg.

ISP_DRC_3900_COMPRES_Y0

Address: Operational Base(0xFF3F3900) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x022e	sw_drc_compres_y1 [3,11], Curve_compress y1, shadow reg.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_drc_compres_y0 [3,11], Curve_compress y0, shadow reg.

ISP_DRC_3900_COMPRES_Y1

Address: Operational Base(0xFF3F3900) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0634	sw_drc_compres_y3 [3,11], Curve_compress y3, shadow reg.
15:14	RO	0x0	reserved
13:0	RW	0x043f	sw_drc_compres_y2 [3,11], Curve_compress y2, shadow reg.

ISP_DRC_3900_COMPRES_Y2

Address: Operational Base(0xFF3F3900) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x09d3	sw_drc_compres_y5 [3,11], Curve_compress y5, shadow reg.
15:14	RO	0x0	reserved
13:0	RW	0x080f	sw_drc_compres_y4 [3,11], Curve_compress y4, shadow reg.

ISP_DRC_3900_COMPRES_Y3

Address: Operational Base(0xFF3F3900) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0d19	sw_drc_compres_y7 [3,11], Curve_compress y7, shadow reg.
15:14	RO	0x0	reserved
13:0	RW	0x0b80	sw_drc_compres_y6 [3,11], Curve_compress y6, shadow reg.

ISP_DRC_3900_COMPRES_Y4

Address: Operational Base(0xFF3F3900) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1179	sw_drc_compres_y9 [3,11], Curve_compress y9, shadow reg.
15:14	RO	0x0	reserved
13:0	RW	0x0ea0	sw_drc_compres_y8 [3,11], Curve_compress y8, shadow reg.

Rockchip Confidencial

ISP_DRC_3900_COMPRES_Y5

Address: Operational Base(0xFF3F3900) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1677	sw_drc_compres_y11 [3,11], Curve_compress y11, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x1413	sw_drc_compres_y10 [3,11], Curve_compress y10, shadow reg;

ISP_DRC_3900_COMPRES_Y6

Address: Operational Base(0xFF3F3900) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1ab6	sw_drc_compres_y13 [3,11], Curve_compress y13, shadow reg.
15:14	RO	0x0	reserved
13:0	RW	0x18ac	sw_drc_compres_y12 [3,11], Curve_compress y12, shadow reg.

ISP_DRC_3900_COMPRES_Y7

Address: Operational Base(0xFF3F3900) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1e5c	sw_drc_compres_y15 [3,11], Curve_compress y15, shadow reg.
15:14	RO	0x0	reserved
13:0	RW	0x1c9a	sw_drc_compres_y14 [3,11], Curve_compress y14, shadow reg.

ISP_DRC_3900_COMPRES_Y8

Address: Operational Base(0xFF3F3900) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x2000	sw_drc_compres_y16 [3,11], Curve_compress y16, shadow reg.

ISP_DRC_3900_SCALE_Y0

Address: Operational Base(0xFF3F3900) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x002	sw_drc_scale_y1 [1,11], Curve_scale y1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_drc_scale_y0 [1,11], Curve_scale y0.

ISP_DRC_3900_SCALE_Y1

Address: Operational Base(0xFF3F3900) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x04c	sw_drc_scale_y3 [1,11], Curve_scale y3.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x014	sw_drc_scale_y2 [1,11], Curve_scale y2.

ISP_DRC_3900_SCALE_Y2

Address: Operational Base(0xFF3F3900) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x17d	sw_drc_scale_y5 [1,11], Curve_scale y5.
15:12	RO	0x0	reserved
11:0	RW	0x0c1	sw_drc_scale_y4 [1,11], Curve_scale y4.

ISP_DRC_3900_SCALE_Y3

Address: Operational Base(0xFF3F3900) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x304	sw_drc_scale_y7 [1,11], Curve_scale y7.
15:12	RO	0x0	reserved
11:0	RW	0x277	sw_drc_scale_y6 [1,11], Curve_scale y6.

ISP_DRC_3900_SCALE_Y4

Address: Operational Base(0xFF3F3900) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x42a	sw_drc_scale_y9 [1,11], Curve_scale y9.
15:12	RO	0x0	reserved
11:0	RW	0x397	sw_drc_scale_y8 [1,11], Curve_scale y8.

ISP_DRC_3900_SCALE_Y5

Address: Operational Base(0xFF3F3900) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x5c7	sw_drc_scale_y11 [1,11], Curve_scale y11.
15:12	RO	0x0	reserved
11:0	RW	0x4bb	sw_drc_scale_y10 [1,11], Curve_scale y10.

ISP_DRC_3900_SCALE_Y6

Address: Operational Base(0xFF3F3900) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x747	sw_drc_scale_y13 [1,11], Curve_scale y13.
15:12	RO	0x0	reserved
11:0	RW	0x6a4	sw_drc_scale_y12 [1,11], Curve_scale y12.

ISP_DRC_3900_SCALE_Y7

Rockchip Confidencial

Address: Operational Base(0xFF3F3900) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x7e8	sw_drc_scale_y15 [1,11], Curve_scale y15.
15:12	RO	0x0	reserved
11:0	RW	0x7b0	sw_drc_scale_y14 [1,11], Curve_scale y14.

ISP_DRC_3900_SCALE_Y8

Address: Operational Base(0xFF3F3900) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_ddr_wr_cycle When not equal to zero, not use software wr_cycle.
15:12	RO	0x0	reserved
11:0	RW	0x800	sw_drc_scale_y16 [1,11], Curve_scale y16.

ISP_DRC_3900_IIRWG_GAIN

Address: Operational Base(0xFF3F3900) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x00	sw_drc_iir_weight [1,6], Range 0~0x40; weight of iir_thumb mix with pre_thumb, shadow reg. Fix this register value equal to zero, cannot be configured. It has been deleted in isp-lite version.
15:0	RW	0x0000	sw_drc_min_ogain [1,15], Drc out gain clip value, shadow reg.

ISP_DRC_3900_LUM3X2_CTRL

Address: Operational Base(0xFF3F3900) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_adrc_gas_t Adrc luma3x2 threshold: {2,11}, luma soft threshold value

ISP_DRC_3900_LUM3X2_GAS

Address: Operational Base(0xFF3F3900) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_adrc_gas_l3 Luma3x2 gaussian factor of top-left/top-right pix
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_adrc_gas_l2 Luma3x2 gaussian factor of top pix
15:14	RO	0x0	reserved
13:8	RW	0x00	sw_adrc_gas_l1 Luma3x2 gaussian factor of left/right pix
7	RO	0x0	reserved
6:0	RW	0x40	sw_adrc_gas_l0 Luma3x2 gaussian factor of center pix, disable 3x2 flt when value=0x64

Rockchip Confidencial

2.4.2.12 DEBAYER

ISP_DEBAYER_2500_CONTROL

Address: Operational Base(0xFF3F2500) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_debayer_filter_c_en_shd The shadow register of sw_debayer_filter_c_en
30	RO	0x0	ro_debayer_filter_g_en_shd The shadow register of sw_debayer_filter_g_en
29	RO	0x0	ro_debayer_en_shd The shadow register of sw_debayer_en
28	RO	0x0	ro_debayer_working 1'b0: Debayer module is not working 1'b1: Debayer module is working
27:9	RO	0x00000	reserved
8	RW	0x1	sw_debayer_filter_c_en 1'b0: C filter module will bypass 1'b1: Enable c filter module
7:5	RO	0x0	reserved
4	RW	0x1	sw_debayer_filter_g_en 1'b0: G filter module will bypass 1'b1: Enable g filter
3:1	RO	0x0	reserved
0	RW	0x0	sw_debayer_en 1'b0: Debayer module will bypass 1'b1: Enable debayer

ISP_DEBAYER_2500_G_INTERP

Address: Operational Base(0xFF3F2500) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x04	sw_debayer_max_ratio The level of sharp in the g interpolation. Range: [0,15.75] Fixed-point: [0,4,2]
23:16	RW	0x0d	sw_debayer_select_thed Select thed
15:12	RW	0x6	sw_debayer_thed1 Range: [0,0.5] Fixed-point: [0,0,4]
11:8	RW	0x3	sw_debayer_thed0 Range: [0,0.5] Fixed-point: [0,0,4]
7:4	RW	0x8	sw_debayer_dist_scale Range: [0,1.875] Fixed-point: [0,1,3]
3:1	RO	0x0	reserved
0	RW	0x1	sw_debayer_clip_en Clip enable for g interpolation If enable this bit, the interpolated g will be cliped to [Gmin,Gmax].

ISP_DEBAYER_2500_G_INTERP_FILTER1

Address: Operational Base(0xFF3F2500) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RW	0x04	sw_debayer_filter1_coe4 Range: [-16,15] Fixed-point: [1,0,4] Note: coe3+coe4=0
23:21	RO	0x0	reserved
20:16	RW	0x1c	sw_debayer_filter1_coe3 Range: [-16,15] Fixed-point: [1,0,4] Note: coe3+coe4=0
15:13	RO	0x0	reserved
12:8	RW	0x02	sw_debayer_filter1_coe2 Range: [-16,15] Fixed-point: [1,0,4] Note: coe1+coe2=0
7:5	RO	0x0	reserved
4:0	RW	0x1e	sw_debayer_filter1_coe1 Range: [-16,15] Fixed-point: [1,0,4] Note: coe1+coe2=0

ISP_DEBAYER_2500_G_INTERP_FILTER2

Address: Operational Base(0xFF3F2500) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	sw_debayer_filter2_coe4 Range: [-16,15] Fixed-point: [1,0,4] Note: 2*coe3+coe4=0
23:21	RO	0x0	reserved
20:16	RW	0x1e	sw_debayer_filter2_coe3 Range: [-16,15] Fixed-point: [1,0,4] Note: 2*coe3+coe4=0
15:13	RO	0x0	reserved
12:8	RW	0x02	sw_debayer_filter2_coe2 Range: [-16,15] Fixed-point: [1,0,4] Note: 2*coe1+coe2=0
7:5	RO	0x0	reserved
4:0	RW	0x1f	sw_debayer_filter2_coe1 Range: [-16,15] Fixed-point: [1,0,4] Note: 2*coe1+coe2=0

ISP_DEBAYER_2500_G_INTERP_OFFSET

Address: Operational Base(0xFF3F2500) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0080	sw_debayer_hf_offset Hf offset for G interpolation
15:12	RO	0x0	reserved
11:0	RW	0x004	sw_debayer_gain_offset Gain offset for G interpolation

ISP_DEBAYER_2500_G_FILTER_OFFSET

Address: Operational Base(0xFF3F2500) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x001	sw_debayer_offset Offset for G filter

2.4.2.13 CCM

ISP_CCM_0700_CTRL

Address: Operational Base(0xFF3F0700) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_ccm_en_shd Shadow of CCM module enable.
30	RO	0x0	ccm_working Ccm working
29	RO	0x0	sw_ccm_enh_adj_en_shd Shadow of CCM color enhance adjust enable.
28	RO	0x0	sw_ccm_asym_adj_en_shd Shadow of asymmetrical curve for luminance adjust enable.
27:4	RO	0x000000	reserved
3	RW	0x0	sw_ccm_asym_adj_en Enable asymmetrical curve for luminance adjust. 1'b1: Use asymmetrical curve 1'b0: Use symmetrical curve
2	RW	0x0	sw_ccm_enh_adj_en Enable CCM color enhance adjust 1'b1: Enable 1'b0: Disable
1	RW	0x0	sw_ccm_highy_adjust_dis Disable CCM high Y alpha adjustment bit 1'b1: High Y alpha adjustment disable 1'b0: High Y alpha adjustment
0	RW	0x0	sw_ccm_en_i Enable CCM module 1'b1: Enable 1'b0: Disable The reset value is 1'b0

ISP_CCM_0700_COEFF0_R

Address: Operational Base(0xFF3F0700) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x7b7	sw_ccm_coeff1_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x065	sw_ccm_coeff0_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_R

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Address: Operational Base(0xFF3F0700) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_r The R offset value for CCM calculation. The range of offset value is from -4096 to 4095.
15:11	RO	0x00	reserved
10:0	RW	0x7e4	sw_ccm_coeff2_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_G

Address: Operational Base(0xFF3F0700) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x058	sw_ccm_coeff1_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x7d9	sw_ccm_coeff0_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_G

Address: Operational Base(0xFF3F0700) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x7cf	sw_ccm_coeff2_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_B

Address: Operational Base(0xFF3F0700) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x7b7	sw_ccm_coeff1_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x002	sw_ccm_coeff0_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_B

Address: Operational Base(0xFF3F0700) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x046	sw_ccm_coeff2_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_Y

Address: Operational Base(0xFF3F0700) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x04b	sw_ccm_coeff1_y The G coefficient value of RGB2Y calculation. The value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x026	sw_ccm_coeff0_y The R coefficient value of RGB2Y calculation. The value is expanded 128 times.

ISP_CCM_0700_COEFF1_Y

Address: Operational Base(0xFF3F0700) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x00f	sw_ccm_coeff2_y The B coefficient value of RGB2Y calculation. The value is expanded 128 times.

ISP_CCM_0700_ALP_Y0

Address: Operational Base(0xFF3F0700) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y1 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y0 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y1

Address: Operational Base(0xFF3F0700) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y3 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y2 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y2

Address: Operational Base(0xFF3F0700) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y5 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x400	sw_ccm_alp_y4 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y3

Address: Operational Base(0xFF3F0700) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y7 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y6 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y4

Address: Operational Base(0xFF3F0700) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y9 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y8 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y5

Address: Operational Base(0xFF3F0700) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y11 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y10 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y6

Address: Operational Base(0xFF3F0700) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y13 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y12 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y7

Address: Operational Base(0xFF3F0700) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y15 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x400	sw_ccm_alp_y14 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y8

Address: Operational Base(0xFF3F0700) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y17 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, this register is useless. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y16 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_BOUND_BIT

Address: Operational Base(0xFF3F0700) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0xa	sw_ccm_right_bit CCM alpha interpolation curve's inflection right point. The inflection point is 2^sw_ccm_right_bit. When sw_ccm_asym_adj_en = 0, this register is useless. When sw_ccm_asym_adj_en = 1, the max value is 4'd11 because the inflection point's max value is 2048.
3:0	RW	0xa	sw_ccm_bound_bit CCM alpha interpolation curve's inflection point. The inflection point is 2^sw_ccm_bound_bit. When sw_ccm_asym_adj_en = 0, the max value is 4'd10 because the inflection point's max value is 1024. When sw_ccm_asym_adj_en = 1, the max value is 4'd11 because the inflection point's max value is 2048.

ISP_CCM_0700_ENHANCE0

Address: Operational Base(0xFF3F0700) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x04b	sw_ccm_color_coef1_g2y The R coefficient value of RGB2Y calculation, use in color enhance adjust enable. The value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x026	sw_ccm_color_coef0_r2y The R coefficient value of RGB2Y calculation, use in color enhance adjust enable. The value is expanded 128 times.

ISP_CCM_0700_ENHANCE1

Address: Operational Base(0xFF3F0700) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_ccm_color_enh_rat_max Maximum compression ratio limit for dynamic range in enhance mode.
15:11	RO	0x00	reserved
10:0	RW	0x00f	sw_ccm_color_coef2_b2y The R coefficient value of RGB2Y calculation, use in color enhance adjust enable. The value is expanded 128 times.

2.4.2.14 GAMMA_OUT

ISP_GAMMA_OUT_0900_CTRL

Address: Operational Base(0xFF3F0900) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_gamma_out_en_shd Gamma_out enable shadow
30	RO	0x0	gamma_out_working Gamma_out working status
29:3	RO	0x0000000	reserved
2	RW	0x0	sw_gamma_out_finalx4_dense_en If this bit set 1, the 44 segments gamma out curve will change to 48 segments. The adder 4 segments will add at the final. The detail as follows: the segmentation from 0 to 4095 (48 segments): 1111 1111 2222 4444 8888 16.16.16.16 32.32.32.32 64.64.64.64 128.128.128.128 256.256.256.256 256.256.256.256 256.256.256.256; (old 512.512.512.512 change to new 256.256.256.256 256.256.256.256) Note: If this bit is 0, only need configure sw_gamma_out_y0 to sw_gamma_out_y44. if this bit is 1, need configure sw_gamma_out_y0 to sw_gamma_out_y48.
1	RW	0x0	sw_gamma_out_equ_segm 1'b0: Division like segmentation of gamma curve (default after reset) the segmentation from 0 to 4095 (44 segments): 1111 1111 2222 4444 8888 16.16.16.16 32.32.32.32 64.64.64.64 128.128.128.128 256.256.256.256 512.512.512.512; 1'b1: Equidistant segmentation (all segments are equally)

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_gamma_out_en 1'b0: Gamma_out disable 1'b1: Gamma_out enable

ISP_GAMMA_OUT_0900_OFFSET

Address: Operational Base(0xFF3F0900) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_gamma_out_offset Offset value of gamma_out curve

ISP_GAMMA_OUT_0900_Y0

Address: Operational Base(0xFF3F0900) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x001	sw_gamma_out_y1 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_gamma_out_y0 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y1

Address: Operational Base(0xFF3F0900) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x003	sw_gamma_out_y3 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x002	sw_gamma_out_y2 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y2

Address: Operational Base(0xFF3F0900) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x005	sw_gamma_out_y5 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x004	sw_gamma_out_y4 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y3

Address: Operational Base(0xFF3F0900) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x007	sw_gamma_out_y7 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x006	sw_gamma_out_y6 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y4

Address: Operational Base(0xFF3F0900) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	sw_gamma_out_y9 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x008	sw_gamma_out_y8 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y5

Address: Operational Base(0xFF3F0900) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00e	sw_gamma_out_y11 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x00c	sw_gamma_out_y10 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y6

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Address: Operational Base(0xFF3F0900) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x014	sw_gamma_out_y13 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x010	sw_gamma_out_y12 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y7

Address: Operational Base(0xFF3F0900) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x01c	sw_gamma_out_y15 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x018	sw_gamma_out_y14 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y8

Address: Operational Base(0xFF3F0900) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x028	sw_gamma_out_y17 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x020	sw_gamma_out_y16 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y9

Address: Operational Base(0xFF3F0900) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x038	sw_gamma_out_y19 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x030	sw_gamma_out_y18 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y10

Address: Operational Base(0xFF3F0900) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x050	sw_gamma_out_y21 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x040	sw_gamma_out_y20 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y11

Address: Operational Base(0xFF3F0900) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x070	sw_gamma_out_y23 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x060	sw_gamma_out_y22 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y12

Address: Operational Base(0xFF3F0900) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a0	sw_gamma_out_y25 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x080	sw_gamma_out_y24 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

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ISP_GAMMA_OUT_0900_Y13

Address: Operational Base(0xFF3F0900) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e0	sw_gamma_out_y27 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x0c0	sw_gamma_out_y26 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y14

Address: Operational Base(0xFF3F0900) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x140	sw_gamma_out_y29 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x100	sw_gamma_out_y28 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y15

Address: Operational Base(0xFF3F0900) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x1c0	sw_gamma_out_y31 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x180	sw_gamma_out_y30 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y16

Address: Operational Base(0xFF3F0900) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x280	sw_gamma_out_y33 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_gamma_out_y32 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y17

Address: Operational Base(0xFF3F0900) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x380	sw_gamma_out_y35 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x300	sw_gamma_out_y34 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y18

Address: Operational Base(0xFF3F0900) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x500	sw_gamma_out_y37 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x400	sw_gamma_out_y36 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y19

Address: Operational Base(0xFF3F0900) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x700	sw_gamma_out_y39 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x600	sw_gamma_out_y38 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y20

Address: Operational Base(0xFF3F0900) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xa00	sw_gamma_out_y41 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x800	sw_gamma_out_y40 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y21

Address: Operational Base(0xFF3F0900) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xe00	sw_gamma_out_y43 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0xc00	sw_gamma_out_y42 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y22

Address: Operational Base(0xFF3F0900) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfff	sw_gamma_out_y45 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0xfff	sw_gamma_out_y44 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y23

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Address: Operational Base(0xFF3F0900) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfff	sw_gamma_out_y47 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0xfff	sw_gamma_out_y46 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y24

Address: Operational Base(0xFF3F0900) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xfff	sw_gamma_out_y48 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

2.4.2.15 DEHAZE_ENHANCE

ISP_DHAZ_3C00_CTRL

Address: Operational Base(0xFF3F3C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd Dehaze self force update
30	RO	0x0	dhaz_working Dehaze working flag, read only. 1'b0: Closed 1'b1: Working
29	RO	0x0	reserved
28	RW	0x0	sw_dhaz_enh_luma_en Luma curve enable in enhance mode. 1'b0: Use sw_dhaz_enhance_value 1'b1: Use luma curve
27	RW	0x0	sw_dhaz_color_deviate_en Color deviation enable, only use in enhance mode. 1'b0: Use sw_dhaz_enhance_chroma 1'b1: Correct color deviation in enhance mode
26	RW	0x0	sw_dhaz_round_en Dehaze input round enable 1'b0: 12 bit cut 10 bit(floor) 1'b1: 12 bit cut 10 bit(round)
25	RW	0x0	sw_dhaz_soft_wr_en Dehaze soft write register, must shadow. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
24	RW	0x0	sw_dhaz_ckg_dis Clock gating 1'b0: Enable 1'b1: Disable
23:21	RO	0x0	reserved
20	RW	0x0	sw_dhaz_enhance_en Work mode control, must shadow. 1'b0: Dehaze mode 1'b1: Enhance mode
19:17	RO	0x0	reserved
16	RW	0x0	sw_dhaz_air_lc_en Only dehaze mode valid, must shadow. 1'b0: Use adaption air_base 1'b1: Use (max(r,g,b),air_base)
15:13	RO	0x0	reserved
12	RW	0x0	sw_dhaz_hpara_en Hist parameter, must shadow. 1'b0: Disable 1'b1: Enable
11:9	RO	0x0	reserved
8	RW	0x1	sw_dhaz_hist_en Hist equalization, must shadow. 1'b0: Disable 1'b1: Enable
7:5	RO	0x0	reserved
4	RW	0x1	sw_dhaz_dc_en Dehaze dark channel, must shadow. 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	sw_dhaz_en_mux Dehaze module enable, must shadow. 1'b0: Disable 1'b1: Enable

ISP_DHAZ_3C00_ADP0

Address: Operational Base(0xFF3F3C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x1b	sw_dhaz_yblk_th Y channel self-adaption threshold of block ratio. Range: [0, 255], from 0.002*col_blk*row_blk to 0.01*col_blk*row_blk Fixed-point: [0, 8, 0]
23:16	RW	0xf9	sw_dhaz_yhist_th Y channel self-adaption high light threshold. Range: [0, 255] Fixed-point: [0, 8, 0]
15:8	RW	0xc0	sw_dhaz_dc_max_th Dark channel self-adaption high light threshold. Range: [0, 255] Fixed-point: [0, 8, 0]
7:0	RW	0x40	sw_dhaz_dc_min_th Dark channel self-adaption minimum threshold. Range: [0, 255] Fixed-point: [0, 8, 0]

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ISP_DHAZ_3C00_ADP1

Address: Operational Base(0xFF3F3C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0e6	sw_dhaz_wt_max Strength of dehaze(wt) self-adaption maximum threshold. Range: [0, 1] Fixed-point: [0, 1, 8]
15:8	RW	0xf0	sw_dhaz_bright_max Luminance self-adaption maximum threshold. Range: [0, 255] Fixed-point: [0, 8, 0]
7:0	RW	0xb4	sw_dhaz_bright_min Luminance self-adaption minimum threshold. Range: [0, 255] Fixed-point: [0, 8, 0]

ISP_DHAZ_3C00_ADP2

Address: Operational Base(0xFF3F3C00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x7d	sw_dhaz_tmax_base Tmax self-adaption base value. Range: [0, 1] Fixed-point: [0, 0, 8]
23:16	RW	0xfa	sw_dhaz_dark_th Strength of dehaze self-adaption minimum threshold. Range: [0, 255] Fixed-point: [0, 8, 0]
15:8	RW	0xfa	sw_dhaz_air_max Air self-adaption maximum threshold. Range: [0, 255] Fixed-point: [0, 8, 0]
7:0	RW	0xe6	sw_dhaz_air_min Air self-adaption minimum threshold Range: [0, 255] Fixed-point: [0, 8, 0]

ISP_DHAZ_3C00_ADP_TMAX

Address: Operational Base(0xFF3F3C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x200	sw_dhaz_tmax_max Tmax self-adaption maximum threshold. Range: [0, 1023] Fixed-point: [0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x066	sw_dhaz_tmax_off Tmax self-adaption offset threshold. Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ADP_HIST0

Address: Operational Base(0xFF3F3C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:16	RW	0x004	sw_dhaz_hist_min The minimum statistical threshold of hist. Range: [0, 1] Fixed-point: [0, 1, 8]
15:8	RW	0x40	sw_dhaz_hist_th_off The statistical threshold offset of hist. Range: [0, 255] Fixed-point: [0, 8, 0]
7:5	RO	0x0	reserved
4:0	RW	0x08	sw_dhaz_hist_k Amplify times of hist self-adaption. Range: [0, 9] Fixed-point: [0, 3, 2]

ISP_DHAZ_3C00_ADP_HIST1

Address: Operational Base(0xFF3F3C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x10	sw_dhaz_hist_gratio The strength ratio of hist. Range: [0, 4] Fixed-point: [0, 3, 5]
15:13	RO	0x0	reserved
12:0	RW	0x00e6	sw_dhaz_hist_scale Dehaze hist scale use user configuration while sw_dhaz_hpara_en is enabled. Range: [0, 31.99] Fixed-point: [0, 5, 8]

ISP_DHAZ_3C00_ENHANCE

Address: Operational Base(0xFF3F3C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0600	sw_dhaz_enhance_value The enhancement factor of the light. Range: [0, 15.99] Fixed-point: [0, 4, 10]
15:14	RO	0x0	reserved
13:0	RW	0x04cc	sw_dhaz_enhance_chroma The light enhance chrominance Range: [0, 15.99] Fixed-point: [0, 4, 10]

ISP_DHAZ_3C00_IIR0

Address: Operational Base(0xFF3F3C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x00f	sw_dhaz_iir_wt_sigma The iir sigma value of internal dehaze strength(wt). Range: [0, 7.999] Fixed-point: [0, 3, 8]
15:8	RW	0x01	sw_dhaz_iir_sigma The sigma value of iir control, maximum value is 255. Range: [0, 7.99] Fixed-point: [0, 3, 5]

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Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4:0	RW	0x08	sw_dhaz_stab_fnum The maximum number of frames to achieve stabilization. Range: [1, 31] Fixed-point: [0, 5, 0]

ISP_DHAZ_3C00_IIR1

Address: Operational Base(0xFF3F3C00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x7	sw_dhaz_iir_pre_wet Weight of previous down scale and current down scale, must > 0. Range: [1, 15] Fixed-point: [0, 4, 0]
23:19	RO	0x00	reserved
18:8	RW	0x05f	sw_dhaz_iir_tmax_sigma The iir sigma value of internal tmax. Range: [0, 1024] Fixed-point: [0, 11, 0]
7:0	RW	0x08	sw_dhaz_iir_air_sigma The iir sigma value of internal airlight. Range: [0, 255] Fixed-point: [0, 8, 0]

ISP_DHAZ_3C00_SOFT_CFG0

Address: Operational Base(0xFF3F3C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0cc	sw_dhaz_cfg_wt Software configure dehaze strength(wt). Range: [0, 1] Fixed-point: [0, 1, 8]
15:8	RW	0xd2	sw_dhaz_cfg_air Software configure airlight Range: [0, 255] Fixed-point: [0, 8, 0]
7:0	RW	0x00	sw_dhaz_cfg_alpha The weight of configure data Range: [0, 255], 255 parsing to 256. Notes: wt = ((sw_dhaz_cfg_alpha * sw_dhaz_cfg_wt + (256 - sw_dhaz_cfg_alpha) * wt_cur)/256)

ISP_DHAZ_3C00_SOFT_CFG1

Address: Operational Base(0xFF3F3C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0200	sw_dhaz_cfg_gratio Software configure gratio Range: [0, 31.99] Fixed-point: [0, 5, 8]
15:10	RO	0x00	reserved
9:0	RW	0x0cc	sw_dhaz_cfg_tmax Software configure tmax Range: [0, 1023] Fixed-point: [0, 10, 0]

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ISP_DHAZ_3C00_BF_SIGMA

Address: Operational Base(0xFF3F3C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x080	sw_dhaz_range_sigma Range sigma of bilateral filter Range: [0, 256] Fixed-point: [0, 9, 0]
15:8	RW	0x4d	sw_dhaz_space_sigma_pre Space sigma of previous bilateral filter. Range: [0, 255] Fixed-point: [0, 8, 0]
7:0	RW	0x99	sw_dhaz_space_sigma_cur Space sigma of current bilateral filter. Range: [0, 255] Fixed-point: [0, 8, 0]

ISP_DHAZ_3C00_BF_WET

Address: Operational Base(0xFF3F3C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x100	sw_dhaz_dc_weitcur Current center weight of bilateral filter Range: [0, 1] Fixed-point: [0, 1, 8]
15:9	RO	0x00	reserved
8:0	RW	0x080	sw_dhaz_bf_weight Weight of bilateral filter Range: [0, 1] Fixed-point: [0, 1, 8]

ISP_DHAZ_3C00_ENH_CURVE0

Address: Operational Base(0xFF3F3C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	sw_dhaz_curve1 Map curve 1 Range: [0, 1023] Fixed-point: [0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_dhaz_curve0 Map curve 0 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_CURVE1

Address: Operational Base(0xFF3F3C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x0c0	sw_dhaz_curve3 Map curve 3 Range: [0, 1023] Fixed-point: [0, 10, 0]
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x080	sw_dhaz_curve2 Map curve 2 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_CURVE2

Address: Operational Base(0xFF3F3C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x140	sw_dhaz_curve5 Map curve 5 Range: [0, 1023] Fixed-point: [0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x100	sw_dhaz_curve4 Map curve 4 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_CURVE3

Address: Operational Base(0xFF3F3C00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x1c0	sw_dhaz_curve7 Map curve 7 Range: [0, 1023] Fixed-point: [0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x180	sw_dhaz_curve6 Map curve 6 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_CURVE4

Address: Operational Base(0xFF3F3C00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x240	sw_dhaz_curve9 Map curve 9 Range: [0, 1023] Fixed-point: [0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_curve8 Map curve 8 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_CURVE5

Address: Operational Base(0xFF3F3C00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x2c0	sw_dhaz_curve11 Map curve 11 Range: [0, 1023] Fixed-point: [0, 10, 0]

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x280	sw_dhaz_curve10 Map curve 10 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_CURVE6

Address: Operational Base(0xFF3F3C00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x340	sw_dhaz_curve13 Map curve 13 Range: [0, 1023] Fixed-point: [0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x300	sw_dhaz_curve12 Map curve 12 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_CURVE7

Address: Operational Base(0xFF3F3C00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3c0	sw_dhaz_curve15 Map curve 15 Range: [0, 1023] Fixed-point: [0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x380	sw_dhaz_curve14 Map curve 14 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_CURVE8

Address: Operational Base(0xFF3F3C00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x3ff	sw_dhaz_curve16 Map curve 16 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_GAUS

Address: Operational Base(0xFF3F3C00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x02	sw_dhaz_gaus_h2 The gaussian filter coefficient, 3*3window, 32/32 normalization.(h0+4*h1+4*h2=32)
15:14	RO	0x0	reserved
13:8	RW	0x04	sw_dhaz_gaus_h1 The gaussian filter coefficient, 3*3window, 32/32 normalization.(h0+4*h1+4*h2=32)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x08	sw_dhaz_gaus_h0 The gaussian filter coefficient, 3*3window, 32/32 normalization.(h0+4*h1+4*h2=32)

ISP_DHAZ_3C00_GAIN_IDX0

Address: Operational Base(0xFF3F3C00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	sw_dhaz_sigma_idx3 Dehaze gain sigma index 3
23:16	RW	0x30	sw_dhaz_sigma_idx2 Dehaze gain sigma index 2
15:8	RW	0x20	sw_dhaz_sigma_idx1 Dehaze gain sigma index 1
7:0	RW	0x10	sw_dhaz_sigma_idx0 Dehaze gain sigma index 0

ISP_DHAZ_3C00_GAIN_IDX1

Address: Operational Base(0xFF3F3C00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	sw_dhaz_sigma_idx7 Dehaze gain sigma index 7
23:16	RW	0x70	sw_dhaz_sigma_idx6 Dehaze gain sigma index 6
15:8	RW	0x60	sw_dhaz_sigma_idx5 Dehaze gain sigma index 5
7:0	RW	0x50	sw_dhaz_sigma_idx4 Dehaze gain sigma index 4

ISP_DHAZ_3C00_GAIN_IDX2

Address: Operational Base(0xFF3F3C00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:24	RW	0xc0	sw_dhaz_sigma_idx11 Dehaze gain sigma index 11
23:16	RW	0xb0	sw_dhaz_sigma_idx10 Dehaze gain sigma index 10
15:8	RW	0xa0	sw_dhaz_sigma_idx9 Dehaze gain sigma index 9
7:0	RW	0x90	sw_dhaz_sigma_idx8 Dehaze gain sigma index 8

ISP_DHAZ_3C00_GAIN_IDX3

Address: Operational Base(0xFF3F3C00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0xf0	sw_dhaz_sigma_idx14 Dehaze gain sigma index 14
15:8	RW	0xe0	sw_dhaz_sigma_idx13 Dehaze gain sigma index 13
7:0	RW	0xd0	sw_dhaz_sigma_idx12 Dehaze gain sigma index 12

ISP_DHAZ_3C00_GAIN_LUT0

Address: Operational Base(0xFF3F3C00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x200	sw_dhaz_sigma_lut1 Dehaze gain sigma data 1 of look up table Range: [1, 1023]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut0 Dehaze gain sigma data 0 of look up table Range: [1, 1023]

ISP_DHAZ_3C00_GAIN_LUT1

Address: Operational Base(0xFF3F3C00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x200	sw_dhaz_sigma_lut3 Dehaze gain sigma data 3 of look up table Range: [1, 1023]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut2 Dehaze gain sigma data 2 of look up table Range: [1, 1023]

ISP_DHAZ_3C00_GAIN_LUT2

Address: Operational Base(0xFF3F3C00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x200	sw_dhaz_sigma_lut5 Dehaze gain sigma data 5 of look up table Range: [1, 1023]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut4 Dehaze gain sigma data 4 of look up table Range: [1, 1023]

ISP_DHAZ_3C00_GAIN_LUT3

Address: Operational Base(0xFF3F3C00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x200	sw_dhaz_sigma_lut7 Dehaze gain sigma data 7 of look up table Range: [1, 1023]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut6 Dehaze gain sigma data 6 of look up table Range: [1, 1023]

ISP_DHAZ_3C00_GAIN_LUT4

Address: Operational Base(0xFF3F3C00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x200	sw_dhaz_sigma_lut9 Dehaze gain sigma data 9 of look up table Range: [1, 1023]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut8 Dehaze gain sigma data 8 of look up table Range: [1, 1023]

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ISP_DHAZ_3C00_GAIN_LUT5

Address: Operational Base(0xFF3F3C00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x200	sw_dhaz_sigma_lut11 Dehaze gain sigma data 11 of look up table Range: [1, 1023]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut10 Dehaze gain sigma data 10 of look up table Range: [1, 1023]

ISP_DHAZ_3C00_GAIN_LUT6

Address: Operational Base(0xFF3F3C00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x200	sw_dhaz_sigma_lut13 Dehaze gain sigma data 13 of look up table Range: [1, 1023]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut12 Dehaze gain sigma data 12 of look up table Range: [1, 1023]

ISP_DHAZ_3C00_GAIN_LUT7

Address: Operational Base(0xFF3F3C00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x200	sw_dhaz_sigma_lut15 Dehaze gain sigma data 15 of look up table Range: [1, 1023]
15:10	RO	0x00	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut14 Dehaze gain sigma data 14 of look up table Range: [1, 1023]

ISP_DHAZ_3C00_GAIN_LUT8

Address: Operational Base(0xFF3F3C00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x200	sw_dhaz_sigma_lut16 Dehaze gain sigma data 16 of look up table Range: [1, 1023]

ISP_DHAZ_3C00_SUMH_RD

Address: Operational Base(0xFF3F3C00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_pic_sumh Picture hist sum, read only.

ISP_DHAZ_3C00_HIST_WR0

Address: Operational Base(0xFF3F3C00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x020	hist_wr2 Soft write hist rgb register 2, shadow read.
19:10	RW	0x010	hist_wr1 Soft write hist rgb register 1, shadow read.
9:0	RW	0x000	hist_wr0 Soft write hist rgb register 0, shadow read.

ISP_DHAZ_3C00_HIST_WR1

Address: Operational Base(0xFF3F3C00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x050	hist_wr5 Soft write hist rgb register 5, shadow read.
19:10	RW	0x040	hist_wr4 Soft write hist rgb register 4, shadow read.
9:0	RW	0x030	hist_wr3 Soft write hist rgb register 3, shadow read.

ISP_DHAZ_3C00_HIST_WR2

Address: Operational Base(0xFF3F3C00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x080	hist_wr8 Soft write hist rgb register 8, shadow read.
19:10	RW	0x070	hist_wr7 Soft write hist rgb register 7, shadow read.
9:0	RW	0x060	hist_wr6 Soft write hist rgb register 6, shadow read.

ISP_DHAZ_3C00_HIST_WR3

Address: Operational Base(0xFF3F3C00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0b0	hist_wr11 Soft write hist rgb register 11, shadow read.
19:10	RW	0x0a0	hist_wr10 Soft write hist rgb register 10, shadow read.
9:0	RW	0x090	hist_wr9 Soft write hist rgb register 9, shadow read.

ISP_DHAZ_3C00_HIST_WR4

Address: Operational Base(0xFF3F3C00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0e0	hist_wr14 Soft write hist rgb register 14, shadow read.
19:10	RW	0x0d0	hist_wr13 Soft write hist rgb register 13, shadow read.
9:0	RW	0x0c0	hist_wr12 Soft write hist rgb register 12, shadow read.

ISP_DHAZ_3C00_HIST_WR5

Address: Operational Base(0xFF3F3C00) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x110	hist_wr17 Soft write hist rgb register 17, shadow read.
19:10	RW	0x100	hist_wr16 Soft write hist rgb register 16, shadow read.
9:0	RW	0x0f0	hist_wr15 Soft write hist rgb register 15, shadow read.

ISP_DHAZ_3C00_HIST_WR6

Address: Operational Base(0xFF3F3C00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x140	hist_wr20 Soft write hist rgb register 20, shadow read.
19:10	RW	0x130	hist_wr19 Soft write hist rgb register 19, shadow read.
9:0	RW	0x120	hist_wr18 Soft write hist rgb register 18, shadow read.

ISP_DHAZ_3C00_HIST_WR7

Address: Operational Base(0xFF3F3C00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x170	hist_wr23 Soft write hist rgb register 23, shadow read.
19:10	RW	0x160	hist_wr22 Soft write hist rgb register 22, shadow read.
9:0	RW	0x150	hist_wr21 Soft write hist rgb register 21, shadow read.

ISP_DHAZ_3C00_HIST_WR8

Address: Operational Base(0xFF3F3C00) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x1a0	hist_wr26 Soft write hist rgb register 26, shadow read.
19:10	RW	0x190	hist_wr25 Soft write hist rgb register 25, shadow read.
9:0	RW	0x180	hist_wr24 Soft write hist rgb register 24, shadow read.

ISP_DHAZ_3C00_HIST_WR9

Address: Operational Base(0xFF3F3C00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x1d0	hist_wr29 Soft write hist rgb register 29, shadow read.
19:10	RW	0x1c0	hist_wr28 Soft write hist rgb register 28, shadow read.
9:0	RW	0x1b0	hist_wr27 Soft write hist rgb register 27, shadow read.

ISP_DHAZ_3C00_HIST_WR10

Address: Operational Base(0xFF3F3C00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x200	hist_wr32 Soft write hist rgb register 32, shadow read.
19:10	RW	0x1f0	hist_wr31 Soft write hist rgb register 31, shadow read.
9:0	RW	0x1e0	hist_wr30 Soft write hist rgb register 30, shadow read.

ISP_DHAZ_3C00_HIST_WR11

Address: Operational Base(0xFF3F3C00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x230	hist_wr35 Soft write hist rgb register 35, shadow read.
19:10	RW	0x220	hist_wr34 Soft write hist rgb register 34, shadow read.
9:0	RW	0x210	hist_wr33 Soft write hist rgb register 33, shadow read.

ISP_DHAZ_3C00_HIST_WR12

Address: Operational Base(0xFF3F3C00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x260	hist_wr38 Soft write hist rgb register 38, shadow read.
19:10	RW	0x250	hist_wr37 Soft write hist rgb register 37, shadow read.
9:0	RW	0x240	hist_wr36 Soft write hist rgb register 36, shadow read.

ISP_DHAZ_3C00_HIST_WR13

Address: Operational Base(0xFF3F3C00) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x290	hist_wr41 Soft write hist rgb register 41, shadow read.
19:10	RW	0x280	hist_wr40 Soft write hist rgb register 40, shadow read.
9:0	RW	0x270	hist_wr39 Soft write hist rgb register 39, shadow read.

ISP_DHAZ_3C00_HIST_WR14

Address: Operational Base(0xFF3F3C00) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x2c0	hist_wr44 Soft write hist rgb register 44, shadow read.
19:10	RW	0x2b0	hist_wr43 Soft write hist rgb register 43, shadow read.
9:0	RW	0x2a0	hist_wr42 Soft write hist rgb register 42, shadow read.

ISP_DHAZ_3C00_HIST_WR15

Address: Operational Base(0xFF3F3C00) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x2f0	hist_wr47 Soft write hist rgb register 47, shadow read.
19:10	RW	0x2e0	hist_wr46 Soft write hist rgb register 46, shadow read.
9:0	RW	0x2d0	hist_wr45 Soft write hist rgb register 45, shadow read.

ISP_DHAZ_3C00_HIST_WR16

Address: Operational Base(0xFF3F3C00) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x320	hist_wr50 Soft write hist rgb register 50, shadow read.
19:10	RW	0x310	hist_wr49 Soft write hist rgb register 49, shadow read.
9:0	RW	0x300	hist_wr48 Soft write hist rgb register 48, shadow read.

ISP_DHAZ_3C00_HIST_WR17

Address: Operational Base(0xFF3F3C00) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x350	hist_wr53 Soft write hist rgb register 53, shadow read.
19:10	RW	0x340	hist_wr52 Soft write hist rgb register 52, shadow read.
9:0	RW	0x330	hist_wr51 Soft write hist rgb register 51, shadow read.

ISP_DHAZ_3C00_HIST_WR18

Address: Operational Base(0xFF3F3C00) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x380	hist_wr56 Soft write hist rgb register 56, shadow read.
19:10	RW	0x370	hist_wr55 Soft write hist rgb register 55, shadow read.
9:0	RW	0x360	hist_wr54 Soft write hist rgb register 54, shadow read.

ISP_DHAZ_3C00_HIST_WR19

Address: Operational Base(0xFF3F3C00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3b0	hist_wr59 Soft write hist rgb register 59, shadow read.
19:10	RW	0x3a0	hist_wr58 Soft write hist rgb register 58, shadow read.
9:0	RW	0x390	hist_wr57 Soft write hist rgb register 57, shadow read.

ISP_DHAZ_3C00_HIST_WR20

Address: Operational Base(0xFF3F3C00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x3e0	hist_wr62 Soft write hist rgb register 62, shadow read.
19:10	RW	0x3d0	hist_wr61 Soft write hist rgb register 61, shadow read.
9:0	RW	0x3c0	hist_wr60 Soft write hist rgb register 60, shadow read.

ISP_DHAZ_3C00_HIST_WR21

Address: Operational Base(0xFF3F3C00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x3f0	hist_wr63 Soft write hist rgb register 63, shadow read.

ISP_DHAZ_3C00_CTRL_SHD

Address: Operational Base(0xFF3F3C00) + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	dhaz_gain_working Dehaze gain module working flag 1'b0: Not working 1'b1: Working
30	RO	0x0	dhaz_hist_working Dehaze hist equalization module working flag 1'b0: Not working 1'b1: Working
29	RO	0x0	dhaz_bilat_working Dehaze dark channel module working flag 1'b0: Not working 1'b1: Working
28	RO	0x0	dhaz_enh_luma_en_shd Enhance luma curve enable shadow
27	RO	0x0	dhaz_color_deviate_en_shd Color deviation enable shadow
26:21	RO	0x00	reserved
20	RO	0x0	sw_dhaz_enhance_en_shd Enhance mode enable shadow
19:17	RO	0x0	reserved
16	RO	0x0	sw_dhaz_air_lc_shd Dehaze airlight use large channel enable shadow
15:13	RO	0x0	reserved
12	RO	0x0	sw_dhaz_hpara_en_shd Dehaze hist parameter enable shadow
11:9	RO	0x0	reserved
8	RO	0x0	sw_dhaz_hist_en_shd Dehaze hist equilibration enable shadow
7:5	RO	0x0	reserved
4	RO	0x0	sw_dhaz_dc_en_shd Dehaze dark channel enable shadow
3:0	RO	0x0	reserved

ISP_DHAZ_3C00_ADP_RD0

Address: Operational Base(0xFF3F3C00) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RO	0xc8	dhaz_adp_air_base Self-adaptive value of air_base, read only.
15:9	RO	0x00	reserved
8:0	RO	0x003	dhaz_adp_wt Self-adaptive value of dehaze strength(wt) , read only.

ISP_DHAZ_3C00_ADP_RD1

Address: Operational Base(0xFF3F3C00) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0009	dhaz_adp_gratio Self-adaptive value of hist gratio, read only.
15:10	RO	0x00	reserved
9:0	RO	0x0cd	dhaz_adp_tmax Self-adaptive value of tmax, read only.

ISP_DHAZ_3C00_HIST_REG0

Address: Operational Base(0xFF3F3C00) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x010	h_rgb_iir1 Histogram register 1 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x000	h_rgb_iir0 Histogram register 0 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG1

Address: Operational Base(0xFF3F3C00) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x030	h_rgb_iir3 Histogram register 3 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x020	h_rgb_iir2 Histogram register 2 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG2

Address: Operational Base(0xFF3F3C00) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x050	h_rgb_iir5 Histogram register 5 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x040	h_rgb_iir4 Histogram register 4 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG3

Address: Operational Base(0xFF3F3C00) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x070	h_rgb_iir7 Histogram register 7 of rgb iir, read only.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x060	h_rgb_iir6 Histogram register 6 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG4

Address: Operational Base(0xFF3F3C00) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x090	h_rgb_iir9 Histogram register 9 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x080	h_rgb_iir8 Histogram register 8 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG5

Address: Operational Base(0xFF3F3C00) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x0b0	h_rgb_iir11 Histogram register 11 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x0a0	h_rgb_iir10 Histogram register 10 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG6

Address: Operational Base(0xFF3F3C00) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x0d0	h_rgb_iir13 Histogram register 13 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x0c0	h_rgb_iir12 Histogram register 12 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG7

Address: Operational Base(0xFF3F3C00) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x0f0	h_rgb_iir15 Histogram register 15 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x0e0	h_rgb_iir14 Histogram register 14 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG8

Address: Operational Base(0xFF3F3C00) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x110	h_rgb_iir17 Histogram register 17 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x100	h_rgb_iir16 Histogram register 16 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG9

Address: Operational Base(0xFF3F3C00) + offset (0x0134)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x130	h_rgb_iir19 Histogram register 19 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x120	h_rgb_iir18 Histogram register 18 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG10

Address: Operational Base(0xFF3F3C00) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x150	h_rgb_iir21 Histogram register 21 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x140	h_rgb_iir20 Histogram register 20 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG11

Address: Operational Base(0xFF3F3C00) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x170	h_rgb_iir23 Histogram register 23 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x160	h_rgb_iir22 Histogram register 22 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG12

Address: Operational Base(0xFF3F3C00) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x190	h_rgb_iir25 Histogram register 25 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x180	h_rgb_iir24 Histogram register 24 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG13

Address: Operational Base(0xFF3F3C00) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x1b0	h_rgb_iir27 Histogram register 27 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x1a0	h_rgb_iir26 Histogram register 26 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG14

Address: Operational Base(0xFF3F3C00) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x1d0	h_rgb_iir29 Histogram register 29 of rgb iir, read only.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x1c0	h_rgb_iir28 Histogram register 28 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG15

Address: Operational Base(0xFF3F3C00) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x1f0	h_rgb_iir31 Histogram register 31 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x1e0	h_rgb_iir30 Histogram register 30 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG16

Address: Operational Base(0xFF3F3C00) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x210	h_rgb_iir33 Histogram register 33 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x200	h_rgb_iir32 Histogram register 32 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG17

Address: Operational Base(0xFF3F3C00) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x230	h_rgb_iir35 Histogram register 35 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x220	h_rgb_iir34 Histogram register 34 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG18

Address: Operational Base(0xFF3F3C00) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x250	h_rgb_iir37 Histogram register 37 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x240	h_rgb_iir36 Histogram register 36 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG19

Address: Operational Base(0xFF3F3C00) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x270	h_rgb_iir39 Histogram register 39 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x260	h_rgb_iir38 Histogram register 38 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG20

Address: Operational Base(0xFF3F3C00) + offset (0x0160)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x290	h_rgb_iir41 Histogram register 41 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x280	h_rgb_iir40 Histogram register 40 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG21

Address: Operational Base(0xFF3F3C00) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x2b0	h_rgb_iir43 Histogram register 43 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x2a0	h_rgb_iir42 Histogram register 42 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG22

Address: Operational Base(0xFF3F3C00) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x2d0	h_rgb_iir45 Histogram register 45 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x2c0	h_rgb_iir44 Histogram register 44 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG23

Address: Operational Base(0xFF3F3C00) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x2f0	h_rgb_iir47 Histogram register 47 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x2e0	h_rgb_iir46 Histogram register 46 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG24

Address: Operational Base(0xFF3F3C00) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x310	h_rgb_iir49 Histogram register 49 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x300	h_rgb_iir48 Histogram register 48 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG25

Address: Operational Base(0xFF3F3C00) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x330	h_rgb_iir51 Histogram register 51 of rgb iir, read only.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x320	h_rgb_iir50 Histogram register 50 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG26

Address: Operational Base(0xFF3F3C00) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x350	h_rgb_iir53 Histogram register 53 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x340	h_rgb_iir52 Histogram register 52 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG27

Address: Operational Base(0xFF3F3C00) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x370	h_rgb_iir55 Histogram register 55 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x360	h_rgb_iir54 Histogram register 54 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG28

Address: Operational Base(0xFF3F3C00) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x390	h_rgb_iir57 Histogram register 57 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x380	h_rgb_iir56 Histogram register 56 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG29

Address: Operational Base(0xFF3F3C00) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x3b0	h_rgb_iir59 Histogram register 59 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x3a0	h_rgb_iir58 Histogram register 58 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG30

Address: Operational Base(0xFF3F3C00) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x3d0	h_rgb_iir61 Histogram register 61 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x3c0	h_rgb_iir60 Histogram register 60 of rgb iir, read only.

ISP_DHAZ_3C00_HIST_REG31

Address: Operational Base(0xFF3F3C00) + offset (0x018C)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x3f0	h_rgb_iir63 Histogram register 63 of rgb iir, read only.
15:10	RO	0x00	reserved
9:0	RO	0x3e0	h_rgb_iir62 Histogram register 62 of rgb iir, read only.

ISP_DHAZ_3C00_ENH_LUMA0

Address: Operational Base(0xFF3F3C00) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x040	sw_dhaz_enh_luma2 Enhance luma register2 Range: [0, 1023] Fixed-point: [0, 10, 0]
19:10	RW	0x040	sw_dhaz_enh_luma1 Enhance luma register1 Range: [0, 1023] Fixed-point: [0, 10, 0]
9:0	RW	0x040	sw_dhaz_enh_luma0 Enhance luma register0 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_LUMA1

Address: Operational Base(0xFF3F3C00) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x040	sw_dhaz_enh_luma5 Enhance luma register5 Range: [0, 1023] Fixed-point: [0, 10, 0]
19:10	RW	0x040	sw_dhaz_enh_luma4 Enhance luma register4 Range: [0, 1023] Fixed-point: [0, 10, 0]
9:0	RW	0x040	sw_dhaz_enh_luma3 Enhance luma register3 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_LUMA2

Address: Operational Base(0xFF3F3C00) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0c0	sw_dhaz_enh_luma8 Enhance luma register8 Range: [0, 1023] Fixed-point: [0, 10, 0]
19:10	RW	0x080	sw_dhaz_enh_luma7 Enhance luma register7 Range: [0, 1023] Fixed-point: [0, 10, 0]

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9:0	RW	0x040	sw_dhaz_enh_luma6 Enhance luma register6 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_LUMA3

Address: Operational Base(0xFF3F3C00) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x100	sw_dhaz_enh_luma11 Enhance luma register11 Range: [0, 1023] Fixed-point: [0, 10, 0]
19:10	RW	0x100	sw_dhaz_enh_luma10 Enhance luma register10 Range: [0, 1023] Fixed-point: [0, 10, 0]
9:0	RW	0x0c0	sw_dhaz_enh_luma9 Enhance luma register9 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_LUMA4

Address: Operational Base(0xFF3F3C00) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x100	sw_dhaz_enh_luma14 Enhance luma register14 Range: [0, 1023] Fixed-point: [0, 10, 0]
19:10	RW	0x100	sw_dhaz_enh_luma13 Enhance luma register13 Range: [0, 1023] Fixed-point: [0, 10, 0]
9:0	RW	0x100	sw_dhaz_enh_luma12 Enhance luma register12 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_ENH_LUMA5

Address: Operational Base(0xFF3F3C00) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x100	sw_dhaz_enh_luma16 Enhance luma register16 Range: [0, 1023] Fixed-point: [0, 10, 0]
9:0	RW	0x100	sw_dhaz_enh_luma15 Enhance luma register15 Range: [0, 1023] Fixed-point: [0, 10, 0]

ISP_DHAZ_3C00_STAB_FRAME

Address: Operational Base(0xFF3F3C00) + offset (0x01F8)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_dhaz_stab_frame_cnt3 Hist iir stable frame count of sensor3
23:21	RO	0x0	reserved
20:16	RW	0x00	sw_dhaz_stab_frame_cnt2 Hist iir stable frame count of sensor2
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_dhaz_stab_frame_cnt1 Hist iir stable frame count of sensor1
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_dhaz_stab_frame_cnt0 Hist iir stable frame count of sensor0

ISP_DHAZ_3C00_PRE_FRAME

Address: Operational Base(0xFF3F3C00) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	sw_dhaz_pre_frame_cnt3 Thumb iir frame count of sensor3
11:8	RW	0x0	sw_dhaz_pre_frame_cnt2 Thumb iir frame count of sensor2
7:4	RW	0x0	sw_dhaz_pre_frame_cnt1 Thumb iir frame count of sensor1
3:0	RW	0x0	sw_dhaz_pre_frame_cnt0 Thumb iir frame count of sensor0

2.4.2.16 3DLUT

ISP_3DLUT_3E00_CTRL

Address: Operational Base(0xFF3F3E00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_lut3d_en_shd Sw_lut3d_en shadow bit
30	RO	0x0	lut3d_working 1'b0: Module not working 1'b1: Module working
29	RO	0x0	ro_lut_load_err_all Lut load err flag
28	RO	0x0	ddr_fetch_working Get the LUT from DDR working signal.
27:26	RO	0x0	reserved
25:24	RW	0x0	sys_itself_lut_mode Lut update mode 2'b00: Open frame_end and force update load lut mode 2'b11: soft control force update load lut mode Suggest use force-upd load lut mode.
23:1	RO	0x000000	reserved
0	RW	0x0	sw_lut3d_en 1'b0: Disable 1'b1: Enable

ISP_3DLUT_3E00_UPDATE

Address: Operational Base(0xFF3F3E00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	WO	0x0	sw_lut3d_lut_update_en LUT3D lut update pulse signal: 1'b0: Disable 1'b1: Enable

2.4.2.17 YNR

YNR_2700_GLOBAL_CTRL

Address: Operational Base(0xFF3F2700) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_ynr_en_shd YNR enable shadow bit
30	RO	0x0	sw_gain_en_shd GAIN enable shadow bit
29:28	RO	0x0	reserved
27	RW	0x0	sw_ynr_exgain_bypass_en_shd EXGAIN bypass enable shadow bit
26	RW	0x0	sw_ynr_rnr_en RNR enable bit
25	RW	0x0	sw_ynr_gate_dis A backdoor for YNR internal gating
24	RW	0x0	sw_ynr_thumb_mix_cur_en Pre thumb data mix current frame thumb data enable bit
23:20	RW	0x8	sw_ynr_global_gain_alpha Global gain alpha for YNR 1i,3f data range:[0,8]. Gain = (sw_ynr_global_gain_alpha * sw_ynr_global_gain + (8-sw_ynr_global_gain_alpha)*local_gain)>>3
19:18	RO	0x0	reserved
17:8	RW	0x010	sw_ynr_global_gain Global gain for YNR (6i,4f)
7:6	RW	0x0	sw_ynr_flt1x1_bypass_sel 2'b00: Lgft3x3_data 2'b01: Bft3x3_data 2'b10: Gauss_data
5	RW	0x0	sw_ynr_nlm11x11_bypass YNR NLM11x11 bypass bit
4	RW	0x0	sw_ynr_flt1x1_bypass YNR FT1X1 bypass bit
3	RW	0x0	sw_ynr_lgft3x3_bypass YNR LGFT3X3 bypass bit
2	RW	0x0	sw_ynr_lbft5x5_bypass YNR LBFT5X5 bypass bit
1	RW	0x0	sw_ynr_bft3x3_bypass YNR BFT3X3 bypass bit
0	RW	0x0	sw_ynr_en YNR enable bit

YNR_2700_RNR_MAX_R

Address: Operational Base(0xFF3F2700) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x80	sw_ynr_local_gainscale 1 bit integer and 7 bit fraction, for localgain/iso.
15:14	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
13:0	RW	0x3754	sw_ynr_rnr_max_r 9 bit integer and 5 bit fraction M(9bit),E(5bit).1/R^2= M/(2^E), M and E will be calculated automatically by driver. Use RNR module when no exgain. RNR module will reduce the influence of LSC.

YNR_2700_RNR_CENTER_COOR

Address: Operational Base(0xFF3F2700) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_ynr_rnr_center_coorv RNR center coordinate
15:13	RO	0x0	reserved
12:0	RW	0x0001	sw_ynr_rnr_center_coorh RNR center coordinate. Note: The bit0 =0 means RNR use configure mode, the default mode is not configure mode.

YNR_2700_LOCAL_GAIN_CTRL

Address: Operational Base(0xFF3F2700) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x10	sw_ynr_localgain_adj 4 bit integer and 4 bit fraction, for local gain adjust.
15:10	RO	0x00	reserved
9:0	RW	0x010	sw_ynr_localgain_adj_thresh 6 bit integer and 4 bit fraction.

YNR_2700_LOWNR_CTRL0

Address: Operational Base(0xFF3F2700) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0100	sw_ynr_low_bf_inv1 5 bit integer and 9 bit fraction. This signal will adjust the strength of bilateral filtering of LBFT5X5 module. Note: This signal is reciprocal value which means the smaller of this signal, the bigger of reducing noise function.
15:14	RO	0x0	reserved
13:0	RW	0x0100	sw_ynr_low_bf_inv0 5 bit integer and 9 bit fraction. This signal will adjust the strength of bilateral filtering of BFT3X3 module. Note: This signal is reciprocal value which means the smaller of this signal, the bigger of reducing noise function.

YNR_2700_LOWNR_CTRL1

Address: Operational Base(0xFF3F2700) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_ynr_low_peak_supress 1 bit integer and 7 bit fraction. This signal will adjust restrain the big hot pixel. The bigger of this signal, the more strength of reducing the isolated big hot pixel.
15:11	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
10:0	RW	0x080	sw_ynr_low_thred_adj 5 bit integer and 6 bit fraction. Adjust the threshold of low frequency filter. The bigger this signal, the stronger reducing noise.

YNR_2700_LOWNR_CTRL2

Address: Operational Base(0xFF3F2700) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x010	sw_ynr_low_dist_adj 7 bit integer and 2 bit fraction. Adjust the distance weight of LBFT5X5 bilateral filter. The bigger of this signal, the smaller of reducing noise effect.
15:10	RO	0x00	reserved
9:0	RW	0x007	sw_ynr_low_edge_adj_thresh 11 bit integer, and 0 bit fraction. Adjust the edge weight of LBFT5X5 bilateral filter. The bigger of this signal, the smaller of reducing noise effect.

YNR_2700_LOWNR_CTRL3

Address: Operational Base(0xFF3F2700) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	sw_ynr_low_bi_weight 1 bit integer and 7 bit fraction, use for original ydata merge with bft3x3 output data. The bigger of this signal, the bigger strength of low frequency reducing noise.
23:16	RW	0x64	sw_ynr_low_weight 1 bit integer and 7 bit fraction. The weight of reducing value. The bigger of this signal, the bigger strength of low frequency reducing noise.
15:11	RO	0x00	reserved
10:0	RW	0x133	sw_ynr_low_center_weight 1 bit integer and 10 bit fraction. The weight of LBFT5X5 module of center data. The bigger of this signal, the smaller strength of low frequency reducing noise.

YNR_2700_LOWNR_CTRL4

Address: Operational Base(0xFF3F2700) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_ynr_frame_full_size For frame buffer frame_full_size signal configurable. May only used for 4352x6048.
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_ynr_lbf_weight_thres For lbff5x5 MAX(weight-minclip0)

YNR_2700_GAUSS1_COEFF

Address: Operational Base(0xFF3F2700) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x054	sw_ynr_low_gauss1_coeff2 1 bit integer and 8 bit fraction
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x20	sw_ynr_low_gauss1_coeff1 0 bit integer and 6 bit fraction
7:6	RO	0x0	reserved
5:0	RW	0x0b	sw_ynr_low_gauss1_coeff0 0 bit integer and 6 bit fraction

YNR_2700_GAUSS2_COEFF

Address: Operational Base(0xFF3F2700) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x040	sw_ynr_low_gauss2_coeff2 1 bit integer and 8 bit fraction
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_ynr_low_gauss2_coeff1 0 bit integer and 6 bit fraction
7:6	RO	0x0	reserved
5:0	RW	0x10	sw_ynr_low_gauss2_coeff0 0 bit integer and 6 bit fraction

YNR_2700_SGM_DX_0_1

Address: Operational Base(0xFF3F2700) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x040	sw_ynr_luma_points_x1 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_ynr_luma_points_x0 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_2_3

Address: Operational Base(0xFF3F2700) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x0c0	sw_ynr_luma_points_x3 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x080	sw_ynr_luma_points_x2 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_4_5

Address: Operational Base(0xFF3F2700) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x140	sw_ynr_luma_points_x5 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x100	sw_ynr_luma_points_x4 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_6_7

Address: Operational Base(0xFF3F2700) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x1c0	sw_ynr_luma_points_x7 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x180	sw_ynr_luma_points_x6 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_8_9

Address: Operational Base(0xFF3F2700) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x240	sw_ynr_luma_points_x9 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x200	sw_ynr_luma_points_x8 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_10_11

Address: Operational Base(0xFF3F2700) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x2c0	sw_ynr_luma_points_x11 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x280	sw_ynr_luma_points_x10 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_12_13

Address: Operational Base(0xFF3F2700) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x340	sw_ynr_luma_points_x13 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x300	sw_ynr_luma_points_x12 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_14_15

Address: Operational Base(0xFF3F2700) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x3c0	sw_ynr_luma_points_x15 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x380	sw_ynr_luma_points_x14 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_16

Address: Operational Base(0xFF3F2700) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x400	sw_ynr_luma_points_x16 Sigma point x coordinate [0-1024]

YNR_2700_LSGM_Y_0_1

Address: Operational Base(0xFF3F2700) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a0	sw_ynr_lsgm_y1 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x04c	sw_ynr_lsgm_y0 4bit unsigned, 9bit integer and 5bit fraction. The interval widths in x direction are defined in SGM_DX_1_8 or SGM_DX_9_16.

YNR_2700_LSGM_Y_2_3

Address: Operational Base(0xFF3F2700) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e4	sw_ynr_lsgm_y3 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0d0	sw_ynr_lsgm_y2 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_LSGM_Y_4_5

Address: Operational Base(0xFF3F2700) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e4	sw_ynr_lsgm_y5 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0e8	sw_ynr_lsgm_y4 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_LSGM_Y_6_7

Address: Operational Base(0xFF3F2700) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0cc	sw_ynr_lsgm_y7 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0d8	sw_ynr_lsgm_y6 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_LSGM_Y_8_9

Address: Operational Base(0xFF3F2700) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0c0	sw_ynr_lsgm_y9 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0c4	sw_ynr_lsgm_y8 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_LSGM_Y_10_11

Address: Operational Base(0xFF3F2700) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x0b8	sw_ynr_lsgm_y11 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0bc	sw_ynr_lsgm_y10 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_LSGM_Y_12_13

Address: Operational Base(0xFF3F2700) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a4	sw_ynr_lsgm_y13 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0b4	sw_ynr_lsgm_y12 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_LSGM_Y_14_15

Address: Operational Base(0xFF3F2700) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x054	sw_ynr_lsgm_y15 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x088	sw_ynr_lsgm_y14 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_LSGM_Y_16

Address: Operational Base(0xFF3F2700) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x028	sw_ynr_lsgm_y16 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_RNR_STRENGTH03

Address: Operational Base(0xFF3F2700) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_ynr_rnr_strength3 4 bit integer and 4 bit fraction
23:16	RW	0x10	sw_ynr_rnr_strength2 4 bit integer and 4 bit fraction
15:8	RW	0x10	sw_ynr_rnr_strength1 4 bit integer and 4 bit fraction
7:0	RW	0x10	sw_ynr_rnr_strength0 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH47

Address: Operational Base(0xFF3F2700) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_ynr_rnr_strength7 4 bit integer and 4 bit fraction
23:16	RW	0x10	sw_ynr_rnr_strength6 4 bit integer and 4 bit fraction
15:8	RW	0x10	sw_ynr_rnr_strength5 4 bit integer and 4 bit fraction

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Bit	Attr	Reset Value	Description
7:0	RW	0x10	sw_ynr_rnr_strength4 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH8b

Address: Operational Base(0xFF3F2700) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_ynr_rnr_strength11 4 bit integer and 4 bit fraction
23:16	RW	0x10	sw_ynr_rnr_strength10 4 bit integer and 4 bit fraction
15:8	RW	0x10	sw_ynr_rnr_strength9 4 bit integer and 4 bit fraction
7:0	RW	0x10	sw_ynr_rnr_strength8 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTHcf

Address: Operational Base(0xFF3F2700) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_ynr_rnr_strength15 4 bit integer and 4 bit fraction
23:16	RW	0x10	sw_ynr_rnr_strength14 4 bit integer and 4 bit fraction
15:8	RW	0x10	sw_ynr_rnr_strength13 4 bit integer and 4 bit fraction
7:0	RW	0x10	sw_ynr_rnr_strength12 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH16

Address: Operational Base(0xFF3F2700) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x10	sw_ynr_rnr_strength16 4 bit integer and 4 bit fraction

YNR_2700_NLM_SIGMA_GAIN

Address: Operational Base(0xFF3F2700) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x020	sw_ynr_nlm_hi_bf_scale Denoise scale of high frequency noise. Range: [0,16) Fixed-point: [0,4,6]
15:11	RW	0x10	sw_ynr_nlm_hi_gain_alpha Control the use ratio of local gain and global gain. Range: [0,1] Fixed-point: [0,1,4]
10:0	RW	0x00e	sw_ynr_nlm_min_sigma Minimum noise sigma for high frequency noise.

YNR_2700_NLM_COE

Address: Operational Base(0xFF3F2700) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:20	RW	0x3	sw_ynr_nlm_coe_5 Coefficient 5 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]
19:16	RW	0x5	sw_ynr_nlm_coe_4 Coefficient 4 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]
15:12	RW	0x6	sw_ynr_nlm_coe_3 Coefficient 3 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]
11:8	RW	0x3	sw_ynr_nlm_coe_2 Coefficient 2 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]
7:4	RW	0x6	sw_ynr_nlm_coe_1 Coefficient 1 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]
3:0	RW	0x7	sw_ynr_nlm_coe_0 Coefficient 0 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]

YNR_2700_NLM_WEIGHT

Address: Operational Base(0xFF3F2700) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:10	RW	0x00400	sw_ynr_nlm_center_weight Extra weight for original central pixel.
9:0	RW	0x005	sw_ynr_nlm_weight_offset Offset that subtracted from calculated weight of each pixel.

YNR_2700_NLM_NR_WEIGHT

Address: Operational Base(0xFF3F2700) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x400	sw_ynr_nlm_nr_weight Control the ratio of high frequency noise that is extracted the original image. Range: [0,1] Fixed-point: [0,1,10]

2.4.2.18 CNR

ISP_CNR_2800_CTRL

Address: Operational Base(0xFF3F2800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_cnr_en_shd CNR enable shadow register
30	RO	0x0	ro_cnr_working CNR working status

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Bit	Attr	Reset Value	Description
29	RO	0x0	sw_gain_en_shd CNR gain enable shadow signal 1'b0: Disable 1'b1: Enable
28:9	RO	0x00000	reserved
8	RW	0x0	sw_cnr_bf3x3_wgt0_sel CNR bf3x3 outdata select when bf3x3 weight is 0. 1'b0: Source data 1'b1: Gaussian data
7:6	RO	0x0	reserved
5:4	RW	0x0	sw_cnr_thumb_mode CNR down sampling mode 2'b00: 2x2 mode 2'b01: 4x4 mode 2'b10: 8x6 mode 2'b11: 8x4 mode 3562 CNR only support 4x4 and 8x4 mode.
3	RO	0x0	reserved
2	RO	0x0	sw_cnr_yuv422_mode Always be 0, reserved for later version. 3562 CNR can only support 420 mode.
1	RW	0x1	sw_cnr_exgain_bypass External gain bypass enable signal, read back is shadow register. 1'b1: Bypass is enable, external gain value is fixed to sw_cnr_egain_mux. 1'b0: Bypass is disable, use external gain.
0	RW	0x0	sw_cnr_en_i CNR enable signal 1'b1: CNR enable 1'b0: CNR disable

ISP_CNR_2800_EXGAIN

Address: Operational Base(0xFF3F2800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_cnr_gain_iso To enlarge external gain, range from 8 to 128.
15:12	RW	0x8	sw_cnr_global_gain_alpha Global gain alpha for CNR, data range [0,8]. Gain = (sw_cnr_global_gain_alpha * sw_cnr_global_gain + (8 - sw_cnr_global_gain_alpha) * local_gain) >> 3
11:10	RO	0x0	reserved
9:0	RW	0x080	sw_cnr_global_gain Global gain for CNR

ISP_CNR_2800_THUMB1

Address: Operational Base(0xFF3F2800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x00c0	sw_cnr_thumb_sigma_y The sigma Y used in lbf1x7 module. Range: [1,16383] Fixed-point:[0,0,14]
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x00a0	sw_cnr_thumb_sigma_c The sigma UV used in lbf1x7 module. Range: [1,16383] Fixed-point:[0,0,14]

ISP_CNR_2800_THUMB_BF_RATIO

Address: Operational Base(0xFF3F2800) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x400	sw_cnr_thumb_bf_ratio Control the weight of in_data in lbf1x7 module out_data. range from 0 to 1024. Range: [0,1024] Fixed-point:[0,1,7]

ISP_CNR_2800_LBF_WEITD

Address: Operational Base(0xFF3F2800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	sw_lbf1x7_weit_d3 The distance weight3 in lbf1x7 module. Range: [0,128] Fixed-point:[0,1,7]
23:16	RW	0x80	sw_lbf1x7_weit_d2 The distance weight2 in lbf1x7 module. Range: [0,128] Fixed-point:[0,1,7]
15:8	RW	0x80	sw_lbf1x7_weit_d1 The distance weight1 in lbf1x7 module. Range: [0,128] Fixed-point:[0,1,7]
7:0	RW	0x80	sw_lbf1x7_weit_d0 The distance weight0 in lbf1x7 module. Range: [0,128] Fixed-point:[0,1,7]

ISP_CNR_2800_IIR_PARA1

Address: Operational Base(0xFF3F2800) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x05a	sw_cnr_wgt_slope The delete number of weit_i in IIR filter Fixed-point:[0,3,7]
19:18	RO	0x0	reserved
17:12	RW	0x04	sw_cnr_exp_shift Control shift in IIR filter, bit 6 control the shift direction. 1'b1: Shift left 1'b0: Shift right Bit 0~5 control the shift number. When shift left, the max value of bit 0~5 is 4; When shift right, the max value of bit 0~5 is 16.
11:4	RW	0xd8	sw_cnr_iir_strength The strength of IIR filter Fixed-point:[0,0,8]
3:0	RW	0x5	sw_cnr_iir_uvgain UV gain of IIR filter. Range: [0,8]

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ISP_CNR_2800_IIR_PARA2

Address: Operational Base(0xFF3F2800) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x3a	sw_cnr_iir_uv_clip Clip out weight sum in IIR filter, range from 1 to 63. Fixed-point:[0,4,3]
7:6	RO	0x0	reserved
5:0	RW	0x02	sw_cnr_chroma_ghost IIR filter min wei_i Fixed-point:[0,0,6]

ISP_CNR_2800_GAUS_COE1

Address: Operational Base(0xFF3F2800) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x06	sw_cnr_gaus_coe3 Gaussian filter coefficient3 Fixed-point:[0,0,7]
23	RO	0x0	reserved
22:16	RW	0x1c	sw_cnr_gaus_coe2 Gaussian filter coefficient2 Fixed-point:[0,0,7]
15	RO	0x0	reserved
14:8	RW	0x11	sw_cnr_gaus_coe1 Gaussian filter coefficient1 Fixed-point:[0,0,7]
7	RO	0x0	reserved
6:0	RW	0x04	sw_cnr_gaus_coe0 Gaussian filter coefficient0 Fixed-point:[0,0,7]

ISP_CNR_2800_GAUS_COE2

Address: Operational Base(0xFF3F2800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x30	sw_cnr_gaus_coe5 Gaussian filter coefficient5 Fixed-point:[0,0,7]
7	RO	0x0	reserved
6:0	RW	0x1c	sw_cnr_gaus_coe4 Gaussian filter coefficient4 Fixed-point:[0,0,7]

ISP_CNR_2800_GAUS_RATIO

Address: Operational Base(0xFF3F2800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:20	RW	0x400	sw_cnr_global_alpha The in_data weight of bf3x3 out_data, range from 0 to 1024. Fixed-point:[0,1,10]
19:12	RW	0x00	sw_cnr_bf_wgt_clip The min weight in bf3x3 module, range from 0 to 128. Fixed-point:[0,0,8]
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x400	sw_cnr_gaus_ratio The src_data weight of gaus_out_data, range from 0 to 1024. Fixed-point:[0,1,10]

ISP_CNR_2800_BF_PARA1

Address: Operational Base(0xFF3F2800) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	sw_cnr_bf_ratio The in_data ratio in bf3x3 bilateral filter Fixed-point:[0,1,7]
23:22	RO	0x0	reserved
21:8	RW	0x01b3	sw_cnr_sigma_r The sigma of bf3x3 module Fixed-point:[0,0,14]
7	RO	0x0	reserved
6:0	RW	0x40	sw_cnr_uv_gain UV gain of bf3x3 module Fixed-point:[0,3,4]

ISP_CNR_2800_BF_PARA2

Address: Operational Base(0xFF3F2800) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_cnr_adj_ratio The adjust ratio in bf3x3 module, range from 0 to 16384. Fixed-point:[0,15,10]
15:9	RO	0x00	reserved
8:0	RW	0x014	sw_cnr_adj_offset The adjust offset in bf3x3 module

ISP_CNR_2800_SIGMA0

Address: Operational Base(0xFF3F2800) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	sw_cnr_sigma_y3 Sigma curve y3 Fixed-point:[0,2,6]
23:16	RW	0x55	sw_cnr_sigma_y2 Sigma curve y2 Fixed-point:[0,2,6]
15:8	RW	0x80	sw_cnr_sigma_y1 Sigma curve y1 Fixed-point:[0,2,6]
7:0	RW	0xff	sw_cnr_sigma_y0 Sigma curve y0 Fixed-point:[0,2,6]

ISP_CNR_2800_SIGMA1

Address: Operational Base(0xFF3F2800) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_cnr_sigma_y7 Sigma curve y7 Fixed-point:[0,2,6]
23:16	RW	0x15	sw_cnr_sigma_y6 Sigma curve y6 Fixed-point:[0,2,6]

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Bit	Attr	Reset Value	Description
15:8	RW	0x20	sw_cnr_sigma_y5 Sigma curve y5 Fixed-point:[0,2,6]
7:0	RW	0x2b	sw_cnr_sigma_y4 Sigma curve y4 Fixed-point:[0,2,6]

ISP_CNR_2800_SIGMA2

Address: Operational Base(0xFF3F2800) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	sw_cnr_sigma_y11 Sigma curve y11 Fixed-point:[0,2,6]
23:16	RW	0x02	sw_cnr_sigma_y10 Sigma curve y10 Fixed-point:[0,2,6]
15:8	RW	0x04	sw_cnr_sigma_y9 Sigma curve y9 Fixed-point:[0,2,6]
7:0	RW	0x08	sw_cnr_sigma_y8 Sigma curve y8 Fixed-point:[0,2,6]

ISP_CNR_2800_SIGMA3

Address: Operational Base(0xFF3F2800) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	sw_cnr_sigma_y12 Sigma curve y12 Fixed-point:[0,2,6]

ISP_CNR_2800_IIR_GLOBAL_GAIN

Address: Operational Base(0xFF3F2800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_cnr_iir_gain_alpha IIR gain alpha control. This value can only be 8 in current version.
7:0	RW	0x40	sw_cnr_iir_global_gain The global gain in IIR filter Fixed-point:[0,4,4]

2.4.2.19 SHARP

ISP_SHARP_2900_EN

Address: Operational Base(0xFF3F2900) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_sharp_bypass_shd Shadow of sw_sharp_bypass 1'b0: Not bypass 1'b1: Bypass
30	RO	0x0	ro_sharp_en_shd Shadow of sw_sharp_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
29	RO	0x0	ro_sharp_working Sharp working flag 1'b0: Not working 1'b1: Working
28	RO	0x0	ro_sharp_center_mode_shd Shadow of sw_sharp_center_mode 1'b0: Disable 1'b1: Enable
27	RO	0x0	ro_sharp_exgain_bypass_shd Shadow of sw_sharp_exgain_bypass 1'b0: Disable 1'b1: Enable
26	RW	0x0	sw_sharp_radius_ds_mode_shd Shadow of sharp radius strength down scale mode. 1'b0: Down scale is 128 1'b1: Down scale is 256
25:17	RO	0x000	reserved
16	RW	0x0	ro_sharp_clk_dis_shd Shadow of sw_sharp_clk_dis 1'b0: Not disable 1'b1: Disable
15	RW	0x0	sw_sharp_clk_dis Clock gating 1'b0: Not disable 1'b1: Disable
14:8	RO	0x00	reserved
7	RW	0x0	sw_sharp_add_mode Final output add mode. 1'b0: Use bilateral filter data add 1'b1: Use sharp input data add
6	RW	0x0	sw_sharp_clip_hf_mode High filter luminance lut clip mode. 1'b0: Use sharp input data 1'b1: Use gaussian filter output data
5	RO	0x0	reserved
4	RW	0x0	sw_sharp_radius_ds_mode Sharp radius of strength down scale mode. 1'b0: Down scale is 128 1'b1: Down scale is 256
3	RW	0x0	sw_sharp_exgain_bypass Sharp external gain bypass 1'b0: Disable, use sw_sharp_global_gain 1'b1: Enable, use external up scale gain
2	RW	0x0	sw_sharp_center_mode Sharp center mode 1'b1: Use configure image center coordinate 1'b0: Use image size, center_width = pic_width/2, center_height = pic_height/2
1	RW	0x0	sw_sharp_bypass Sharp bypass 1'b0: Not bypass 1'b1: Bypass

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_sharp_en Sharp module enable 1'b0: Disable 1'b1: Enable

ISP_SHARP_2900_RATIO

Address: Operational Base(0xFF3F2900) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x28	sw_sharp_sharp_ratio Sharp ratio Range: [0, 31.275] Fixed-point: [0, 5, 2]
23:16	RW	0x80	sw_sharp_bf_ratio Sharp bilateral filter ratio. Range: [0, 1] Fixed-point: [0, 1, 7]
15:8	RW	0x00	sw_sharp_gaus_ratio Sharp gauss ratio. Range: [0, 1] Fixed-point: [0, 1, 7]
7:0	RW	0x33	sw_sharp_pbf_ratio Sharp pre-bilateral filter ratio. Range: [0, 1] Fixed-point: [0, 1, 7]

ISP_SHARP_2900_LUMA_DX

Address: Operational Base(0xFF3F2900) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x7	sw_sharp_luma_dx7 Distance between point 6 and point 7. The actual distance is equal to 2^sw_sharp_luma_dx7
23:20	RW	0x8	sw_sharp_luma_dx6 Distance between point 5 and point 6. The actual distance is equal to 2^sw_sharp_luma_dx6
19:16	RW	0x8	sw_sharp_luma_dx5 Distance between point 4 and point 5. The actual distance is equal to 2^sw_sharp_luma_dx5
15:12	RW	0x7	sw_sharp_luma_dx4 Distance between point 3 and point 4. The actual distance is equal to 2^sw_sharp_luma_dx4
11:8	RW	0x7	sw_sharp_luma_dx3 Distance between point 2 and point 3. The actual distance is equal to 2^sw_sharp_luma_dx3
7:4	RW	0x6	sw_sharp_luma_dx2 Distance between point 1 and point 2. The actual distance is equal to 2^sw_sharp_luma_dx2
3:0	RW	0x6	sw_sharp_luma_dx1 Distance between point 0 and point 1. The actual distance is equal to 2^sw_sharp_luma_dx1 Notes: The total distance must be equal to 1024

ISP_SHARP_2900_PBF_SIGMA_INV_0

Rockchip Confidencial

Address: Operational Base(0xFF3F2900) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x094	sw_sharp_pbf_sigma_inv_2 Sharp pre bilateral filter sigma inverse 2 Range: [10, 512]
19:10	RW	0x0c1	sw_sharp_pbf_sigma_inv_1 Sharp pre bilateral filter sigma inverse 1 Range: [10, 512]
9:0	RW	0x115	sw_sharp_pbf_sigma_inv_0 Sharp pre bilateral filter sigma inverse 0 Range: [10, 512]

ISP_SHARP_2900_PBF_SIGMA_INV_1

Address: Operational Base(0xFF3F2900) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x078	sw_sharp_pbf_sigma_inv_5 Sharp pre bilateral filter sigma inverse 5 Range: [10, 512]
19:10	RW	0x065	sw_sharp_pbf_sigma_inv_4 Sharp pre bilateral filter sigma inverse 4 Range: [10, 512]
9:0	RW	0x094	sw_sharp_pbf_sigma_inv_3 Sharp pre bilateral filter sigma inverse 3 Range: [10, 512]

ISP_SHARP_2900_PBF_SIGMA_INV_2

Address: Operational Base(0xFF3F2900) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x094	sw_sharp_pbf_sigma_inv_7 Sharp pre bilateral filter sigma inverse 7 Range: [10, 512]
9:0	RW	0x094	sw_sharp_pbf_sigma_inv_6 Sharp pre bilateral filter sigma inverse 6 Range: [10, 512]

ISP_SHARP_2900_BF_SIGMA_INV_0

Address: Operational Base(0xFF3F2900) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0f1	sw_sharp_bf_sigma_inv_2 Sharp bilateral filter sigma inverse 2 Range: [10, 512]
19:10	RW	0x13b	sw_sharp_bf_sigma_inv_1 Sharp bilateral filter sigma inverse 1 Range: [10, 512]
9:0	RW	0x1c7	sw_sharp_bf_sigma_inv_0 Sharp bilateral filter sigma inverse 0 Range: [10, 512]

ISP_SHARP_2900_BF_SIGMA_INV_1

Address: Operational Base(0xFF3F2900) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
29:20	RW	0x0c3	sw_sharp_bf_sigma_inv_5 Sharp bilateral filter sigma inverse 5 Range: [10, 512]
19:10	RW	0x0a4	sw_sharp_bf_sigma_inv_4 Sharp bilateral filter sigma inverse 4 Range: [10, 512]
9:0	RW	0x0f1	sw_sharp_bf_sigma_inv_3 Sharp bilateral filter sigma inverse 3 Range: [10, 512]

ISP_SHARP_2900_BF_SIGMA_INV_2

Address: Operational Base(0xFF3F2900) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x0f1	sw_sharp_bf_sigma_inv_7 Sharp bilateral filter sigma inverse 7 Range: [10, 512]
9:0	RW	0x0f1	sw_sharp_bf_sigma_inv_6 Sharp bilateral filter sigma inverse 6 Range: [10, 512]

ISP_SHARP_2900_SIGMA_SHIFT

Address: Operational Base(0xFF3F2900) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x7	sw_sharp_bf_sigma_shift Sharp bilateral filter sigma shift bits. Range: [4, 15]
3:0	RW	0x6	sw_sharp_pbf_sigma_shift Sharp pre bilateral filter sigma shift bits. Range: [4, 15]

ISP_SHARP_2900_EHF_TH_0

Address: Operational Base(0xFF3F2900) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x080	sw_sharp_ehf_th_2 Sharp ehf threshold 2
19:10	RW	0x080	sw_sharp_ehf_th_1 Sharp ehf threshold 1
9:0	RW	0x080	sw_sharp_ehf_th_0 Sharp ehf threshold 0

ISP_SHARP_2900_EHF_TH_1

Address: Operational Base(0xFF3F2900) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x080	sw_sharp_ehf_th_5 Sharp ehf threshold 5
19:10	RW	0x080	sw_sharp_ehf_th_4 Sharp ehf threshold 4
9:0	RW	0x080	sw_sharp_ehf_th_3 Sharp ehf threshold 3

ISP_SHARP_2900_EHF_TH_2

Rockchip Confidencial

Address: Operational Base(0xFF3F2900) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x001	sw_sharp_ehf_th_7 Sharp ehf threshold 7
9:0	RW	0x040	sw_sharp_ehf_th_6 Sharp ehf threshold 6

ISP_SHARP_2900_CLIP_HF_0

Address: Operational Base(0xFF3F2900) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x088	sw_sharp_clip_hf_2 Sharp clip of high frequency 2
19:10	RW	0x058	sw_sharp_clip_hf_1 Sharp clip of high frequency 1
9:0	RW	0x040	sw_sharp_clip_hf_0 Sharp clip of high frequency 0

ISP_SHARP_2900_CLIP_HF_1

Address: Operational Base(0xFF3F2900) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0e0	sw_sharp_clip_hf_5 Sharp clip of high frequency 5
19:10	RW	0x0f8	sw_sharp_clip_hf_4 Sharp clip of high frequency 4
9:0	RW	0x0b4	sw_sharp_clip_hf_3 Sharp clip of high frequency 3

ISP_SHARP_2900_CLIP_HF_2

Address: Operational Base(0xFF3F2900) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	sw_sharp_clip_hf_7 Sharp clip of high frequency 7
9:0	RW	0x048	sw_sharp_clip_hf_6 Sharp clip of high frequency 6

ISP_SHARP_2900_PBF_COEF

Address: Operational Base(0xFF3F2900) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x0a	sw_sharp_pbf_coef_2 Sharp pbf coefficient of corner
15	RO	0x0	reserved
14:8	RW	0x10	sw_sharp_pbf_coef_1 Sharp pbf coefficient of up/down/left/right
7	RO	0x0	reserved
6:0	RW	0x18	sw_sharp_pbf_coef_0 Sharp pbf coefficient of center Notes: sw_sharp_pbf_coef_0+4*sw_sharp_pbf_coef_1+4*sw_sharp_pbf_coef_2 must be equal to 128

ISP_SHARP_2900_BF_COEF

Rockchip Confidencial

Address: Operational Base(0xFF3F2900) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x0a	sw_sharp_bf_coef_2 Sharp bf coefficient of corner
15	RO	0x0	reserved
14:8	RW	0x10	sw_sharp_bf_coef_1 Sharp bf coefficient of up/down/left/right
7	RO	0x0	reserved
6:0	RW	0x18	sw_sharp_bf_coef_0 Sharp bf coefficient of center Notes: sw_sharp_bf_coef_0+4*sw_sharp_bf_coef_1+4*sw_sharp_bf_coef_2 must be equal to 128

ISP_SHARP_2900_GAUS_COEF_0

Address: Operational Base(0xFF3F2900) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x06	sw_sharp_gaus_coef_2 Sharp gauss coefficient of corner
15	RO	0x0	reserved
14:8	RW	0x07	sw_sharp_gaus_coef_1 Sharp gauss coefficient of up/down/left/right
7	RO	0x0	reserved
6:0	RW	0x0c	sw_sharp_gaus_coef_0 Sharp gauss coefficient of center Notes: sw_sharp_gaus_coef_0+4*sw_sharp_gaus_coef_1+4*sw_sharp_gaus_coef_2 must be equal to 128

ISP_SHARP_2900_GAUS_COEF_1

Address: Operational Base(0xFF3F2900) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x03	sw_sharp_gaus_coef_5 Sharp gauss coefficient of corner
15	RO	0x0	reserved
14:8	RW	0x04	sw_sharp_gaus_coef_4 Sharp gauss coefficient of up/down/left/right
7	RO	0x0	reserved
6:0	RW	0x05	sw_sharp_gaus_coef_3 Sharp gauss coefficient of center Notes: sw_sharp_gaus_coef_0+4*sw_sharp_gaus_coef_1+4*sw_sharp_gaus_coef_2 must be equal to 128

ISP_SHARP_2900_GAIN

Address: Operational Base(0xFF3F2900) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	sw_sharp_local_gainscale Sharp local gain scale. Range: [0, 1] Fixed-point: [0, 1, 7]
23:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	sw_sharp_global_gain_alpha Sharp global gain alpha. Range: [0, 1] Fixed-point: [0, 1, 3]
15:10	RO	0x00	reserved
9:0	RW	0x010	sw_sharp_global_gain Sharp global gain Range: [0, 63] Fixed-point: [0, 6, 4]

ISP_SHARP_2900_GAIN_ADJUST0

Address: Operational Base(0xFF3F2900) + offset (0x0054)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x2000	sw_sharp_gain_adj1 Sharp gain adjust 1, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]
15	RO	0x0	reserved
14:0	RW	0x4000	sw_sharp_gain_adj0 Sharp gain adjust 0, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]

ISP_SHARP_2900_GAIN_ADJUST1

Address: Operational Base(0xFF3F2900) + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0800	sw_sharp_gain_adj3 Sharp gain adjust 3, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]
15	RO	0x0	reserved
14:0	RW	0x1000	sw_sharp_gain_adj2 Sharp gain adjust 2, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]

ISP_SHARP_2900_GAIN_ADJUST2

Address: Operational Base(0xFF3F2900) + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0400	sw_sharp_gain_adj5 Sharp gain adjust 5, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]
15	RO	0x0	reserved
14:0	RW	0x0550	sw_sharp_gain_adj4 Sharp gain adjust 4, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]

ISP_SHARP_2900_GAIN_ADJUST3

Address: Operational Base(0xFF3F2900) + offset (0x0060)

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Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0400	sw_sharp_gain_adj7 Sharp gain adjust 7, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]
15	RO	0x0	reserved
14:0	RW	0x0400	sw_sharp_gain_adj6 Sharp gain adjust 6, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]

ISP_SHARP_2900_GAIN_ADJUST4

Address: Operational Base(0xFF3F2900) + offset (0x0064)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0400	sw_sharp_gain_adj9 Sharp gain adjust 9, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]
15	RO	0x0	reserved
14:0	RW	0x0400	sw_sharp_gain_adj8 Sharp gain adjust 8, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]

ISP_SHARP_2900_GAIN_ADJUST5

Address: Operational Base(0xFF3F2900) + offset (0x0068)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0100	sw_sharp_gain_adj11 Sharp gain adjust 11, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]
15	RO	0x0	reserved
14:0	RW	0x0200	sw_sharp_gain_adj10 Sharp gain adjust 10, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]

ISP_SHARP_2900_GAIN_ADJUST6

Address: Operational Base(0xFF3F2900) + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0001	sw_sharp_gain_adj13 Sharp gain adjust 13, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]
15	RO	0x0	reserved
14:0	RW	0x0080	sw_sharp_gain_adj12 Sharp gain adjust 12, the maximum is 16384. Range: [0, 32] Fixed-point: [0, 6, 9]

ISP_SHARP_2900_CENTER

Address: Operational Base(0xFF3F2900) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0100	sw_sharp_center_het Vertical center point of picture, need sw_sharp_center_mode = 1, max is 6048/2
15:13	RO	0x0	reserved
12:0	RW	0x0080	sw_sharp_center_wid Horizontal center point of picture, need sw_sharp_center_mode = 1, max is 4672

ISP_SHARP_2900_GAIN_DIS_STRENGTH0

Address: Operational Base(0xFF3F2900) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	sw_sharp_strength3 Sharp gain radius strength 3, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
23:16	RW	0x80	sw_sharp_strength2 Sharp gain radius strength 2, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
15:8	RW	0x80	sw_sharp_strength1 Sharp gain radius strength 1, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
7:0	RW	0x80	sw_sharp_strength0 Sharp gain radius strength 0, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]

ISP_SHARP_2900_GAIN_DIS_STRENGTH1

Address: Operational Base(0xFF3F2900) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	sw_sharp_strength7 Sharp gain radius strength 7, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
23:16	RW	0x80	sw_sharp_strength6 Sharp gain radius strength 6, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
15:8	RW	0x80	sw_sharp_strength5 Sharp gain radius strength 5, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
7:0	RW	0x80	sw_sharp_strength4 Sharp gain radius strength 4, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]

ISP_SHARP_2900_GAIN_DIS_STRENGTH2

Address: Operational Base(0xFF3F2900) + offset (0x007C)

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Bit	Attr	Reset Value	Description
31:24	RW	0x80	sw_sharp_strength11 Sharp gain radius strength 11, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
23:16	RW	0x80	sw_sharp_strength10 Sharp gain radius strength 10, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
15:8	RW	0x80	sw_sharp_strength9 Sharp gain radius strength 9, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
7:0	RW	0x80	sw_sharp_strength8 Sharp gain radius strength 8, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]

ISP_SHARP_2900_GAIN_DIS_STRENGTH3

Address: Operational Base(0xFF3F2900) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	sw_sharp_strength15 Sharp gain radius strength 15, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
23:16	RW	0x01	sw_sharp_strength14 Sharp gain radius strength 14, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
15:8	RW	0x01	sw_sharp_strength13 Sharp gain radius strength 13, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
7:0	RW	0x01	sw_sharp_strength12 Sharp gain radius strength 12, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]

ISP_SHARP_2900_GAIN_DIS_STRENGTH4

Address: Operational Base(0xFF3F2900) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	sw_sharp_strength19 Sharp gain radius strength 19, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
23:16	RW	0x01	sw_sharp_strength18 Sharp gain radius strength 18, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
15:8	RW	0x01	sw_sharp_strength17 Sharp gain radius strength 17, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]

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Bit	Attr	Reset Value	Description
7:0	RW	0x01	sw_sharp_strength16 Sharp gain radius strength 16, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]

ISP_SHARP_2900_GAIN_DIS_STRENGTH5

Address: Operational Base(0xFF3F2900) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x01	sw_sharp_strength21 Sharp gain radius strength 21, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]
7:0	RW	0x01	sw_sharp_strength20 Sharp gain radius strength 20, the maximum is 128. Range: [0, 1] Fixed-point: [0, 1, 7]

ISP_SHARP_2900_CLIP_NEG_0

Address: Operational Base(0xFF3F2900) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_sharp_clip_neg_2 Sharp negative clip of high frequency 2
19:10	RW	0x000	sw_sharp_clip_neg_1 Sharp negative clip of high frequency 1
9:0	RW	0x000	sw_sharp_clip_neg_0 Sharp negative clip of high frequency 0

ISP_SHARP_2900_CLIP_NEG_1

Address: Operational Base(0xFF3F2900) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_sharp_clip_neg_5 Sharp negative clip of high frequency 5
19:10	RW	0x000	sw_sharp_clip_neg_4 Sharp negative clip of high frequency 4
9:0	RW	0x000	sw_sharp_clip_neg_3 Sharp negative clip of high frequency 3

ISP_SHARP_2900_CLIP_NEG_2

Address: Operational Base(0xFF3F2900) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	sw_sharp_clip_neg_7 Sharp negative clip of high frequency 7
9:0	RW	0x000	sw_sharp_clip_neg_6 Sharp negative clip of high frequency 6

2.4.2.20 LDCH

ISP_LDCH_3B00_LDCH_ADR_STS

Address: Operational Base(0xFF3F3B00) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31	RO	0x0	sw_ldch_en_shd LDCH enable signal shadow
30	RO	0x0	ldch_working LDCH working status
29	RO	0x0	ldch_map_data_err LDCH error interrupt signal
28:9	RO	0x00000	reserved
8	RW	0x0	sw_ldch_lut_mode 1'b1: use ldch_en and frm_end to start lut_rd 1'b0: use debayer frm_st to start lut_rd Note: Only valid when sw_ldch_force_map_en is 1.
7	RW	0x0	sw_ldch_map13p3_en 1'b1: Every 16bit in LDCH table consist of 13bit integers and 3bit decimals. 1'b0: Every 16bit in LDCH table consist of 12bit integers and 4bit decimals. Note: Only valid when sw_ldch_force_map_en is 1.
6	RW	0x0	sw_ldch_force_map_en When value is 1, the number of bits used for integer part or decimal part is configured by software. Always set to 0 for 1106.
5	RO	0x0	reserved
4	RW	0x0	sw_bic_mode_en 1'b0: LDCH use bilinear mode. 1'b1: LDCH use bicubic mode.
3	RW	0x0	sw_sample_avr_en 1'b0: Use UV values of the pixel on the left when YUV444->YUV422. 1'b1: Use average of the left and right UV values when YUV444->YUV422.
2	RW	0x0	sw_zero_interp_en 1'b0: The coefficient is equal to 32'h00008000 when index is 0 in bicubic mode. 1'b1: The coefficient is equal to sw_ldch_bic_table0 when index is 0 in bicubic mode.
1	RW	0x0	sw_ldch_frm_end_dis 1'b0: Use last_frm_end to be frm_end 1'b1: Use in_frm_end to be frm_end
0	RW	0x1	sw_ldch_en_i LDCH enable signal

ISP_LDCH_3B00_LDCH_BIC_TABLE0

Address: Operational Base(0xFF3F3B00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table0 LDCH bicubic mode table0

ISP_LDCH_3B00_LDCH_BIC_TABLE1

Address: Operational Base(0xFF3F3B00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table1 LDCH bicubic mode table1

ISP_LDCH_3B00_LDCH_BIC_TABLE2

Address: Operational Base(0xFF3F3B00) + offset (0x000C)

Rockchip Confidential

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table2 LDCH bicubic mode table2

ISP_LDCH_3B00_LDCH_BIC_TABLE3

Address: Operational Base(0xFF3F3B00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table3 LDCH bicubic mode table3

ISP_LDCH_3B00_LDCH_BIC_TABLE4

Address: Operational Base(0xFF3F3B00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table4 LDCH bicubic mode table4

ISP_LDCH_3B00_LDCH_BIC_TABLE5

Address: Operational Base(0xFF3F3B00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table5 LDCH bicubic mode table5

ISP_LDCH_3B00_LDCH_BIC_TABLE6

Address: Operational Base(0xFF3F3B00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table6 LDCH bicubic mode table6

ISP_LDCH_3B00_LDCH_BIC_TABLE7

Address: Operational Base(0xFF3F3B00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table7 LDCH bicubic mode table7

ISP_LDCH_3B00_LDCH_BIC_TABLE8

Address: Operational Base(0xFF3F3B00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table8 LDCH bicubic mode table8

2.4.2.21 GAIN

ISP_GAIN_3F00_CTRL

Address: Operational Base(0xFF3F3F00) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31	RO	0x0	gain_wctrl_working 1'b0: Gain module is not working 1'b1: Gain module is working
30:28	RO	0x0	reserved
27	RW	0x0	sw_gain2ddr_force_ack1 The backdoor for force GAIN to DDR ack to 1.
26:25	RW	0x0	sw_gain2ddr_mode 2'b00: 4x8 mode 2'b01: 2x8 mode 2'b10: 1x8 mode 2'b11: 4x8 mode
24	RW	0x0	sw_gain2ddr_wr_en Global gain to DDR enable bit
23:17	RO	0x0	reserved
16	RW	0x0	sw_dhaz_gain_bypass_en This bit is a backdoor when module open while not use its gain source.
15:13	RO	0x0	reserved
12	RW	0x0	sw_adrc_gain_bypass_en This bit is a backdoor when module open while not use its gain source.
11:10	RO	0x0	reserved
9	RW	0x0	sw_force_lsc_indly Back door for LSC INDLY module always on.
8	RW	0x0	sw_lsc_gain_bypass_en This bit is a backdoor when module open while not use its gain source.
7:6	RO	0x0	reserved
5	RW	0x0	sw_gain_dmard_mode_en In dma read mode, set this bit to 1 will save some power.
4	RW	0x0	sw_bayer3dnr_gain_bypas_en This bit is a backdoor when module open while not use its gain source.
3	RW	0x0	sw_gain_mp_pipe_dis Back door for main path delay module
2	RW	0x0	sw_gain_gate_always_on Back door for gating
1	RW	0x0	sw_mge_gain_bypass_en This bit is a backdoor when module open while not use its gain source.
0	RW	0x0	sw_gain_en GAIN enable bit

ISP_GAIN_3F00_GAIN_G0

Address: Operational Base(0xFF3F3F00) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00040	sw_gain0 HDR merge gain0, [0/64, 262144/64] when sw_mge_gain_en high. Or sw_gain_init (this signal is 12.9, here replace12.6 low 3bit assert to 0)

ISP_GAIN_3F00_GAIN_G1_G2

Address: Operational Base(0xFF3F3F00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0040	sw_gain2 HDR merge gain2, [0/64, 16383/64]
15:14	RO	0x0	reserved
13:0	RW	0x0040	sw_gain1 HDR merge gain1, [0/64, 16383/64]

ISP_GAIN_3F00_FIFO_STATUS

Address: Operational Base(0xFF3F3F00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	W1C	0x0	err_clr For clear error flag
30:16	RO	0x0000	reserved
15:8	RW	0x00	fifo_err_flag Could be cleared by error flag signal
7:6	RO	0x0	reserved
5	RO	0x0	ro_gain_out Gain out frame end
4	RO	0x0	ro_ynrgain_in_fifo_full FIFO full flag
3	RO	0x0	ro_adrc2dhaz_fifo_full FIFO full flag
2	RO	0x0	ro_lsc2adrc_fifo_full FIFO full flag
1	RO	0x0	ro_bay2lsc_fifo_full FIFO full flag
0	RO	0x0	ro_mgegainfifo_full FIFO full flag

2.4.2.22 SELF_RESIZE

SELF_RESIZE_0C00_1000_0E00_CTRL

Address: Operational Base(0xFF3F0C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	sw_scl_in_clip_en Use for 8K 1'b0: Disable scale in clip 1'b1: Enable scale in clip
11	RW	0x0	sw_scl_clip_en Use for 8K 1'b0: Disable scale out clip 1'b1: Enable scale out clip

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Bit	Attr	Reset Value	Description
10	RW	0x0	sw_scl_hphase_en Use for 8K 1'b0: Disable scale phase adjustment 1'b1: Enable scale phase adjustment
9	RW	0x0	auto_upd 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
8	RW	0x0	cfg_upd 1'b0: Nothing happens 1'b1: Update shadow registers read: Always 0
7	RW	0x0	scale_vc_up 1'b1: Vertical chrominance up-scaling selected 1'b0: Vertical chrominance down-scaling selected
6	RW	0x0	scale_vy_up 1'b1: Vertical luminance up-scaling selected 1'b0: Vertical luminance down-scaling selected
5	RW	0x0	scale_hc_up 1'b1: Horizontal chrominance up-scaling selected 1'b0: Horizontal chrominance down-scaling selected
4	RW	0x0	scale_hy_up 1'b1: Horizontal luminance up-scaling selected 1'b0: Horizontal luminance down-scaling selected
3	RW	0x0	scale_vc_enable 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RW	0x0	scale_vy_enable 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RW	0x0	scale_hc_enable 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RW	0x0	scale_hy_enable 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

SELF_RESIZE_0C00_1000_0E00_SCALE_HY

Address: Operational Base(0xFF3F0C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	scale_hy This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor. --- SRSZ_SCALE_HY --- Note: The size of the output picture is calculated as follows: up-scaling: (size_in - 1) / (size_out - 1)) = scale down-scaling: (size_out - 1) / (size_in - 1)) = scale, where size_in/out is the width or height of the in/output picture. The value of the respective SRSZ_SCALE register then has to be int(scale x 2^16) for up-scaling and int(scale x 2^16)+1 for down-scaling. For down-scaling this formula has no restriction. In up-scaling processes the limit is factor 5. If a format conversion is performed, the scale factors have to be different for the luminance and the chrominance component, respectively. For example, for a format conversion from 4:2:2 to 4:2:0 the scale register value for the vertical chrominance component should be half of the vertical luminance scale register value.

SELF_RESIZE_0C00_1000_0E00_SCALE_HCB

Address: Operational Base(0xFF3F0C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	scale_hcb This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor.

SELF_RESIZE_0C00_1000_0E00_SCALE_HCR

Address: Operational Base(0xFF3F0C00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	scale_hcr This register is set to the horizontal Cr downscale factor or to the reciprocal of the horizontal Cr upscale factor.

SELF_RESIZE_0C00_1000_0E00_SCALE_VY

Address: Operational Base(0xFF3F0C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	scale_vy This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor.

SELF_RESIZE_0C00_1000_0E00_SCALE_VC

Address: Operational Base(0xFF3F0C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	scale_vc This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor.

SELF_RESIZE_0C00_1000_0E00_PHASE_HY

Address: Operational Base(0xFF3F0C00) + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phase_hy This register is set to the horizontal luminance phase offset.

SELF_RESIZE_0C00_1000_0E00_PHASE_HC

Address: Operational Base(0xFF3F0C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phase_hc This register is set to the horizontal chrominance phase offset.

SELF_RESIZE_0C00_1000_0E00_PHASE_VY

Address: Operational Base(0xFF3F0C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phase_vy This register is set to the vertical luminance phase offset.

SELF_RESIZE_0C00_1000_0E00_PHASE_VC

Address: Operational Base(0xFF3F0C00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phase_vc This register is set to the vertical chrominance phase offset.

SELF_RESIZE_0C00_1000_0E00_SCALE_LUT_ADDR

Address: Operational Base(0xFF3F0C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	scale_lut_addr Pointer to entry of lookup table

SELF_RESIZE_0C00_1000_0E00_SCALE_LUT

Address: Operational Base(0xFF3F0C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	scale_lut Entry of lookup table at position scale_lut_addr. The lookup table must be filled with appropriate values before the up- scaling functionality can be used.

SELF_RESIZE_0C00_1000_0E00_CTRL_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	scale_vc_up_shd 1'b1: Vertical chrominance up-scaling selected 1'b0: Vertical chrominance down-scaling selected
6	RO	0x0	scale_vy_up_shd 1'b1: Vertical luminance up-scaling selected 1'b0: Vertical luminance down-scaling selected
5	RO	0x0	scale_hc_up_shd 1'b1: Horizontal chrominance up-scaling selected 1'b0: Horizontal chrominance down-scaling selected

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Bit	Attr	Reset Value	Description
4	RO	0x0	scale_hy_up_shd 1'b1: Horizontal luminance up-scaling selected 1'b0: Horizontal luminance down-scaling selected
3	RO	0x0	scale_vc_enable_shd 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RO	0x0	scale_vy_enable_shd 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RO	0x0	scale_hc_enable_shd 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RO	0x0	scale_hy_enable_shd 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

SELF_RESIZE_0C00_1000_0E00_SCALE_HY_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_hy_shd This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor.

SELF_RESIZE_0C00_1000_0E00_SCALE_HCB_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_hcb_shd This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor.

SELF_RESIZE_0C00_1000_0E00_SCALE_HCR_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_hcr_shd This register is set to the horizontal r downscale factor or to the reciprocal of the horizontal r upscale factor.

SELF_RESIZE_0C00_1000_0E00_SCALE_VY_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_vy_shd This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor.

SELF_RESIZE_0C00_1000_0E00_SCALE_VC_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_vc_shd This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor.

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SELF_RESIZE_0C00_1000_0E00_PHASE_HY_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	phase_hy_shd This register is set to the horizontal luminance phase offset.

SELF_RESIZE_0C00_1000_0E00_PHASE_HC_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	phase_hc_shd This register is set to the horizontal chrominance phase offset

SELF_RESIZE_0C00_1000_0E00_PHASE_VY_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	phase_vy_shd This register is set to the vertical luminance phase offset.

SELF_RESIZE_0C00_1000_0E00_PHASE_VC_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	phase_vc_shd This register is set to the vertical chrominance phase offset.

SELF_RESIZE_0C00_1000_0E00_HY_SIZE

Address: Operational Base(0xFF3F0C00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_scl_hy_size Scale out y size, only works when sw_scl_clip_en equal to 1

SELF_RESIZE_0C00_1000_0E00_HC_SIZE

Address: Operational Base(0xFF3F0C00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_scl_hc_size Scale out uv size, only works when sw_scl_clip_en equal to 1

SELF_RESIZE_0C00_1000_0E00_HY_OFFS_MI

Address: Operational Base(0xFF3F0C00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_scl_hy_offs_mi The offset of first Y pix in 128bit, which rang from 0~15.

SELF_RESIZE_0C00_1000_0E00_HC_OFFS_MI

Address: Operational Base(0xFF3F0C00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_scl_hc_offs_mi The offset of first UV pix in 128bit, which rang from 0~15.

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SELF_RESIZE_0C00_1000_0E00_HY_SIZE_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_scl_hy_size_shd Scale out y size shadow signal

SELF_RESIZE_0C00_1000_0E00_HC_SIZE_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_scl_hc_size_shd Scale out uv size, only works when sw_scl_clip_en equal to 1

SELF_RESIZE_0C00_1000_0E00_HY_OFFS_MI_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	sw_scl_hy_offs_mi_shd Shadow signal of sw_scl_hy_offs_mi

SELF_RESIZE_0C00_1000_0E00_HC_OFFS_MI_SHD

Address: Operational Base(0xFF3F0C00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	sw_scl_hc_offs_mi_shd Shadow signal of sw_scl_hy_offs_mi

SELF_RESIZE_0C00_1000_0E00_IN_CROP_OFFSET

Address: Operational Base(0xFF3F0C00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sw_scl_in_hc_offs Scale in uv data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.
3:0	RW	0x0	sw_scl_in_hy_offs Scale in y data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.

2.4.2.23 BILINEAR_SCALE

BILINEAR_SCALE_1000_SCALE_CTRL

Address: Operational Base(0xFF3F1000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_scl_in_clip_en Use for 8K 1'b0: Disable scale in clip 1'b1: Enable scale in clip
13	RW	0x0	sw_scl_clip_en Use for 8K 1'b0: Disable scale out clip 1'b1: Enable scale out clip

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Bit	Attr	Reset Value	Description
12	RW	0x0	sw_scl_hphase_en Use for 8K 1'b0: Disable scale phase adjustment 1'b1: Enable scale phase adjustment
11:10	RO	0x0	reserved
9	RW	0x0	sw_avg_scale_v_en 1'b1: Enable vertical average scaling 1'b0: Default vertical bilinear scaling
8	RW	0x0	sw_avg_scale_h_en 1'b1: Enable horizontal average scaling 1'b0: Default horizontal bilinear scaling
7:4	RO	0x0	reserved
3	RW	0x0	sw_scale_vc_en 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RW	0x0	sw_scale_vy_en 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RW	0x0	sw_scale_hc_en 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RW	0x0	sw_scale_hy_en 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

BILINEAR_SCALE_1000_SCALE_UPDATE

Address: Operational Base(0xFF3F1000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	sys_cfg_gen_upd 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
8	WO	0x0	sys_cfg_force_upd 1'b0: Nothing happens 1'b1: Update shadow registers
7:0	RO	0x00	reserved

BILINEAR_SCALE_1000_SCALE_SRC_SIZE

Address: Operational Base(0xFF3F1000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_scale_src_height Scale height of source (input)
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_scale_src_width Scale width of source (input)

BILINEAR_SCALE_1000_SCALE_DST_SIZE

Address: Operational Base(0xFF3F1000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_scale_dst_height Scale height of destination (output)
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_scale_dst_width Scale width of destination (output)

BILINEAR_SCALE_1000_SCALE_HY_FAC

Address: Operational Base(0xFF3F1000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_hy_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (width_in - 1) / (width_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12). Average: (width_out - 1) / (width_in - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^16) + 1.

BILINEAR_SCALE_1000_SCALE_HC_FAC

Address: Operational Base(0xFF3F1000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_scale_hc_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: ((width_in / 2) - 1) / ((width_out / 2) - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12). Average: ((width_out / 2) - 1) / ((width_in / 2) - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^16) + 1.

BILINEAR_SCALE_1000_SCALE_VY_FAC

Address: Operational Base(0xFF3F1000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_vy_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (height_in - 1) / (height_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12). Average: (height_out - 1) / (height_in - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^16) + 1.

BILINEAR_SCALE_1000_SCALE_VC_FAC

Address: Operational Base(0xFF3F1000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:0	RW	0x00000	sw_scale_vc_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (height_in - 1) / (height_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12). Average: (height_out - 1) / (height_in - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^16) + 1.

BILINEAR_SCALE_1000_SCALE_HY_OFFS

Address: Operational Base(0xFF3F1000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_hy_offs This register is set to the horizontal luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_HC_OFFS

Address: Operational Base(0xFF3F1000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_hc_offs This register is set to the horizontal chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_PHASE_HY

Address: Operational Base(0xFF3F1000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_scale_phase_hy This register is set to the horizontal luminance phase offset for average.

BILINEAR_SCALE_1000_SCALE_PHASE_HC

Address: Operational Base(0xFF3F1000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_phase_hc This register is set to the horizontal chrominance phase offset for average.

BILINEAR_SCALE_1000_SCALE_PHASE_VY

Address: Operational Base(0xFF3F1000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_phase_vy This register is set to the vertical luminance phase offset for average.

BILINEAR_SCALE_1000_SCALE_PHASE_VC

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Address: Operational Base(0xFF3F1000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_phase_vc This register is set to the vertical chrominance phase offset for average.

BILINEAR_SCALE_1000_SCALE_HY_SIZE

Address: Operational Base(0xFF3F1000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_scl_hy_size Scale out Y size, only works when sw_scl_clip_en equal to 1.

BILINEAR_SCALE_1000_SCALE_HC_SIZE

Address: Operational Base(0xFF3F1000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_scl_hc_size Scale out UV size, only works when sw_scl_clip_en equal to 1.

BILINEAR_SCALE_1000_SCALE_HY_OFFS_MI

Address: Operational Base(0xFF3F1000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_scl_hy_offs_mi The offset of first Y pixel in 128bit, which range from 0~15.

BILINEAR_SCALE_1000_SCALE_HC_OFFS_MI

Address: Operational Base(0xFF3F1000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_scl_hc_offs_mi The offset of first UV pixel in 128bit, which range from 0~15.

BILINEAR_SCALE_1000_SCALE_IN_CROP_OFFSET

Address: Operational Base(0xFF3F1000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sw_scl_in_hc_offs Scale in UV data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.
3:0	RW	0x0	sw_scl_in_hy_offs Scale in Y data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.

BILINEAR_SCALE_1000_SCALE_CTRL_SHD

Address: Operational Base(0xFF3F1000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_scl_in_clip_en_shd Use for 8K 1'b0: Disable scale in clip 1'b1: Enable scale in clip

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Bit	Attr	Reset Value	Description
13	RW	0x0	sw_scl_clip_en_shd Use for 8K 1'b0: Disable scale out clip 1'b1: Enable scale out clip
12	RW	0x0	sw_scl_hphase_en_shd Use for 8K 1'b0: Disable scale phase adjustment 1'b1: Enable scale phase adjustment
11:10	RO	0x0	reserved
9	RW	0x0	sw_avg_scale_v_en_shd 1'b1: Enable vertical average scaling 1'b0: Default vertical bilinear scaling
8	RW	0x0	sw_avg_scale_h_en_shd 1'b1: Enable horizontal average scaling 1'b0: Default horizontal bilinear scaling
7:4	RO	0x0	reserved
3	RW	0x0	sw_scale_vc_en_shd 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RW	0x0	sw_scale_vy_en_shd 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RW	0x0	sw_scale_hc_en_shd 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RW	0x0	sw_scale_hy_en_shd 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

BILINEAR_SCALE_1000_SCALE_SRC_SIZE_SHD

Address: Operational Base(0xFF3F1000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_scale_src_height_shd Scale height of source (input)
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_scale_src_width_shd Scale width of source (input)

BILINEAR_SCALE_1000_SCALE_DST_SIZE_SHD

Address: Operational Base(0xFF3F1000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_scale_dst_height_shd Scale height of destination(output)
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_scale_dst_width_shd Scale width of destination (output)

BILINEAR_SCALE_1000_SCALE_HY_FAC_SHD

Address: Operational Base(0xFF3F1000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:0	RW	0x00000	sw_scale_hy_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (width_in - 1) / (width_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12). Average: (width_out - 1) / (width_in - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^16) + 1.

BILINEAR_SCALE_1000_SCALE_HC_FAC_SHD

Address: Operational Base(0xFF3F1000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_scale_hc_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: ((width_in / 2) - 1) / ((width_out / 2) - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12). Average: ((width_out / 2) - 1) / ((width_in / 2) - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^16) + 1.

BILINEAR_SCALE_1000_SCALE_VY_FAC_SHD

Address: Operational Base(0xFF3F1000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_vy_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (height_in - 1) / (height_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12). Average: (height_out - 1) / (height_in - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^16) + 1.

BILINEAR_SCALE_1000_SCALE_VC_FAC_SHD

Address: Operational Base(0xFF3F1000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:0	RW	0x00000	sw_scale_vc_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (height_in - 1) / (height_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12). Average: (height_out - 1) / (height_in - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^16) + 1.

BILINEAR_SCALE_1000_SCALE_HY_OFFS_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_hy_offs_shd This register is set to the horizontal luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_HC_OFFS_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_hc_offs_shd This register is set to the horizontal chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_PHASE_HY_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	sw_phase_hy_shd This register is set to the horizontal luminance phase offset.

BILINEAR_SCALE_1000_SCALE_PHASE_HC_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	sw_phase_hc_shd This register is set to the horizontal chrominance phase offset.

BILINEAR_SCALE_1000_SCALE_PHASE_VY_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	sw_phase_vy_shd This register is set to the vertical luminance phase offset.

BILINEAR_SCALE_1000_SCALE_PHASE_VC_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	sw_phase_vc_shd This register is set to the vertical chrominance phase offset.

BILINEAR_SCALE_1000_SCALE_HY_SIZE_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_scl_hy_size_shd Scale out Y size shadow signal

BILINEAR_SCALE_1000_SCALE_HC_SIZE_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_scl_hc_size_shd Scale out UV size, only works when sw_scl_clip_en equal to 1.

BILINEAR_SCALE_1000_SCALE_HY_OFFS_MI_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	sw_scl_hy_offs_mi_shd Shadow signal of sw_scl_hy_offs_mi

BILINEAR_SCALE_1000_SCALE_HC_OFFS_MI_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	sw_scl_hc_offs_mi_shd Shadow signal of sw_scl_hy_offs_mi

BILINEAR_SCALE_1000_SCALE_IN_CROP_OFFSET_SHD

Address: Operational Base(0xFF3F1000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sw_scl_in_hc_offs_shd Scale in UV data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.
3:0	RW	0x0	sw_scl_in_hy_offs_shd Scale in Y data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.

2.4.2.24 DUAL_CROP

DUAL_CROP_0880_CTRL

Address: Operational Base(0xFF3F0880) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	in_upd_dis Input frame end update shadow registers disable 1'b0: update shadow with input frame end 1'b1: update shadow with output frame end Note: Since the input size is larger than the output size, the shadow registers should be updated with the input frame end.
30:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28	RO	0x0	regs_fbc_mode_shd regs_fbc_mode_shd Note: Shadow will only take effect when in_upd_dis is 0.
27:26	RO	0x0	regs_sp_mode_shd regs_sp_mode_shd Note: Shadow will only take effect when in_upd_dis is 0.
25:24	RO	0x0	regs_mp_mode_shd regs_mp_mode_shd Note: Shadow will only take effect when in_upd_dis is 0.
23:9	RO	0x0000	reserved
8	RW	0x0	regs_fbc_mode Fbc clipping enable signal
7	RO	0x0	reserved
6	RW	0x0	regs_gen_cfg_upd 1'b1: Generate frame synchronous configuration signal at the output of ISP for shadow registers of the following processing modules, write only
5	WO	0x0	regs_cfg_upd 1'b1: Immediately configure (update) shadow registers, write onlyd
4	WO	0x0	regs_gen_cfg_upd_fix 1'b1: Permanent configure (update) shadow registers on frame end
3:2	RW	0x0	regs_sp_mode regs_sp_mode 2'b00: Bypass mode 2'b01: Yuv mode 2'b10: Rgb bayer mode 2'b11: Data mode
1:0	RW	0x0	regs_mp_mode regs_mp_mode 2'b00: Bypass mode 2'b01: Yuv mode 2'b10: Rgb bayer mode 2'b11: Data mode

DUAL_CROP_0880_M_H_OFFS

Address: Operational Base(0xFF3F0880) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	m_h_offs MP path h offset

DUAL_CROP_0880_M_V_OFFS

Address: Operational Base(0xFF3F0880) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	m_v_offs MP path v offset

DUAL_CROP_0880_M_H_SIZE

Address: Operational Base(0xFF3F0880) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0080	m_h_size MP path h size

DUAL_CROP_0880_M_V_SIZE

Address: Operational Base(0xFF3F0880) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0c00	m_v_size MP path v size

DUAL_CROP_0880_S_H_OFFS

Address: Operational Base(0xFF3F0880) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	s_h_offs SP path h offset

DUAL_CROP_0880_S_V_OFFS

Address: Operational Base(0xFF3F0880) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	s_v_offs SP path v offset

DUAL_CROP_0880_S_H_SIZE

Address: Operational Base(0xFF3F0880) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	s_h_size SP path h size

DUAL_CROP_0880_S_V_SIZE

Address: Operational Base(0xFF3F0880) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0c00	s_v_size SP path v size

DUAL_CROP_0880_M_H_OFFS_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	m_h_offs_shd MP path h offset shadow signal

DUAL_CROP_0880_M_V_OFFS_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	m_v_offs_shd MP path v offset shadow signal

DUAL_CROP_0880_M_H_SIZE_SHD

Address: Operational Base(0xFF3F0880) + offset (0x002C)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	m_h_size_shd MP path h size shadow signal

DUAL_CROP_0880_M_V_SIZE_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	m_v_size_shd MP path v size shadow signal

DUAL_CROP_0880_S_H_OFFS_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	s_h_offs_shd SP path h offset shadow signal

DUAL_CROP_0880_S_V_OFFS_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	s_v_offs_shd SP path v offset shadow signal

DUAL_CROP_0880_S_H_SIZE_SHD

Address: Operational Base(0xFF3F0880) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	s_h_size_shd SP path h size shadow signal

DUAL_CROP_0880_S_V_SIZE_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RC	0x0080	s_v_size_shd SP path v size shadow signal

DUAL_CROP_0880_FBC_H_OFFS

Address: Operational Base(0xFF3F0880) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	fbc_h_offs FBC path h offset

DUAL_CROP_0880_FBC_V_OFFS

Address: Operational Base(0xFF3F0880) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	fbc_v_offs FBC path v offset

DUAL_CROP_0880_FBC_H_SIZE

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Address: Operational Base(0xFF3F0880) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	fbc_h_size FBC path h size

DUAL_CROP_0880_FBC_V_SIZE

Address: Operational Base(0xFF3F0880) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	fbc_v_size FBC path v size

DUAL_CROP_0880_FBC_H_OFFS_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	fbc_h_offs_shd FBC path h offset shadow signal

DUAL_CROP_0880_FBC_V_OFF_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	fbc_v_offs_shd FBC path v offset shadow signal

DUAL_CROP_0880_FBC_H_SIZE_SHD

Address: Operational Base(0xFF3F0880) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	fbc_h_size_shd FBC path h size shadow signal

DUAL_CROP_0880_FBC_V_SIZE_SHD

Address: Operational Base(0xFF3F0880) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	fbc_v_size_shd FBC path v size shadow signal

2.4.2.25 FLASH

ISP_FLASH_0660_CMD

Address: Operational Base(0xFF3F0660) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	preflash_on Preflash on 1'b0: No effect 1'b1: Flash delay counter is started at next trigger event No capture event is signaled to the sensor interface block.

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Bit	Attr	Reset Value	Description
1	WO	0x0	flash_on Flash on 1'b0: No effect 1'b1: Flash delay counter is started at next trigger event A capture event is signaled to the sensor interface block.
0	WO	0x0	prelight_on Prelight on 1'b0: Prelight is switched off at next trigger event 1'b1: Prelight is switched on at next trigger event --- ISP_FLASH_CMD --- Note: This is the command register for flash light and prelight activation. If the "rw" bits (e.g. "fl_cap_del") are re-programmed during operation, the following scheme shall be applied: i) Prelight is active (prelight_on = 1 has been set before): Every write access to this register shall use prelight_on = 1 (to prevent undesired switch off of the prelight). ii) Prelight is off: Every write access to this register shall use prelight_on = 0 (to prevent undesired switch on of the prelight).

ISP_FLASH_0660_CONFIG

Address: Operational Base(0xFF3F0660) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	fl_cap_del Capture delay Frame number (0 to 15) to be captured after trigger event
3	RW	0x0	fl_trig_src Trigger source for flash and prelight 1'b0: Use vds_vsync for trigger event (with evaluation of vs_in_edge) 1'b1: Use fl_trig for trigger event (positive edge)
2	RW	0x0	fl_pol Polarity of flash related signals 1'b0: flash_trig, prelight_trig are high active 1'b1: flash_trig, prelight_trig are low active
1	RW	0x0	vs_in_edge VSYNC edge 1'b0: Use negative edge of "vds_vsync" if generating a trigger event 1'b1: Use positive edge of "vds_vsync" if generating a trigger event
0	RW	0x0	prelight_mode Prelight mode 1'b0: Prelight is switched off at begin of flash 1'b1: Prelight is switched off at end of flash

ISP_FLASH_0660_PREDIV

Address: Operational Base(0xFF3F0660) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	fl_pre_div Pre-divider for flush/preflash counter

ISP_FLASH_0660_DELAY

Address: Operational Base(0xFF3F0660) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	fl_delay Counter value for flash/preflash delay open_delay = (fl_delay + 1) * (fl_pre_div+1) / clk_isp fl_delay = (open_delay * clk_isp) / (fl_pre_div+1) - 1 --- ISP_FLASH_DELAY --- Note: Example: fl_delay = (10s * 100MHz) / (1023 + 1) C 1 = 976561

ISP_FLASH_0660_TIME

Address: Operational Base(0xFF3F0660) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	fl_time Counter value for flash/preflash time open_time = (fl_time + 1) * (fl_pre_div+1) / clk_isp fl_time = (open_time * clk_isp) / (fl_pre_div+1) - 1 --- ISP_FLASH_TIME --- Note: Example: fl_time = (500ms * 100MHz) / (700 + 1) C 1 = 71530

ISP_FLASH_0660_MAXP

Address: Operational Base(0xFF3F0660) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	fl_maxp Maximum period value for flash or preflash max. flash/preflash period = 214 * (fl_maxp + 1) / clk_isp fl_maxp = (max_period * clk_isp) / 214 - 1 --- ISP_FLASH_MAXP --- Note: Example: fl_maxp = (10s * 100MHz) / (16384) C 1 = 61034

2.4.2.26 SHUTTER

ISP_SHUTTER_0680_CTRL

Address: Operational Base(0xFF3F0680) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sh_open_pol Shutter_open polarity 1'b0: Shutter_open is high active 1'b1: Shutter_open is low active
3	RW	0x0	sh_trig_en Mechanical shutter trigger edge 1'b0: Use negative edge of trigger signal 1'b1: Use positive edge of trigger signal
2	RW	0x0	sh_trig_src Mechanical shutter trigger source 1'b0: Use "vds_vsync" for trigger event 1'b1: Use "shutter_trig" for trigger event

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Bit	Attr	Reset Value	Description
1	RW	0x0	sh_rep_en Mechanical shutter repetition enable 1'b0: Shutter is opened only once 1'b1: Shutter is opened with the repetition rate of the trigger signal
0	RW	0x0	sh_en Mechanical shutter enable 1'b0: Mechanical shutter function is disabled 1'b1: Mechanical shutter function is enabled

ISP_SHUTTER_0680_PREDIV

Address: Operational Base(0xFF3F0680) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	sh_pre_div Pre-divider for mechanical shutter open_delay and open_time counter

ISP_SHUTTER_0680_DELAY

Address: Operational Base(0xFF3F0680) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sh_delay Shutter counter value for delay open_delay = (sh_delay + 1) * (fl_pre_div+1) / clk_isp sh_delay = (open_delay * clk_isp) / (sh_pre_div+1) C 1 --- ISP_SH_DELAY --- Note: Example: sh_delay = (250us * 100MHz) / (50 + 1) C 1 = 489

ISP_SHUTTER_0680_TIME

Address: Operational Base(0xFF3F0680) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sh_time Shutter counter value for time open_time = (sh_time + 1) * (fl_pre_div+1) / clk_isp sh_time = (open_time * clk_isp) / (sh_pre_div+1) - 1 --- ISP_SH_TIME --- Note: Example: sh_time = (10s * 100MHz) / (1023 + 1) C 1 = 976561

2.4.2.27 RAWAF

ISP_RAWAF_4D00_CTRL

Address: Operational Base(0xFF3F4D00) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawaf_meas_flag When rawaf measurement is over, this bit will be pulled up by hardware itself, then software could read the result of rawaf. When read is over, it must been pulled down by software, and rawaf will work again at the beginning of next frame after pulled down.
30	RO	0x0	reserved
29	RW	0x0	sw_rawaf_ae_sel 1'b0: RAWAF reuse RAWAEBIG 1'b1: RAWAF reuse RAWAELITE0
28	W1C	0x0	sys_3a_itself_force_update_p Just a back door
27	RW	0x0	sw_rawaf_v2_acc_mode 1'b0: Sum all 1'b1: Sum max(tileline) It has been deleted in isp-lite version.
26	RW	0x0	sw_rawaf_v1_acc_mode 1'b0: Sum all 1'b1: Sum max(tileline)
25	RW	0x0	sw_rawaf_h2_acc_mode 1'b0: Sum all 1'b1: Sum max(tileline) It has been deleted in isp-lite version.
24	RW	0x0	sw_rawaf_h1_acc_mode 1'b0: Sum all 1'b1: Sum max(tileline)
23	RW	0x1	sw_rawaf_avg_ds_mode 1'b0: 8x8 down scale mode 1'b1: 16x16 down scale mode
22	RW	0x1	sw_rawaf_avg_ds_en RAWAF average down scale enable bit
21	RW	0x0	sw_rawaf_hiir_left_border_mode 1'b0: HIIR left border use above line right border out 1'b1: HIIR left border use cur line pixel
20	RW	0x0	sw_rawaf_ae_config_use 1'b0: AE use RAWAF configure 1'b1: AE use Itself configure
19	RW	0x0	sw_rawaf_from_ynr RAWAF input data come from YNR
18	RW	0x0	sw_rawaf_from_awb RAWAF input data come from RAWAWB

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17:16	RW	0x1	sw_rawaf_v_dnscl_mode V direction downscale mode 2'b00: V direction downscale disable 2'b01: V direction each two lines drop one line 2'b10: V direction each four lines drop three line and H direction do 1/2 average downsample 2'b11: V direction down scale disable
15	RW	0x0	sw_rawaf_sobel_sel SOBEL input select (just a back door). 1'b0: Data from viir out 1'b1: Data from gamma out
14	RW	0x0	sw_rawaf_vldg_sel V direction LDG input luma select. 1'b1: Data from gamma out 1'b0: Data from gauss out
13	RW	0x0	sw_rawaf_y_mode RAWAF cal data is Y (based input 5 RAW lines to 3 Y lines).
12	RW	0x0	sw_rawaf_ae_mode RAWAF will use RAWAE_BIG to get 15x15 AE data.
11	RW	0x0	sw_rawaf_v2_fv_outmode 1'b0: Square mode 1'b1: Absolute mode It has been deleted in isp-lite version.
10	RW	0x0	sw_rawaf_v1_fv_outmode 1'b0: Square mode 1'b1: Absolute mode
9	RW	0x0	sw_rawaf_h2_fv_outmode 1'b0: Square mode 1'b1: Absolute mode It has been deleted in isp-lite version.
8	RW	0x0	sw_rawaf_h1_fv_outmode 1'b0: Square mode 1'b1: Absolute mode
7	RW	0x1	sw_rawaf_ldg_en LDG enable bit
6	RW	0x0	sw_rawaf_accu_use_8bit_mode If this signal set 1, luma lumb suma sumb accumulate will use old 8bit version.
5	RW	0x1	sw_rawaf_viir_en Viir enable bit
4	RW	0x1	sw_rawaf_hiir_en Hiir enable bit
3	RW	0x0	sw_rawaf_v1_fir_sel 1'b0: Select sobel output 1'b1: Select v1fir output

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2	RW	0x1	sw_gaus_en Gaus module enable bit
1	RW	0x1	sw_gamma_en Gamma module enable bit
0	RW	0x0	sw_rawaf_en AF measurement enable. Writing a 1 to this register starts a new measurement and resets the afm_fin (measurement finished) interrupt to 0.

ISP_RAWAF_4D00_OFFSET_WINA

Address: Operational Base(0xFF3F4D00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0003	sw_a_h_l First pixel of window A (horizontal left row), value must be greater or equal 2.
15:13	RO	0x0	reserved
12:0	RW	0x0003	sw_a_v_t First line of window A (vertical top line), value must be greater or equal 1.

ISP_RAWAF_4D00_SIZE_WINA

Address: Operational Base(0xFF3F4D00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_a_h_size Horizontal size of window A, value must be lower than (width of picture - 2 -- a_h_l). This value must be an integer multiple of 15.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_a_v_size Vertical size of window A, value must be lower than (number of lines -2 -- a_v_t). This value must be an integer multiple of 15.

ISP_RAWAF_4D00_OFFSET_WINB

Address: Operational Base(0xFF3F4D00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_b_h_l First pixel of window B (horizontal left row), value must be greater or equal 2
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_b_v_t First line of window B (vertical top line), value must be greater or equal 1

ISP_RAWAF_4D00_SIZE_WINB

Address: Operational Base(0xFF3F4D00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_b_h_size Horizontal size of window A, value must be lower than (width of picture - 2 -- a_h_l)
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_b_v_size Vertical size of window A, value must be lower than (number of lines - 2 -- a_v_t)

ISP_RAWAF_4D00_INT_LINE

Address: Operational Base(0xFF3F4D00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_int_line4_en Int line4 is valid to produce an interrupt signal at the end of the line4 number is measured. 1'b0: AF line4 interrupt is disabled 1'b1: AF line4 interrupt is enabled
30	RW	0x0	sw_int_line3_en Int line3 is valid to produce an interrupt signal at the end of the line3 number is measured. 1'b0: AF line3 interrupt is disabled 1'b1: AF line3 interrupt is enabled
29	RW	0x0	sw_int_line2_en Int line2 is valid to produce an interrupt signal at the end of the line2 number is measured. 1'b0: AF line2 interrupt is disabled 1'b1: AF line2 interrupt is enabled
28	RW	0x0	sw_int_line1_en Int line1 is valid to produce an interrupt signal at the end of the line1 number is measured. 1'b0: AF line1 interrupt is disabled 1'b1: AF line1 interrupt is enabled
27	RW	0x0	sw_int_line0_en Int line0 is valid to produce an interrupt signal at the end of the line0 number is measured. 1'b0: AF line0 interrupt is disabled 1'b1: AF line0 interrupt is enabled
26:20	RO	0x00	reserved
19:16	RW	0xf	sw_int_line4 Fifth line number which need to produce int signal, range from 1 to 15, line4 need to be > line3, the interrupt will be produced at the at of ine_line4 - 1
15:12	RW	0xc	sw_int_line3 Fourth line number which need to produce int signal, range from 1 to 15, line3 need to be > line2, the interrupt will be produced at the at of ine_line3 - 1
11:8	RW	0x9	sw_int_line2 Third line number which need to produce int signal, range from 1 to 15, line2 need to be > line1, the interrupt will be produced at the at of ine_line2 - 1
7:4	RW	0x6	sw_int_line1 Second line number which need to produce int signal, range from 1 to 15, line1 need to be > line0, the interrupt will be produced at the at of ine_line1 - 1
3:0	RW	0x3	sw_int_line0 First line number which need to produce interrupt signal, range from 1 to 15, the interrupt will be produced at the at of ine_line0 - 1

ISP_RAWAF_4D00_CTRL1

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Address: Operational Base(0xFF3F4D00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x0	sw_rawaf_hldg_dilate_num 0 means not do HLDG dilate N means do (N+1) left direction dilate
15:13	RO	0x0	reserved
12	RW	0x0	sw_rawaf_bls_en RAWAF BLS enablt bit.
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawaf_bls_offset Function: in_data - sw_rawaf_bls_offset Note: this signal is signed 1bit signed + 8bit interger

ISP_RAWAF_4D00_THRES

Address: Operational Base(0xFF3F4D00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_ram_star_addr If ine_line0_en is 1, it need to be small than value of (ine_line0 - 1) * 15; Else if ine_line1_en is 1, it need to be small than value of (ine_line1 - 1) * 15, and so on
15:0	RW	0x0000	sw_afm_thres AF measurement threshold. This register defines a threshold which can be used for minimizing the influence of noise in the measurement result

ISP_RAWAF_4D00_VAR_SHIFT

Address: Operational Base(0xFF3F4D00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	sw_lum_var_shift_b Variable shift for luminance summation
19	RO	0x0	reserved
18:16	RW	0x0	sw_lum_var_shift_a Variable shift for luminance summation. The lum_var_shift defines the number of bits for the shift operation of the value of the current pixel before summation. The shift operation is used to avoid a luminance sum overflow
15:12	RO	0x0	reserved
11:8	RW	0x0	sw_rawaf_tnrin_shift Variable shift for TNR input data. RAWAF_IN_TMP = (TNR_IN >>(sw_rawaf_tnrin_shift)). RAWAF_IN_REAL = RAWAF_IN_TMP >> 2. Note: in no HDR mode, valid 12bit data of TNR_IN is TNR_IN[11:0].
7	RO	0x0	reserved
6:4	RW	0x0	sw_afm_var_shift_b Variable shift for AF measurement
3	RO	0x0	reserved
2:0	RW	0x0	sw_afm_var_shift_a Variable shift for AF measurement. The afm_var_shift defines the number of bits for the shift operation at the end of the calculation chain. The shift operation is used to avoid an AF measurement sum overflow

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ISP_RAWAF_4D00_HVIIR_VAR_SHIFT

Address: Operational Base(0xFF3F4D00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x0	sw_rawaf_v2iir_var_shift Variable shift for RAWAF v1iir channel It has been deleted in isp-lite version.
11	RO	0x0	reserved
10:8	RW	0x0	sw_rawaf_v1iir_var_shift Variable shift for RAWAF v1iir channel
7	RO	0x0	reserved
6:4	RW	0x0	sw_rawaf_h2iir_var_shift Variable shift for RAWAF h2iir channel It has been deleted in isp-lite version.
3	RO	0x0	reserved
2:0	RW	0x0	sw_rawaf_h1iir_var_shift Variable shift for RAWAF h1iir channel

ISP_RAWAF_4D00_SUM_B

Address: Operational Base(0xFF3F4D00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_afm_sum_b Sharpness value of window B

ISP_RAWAF_4D00_LUM_B

Address: Operational Base(0xFF3F4D00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	ro_afm_lum_b Luminance value of window B

ISP_RAWAF_4D00_GAMMA_Y0

Address: Operational Base(0xFF3F4D00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x02d	sw_y1 y1 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_y0 y0 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y1

Address: Operational Base(0xFF3F4D00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x0b3	sw_y3 y3 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x06c	sw_y2 y2 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y2

Address: Operational Base(0xFF3F4D00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x158	sw_y5 y5 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x0f5	sw_y4 y4 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y3

Address: Operational Base(0xFF3F4D00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x1cb	sw_y7 y7 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x199	sw_y6 y6 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y4

Address: Operational Base(0xFF3F4D00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x237	sw_y9 y9 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x1f4	sw_y8 y8 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y5

Address: Operational Base(0xFF3F4D00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x2a4	sw_y11 y11 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x26e	sw_y10 y10 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y6

Address: Operational Base(0xFF3F4D00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x341	sw_y13 y13 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x2f7	sw_y12 y12 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y7

Address: Operational Base(0xFF3F4D00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3c2	sw_y15 y15 value of gamma table
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x380	sw_y14 y14 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y8

Address: Operational Base(0xFF3F4D00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x3ff	sw_y16 y16 value of gamma table

ISP_RAWAF_4D00_INT_STATE

Address: Operational Base(0xFF3F4D00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	overflow_h2_sum Overflow flag for H2 sum. When sw_rawaf_meas_flag is pull down, this state can also be pull down
11	RO	0x0	overflow_h1_sum Overflow flag for H1 sum. When sw_rawaf_meas_flag is pull down, this state can also be pull down
10	RO	0x0	overflow_v2_sum Overflow flag for V2 sum. When sw_rawaf_meas_flag is pull down, this state can also be pull down
9	RO	0x0	overflow_v1_sum Overflow flag for V1 sum. When sw_rawaf_meas_flag is pull down, this state can also be pull down
8	RO	0x0	overflow_afm_sum_b Overflow flag for AFM sum b. When sw_rawaf_meas_flag is pull down, this state can also be pull down
7:5	RO	0x0	reserved
4	RO	0x0	int_line4_state When int_line4_en is 1 and at the end of line4 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must be pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down
3	RO	0x0	int_line3_state When int_line3_en is 1 and at the end of line3 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must be pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down
2	RO	0x0	int_line2_state When int_line2_en is 1 and at the end of line2 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must be pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down

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Bit	Attr	Reset Value	Description
1	RO	0x0	int_line1_state When int_line1_en is 1 and at the end of line1 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum . When read is over, it must be pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down
0	WO	0x0	int_line0_state When int_line0_en is 1 and at the end of line0 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must be pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down

ISP_RAWAF_4D00_HIIR_THRESH

Address: Operational Base(0xFF3F4D00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x020	sw_rawaf_v_fv_thresh This register defines a threshold which can be used for minimizing the influence of noise in the measurement result
15:12	RO	0x0	reserved
11:0	RW	0x020	sw_rawaf_h_fv_thresh This register defines a threshold which can be used for minimizing the influence of noise in the measurement result

ISP_RAWAF_4D00_H1_IIR1_COE01

Address: Operational Base(0xFF3F4D00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x2bb	sw_rawaf_h1iir1_coe1 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_h1iir1_coe0 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H1_IIR1_COE23

Address: Operational Base(0xFF3F4D00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x03f	sw_rawaf_h1iir1_coe3 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0xf19	sw_rawaf_h1iir1_coe2 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H1_IIR1_COE45

Address: Operational Base(0xFF3F4D00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xeb1	sw_rawaf_h1iir1_coe5 HIIR related coefficient ({1s,2i,9f})

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_h1iir1_coe4 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H_CURVEL

Address: Operational Base(0xFF3F4D00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0506	sw_rawaf_h_ldg_gslp0 LDG curve luma low slope({5i,8f})
15:8	RW	0x1c	sw_rawaf_h_ldg_gain0 LDG curve luma low minimum gain({8f})
7:0	RW	0x40	sw_rawaf_h_ldg_lumth0 LDG curve luma low threshold ({8f})

ISP_RAWAF_4D00_H1_IIR2_COE01

Address: Operational Base(0xFF3F4D00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x1bf	sw_rawaf_h1iir2_coe1 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_h1iir2_coe0 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H1_IIR2_COE23

Address: Operational Base(0xFF3F4D00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ac	sw_rawaf_h1iir2_coe3 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0xe7e	sw_rawaf_h1iir2_coe2 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H1_IIR2_COE45

Address: Operational Base(0xFF3F4D00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfc1	sw_rawaf_h1iir2_coe5 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_h1iir2_coe4 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H_CURVEH

Address: Operational Base(0xFF3F4D00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0578	sw_rawaf_h_ldg_gslp1 LDG curve luma high slope({5i,8f})
15:8	RW	0x08	sw_rawaf_h_ldg_gain1 LDG curve luma high minimum gain({8f})

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Bit	Attr	Reset Value	Description
7:0	RW	0xb9	sw_rawaf_h_ldg_lumth1 LDG curve luma high threshold ({8f})

ISP_RAWAF_4D00_H2_IIR1_COE01

Address: Operational Base(0xFF3F4D00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x272	sw_rawaf_h2iir1_coe1 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_h2iir1_coe0 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.

ISP_RAWAF_4D00_H2_IIR1_COE23

Address: Operational Base(0xFF3F4D00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x067	sw_rawaf_h2iir1_coe3 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0xecb	sw_rawaf_h2iir1_coe2 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.

ISP_RAWAF_4D00_H2_IIR1_COE45

Address: Operational Base(0xFF3F4D00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xf99	sw_rawaf_h2iir1_coe5 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_h2iir1_coe4 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.

ISP_RAWAF_4D00_V_CURVEL

Address: Operational Base(0xFF3F4D00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0506	sw_rawaf_v_ldg_gslp0 LDG curve luma low slope({5i,8f})
15:8	RW	0x1c	sw_rawaf_v_ldg_gain0 LDG curve luma low minimum gain({8f})
7:0	RW	0x40	sw_rawaf_v_ldg_lumth0 LDG curve luma low threshold ({8f})

ISP_RAWAF_4D00_H2_IIR2_COE01

Address: Operational Base(0xFF3F4D00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x1bf	sw_rawaf_h2iir2_coe1 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_h2iir2_coe0 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.

ISP_RAWAF_4D00_H2_IIR2_COE23

Address: Operational Base(0xFF3F4D00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ac	sw_rawaf_h2iir2_coe3 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0xe9f	sw_rawaf_h2iir2_coe2 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.

ISP_RAWAF_4D00_H2_IIR2_COE45

Address: Operational Base(0xFF3F4D00) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xf54	sw_rawaf_h2iir2_coe5 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_h2iir2_coe4 HIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.

ISP_RAWAF_4D00_V_CURVEH

Address: Operational Base(0xFF3F4D00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0578	sw_rawaf_v_ldg_gslp1 LDG curve luma high slope({5i,8f})
15:8	RW	0x08	sw_rawaf_v_ldg_gain1 LDG curve luma high minimum gain({8f})
7:0	RW	0xb9	sw_rawaf_v_ldg_lumth1 LDG curve luma high threshold ({8f})

ISP_RAWAF_4D00_V_IIR_COE0

Address: Operational Base(0xFF3F4D00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ab	sw_rawaf_v2iir_coe0 VIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x0ab	sw_rawaf_v1iir_coe0 VIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_IIR_COE1

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Address: Operational Base(0xFF3F4D00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x033	sw_rawaf_v2iir_coe1 VIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x033	sw_rawaf_v1iir_coe1 VIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_IIR_COE2

Address: Operational Base(0xFF3F4D00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e7	sw_rawaf_v2iir_coe2 VIIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x0e7	sw_rawaf_v1iir_coe2 VIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_CORING_H

Address: Operational Base(0xFF3F4D00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0e7	sw_rawaf_h_fv_slope CORING slope ({1i,8f})
15:10	RO	0x00	reserved
9:0	RW	0x0e7	sw_rawaf_h_fv_limit CORING limit ({10i})

ISP_RAWAF_4D00_V_FIR_COE0

Address: Operational Base(0xFF3F4D00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x200	sw_rawaf_v2fir_coe0 VFIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_v1fir_coe0 VFIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_FIR_COE1

Address: Operational Base(0xFF3F4D00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawaf_v2fir_coe1 VFIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_v1fir_coe1 VFIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_FIR_COE2

Address: Operational Base(0xFF3F4D00) + offset (0x00B8)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xe00	sw_rawaf_v2fir_coe2 VFIR related coefficient ({1s,2i,9f}) It has been deleted in isp-lite version.
15:12	RO	0x0	reserved
11:0	RW	0xe00	sw_rawaf_v1fir_coe2 VFIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_CORING_V

Address: Operational Base(0xFF3F4D00) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0e7	sw_rawaf_v_fv_slope CORING slope ({1i,8f})
15:10	RO	0x00	reserved
9:0	RW	0x0e7	sw_rawaf_v_fv_limit CORING limit ({10i})

ISP_RAWAF_4D00_GAUS_COE_03

Address: Operational Base(0xFF3F4D00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_rawaf_gaus_coe3 GAUS related coefficient ({1i,7f})
23:16	RW	0x08	sw_rawaf_gaus_coe2 GAUS related coefficient({1i,7f})
15:8	RW	0x10	sw_rawaf_gaus_coe1 GAUS related coefficient ({1i,7f})
7:0	RW	0x08	sw_rawaf_gaus_coe0 GAUS related coefficient ({1i,7f})

ISP_RAWAF_4D00_GAUS_COE_47

Address: Operational Base(0xFF3F4D00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_rawaf_gaus_coe7 GAUS related coefficient ({1i,7f})
23:16	RW	0x08	sw_rawaf_gaus_coe6 GAUS related coefficient ({1i,7f})
15:8	RW	0x10	sw_rawaf_gaus_coe5 GAUS related coefficient ({1i,7f})
7:0	RW	0x20	sw_rawaf_gaus_coe4 GAUS related coefficient ({1i,7f})

ISP_RAWAF_4D00_GAUS_COE_8

Address: Operational Base(0xFF3F4D00) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	sw_rawaf_gaus_coe8 GAUS related coefficient ({1i,7f})

ISP_RAWAF_4D00_HIGHLIT_THRESH

Address: Operational Base(0xFF3F4D00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x3cc	sw_rawaf_highlit_thresh If current data bigger than sw_rawaf_highlit_thresh, current data will be counted

ISP_RAWAF_4D00_HIGHLIT_CNT_WINB

Address: Operational Base(0xFF3F4D00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	ro_rawaf_highlit_cnt_winb High light count of window B

ISP_RAWAF_4D00_RAM_DATA

Address: Operational Base(0xFF3F4D00) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sum_data_wndx Total 5x5 windows, each window has 32 * 2bits. In the first 25 word, data in each word is {out_hiir_wnd_data}. In the remaining 25 word, data in each word is {out_viir_wnd_data}. It has been modified in isp-lite version.

2.4.2.28 RAWAE

RAWAE_BIG_4400_4600_4700_CTRL

Address: Operational Base(0xFF3F4400) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aemeas_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.
30	RO	0x0	ro_working_r Module working signal
29:9	RO	0x000000	reserved
8	RW	0x0	sw_aemeas_debug_en The debug signal will toggle when this bit asset
7	RW	0x0	sw_rawae_big_wnd4_en 1'b0: Window close 1'b1: Window open
6	RW	0x0	sw_rawae_big_wnd3_en 1'b0: Window close 1'b1: Window open
5	RW	0x0	sw_rawae_big_wnd2_en 1'b0: Window close 1'b1: Window open
4	RW	0x0	sw_rawae_big_wnd1_en 1'b0: Window close 1'b1: Window open
3	RO	0x0	ro_rd_ram_en User need assert this bit to 1 before reading back RAM data and set to 0 after read operation

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	sw_aemeas_wnd0_num 2'b0: 1x1 2'b1: 5x5 2'b2: 15x15 2'b3: 15x15
0	RW	0x0	sw_aemeas_en 1'b0: Disable this module 1'b1: Enable this module

RAWAE_BIG_4400_4600_4700_WND0_BLK_SIZE

Address: Operational Base(0xFF3F4400) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size Vertical offset of first block in pixels. Note: The vertical size must be oven, and need leave 2lines at last.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size Horizontal size in pixels of one block. Note: exp_h_size x window_num must be less (not equal) than the horizontal size of the picture

RAWAE_BIG_4400_4600_4700_WND0_OFFSET

Address: Operational Base(0xFF3F4400) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels.

RAWAE_BIG_4400_4600_4700_RAM_CTRL

Address: Operational Base(0xFF3F4400) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_ram_en Just for debug
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_cnt Ram cnt
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_ram_offset Ram offset

RAWAE_BIG_4400_4600_4700_WND1_SIZE

Address: Operational Base(0xFF3F4400) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window. Note: This signal is not this window's vertical size.
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window. Note: This signal is not this window's horizontal size.

RAWAE_BIG_4400_4600_4700_WND1_OFFSET

Address: Operational Base(0xFF3F4400) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels.

RAWAE_BIG_4400_4600_4700_WND2_SIZE

Address: Operational Base(0xFF3F4400) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window. Note: This signal is not this window's vertical size. It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window. Note: This signal is not this window's horizontal size. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND2_OFFSET

Address: Operational Base(0xFF3F4400) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels. It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND3_SIZE

Address: Operational Base(0xFF3F4400) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window. Note: This signal is not this window's vertical size. It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window. Note: This signal is not this window's horizontal size. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND3_OFFSET

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Address: Operational Base(0xFF3F4400) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels. It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND4_SIZE

Address: Operational Base(0xFF3F4400) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window. Note: This signal is not this window's vertical size. It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window. Note: This signal is not this window's horizontal size. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND4_OFFSET

Address: Operational Base(0xFF3F4400) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels. It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND1_SUMR

Address: Operational Base(0xFF3F4400) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd1_sumr Sum R channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND2_SUMR

Address: Operational Base(0xFF3F4400) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd2_sumr Sum R channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND3_SUMR

Address: Operational Base(0xFF3F4400) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd3_sumr Sum R channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND4_SUMR

Address: Operational Base(0xFF3F4400) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd4_sumr Sum R channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND1_SUMG

Address: Operational Base(0xFF3F4400) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd1_sumg Sum G channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND2_SUMG

Address: Operational Base(0xFF3F4400) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd2_sumg Sum G channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND3_SUMG

Address: Operational Base(0xFF3F4400) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd3_sumg Sum G channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND4_SUMG

Address: Operational Base(0xFF3F4400) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd4_sumg Sum G channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND1_SUMB

Address: Operational Base(0xFF3F4400) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd1_sumb Sum B channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND2_SUMB

Address: Operational Base(0xFF3F4400) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:0	RO	0x00000000	ro_rawae_big_wnd2_sumb Sum B channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND3_SUMB

Address: Operational Base(0xFF3F4400) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd3_sumb Sum B channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_WND4_SUMB

Address: Operational Base(0xFF3F4400) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd4_sumb Sum B channel data for this single separated window. It has been deleted in isp-lite version.

RAWAE_BIG_4400_4600_4700_RO_MEAN_BASE_ADDR

Address: Operational Base(0xFF3F4400) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	ro_rawae_mean_channelr_xy Channel r mean luminance value of block 00~44 (x,y) xy means x and y coordinate
21:12	RO	0x000	ro_rawae_mean_channelb_xy Channel b mean luminance value of block 00~44 (x,y) xy means x and y coordinate
11:0	RO	0x000	ro_rawae_mean_channelg_xy Channel g mean luminance value of block 00~44 (x,y) xy means x and y coordinate

ISP_RAWAE_LITE_4500_CTRL

Address: Operational Base(0xFF3F4500) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aemeas_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.
30	RW	0x0	ro_working_r Module working signal
29:9	RO	0x000000	reserved
8	RW	0x0	sw_aemeas_debug_en The debug signal will toggle when this bit asset
7:2	RO	0x00	reserved
1	RW	0x0	sw_aemeas_wnd_num 1'b0: 1x1 1'b1: 5x5
0	RW	0x0	sw_aemeas_en 1'b0: No mean 1'b1: Start ae module (auto clear)

ISP_RAWAE_LITE_4500_BLK_SIZE

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Address: Operational Base(0xFF3F4500) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size Vertical offset of first block in pixels. Note: The vertical size must be oven, and need leave 2lines at last.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size Horizontal size in pixels of one block. Note: exp_h_size x window_num must be less (not equal) than the horizontal size of the picture

ISP_RAWAE_LITE_4500_OFFSET

Address: Operational Base(0xFF3F4500) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels.

ISP_RAWAE_LITE_4500_RO_MEAN_XX

Address: Operational Base(0xFF3F4500) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	ro_rawae_mean_channelr_xy Channel r mean luminance value of block 00~44 (x,y), and xy means x and y coordinate. The reg address range increased from 0x10 to 0x70. It has been modified in isp-lite version.
21:12	RO	0x000	ro_rawae_mean_channelb_xy Channel b mean luminance value of block 00~44 (x,y), and xy means x and y coordinate. The reg address range increased from 0x10 to 0x70. It has been modified in isp-lite version.
11:0	RO	0x000	ro_rawae_mean_channelg_xy Channel g mean luminance value of block 00~44 (x,y), and xy means x and y coordinate. The reg address range increased from 0x10 to 0x70. It has been modified in isp-lite version.

2.4.2.29 RAWAWB

ISP_RAWAWB_5000_CTRL

Address: Operational Base(0xFF3F5000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawawb_meas_done When rawawb measurement is over, this bit is pulled up by hardware itself, then software could read the result of rawawb. When read is over, it should been pulled down by software, and rawawb will work again at the beginning of next frame after pulled down

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Bit	Attr	Reset Value	Description
30	RO	0x0	ro_rawawb_working Rawawb working state read back 1'b1: Working 1'b0: Not working
29	RO	0x0	ro_rawawb2ddr_path_err RAWAWB2DDR path has error
28	RW	0x0	sw_rawawbin_low12bit_val For control the RAWAWB input data valid bit.
27	RW	0x0	sw_rawawb_2ddr_path_sel RAWAWB2DDR path select bit 1'b0: RAWAWB in (12'b0,rawawb_in[19:0]) 1'b1: RAWAWB dsout (R10 G12 B10)
26	RW	0x0	sw_rawawb_3dyuv_en1 1'b1: 3DYUV detect Enable for all light and big window 1'b0: 3DYUV detect disable for all light and big window
25	RW	0x0	sw_rawawb_xy_en1 1'b1: XY detect Enable for all light and big window 1'b0: XY detect disable for all light and big window
24	RW	0x0	sw_rawawb_uv_en1 1'b1: UV detect Enable for all light and big window 1'b0: UV detect disable for all light and big window
23	RW	0x0	sw_rawawb_2ddr_path_en RAWAWB2DDR path enable bit
22:20	RW	0x0	sw_rawawb_light_num Number of light sources, and range is from 0 to 7
19	RW	0x0	sw_rawlsc_bypass_en 1'b1: Rawlsc bypass Enable 1'b0: Rawlsc bypass disable
18	RW	0x0	sw_rawawb_wind_size Raw to RGB down sample window size 1'b0: 8x8 window 1'b0: 4x4 window If sw_rawawb_h_size > 2560, the window size would been 8x8 forced by hardware
17	RW	0x0	sw_rawawb_in_overexposure_check_en RAWAWB input data over exposure check enable bit
16	RW	0x0	sw_rawawb_in_rshift_to_12bit_en RAWAWB input data shift to 12bit enable bit
15:13	RW	0x0	sw_rawawb_3dyuv_ls_idx3 Light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to support maximum 4 lights white point detection at the same time. 3'd0: Light 0 for 3dyuv white point detected logic 3 .. 3'd6: Light 6 for 3dyuv white point detected logic 3 3'd7: Disable for 3dyuv white point detected logic 3
12:10	RW	0x0	sw_rawawb_3dyuv_ls_idx2 Light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to support maximum 4 lights white point detection at the same time. 3'd0: Light 0 for 3dyuv white point detected logic 2 .. 3'd6: Light 6 for 3dyuv white point detected logic 2 3'd7: Disable for 3dyuv white point detected logic 2

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Bit	Attr	Reset Value	Description
9:7	RW	0x0	sw_rawawb_3dyuv_ls_idx1 Light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to support maximum 4 lights white point detection at the same time 3'd0: Light 0 for 3dyuv white point detected logic 1 .. 3'd6: Light 6 for 3dyuv white point detected logic 1 3'd7: Disable for 3dyuv white point detected logic 1
6:4	RW	0x0	sw_rawawb_3dyuv_ls_idx0 Light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to support maximum 4 lights white point detection at the same time 3'd0: Light 0 for 3dyuv white point detected logic 0 .. 3'd6: Light 6 for 3dyuv white point detected logic 0 3'd7: Disable for 3dyuv white point detected logic 0
3	RW	0x0	sw_rawawb_3dyuv_en0 1'b1: 3DYUV detect Enable for all light and normal window 1'b0: 3DYUV detect disable for all light and normal window
2	RW	0x0	sw_rawawb_xy_en0 1'b1: XY detect Enable for all light and normal window 1'b0: XY detect disable for all light and normal window
1	RW	0x0	sw_rawawb_uv_en0 1'b1: UV detect Enable for all light and normal window 1'b0: UV detect disable for all light and normal window
0	RW	0x0	sw_rawawb_en 1'b1: Rawawb Enable 1'b0: Rawawb disable

ISP_RAWAWB_5000_BLK_CTRL

Address: Operational Base(0xFF3F5000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0xffff	sw_rawawb_in_overexposure_threshold Over exposure threshold (compare high 16bit with rawawb input 20bit data)
15:9	RO	0x00	reserved
8	RW	0x0	sw_rawawb_blk_with_luma_wei_en Block luma weight Enable bit
7	RW	0x0	sw_rawawb_ds16x8_mode_en Raw to RGB down sample 16x8 mode enable bit(used for 8K size)
6:4	RW	0x0	sw_rawawb_blk_measure_illu_idx 3'b0: Select source light 3'b1: Select source light .. 3'b7: Select all lights
3	RW	0x0	sw_rawawb_blk_rtdw_measure_en The right and down corner of block measure Enable bit
2	RW	0x0	sw_rawawb_blk_measure_xytype 1'b0: Select normal window 1'b1: Select big window
1	RW	0x0	sw_rawawb_blk_measure_mode 1'b0: Measure all pixel 1'b1: Measure real one
0	RW	0x0	sw_rawawb_blk_measure_en Block measure Enable bit

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ISP_RAWAWB_5000_WIN_OFFS

Address: Operational Base(0xFF3F5000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_v_offs AWB vertical offset of crop measure window, and bit16 is written to 0 by hardware to align offset to 2
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_h_offs AWB horizontal offset of crop measure window, and bit0 is written to 0 by hardware to align offset to 2

ISP_RAWAWB_5000_WIN_SIZE

Address: Operational Base(0xFF3F5000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_v_size AWB vertical crop window size 8x8 down sample window: bit16 to bit18 are written to 0 by hardware to align size to 8 4x4 down sample window: bit16 to bit17 are written to 0 by hardware to align size to 4
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_h_size AWB horizontal window size down sample window 8x8: bit0 to bit2 are written to 0 by hardware to align size to 8 down sample window 4x4: bit0 to bit1 are written to 0 by hardware to align size to 4

ISP_RAWAWB_5000_LIMIT_RG_MAX

Address: Operational Base(0xFF3F5000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_g_max Max green value in white point detection
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_r_max Max red value in white point detection

ISP_RAWAWB_5000_LIMIT_BY_MAX

Address: Operational Base(0xFF3F5000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_y_max Max luminance value in white point detection
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_b_max Max blue value in white point detection

ISP_RAWAWB_5000_LIMIT_RG_MIN

Address: Operational Base(0xFF3F5000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	sw_rawawb_g_min Min green value in white point detection
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_r_min Min red value in white point detection

ISP_RAWAWB_5000_LIMIT_BY_MIN

Address: Operational Base(0xFF3F5000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_y_min Min luminance value in white point detection
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_b_min Min blue value in white point detection

ISP_RAWAWB_5000_WEIGHT_CURVE_CTRL

Address: Operational Base(0xFF3F5000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_rawawb_wp_hist_xytype Select normal or big window for YHIST 1'b0: Normal window 1'b1: Big window
3	RW	0x0	sw_rawawb_wp_blk_wei_en1 Block weight enable bit for big window
2	RW	0x0	sw_rawawb_wp_blk_wei_en0 Block weight enable bit for normal window
1	RW	0x0	sw_rawawb_wp_luma_wei_en1 Y weight curve enable for big window
0	RW	0x0	sw_rawawb_wp_luma_wei_en0 Y weight curve enable for normal window

ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR03

Address: Operational Base(0xFF3F5000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x60	sw_rawawb_wp_luma_weicurve_y3 Y weight curve x coordinate
23:16	RW	0x40	sw_rawawb_wp_luma_weicurve_y2 Y weight curve x coordinate
15:8	RW	0x20	sw_rawawb_wp_luma_weicurve_y1 Y weight curve x coordinate
7:0	RW	0x00	sw_rawawb_wp_luma_weicurve_y0 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR47

Address: Operational Base(0xFF3F5000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0xe0	sw_rawawb_wp_luma_weicurve_y8 Y weight curve x coordinate
23:16	RW	0xc0	sw_rawawb_wp_luma_weicurve_y7 Y weight curve x coordinate
15:8	RW	0xa0	sw_rawawb_wp_luma_weicurve_y6 Y weight curve x coordinate

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Bit	Attr	Reset Value	Description
7:0	RW	0x80	sw_rawawb_wp_luma_weicurve_y5 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR8

Address: Operational Base(0xFF3F5000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	sw_rawawb_wp_luma_weicurve_y8 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR03

Address: Operational Base(0xFF3F5000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_rawawb_wp_luma_weicurve_w3 Y weight curve y coordinate
23:22	RO	0x0	reserved
21:16	RW	0x20	sw_rawawb_wp_luma_weicurve_w2 Y weight curve y coordinate
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_rawawb_wp_luma_weicurve_w1 Y weight curve y coordinate
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w0 Y weight curve y coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR47

Address: Operational Base(0xFF3F5000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_rawawb_wp_luma_weicurve_w7 Y weight curve y coordinate
23:22	RO	0x0	reserved
21:16	RW	0x20	sw_rawawb_wp_luma_weicurve_w6 Y weight curve y coordinate
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_rawawb_wp_luma_weicurve_w5 Y weight curve y coordinate
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w4 Y weight curve y coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR8

Address: Operational Base(0xFF3F5000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0100	sw_rawawb_pre_wbgain_inv_r For some sensor has already do awb-gain need do some pre-white-balance gain operation or use for rawawb gain
15:6	RO	0x000	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w8 Y weight curve y coordinate

ISP_RAWAWB_5000_PRE_WBGAIN_INV

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Address: Operational Base(0xFF3F5000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0100	sw_rawawb_pre_wbgain_inv_b For some sensor has already do awb-gain need do some pre-white-balance gain operation or use for rawawb gain
15:13	RO	0x0	reserved
12:0	RW	0x0100	sw_rawawb_pre_wbgain_inv_g For some sensor has already do awb-gain need do some pre-white-balance gain operation or use for rawawb gain

ISP_RAWAWB_5000_UV_DETC_VERTEX0_0

Address: Operational Base(0xFF3F5000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_0 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_0 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_0

Address: Operational Base(0xFF3F5000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_0 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_0 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_0

Address: Operational Base(0xFF3F5000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_0 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_0 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_0

Address: Operational Base(0xFF3F5000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_0 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_0 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_0

Address: Operational Base(0xFF3F5000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:0	RW	0x00000	sw_rawawb_islope01_0 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_0

Address: Operational Base(0xFF3F5000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope12_0 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_0

Address: Operational Base(0xFF3F5000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope23_0 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_0

Address: Operational Base(0xFF3F5000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope30_0 Slope inversion

ISP_RAWAWB_5000_UV_DETC_VERTEX0_1

Address: Operational Base(0xFF3F5000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_1 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_1 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_1

Address: Operational Base(0xFF3F5000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_1 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_1 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_1

Address: Operational Base(0xFF3F5000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_1 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_1 Vertex coordinate

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ISP_RAWAWB_5000_UV_DETC_VERTEX3_1

Address: Operational Base(0xFF3F5000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_1 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_1 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_1

Address: Operational Base(0xFF3F5000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope01_1 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_1

Address: Operational Base(0xFF3F5000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope12_1 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_1

Address: Operational Base(0xFF3F5000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope23_1 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_1

Address: Operational Base(0xFF3F5000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope30_1 Slope inversion

ISP_RAWAWB_5000_UV_DETC_VERTEX0_2

Address: Operational Base(0xFF3F5000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_2 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_2 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_2

Address: Operational Base(0xFF3F5000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_2 Vertex coordinate
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	sw_rawawb_vertex1_u_2 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_2

Address: Operational Base(0xFF3F5000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_2 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_2 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_2

Address: Operational Base(0xFF3F5000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_2 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_2 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_2

Address: Operational Base(0xFF3F5000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope01_2 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_2

Address: Operational Base(0xFF3F5000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope12_2 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_2

Address: Operational Base(0xFF3F5000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope23_2 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_2

Address: Operational Base(0xFF3F5000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope30_2 Slope inversion

ISP_RAWAWB_5000_UV_DETC_VERTEX0_3

Address: Operational Base(0xFF3F5000) + offset (0x00A0)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_3 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_3 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_3

Address: Operational Base(0xFF3F5000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_3 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_3 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_3

Address: Operational Base(0xFF3F5000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_3 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_3 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_3

Address: Operational Base(0xFF3F5000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_3 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_3 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_3

Address: Operational Base(0xFF3F5000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope01_3 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_3

Address: Operational Base(0xFF3F5000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope12_3 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_3

Address: Operational Base(0xFF3F5000) + offset (0x00B8)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope23_3 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_3

Address: Operational Base(0xFF3F5000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope30_3 Slope inversion

ISP_RAWAWB_5000_YUV_RGB2ROTY_0

Address: Operational Base(0xFF3F5000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_rawawb_rgb2ryuvmat1_y RGB2ROTY matrix, coefficient 1
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat0_y RGB2ROTY matrix, coefficient 0

ISP_RAWAWB_5000_YUV_RGB2ROTY_1

Address: Operational Base(0xFF3F5000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_rgb2ryuvofs_y RGB2ROTY matrix, offset
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat2_y RGB2ROTY matrix, coefficient 2

ISP_RAWAWB_5000_YUV_RGB2ROTU_0

Address: Operational Base(0xFF3F5000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_rawawb_rgb2ryuvmat1_u RGB2ROTU matrix, coefficient 1
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat0_u RGB2ROTU matrix, coefficient 0

ISP_RAWAWB_5000_YUV_RGB2ROTU_1

Address: Operational Base(0xFF3F5000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_rgb2ryuvofs_u RGB2ROTU matrix, offset
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat2_u RGB2ROTU matrix, coefficient 2

ISP_RAWAWB_5000_YUV_RGB2ROTV_0

Address: Operational Base(0xFF3F5000) + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_rawawb_rgb2ryuvmat1_v RGB2ROTV matrix, coefficient 1
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat0_v RGB2ROTV matrix, coefficient 0

ISP_RAWAWB_5000_YUV_RGB2ROTV_1

Address: Operational Base(0xFF3F5000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_rgb2ryuvofs_v RGB2ROTY matrix, offset
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat2_v RGB2ROTY matrix, coefficient 2

ISP_RAWAWB_5000_YUV_X_COOR_Y_0

Address: Operational Base(0xFF3F5000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls0_y Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls0_y Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_U_0

Address: Operational Base(0xFF3F5000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls0_u Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls0_u Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_V_0

Address: Operational Base(0xFF3F5000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls0_v Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls0_v Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X1X2_DIS_0

Address: Operational Base(0xFF3F5000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu1_ls0 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu0_ls0 The x coordinate of u interpolation curve

Rockchip Confidencial

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved
4:0	RW	0x00	sw_rawawb_dis_x1x2_ls0 The distance between x1 and x2 (must 2^n)

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_0

Address: Operational Base(0xFF3F5000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu5_ls0 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu4_ls0 The x coordinate of u interpolation curve
15:8	RW	0x00	sw_rawawb_rotu3_ls0 The x coordinate of u interpolation curve
7:0	RW	0x00	sw_rawawb_rotu2_ls0 The x coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_0

Address: Operational Base(0xFF3F5000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th1_ls0 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th0_ls0 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_0

Address: Operational Base(0xFF3F5000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th3_ls0 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th2_ls0 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_0

Address: Operational Base(0xFF3F5000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th5_ls0 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th4_ls0 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_X_COOR_Y_1

Address: Operational Base(0xFF3F5000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls1_y Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_rawawb_coor_x1_ls1_y Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_U_1

Address: Operational Base(0xFF3F5000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls1_u Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls1_u Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_V_1

Address: Operational Base(0xFF3F5000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls1_v Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls1_v Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X1X2_DIS_1

Address: Operational Base(0xFF3F5000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu1_ls1 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu0_ls1 The x coordinate of u interpolation curve
15:5	RO	0x000	reserved
4:0	RW	0x00	sw_rawawb_dis_x1x2_ls1 The distance between x1 and x2 (must 2^n)

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_1

Address: Operational Base(0xFF3F5000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu5_ls1 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu4_ls1 The x coordinate of u interpolation curve
15:8	RW	0x00	sw_rawawb_rotu3_ls1 The x coordinate of u interpolation curve
7:0	RW	0x00	sw_rawawb_rotu2_ls1 The x coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_1

Address: Operational Base(0xFF3F5000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th1_ls1 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_rawawb_th0_ls1 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_1

Address: Operational Base(0xFF3F5000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th3_ls1 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th2_ls1 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_1

Address: Operational Base(0xFF3F5000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th5_ls1 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th4_ls1 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_X_COOR_Y_2

Address: Operational Base(0xFF3F5000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls2_y Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls2_y Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_U_2

Address: Operational Base(0xFF3F5000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls2_u Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls2_u Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_V_2

Address: Operational Base(0xFF3F5000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls2_v Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls2_v Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X1X2_DIS_2

Rockchip Confidencial

Address: Operational Base(0xFF3F5000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu1_ls2 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu0_ls2 The x coordinate of u interpolation curve
15:5	RO	0x000	reserved
4:0	RW	0x00	sw_rawawb_dis_x1x2_ls2 The distance between x1 and x2 (must 2^n)

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_2

Address: Operational Base(0xFF3F5000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu5_ls2 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu4_ls2 The x coordinate of u interpolation curve
15:8	RW	0x00	sw_rawawb_rotu3_ls2 The x coordinate of u interpolation curve
7:0	RW	0x00	sw_rawawb_rotu2_ls2 The x coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_2

Address: Operational Base(0xFF3F5000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th1_ls2 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th0_ls2 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_2

Address: Operational Base(0xFF3F5000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th3_ls2 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th2_ls2 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_2

Address: Operational Base(0xFF3F5000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th5_ls2 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th4_ls2 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_X_COOR_Y_3

Address: Operational Base(0xFF3F5000) + offset (0x01A0)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls3_y Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls3_y Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_U_3

Address: Operational Base(0xFF3F5000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls3_u Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls3_u Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_V_3

Address: Operational Base(0xFF3F5000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls3_v Signed, 8 integer and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls3_v Unsigned, 8 integer and 4 fraction

ISP_RAWAWB_5000_YUV_X1X2_DIS_3

Address: Operational Base(0xFF3F5000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu1_ls3 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu0_ls3 The x coordinate of u interpolation curve
15:5	RO	0x000	reserved
4:0	RW	0x00	sw_rawawb_dis_x1x2_ls3 The distance between x1 and x2 (must 2^n)

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_3

Address: Operational Base(0xFF3F5000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu5_ls3 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu4_ls3 The x coordinate of u interpolation curve
15:8	RW	0x00	sw_rawawb_rotu3_ls3 The x coordinate of u interpolation curve
7:0	RW	0x00	sw_rawawb_rotu2_ls3 The x coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_3

Address: Operational Base(0xFF3F5000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
27:16	RW	0x000	sw_rawawb_th1_ls3 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th0_ls3 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_3

Address: Operational Base(0xFF3F5000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th3_ls3 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th2_ls3 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_3

Address: Operational Base(0xFF3F5000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th5_ls3 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th4_ls3 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_RGB2XY_WT01

Address: Operational Base(0xFF3F5000) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_wt1 RGB2XY weight matrix, coefficient 1
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_wt0 RGB2XY weight matrix, coefficient 0

ISP_RAWAWB_5000_RGB2XY_WT2

Address: Operational Base(0xFF3F5000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_rawawb_wt2 RGB2XY weight matrix, coefficient 0

ISP_RAWAWB_5000_RGB2XY_MAT0_XY

Address: Operational Base(0xFF3F5000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat0_y RGB2XY, rotation matrix, first column XY
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat0_x RGB2XY, rotation matrix, first column XY

ISP_RAWAWB_5000_RGB2XY_MAT1_XY

Rockchip Confidencial

Address: Operational Base(0xFF3F5000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat1_y RGB2XY, rotation matrix, second column XY
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat1_x RGB2XY, rotation matrix, second column XY

ISP_RAWAWB_5000_RGB2XY_MAT2_XY

Address: Operational Base(0xFF3F5000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat2_y RGB2XY, rotation matrix, third column XY
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat2_x RGB2XY, rotation matrix, third column XY

ISP_RAWAWB_5000_XY_DETC_NOR_X_0

Address: Operational Base(0xFF3F5000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_0 XY detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_0 XY detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_0

Address: Operational Base(0xFF3F5000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_0 XY detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_0 XY detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_0

Address: Operational Base(0xFF3F5000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_0 XY detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_0 XY detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_0

Address: Operational Base(0xFF3F5000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_0 XY detect, down y boundary of big range

Rockchip Confidencial

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_0 XY detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_1

Address: Operational Base(0xFF3F5000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_1 XY detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_1 XY detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_1

Address: Operational Base(0xFF3F5000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_1 XY detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_1 XY detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_1

Address: Operational Base(0xFF3F5000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_1 XY detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_1 XY detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_1

Address: Operational Base(0xFF3F5000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_1 XY detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_1 XY detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_2

Address: Operational Base(0xFF3F5000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_2 XY detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_2 XY detect, left x boundary of normal range

Rockchip Confidencial

ISP_RAWAWB_5000_XY_DETC_NOR_Y_2

Address: Operational Base(0xFF3F5000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_2 XY detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_2 XY detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_2

Address: Operational Base(0xFF3F5000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_2 XY detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_2 XY detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_2

Address: Operational Base(0xFF3F5000) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_2 XY detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_2 XY detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_3

Address: Operational Base(0xFF3F5000) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_3 XY detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_3 XY detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_3

Address: Operational Base(0xFF3F5000) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_3 XY detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_3 XY detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_3

Address: Operational Base(0xFF3F5000) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_rawawb_big_x1_3 XY detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_3 XY detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_3

Address: Operational Base(0xFF3F5000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_3 XY detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_3 XY detect, up y boundary of big range

ISP_RAWAWB_5000_MULTIWINDOW_EXC_CTRL

Address: Operational Base(0xFF3F5000) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawawb_multiwindow_en The multi-window measure enable 1'b1: Enable 1'b0: Disable
30:28	RO	0x0	reserved
27	RW	0x0	sw_rawawb_exc_wp_region6_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
26	RO	0x0	reserved
25:24	RW	0x0	sw_rawawb_exc_wp_region6_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
23	RW	0x0	sw_rawawb_exc_wp_region5_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
22	RO	0x0	reserved
21:20	RW	0x0	sw_rawawb_exc_wp_region5_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
19	RW	0x0	sw_rawawb_exc_wp_region4_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
18	RO	0x0	reserved
17:16	RW	0x0	sw_rawawb_exc_wp_region4_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
15	RW	0x0	sw_rawawb_exc_wp_region3_domain The domain of exclude region 1'b1: XY range 1'b0: UV range

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Bit	Attr	Reset Value	Description
14	RW	0x0	sw_rawawb_exc_wp_region3_measen The measurement enable of exclude region in XY or UV range 1'b1: Enable 1'b0: Disable
13:12	RW	0x0	sw_rawawb_exc_wp_region3_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
11	RW	0x0	sw_rawawb_exc_wp_region2_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
10	RW	0x0	sw_rawawb_exc_wp_region2_measen The measurement enable of exclude region in XY or UV range 1'b1: Enable 1'b0: Disable
9:8	RW	0x0	sw_rawawb_exc_wp_region2_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
7	RW	0x0	sw_rawawb_exc_wp_region1_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
6	RW	0x0	sw_rawawb_exc_wp_region1_measen The measurement enable of exclude region in XY or UV range 1'b1: Enable 1'b0: Disable
5:4	RW	0x0	sw_rawawb_exc_wp_region1_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
3	RW	0x0	sw_rawawb_exc_wp_region0_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
2	RW	0x0	sw_rawawb_exc_wp_region0_measen The measurement enable of exclude region in XY or UV range 1'b1: Enable 1'b0: Disable
1:0	RW	0x0	sw_rawawb_exc_wp_region0_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window

ISP_RAWAWB_5000_MULTIWINDOW0_OFFS

Address: Operational Base(0xFF3F5000) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow0_v_offs The multi-window vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow0_h_offs The multi-window horizontal offset

ISP_RAWAWB_5000_MULTIWINDOW0_SIZE

Address: Operational Base(0xFF3F5000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_rawawb_multiwindow0_v_size The multi-window vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow0_h_size The multi-window horizontal size

ISP_RAWAWB_5000_MULTIWINDOW1_OFFS

Address: Operational Base(0xFF3F5000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow1_v_offs The multi-window vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow1_h_offs The multi-window horizontal offset

ISP_RAWAWB_5000_MULTIWINDOW1_SIZE

Address: Operational Base(0xFF3F5000) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow1_v_size The multi-window vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow1_h_size The multi-window horizontal size

ISP_RAWAWB_5000_MULTIWINDOW2_OFFS

Address: Operational Base(0xFF3F5000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow2_v_offs The multi-window vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow2_h_offs The multi-window horizontal offset

ISP_RAWAWB_5000_MULTIWINDOW2_SIZE

Address: Operational Base(0xFF3F5000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow2_v_size The multi-window vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow2_h_size The multi-window horizontal size

ISP_RAWAWB_5000_MULTIWINDOW3_OFFS

Address: Operational Base(0xFF3F5000) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow3_v_offs The multi-window vertical offset
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_rawawb_multiwindow3_h_offs The multi-window horizontal offset

ISP_RAWAWB_5000_MULTIWINDOW3_SIZE

Address: Operational Base(0xFF3F5000) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow3_v_size The multi-window vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow3_h_size The multi-window horizontal size

ISP_RAWAWB_5000_EXC_WP_REGION0_XU

Address: Operational Base(0xFF3F5000) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region0_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region0_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION0_YV

Address: Operational Base(0xFF3F5000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region0_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region0_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION1_XU

Address: Operational Base(0xFF3F5000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region1_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION1_YV

Address: Operational Base(0xFF3F5000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region1_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION2_XU

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Address: Operational Base(0xFF3F5000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region2_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION2_YV

Address: Operational Base(0xFF3F5000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region2_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region2_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION3_XU

Address: Operational Base(0xFF3F5000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region3_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region3_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION3_YV

Address: Operational Base(0xFF3F5000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region3_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region3_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION4_XU

Address: Operational Base(0xFF3F5000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region4_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region4_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION4_YV

Address: Operational Base(0xFF3F5000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region4_yv1 The bottom boundary of exclude region in XY or UV range

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region4_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION5_XU

Address: Operational Base(0xFF3F5000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region5_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region5_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION5_YV

Address: Operational Base(0xFF3F5000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region5_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region5_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION6_XU

Address: Operational Base(0xFF3F5000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region6_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region6_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION6_YV

Address: Operational Base(0xFF3F5000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region6_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region6_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_WEIGHT0_3

Address: Operational Base(0xFF3F5000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x3f	sw_rawawb_exc_wp_region3_weight The white point weight of exclude region3
23:22	RO	0x0	reserved
21:16	RW	0x3f	sw_rawawb_exc_wp_region2_weight The white point weight of exclude region2
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x3f	sw_rawawb_exc_wp_region1_weight The white point weight of exclude region1
7:6	RO	0x0	reserved
5:0	RW	0x3f	sw_rawawb_exc_wp_region0_weight The white point weight of exclude region0

ISP_RAWAWB_5000_EXC_WP_WEIGHT4_6

Address: Operational Base(0xFF3F5000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x3f	sw_rawawb_exc_wp_region6_weight The white point weight of exclude region6
15:14	RO	0x0	reserved
13:8	RW	0x3f	sw_rawawb_exc_wp_region5_weight The white point weight of exclude region5
7:6	RO	0x0	reserved
5:0	RW	0x3f	sw_rawawb_exc_wp_region4_weight The white point weight of exclude region4

ISP_RAWAWB_5000_SUM_RGAIN_NOR_0

Address: Operational Base(0xFF3F5000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_0 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_0

Address: Operational Base(0xFF3F5000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_0 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_NOR_0

Address: Operational Base(0xFF3F5000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_0 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_0

Address: Operational Base(0xFF3F5000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_0 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_0

Address: Operational Base(0xFF3F5000) + offset (0x0358)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_0 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_BIG_0

Address: Operational Base(0xFF3F5000) + offset (0x035C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:0	RO	0x0000000	ro_rawawb_wp_num_big_0 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_1

Address: Operational Base(0xFF3F5000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_1 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_1

Address: Operational Base(0xFF3F5000) + offset (0x0378)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_1 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_NOR_1

Address: Operational Base(0xFF3F5000) + offset (0x037C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_1 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_1

Address: Operational Base(0xFF3F5000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_1 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_1

Address: Operational Base(0xFF3F5000) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_1 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_BIG_1

Address: Operational Base(0xFF3F5000) + offset (0x038C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_1 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_2

Address: Operational Base(0xFF3F5000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_2 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_2

Address: Operational Base(0xFF3F5000) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_2 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_NOR_2

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Address: Operational Base(0xFF3F5000) + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_2 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_2

Address: Operational Base(0xFF3F5000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_2 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_2

Address: Operational Base(0xFF3F5000) + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_2 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_BIG_2

Address: Operational Base(0xFF3F5000) + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_2 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_3

Address: Operational Base(0xFF3F5000) + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_3 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_3

Address: Operational Base(0xFF3F5000) + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_3 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_NOR_3

Address: Operational Base(0xFF3F5000) + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_3 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_BGAIN_BIG_3

Address: Operational Base(0xFF3F5000) + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_3 Read only: white point sum of B-gain

ISP_RAWAWB_5000_SUM_RGAIN_BIG_3

Address: Operational Base(0xFF3F5000) + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_3 Read only: white point sum of R-gain

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ISP_RAWAWB_5000_WP_NUM_BIG_3

Address: Operational Base(0xFF3F5000) + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_3 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_R_EXC_0

Address: Operational Base(0xFF3F5000) + offset (0x05E0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_r_exc_0 The R-gain component summation in the exclude range

ISP_RAWAWB_5000_SUM_B_EXC_0

Address: Operational Base(0xFF3F5000) + offset (0x05E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_b_exc_0 The B-gain component summation in the exclude range

ISP_RAWAWB_5000_WP_NM_EXC_0

Address: Operational Base(0xFF3F5000) + offset (0x05EC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_nm_exc_0 The number of white point in the exclude region

ISP_RAWAWB_5000_SUM_R_EXC_1

Address: Operational Base(0xFF3F5000) + offset (0x05F0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_r_exc_1 The R-gain component summation in the exclude range

ISP_RAWAWB_5000_SUM_B_EXC_1

Address: Operational Base(0xFF3F5000) + offset (0x05F8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_b_exc_1 The B-gain component summation in the exclude range

ISP_RAWAWB_5000_WP_NM_EXC_1

Address: Operational Base(0xFF3F5000) + offset (0x05FC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_nm_exc_1 The number of white point in the exclude region

ISP_RAWAWB_5000_SUM_R_EXC_2

Address: Operational Base(0xFF3F5000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:0	RO	0x00000000	ro_sum_r_exc_2 The R-gain component summation in the exclude range

ISP_RAWAWB_5000_SUM_B_EXC_2

Address: Operational Base(0xFF3F5000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_b_exc_2 The B-gain component summation in the exclude range

ISP_RAWAWB_5000_WP_NM_EXC_2

Address: Operational Base(0xFF3F5000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_nm_exc_2 The number of white point in the exclude region

ISP_RAWAWB_5000_SUM_R_EXC_3

Address: Operational Base(0xFF3F5000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_r_exc_3 The R-gain component summation in the exclude range

ISP_RAWAWB_5000_SUM_B_EXC_3

Address: Operational Base(0xFF3F5000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_b_exc_3 The B-gain component summation in the exclude range

ISP_RAWAWB_5000_WP_NM_EXC_3

Address: Operational Base(0xFF3F5000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_nm_exc_3 The number of white point in the exclude region

ISP_RAWAWB_5000_Y_HIST01

Address: Operational Base(0xFF3F5000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin1 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin0 The bin of YHIST

ISP_RAWAWB_5000_Y_HIST23

Address: Operational Base(0xFF3F5000) + offset (0x0624)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin3 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin2 The bin of YHIST

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ISP_RAWAWB_5000_Y_HIST45

Address: Operational Base(0xFF3F5000) + offset (0x0628)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin5 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin4 The bin of YHIST

ISP_RAWAWB_5000_Y_HIST67

Address: Operational Base(0xFF3F5000) + offset (0x062C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin7 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin6 The bin of YHIST

ISP_RAWAWB_5000_WPNUM2_0

Address: Operational Base(0xFF3F5000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_num2_0 White pixel num when XY and UV all white pixel

ISP_RAWAWB_5000_WPNUM2_1

Address: Operational Base(0xFF3F5000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_num2_1 White pixel num when XY and UV all white pixel

ISP_RAWAWB_5000_WPNUM2_2

Address: Operational Base(0xFF3F5000) + offset (0x0638)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_num2_2 White pixel num when XY and UV all white pixel

ISP_RAWAWB_5000_WPNUM2_3

Address: Operational Base(0xFF3F5000) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_num2_3 White pixel num when XY and UV all white pixel

ISP_RAWAWB_5000_RAM_CTRL

Address: Operational Base(0xFF3F5000) + offset (0x0650)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawawb_rd_ram_en This bit is not need configuration in normal case, software could read the ram directly when rawawb interruption is valid. But the software could read the information in the ram in case the rawawb is failed to create interruption or stuck. The bit is need pulled down again before the next valid frame statistics
30:22	RO	0x000	ro_ram_rdaddr_cnt RAM real address when read 15x15 window statistics in ram, read only

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Bit	Attr	Reset Value	Description
21:9	RO	0x0000	reserved
8:0	RW	0x000	sw_rawawb_ram_offs The 15x15 windows statistics information is stored in ram, the real size of ram is 225x57. Each ram address is for one window. The sw_rawawb_ram_offs is ram offset address when reading, so it is meas the software could read statistics from the offset window

ISP_RAWAWB_5000_WRAM_CTRL

Address: Operational Base(0xFF3F5000) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	ro_rawawb_ram_cnt Configure ram count
15:0	RO	0x0000	reserved

ISP_RAWAWB_5000_WIN_WEIGHT_0

Address: Operational Base(0xFF3F5000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	sw_rawawb_weight_reg0 Sub-window weight from blk00 to blk04. It has been modified in isp-lite version.

ISP_RAWAWB_5000_WIN_WEIGHT_1

Address: Operational Base(0xFF3F5000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	sw_rawawb_weight_reg1 Sub-window weight from blk10 to blk14. It has been modified in isp-lite version.

ISP_RAWAWB_5000_WIN_WEIGHT_2

Address: Operational Base(0xFF3F5000) + offset (0x0668)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	sw_rawawb_weight_reg2 Sub-window weight from blk20 to blk24. It has been modified in isp-lite version.

ISP_RAWAWB_5000_WIN_WEIGHT_3

Address: Operational Base(0xFF3F5000) + offset (0x066C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	sw_rawawb_weight_reg3 Sub-window weight from blk30 to blk34. It has been modified in isp-lite version.

ISP_RAWAWB_5000_WIN_WEIGHT_4

Address: Operational Base(0xFF3F5000) + offset (0x0670)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:0	RW	0x00000000	sw_rawawb_weight_reg4 Sub-window weight from blk40 to blk44. It has been modified in isp-lite version.

ISP_RAWAWB_5000_REG_DATA_BASE

Address: Operational Base(0xFF3F5000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_wind5x5 There is 25 window information, each information is 78bits, 21bits for each RGB channel and 15bits for white point number. In the first 50 words, in each even word: {G[10:0], R[20:0]}, and in each odd word: {B[20:0], G[20:11]}. In the remaining 13 words, in each word: {Wpnum1[14:0], Wpnum0[14:0]}. The read reg address should equal this base address each read reg option, and reg address is added by hardware. It has been modified in isp-lite version.

2.4.2.30 RAWHIST

ISP_RAWHIST_BIG_4800_4A00_4B00_CTRL

Address: Operational Base(0xFF3F4800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aehist_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.
30	RO	0x0	ro_aehist_working This module working signal
29:28	RW	0x2	sw_aehist_wnd_num 2'd0, 2'd1: 5x5 2'd2, 2'd3: 15x15
27	RO	0x0	reserved
26:24	RW	0x0	sw_aehist_data_sel 3'd0: Input_data[11:4] 3'd1: Input_data[10:3] 3'd2: Input_data[9:2] 3'd3: Input_data[8:1] 3'd4: Input_data[7:0] others: Input_data[7:0] It has been deleted in isp-lite version.
23:12	RW	0x000	sw_aehist_waterline For region statics It has been deleted in isp-lite version.
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	sw_aehist_mode Histogram mode, luminance is taken at ISP output before output formatter 3'd7, 3'd6: Must not be used 3'd5: Y (luminance) histogram 3'd4: B histogram 3'd3: G histogram 3'd2: R histogram 3'd1: Reserved 3'd0: Disable, no measurements Note: If RGB combined mode is used, then the 3 color components are sampled one after the other. The software has to assure that all 3 color components are inside the selected window.
7	RW	0x0	sw_aehist_debug_en The debug signal will toggle when this bit enable.
6:4	RO	0x0	reserved
3:1	RW	0x0	sw_aehist_stepsize Histogram previous divider, process every (step size) pixel, all other pixels are skipped
0	RW	0x0	sw_aehist_en Module enable bit

ISP_RAWHIST_BIG_4800_4A00_4B00_SIZE

Address: Operational Base(0xFF3F4800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_aehist_v_size Vertical size in lines of one sub-window
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_aehist_h_size Horizontal size in pixels of one sub-window

ISP_RAWHIST_BIG_4800_4A00_4B00_OFFS

Address: Operational Base(0xFF3F4800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aehist_v_offset Vertical offset of first window in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aehist_h_offset Horizontal offset of first window in pixels.

ISP_RAWHIST_BIG_4800_4A00_4B00_HRAM_CTRL

Address: Operational Base(0xFF3F4800) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_ram_en Just for debug
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_cnt RAM counter for write or read
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_ram_offset RAM offset for write or read

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ISP_RAWHIST_BIG_4800_4A00_4B00_RAW2Y_CC

Address: Operational Base(0xFF3F4800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawae_off The coefficient of RAW2Y formula
23:16	RW	0x0d	sw_rawae_bcc RAW2Y blue channel coefficient
15:8	RW	0x20	sw_rawae_gcc RAW2Y green channel coefficient
7:0	RW	0x21	sw_rawae_rcc RAW2Y red channel coefficient

ISP_RAWHIST_BIG_4800_4A00_4B00_WRAM_CTRL

Address: Operational Base(0xFF3F4800) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	ro_ram_cnt RAM counter for write or read
15:6	RO	0x000	reserved
5:0	RW	0x00	sw_ram_offset RAM offset for write or read

ISP_RAWHIST_BIG_4800_4A00_4B00_WEIGHT_BASE

Address: Operational Base(0xFF3F4800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_aehist_weight_wnd4 Sub-window weight from num0 to num224
23:18	RW	0x20	sw_aehist_weight_wnd3 Sub-window weight from num0 to num224
17:12	RW	0x20	sw_aehist_weight_wnd2 Sub-window weight from num0 to num224
11:6	RW	0x20	sw_aehist_weight_wnd1 Sub-window weight from num0 to num224
5:0	RW	0x20	sw_aehist_weight_wnd0 Sub-window weight from num0 to num224

ISP_RAWHIST_BIG_4800_4A00_4B00_RO_BASE_BIN

Address: Operational Base(0xFF3F4800) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_aehist_bin_x Measured bin count as 28-bit unsigned integer value with 5 fractional part

ISP_RAWHIST_LITE_4900_CTRL

Address: Operational Base(0xFF3F4900) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aehist_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.

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Bit	Attr	Reset Value	Description
30	RO	0x0	ro_aehist_working This module working signal
29:27	RO	0x0	reserved
26:24	RW	0x0	sw_aehist_data_sel 3'd0: Input_data[11:4] 3'd1: Input_data[10:3] 3'd2: Input_data[9:2] 3'd3: Input_data[8:1] 3'd4: Input_data[7:0] others: Input_data[7:0] It has been deleted in isp-lite version.
23:12	RW	0x000	sw_aehist_waterline For region statics It has been deleted in isp-lite version.
11	RO	0x0	reserved
10:8	RW	0x0	sw_aehist_mode Histogram mode, luminance is taken at ISP output before output formatter 3'd7, 3'd 6: Must not be used 3'd5: Y (luminance) histogram 3'd4: B histogram 3'd3: G histogram 3'd2: R histogram 3'd1: Reserved 3'd0: Disable, no measurements Note: If RGB combined mode is used, then the 3 color components are sampled one after the other. The software has to assure that all 3 color components are inside the selected window.
7	RW	0x0	sw_aehist_debug_en The debug signal will toggle when this bit enable.
6:4	RO	0x0	reserved
3:1	RW	0x0	sw_aehist_stepsize Histogram previous divider, process every (step size) pixel, all other pixels are skipped
0	RW	0x0	sw_aehist_en Module enable bit

ISP_RAWHIST_LITE_4900_SIZE

Address: Operational Base(0xFF3F4900) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_aehist_v_size Vertical size in lines of one sub-window
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_aehist_h_size Horizontal size in pixels of one sub-window

ISP_RAWHIST_LITE_4900_OFFS

Address: Operational Base(0xFF3F4900) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aehist_v_offset Vertical offset of first window in pixels.

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aehist_h_offset Horizontal offset of first window in pixels.

ISP_RAWHIST_LITE_4900_RAM_CTRL

Address: Operational Base(0xFF3F4900) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_ram_en Just for debug
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_cnt RAM counter for write or read
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_ram_offset RAM offset for write or read

ISP_RAWHIST_LITE_4900_RAW2Y_CC

Address: Operational Base(0xFF3F4900) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawae_off The offset of RAW2Y formula
23:16	RW	0x0d	sw_rawae_bcc RAW2Y blue channel coefficient
15:8	RW	0x20	sw_rawae_gcc RAW2Y green channel coefficient
7:0	RW	0x21	sw_rawae_rcc RAW2Y red channel coefficient

ISP_RAWHIST_LITE_4900_WEIGHT_0

Address: Operational Base(0xFF3F4900) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_aehist_weight_wnd3 Sub-window weight from num0 to num24
23:22	RO	0x0	reserved
21:16	RW	0x20	sw_aehist_weight_wnd2 Sub-window weight from num0 to num24
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_aehist_weight_wnd1 Sub-window weight from num0 to num24
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_aehist_weight_wnd0 Sub-window weight from num0 to num24

ISP_RAWHIST_LITE_4900_RO_BASE_BIN

Address: Operational Base(0xFF3F4900) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_aehist_bin_x Measured bin count as 28-bit unsigned integer value with 5 fractional part. It has been modified in isp-lite version.

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2.4.2.31 IMG_EFF

IMG_EFF_0200_IMG_EFF_CTRL

Address: Operational Base(0xFF3F0200) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	full_range 1'b0: Pixel value range according to BT.601 1'b1: YCbCr full range 0~255 It has been deleted in isp-lite version.
4	RW	0x0	cfg_upd 1'b0: Nothing happens 1'b1: Update shadow registers read: always '0' It has been deleted in isp-lite version.
3:1	RW	0x0	effect_mode Effect mod 3'b000: Black & white effect (grayscale) 3'b001: Negative 3'b010: Sepia effect 3'b011: Color selection effect Others: Reserved It has been deleted in isp-lite version.
0	RW	0x0	bypass_mode Bypass mode 1'b1: Processing is activated 1'b0: Processing is deactivated, bypass mode is selected --- IMG_EFF_CTRL --- Note: full_range for image effects is supported in MARVIN M5_v6, M5_v7 only.

IMG_EFF_0200_IMG_EFF_COLOR_SEL

Address: Operational Base(0xFF3F0200) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	color_threshold Threshold value of the RGB colors for the color selection effect It has been deleted in isp-lite version.
7:3	RO	0x00	reserved
2:0	RW	0x0	color_selection Defining the maintained color: 3'b000: Red green and blue 3'b001: Blue 3'b010: Green 3'b011: Green and blue 3'b100: Red 3'b101: Red and blue 110: red and green 111: red green and blue It has been deleted in isp-lite version.

IMG_EFF_0200_IMG_EFF_TINT

Address: Operational Base(0xFF3F0200) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0x88	incr_cr Cr increment value of a tint. 7 bits for value, 1 sign bit. Default tint is R=162 G=138 B=101, which is used for the sepia effect. See below for the calculation of the entries It has been deleted in isp-lite version.
7:0	RW	0x0c	incr_cb Cb increment value of a tint. 7 bits for value, 1 sign bit. Default tint is R=162 G=138 B=101, which is used for the sepia effect. See below for the calculation of the entries. --- IMG_EFF_TINT --- Note: Calculation process of incr_cr and incr_cb: - tint values given in RGB format: R G B - converted to Cb and Cr: Cb = -0.148*R - 0.291*G + 0.439*B + 128 Cr = 0.439*R - 0.368*G - 0.071*B + 128 - calculating of the increments inc_Cb = (128 C Cb)/110 inc_Cr = (128 C Cr)/110 - register entry of the increments with an accuracy of 1/64 incr_cb = inc_Cb * 64 incr_cr = inc_Cr * 64 It has been deleted in isp-lite version.

IMG_EFF_0200_IMG_EFF_CTRL_SHD

Address: Operational Base(0xFF3F0200) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:1	RO	0x0	effect_mode_shd Effect mode 3'b000: Black & white effect (grayscale) 3'b001: Negative 3'b010: Sepia effect 3'b011: Color selection effect 3'b100: Emboss effect 3'b101: Sketch effect 3'b110: Sharpen effect 3'b111: Reserved It has been deleted in isp-lite version.
0	RO	0x0	reserved

2.5 Application Notes

2.5.1 VICAP Interface

ISP support VICAP direct path into ISP process, including HDR/no-HDR on the fly mode.

2.5.1.1 normal mode (Single ID)

For this mode:
Configure sw_ibuf_op_mode = 0.
All DMATX are available, but all DMARX are unavailable.
For example: raw10, lanex4
CTRL0 = 0x0. (If sensor AR0239, CTRL0 = 0x4; If sensor IMX327, CTRL0 = 0x8)
CTRL1 = 0x3.
DATA_IDS_1 = 0x2b.

2.5.1.2 frame_x2_ddr mode (2IDs--HDR mode)

For this mode:

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Configure sw_ibuf_op_mode = 8.
For example: raw10, lanex4
CTRL0 = 0x800.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.
Configure ISP MI register for address and size:
RAW0_WR_BASE = "DMATX0 base address in DDR".
RAW0_WR_SIZE = "pic_width * pic_height * 1.5".

2.5.2 line_x2_ddr_mode (2IDs--HDR mode)

For this mode:
Configure sw_ibuf_op_mode = 9.
For example: raw10, lanex4
CTRL0 = 0x900.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.
Configure ISP_MI register for address and size:
RAW0_WR_BASE = "DMATX0 base address in DDR".
RAW0_WR_SIZE = "pic_width * pic_height * 1.5".

2.5.2.1 line_x2_noddr mode (2IDs--HDR mode)

For this mode:
Configure sw_ibuf_op_mode = 10.
For example: raw10, lanex4
CTRL0 = 0xa00.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.

2.5.2.2 user mode

For this mode:
Configure sw_ibuf_op_mode = 3.
User defined mode. All DMATX and DMARX are available.

2.5.2.3 raw_rdback_framex1 mode

For this mode:
Configure sw_ibuf_op_mode = 4.
For example: raw10, lanex4 (all DMATX configurable, recommend DMATX2)
CTRL0 = 0x400.
CTRL1 = 0x3.
DATA_IDS_1 = 0x2b.
RAW2_WR_CTRL = 0x101.
Configure ISP_MI register for address and size:
MI_WR_CTRL2 = 0x1.
RAW2_WR_BASE = "DMATX2 base address in DDR".
RAW2_WR_SIZE = "pic_width * pic_height*1.5".
RAWS_RD_BASE = RAW2_WR_BASE.
Then, the time to start DMARXS is up to the user (maybe DMATX2 frame end):
Configure CTRL0 = 0x401.

2.5.2.4 raw_rdback_framex2 mode (HDR mode)

For this mode:
Configure sw_ibuf_op_mode = 5.
For example: raw10, lanex4 (all DMATX configurable, recommend DMATX2 and DMATX0)
CTRL0 = 0x500.
CTRL1 = 0x103.
DATA_IDS_1 = 0x6b2b.
RAW2_WR_CTRL = 0x101.
RAW0_WR_CTRL = 0x201.
Configure ISP_MI register for address and size:
MI_WR_CTRL2 = 0x3.
RAW2_WR_BASE = "DMATX2 base address in DDR".
RAW2_WR_SIZE = "pic_width * pic_height * 1.5".

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RAW0_WR_BASE = "DMATX0 base address in DDR".
RAW0_WR_SIZE = "pic_width * pic_height * 1.5".
RAWS_RD_BASE = RAW2_WR_BASE.
RAW0_RD_BASE = RAW0_WR_BASE.
Then, the time to start DMARXS is up to the user (maybe both DMATX2 and DMATX20 frame end):
Configure CTRL0 = 0x501.

2.5.3 MI

Three are 4 points to note:

1) The signal sw_mi_wr_init_offset_en (address offset 0x1400[21]) in MI_WR_CTRL register needs to be set to 1, otherwise, the address of MI will not be updated.
2) If output address need ping-pong, the signal sw_mp_wr_auto_upd (address offset 0x1400[13]) in MI_WR_CTRL register needs to be set to 1.
3) The signal sys_mi_cfg_upd (address offset 0x1404[4]) in MI_WR_INIT register needs to be set to 1 after all MI registers configuration complete when the 1st frame.
4) The respective force update (sys_dbrself_force_upd, sys_gainself_force_upd, sys_bay3dself_force_upd) is added to the register MI_WR_CTRL2 (address offset 0x1800), can be used to update the enable signal and shadow address.

2.5.4 HDRMGE

1) Global register configuration:
   Enable and select mode, choose gain or Anti-gain, other configurations such as curves is recommended to use the default typical value.
2) Curve configuration:
   L curve: The first quarter is divided into 16 sections, other is equal to 1023.
   S curve: Middle 1/2 divided into 16 sections, other is equal to 1023.
   E curve: Last 1/2 divided into 16 segments, other is equal to 0.
3) Software configuration:
   sw_hdr_mode: 0: normal; 1: framex2.
   sw_hdr_lightz = 0.1 * (short_gain / 16) ^ 3).
   sw_hdr_gain2 = 1.
   sw_hdr_gain1 = exposure_L / exposure_M; (Anti-gain1 is 1/gain1).
   sw_hdr_gain0 = exposure_L / exposure_S; (Anti-gain0 is 1/gain0).
   sw_hdr_lightzone = 0.1 * (short_gain / 16) ^ 3.
   light_zone = img_short > sw_hdr_lightzone = 0.1 * (short_gain / 16) ^ 3.

2.5.5 BAY3D

BAY3D related configuration:

1) Configure sw_bay3d_en_i (address offset 0x2c00[0]) to 1 to enable BAY3D module. When BAY3D module is enabled, BAYNR module must be enabled too.
2) When BAY3D module is enabled, sys_raw3d_fst_frame (address offset 0x0404[27]) must be configured to 1 in the 1st frame, which is auto clear.
3) When sw_bay3d_bypass_en (address offset 0x2c00[1]) is configured to 1, BAY3D all data bypass. When sw_bay3d_lobypass_en (address offset 0x2c00[3]) is configured to 1, BAY3D only low frequency data bypass. When sw_bay3d_hibypass_en (address offset 0x2c00[2]) is configured to 1 and sw_bay3d_lobypass_en is configured to 0, BAY3D only high frequency data bypass.
4) High or low frequency filter in each level in BAY3D module can be enabled independently, which depended on tuning. The weight between high and low frequency can be adjusted by configuring sw_bay3d_wgtmix_en (address offset 0x2c0c[12]) and sw_bay3d_hiwgt_opt_en (address offset 0x2c0c[0]) to 1 when sw_bay3d_hibypass_en & sw_bay3d_lobypass_en == 0.
5) When sw_bay3d_lo4x4_en (address offset 0x2c0c[4]) or sw_bay3d_lo4x8_en (address offset 0x2c0c[3]) is 1, BAY3D low frequency down sampling mode is enable, sw_bay3d_lo4x4_en == 1 means 4x4 down sampling, sw_bay3d_lo4x4_en == 0 && sw_bay3d_lo4x8_en == 1 means 4x8 down sampling, sw_bay3d_lo4x4_en == 0 && sw_bay3d_lo4x8_en == 0 means 8x8 down sampling. When sw_bay3d_lo4x4_en | sw_bay3d_lo4x8_en == 1, BAY3D module supports maximum 4224pixel input image width; When sw_bay3d_lo4x4_en | sw_bay3d_lo4x8_en == 0, BAY3D module supports

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maximum 2112pixel input image width. Whether to enable BAY3D low frequency down sampling mode and the window size of down sampling are depended on tuning.

6) When sw_bay3d_bwsaving_en (address offset 0x2c00[13], defaults to 0) is configured to 1, BAY3D module will reduce 1/4 MI data bandwidth, which is recommended for developers to use it. Similarly, sw_bay3d_bwopt_gain_dis (address offset 0x2c0c[2], defaults to 0) will reduce 1/16 gain data bandwidth by default.
7) When sw_bay3d_glbpk_en (address offset 0x2c00[11]) is configured to 1, sw_bay3d_glbpk2 (address offset 0x2c08[27:0]) must also be configured to calculate global gain. To ensure noise reduction effect, sw_bay3d_glbpk_en is recommended to be 0.
8) BAY3D module does NOT support soft mode in the current version.
9) When BAY3D module is disabled, sw_bay3d_gain_en (address offset 0x3a00[16]) must be configured to 0.
10) The abscissa difference between two adjacent points must be the power of 2 in all sigma curve configuration. SigmaX curve configuration includes sw_bay3d_sigX_x0~sw_bay3d_sigX_x15, sw_bay3d_sigX_y0~sw_bay3d_sigX_y15, where X can be 0~2.
11) Gaussian filter in BAY3D module is enabled when sw_bay3d_higaus_bypass_en (address offset 0x2c00[5]) is 0 by default. When Gaussian filter is enabled, the priority of several modes is shown as below:
    a. 5x5 all channel filter with Bayer pattern balance correction, enabled when sw_bay3d_hichncor_en (address offset 0x2c0c[1]) is configured to 1.
    b. 3x3 all channel filter, enabled when sw_bayer_higaus3_mode (address offset 0x2c0c[10:9]) is NOT configured to 0.
    c. 5x5 single channel filter, equivalent to 3x3 single channel filter, enabled when sw_bay3d_hichnsplit_en (address offset 0x2c00[7]) is configured to 1.
    d. 5x5 all channels filter, enabled when sw_bay3d_hichnsplit_en (address offset 0x2c0c[11]) is configured to 1.
    e. 5x7 all channels filter, enabled when sw_bay3d_hichnsplit_en is 0.

BAY3D MI related configuration:

1) Configure reference IIR frame read/write base address, sw_bay3d_iir_rd_base (address offset 0x19b0) and sw_bay3d_iir_wr_base (address offset 0x19a0). The force update signal of BAY3D IIR MI read is configured to address offset 0x1800[7], the force update signal of BAY3D IIR MI write is configured to address offset 0x1800[22].
2) Configure BAY3D IIR MI read width, sw_acq_h_size_bay3dmi (address offset 0x0410[31:16]), whose unit is pixel and must be 16pixel aligned. When sw_acq_h_size_bay3dmi is 0, module will auto calculate inside, which is recommended for developers. The calculation formula inside is: sw_acq_h_size_bay3dmi = hsize_16align * 2 * (sw_bay3d_bwsaving_en * 3 / 4 + !sw_bay3d_bwsaving_en * 1) + !sw_bay3d_glbpk_en * (hsize_16align >> 3). Here hsize_16align = ((sw_acq_h_size + 15) >> 4) << 4, where sw_acq_h_size is configured to address offset 0x414[14:0].
3) Configure BAY3D IIR MI write size, sw_bay3d_iir_wr_size (address offset 0x19a4), whose unit is byte and must be 16byte aligned. The calculation formula is: sw_bay3d_iir_wr_size = (((sw_acq_h_size_bay3dmi * 2byte * sw_acq_v_size / 2) + 15) >> 4) << 4), where sw_acq_v_size is configured to address offset 0x0414[13:0].
4) Configure BAY3D current frame (CUR for short) MI read/write base address, sw_bay3d_cur_rd_base (offset 0x19d0) and sw_bay3d_cur_wr_base (address offset 0x19c0). The force update signal of BAY3D CUR MI read is configured to address offset 0x1800[7], the force update signal of BAY3D CUR MI write is configured to address offset 0x1800[23].
5) Configure BAY3D CUR MI read/write virtual stride, sw_bay3d_cur_rd_length (address offset 0x19d4) and sw_bay3d_cur_wr_length (address offset 0x19c8), whose unit is byte and must be 16byte aligned. The calculation formula is: sw_bay3d_cur_rw_length = (((hsize_16align * 2 * (sw_bay3d_bwsaving_en * 3 / 4 + !sw_bay3d_bwsaving_en * 1) * 2byte + hdr_en * (hsize_16align >> 3) * 2byte +15) >> 4) << 4). Here hdr_en = sw_hdrmge_en_i == 1 || sw_isp_ob_predgain > 0, where sw_hdrmge_en_i is configured to address offset 0x3800[0], sw_isp_ob_predgain is configured to address

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offset 0x3060[15:0].

6) Configure line number of BAY3D CUR MI WRAP read/write clamp, sw_bay3d_mi_safe_cnt (address offset 0x2cc8[22:16]). The calculation formula is: sw_bay3d_mi_safe_cnt = sw_bay3d_lo4x8_en | sw_bay3d_lo4x4_en == 0 ? 64 : 32.
7) Configure BAY3D CUR MI read/write size, sw_bay3d_cur_wr_size (address offset 0x19c4) and sw_bay3d_cur_rd_frmsize (address offset 0x19dc), whose unit is byte and must be 16byte aligned. The calculation formula is sw_bay3d_cur_rw_size = (((sw_bay3d_cur_rw_length * sw_bay3d_mi_safe_cnt / 2) + 15) >> 4) << 4).
8) Configure BAY3D downscale MI read/write base address, sw_bay3d_ds_rd_base (address offset 0x19f0) and sw_bay3d_ds_wr_base (address offset 0x19e0). The force update signal of BAY3D downscale MI read is configured to address offset 0x1800[7], the force update signal of BAY3D downscale MI write is configured to address offset 0x1800[24].
9) Configure BAY3D CUR downscale MI write size, sw_bay3d_ds_wr_size (address offset 0x19e4), whose unit is byte and must be 16byte aligned. The calculation formula is: sw_bay3d_ds_wr_size = (((hsize_16align * vsize_16align / (sw_bay3d_lo4x4_en ? 16 : (sw_bay3d_lo4x8_en ? 32 : 64)) * 2 + 15) >>4) <<4), where vsize_16align = (((sw_acq_v_size + 15) >> 4) << 4).
10) BAY3D CUR MI read will start when the number of lines of input image reaches sw_bay3d_mi2cur_linecnt (address offset 0x2c08[6:0], defaults to 20).
11) The force update signal of BAY3D MI must be configured after the configuration of sw_bay3d_en_i.

2.5.6 HDR-DRC

HDR-DRC global register configuration:
Enabling and select mode, lgscl and lgscl_inv, other configurations such as curves is recommended to use the default typical value.

2.5.7 DEBAYER

The DEBAYER module has 4 important register configurations:

1) sw_debayer_en: When it is 0, it corresponds to black and white mode; When it is 1, it corresponds to RGB mode.
2) sw_debayer_filter_g_en: When it is 0, G filter module will be bypassed.
3) sw_debayer_clip_en: Determine whether the horizontal and vertical interpolation result will clip according to the maximum value in the window when G interpolation.
4) The rest of the configuration is to adjust the algorithm effect. The following points need to be noted:
   - sw_debayer_filter1_coe and sw_debayer_filter2_coe is a signed number, the value range is -16~15.

coe1	0	coe2
coe3	0	coe4
coe1	0	coe2

Filter1

coe1	coe2	coe1
coe3	coe4	coe3
coe1	coe2	coe1

Filter2

Fig. 2-8 sw_debayer_filter1/2_coe arrangement

   - The step of sw_debayer_max_ratio is 1/4, the step of sw_debayer_dist_scale is 1/8, the step of sw_debayer_thed0 and sw_debayer_thed1 is 1/32.
   - sw_debayer_guide_gaus_0/sw_debayer_guide_gaus_1/sw_debayer_guide_gaus_2 respectively represent the center point of the filtering coefficient, four points on the upper and lower left and right sides, and four points on the 45-degree angle. The sum of the nine coefficients should be guaranteed to be 256.
   - sw_debayer_ce_gaus_0/sw_debayer_ce_gaus_1/sw_debayer_ce_gaus_2 respectively represent the center point of the filtering coefficient, four points on the upper and lower left and right sides, and four points on the 45-degree angle. The sum

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of the nine coefficients should be guaranteed to be 256.

- sw_debayer_alpha_gaus_0/sw_debayer_alpha_gaus_1/sw_debayer_alpha_gaus_2 respectively represent the center point of the filtering coefficient, four points on the upper and lower left and right sides, and four points on the 45-degree angle. The sum of the nine coefficients should be guaranteed to be 256.
- The most significant bit of sw_debayer_exp_shift represents the direction of the shift (0 for right, 1 for left). The remaining bits represent the number of the shift.

2.5.8 CCM

1) Set sw_ccm_en_i to 1, open CCM module, otherwise, CCM module will be close, and data path will be bypassed.
2) Signals sw_ccm_coeff0_r~sw_ccm_coeff2_b are CCM 3x3 matrix parameters. These nine parameters are all 11bit signed numbers which have 7bit integer. The range is [-8,7.992].
3) Signals sw_ccm_offset_r, sw_ccm_offset_g, and sw_ccm_offset_b are offsets in calculation, which are 12bit signed integers.
4) Signals sw_ccm_coeff0_y~sw_ccm_coeff2_y are RGB2Y parameters, which are 11bit signed number with 7bit integer, range from -2 to 1.992.
5) The brightness interpolation curve in CCM mode supports symmetric and asymmetric modes:
   When sw_ccm_asym_adj_en is configured to 0, CCM module uses symmetric interpolation mode, sw_ccm_alp_y0~sw_ccm_alp_y16 are the 17 vertices of the 16 segments of alpha interpolation curve, and sw_ccm_bound_bit is the alpha power exponent configuration of inflexion of interpolation curve. The value of the inflection point is 2 ^ sw_ccm_bound_bit, sw_ccm_bound_bit is ranged from 4 to 10.
   When sw_ccm_asym_adj_en is configured to 1, CCM module uses asymmetric interpolation mode, sw_ccm_alp_y0~sw_ccm_alp_y8 are the 9 vertices of the 8 segments of the left alpha interpolation curve, sw_ccm_alp_y9~sw_ccm_alp_y17 are the 9 vertices of the 8 segments of the right alpha interpolation curve, and sw_ccm_right_bit is the alpha power exponent configuration of the right inflexion of interpolation curve. The value of the inflection point is 2 ^ sw_ccm_right_bit, sw_ccm_right_bit is ranged from 3 to 11.

2.5.9 GAMMA_OUT

1) The GAMMA_OUT module is enabled when sw_gamma_out_en is configured to 1. This module is realized by interpolation.
2) When sw_gamma_out_equ is configured to 1, the segment length of x orientation is equal and the curve uses 32 segments to interpolate.
3) When sw_gamma_out_equ is asserted to 0, the segment length of x orientation is not equal and the curve uses 44 segments to interpolate.

2.5.10 DEHAZE

1) Configure sw_dhaz_en to 1 to enable DEHAZE module.
2) When sw_dhaz_en and sw_dhaz_dc_en is configured to 1, the dark channel function is enabled.
3) When sw_dhaz_en and set sw_dhaz_hist_en is configured to 1, the histogram equalization function is enabled. If sw_dhaz_para_en is also configured to 1, sw_dhaz_hist_scale needs to be configured too.
4) When sw_dhaz_enhance_en is configured to 1, sw_dhaz_enhance_value and sw_dhaz_enhance_chroma need to be configured too.
5) Configure sw_dhaz_stab_fnum to control the number of iterative frames for histogram IIR, the internal sigma values will be gradually converged to a certain value according to the configuration, and the minimum value of sw_dhaz_stab_fnum is 1.
6) Configure sw_dhaz_iir_pre_wet to control the number of iterative frames for dark channel IIR, the internal weight values will be gradually converged to a certain value according to the configuration, and the minimum value of sw_dhaz_iir_pre_wet is 1.
7) If user needs adaptive dehaze parameter, configure sw_dhaz_cfg_alpha to 0, otherwise sw_dhaz_cfg_air, sw_dhaz_cfg_wt, sw_dhaz_cfg_tmax and sw_dhaz_cfg_gratio need to be configured by software. There is no adaptive parameter in enhance mode, all the parameters need to be configured by software.

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2.5.11 3DLUT

1) The 3DLUT module is enabled when sw_lut3d_en is configured to 1.
2) The LUT of this module is updated by configuring sw_lut3d_lut_update_en to 1.

2.5.12 YNR

1) Configure sw_ynr_en to 1 to enable YNR module.
2) To facilitate debugging effects, each internal module has bypass mode. The corresponding register is sw_ynr_xxx_bypass.
3) The remaining configurations can be configured by default, or use reference configuration after tuning to achieve the best graphic quality.
4) If sw_ynr_thumb_mix_cur_en is configured to 1 to enable thumbnail, the minimum input resolution is 114x82 in normal mode and 126x162 in big mode.

2.5.13 CNR

1) Configure sw_cnr_en to 1 to enable CNR module.
2) YNR, CNR, SHARP module must be enabled or disabled uniformly.
3) CNR module is not support YUV422 format in this version, so sw_cnr_yuv_422 is always configured to 0.
4) The remaining configurations can be configured according to the default values, or use reference configuration after tuning to achieve the best graphic quality.

2.5.14 SHARP

1) Configure sw_sharp_en to 1 to enable SHARP module, otherwise it is bypass mode.
2) The value of sw_sharp_luma_dx1~sw_sharp_luma_dx7 is 2^n, the sum of the seven coefficients should be guaranteed to be 1024.
3) The signal sw_sharp_pbf_coef_0, sw_sharp_pbf_coef_1, sw_sharp_pbf_coef_2 respectively represent the center point of the filtering coefficient, 4 points on the upper and lower left and right sides, and 4 points on the 45-degree angle. The sum of the nine coefficients should be guaranteed to be 128.
4) The signal sw_sharp_bf_coef_0, sw_sharp_bf_coef_1, sw_sharp_bf_coef_2 respectively represent the center point of the filtering coefficient, 4 points on the upper and lower left and right sides, and 4 points on the 45-degree angle. The sum of the nine coefficients should be guaranteed to be 128.
5) The sum of sw_sharp_gaus_coef_0, sw_sharp_gaus_coef_1, sw_sharp_gaus_coef_2, sw_sharp_gaus_coef_3, sw_sharp_gaus_coef_4 and sw_sharp_gaus_coef_5 should be guaranteed to be 128 with different weights.

2.5.15 GAIN

1) Configure sw_gain_en to 1 to enable global gain module.
2) Configure sw_mge_gain_en, sw_lsc_gain_en, sw_adrc_gain_en, sw_b3dnr_gain_en, sw_dhaz_gain_en when the corresponding module is enabled. When these signals are not be configured, GAIN module will also enable the corresponding gain according to the enable of each module adaptively.
3) The signal sw_gain0 is a reused configuration. When sw_mge_gain_en is configured to 1, sw_gain0 is composed of integer of 12 bits and decimal of 6 bits, which is used for the initial value of weight0 of gain of HDR-MGE module. When sw_mge_gain_en is configured to 0, the upper 12 bits of sw_gain0 is the integer part of sw_gain_init, and the lower 6 bits is the decimal part of sw_gain_init, which means sw_gain_init = {sw_gain0, 3'b0}.
4) The signal sw_gain1 and sw_gain2 is valid when sw_mge_gain_en is configured to 1.

2.5.16 AF

1) Configure sw_rawaf_en to 1 to enable RAWAF module.
2) When sw_rawaf_viir_en is configured to 1, RAWAF module will open V1channel.
3) When sw_rawaf_hiir_en is configured to 1, RAWAF module will open H1 channel.
4) When sw_gamma_en is configured to 1, sw_rawaf_viir_en must be configured to 1 too.
5) If sw_rawaf_v1_fir_sel is 0, V1 channel will get old Sobel output, otherwise V1 channel will get new VIIR+VFIR output.
6) When sw_rawaf_ae_mode is configured to 1, RAWAF module will enable 5x5 luminance mean statistics, which is reused in RAWAE_BIG module.

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2.5.17 AE

Two versions of AE are named RAWAE_BIG and RAWAE_LITE here. The mean of reading back statistic is different. RAWAE_LITE uses normal method which give an address and then read back. RAWAE_BIG read the fix address RO_MEAN_BASE_ADDR 225 times. RAWAE_BIG supports 15x15 window grid, it still supports 4 separated windows.

1) RAWAE module needs configure as follows:
   - Configure window size, window offset, and so on.
   - Configure sw_aemeas_en to 1 to enable RAWAE module.
   - Waiting for interruption of RAWAE module.
   - Read back the statistics data when the interruption is available.
   - Configure sw_aemeas_done to 1 to clear this signal and restart RAWAE module.
   - Waiting for the interruption of next frame.
2) It is a large amount of readback data. When the statistics data of the 1st frame is ready but not completely readback during vblank of 1st frame until the middle of the 2nd frame, if the enable of statistics is configured at this time, RAWAE module will get statistics data at the 3rd frame, and generate interruption after the statistics data of the 3rd frame is ready. When the statistics data of the 1st frame is ready and completely readback during vblank of 1st frame, if the enable of statistics is configured at this time, RAWAE module will get statistics data at the 2nd frame.

Here have some constraints for AE:

3) The sub-window size and offset must even. For non-independent sub-windows, it is required that the data of last two lines of a frame cannot be used in statistics. Each sub-window size is at least 16x4, and each sub window cannot exceed the right boundary and lower boundary of the input image after configuration.
4) The statistics of RAWAE_LITE module is stored at register, while the statistics of RAWAE_BIG module is stored at DDR, so it is necessary to use a for loop to read RAWAE_BIG_RO_MEAN_BASE_ADDR repeatedly. RAWAE_BIG module supports RAM address offset to get the statistics in a certain address by configuring sw_ram_offset.
5) One window in RAWAE_BIG module should be configured by using coordinate directly instead of window size, whose enable is configured in sw_rawae_big_wnd1. The statistics of this window is stored without division operation, so it needs to divide by window size manually. The maximum window size is 2kx1k. If statistics overflow, all the bits of statistics will be 0xf.
6) RAWAE_LITE module supports 1x1 and 5x5 window size, RAWAE_BIG module supports 1x1, 5x5, 15x15 window size.

2.5.18 AWB

1) Data Pre-Process
   RAWAWB input data is 12bit raw format and the input picture could crop by the crop module. The cropped picture should align at the down sample window size, 4 or 8 configurable, and the hardware would guarantee this by force. The RGB data down sampled from RAW data and Y data converted from RGB data will do some limitation (the limitation is configurable) and then output to detection module.
2) White Point Detection
   There are three region white point detection method, XY region, UV region and YUV region. These three methods will do and logic to catching the white point. The enable of three detection method is configurable.
3) Block Measurement
   The down sampled picture would divide into 5x5 blocks and then accumulate each block input data. The input data could be down sampled data, XY white point data or UV white point data and it is configured by sw_rawawb_blk_measure_mode.
4) Data Read Back
   All measurement information could read back to software by AHB bus. When the measurement is over the hardware will pull up the sw_rawawb_meas_done signal. And then the software could read back all the information. The software should pull the signal down by setting this signal to 1 when read is over. The next frame measurement is valid only if the sw_rawawb_meas_done is 0 before the next frame start.

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2.5.19 HIST

Two versions of HIST are named RAWHIST_BIG and RAWHIST_LITE here. The mean of reading back statistic is same for them. RAWHIST_BIG module needs to read the fix address RO_BASE_BIN 256 times when read back, and 64 times for RAWHIST_LITE module

1) RAWHIST module needs configure as follows:
   - Configure window size, window offset, and so on.
   - Configure sw_aehist_en to 1.
   - Waiting for interruption of RAWHIST module.
   - Read back the statistics data when the interruption is available.
   - Configure sw_aehist_done to 1 to clear this signal and restart RAWAE module.
   - Waiting for the interruption of next frame.

Here have some constraints for HIST:

2) The sub-window size and offset must even.
3) When user sets the weights of RAWHIST_BIG, sw_config_wram_en needs to be configured to 1 ahead.
4) The coefficient sw_rawae_gcc needs half because there are two G (Gr, Gb) in the RAW2Y formula.

The readback data of 3A are shown as follows:

Table 2-3 3A readback data

Module	Address	Count	Data
RAWAF	0x4DE0	50	Count: 0 - 24 {out_hiir_wnd_data[count]} Count: 25 - 49 {out_viir_wnd_data[count - 25]}
RAWAWB	0x5700	63	Index = count / 2 Count: 0-49 {sum_blk_g[10:0][index], sum_blk_r[20:0][index]} (even count) {1'b0, sum_blk_b[20:0][index], sum_blk_g[20:11][index]} (odd count) Count: 50-62 {2'b0, sum_blk_wp[13:0][count*2+1], 2'b0, sum_blk_wp[13:0][count*2]}
RAWAE_BIG	0x4480	225	{mean_data_channelr, mean_data_channelb, mean_data_channelg}
RAWAE_LITE	0x4510	25	{mean_data_channelr, mean_data_channelb, mean_data_channelg}
HIST_BIG	0x4880	256	{4'b0, bin_data}
HIST_LITE	0x4980	64	{4'b0, bin_data}

2.5.20 IRQ

There are three important interrupt registers in ISP, one is ISP_MIS (address offset 0x05c4), one is ISP3A_MIS (address offset 0x05d8), the other is MI_MIS (address offset 0x1500).

The following chart shows the interrupt sequence between several interrupts:

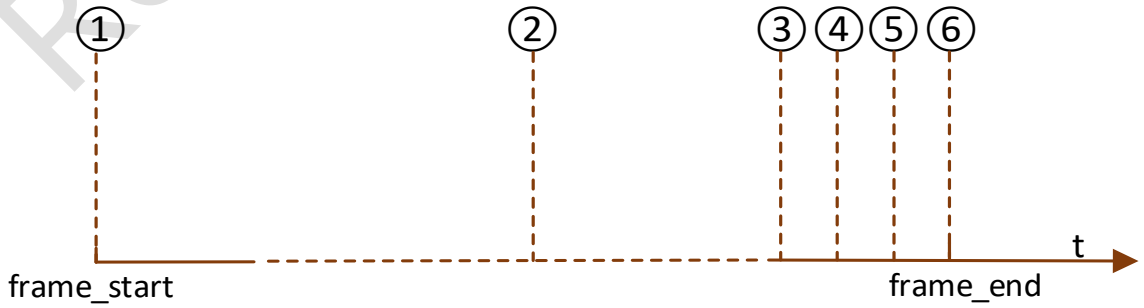

Fig. 2-9 Interrupt Sequence

The meanings of the above numerical symbols are as follows:

Table 2-4 Meaning of IRQ

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No.	Interrupt name	Register name	Meaning
1	MIS_V_START	ISP_MIS	start edge of v_sync, pull up time is the same as first pixel valid is ISP
2	MIS_RAWXX_DONE	ISP3A_MIS	3A module done signal
3	MIS_FRAME_IN	ISP_MIS	INFORM module frame end signal
4	MIS_HDR_DONE	ISP_MIS	HDR module frame end signal
5	MIS_FRAME_OUT	ISP_MIS	ISP module frame end signal
6	mp_frame_end	MI_MIS	MI module frame end signal

MIS_RAWXX_DONE of above table indicates different 3A interrupts, which interrupt time are determined by the size of the window in different 3A module.

2.5.21 SHD_REG

All shadow registers are list in following table:

Table 2-5 Shadow Register List

Signal	In which module	Registers addr	Bit	Meaning
sw_csi_raw0_wr_en_shd	MIPI	0x1C40	31	Raw0_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to DDR. 1'b1: Enable the channel 1'b0: Disable the channel
sw_csi_raw1_wr_en_shd	MIPI	0x1C50	31	Raw1_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to DDR. 1'b1: Enable the channel 1'b0: Disable the channel
sw_csi_raw2_wr_en_shd	MIPI	0x1C60	31	Raw2_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to DDR. 1'b1: Enable the channel 1'b0: Disable the channel
sw_csi_raw3_wr_en_shd	MIPI	0x1C70	31	Raw3_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to DDR. 1'b1: Enable the channel 1'b0: Disable the channel
path_enable_in	MI	0x1474	3:0	path_enable shadow register for module MI_IN (former raw_enable_in, jpeg_enable_in, sp_enable_in, mp_enable_in)
path_enable_out	MI	0x1474	19:16	path_enable shadow register for module MI_OUT (former raw_enable_out, jpeg_enable_out, sp_enable_out, mp_enable_out)
sw_mp_wr_y_base_shd	MI	0x1478	31:4	Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_mp_wr_y_siz	MI	0x147C	28:4	Size of main picture Y component ring

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Signal	In which module	Registers addr	Bit	Meaning
e_shd				buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_y_offs_cnt_shd	MI	0x1480	28:4	Current offset counter of main picture Y component, JPEG or raw data ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_y_irq_offs_shd	MI	0x1484	28:4	Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cb_base_shd	MI	0x1488	31:4	Base address of main picture Cb component ring buffer. --- MI_MP_WR_CB_BASE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cb_size_shd	MI	0x148C	27:4	Size of main picture Cb component ring buffer. --- MI_MP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cb_offs_cnt_shd	MI	0x1490	27:4	Current offset counter of main picture Cb component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_base_shd	MI	0x1494	31:4	Base address of main picture Cr component ring buffer. --- MI_MP_CR_BASE_AD_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_size_shd	MI	0x1498	27:4	Size of main picture Cr component ring buffer. --- MI_MP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_offs_cnt_shd	MI	0x149C	27:4	Current offset counter of main picture Cr component ring buffer for address generation. Note: Soft reset will reset the contents to reset value.

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Signal	In which module	Registers addr	Bit	Meaning
				--- MI_MP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_base_shd	MI	0x14A0	31:4	Base address of self picture Y component ring buffer. --- MI_SP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_size_shd	MI	0x14A4	28:4	Size of self picture Y component ring buffer. --- MI_SP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_offs_cnt_shd	MI	0x14A8	28:4	Current offset counter of self picture Y component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cb_base_shd	MI	0x14B0	31:4	Base address of self picture Cb component ring buffer. --- MI_SP_WR_CB_BASE_AD_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cb_size_shd	MI	0x14B4	27:4	Size of self picture Cb component ring buffer. --- MI_SP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cb_offs_cnt_shd	MI	0x14B8	27:4	Current offset counter of self picture Cb component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cr_base_shd	MI	0x14BC	31:4	Base address of self picture Cr component ring buffer. --- MI_SP_WR_CR_BASE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cr_size_shd	MI	0x14C0	27:4	Size of self picture Cr component ring buffer. --- MI_SP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cr_offs_cnt_shd	MI	0x14C4	27:4	Current offset counter of self picture Cr component ring buffer for address generation. Note: Soft reset will reset the contents to reset value.

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Signal	In which module	Registers addr	Bit	Meaning
				--- MI_SP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_mp_wr_y_irq_offs2_shd	MI	0x15E4	28:4	Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_y_base_shd	MI	0x1634	31:4	Base address of bypass picture Y component ring buffer. --- MI_BP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_y_size_shd	MI	0x1638	28:4	Size of bypass picture Y component ring buffer. --- MI_BP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_y_offs_cnt_shd	MI	0x163c	28:4	Current offset counter of bypass picture Y component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_BP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_bp_wr_cb_base_shd	MI	0x1640	31:4	Base address of bypass picture Cb component ring buffer. --- MI_BP_WR_CB_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_cb_size_shd	MI	0x1644	27:4	Size of bypass picture Cb component ring buffer. --- MI_BP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_cb_offs_cnt_shd	MI	0x1648	27:4	Current offset counter of bypass picture Cb component ring buffer for address generation

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Signal	In which module	Registers addr	Bit	Meaning
				Note: Soft reset will reset the contents to reset value. --- MI_BP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_raw0_wr_base_shd	MI	0x182C	31:4	Base address of raw0 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw1_wr_base_shd	MI	0x183C	31:4	Base address of raw1 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw2_wr_base_shd	MI	0x184C	31:4	Base address of raw2 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw3_wr_base_shd	MI	0x185C	31:4	Base address of raw3 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw0_rd_base_shd	MI	0x1878	31:4	Base shadow address of raw0 rx data ring buffer
sw_raw1_rd_base_shd	MI	0x1888	31:4	Base shadow address of raw1 rx data ring buffer
sw_raws_rd_base_shd	MI	0x1898	31:4	Base shadow address of raws rx data ring buffer
dbr_wr_base_shd	MI	0x196C	31:4	Base address of mimux write data ring buffer. --- DBR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to DBR_WR_BASE register description for details.
dbr_rd_base_shd	MI	0x1978	31:4	Base shadow address of mimux read data ring buffer
gain_wr_base_shd	MI	0x1990	31:4	Base address of gain write data ring buffer. --- GAIN_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to GAIN_WR_BASE register description for details.

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Signal	In which module	Registers addr	Bit	Meaning
bay3d_wr_iir_base_shd	MI	0x19ac	31:4	Base address shadow register for bayer 3dnr iir write data ring buffer
bay3d_iir_rd_base_shd	MI	0x19b8	31:4	Base shadow address of bayer 3dnr iir read data ring buffer.
bay3d_cur_wr_base_shd	MI	0x19cc	31:4	Base address of bayer 3dnr current write data ring buffer. --- BAY3D_CUR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_CUR_WR_BASE register description for details.
bay3d_cur_rd_base_shd	MI	0x19d8	31:4	Base shadow address of bayer 3dnr current read data ring buffer.
bay3d_ds_wr_base_shd	MI	0x19ec	31:4	Base address of bayer 3dnr iir write data ring buffer. --- BAY3D_IIR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_IIR_WR_BASE register description for details.
bay3d_ds_rd_base_shd	MI	0x19f8	31:4	Base shadow address of bayer 3dnr down scale read data ring buffer.
sw_hdrmge_en_shd	HDRMGE	0x3800	31	HDR-Merge enable shadow
sw_hdrmge_each_raw_en	HDRMGE	0x3800	6	Enable each_raw merge for noise reduce
sw_hdrmge_mode	HDRMGE	0x3800	3:2	HDR-Merge mode 2'b00: Normal 2'b01: Framex2 2'b10: Framex3
sw_hdrmge_s_base	HDRMGE	0x3800	1	HDR-Merge hugemsk enable, shadow reg 1'b0: Long base method 1'b1: Short base method
sw_bay3d_en_shd	BAY3D	0x2C00	16	BAY3D enable shadow 1'b1: Enable 1'b0: Disable
sw_bay3d_bypass_en_shd	BAY3D	0x2C00	17	BAY3D data path bypass shadow 1'b1: Enable 1'b0: Disable
sw_bay3d_hibypass_en_shd	BAY3D	0x2C00	18	BAY3D high weight data path bypass shadow 1'b1: Enable 1'b0: Disable
sw_bay3d_lobypass_en_shd	BAY3D	0x2C00	19	BAY3D low weight data path bypass shadow 1'b1: Enable 1'b0: Disable

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Signal	In which module	Registers addr	Bit	Meaning
sw_bay3d_himed_bypass_en_shd	BAY3D	0x2C00	20	High weight calculate median filter bypass shadow 1'b1: Enable 1'b0: Disable
sw_bay3d_higaus_bypass_en_shd	BAY3D	0x2C00	21	High weight calculate Gaussian filter bypass shadow 1'b1: Enable 1'b0: Disable
sw_bay3d_hiabs_possel_shd	BAY3D	0x2C00	22	High weight calculate abs position select shadow 1'b0: Difference->median->Gaussian->abs 1'b1: Difference->median->abs->Gaussian
sw_bay3d_hichnsplit_en_shd	BAY3D	0x2C00	23	High weight calculate Gaussian filter GRBG 4 channel split enable shadow 1'b1: 4 channels 3x3 Gaussian 1'b0: 1 channel 5x7 Gaussian
sw_bay3d_lomed_bypass_en_shd	BAY3D	0x2C00	24	Low weight calculate median filter bypass shadow 1'b1: Enable 1'b0: Disable
sw_bay3d_logaus5_bypass_en_shd	BAY3D	0x2C00	25	Low weight calculate Bayer Gaussian filter bypass shadow 1'b1: Enable 1'b0: Disable
sw_bay3d_logaus3_bypass_en_shd	BAY3D	0x2C00	26	Low weight calculate 3x3 Gaussian filter bypass shadow 1'b1: Enable 1'b0: Disable
sw_bay3d_glbpk_en_shd	BAY3D	0x2C00	27	Global pk enable shadow 1'b1: Global pk from sw_bay3d_glbpk2 1'b0: Local pk from DDR
sw_bay3d_ack_frm_pro_en_shd	BAY3D	0x2C00	28	Small v_blank protect enable 1'b1: Enable 1'b0: Disable Read shadow
sw_bay3d_bwsaving_en_shd	BAY3D	0x2C00	29	Bandwidth saving optimise shadow 1'b1: Optimise 1'b0: No optimise
sw_bay3d_soft_mode_shd	BAY3D	0x2C00	30	Software calculate low weight shadow 1'b1: Backdoor enable for software calculate low weight 1'b0: Hardware calculate low weight
sw_ccm_en_shd	CCM	0x0700	31	Shadow of CCM module enable

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Signal	In which module	Registers addr	Bit	Meaning
sw_ccm_enh_adj_en_shd	CCM	0x0700	29	Shadow of CCM color enhance adjust enable
sw_ccm_asym_adj_en_shd	CCM	0x0700	28	Shadow of asymmetrical curve for luminance adjust enable
sw_hdrdrc_en_shd	HDRDRC	0x3900	31	HDRTMO enable shadow, read back
sw_pre_mem_ddr_wr_en_shd	HDRDRC	0x3900	6	last frame pre memory data write to DDR enable shadow
sw_adrc_compress_scl	HDRDRC	0x3904	26:14	[2,11] scale plgmax range(0~24576) for trans compress
sw_adrc_bilat_soft_shd	HDRDRC	0x391c	29:16	{3,11},soft_thd constrain bilateral luminance for clip(org_luma-soft_thd,org_luma+soft_thd), shadow reg
sw_adrc_enable_soft_shd	HDRDRC	0x391c	31	high valid, enable soft_thd constrain bilateral luminance for clip(org_luma-soft_thd,org_luma+soft_thd), shadow reg
sw_adrc_gain_y0~g16	HDRDRC	0x3920	31:0	curve_gain2raw y0~y16, {3,10}
sw_adrc_compress_y0~y16	HDRDRC	0x3944	31:0	curve_compress y0~y16
sw_debayer_en_shd	DEBAYER	0x2500	24	The shadow register of sw_debayer_en
sw_debayer_filter_g_en_shd	DEBAYER	0x2500	25	The shadow register of sw_debayer_filter_g_en
sw_gamma_out_en_shd	GAMMA_OUT	0x0900	31	sw_gamma_out_en_shd
sw_dhaz_en_shd	DHAZ	0x3C00	31	Dehaze enable shadow
hist_wr0~hist_wr63	DHAZ	0x3CA8	31:0	Soft write hist rgb reg0~reg63 data, shadow read
sw_dhaz_dc_en_shd	DHAZ	0x3D00	4	Dehaze dark channel enable shadow
sw_dhaz_hist_en_shd	DHAZ	0x3D00	8	Dehaze hist equalization enable shadow
sw_dhaz_hpara_en_shd	DHAZ	0x3D00	12	Dehaze hist parameter enable shadow
sw_dhaz_air_lc_shd	DHAZ	0x3D00	16	Dehaze rgb channel separate shadow
sw_dhaz_enhance_en_shd	DHAZ	0x3D00	20	Dehaze enhance enable shadow
sw_dhaz_color_deviate_en	DHAZ	0x3D00	27	Color deviation enable, only use in enhance mode. 1'b0: Use sw_dhaz_enhance_chroma 1'b1: Correct color deviation in enhance mode
sw_dhaz_enh_luma_en	DHAZ	0x3D00	28	Luma curve enable in enhance mode. 1'b0: Use sw_dhaz_enhance_value 1'b1: Use luma curve
sw_lut3d_en_shd	3DLUT	0x3E00	31	sw_lut3d_en_shd

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Signal	In which module	Registers addr	Bit	Meaning
scale_hy_enable_shd	SELF_RESIZE	0x0C30, 0x1030	0	1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit
scale_hc_enable_shd	SELF_RESIZE	0x0C30, 0x1030	1	1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
scale_vy_enable_shd	SELF_RESIZE	0x0C30, 0x1030	2	1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
scale_vc_enable_shd	SELF_RESIZE	0x0C30, 0x1030	3	1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
scale_hy_up_shd	SELF_RESIZE	0x0C30, 0x1030	4	1'b1: Horizontal luminance up-scaling selected 1'b0: Horizontal luminance down-scaling selected
scale_hc_up_shd	SELF_RESIZE	0x0C30, 0x1030	5	1'b1: Horizontal chrominance up-scaling selected 1'b0: Horizontal chrominance down-scaling selected
scale_vy_up_shd	SELF_RESIZE	0x0C30, 0x1030	6	1'b1: Vertical luminance up-scaling selected 1'b0: Vertical luminance down-scaling selected
scale_vc_up_shd	SELF_RESIZE	0x0C30, 0x1030	7	1'b1: Vertical chrominance up-scaling selected 1'b0: Vertical chrominance down-scaling selected
scale_hy_shd	SELF_RESIZE	0x0C34, 0x1034	15:0	This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor.
scale_hcb_shd	SELF_RESIZE	0x0C38, 0x1038	15:0	This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor.
scale_hcr_shd	SELF_RESIZE	0x0C3C, 0x103C	15:0	This register is set to the horizontal r downscale factor or to the reciprocal of the horizontal r upscale factor.
scale_vy_shd	SELF_RESIZE	0x0C40, 0x1040	15:0	This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor.
scale_vc_shd	SELF_RESIZE	0x0C44, 0x1044	15:0	This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor.
phase_hy_shd	SELF_RESIZE	0x0C48, 0x1048	15:0	This register is set to the horizontal luminance phase offset
phase_hc_shd	SELF_RESIZE	0x0C4C, 0x104C	15:0	This register is set to the horizontal chrominance phase offset.

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Signal	In which module	Registers addr	Bit	Meaning
phase_vy_shd	SELF_RESIZE	0x0C50, 0x1050	15:0	This register is set to the vertical luminance phase offset.
phase_vc_shd	SELF_RESIZE	0x0C54, 0x1054	15:0	This register is set to the vertical chrominance phase offset.
isp_enable_shd	ISP_CTRL	0x5A8	0	ISP enable shadow register shows, if ISP currently outputs data (1) or not (0)
isp_inform_enable_shd	ISP_CTRL	0x5A8	1	Input formatter enable shadow register
isp_out_h_offs_shd	ISP_CTRL	0x5AC	13:0	Current vertical pic offset in lines
isp_out_v_offs_shd	ISP_CTRL	0x5B0	13:0	Current vertical pic offset in lines
isp_out_h_size_shd	ISP_CTRL	0x5B4	14:0	Current horizontal pic size in pixel
isp_out_v_size_shd	ISP_CTRL	0x5B8	13:0	Vertical pic size in lines
sw_sws_en_shd	SWS	0x1C	30	sw_sws_en_shd
sw_ldch_en_shd	LDCH	0x3B00	31	Module ldch enable signal,shadow.
sw_ynr_en_shd	YNR	0x2700	31	YNR enable shadow bit
sw_gain_en_shd	YNR	0x2700	30	GAIN enable shadow bit
sw_ynr_exgain_bypass_en_shd	YNR	0x2700	27	EXGAIN bypass enable shadow bit
sw_ynr_nlm11x11_bypass	YNR	0x2700	5	YNR NLM11x11 bypass bit
sw_ynr_flt1x1_bypass_shd	YNR	0x2700	4	YNR FT1X1 bypass bit
sw_ynr_lgft3x3_bypass_shd	YNR	0x2700	3	YNR LGFT3X3 bypass bit
sw_ynr_lbft5x5_bypass_shd	YNR	0x2700	2	YNR LBFT5X5 bypass bit
sw_ynr_bft3x3_bypass_shd	YNR	0x2700	1	YNR BFT3X3 bypass bit
sw_cnr_en_shd	CNR	0x2800	31	CNR enable shadow register
sw_gain_en_shd	CNR	0x2800	29	CNR gain enable shadow signal 1'b0: Disable 1'b1: Enable
sw_cnr_thumb_mode	CNR	0x2800	5:4	CNR down sampling mode 2'b00: 2x2 mode 2'b01: 4x4 mode 2'b10: 8x6 mode 2'b11: Reserved
sw_cnr_yuv422_mode	CNR	0x2800	2	Always be 0, reserved for later version. 3562 CNR can only support 420 mode.
sw_cnr_exgain_bypass	CNR	0x2800	1	External gain bypass enable signal, read back is shadow register. 1'b1: Bypass is enable, external gain value is fixed to sw_cnr_egain_mux. 1'b0: Bypass is disable, use external gain. Note: 1106 CNR does not support

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Signal	In which module	Registers addr	Bit	Meaning
				bypass disable.
sw_sharp_bypass_shd	Sharp	0x2900	31	Shadow of sw_sharp_bypass 1'b0: Not bypass 1'b1: Bypass
sw_sharp_en_shd	Sharp	0x2900	30	Shadow of sw_sharp_en 1'b0: Disable 1'b1: Enable
sharp_center_mode_shd	Sharp	0x2900	28	Shadow of sw_sharp_center_mode 1'b0: Disable 1'b1: Enable
sharp_exgain_bypass_shd	Sharp	0x2900	27	Shadow of sw_sharp_exgain_bypass 1'b0: Disable 1'b1: Enable
sw_sharp_radius_ds_mode_shd	Sharp	0x2900	26	Shadow of sharp radius strength down scale mode. 1'b0: Down scale is 128 1'b1: Down scale is 256
sharp_clk_dis_shd	Sharp	0x2900	16	Shadow of sw_sharp_clk_dis 1'b0: Not disable 1'b1: Disable

How to update the shadow register:

- You can choose to update through forced_upd and frame end update.
- The forced update is generally used before the start of a frame. The configuration mode is to enable ISP control, which is the 9th bit of address offset 0x0400.
- If you need to enable the end of frame update, you need to pull up the 8th bit of address offset 0x0400, otherwise it will not be updated by default.
- 10th bit of address offset 0x0400 can update shadow registers only one time while frame end is coming.

2.5.22 Multi-Sensor

Multi-sensor mainly uses the frame buffers to cache the data of the previous frame to solve the problem of previous frame data caching. The maximum resolution of frame buffer with different sensors is supported as follows.

1) sensor_mode0 (single sensor): the maximum resolution is 4224x3136

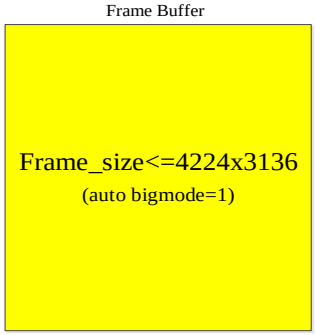

Fig. 2-10 Frame Buffer of Single Sensor

2) sensor_mode1 (dual-sensor with the same size): The previous frame data is stored by dividing the frame buffer in two, and the storage space is reduced by half. In normal mode, the maximum frame_size need to be small than or equal to 1920x1080, the max width of image is 1920. In big mode, frame_size need to be small than or equal to 3840x2160, the max width of image is 3840.

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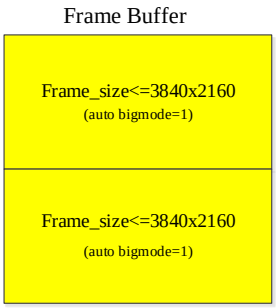

Figure 2-11 Frame Buffer of Dual-Sensor

3) sensor_mode2 (4 sensors with the same size): The previous frame data is stored by dividing the frame buffer in four, and the storage space is reduced by half. In normal mode, the maximum frame_size need to be small than or equal to 1280x800. In big mode, frame_size need to be small than or equal to 2688x1536.

Fig. 2-12 Frame Buffer of Four Sensors

4) sensor_mode4 (3 sensors with two small and one big): This mode supports two 4M (2688x1536) and one 8M (3840x2160) sensors, the previous frame data is stored by dividing the frame buffer in two parts of small size and one parts of big size.

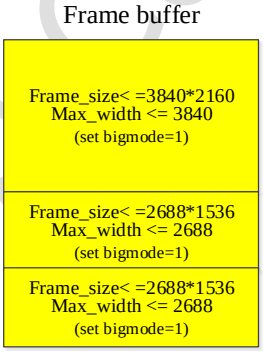

Fig. 2-13 Frame Buffer of Three Sensors

5) sensor_mode5 (dual-sensor with one big and one small): This mode supports one 13M (4224x3136) and one 2M (1920x1080) sensors, the previous frame data is stored by dividing the frame buffer in one part of big size and one parts of small size.

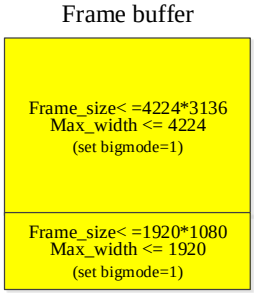

Fig. 2-14 Frame Buffer of Dual-Sensor

Multi-sensor register configuration at address offset 0x0408, and there are two registers to configure:

1) sw_sensor_mode: used to configure the number of sensors

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3’d0: one sensor
3’d1: two sensors
3’d2: four sensors
3’d4: three sensors with one big and two small (8M + 4M + 4M)
3’d5: two sensors with one big and one small (13M + 2M)

2) sw_sensor_index: sensor ID of the current sensor. software is required to number and configure each sensor.

Switching parameters between different sensors need to be configured at the end of current and before of next frame. The shadow register can be configured using force_upd or frame end update. Note: different sensor switch need set first_frame register (address offset 0x0404) in multi-sensor mode.

2.5.23 LDCH

LDCH module supports minimum resolution of 256x256 because of the constraint of LUT. When bicubic mode, LDCH will read 16bit table data from DDR, where the upper 12bit is integer part, which is used to strobe 4 pixels for calculation, and the lower 4bit is decimal part, which is used to strobe 4 coefficients of bicubic table for calculation. If the resolution is bigger than 4080, the 16bit table data is comprised of 13bit integer and 3bit decimal, at this time module will right shift the 3bit decimal to get a 4bit decimal for calculation when strobing bicubic table. This process is show below:

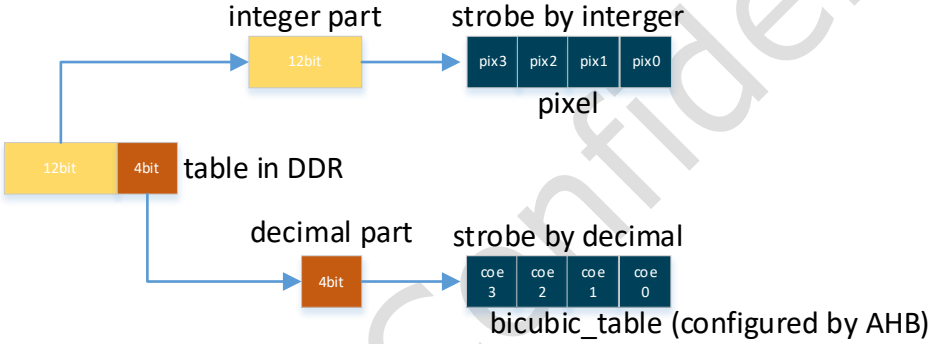

Fig. 2-15 LDCH process

When the 4bit decimal is 0, LDCH will use bicubic_table0 in zero_interp mode or fixed value 32’h00008000 in normal as the weight.

2.5.24 AXI Register Readback

When sys_axi_conf_rd_st (address offset 0x1a40[0]) is enabled, AXI will readback register configuration from DDR to configure ISP, MI and CSI2RX. AXI register readback and AHB register configuration can work at the same time, and the latter has higher priority.

AXI register configuration is composed of head (address offset + mode + counter) + data, which is shown as below:

	[31:18]	[17:16]	[15:0]
head	addr[15:2]	mode	counter
data	data(32bit)		

Fig. 2-16 AXI register configuration

mode 2’b00 is increased mode, mode 2’b11 is fixed mode, counter is the number of register configuration, which must be consistent with data number. When data is 32’hffffffff, AXI Register Readback is finished. Here is an example of AXI register readback:

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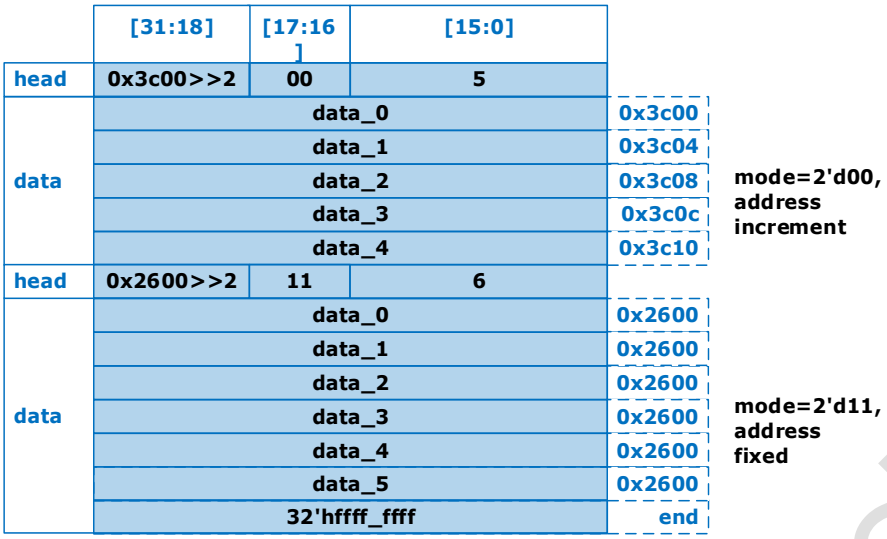

Fig. 2-17 an example of AXI register readback

The step of AXI register readback:

1) Calculate the word number of configuration, configure sw_axi_conf_wsize (address offset 0x1a48) and sw_axi_conf_vsize (address offset 0x1a4c). The word number of configuration is sw_axi_conf_wsize * sw_axi_conf_vsize (this product results must be greater than or equal to 64). When sw_axi_conf_wsize is no more than 8192, sw_axi_conf_vsize is 1, otherwise when sw_axi_conf_wsize is no more than 8192 * 2, sw_axi_conf_vsize is 2, and so on.

2) Configure sw_axi_conf_rd_base (address offset 0x1a44), where has loaded the AXI register configuration.

3) Configure sys_axi_conf_rd_st (address offset 0x1a40[0]) to 1 to start AXI register readback. There are two modes of AXI register readback. When sys_axi_conf_rd_st_mode (address offset 0x1a40[1]) is configured to 1, AXI register readback start by configuring sys_axi_conf_rd_st to 1 in each frame. When sys_axi_conf_rd_st_mode is 0, AXI register readback start by sys_axi_conf_rd_st in first frame, then will start by frame end signal automatically, and on this condition axi_conf_rd_status (address offset 0x1a40[31]) must be cleared by configuring axi_conf_rd_clear (address offset 0x1a40[4]) to 1 during current frame.

4) Constraint: The MMU and 3A registers need to be configured by AHB.

2.5.25 Frame Buffer to DDR

When frame buffer to DDR is enabled, CNR module must be enabled too, and the start signal of frame buffer read from DDR is reused with AXI register readback, so AXI register readback must be enabled too.

The step of frame buffer to DDR:

1) Configure sw_frm_buf_wr_base (address offset 0x1a50)

2) Configure sw_wr_frm_buf_en (address offset 0x1a40[8]) and sys_frm_buf_self_force_upd (address offset 0x1a40[16]) to 1 to enable frame buffer write to DDR in current frame.

3) Configure sw_rd_frm_buf_en (address offset 0x1a40[9]), sys_frm_buf_self_force_upd and sys_axi_conf_rd_st to 1 to enable frame buffer read from DDR, sys_axi_conf_rd_st_mode works the same as mentioned above.

Frame buffer can only write to DDR but not read in first frame, and can read and write in subsequent frames, which should be noted.

2.5.26 Slice Start

ISP support slice start in this version. Configure sw_isp_irq_line0 (address offset 0x0564[13:0]) to the line number you want to suspend, sw_isp_irq_line0 > 0 will enable slice start function, and sw_isp_irq_line0 = 0 will disable slice start function. The signal isp_slice_done (address offset 0x06a4[31]) will be 1 when ISP output line number equal to sw_isp_irq_line0, then configure sys_isp_slice_st (address offset 0x06a4[0]) to 1 to continue ISP process. When slice start is enabled, the range of sw_isp_irq_line0 is 0 < sw_isp_irq_line0 < sw_csi_col.

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Chapter 3 Video Output Processor (VOP)

3.1 Overview

The VOP (video output process) module is a display output processor. It reads video data and UI data from the frame buffer of the system memory, performs corresponding processing such as cropping, color gamut space conversion, scaling, overlay and outputs to each high-speed via video port display interface.
VOP supports the following features:

- Bus
  - One 32 bit AHB Slave to configure registers
  - One 128 bit readable and writable AXI Bus
- Video Ports
  - Video Port0/1
    - Resolution:
      - Max output resolution: 2048x1080 @60Hz
      - Max horizontal active: 2048
      - Max vertical active: 1080
      - Bits per component: 8
    - Scale_down:
      - Support horizontal scale rate 1/2~1
      - Support vertical scale rate 1/2~1
    - Color bar:
      - Horizontal mode
      - Vertical mode
    - BCSH(8bit):
      - Brightness(6bit), Contrast(9bit), Saturation(10bit), Hue adjustment(9bit)
    - 3D_LUT(Video Port0 only):
      - Support 9x9x9 LUT
    - CSC:
      - YUV2RGB: BT601-F /BT709-L/BT601-L/BT2020
      - RGB2YUV: BT601-F/BT709-L/BT601-L/BT2020
    - Dual Gamma(8bit)
    - Dither down:
      - Allegro
      - FRC
    - Post LB mode:
      - 2048 pixels x 4 mode
      - 1024 pixels x 8 mode
    - Display mode:
      - P2I/Interlace display
      - Blank display
      - Black display
      - Standby mode
- Esmart 0/1/2/3
  - Horizontal scale up:
    - Input max resolution: 2048x2160
    - Output max resolution: 4096x2304
  - Horizontal scale down:
    - Input max resolution: 4096x2304
    - Output max resolution: 2048x2160
  - Data format
    - RGB: ARGB8888/RGB888/RGB565
    - YUV: YUV420/YUV422/YUV444 8bit/10bit
    - YUYV: YUYV422/UYVY422
    - BPP: 8BPP
  - Image
    - Support virtual width

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- Support active offset
- Support display offset
- Support Y-mirror
- Support Swap: alpha/RB/UV swap
- Support YUV clip

- Multi-region
  - Only one region at one line
  - All regions are RGB or YUV format
  - Up to 4 regions
- Scale
  - Scale down:
    - Support scale rate (1/8:1]
    - Horizontal support 2 level-scale: pre-scale(avg2/4,gt2/4)
    - Vertical support 2 level-scale: pre-scale(avg2/4,gt2/4)
    - Scale mode: nearest/bilinear
  - Scale up:
    - Support scale rate [1:8]
    - Scale mode: nearest/bilinear/bicubic
- CSC
  - YUV2RGB: bt601-f/bt709-l/bt601-l/bt2020
  - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020

- Overlay
  - Support 4 layers overlay on port
  - Support RGB/YUV domain overlay
  - Support layers mux
  - Support per-pixel/global alpha
- Write Back
  Format: XRGB8888/RGB888/RGB565/YUV420
  Max resolution: 1920x1080
  - Support automatic write back and one frame write back model
  - Support horizontal scale down: [1/2:1]
  - Support Vertical scale down: gt2
- Interrupt
  - Vop_intr
    - System interrupt:
      - AXI bus error
      - AXI dma finish
      - Write back YRGB FIFO overflow
      - Write back dma finish
      - MMU interrupt
    - Video port0/1 interrupt:
      - Frame start interrupt
      - Line flag 0 interrupt
      - Line flag 1 interrupt
      - Post empty interrupt
      - Field start interrupt
      - Display hold interrupt
      - Video front porch interrupt
      - Post almost full interrupt
  - Vop_intr_ddr
    - Vop_dma_finish
  - Vop_intr_lb
    - Video port0 post almost full
    - Video port1 post almost full

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3.2 Block Diagram

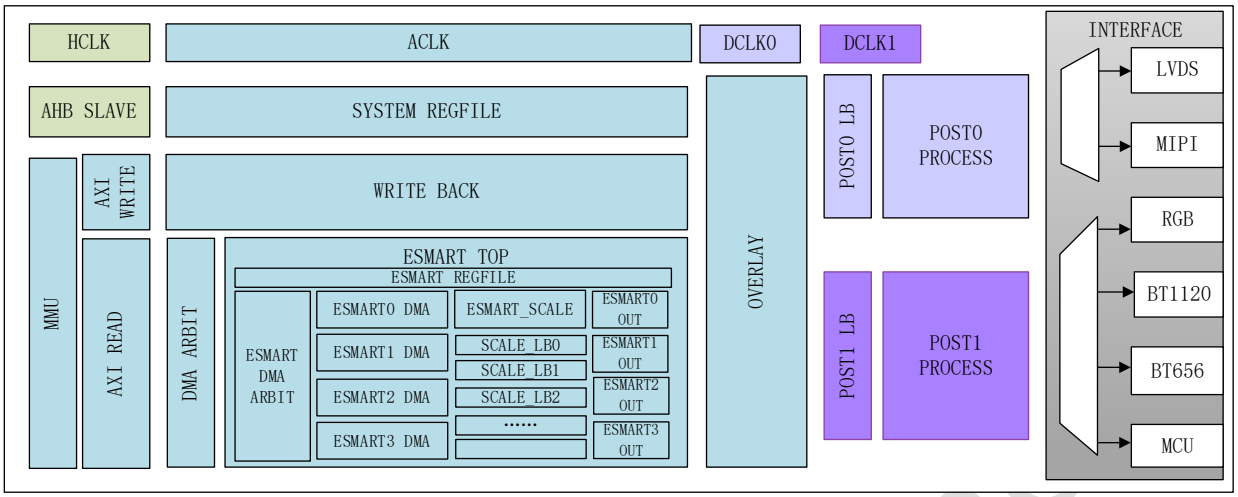

Fig.3-1 VOP3 Block Diagram

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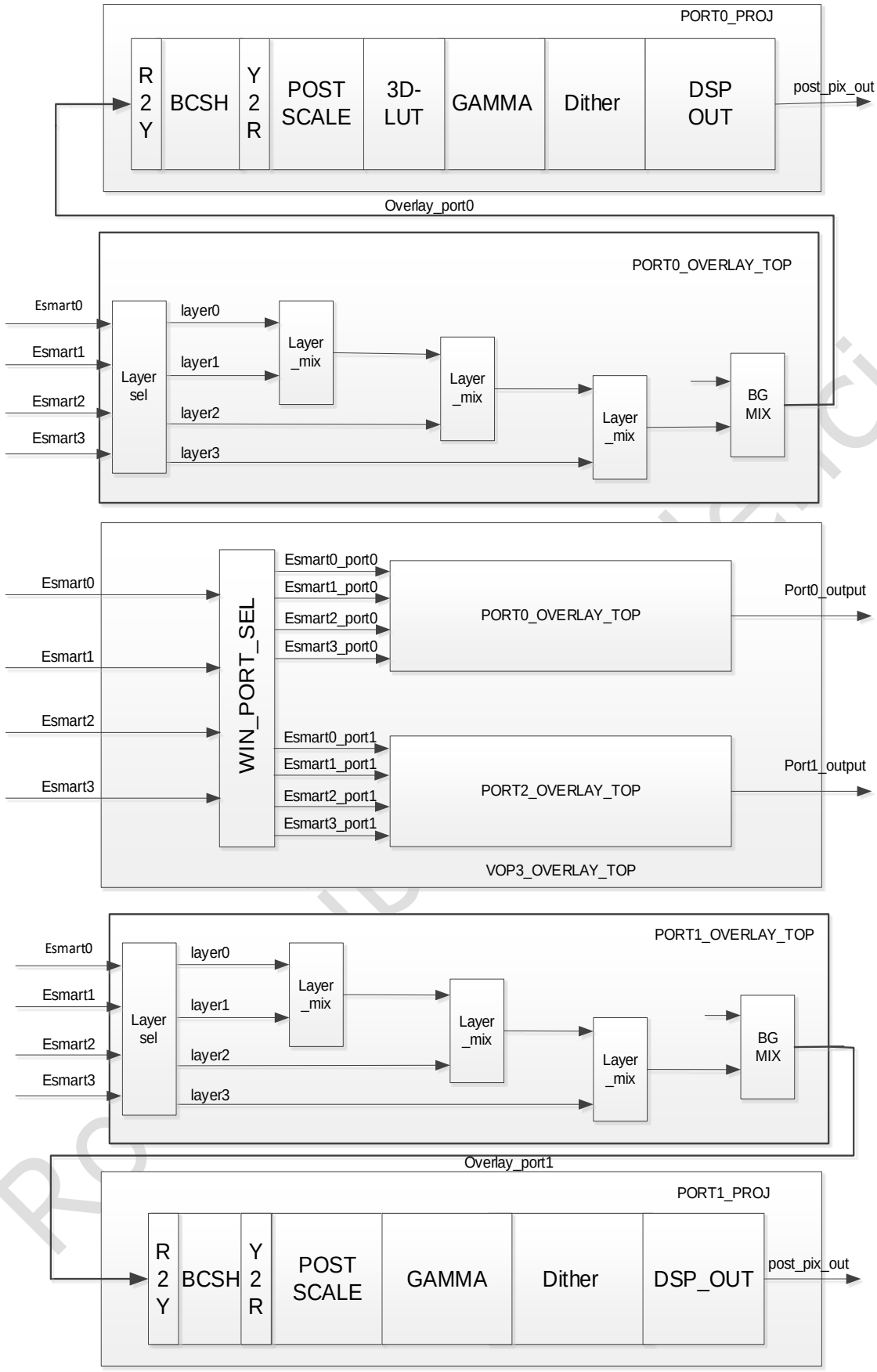

Fig.3-2 VOP Overlay and Post Diagram

VOP3 is comprised of:

- **AHB SLAVE**

When the VOP is the AHB slave, the master device can read and write registers to the VOP through the AHB bus. For example, when the CPU is the host, the master device can

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configure the transmission parameters of the VOP through the AHB bus.

- **SYSTEM REGFILE**

The register arrays, including system control, layer, overlay, and post process registers, are all in the ACLK domain, and read and write from HCLK to the ACLK domain through synchronization logic.

- **MMU**

The Memory Management Unit maps the configured virtual address to the physical address through the page table. Since there are one buses in the system, there are one MMU addresses. In the security mode, the address of the security layer is configured as a physical address from the MMU according to the configuration. The module is bypassed, so as to avoid the address being rewritten when the MMU is mapped.

- **AXI READ/WRITE**

There are AXI bus in VOP interface. The AXI supports both write and read channel.

- **DMA ARBITER**

Each layer in the system will initiate a different read request, and DMA arbiter will perform a global arbitration for internal requests based on priority settings and FIFO status.

- **ESMARTx**

Esmart layer only supports line mode and support display up to 4 regions where the regions can't overlap horizontally.

- **OVERLAY**

Perform the synthesis operation between layers according to the configuration and send it to the corresponding post process modules.

- **POST PROCESS**

Including dual-gamma, bcsh, 3d-lut and other post-processing modules. The data is processed by the post-processing module and then store them into the post line buffer.

- **POST LINE BUFFER**

The Post Process line buffer is used to store the data processed by the post process modules and output to corresponding display interface.

- **INTERFACE MUX**

The VOP supports variety of output interface including MIPI, LVDS, RGB, BT.1120, BT 656, MCU. By setting the interface mux module, the corresponding PORT can be selected and output to the corresponding interface.

3.3 Operating Mode

3.3.1 Clock and Reset Description

- **HCLK**

The maximum operating frequency: 200MHz

- **ACLK**

The maximum operating frequency: 400MHz

- **DCLK0/1**

The maximum operating frequency of DCLK0/1: 200MHz

- **Hardware Reset**

System hardware reset, that is, the hardware reset of the entire VOP through the system, all the logic inside the VOP will enter the initial state, if the current screen is being displayed, there will be abnormal phenomena such as a black screen.

- **Software Frame Reset**

The frame reset of each layer is supported, that is, when the vsync signal of each frame arrives, the layer's internal logic will be reset exclude register logic.

- **CLK_AUTO_GATING**

Rich auto_gating registers are provided in the sys module, which can optimize the clock to reduce power consumption when the module is not enabled. Among them, if AUTO_GATING_CTRL_IMD[31] is enabled, it means that auto_gating of all modules is turned on, and no separate control is required.

3.3.2 Bus Description

- **AHB Bus**

Configuration bus for register/LUT.

- **AXI Bus**

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The AXI bus is readable and writable, which supports write back function.

- **RID Default Configuration**

There are 15 IDs available for each bus. The driver allocates the rid according to the data of the layer on the bus. If it exceeds 0xf, another bus is required to be enabled.

- **Hurry/QoS**

VOP3 hurry has an enable bit and hurry value. Initiating a hurry request depends on whether the memory of the layer initiates a hurry request. When the layer's esmart_dma_rreq_hurry_en is enabled and the number of empty memory is greater than the set waterline, a hurry request is initiated.

VOP3 QoS has an enable bit in SYS_CTRL_SYS_AXI_HURRY_CTRL0_IMD. When QoS is enabled and rid is greater than or equal to 0xa, QoS signal is asserted.

- **MMU Frame Valid Mechanism**

MMU supports the bypass function in register mmu_bypass_en and mmu_bypass_id. When rid>=mmu_bypass_id, the AXI request and the returned data will bypass MMU. Noted that mmu_bypass_en and mmu_bypass_id is enabled immediately. At that time, rid is effective frame for the layer, so it can realize whether the layer data access is mmu_bypass.

- **Protection Mechanism**

In the protection mode, the port number of the protected layer can be set and sent to the designated protected port, otherwise the layer will be forcibly closed.

3.3.3 Display Output Interface Description

The following figure shows the interface connection diagram of VOP3. There are 2 ports in the VOP to distribute video data to different high-speed interfaces through the software setting interface MUX.

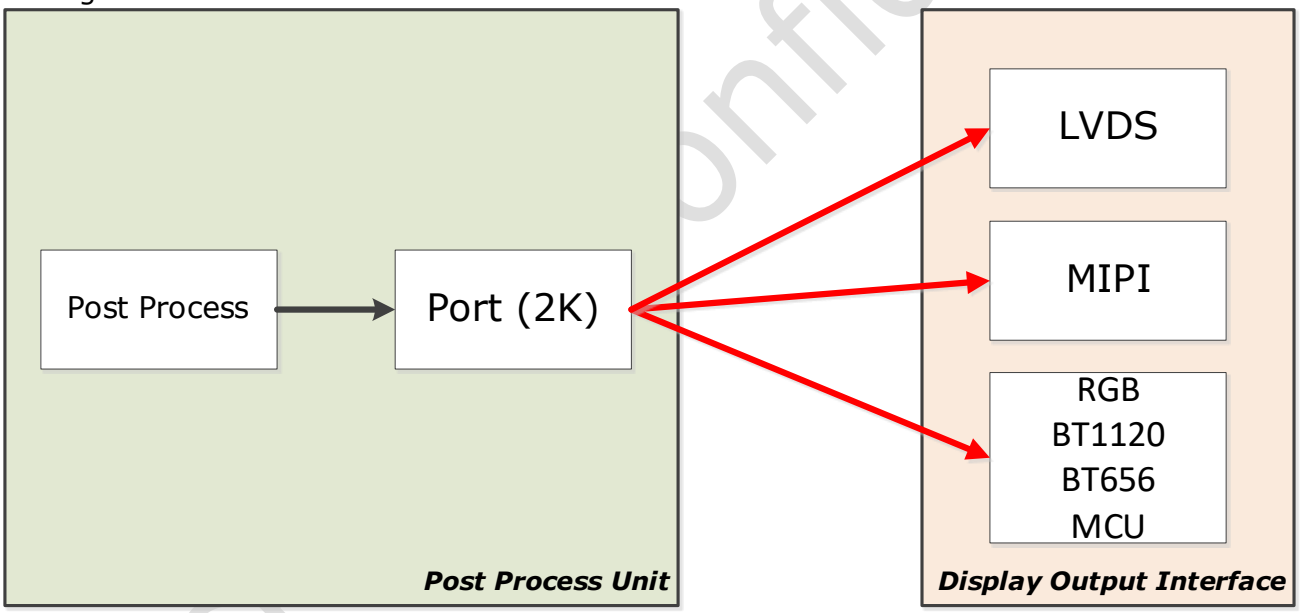

Fig.3-3 Schematic Diagram of Display Output Interface

- LVDS Interface
  - The maximum resolution supports 1280x800@60p
- MIPI TX Interface
  - The maximum resolution supports 2048x1080@60p
- BT656/BT1120/RGB
  - BT1120 maximum resolution support: 1920x1080@60p
  - RGB maximum resolution support: 2048x1080@60p
  - BT656 maximum resolution support: 720x576@60p
  - BT1120 support interlace mode, maximum resolution support: 1920x1080@60i
  - BT656 support interlace mode, maximum resolution support: 720x567@60i
  - The data source of the parallel interface is directly connected to port interface
  - The three modes share one I/O group, which contains 1-bit clock signal and 24-bit data signals
- MCU
  - Maximum resolution support: 720x480@60p
  - The data source of the para interface is directly connected to port 0/1

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- RGB/MCU/BT1120/BT656

The bit mapping relationship corresponding to each interface is as shown in the figure Below.

Table 3-1 Map of parallel port I/O output

GPIO	RGB888(MCU)	RGB666(MCU)	RGB565(MCU)	BT656	BT1120	MCU（RGB）Serial 3*8-bit
DCLK	DCLK	DCLK	DCLK	BT656_DCLK	BT1120_DCLK	MCU_RS
HSYNC	HSYNC	HSYNC	HSYNC	NA	NA	MCU_WEN
VSYNC	VSYNC	VSYNC	VSYNC	NA	NA	MCU_CS
DEN	DEN	DEN	DEN	NA	NA	MCU_REN
D23	D23	D17	D15	NA	BT1120_D15	MCU_D7
D22	D22	D16	D14	NA	BT1120_D14	MCU_D6
D21	D21	D15	D13	NA	BT1120_D13	MCU_D5
D20	D20	D14	D12	NA	BT1120_D12	MCU_D4
D19	D19	D13	D11	NA	BT1120_D11	MCU_D3
D18	D18	D12	NA	NA	NA	NA
D17	D17	NA	NA	NA	NA	NA
D16	D16	NA	NA	NA	NA	NA
D15	D15	D11	D10	NA	BT1120_D10	MCU_D2
D14	D14	D10	D9	NA	BT1120_D9	MCU_D1
D13	D13	D9	D8	NA	BT1120_D8	MCU_D0
D12	D12	D8	D7	BT656_D7	BT1120_D7	MCU_D7
D11	D11	D7	D6	BT565_D6	BT1120_D6	MCU_D6
D10	D10	D6	D5	BT565_D5	BT1120_D5	MCU_D5
D9	D9	NA	NA	NA	NA	NA
D8	D8	NA	NA	NA	NA	NA
D7	D7	D5	D4	BT656_D4	BT1120_D4	MCU_D4
D6	D6	D4	D3	BT565_D3	BT1120_D3	MCU_D3
D5	D5	D3	D2	BT565_D2	BT1120_D2	MCU_D2
D4	D4	D2	D1	BT565_D1	BT1120_D1	MCU_D1
D3	D3	D1	D0	BT565_D0	BT1120_D0	MCU_D0
D2	D2	D0	NA	NA	NA	NA
D1	D1	NA	NA	NA	NA	NA
D0	D0	NA	NA	NA	NA	NA

- The output pixel clock supports Delay-Line function which maximum adjustable range is 3~5ns
- support output pixel clock polarity inversion function
- support clk_delay_cycle set. rgb_dclk_delay_num = VO_IO_CON[15:8];
- VO_IO_CON_raddr = 0xFF070500;

3.3.4 Interrupt Description

There are three interrupt signals.

VOP_intr: Including the following groups of interrupt sources.

- VOP_intr_sys
- VOP_intr_post

VOP_intr_DDR: Conditional interrupt source dma_finish from DDR frequency conversion, refer to frequency conversion description for details.

VOP_intr_lb: Including the following groups of interrupt sources, which can set the buffer waterline to notify the CPU that the predetermined waterline has been reached.

- Int_status_post_full0
- Int_status_post_full1

3.3.5 Maximum Performance and Functional Attributes of each PORT

- PORT0
  - The maximum supported resolution for the port line direction is 2048 pixel
  - Dual gamma(8bit)
  - 9x9x9 3DLUT
- PORT1
  - The maximum supported resolution for the port line direction is 2048 pixel

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- Dual gamma(8bit)

3.3.6 DDR Frequency Conversion Instructions

1. dma_finish interrupt source

This interrupt is connected to DCF and DCF can handle frequency conversion.

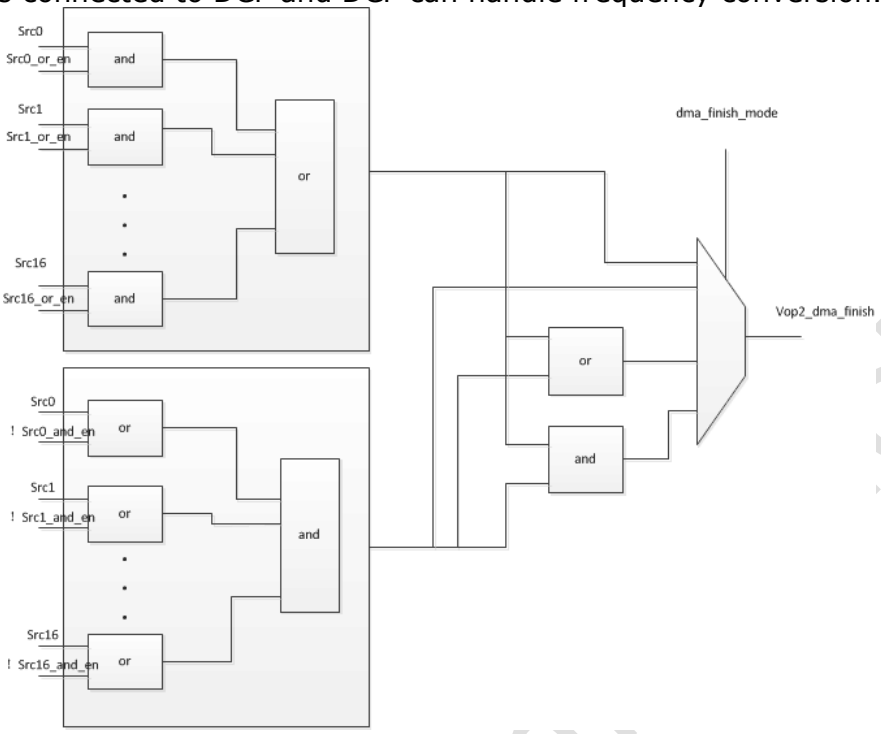

Fig.3-4 DMA finish interrupt structure diagram

The source of dma_finish is as follows, and the logic from win almost full, vp line flag, dsp hold and almost full is combined and output.

Table 3-2 dma finish interrupt source description

source list	name	remark
dma_finish	src0	AXI0_dma_finish
wb_dma_finish	src1	WB DMA finish detected
vp0_line_flag	src2	When port0 line count equals the configured line flag number
vp1_line_flag	src3	When port1 line count equals the configured line flag number
vp0_dsp_hold	src6	Port0 hold status detected
vp1_dsp_hold	src7	Port1 hold status detected
vp0_almost_full	src10	When port0 post line buffer number equals dsp_almost_full_thold
vp1_almost_full	src11	When port1 post line buffer number equals dsp_almost_full_thold

2. VOP_intr_DDR

The VOP_intr_DDR signal comes from dma_finish, which is connected to the system interrupt controller through an interrupt signal, and the frequency can be converted through the interrupt, which is consistent with the DCF function.

3. VOP_intr_lb

Set the waterline of the post line buffer, and realize real-time frequency conversion through the status of line buffer, which can provide about 20us for frequency conversion.

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3.4 Function Description

3.4.1 Esmart layer

3.4.1.1 Schematic diagram of esmart

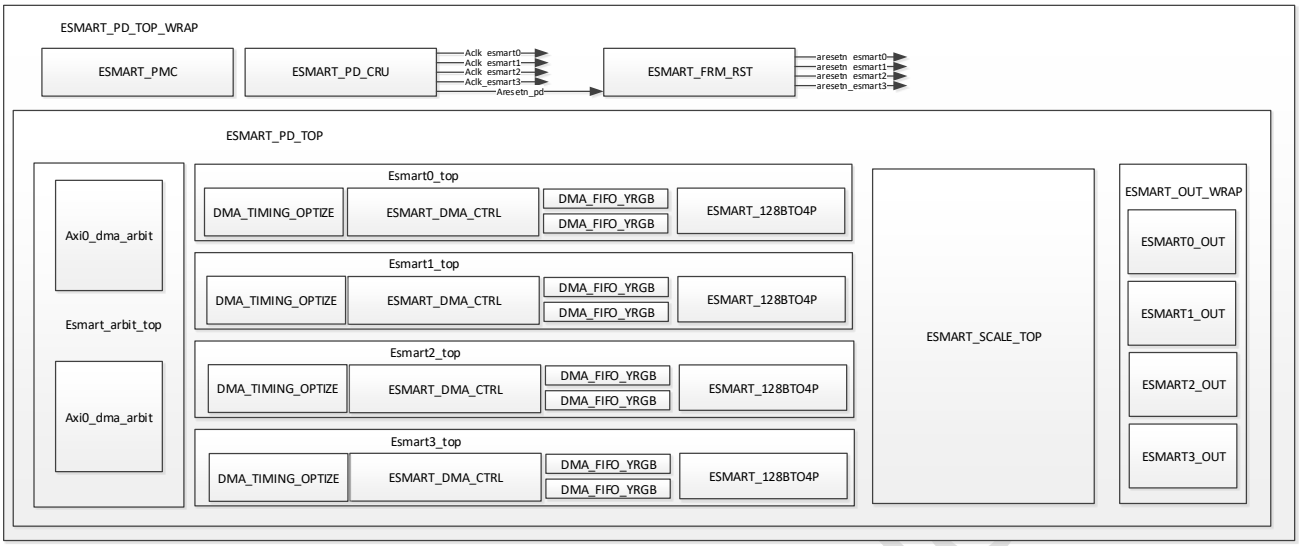

Fig.3-5 VOP3 esmart block diagram

3.4.1.2 Layer

1. Feature

- Support line mode
- Support color gamut space conversion
- Support 4 area display
- Support 1/8~8 times infinite scale
- Support image virtual width/cropping
- Support y_mirror

2. Basic bus

The bus behavior of the esmart layer is to take one line of buffers when one line is free. It cannot be taken in two lines at a time like the 8 lines of the cluster layer. Basically, each line has a part of time for bus access. The power consumption of DDR is also not very friendly.

3. Power consumption description

The logical power consumption of the smart layer is smaller than that of the cluster layer, but because the cluster has AFBCD modules, plus the power consumption of the DDR controller and phy, the overall power consumption of the smart layer is much larger than the overall power consumption of the cluster layer.

It is recommended to use AFBCD as much as possible for those AFBCD application, and smart layer may be used in multi-region features.

3.4.1.3 Format

Table 3-3 Swap configuration table in esmart default format

esmart		
Format	**rb_swap**	**uv_swap**
ARGB	1	0
RGB888	1	0
RGB565	0	0
YUV420	0	1
YUV422	0	1
YUV444	0	1
YVYU422	0	1
VYUY422	0	1

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esmart		
Format	**rb_swap**	**uv_swap**
YUV420_10b	0	1
YUV422_10b	0	1
YUV444_10b	0	1

3.4.1.4 CSC

Support yuv2rgb(10bit), rgb2yuv(10bit) color gamut space conversion, you can select the corresponding csc according to the input image format and the spatial gamut of the overlay.

- RGB2YUV supports the following modes:
  - BT_601_L

$$Y_{601_L} = 0.257R + 0.504G + 0.098B + 64$$
$$Cb = -0.148R - 0.291G + 0.439B + 512$$
$$Cr = 0.439R - 0.368G - 0.071B + 512$$

  - BT_709_L

$$Y_{709} = 0.183R + 0.614G + 0.062B + 64$$
$$Cb = -0.101R - 0.338G + 0.439B + 512$$
$$Cr = 0.439R - 0.339G - 0.040B + 512$$

  - BT_601_F

$$Y_{601_F} = 0.2990R + 0.5870G + 0.1140B + 0$$
$$Cb = -0.1687R - 0.3313G + 0.5000B + 512$$
$$Cr = 0.5000R - 0.4187G - 0.0813B + 512$$

  - BT_2020

$$Y_{2020} = 0.2250R + 0.5807G + 0.0508B + 64$$
$$Cb = -0.1223R - 0.3157G + 0.4380B + 512$$
$$Cr = 0.4380R - 0.4028G - 0.0352B + 512$$

- YUV2RGB supports the following modes:
  - BT_601_L

$$R = 1.164(Y - 64) + 1.596(V - 512)$$
$$G = 1.164(Y - 64) - 0.391(U - 512) - 0.813(V - 512)$$
$$B = 1.164(Y - 64) + 2.018(U - 512)$$

  - BT_601_F

$$R = Y + 1.402(V - 512)$$
$$G = Y - 0.344(U - 512) - 0.714(V - 512)$$
$$B = Y + 1.772(U - 512)$$

  - BT_709_L

$$R = 1.164(Y - 64) + 1.793(V - 512)$$
$$G = 1.164(Y - 64) - 0.213(U - 512) - 0.534(V - 512)$$
$$B = 1.164(Y - 64) + 2.115(U - 512)$$

  - BT_2020

$$R = 1.1636(Y - 64) + 1.6778(V - 512)$$
$$G = 1.1636(Y - 64) - 0.1872(U - 512) - 0.6501(V - 512)$$
$$B = 1.1636(Y - 64) + 2.1406(U - 512)$$

In BT2020 mode, it defaults to limit range, and there is no full range option.

3.4.1.5 Scale

Horizontal direction algorithm:

- Scl up: best-neigh/bilinear/bicubic
- Scl dn: best-neigh/bilinear(support 2 Level-Scale)

Vertical direction algorithm:

- Scl up: best-neigh/bilinear/bicubic
- Scl dn: best-neigh/bilinear

Sample:2 level-scale sample: A picture with a width of 400 and a height of 400 is scaled to a picture with a width of 150 and a height of 400 by vop:

1. Act_width=src_width(400)-1;act_height=src_height(400)-1;write act_width to DSP_INFO[15:0]. write act_height to DSP_INFO[31:16].
2. Dsp_width=dst_width(150)-1;dsp_height=dst_height(400)-1;write dsp_width to DSP

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_INFO[15:0]. write dsp_height to DSP_INFO[31:16].
3. Set regionx_xpre_scl_mode(REGIONx_MST_CTL[23:22]) = 2'b00.
4. Enable xavg_en(REGIONx_MST_CTL[20]) or xgr_en(REGIONx_MST_CTL[21]).
5. After the 1 level-scale, act_width becomes 200.
6. Calculate the scale_factor width 200 to 150, set regionx_yrgb_xfactor(REGIONx_SCL _FACTOR_YGB[15:0]) = scale_factor.
7. Enable regionx_xsd_en(REGIONx_SCL_CTRL[1]).

3.4.1.6 ESMART LB_MODE

Esmart0/1/2/3 share 8k line buff:

- Esmart lb_mode = 2'b00: support one layer display up to 8k pixels.
- Esmart lb_mode = 2'b01: support two layer display up to 4k pixels.
- Esmart lb_mode = 2'b10: support one layer display up to 4k pixels, two layer display up to 2k pixels.
- Esmart lb_mode = 2'b11: support four layer display up to 2k pixels.

3.4.1.7 Usage Constraints

(1) The esmart layer no longer supports the YUYV420/UYVY420 format.
(2) YUYV422 and UYVY422 are not supported when the esmart layer is displayed in four areas at the same time.
(3) The esmart layer YUV422/YUV420 requires act_width and act_xoffset to be even aligned.
(4) The esmart layer YUV420/YUV420_10bit requires act_height and act_yoffset to be even aligned.
(5) The esmart layer YUV420_10bit requires act_xoffset n*8 to be aligned.
(6) The esmart layer YUV444_10bit/YUV422_10bit requires act_xoffset n*4 to be aligned.
(7) The esmart layer YUV422_10bit/YUV422_10bit requires act_act_width n*2 to be aligned.

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3.4.2 Overlay

3.4.2.1 Schematic diagram of layer data path

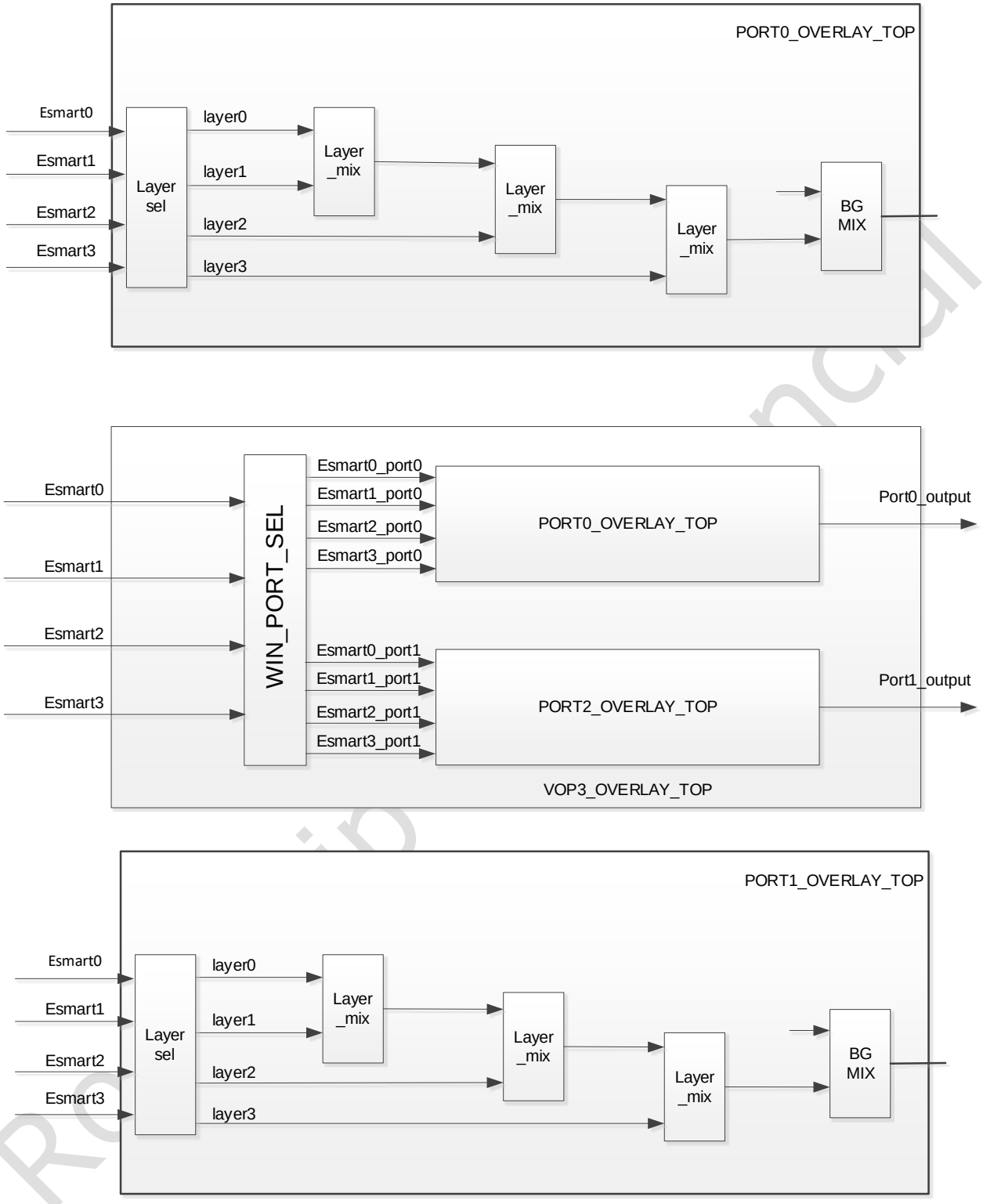

Fig.3-6 VOP3 overlay block diagram

3.4.2.2 Delay setting of each function

As shown in the figure above, in the new overlay architecture, all vp are output from the last stage of mux, so the value of each vp should be a fixed delay_num, and its default value is shown in the following table.

Typical settings are as follows:

Table 3-4 Default table of layer delay number

Block	Delay_num
esmart	27
The delay of the port0/1 last mux output	43

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	43

3.4.2.3 Alpha module

If there is no alpha processing, it is a direct coverage effect. Therefore, it is necessary to do an alpha effect on the corresponding layer or the corresponding position to achieve the overlay of the UI and the background or video. Most of them are aimed at the RGB data with alpha output by the GPU, such as RGBA8888; or the global alpha of the layer is configured inside the VOP to realize the special effect of superimposing between the layers.
The following picture shows the basic alpha overlay effect:

Fig.3-7 Schematic diagram of alpha effect

1. Per-pixel Alpha

Per-pixel alpha, as the name implies, is that each point has corresponding alpha information. As shown in the picture above, the alpha value of each point in Jordan's picture increases from 0 to 255 in cycles from left to right, and the effect gradually changes from fully transparent to impermeable.

2. Global Alpha

The global alpha has nothing to do with the original data. You can set the alpha value of the entire layer separately. As shown in the figure above, the little bee layer is a global alpha effect, and the transparency of the entire layer is the same.

3. Pre-mult Alpha

Pre-multiplied alpha means that in the process of GPU operation, the original data and alpha have been multiplied accordingly, and there is no need to multiply alpha by its own RGB value during subsequent overlay.
The modes of Alpha are shown in the figure below:

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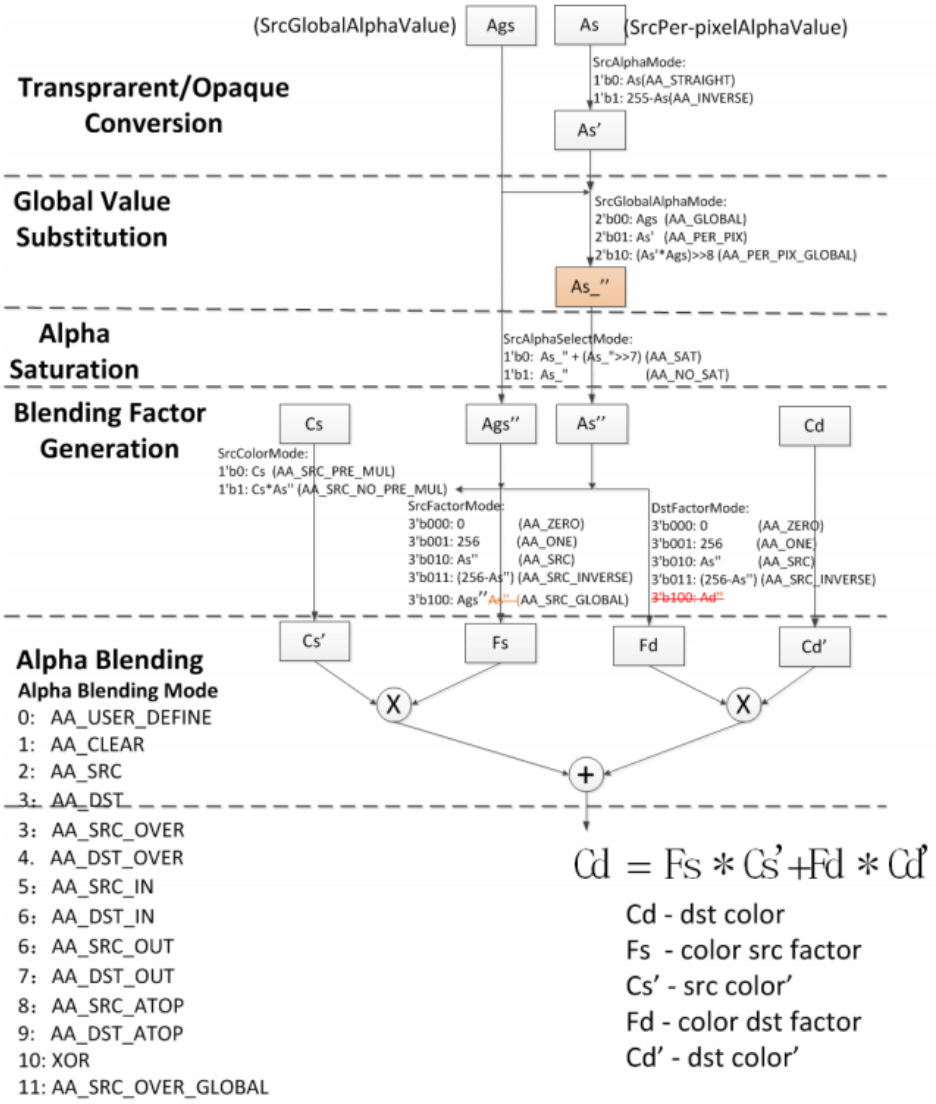

Fig.3-8 Alpha structure diagram

3.4.3 Write Back

3.4.3.1 Support format

1. Support format

- ARGB888
- RGB888
- RGB565
- YUV420

2. Color gamut conversion

Since the main application scenario output is RGB, but there is a need for YUV420 write-back, the write-back module adds RGB2YUV format conversion, which is enabled by configuring wb_rgb2yuv_en register bit.

3.4.3.2 Single frame/multi frame mode

(1) Single frame mode

Operating in single frame mode, enable the oneframe_clr register, and automatically disable wb_en after each frame is written, so that only one frame of content will be written out.

(2) Multi-frame mode

Each frame is configured with a different address, and the wb module will continuously write out the corresponding whole frame content.

(3) Line write mode

After enabling, the pixels accumulated in a line are written back to DDR in a concentrated manner to improve the efficiency of write back.

3.4.3.3 Horizontal scaling

The bilinear scaling algorithm is used in the horizontal direction.

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3.4.3.4 Vertical stroke

Due to the limitation of memory, there is not enough linebuffer opened separately, so no scaling is done in the y direction. If more than twice, wb_ythrow_en is configured to control the line-throwing operation to reduce the output bandwidth.

3.4.3.5 Usage Constraints

(1) In the case of YUV domain output, the conversion of YUV2RGB is not supported, that is, RGB format cannot be written back under YUV domain.
(2) Act_width must be an integer multiple of 16 in write-back mode.

3.4.4 Post process

Function of each PORT 0/1 and the post-processing modules included in each PORT.

3.4.4.1 DSP_BLANK

When DSP_OUT_BLANK enabled, VSYNC/HSYNC/DATAEN and DATA signals are all cleared to zero.

3.4.4.2 DSP_OUT_ZERO

When DSP_OUT_ZERO enabled, the VSYNC/HSYNC/DATAEN signal is pulled low, and DATA_BUS is output normally.

3.4.4.3 DSP_BLACK

When DSP_BLACK enabled, the timing-related scan timing will be output normally, and data will be 0 on the data bus.

3.4.4.4 Color bar

Each PORT has a corresponding color bar setting, which can be used to debug to eliminate bus and layer problems, and it can also bypass the layer to directly adjust each high-speed output interface.
Control register color_bar_en to enable colorbar of PORT.
Control register color_bar_mode to switch horizontal colorbar or vertical colorbar.

3.4.4.5 Dither

If an 8bit film source needs to be output to the rgb666 screen, if there is no dither, it is directly connected to the screen with a high 6-bit. In this case, the color gradation will be caused.
In principle, the smooth curve becomes a ladder after losing the low position. In order to solve this problem, noise is added to the ladder, so that the transition can restore the original smooth curve as much as possible.

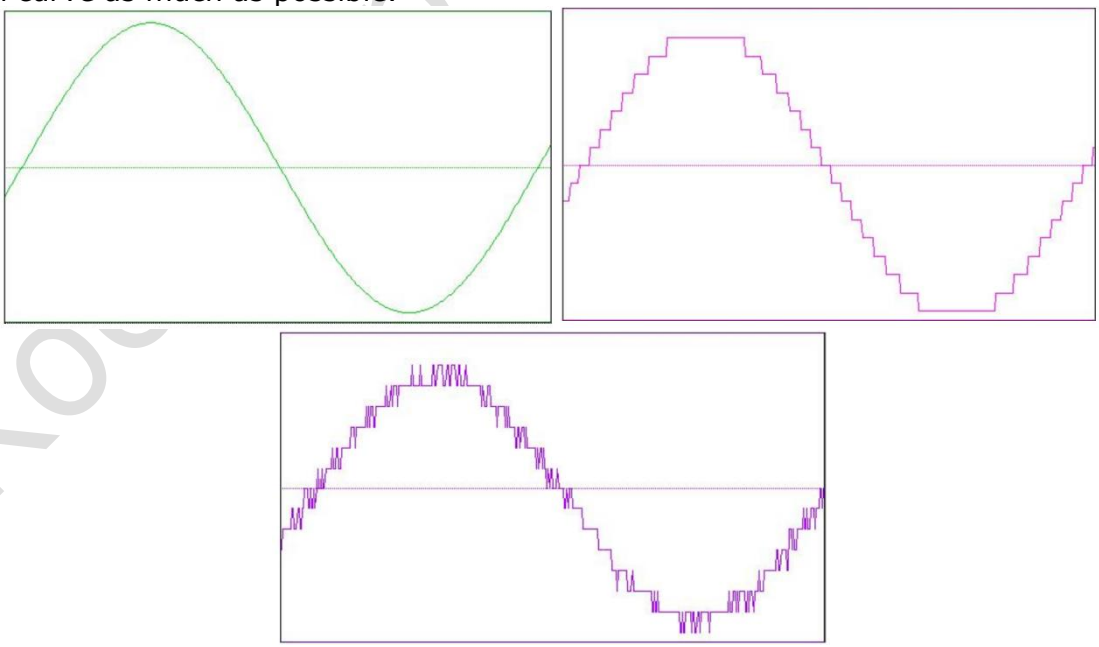

Fig.3-9 Schematic diagram of dither principle

VOP has ALG in the dither algorithm of 10bit->8bit; there are ALG and FRC in the dither algorithm for 8bit->666/565, which can be selected by dither_down_mode.
ALG algorithm: Add fixed noise, the possible negative effect is that there will be more regular stripes similar to tire tracks.
FRC algorithm: time-domain jitter is added to the space, which works well in high frame

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rate scenes, and low frame rate scenes may feel a little flickering and jittery.

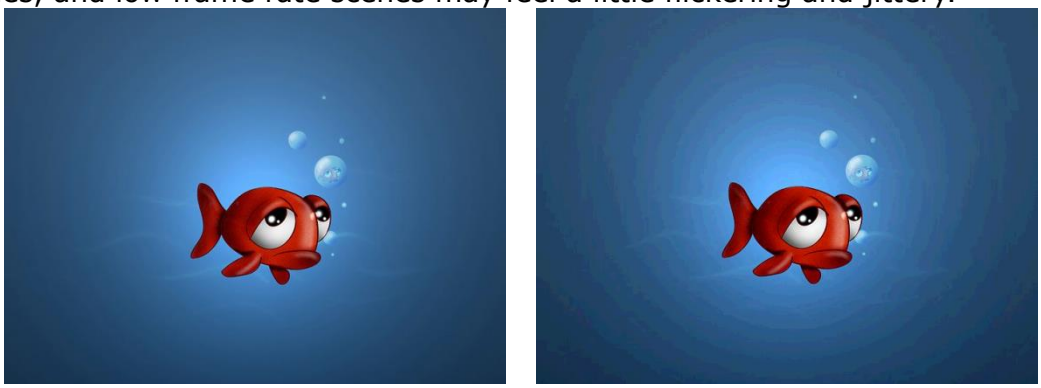

Fig.3-10 dither effect diagram

Left: original picture; right: direct clip effect

The above picture shows the color scale effect of the original picture and the direct clip. The figure below is the figure processed by the dither algorithm. The overall effect is obvious to solve the color gradation problem caused by dither, but after partial magnification, the tire-like effect on the right side of the figure below will appear.

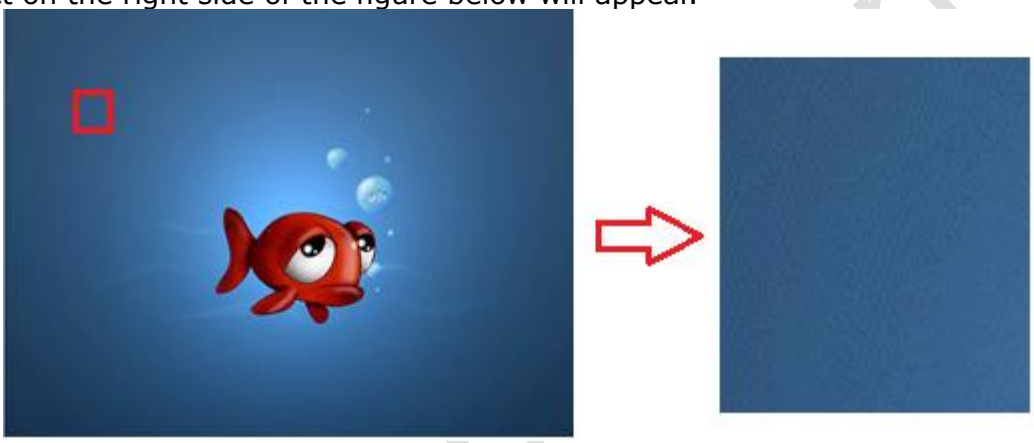

Fig.3-11 Schematic diagram of dither's tire pattern

3.4.4.6 BCSH

BCSH mainly adjusts the following effects:

(1) CON: Contrast coefficient

(2) BRT: Bright picture adjustment value

(3) HUE: hue adjustment angle

(4) SAT: Saturation coefficient

Y processing calculation formula

$Y_0=Y_{input}-16;$	(0<Y0<239)
$Y_1=Y_0*CON;$ (0<CON<1.992)	(0<Y1<478)
$Y_2=Y_1+BRT;$(-32<BRT<31)	(-32<Y2<509)
$Y_3=Y_2+16;$	(-16<Y3<525)
Y_{output}= 4 mux 1	

U processing calculation formula

$U_0=U_{input}-128;$	(-128,127)
$U_1=U_0*\cos(HUE) + V_0*\sin(HUE)$ (-30^o<HUE<30^o)	(-175,174)
$U_2=U_1*CON*SAT;$ (0<CON<1.992,0<SAT<1.992)	(-695,691)
$U_3=U_2+128;$	(-567,819)
U_{output}= 4 mux 1	

Cos(HUE)+sin(HUE) = (1+1/2*sin(2HUE))1/2;

So this value increases monotonically with the increase of the value of HUE. The value range of HUE is -30^o~30^o.

V processing calculation formula

$V_0=V_{input}-128;$	(-128,127)
$V_1=V_0*\cos(HUE)$ - U0*sin(HUE) (-30^o<HUE<30^o)	(-175,174)
$V_2=V_1*CON*SAT;$ (0<CON<1.992,0<SAT<1.992)	(-695,691)
$V_3=V2+128;$	(-567,819)

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V_{output}= 4 mux 1
Cos(HUE)-sin(HUE) = $(1+1/2*\sin(-2HUE))^{1/2}$;

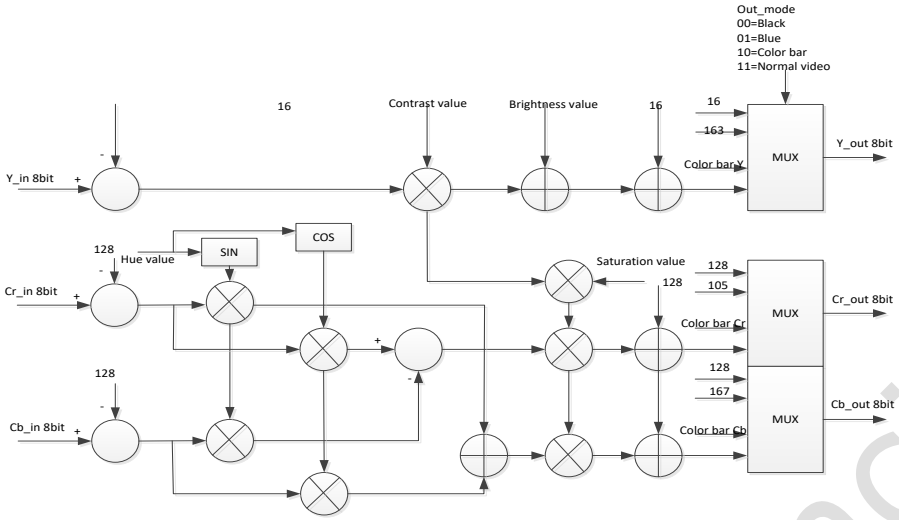

Fig.3-12 Schematic diagram of BCSH algorithm

3.4.4.7 Gamma

Gamma basic principle:

Gamma can be understood as a 1:1 remapping of the RGB on the display channel. The three RGB curves can be consistent or inconsistent. Therefore, the display color temperature and blue light removal effects can be adjusted through the mapping relationship of the three curves.

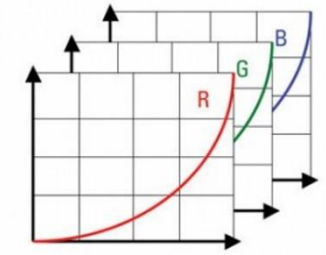

Fig.3-13 Schematic of gamma

Dual gamma:

Because the application may adjust the gamma curve to achieve dynamic adjustment of some color temperature effects. However, the memory of the gamma table is a single-port memory. When a new table is written, it is necessary to disable gamma, which will cause screen flicker when dynamically adjusting the gamma curve.

In order to solve this flicker phenomenon, VOP adopts the ping-pong dual gamma. By statically switching gamma, one table is displayed and used in real time, and the other table is a new table that can be configured.

3.4.4.8 3D LUT

Gamma can be regarded as a 1D LUT. The RGB data in the 1D LUT are independent of each other, which means that the 1D LUT can only control the gamma value, RGB balance (gray scale) and white point. In order to overcome the limitation of 1D LUT, we can form a 3×3 matrix of three 1D LUTs of RGB to control the color saturation and brightness, and perform linear scaling in the complete color space. The 3D LUT can affect the hue, saturation, brightness, etc. in a full three-dimensional color space control method.

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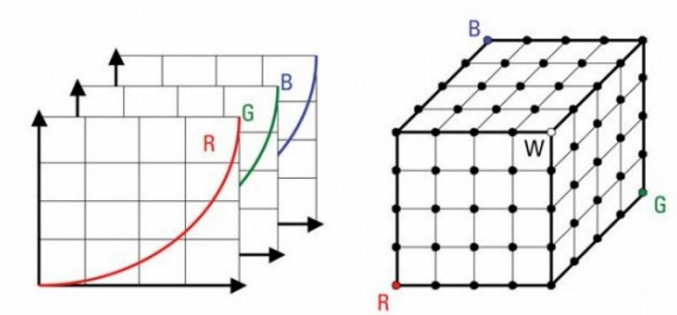

Fig.3-14 Schematic diagram of 2D/3D-LUT

3D LUT application scenarios:

(1) Calibration (calibration LUT)

It is mainly used for the calibration of hardware and display equipment in color management. The video will be processed by different systems during the shooting, post-processing and final projection, and will appear in different forms. Therefore, the 3D LUT color space mapping can ensure that the video remains visually consistent in different systems.

(2) Technology (Technical LUT)

It is mostly used for conversion under different characteristic curves in different color spaces. Mapping from Log to Rec709 belongs to this type. The color standards of computer monitors, televisions, mobile phones, and Pads that we come into contact with in work and life are very close to Rec.709. However, now a large number of cameras and even SLRs can shoot log (Log) video. If the log video is sent to the Rec.709 standard monitor for monitoring, it cannot be restored normally. The fundamental reason is that the gamma difference between the two is very large, so it needs to be artificially corrected to the display system gamma.

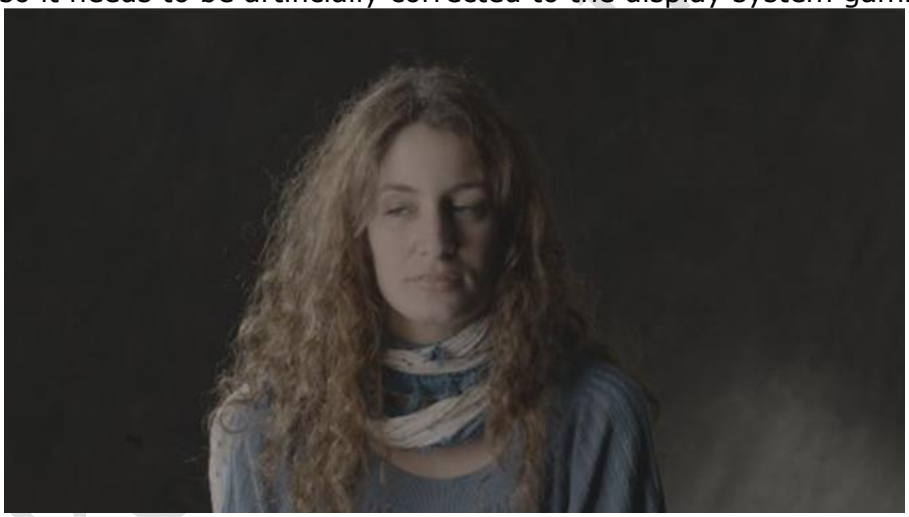

Fig.3-15 Effect picture before correction

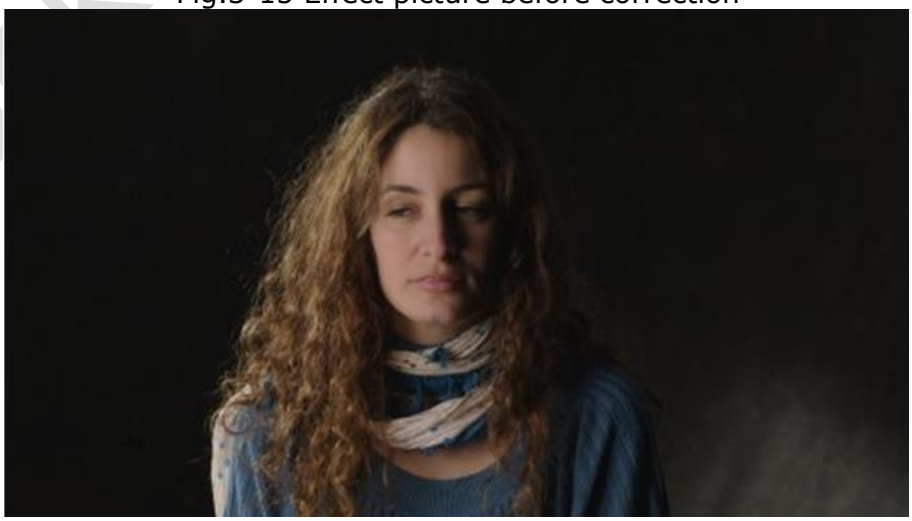

Fig.3-16 Effect picture after correction

(3) Style (Creative LUT/Looks LUT)

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In order to realize a certain style of LUT, the LUT produced by the director of photography during the pre-shooting and can be previewed on-site. Using LUT to calibrate the color of the monitor does not creatively process the video. Another type of use of LUT is to color, that is, creatively process the video.

Fig.3-17 Effect picture before and after toning
Comparison of 3D LUT before (left) and after (right) toning

Accuracy description

Most 3D LUTs use stereo in the range of 9^3 to 65^3. A 9^3 LUT means that each AXIs has 9 points from input to output, and between these points Interpolation is required for the value between. Different systems will achieve this with varying degrees of accuracy.

In the evaluation of accuracy, the linear table adds a random value of 0 to 0.1 to make a non-linear 3DLUT table. Then use 9x9x9, 17x17x17, 33x33x33 table item evaluation respectively, it can be seen that the more table items, the closer the polyline effect can be. Some scenes need to use 33x33x33 3d LUT.

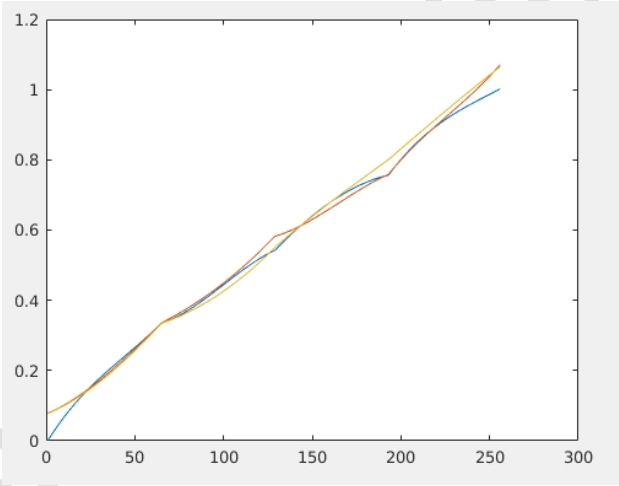

Fig.3-18 9x9x9 table renderings

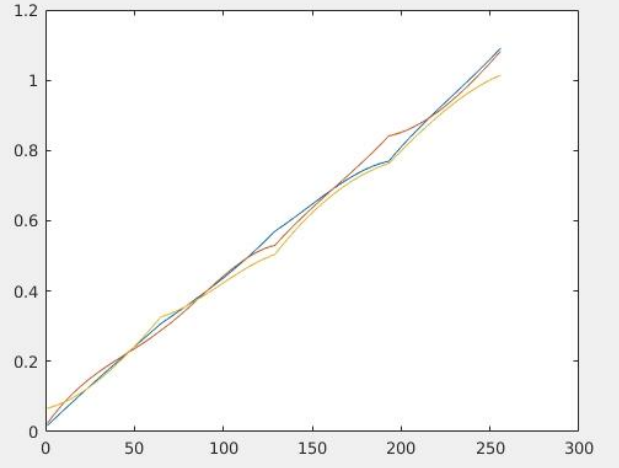

Fig.3-19 17x17x17 table renderings

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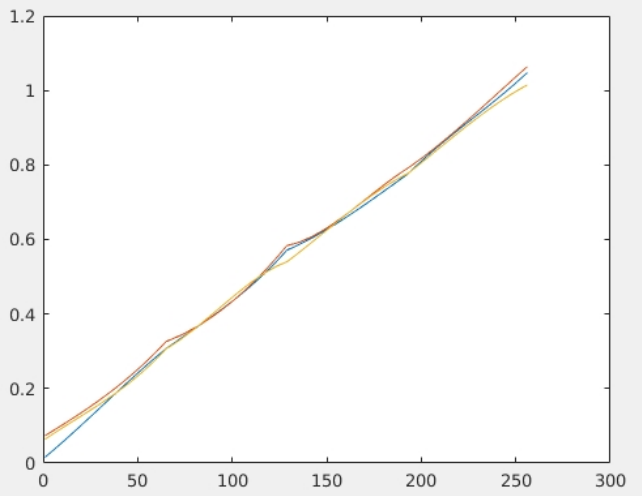

Fig.3-20 33x33x33 table renderings

But from an implementation point of view, the memory area occupied by 33x33x33 is too large.

- 7*7*7 memory area 0.0638*2 = 0.1276 mm²;
- 7*17*17 memory area 0.1742*2 = 0.3484 mm²;
- 33*33*33 memory area 0.4683*2 = 0.9366 mm²;

According to the compromise between application scenarios and area in VOP, the accuracy of 3D LUT is allocated as follows:

- PORT0: 9x9x9;

Application and configuration

In the application, user can adjust the required scene effects through the 3D LUT Creator software and save the 3D LUT table configuration corresponding to 9x9x9 or 17x17x17 to the address corresponding to the VOP.

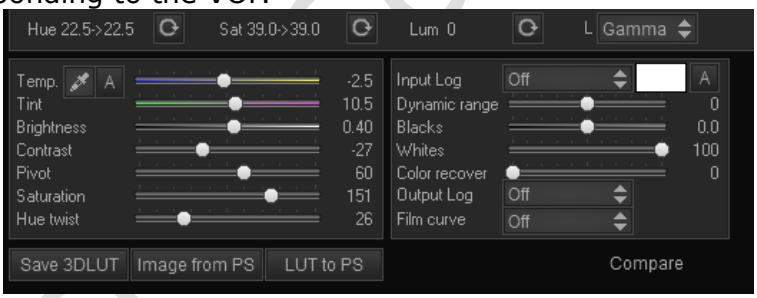

Fig.3-21 Basic operation interface of 3D LUT Creator

For example, for a 9x9x9 LUT table, a 729-point constant needs to be written to the corresponding memory, which can be written through AXI or AHB. The arrangement is as follows:

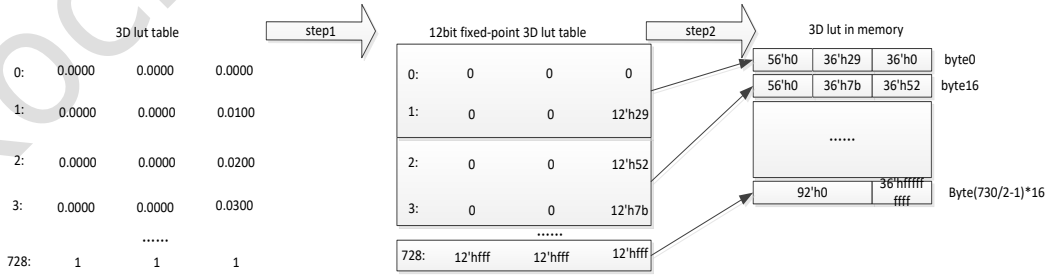

Fig.3-22 3D LUT table sorting diagram

3.4.4.9 Timing description

A. Progressive timing configuration

The POST*_PROC registers need to configure:

- VOP_DSP_HTOTAL_HS_END
- VOP_DSP_HACT_ST_END
- VOP_DSP_VTOTAL_VS_END

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- VOP_DSP_VACT_ST_END

B. p timing chart example

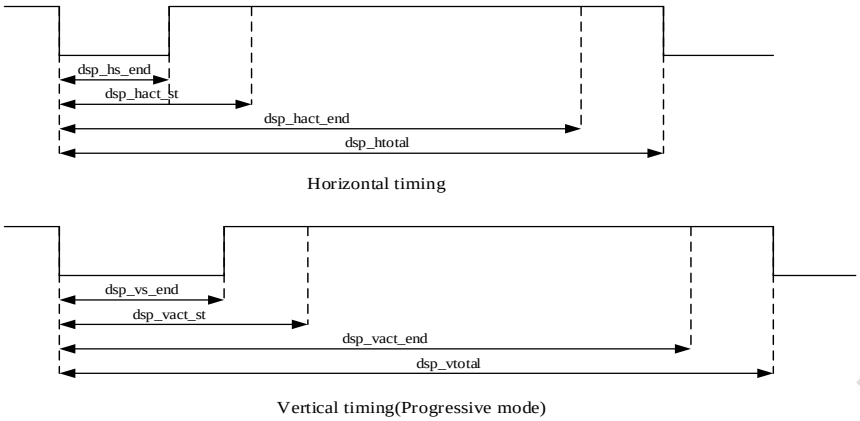

Fig.3-23 VOP RGB interface timing diagram (progressive mode)

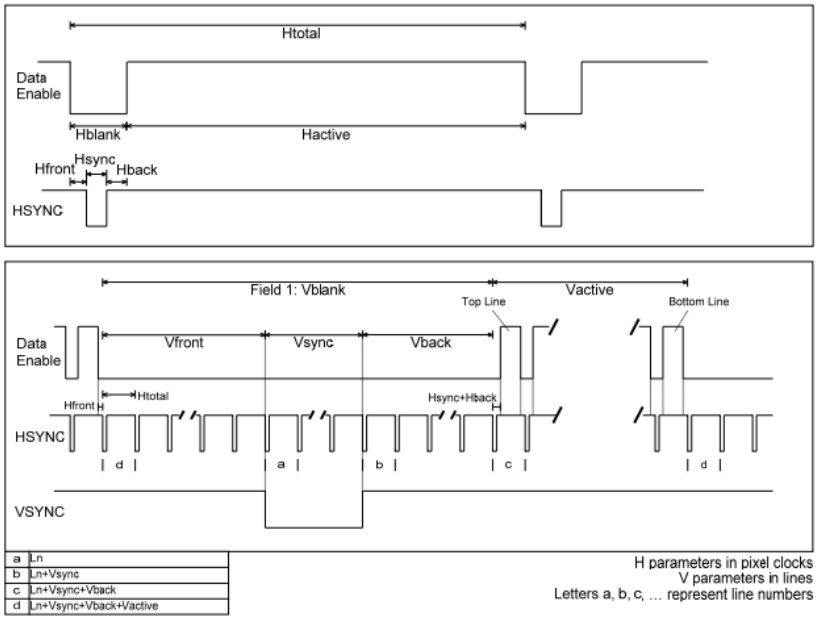

Fig.3-24 CTA-861 standard timing diagram (progressive mode)

C. Interlace timing configuration

Need to configure the following timing registers:

- VOP_DSP_HTOTAL_HS_END
- VOP_DSP_HACT_ST_END
- VOP_DSP_VTOTAL_VS_END
- VOP_DSP_VACT_ST_END
- VOP_DSP_VS_ST_END_F1
- VOP_DSP_VACT_ST_END_F1

D. i timing chart example

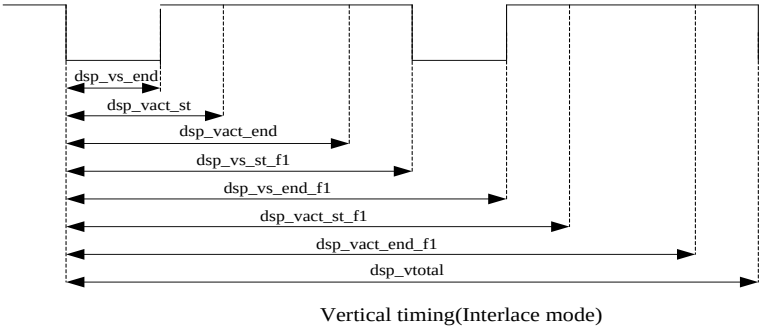

Fig.3-25 VOP RGB interface timing diagram (interlace mode)

Points to note, the starting point of the second field is at 1/2 of htotal.

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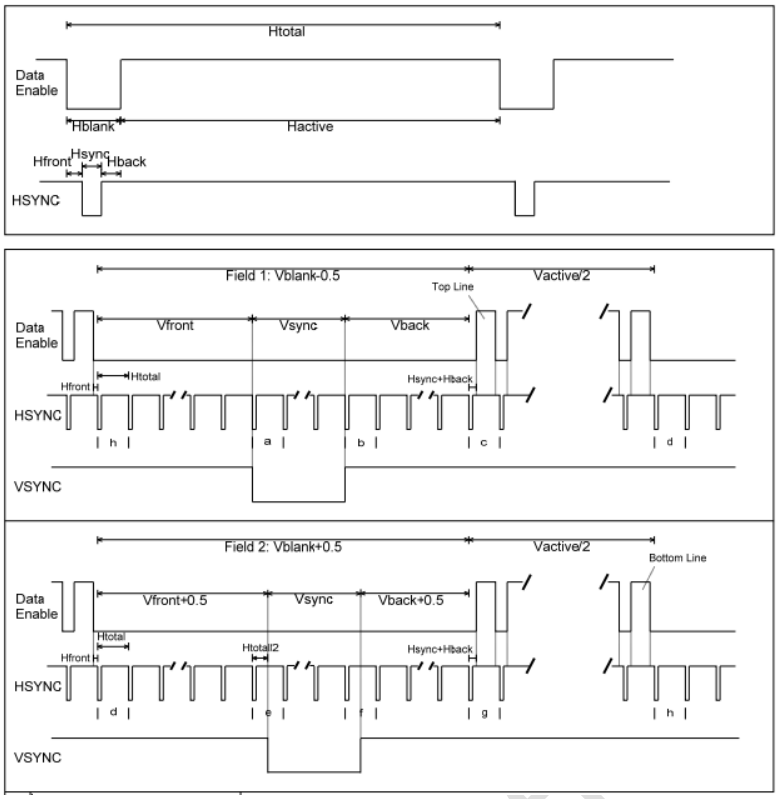


Fig.3-26 CTA-861 standard timing diagram (interlace mode)

VOP extracts the BT656 encoder module separately, the input interface is RGB parallel timing input, and the output is the standard bt656 interface output.

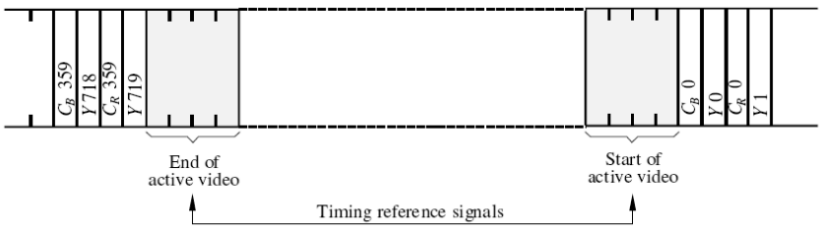
BT656 embeds the line and field synchronization information into the data stream in the form of encoding, which is the so-called Video timing reference codes. Each line includes four parts: SAV, EAV, blanking and video data:

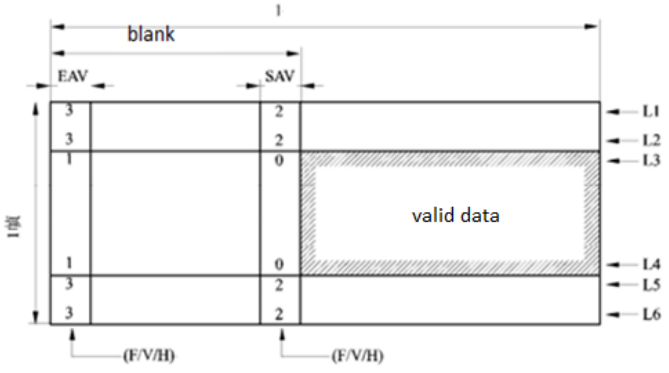
E. BT.1120/BT.656 encoder

VOP extracts the BT1120(BT656) encoder module separately, the input interface is RGB parallel timing input, and the output is the standard BT1120(BT656) interface output.

BT1120(BT656) embeds the line and field synchronization information into the data stream in the form of encoding, which is the so-called Video timing reference codes. Each line includes four parts: SAV, EAV, blanking and video data:

每一行包括SAV、EAV、blanking和video data四个部分：





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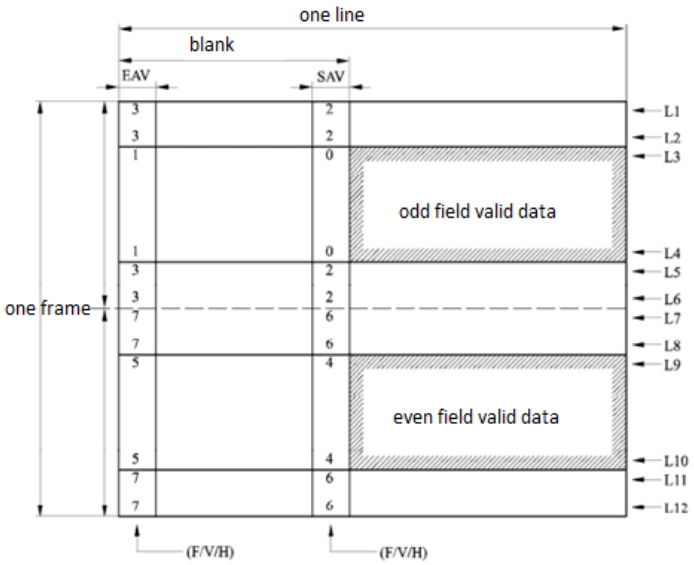

Fig.3-27 Timing description of BT1120/BT656

F. Usage Constraints

1.Pre_scan_hblank must be greater than or equal to 8;

3.5 Register Description

3.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 3-5 VOP3 Address Mapping

Base Address[15:8]	Module	Address Length	Offset Address Range
0x00	SYS_CTRL	256 BYTE	0X0000 ~ 0X00FF
0x05	OVERLAY_SYSTEM	256 BYTE	0X0500 ~ 0X05FF
0x06	OVERLAY_PORT0	256 BYTE	0X0600 ~ 0X06FF
0x07	OVERLAY_PORT1	256 BYTE	0X0700 ~ 0X07FF
0x0c	POST0	256 BYTE	0X0C00 ~ 0X0CFF
0x0d	POST1	256 BYTE	0X0D00 ~ 0X0DFF
0x18	ESMART0	512 BYTE	0X1800 ~ 0X19FF
0x1a	ESMART1	512 BYTE	0X1A00 ~ 0X1BFF
0x1c	ESMART2	512 BYTE	0X1C00 ~ 0X1DFF
0x1e	ESMART3	512 BYTE	0X1E00 ~ 0X1FFF
0x50	GAMMA_LUT_ADDR	4096 BYTE	0X5000 ~ 0X5FFF
0x60	BPP_LUT_ADDR	1024 BYTE	0X6000 ~ 0X63FF
0x7e	MMU	256 BYTE	0X7E00 ~ 0X7EFF

3.5.2 Registers Summary

3.5.2.1 SYS_CTRL

Name	Offset	Size	Reset Value	Description
SYS_CTRL_REG_CFG_DONE	0x0000	W	0x00008000	Register configure done flag.
SYS_CTRL_VERSION_INFO	0x0004	W	0x00000000	RTL version.
SYS_CTRL_AUTO_GATING_CTRL_IMD	0x0008	W	0x86006900	Auto-gating control.

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Name	Offset	Size	Reset Value	Description
SYS_CTRL_WIN_REG_CFG_DONE	0x000C	W	0x00000000	Layers config done control
SYS_CTRL_AXI_CTRL0_IMD	0x0010	W	0x00000000	AXI bus control.
SYS_CTRL_AXI_HURRY_CTRL0_IMD	0x0014	W	0x00000000	AXI hurry mode control.
SYS_CTRL_AXI_OUTSTANDING_CTRL0_IMD	0x001C	W	0x00000000	AXI outstanding number control.
SYS_CTRL_AXI_LUT_CTRL_IMD	0x0024	W	0x00000000	DMA of fetching LUT control.
SYS_CTRL_DSP_INFACE_EN	0x0028	W	0x00000000	Enable display interface.
SYS_CTRL_DSP_INFACE_CTRL	0x002C	W	0x00000000	Configure bt656 and bt1120.
SYS_CTRL_DSP_INFACE_POL	0x0030	W	0x00000000	The polarity of interface control.
SYS_CTRL_VAR_FERQ_CTRL_IMD	0x0038	W	0x00000000	The address is used to bypass MCU command.
SYS_CTRL_WB_CTRL0	0x0040	W	0x70680000	WB control.
SYS_CTRL_WB_XSPD_FACTOR	0x0044	W	0x00000000	The scale factor of WB configure.
SYS_CTRL_WB_YRGB_MST	0x0048	W	0x00000000	WB YRGB memory starting address.
SYS_CTRL_WB_CBR_MST	0x004C	W	0x00000000	WB CbCr memory starting address.
SYS_CTRL_LUT_PORT_SEL	0x0058	W	0x0C000000	Select the video output for LUT.
SYS_CTRL_STATUS0	0x0060	W	0x00000000	The system status of video output0.
SYS_CTRL_STATUS1	0x0064	W	0x00000000	The system status of video output1.
SYS_CTRL_LINE_FLAG0	0x0070	W	0x00000000	Set the line flag of video output0.
SYS_CTRL_LINE_FLAG1	0x0074	W	0x00000000	Set the line flag of video output1.
SYS_CTRL_INTR_EN	0x0080	W	0x00000000	Enable system0 interrupt.
SYS_CTRL_INTR_CLR	0x0084	W	0x00000000	Clear system0 interrupt.
SYS_CTRL_INTR_STATUS	0x0088	W	0x00000000	System0 interrupt status.
SYS_CTRL_INTR_RAW_STATUS	0x008C	W	0x00000000	System0 interrupt raw status.
SYS_CTRL_PORT0_INTR_EN	0x00A0	W	0x00000000	Enable video output0 interrupt.
SYS_CTRL_PORT0_INTR_CLR	0x00A4	W	0x00000000	Clear video output0 interrupt.
SYS_CTRL_PORT0_INTR_STATUS	0x00A8	W	0x00000000	Video output0 interrupt status.
SYS_CTRL_PORT0_INTR_RAW_STATUS	0x00AC	W	0x00000000	Video output0 interrupt raw status.
SYS_CTRL_PORT1_INTR_EN	0x00B0	W	0x00000000	Enable video output1 interrupt.
SYS_CTRL_PORT1_INTR_CLR	0x00B4	W	0x00000000	Clear video output1 interrupt.
SYS_CTRL_PORT1_INTR_STATUS	0x00B8	W	0x00000000	Video output1 interrupt status.
SYS_CTRL_PORT1_INTR_RAW_STATUS	0x00BC	W	0x00000000	Video output1 interrupt raw status.

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*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2.2 OVERLAY_SYSTEM

Name	Offset	Size	Reset Value	Description
OVERLAY_SYSTEM_PORT_SEL_IMD	0x0004	W	0x11000000	OVERLAY layer select
OVERLAY_SYSTEM_GATING_EN_IMD	0x0008	W	0x00000000	OVERLAY clk gating
OVERLAY_SYSTEM_ESMART0_CTRL	0x0020	W	0x0000001B	ESMART0 delay_num
OVERLAY_SYSTEM_ESMART1_CTRL	0x0024	W	0x0000001B	ESMART1 delay_num
OVERLAY_SYSTEM_ESMART2_CTRL	0x0028	W	0x0000001B	ESMART2 delay_num
OVERLAY_SYSTEM_ESMART3_CTRL	0x002C	W	0x0000001B	ESMART3 delay_num

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2.3 OVERLAY_PORT0

Name	Offset	Size	Reset Value	Description
OVERLAY_PORT0_CTRL	0x0000	W	0x00000000	Overlay_ctrl config set
OVERLAY_PORT0_LAYER_SEL	0x0004	W	0x00000010	Overlay_Layer_select
OVERLAY_PORT0_MIX0_SRC_COLOR_CTRL	0x0020	W	0x00000000	MIX0 configure the source color
OVERLAY_PORT0_MIX0_DST_COLOR_CTRL	0x0024	W	0x00000000	MIX0 configure the destination color
OVERLAY_PORT0_MIX0_SRC_ALPHA_CTRL	0x0028	W	0x00000000	MIX0 configure the source alpha
OVERLAY_PORT0_MIX0_DST_ALPHA_CTRL	0x002C	W	0x00000000	MIX0 configure the destination alpha
OVERLAY_PORT0_MIX1_SRC_COLOR_CTRL	0x0030	W	0x00000000	MIX1 configure the source color
OVERLAY_PORT0_MIX1_DST_COLOR_CTRL	0x0034	W	0x00000000	MIX1 configure the destination color
OVERLAY_PORT0_MIX1_SRC_ALPHA_CTRL	0x0038	W	0x00000000	MIX1 configure the source alpha
OVERLAY_PORT0_MIX1_DST_ALPHA_CTRL	0x003C	W	0x00000000	MIX1 configure the destination alpha
OVERLAY_PORT0_MIX2_SRC_COLOR_CTRL	0x0040	W	0x00000000	MIX2 configure the source color
OVERLAY_PORT0_MIX2_DST_COLOR_CTRL	0x0044	W	0x00000000	MIX2 configure the destination color
OVERLAY_PORT0_MIX2_SRC_ALPHA_CTRL	0x0048	W	0x00000000	MIX2 configure the source alpha
OVERLAY_PORT0_MIX2_DST_ALPHA_CTRL	0x004C	W	0x00000000	MIX2 configure the destination alpha
OVERLAY_PORT0_BG_MIX_CTRL	0x0070	W	0x2B000000	OVERLAY_port0 delay_num

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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3.5.2.4 OVERLAY_PORT1

Name	Offset	Size	Reset Value	Description
OVERLAY_PORT1_CTRL	0x0000	W	0x00000000	Overlay_ctrl config set
OVERLAY_PORT1_LAYER_SEL	0x0004	W	0x00000010	Overlay_Layer_select
OVERLAY_PORT1_MIX0_SRC_COLOR_CTRL	0x0020	W	0x00000000	MIX0 configure the source color
OVERLAY_PORT1_MIX0_DST_COLOR_CTRL	0x0024	W	0x00000000	MIX0 configure the destination color
OVERLAY_PORT1_MIX0_SRC_ALPHA_CTRL	0x0028	W	0x00000000	MIX0 configure the source alpha
OVERLAY_PORT1_MIX0_DST_ALPHA_CTRL	0x002C	W	0x00000000	MIX0 configure the destination alpha
OVERLAY_PORT1_MIX1_SRC_COLOR_CTRL	0x0030	W	0x00000000	MIX1 configure the source color
OVERLAY_PORT1_MIX1_DST_COLOR_CTRL	0x0034	W	0x00000000	MIX1 configure the destination color
OVERLAY_PORT1_MIX1_SRC_ALPHA_CTRL	0x0038	W	0x00000000	MIX1 configure the source alpha
OVERLAY_PORT1_MIX1_DST_ALPHA_CTRL	0x003C	W	0x00000000	MIX1 configure the destination alpha
OVERLAY_PORT1_MIX2_SRC_COLOR_CTRL	0x0040	W	0x00000000	MIX2 configure the source color
OVERLAY_PORT1_MIX2_DST_COLOR_CTRL	0x0044	W	0x00000000	MIX2 configure the destination color
OVERLAY_PORT1_MIX2_SRC_ALPHA_CTRL	0x0048	W	0x00000000	MIX2 configure the source alpha
OVERLAY_PORT1_MIX2_DST_ALPHA_CTRL	0x004C	W	0x00000000	MIX2 configure the destination alpha
OVERLAY_PORT1_BG_MIX_CTRL	0x0070	W	0x2B000000	OVERLAY_port0 delay_num

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2.5 POST0

Name	Offset	Size	Reset Value	Description
POST0_CTRL_DSP_CTRL	0x0000	W	0x8000000F	The display mode of video output0 control.
POST0_CTRL_COLOR_CTRL	0x0008	W	0x00000000	Control color bar.
POST0_CTRL_3D_LUT_CTRL	0x0010	W	0x00000000	Control 3D LUT.
POST0_CTRL_3D_LUT_R	0x0014	W	0x00000000	Configure the red component of 3D LUT.
POST0_CTRL_3D_LUT_G	0x0018	W	0x00000000	Configure the green component of 3D LUT.
POST0_CTRL_3D_LUT_B	0x001C	W	0x00000000	Configure the blue component of 3D LUT.
POST0_CTRL_3DLUT_MST	0x0020	W	0x00000000	Configure the starting address of 3D LUT in memory.
POST0_CTRL_DSP_BG	0x002C	W	0x00000000	Configure the background color of video output0.
POST0_CTRL_PRE_SCAN_HTIMING	0x0030	W	0x00000000	Configure the pre-process timing of video output0.

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Name	Offset	Size	Reset Value	Description
POST0_CTRL_DSP_HACT_INFO	0x0034	W	0x00000000	Configure the post-process horizontal timing of video output port.
POST0_CTRL_DSP_VACT_INFO	0x0038	W	0x00000000	Configure the post-process vertical timing of video output port.
POST0_CTRL_SCL_FACTOR_YRGB	0x003C	W	0x00000000	Configure the post-process vertical timing of video output port.
POST0_CTRL_SCL_CTRL	0x0040	W	0x00000000	Post scale enable.
POST0_CTRL_DSP_VACT_INFO_F1	0x0044	W	0x00000000	Configure the interlace vertical timing of video output0.
POST0_CTRL_DSP_HTOTAL_HS_END	0x0048	W	0x00000000	Configure the horizontal timing of video output0.
POST0_CTRL_DSP_HACT_ST_END	0x004C	W	0x00000000	Configure the horizontal timing of video output0.
POST0_CTRL_DSP_VTOTAL_VS_END	0x0050	W	0x00000000	Configure the vertical timing of video output0.
POST0_CTRL_DSP_VACT_ST_END	0x0054	W	0x00000000	Configure the vertical timing of video output0.
POST0_CTRL_DSP_VS_ST_END_F1	0x0058	W	0x00000000	Configure the interlace vertical timing of video output0.
POST0_CTRL_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	Configure the interlace vertical timing of video output0.
POST0_CTRL_BCSH_CTRL	0x0060	W	0x00000000	Control BCSH.
POST0_CTRL_BCSH_BCS	0x0064	W	0x00000000	Configure the brightness, contrast, sat and output mode of BCSH.
POST0_CTRL_BCSH_H	0x0068	W	0x00000000	Configure the hue of BCSH.
POST0_CTRL_BCSH_COLOR_BAR	0x006C	W	0x00000000	Enable BCSH.
POST0_CTRL_MCU_CTRL	0x00F8	W	0x00000000	MCU interface control.
POST0_CTRL_MCU_RW_BYPASS_PORT	0x00FC	W	0x00000000	MCU write_data_bypass.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2.6 POST1

Name	Offset	Size	Reset Value	Description
POST1_CTRL_DSP_CTRL	0x0000	W	0x8000000F	The display mode of video output0 control.
POST1_CTRL_COLOR_CTRL	0x0008	W	0x00000000	Control color bar.
POST1_CTRL_DSP_BG	0x002C	W	0x00000000	Configure the background color of video output0.
POST1_CTRL_PRE_SCAN_HTIMING	0x0030	W	0x00000000	Configure the pre-process timing of video output0.
POST1_CTRL_DSP_HACT_INFO	0x0034	W	0x00000000	Configure the post-process horizontal timing of video output port.
POST1_CTRL_DSP_VACT_INFO	0x0038	W	0x00000000	Configure the post-process vertical timing of video output port.

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Name	Offset	Size	Reset Value	Description
POST1_CTRL_SCL_FACTOR_YRGB	0x003C	W	0x00000000	Configure the post-process vertical timing of video output port.
POST1_CTRL_SCL_CTRL	0x0040	W	0x00000000	Post scale enable.
POST1_CTRL_DSP_VACT_INFO_F1	0x0044	W	0x00000000	Configure the interlace vertical timing of video output0.
POST1_CTRL_DSP_HTOTAL_HS_END	0x0048	W	0x00000000	Configure the horizontal timing of video output0.
POST1_CTRL_DSP_HACT_ST_END	0x004C	W	0x00000000	Configure the horizontal timing of video output0.
POST1_CTRL_DSP_VTOTAL_VS_END	0x0050	W	0x00000000	Configure the vertical timing of video output0.
POST1_CTRL_DSP_VACT_ST_END	0x0054	W	0x00000000	Configure the vertical timing of video output0.
POST1_CTRL_DSP_VS_ST_END_F1	0x0058	W	0x00000000	Configure the interlace vertical timing of video output0.
POST1_CTRL_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	Configure the interlace vertical timing of video output0.
POST1_CTRL_BCSH_CTRL	0x0060	W	0x00000000	Control BCSH.
POST1_CTRL_BCSH_BCS	0x0064	W	0x00000000	Configure the brightness, contrast, sat and output mode of BCSH.
POST1_CTRL_BCSH_H	0x0068	W	0x00000000	Configure the hue of BCSH.
POST1_CTRL_BCSH_COLOR_BAR	0x006C	W	0x00000000	Enable BCSH.
POST1_CTRL_MCU_CTRL	0x00F8	W	0x00000000	MCU interface control.
POST1_CTRL_MCU_RW_BYPASS_PORT	0x00FC	W	0x00000000	MCU write_data_bypass.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2.7 ESMART0

Name	Offset	Size	Reset Value	Description
ESMART0_CTRL0	0x0000	W	0x00000000	Enable the color space convertion of esmart.
ESMART0_CTRL1	0x0004	W	0x0330B0AC	Control the dma of esmart.
ESMART0_AXI_CTRL	0x0008	W	0x00000000	Esmart axi control.
ESMART0_REGION0_MST_CTL	0x0010	W	0x00000000	Enable the region0 of esmart.
ESMART0_REGION0_MST_YRGB	0x0014	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART0_REGION0_MST_CBCR	0x0018	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART0_REGION0_VIR	0x001C	W	0x00000000	Configure the virtual width of data in memory.
ESMART0_REGION0_ACT_INFO	0x0020	W	0x00000000	Configure the active size of data.
ESMART0_REGION0_DSP_INFO	0x0024	W	0x00000000	Configure the dsiplay size of data.
ESMART0_REGION0_DSP_OFFSET	0x0028	W	0x00000000	Configure the dsiplay offset of data.
ESMART0_REGION0_SCL_CTRL	0x0030	W	0x00000000	Enable the scaling of esmart.

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Name	Offset	Size	Reset Value	Description
ESMART0_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	Configure the scaling factor of YRGB.
ESMART0_REGION0_SCL_OFFSET	0x003C	W	0x00000000	Configure the scaling offset of esmart.
ESMART0_REGION1_MST_CTL	0x0040	W	0x00000000	Enable the region0 of esmart.
ESMART0_REGION1_MST_YRGB	0x0044	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART0_REGION1_MST_CBCR	0x0048	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART0_REGION1_VIR	0x004C	W	0x00000000	Configure the virtual width of data in memory.
ESMART0_REGION1_ACT_INFO	0x0050	W	0x00000000	Configure the active size of data.
ESMART0_REGION1_DSP_INFO	0x0054	W	0x00000000	Configure the dsiplay size of data.
ESMART0_REGION1_DSP_OFFSET	0x0058	W	0x00000000	Configure the dsiplay offset of data.
ESMART0_REGION1_SCL_CTRL	0x0060	W	0x00000000	Enable the scaling of esmart.
ESMART0_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	Configure the scaling factor of YRGB.
ESMART0_REGION1_SCL_OFFSET	0x006C	W	0x00000000	Configure the scaling offset of esmart.
ESMART0_REGION2_MST_CTL	0x0070	W	0x00000000	Enable the region0 of esmart.
ESMART0_REGION2_MST_YRGB	0x0074	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART0_REGION2_MST_CBCR	0x0078	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART0_REGION2_VIR	0x007C	W	0x00000000	Configure the virtual width of data in memory.
ESMART0_REGION2_ACT_INFO	0x0080	W	0x00000000	Configure the active size of data.
ESMART0_REGION2_DSP_INFO	0x0084	W	0x00000000	Configure the dsiplay size of data.
ESMART0_REGION2_DSP_OFFSET	0x0088	W	0x00000000	Configure the dsiplay offset of data.
ESMART0_REGION2_SCL_CTRL	0x0090	W	0x00000000	Enable the scaling of esmart.
ESMART0_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	Configure the scaling factor of YRGB.
ESMART0_REGION2_SCL_OFFSET	0x009C	W	0x00000000	Configure the scaling offset of esmart.
ESMART0_REGION3_MST_CTL	0x00A0	W	0x00000000	Enable the region0 of esmart.
ESMART0_REGION3_MST_YRGB	0x00A4	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART0_REGION3_MST_CBCR	0x00A8	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART0_REGION3_VIR	0x00AC	W	0x00000000	Configure the virtual width of data in memory.
ESMART0_REGION3_ACT_INFO	0x00B0	W	0x00000000	Configure the active size of data.

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Name	Offset	Size	Reset Value	Description
ESMART0_REGION3_DSP_INFO	0x00B4	W	0x00000000	Configure the dsiplay size of data.
ESMART0_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	Configure the dsiplay offset of data.
ESMART0_REGION3_SCL_CTRL	0x00C0	W	0x00000000	Enable the scaling of esmart.
ESMART0_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	Configure the scaling factor of YRGB.
ESMART0_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	Configure the scaling offset of esmart.
ESMART0_KEY_CTRL	0x00D0	W	0x00000000	Configure the color key of esmart.
ESMART0_BG_EN	0x00D4	W	0x00000000	Enable the background of esmart.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2.8 ESMART1

Name	Offset	Size	Reset Value	Description
ESMART1_CTRL0	0x0000	W	0x00000000	Enable the color space convertion of esmart.
ESMART1_CTRL1	0x0004	W	0x0330B0AC	Control the dma of esmart.
ESMART1_AXI_CTRL	0x0008	W	0x00000000	Esmart axi control.
ESMART1_REGION0_MST_CTL	0x0010	W	0x00000000	Enable the region0 of esmart.
ESMART1_REGION0_MST_YRGB	0x0014	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART1_REGION0_MST_CBCR	0x0018	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART1_REGION0_VIR	0x001C	W	0x00000000	Configure the virtual width of data in memory.
ESMART1_REGION0_ACT_INFO	0x0020	W	0x00000000	Configure the active size of data.
ESMART1_REGION0_DSP_INFO	0x0024	W	0x00000000	Configure the dsiplay size of data.
ESMART1_REGION0_DSP_OFFSET	0x0028	W	0x00000000	Configure the dsiplay offset of data.
ESMART1_REGION0_SCL_CTRL	0x0030	W	0x00000000	Enable the scaling of esmart.
ESMART1_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	Configure the scaling factor of YRGB.
ESMART1_REGION0_SCL_OFFSET	0x003C	W	0x00000000	Configure the scaling offset of esmart.
ESMART1_REGION1_MST_CTL	0x0040	W	0x00000000	Enable the region0 of esmart.
ESMART1_REGION1_MST_YRGB	0x0044	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART1_REGION1_MST_CBCR	0x0048	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART1_REGION1_VIR	0x004C	W	0x00000000	Configure the virtual width of data in memory.
ESMART1_REGION1_ACT_INFO	0x0050	W	0x00000000	Configure the active size of data.
ESMART1_REGION1_DSP_INFO	0x0054	W	0x00000000	Configure the dsiplay size of data.

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Name	Offset	Size	Reset Value	Description
ESMART1_REGION1_DSP_OFFSET	0x0058	W	0x00000000	Configure the dsiplay offset of data.
ESMART1_REGION1_SCL_CTRL	0x0060	W	0x00000000	Enable the scaling of esmart.
ESMART1_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	Configure the scaling factor of YRGB.
ESMART1_REGION1_SCL_OFFSET	0x006C	W	0x00000000	Configure the scaling offset of esmart.
ESMART1_REGION2_MST_CTL	0x0070	W	0x00000000	Enable the region0 of esmart.
ESMART1_REGION2_MST_YRGB	0x0074	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART1_REGION2_MST_CBCR	0x0078	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART1_REGION2_VIR	0x007C	W	0x00000000	Configure the virtual width of data in memory.
ESMART1_REGION2_ACT_INFO	0x0080	W	0x00000000	Configure the active size of data.
ESMART1_REGION2_DSP_INFO	0x0084	W	0x00000000	Configure the dsiplay size of data.
ESMART1_REGION2_DSP_OFFSET	0x0088	W	0x00000000	Configure the dsiplay offset of data.
ESMART1_REGION2_SCL_CTRL	0x0090	W	0x00000000	Enable the scaling of esmart.
ESMART1_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	Configure the scaling factor of YRGB.
ESMART1_REGION2_SCL_OFFSET	0x009C	W	0x00000000	Configure the scaling offset of esmart.
ESMART1_REGION3_MST_CTL	0x00A0	W	0x00000000	Enable the region0 of esmart.
ESMART1_REGION3_MST_YRGB	0x00A4	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART1_REGION3_MST_CBCR	0x00A8	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART1_REGION3_VIR	0x00AC	W	0x00000000	Configure the virtual width of data in memory.
ESMART1_REGION3_ACT_INFO	0x00B0	W	0x00000000	Configure the active size of data.
ESMART1_REGION3_DSP_INFO	0x00B4	W	0x00000000	Configure the dsiplay size of data.
ESMART1_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	Configure the dsiplay offset of data.
ESMART1_REGION3_SCL_CTRL	0x00C0	W	0x00000000	Enable the scaling of esmart.
ESMART1_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	Configure the scaling factor of YRGB.
ESMART1_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	Configure the scaling offset of esmart.
ESMART1_KEY_CTRL	0x00D0	W	0x00000000	Configure the color key of esmart.
ESMART1_BG_EN	0x00D4	W	0x00000000	Enable the background of esmart.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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3.5.2.9 ESMART2

Name	Offset	Size	Reset Value	Description
ESMART2_CTRL0	0x0000	W	0x00000000	Enable the color space convertion of esmart.
ESMART2_CTRL1	0x0004	W	0x0330B0AC	Control the dma of esmart.
ESMART2_AXI_CTRL	0x0008	W	0x00000000	Esmart axi control.
ESMART2_REGION0_MST_CTL	0x0010	W	0x00000000	Enable the region0 of esmart.
ESMART2_REGION0_MST_YRGB	0x0014	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART2_REGION0_MST_CBCR	0x0018	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART2_REGION0_VIR	0x001C	W	0x00000000	Configure the virtual width of data in memory.
ESMART2_REGION0_ACT_INFO	0x0020	W	0x00000000	Configure the active size of data.
ESMART2_REGION0_DSP_INFO	0x0024	W	0x00000000	Configure the dsiplay size of data.
ESMART2_REGION0_DSP_OFFSET	0x0028	W	0x00000000	Configure the dsiplay offset of data.
ESMART2_REGION0_SCL_CTRL	0x0030	W	0x00000000	Enable the scaling of esmart.
ESMART2_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	Configure the scaling factor of YRGB.
ESMART2_REGION0_SCL_OFFSET	0x003C	W	0x00000000	Configure the scaling offset of esmart.
ESMART2_REGION1_MST_CTL	0x0040	W	0x00000000	Enable the region0 of esmart.
ESMART2_REGION1_MST_YRGB	0x0044	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART2_REGION1_MST_CBCR	0x0048	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART2_REGION1_VIR	0x004C	W	0x00000000	Configure the virtual width of data in memory.
ESMART2_REGION1_ACT_INFO	0x0050	W	0x00000000	Configure the active size of data.
ESMART2_REGION1_DSP_INFO	0x0054	W	0x00000000	Configure the dsiplay size of data.
ESMART2_REGION1_DSP_OFFSET	0x0058	W	0x00000000	Configure the dsiplay offset of data.
ESMART2_REGION1_SCL_CTRL	0x0060	W	0x00000000	Enable the scaling of esmart.
ESMART2_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	Configure the scaling factor of YRGB.
ESMART2_REGION1_SCL_OFFSET	0x006C	W	0x00000000	Configure the scaling offset of esmart.
ESMART2_REGION2_MST_CTL	0x0070	W	0x00000000	Enable the region0 of esmart.
ESMART2_REGION2_MST_YRGB	0x0074	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART2_REGION2_MST_CBCR	0x0078	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART2_REGION2_VIR	0x007C	W	0x00000000	Configure the virtual width of data in memory.

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Name	Offset	Size	Reset Value	Description
ESMART2_REGION2_ACT_INFO	0x0080	W	0x00000000	Configure the active size of data.
ESMART2_REGION2_DSP_INFO	0x0084	W	0x00000000	Configure the dsiplay size of data.
ESMART2_REGION2_DSP_OFFSET	0x0088	W	0x00000000	Configure the dsiplay offset of data.
ESMART2_REGION2_SCL_CTRL	0x0090	W	0x00000000	Enable the scaling of esmart.
ESMART2_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	Configure the scaling factor of YRGB.
ESMART2_REGION2_SCL_OFFSET	0x009C	W	0x00000000	Configure the scaling offset of esmart.
ESMART2_REGION3_MST_CTL	0x00A0	W	0x00000000	Enable the region0 of esmart.
ESMART2_REGION3_MST_YRGB	0x00A4	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART2_REGION3_MST_CBCR	0x00A8	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART2_REGION3_VIR	0x00AC	W	0x00000000	Configure the virtual width of data in memory.
ESMART2_REGION3_ACT_INFO	0x00B0	W	0x00000000	Configure the active size of data.
ESMART2_REGION3_DSP_INFO	0x00B4	W	0x00000000	Configure the dsiplay size of data.
ESMART2_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	Configure the dsiplay offset of data.
ESMART2_REGION3_SCL_CTRL	0x00C0	W	0x00000000	Enable the scaling of esmart.
ESMART2_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	Configure the scaling factor of YRGB.
ESMART2_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	Configure the scaling offset of esmart.
ESMART2_KEY_CTRL	0x00D0	W	0x00000000	Configure the color key of esmart.
ESMART2_BG_EN	0x00D4	W	0x00000000	Enable the background of esmart.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2.10 ESMART3

Name	Offset	Size	Reset Value	Description
ESMART3_CTRL0	0x0000	W	0x00000000	Enable the color space convertion of esmart.
ESMART3_CTRL1	0x0004	W	0x0330B0AC	Control the dma of esmart.
ESMART3_AXI_CTRL	0x0008	W	0x00000000	Esmart axi control.
ESMART3_REGION0_MST_CTL	0x0010	W	0x00000000	Enable the region0 of esmart.
ESMART3_REGION0_MST_YRGB	0x0014	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART3_REGION0_MST_CBCR	0x0018	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART3_REGION0_VIR	0x001C	W	0x00000000	Configure the virtual width of data in memory.
ESMART3_REGION0_ACT_INFO	0x0020	W	0x00000000	Configure the active size of data.

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Name	Offset	Size	Reset Value	Description
ESMART3_REGION0_DSP_INFO	0x0024	W	0x00000000	Configure the dsiplay size of data.
ESMART3_REGION0_DSP_OFFSET	0x0028	W	0x00000000	Configure the dsiplay offset of data.
ESMART3_REGION0_SCL_CTRL	0x0030	W	0x00000000	Enable the scaling of esmart.
ESMART3_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	Configure the scaling factor of YRGB.
ESMART3_REGION0_SCL_OFFSET	0x003C	W	0x00000000	Configure the scaling offset of esmart.
ESMART3_REGION1_MST_CTL	0x0040	W	0x00000000	Enable the region0 of esmart.
ESMART3_REGION1_MST_YRGB	0x0044	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART3_REGION1_MST_CBCR	0x0048	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART3_REGION1_VIR	0x004C	W	0x00000000	Configure the virtual width of data in memory.
ESMART3_REGION1_ACT_INFO	0x0050	W	0x00000000	Configure the active size of data.
ESMART3_REGION1_DSP_INFO	0x0054	W	0x00000000	Configure the dsiplay size of data.
ESMART3_REGION1_DSP_OFFSET	0x0058	W	0x00000000	Configure the dsiplay offset of data.
ESMART3_REGION1_SCL_CTRL	0x0060	W	0x00000000	Enable the scaling of esmart.
ESMART3_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	Configure the scaling factor of YRGB.
ESMART3_REGION1_SCL_OFFSET	0x006C	W	0x00000000	Configure the scaling offset of esmart.
ESMART3_REGION2_MST_CTL	0x0070	W	0x00000000	Enable the region0 of esmart.
ESMART3_REGION2_MST_YRGB	0x0074	W	0x00000000	Configure the starting address of YRGB in memory.
ESMART3_REGION2_MST_CBCR	0x0078	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART3_REGION2_VIR	0x007C	W	0x00000000	Configure the virtual width of data in memory.
ESMART3_REGION2_ACT_INFO	0x0080	W	0x00000000	Configure the active size of data.
ESMART3_REGION2_DSP_INFO	0x0084	W	0x00000000	Configure the dsiplay size of data.
ESMART3_REGION2_DSP_OFFSET	0x0088	W	0x00000000	Configure the dsiplay offset of data.
ESMART3_REGION2_SCL_CTRL	0x0090	W	0x00000000	Enable the scaling of esmart.
ESMART3_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	Configure the scaling factor of YRGB.
ESMART3_REGION2_SCL_OFFSET	0x009C	W	0x00000000	Configure the scaling offset of esmart.
ESMART3_REGION3_MST_CTL	0x00A0	W	0x00000000	Enable the region0 of esmart.
ESMART3_REGION3_MST_YRGB	0x00A4	W	0x00000000	Configure the starting address of YRGB in memory.

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Name	Offset	Size	Reset Value	Description
ESMART3_REGION3_MST_CBCR	0x00A8	W	0x00000000	Configure the starting address of CBCR in memory.
ESMART3_REGION3_VIR	0x00AC	W	0x00000000	Configure the virtual width of data in memory.
ESMART3_REGION3_ACT_INFO	0x00B0	W	0x00000000	Configure the active size of data.
ESMART3_REGION3_DSP_INFO	0x00B4	W	0x00000000	Configure the dsiplay size of data.
ESMART3_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	Configure the dsiplay offset of data.
ESMART3_REGION3_SCL_CTRL	0x00C0	W	0x00000000	Enable the scaling of esmart.
ESMART3_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	Configure the scaling factor of YRGB.
ESMART3_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	Configure the scaling offset of esmart.
ESMART3_KEY_CTRL	0x00D0	W	0x00000000	Configure the color key of esmart.
ESMART3_BG_EN	0x00D4	W	0x00000000	Enable the background of esmart.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2.11 MMU

Name	Offset	Size	Reset Value	Description
MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address.
MMU_STATUS	0x0004	W	0x00000000	MMU status register.
MMU_COMMAND	0x0008	W	0x00000000	MMU command register.
MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault.
MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register.
MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register.
MMU_INT_CLEAR	0x0018	W	0x00000000	MMU interrupt clear register.
MMU_INT_MASK	0x001C	W	0x00000000	MMU interrupt mask register.
MMU_INT_STATUS	0x0020	W	0x00000000	MMU interrupt status register.
MMU_AUTO_GATING	0x0024	W	0x00000000	MMU auto gating.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.3 Detail Register Description

3.5.3.1 SYS_CTRL

SYS_CTRL_REG_CFG_DONE

Address: Operational Base(0x00000000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15	RW	0x1	sw_global_regdone_en Global regdone enable. 1'b0: Disable 1'b1: Enable
14	RW	0x0	reg_load_wb_en In the first setting of the register, the new value was saved into the mirror register. When all the wb register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

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Bit	Attr	Reset Value	Description
13:6	RO	0x00	reserved
5	RW	0x0	reg_load_sys1_en In the first setting of the register, the new value was saved into the mirror register. When all the system1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_sys0_en In the first setting of the register, the new value was saved into the mirror register. When all the system0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3:2	RO	0x0	reserved
1	RW	0x0	reg_load_global1_en In the first setting of the register, the new value was saved into the mirror register. When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
0	RW	0x0	reg_load_global0_en In the first setting of the register, the new value was saved into the mirror register.When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

SYS_CTRL_VERSION_INFO

Address: Operational Base(0x00000000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	major Used for IP structure.
23:16	RW	0x00	minor Big feature change under same structure.
15:0	RW	0x0000	svnbuild RTL current svn number.

SYS_CTRL_AUTO_GATING_CTRL_IMD

Address: Operational Base(0x00000000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x1	auto_gating_en 1'b0: Disable auto gating 1'b1: Enable auto gating Default auto gating enable.
30	RO	0x0	reserved
29	RW	0x0	AXI_aclk_static_auto_gating_en If AXI is not used, AXI_aclk_gating_en and AXI_aclk_static_gating_en can be enabled to reduce power consumption. 1'b0: Disable 1'b1: Enable
28:27	RO	0x0	reserved
26	RW	0x1	port1_aclk_static_auto_gating_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
25	RW	0x1	port0_aclk_static_auto_gating_en 1'b0: Disable 1'b1: Enable
24:16	RO	0x000	reserved
15	RW	0x0	AXI_aclk_auto_gating_en 1'b0: Disable 1'b1: Enable
14	RW	0x1	port_dclk_auto_gating_en 1'b0: Disable 1'b1: Enable
13	RW	0x1	prescan_aclk_auto_gating_en 1'b0: Disable 1'b1: Enable
12	RO	0x0	reserved
11	RW	0x1	wb_aclk_auto_gating_en 1'b0: Disable 1'b1: Enable
10	RO	0x0	reserved
9	RW	0x0	gamma_dclk_auto_gating_en 1'b0: Disable 1'b1: Enable
8	RW	0x1	overlay_aclk_auto_gating_en 1'b0: Disable 1'b1: Enable
7:5	RO	0x0	reserved
4	RW	0x0	esmart_scl_auto_gating_en 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

SYS_CTRL_WIN_REG_CFG_DONE

Address: Operational Base(0x00000000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15:8	RO	0x00	reserved
7	RW	0x0	reg_load_esmart3_en In the first setting of the register, the new value was saved into the mirror register. When all the smart1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
6	RW	0x0	reg_load_esmart2_en In the first setting of the register, the new value was saved into the mirror register. When all the smart1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
5	RW	0x0	reg_load_esmart1_en In the first setting of the register, the new value was saved into the mirror register. When all the smart1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

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Bit	Attr	Reset Value	Description
4	RW	0x0	reg_load_esmart0_en In the first setting of the register, the new value was saved into the mirror register. When all the smart1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3:0	RO	0x0	reserved

SYS_CTRL_AXI_CTRL0_IMD

Address: Operational Base(0x00000000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	AXI_dma_stop Stop AXI dma. 1'b0: Disable 1'b1: Enable

SYS_CTRL_AXI_HURRY_CTRL0_IMD

Address: Operational Base(0x00000000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:13	RW	0x0	AXI_qos_value Noc qos value
12	RW	0x0	AXI_qos_en Noc qos enable. 1'b0: Disable 1'b1: Enable
11	RW	0x0	AXI_hurry_threshold Noc hurry threshold value.
10:9	RW	0x0	AXI_hurry_value Noc hurry value.
8	RW	0x0	AXI_hurry_en Noc hurry enable. 1'b0: Disable 1'b1: Enable
7:5	RO	0x0	reserved
4:3	RW	0x0	AXI_hurry_w_mode 2'b00: Noc_hurry_w disable 2'b01: Left 1/4 fifo empty 2'b10: Left 1/2 fifo empty 2'b11: Left 3/4 fifo empty
2:1	RW	0x0	AXI_hurry_w_value Noc hurry value. 2'b00: Low priority 2'b11: High priority
0	RW	0x0	AXI_hurry_w_en Noc hurry enable.

SYS_CTRL_AXI_OUTSTANDING_CTRL0_IMD

Address: Operational Base(0x00000000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x00	AXI_outstanding_num AXI bus max outstanding number.
2:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	AXI_outstanding_en AXI bus max outstanding enable. 1'b0: Disable 1'b1: Enable

SYS_CTRL_AXI_LUT_CTRL_IMD

Address: Operational Base(0x00000000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RW	0x0	mmu_bypass_en If AXI rid>mmu_bypass_id,bypass mmu. 1'b0: Disable 1'b1: Enable
30:26	RW	0x00	mmu_bypass_id If AXI rid>mmu_bypass_id,bypass mmu.
25:20	RO	0x0	reserved
19:18	RW	0x0	mmu_regdone_sel 1'b0: Disable 1'b1: Enable
17:14	RO	0x0	reserved
13	RW	0x0	vp1_interlace_frm_reg_done Video output1 reg done framd valid. 1'b0: Reg done every field for interlace 1'b1: Reg done every frame for interlace
12	RW	0x0	vp0_interlace_frm_reg_done Video output0 reg done framd valid. 1'b0: Reg done every field for interlace 1'b1: Reg done every frame for interlace
11:8	RO	0x0	reserved
7:4	RW	0x0	lut_dma_rid LUT AXI read id. VP0 lut AXI id=lut_dma_rid VP1 lut AXI id=lut_dma_rid+1
3:2	RW	0x0	lut_dma_rlen LUT AXI read brust. 2'b00: Burst16 2'b01: Burst8 2'b1x: Burst4
1	RW	0x0	lut_dma_stop Stop LUT dma. 1'b0: Disable 1'b1: Enable
0	RW	0x0	lut_dma_en Enable LUT dma. 1'b0: Disable 1'b1: Enable

SYS_CTRL_DSP_INFACE_EN

Address: Operational Base(0x00000000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	lvds_inface_mux Select the display output of LVDS interface. 2'b00: Video output 2'b01: Video output

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Bit	Attr	Reset Value	Description
17:16	RW	0x0	mipi_inface_mux Select the display output of MIPI interface. 2'b00: Video output 2'b01: Video output
15:10	RO	0x00	reserved
9:8	RW	0x0	rgb_inface_mux Select the display output of RGB interface. 2'b00: Video output 2'b01: Video output
7	RW	0x0	bt656_out_en 1'b0: Gating output clk,data and control signal 1'b1: Bt656 interface enable
6	RW	0x0	bt1120_out_en 1'b0: Gating output clk,data and control signal 1'b1: Bt1120 interface enable
5	RW	0x0	lvds_out_en 1'b0: Gating output clk,data and control signal 1'b1: Lvds interface enable
4	RW	0x0	mipi_out_en 1'b0: Gating output clk,data and control signal 1'b1: Mipi interface enable
3:1	RO	0x0	reserved
0	RW	0x0	rgb_out_en 1'b0: Gating output clk,data and control signal 1'b1: Rgb interface enable

SYS_CTRL_DSP_INFACE_CTRL

Address: Operational Base(0x00000000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	bt1120_yc_swap Swap gray and color component. 1'b0: Disable 1'b1: Enable
8	RW	0x0	bt1120_uv_swap Swap U and V component. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	bt656_yc_swap Swap GRAY and COLOR component of BT656. 1'b0: Disable 1'b1: Enable
4	RW	0x0	bt656_uv_swap Swap U and V component of BT656. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

SYS_CTRL_DSP_INFACE_POL

Address: Operational Base(0x00000000) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	regdone_sel Select interface control register regdone. 2'b00: Video output0 2'b01: Video output1
29	RO	0x0	reserved
28	RW	0x0	regdone_imd_en Enable interface control register regdone immediately.
27:15	RO	0x000	reserved
14	RW	0x0	mipi_den_pol 1'b0: Negative 1'b1: Positive
13	RW	0x0	mipi_vsync_pol 1'b0: Negative 1'b1: Positive
12	RW	0x0	mipi_hsync_pol 1'b0: Negative 1'b1: Positive
11:3	RO	0x00	reserved
2	RW	0x0	rgb_lvds_den_pol 1'b0: Negative 1'b1: Positive
1	RW	0x0	rgb_lvds_vsync_pol 1'b0: Negative 1'b1: Positive
0	RW	0x0	rgb_lvds_hsync_pol 1'b0: Negative 1'b1: Positive

SYS_CTRL_VAR_FERQ_CTRL_IMD

Address: Operational Base(0x00000000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	reserved
29	RW	0x0	vp1_almost_full_or_en 1'b0: Disable 1'b1: Enable
28	RW	0x0	vp0_almost_full_or_en 1'b0: Disable 1'b1: Enable
27:26	RW	0x0	reserved
25	RW	0x0	vp1_dsp_hold_or_en 1'b0: Disable 1'b1: Enable
24	RW	0x0	vp0_dsp_hold_or_en 1'b0: Disable 1'b1: Enable
23:22	RW	0x0	reserved
21	RW	0x0	vp1_line_flag_or_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	vp0_line_flag_or_en 1'b0: Disable 1'b1: Enable
19	RW	0x0	wb_dma_finish_or_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
18	RW	0x0	axi_dma_finish_or_en 1'b0: Disable 1'b1: Enable
17:14	RW	0x0	reserved
13	RW	0x0	vp1_almost_full_and_en 1'b0: Disable 1'b1: Enable
12	RW	0x0	vp0_almost_full_and_en 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	reserved
9	RW	0x0	vp1_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	vp0_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	reserved
5	RW	0x0	vp1_line_flag_and_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	vp0_line_flag_and_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	wb_dma_finish_and_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	axi_dma_finish_and_en 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	dma_finish_mode 2'b00: Src_or 2'b01: Src_and 2'b10: Src_or && src_and 2'b11: Src_or || src_and

SYS_CTRL_WB_CTRL0

Address: Operational Base(0x00000000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0xe	wb_uv_id Use default 0xd.
26:23	RO	0x0	reserved
22:19	RW	0xd	wb_yrgb_id Use default 0xc.
18:13	RO	0x00	reserved
12	RW	0x0	wb_oneframe_mode 1'b0: Disable 1'b1: Enable
11	RW	0x0	wb_handshake_mode 1'b0: Full handshake 1'b1: Half handshake
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	wb_ythrow_mode 1'b0: Throw odd line 1'b1: Throw even line
8	RW	0x0	wb_ythrow_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	wb_xpsd_bil_en 1'b0: Enable scale 1'b1: Disable scale
6	RW	0x0	wb_rgb2yuv_mode 1'b0: BT601 1'b1: BT709
5	RW	0x0	wb_rgb2yuv_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	wb_dither_en When wb_fmt is RGB565. 1'b0: No dither, RGB888 clip to RGB565 1'b1: With dither,RGB888 dither to RGB565
3:1	RW	0x0	wb_fmt 3'b000: ARGB888 3'b001: RGB888 3'b010: RGB565 3'b100: YcbCr420 Others: Reserved
0	RW	0x0	wb_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_WB_XSPD_FACTOR

Address: Operational Base(0x00000000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	wb_xpsd_bil_factor Factor=((src_width[11:0])/(dst_width[11:0]))*2^12.
15:10	RO	0x00	reserved
9:0	RW	0x000	fifo_thold When wb_fifo_wcnt < fifo_thold, hold the pre_scan timing. fifo_thold = wb_width * fmt_byte / 16. 3'b000: ARGB888, fmt_byte = 4 3'b001: RGB888, fmt_byte = 3 3'b010: RGB565, fmt_byte = 2 3'b100: YcbCr420, fmt_byte = 1

SYS_CTRL_WB_YRGB_MST

Address: Operational Base(0x00000000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_yrgb_mst YRGB mst address.

SYS_CTRL_WB_CBR_MST

Address: Operational Base(0x00000000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_cbr_mst CBR mst adress.

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SYS_CTRL_LUT_PORT_SEL

Address: Operational Base(0x00000000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RW	0x3	esmart_lb_mode 2'b00: One 8k mode 2'b01: Two 4k mode 2'b10: One 4k + 2 1080p mode 2'b11: 4 1080p mode
25:10	RO	0x0000	reserved
9:8	RW	0x0	wb_port_sel Select WB display output. 2'b00: Video output0 2'b01: Video output1
7:5	RW	0x0	bpp_win_sel Select 8BPP lut esmart num. 2'b00: Esmart0 2'b01: Esmart1 2'b10: Esmart0 2'b11: Esmart1
4	RW	0x0	bpp_lut_en Enable 8BPP LUT. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

SYS_CTRL_STATUS0

Address: Operational Base(0x00000000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt0 Read the video output0 vertical counter.
15:2	RO	0x0000	reserved
1	RW	0x0	mmu_idle MMU idle status.
0	RW	0x0	dma_stop_valid0 AXI dma stop status.

SYS_CTRL_STATUS1

Address: Operational Base(0x00000000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt1 Read the video output1 vertical counter.
15:2	RO	0x0000	reserved
1	RW	0x0	mmu_idle MMU idle status.
0	RW	0x0	dma_stop_valid1 AXI dma stop status.

SYS_CTRL_LINE_FLAG0

Address: Operational Base(0x00000000) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1,intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_LINE_FLAG1

Address: Operational Base(0x00000000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1,intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_INTR_EN

Address: Operational Base(0x00000000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits. When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15:8	RO	0x00	reserved
7	RW	0x0	intr_en_mmu 1'b0: Disable 1'b1: Enable
6	RO	0x0	reserved
5	RW	0x0	int_en_wb_finish 1'b0: Disable 1'b1: Enable
4	RW	0x0	int_en_wb_yrgb_fifo_full 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en_wb_uv_fifo_full 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_dma0_finish 1'b0: Disable 1'b1: Enable
1	RW	0x0	intr_en_bus0_error 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

SYS_CTRL_INTR_CLR

Rockchip Confidential

Address: Operational Base(0x00000000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_clr_mmu Interrupt clear(Auto clear).
6	RO	0x0	reserved
5	RW	0x0	intr_clr_wb_dma_finish WB_DMA finish interrupt clear(Auto clear).
4	RW	0x0	intr_clr_wb_yrgb_fifo_full Interrupt clear(Auto clear).
3	RW	0x0	intr_clr_wb_uv_fifo_full Interrupt clear(Auto clear).
2	RW	0x0	intr_clr_dma_finish DMA finish interrupt clear(Auto clear).
1	RW	0x0	intr_clr_bus_error Bus error Interrupt clear(Auto clear).
0	RO	0x0	reserved

SYS_CTRL_INTR_STATUS

Address: Operational Base(0x00000000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_status_mmu Interrupt status of MMU. 1'b0: Disable 1'b1: Mmu intr flag
6	RO	0x0	reserved
5	RW	0x0	intr_status_wb_dma_finish Interrupt status. 1'b0: Disable 1'b1: Wb_dma intr flag
4	RW	0x0	intr_status_wb_yrgb_fifo_full Interrupt status. 1'b0: Disable 1'b1: Wb_yrgb_fifo_full intr flag
3	RW	0x0	intr_status_wb_uv_fifo_full Interrupt status. 1'b0: Disable 1'b1: Wb_uv_fifo_full intr flag
2	RW	0x0	intr_status_dma_finish DMA finish interrupt status. 1'b0: Disable 1'b1: Dma_finish intr flag
1	RW	0x0	intr_status_bus_error Bus error Interrupt clear status. 1'b0: Disable 1'b1: Bus_error intr flag
0	RO	0x0	reserved

SYS_CTRL_INTR_RAW_STATUS

Address: Operational Base(0x00000000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	intr_raw_status_mmu Interrupt of MMU raw status.
6	RO	0x0	reserved
5	RW	0x0	intr_raw_status_wb_dma_finish Interrupt raw status.
4	RW	0x0	intr_raw_status_wb_yrgb_fifo_full Interrupt raw status.
3	RW	0x0	intr_raw_status_wb_uv_fifo_full Interrupt raw status.
2	RW	0x0	intr_raw_status_dma_finish DMA finish interrupt raw status.
1	RW	0x0	intr_raw_status_bus_error Bus error Interrupt raw status.
0	RO	0x0	reserved

SYS_CTRL_PORT0_INTR_EN

Address: Operational Base(0x00000000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x0	reserved
9	RW	0x0	intr_en_post_full Post buffer almost full interrupt 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp Display vfp interrupt 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid Display hold valid interrupt 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field Field start interrupt clear 1'b0: Disable 1'b1: Clean post field start interrupt
4	RW	0x0	intr_en_post_buf_empty Post buffer empty interrupt 1'b0: Disable 1'b1: Clean post buffer empty start interrupt
3	RW	0x0	intr_en_line_flag1 Line flag 1 Interrupt 1'b0: Disable 1'b1: Clean line flag 0 start interrupt
2	RW	0x0	intr_en_line_flag0 Line flag 0 Interrupt 1'b0: Disable 1'b1: Clean line flag 0 start interrupt
1	RW	0x0	intr_en_fs_new Frame new start interrupt 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RW	0x0	intr_en_fs Frame start interrupt 1'b0: Disable 1'b1: Enable

SYS_CTRL_PORT0_INTR_CLR

Address: Operational Base(0x00000000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean post buffer almost full interrupt
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display vfp interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean display vfp interrupt
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean display hold valid interrupt
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear). 1'b0: Disable 1'b1: Clean post field start interrupt
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean post buffer empty start interrupt
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean line flag 1 start interrupt
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean line flag 0 start interrupt
1	RW	0x0	intr_clr_fs_new Frame new start interrupt clear (Auto clear). 1'b0: Disable 1'b1: Clean frame new start interrupt
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear). 1'b0: Disable 1'b1: Clean frame start interrupt

SYS_CTRL_PORT0_INTR_STATUS

Address: Operational Base(0x00000000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.

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Bit	Attr	Reset Value	Description
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display vfp interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RW	0x0	intr_status_fs_new Frame new start interrupt status.
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT0_INTR_RAW_STATUS

Address: Operational Base(0x00000000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display vfp interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RW	0x0	intr_raw_status_fs_new Frame new start interrupt raw status.
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

SYS_CTRL_PORT1_INTR_EN

Address: Operational Base(0x00000000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full Post buffer almost full interrupt. 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	intr_en_vfp Display vfp interrupt. 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid Display hold valid interrupt. 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field Field start interrupt. 1'b0: disable 1'b1: enable
4	RW	0x0	intr_en_post_buf_empty Post buffer empty interrupt. 1'b0: disable 1'b1: enable
3	RW	0x0	intr_en_line_flag1 Line flag 1 Interrupt 1'b0: disable 1'b1: enable
2	RW	0x0	intr_en_line_flag0 Line flag 0 Interrupt 1'b0: disable 1'b1: enable
1	RO	0x0	intr_en_fs_new Frame new start interrupt 1'b0: disable 1'b1: enable
0	RW	0x0	intr_en_fs Frame start interrupt 1'b0: disable 1'b1: enable

SYS_CTRL_PORT1_INTR_CLR

Address: Operational Base(0x00000000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean post buffer almost full interrupt
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display vfp interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean display vfp interrupt
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean display hold valid interrupt

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear). 1'b0: Disable 1'b1: Clean post field start interrupt
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean post buffer empty start interrupt
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean line flag 1 start interrupt
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear). 1'b0: Disable 1'b1: Clean line flag 0 start interrupt
1	RW	0x0	intr_clr_fs_new Frame new start interrupt clear (Auto clear). 1'b0: Disable 1'b1: Clean frame new start interrupt
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear). 1'b0: Disable 1'b1: Clean frame start interrupt

SYS_CTRL_PORT1_INTR_STATUS

Address: Operational Base(0x00000000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display vfp interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RW	0x0	intr_status_fs_new Frame new start interrupt status.
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT1_INTR_RAW_STATUS

Address: Operational Base(0x00000000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display vfp interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RW	0x0	intr_raw_status_fs_new Frame new start interrupt raw status.
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

3.5.3.2 OVERLAY_SYSTEM

OVERLAY_SYSTEM_PORT_SEL_IMD

Address: Operational Base(0x00000500) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x1	Esmart3_port_sel 2'b00: Video output0 2'b01: Video output1 Others: Reserved
27:26	RO	0x0	reserved
25:24	RW	0x1	Esmart2_port_sel 2'b00: Video output0 2'b01: Video output1 Others: Reserved
23:22	RO	0x0	reserved
21:20	RW	0x0	Esmart1_port_sel 2'b00: Video output0 2'b01: Video output1 Others: Reserved
19:18	RO	0x0	reserved
17:16	RW	0x0	Esmart0_port_sel 2'b00: Video output0 2'b01: Video output1 Others: Reserved
15:0	RO	0x0000	reserved

OVERLAY_SYSTEM_GATING_EN_IMD

Address: Operational Base(0x00000500) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	overlay_auto_gating_en 1'b0: Disable 1'b1: Enable

OVERLAY_SYSTEM_ESMART0_CTRL

Address: Operational Base(0x00000500) + offset (0x0020)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1b	esmart_dly_num Esmart delay cycle number.

OVERLAY_SYSTEM_ESMART1_CTRL

Address: Operational Base(0x00000500) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1b	esmart_dly_num Esmart delay cycle number.

OVERLAY_SYSTEM_ESMART2_CTRL

Address: Operational Base(0x00000500) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1b	esmart_dly_num Esmart delay cycle number.

OVERLAY_SYSTEM_ESMART3_CTRL

Address: Operational Base(0x00000500) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1b	esmart_dly_num Esmart delay cycle number.

3.5.3.3 OVERLAY_PORT0

OVERLAY_PORT0_CTRL

Address: Operational Base(0x00000600) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay

OVERLAY_PORT0_LAYER_SEL

Address: Operational Base(0x00000600) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	layer3_sel Layer3 select port. 4'b0000: Esmart0 4'b0001: Esmart1 4'b0010: Esmart2 4'b0011: Esmart3 4'b1xxx: None
11:8	RW	0x0	layer2_sel Layer2 select port. 4'b0000: Esmart0 4'b0001: Esmart1 4'b0010: Esmart2 4'b0011: Esmart3 4'b1xxx: None

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Bit	Attr	Reset Value	Description
7:4	RW	0x1	layer1_sel Layer1 select port. 4'b0000: Esmart0 4'b0001: Esmart1 4'b0010: Esmart2 4'b0011: Esmart3 4'b1xxx: None
3:0	RW	0x0	layer0_sel Layer0 select port. 4'b0000: Esmart0 4'b0001: Esmart1 4'b0010: Esmart2 4'b0011: Esmart3 4'b1xxx: None

OVERLAY_PORT0_MIX0_SRC_COLOR_CTRL

Address: Operational Base(0x00000600) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT0_MIX0_DST_COLOR_CTRL

Address: Operational Base(0x00000600) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Ags).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT0_MIX0_SRC_ALPHA_CTRL

Address: Operational Base(0x00000600) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_MIX0_DST_ALPHA_CTRL

Address: Operational Base(0x00000600) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_MIX1_SRC_COLOR_CTRL

Address: Operational Base(0x00000600) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT0_MIX1_DST_COLOR_CTRL

Address: Operational Base(0x00000600) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Ags).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT0_MIX1_SRC_ALPHA_CTRL

Address: Operational Base(0x00000600) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_MIX1_DST_ALPHA_CTRL

Address: Operational Base(0x00000600) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_MIX2_SRC_COLOR_CTRL

Address: Operational Base(0x00000600) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT0_MIX2_DST_COLOR_CTRL

Address: Operational Base(0x00000600) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Ags).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT0_MIX2_SRC_ALPHA_CTRL

Address: Operational Base(0x00000600) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_MIX2_DST_ALPHA_CTRL

Address: Operational Base(0x00000600) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_BG_MIX_CTRL

Rockchip Confidencial

Address: Operational Base(0x00000600) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x2b	bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	bg_global_alpha Source global alpha value(Ags).
7:4	RO	0x0	reserved
3	RW	0x0	bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
2	RW	0x0	bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	bg_alpha_mode Select source alpha. 1'b0: Global alpha 1'b1: Per_pixel alpha
0	RW	0x0	bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

3.5.3.4 OVERLAY_PORT1

OVERLAY_PORT1_CTRL

Address: Operational Base(0x00000700) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5	RW	0x1	sdr2hdr_en 1'b0: SDR2HDR disable 1'b1: SDR2HDR enable *This bit must set "0"
4	RW	0x1	hdr10_en 1'b0: HDR10 disable 1'b1: HDR10 enable *This bit must set "0"
3:1	RO	0x0	reserved
0	RW	0x0	overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay

OVERLAY_PORT1_LAYER_SEL

Address: Operational Base(0x00000700) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	layer3_sel Layer3 select port. 4'b0000: Esmart0 4'b0001: Esmart1 4'b0010: Esmart2 4'b0011: Esmart3 4'b1xxx: None

Rockchip Confidencial

Bit	Attr	Reset Value	Description
11:8	RW	0x0	layer2_sel Layer2 select port. 4'b0000: Esmart0 4'b0001: Esmart1 4'b0010: Esmart2 4'b0011: Esmart3 4'b1xxx: None
7:4	RW	0x1	layer1_sel Layer1 select port. 4'b0000: Esmart0 4'b0001: Esmart1 4'b0010: Esmart2 4'b0011: Esmart3 4'b1xxx: None
3:0	RW	0x0	layer0_sel Layer0 select port. 4'b0000: Esmart0 4'b0001: Esmart1 4'b0010: Esmart2 4'b0011: Esmart3 4'b1xxx: None

OVERLAY_PORT1_MIX0_SRC_COLOR_CTRL

Address: Operational Base(0x00000700) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT1_MIX0_DST_COLOR_CTRL

Address: Operational Base(0x00000700) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Ags).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT1_MIX0_SRC_ALPHA_CTRL

Address: Operational Base(0x00000700) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT1_MIX0_DST_ALPHA_CTRL

Address: Operational Base(0x00000700) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT1_MIX1_SRC_COLOR_CTRL

Rockchip Confidencial

Address: Operational Base(0x00000700) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT1_MIX1_DST_COLOR_CTRL

Address: Operational Base(0x00000700) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Ags).
15:8	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT1_MIX1_SRC_ALPHA_CTRL

Address: Operational Base(0x00000700) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

Rockchip Confidencial

OVERLAY_PORT1_MIX1_DST_ALPHA_CTRL

Address: Operational Base(0x00000700) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT1_MIX2_SRC_COLOR_CTRL

Address: Operational Base(0x00000700) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT1_MIX2_DST_COLOR_CTRL

Address: Operational Base(0x00000700) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Ags).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cs 1'b1: Cs*As0"

OVERLAY_PORT1_MIX2_SRC_ALPHA_CTRL

Rockchip Confidencial

Address: Operational Base(0x00000700) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT1_MIX2_DST_ALPHA_CTRL

Address: Operational Base(0x00000700) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags Others: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 Others: Reserved
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

Rockchip Confidencial

OVERLAY_PORT1_BG_MIX_CTRL

Address: Operational Base(0x00000700) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x2b	bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	bg_global_alpha Source global alpha value(Ags).
7:4	RO	0x0	reserved
3	RW	0x0	bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
2	RW	0x0	bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	bg_alpha_mode Select source alpha. 1'b0: Global alpha 1'b1: Per_pixel alpha
0	RW	0x0	bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

3.5.3.5 POST0

POST0_CTRL_DSP_CTRL

Address: Operational Base(0x00000C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x1	vop_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000). 1'b0: Disable 1'b1: Enable
26	RW	0x0	dsp_out_zero 1'b0: Normal output 1'b1: All output '0'
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the Hsync/Vsync/Den output is blank. 1'b0: Disable 1'b1: Enable
23	RW	0x0	post_lb_mode 1'b0: 4x2048 1'b1: 8x1024 if post_act_width > 2048 post_lb_mode =0;else config 0 or 1.
22	RW	0x0	gamma_update_en 1'b0: Disable 1'b1: Enable
21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
19:18	RW	0x0	dither_down_sel 2'b0: Allegro 2'b1: FRC
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	pre_dither_down_en 10bit->8bit (allegro). 1'b0: Disable 1'b1: Enable
15	RW	0x0	dsp_out_rgb_yuv 1'b0: Out rgb_black 1'b1: Out yuv_black
14	RO	0x0	reserved
13	RW	0x0	dsp_x_mir_en 1'b0: Disable x_mirror 1'b1: Enable x_mirror
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: Dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: Disable 1'b1: Enable *See detail description in Delta display charpter.

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Bit	Attr	Reset Value	Description
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: Normal 1'b1: Invert
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RW	0x0	dsp_core_dclk_sel 1'b0: Dclk_core = dclk 1'b1: Dclk_core = dclk/2
3:0	RW	0xf	dsp_out_mode 4'b0000: Parallel 24-bit output {R[7:0],G[7:0],B[7:0]} 4'b0001: Parallel 18-bit RGB666 output {R[5:0],2'b0,G[5:0],2'b0,B[5:0],2'b0} 4'b0010: Parallel 16-bit RGB565 output {R[4:0],3'b0,G[5:0],2'b0,B[4:0],3'b0} 4'b1000: Serial 3x8-bit output {dsp_out_data[7:3],3'b0,dsp_out_data[2:0], dsp_out_data[7:5],2'b0,dsp_out_data[4:0],3'b0} Others: Reserved

POST0_CTRL_COLOR_CTRL

Address: Operational Base(0x00000C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: Horizontal mode 1'b1: Vertical mode
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

POST0_CTRL_3D_LUT_CTRL

Address: Operational Base(0x00000C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_3dlut_addr AHB write or read lut address of 3d_lut.
15:5	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	dsp_3dlut_gating_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	dsp_3dlut_mode 1'b0: Lut is fetched by AXI 1'b1: Lut is fetched by AHB
2	RW	0x0	dsp_3dlut_update_en Update the lut of 3d_lut. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dsp_3dlut_bypass_en Bypass 3d_lut fuction. 1'b0: Disable 1'b1: Enable
0	RW	0x0	dsp_3dlut_en 1'b0: Disable 1'b1: Enable

POST0_CTRL_3D_LUT_R

Address: Operational Base(0x00000C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_r_comp 3d_lut red component.

POST0_CTRL_3D_LUT_G

Address: Operational Base(0x00000C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_g_comp 3d_lut green component.

POST0_CTRL_3D_LUT_B

Address: Operational Base(0x00000C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_b_comp 3d_lut blue component.

POST0_CTRL_3DLUT_MST

Address: Operational Base(0x00000C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	post_3dlut_mst 3d_lut memory start address.

POST0_CTRL_DSP_BG

Address: Operational Base(0x00000C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bg_bypass_display_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.

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Bit	Attr	Reset Value	Description
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

POST0_CTRL_PRE_SCAN_HTIMING

Address: Operational Base(0x00000C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

POST0_CTRL_DSP_HACT_INFO

Address: Operational Base(0x00000C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	post_hact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	post_hact_end_post Panel display scanning horizontal active end point.

POST0_CTRL_DSP_VACT_INFO

Address: Operational Base(0x00000C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	post_vact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	post_vact_end_post Panel display scanning horizontal active end point.

POST0_CTRL_SCL_FACTOR_YRGB

Address: Operational Base(0x00000C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	post_vs_factor Factor=((src_height[31:16])/(dst_height[31:16]))*2^12.
15:12	RO	0x0	reserved
11:0	RW	0x000	post_hs_factor Factor=((src_width[15:0])/(dst_width[15:0]))*2^12.

POST0_CTRL_SCL_CTRL

Address: Operational Base(0x00000C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	post0_ver_sd_en 1'b0: Post ver scl down disable 1'b1: Post ver scl down enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	post0_hor_sd_en 1'b0: Post hor scl down disable 1'b1: Post hor scl down enable

POST0_CTRL_DSP_VACT_INFO_F1

Address: Operational Base(0x00000C00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

POST0_CTRL_DSP_HTOTAL_HS_END

Address: Operational Base(0x00000C00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hs_end Panel display scanning hsync pulse width.

POST0_CTRL_DSP_HACT_ST_END

Address: Operational Base(0x00000C00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end Panel display scanning horizontal active end point.

POST0_CTRL_DSP_VTOTAL_VS_END

Address: Operational Base(0x00000C00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: Valid after frame start 1'b1: Valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end Panel display scanning vsync pulse width.

POST0_CTRL_DSP_VACT_ST_END

Address: Operational Base(0x00000C00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st Panel display scanning vertical active start point.

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end Panel display scanning vertical active end point.

POST0_CTRL_DSP_VS_ST_END_F1

Address: Operational Base(0x00000C00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

POST0_CTRL_DSP_VACT_ST_END_F1

Address: Operational Base(0x00000C00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

POST0_CTRL_BCSH_CTRL

Address: Operational Base(0x00000C00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0: Bypass 1'b1: Enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved
0	RW	0x0	bcsh_y2r_en 1'b0: Bypass 1'b1: Enable

POST0_CTRL_BCSH_BCS

Address: Operational Base(0x00000C00) + offset (0x0064)

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	out_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
29:20	RW	0x000	sat_con Saturation*Contrast*256: {0,1.992*1.992}.
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: {0,1.992}.
7:0	RW	0x00	brightness Brightness: {-32,31}.

POST0_CTRL_BCSH_H

Address: Operational Base(0x00000C00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	cos_hue Cos hue value.
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue Sin hue value.

POST0_CTRL_BCSH_COLOR_BAR

Address: Operational Base(0x00000C00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bcsh_en 1'b0: Bcsh bypass 1'b1: Bcsh enable
30	RO	0x0	reserved
29:20	RW	0x000	color_bar_v V component value of BCSH color bar.
19:10	RW	0x000	color_bar_u U component value of BCSH color bar.
9:0	RW	0x000	color_bar_y Y component value of BCSH color bar.

POST0_CTRL_MCU_CTRL

Address: Operational Base(0x00000C00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output SELECT
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE Select
29	RW	0x0	mcu_rs MCU LCD RS Select 1'b0: Command 1'b1: Data
28	RW	0x0	mcu_frame_st Write"1": MCU HOLD Mode Frame Start Read: MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26:20	RW	0x00	mcu_rw_pend MCU_RW signal end point (0-63).

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	mcu_rw_pst MCU_RW signal start point (0-15).
15:10	RW	0x00	mcu_cs_pend MCU_CS signal end point (0-63).
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15).
5:0	RW	0x00	mcu_pix_total MCU LCD Interface writing period (1-63).

POST0_CTRL_MCU_RW_BYPASS_PORT

Address: Operational Base(0x00000C00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mcu_write_data_bypass MCU write bypass data.

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POST1_CTRL_DSP_CTRL

Address: Operational Base(0x00000D00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x1	vop_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000). 1'b0: Disable 1'b1: Enable
26	RW	0x0	dsp_out_zero 1'b0: Normal output 1'b1: All output '0'

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Bit	Attr	Reset Value	Description
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the Hsync/Vsync/Den output is blank. 1'b0: Disable 1'b1: Enable
23	RW	0x0	post_lb_mode 1'b0: 4x2048 1'b1: 8x1024 if post_act_width > 2048 post_lb_mode =0;else config 0 or 1.
22	RW	0x0	gamma_update_en 1'b0: Disable 1'b1: Enable
21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
19:18	RW	0x0	dither_down_sel 2'b0: Allegro 2'b1: FRC
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	pre_dither_down_en 10bit->8bit (allegro). 1'b0: Disable 1'b1: Enable
15	RW	0x0	dsp_out_rgb_yuv 1'b0: Out rgb_black 1'b1: Out yuv_black
14	RO	0x0	reserved
13	RW	0x0	dsp_x_mir_en 1'b0: Disable x_mirror 1'b1: Enable x_mirror
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: Dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: Disable 1'b1: Enable *See detail description in Delta display charpter.
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: Normal 1'b1: Invert

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Bit	Attr	Reset Value	Description
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RW	0x0	dsp_core_dclk_sel 1'b0: Dclk_core = dclk 1'b1: Dclk_core = dclk/2
3:0	RW	0xf	dsp_out_mode 4'b0000: Parallel 24-bit output {R[7:0],G[7:0],B[7:0]} 4'b0001: Parallel 18-bit RGB666 output {R[5:0],2'b0,G[5:0],2'b0,B[5:0],2'b0} 4'b0010: Parallel 16-bit RGB565 output {R[4:0],3'b0,G[5:0],2'b0,B[4:0],3'b0} 4'b1000: Serial 3x8-bit output {dsp_out_data[7:3],3'b0,dsp_out_data[2:0], dsp_out_data[7:5],2'b0,dsp_out_data[4:0],3'b0} Others: Reserved

POST1_CTRL_COLOR_CTRL

Address: Operational Base(0x00000D00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: Horizontal mode 1'b1: Vertical mode
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

POST1_CTRL_DSP_BG

Address: Operational Base(0x00000D00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bg_bypass_display_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

POST1_CTRL_PRE_SCAN_HTIMING

Address: Operational Base(0x00000D00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

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POST1_CTRL_DSP_HACT_INFO

Address: Operational Base(0x00000D00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	post_hact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	post_hact_end_post Panel display scanning horizontal active end point.

POST1_CTRL_DSP_VACT_INFO

Address: Operational Base(0x00000D00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	post_vact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	post_vact_end_post Panel display scanning horizontal active end point.

POST1_CTRL_SCL_FACTOR_YRGB

Address: Operational Base(0x00000D00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	post_vs_factor Factor=((src_height[31:16])/(dst_height[31:16]))*2^12.
15:12	RO	0x0	reserved
11:0	RW	0x000	post_hs_factor Factor=((src_width[15:0])/(dst_width[15:0]))*2^12.

POST1_CTRL_SCL_CTRL

Address: Operational Base(0x00000D00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	post0_ver_sd_en 1'b0: Post ver scl down disable 1'b1: Post ver scl down enable
0	RW	0x0	post0_hor_sd_en 1'b0: Post hor scl down disable 1'b1: Post hor scl down enable

POST1_CTRL_DSP_VACT_INFO_F1

Address: Operational Base(0x00000D00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

POST1_CTRL_DSP_HTOTAL_HS_END

Address: Operational Base(0x00000D00) + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hs_end Panel display scanning hsync pulse width.

POST1_CTRL_DSP_HACT_ST_END

Address: Operational Base(0x00000D00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end Panel display scanning horizontal active end point.

POST1_CTRL_DSP_VTOTAL_VS_END

Address: Operational Base(0x00000D00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: Valid after frame start 1'b1: Valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end Panel display scanning vsync pulse width.

POST1_CTRL_DSP_VACT_ST_END

Address: Operational Base(0x00000D00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st Panel display scanning vertical active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end Panel display scanning vertical active end point.

POST1_CTRL_DSP_VS_ST_END_F1

Address: Operational Base(0x00000D00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

POST1_CTRL_DSP_VACT_ST_END_F1

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Address: Operational Base(0x00000D00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

POST1_CTRL_BCSH_CTRL

Address: Operational Base(0x00000D00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0: Bypass 1'b1: Enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved
0	RW	0x0	bcsh_y2r_en 1'b0: Bypass 1'b1: Enable

POST1_CTRL_BCSH_BCS

Address: Operational Base(0x00000D00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	out_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
29:20	RW	0x000	sat_con Saturation*Contrast*256: {0,1.992*1.992}.
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: {0,1.992}.
7:0	RW	0x00	brightness Brightness: {-32,31}.

POST1_CTRL_BCSH_H

Address: Operational Base(0x00000D00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:16	RW	0x000	cos_hue Cos hue value.
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue Sin hue value.

POST1_CTRL_BCSH_COLOR_BAR

Address: Operational Base(0x00000D00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bcsh_en 1'b0: Bcsh bypass 1'b1: Bcsh enable
30	RO	0x0	reserved
29:20	RW	0x000	color_bar_v V component value of BCSH color bar.
19:10	RW	0x000	color_bar_u U component value of BCSH color bar.
9:0	RW	0x000	color_bar_y Y component value of BCSH color bar.

POST1_CTRL_MCU_CTRL

Address: Operational Base(0x00000D00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output SELECT
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE Select
29	RW	0x0	mcu_rs MCU LCD RS Select 1'b0: Command 1'b1: Data
28	RW	0x0	mcu_frame_st Write"1": MCU HOLD Mode Frame Start Read: MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26:20	RW	0x00	mcu_rw_pend MCU_RW signal end point (0-63).
19:16	RW	0x0	mcu_rw_pst MCU_RW signal start point (0-15).
15:10	RW	0x00	mcu_cs_pend MCU_CS signal end point (0-63).
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15).
5:0	RW	0x00	mcu_pix_total MCU LCD Interface writing period (1-63).

POST1_CTRL_MCU_RW_BYPASS_PORT

Address: Operational Base(0x00000D00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mcu_write_data_bypass MCU write bypass data.

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ESMART0_CTRL0

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Address: Operational Base(0x00001800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:14	RO	0x00000	reserved
13:12	RW	0x0	esmart_scl_num 2'b00: Scale engine0 2'b01: Scale engine1 2'b10: Scale engine2 2'b11: Scale engine3
11:10	RO	0x0	reserved
9	RW	0x0	esmart_endian_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte0,byte1,byte2,byte3}
8	RW	0x0	esmart_mid_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte3,byte1,byte2,byte0}
7:6	RO	0x0	reserved
5	RW	0x0	esmart_8bpp_alpha_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

ESMART0_CTRL1

Address: Operational Base(0x00001800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold.If esmart empty lb number>=esmart_dma_rreq_thold,dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x3	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x3	esmart_yrgb_gather_num The gather number of YRGB.
19:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:12	RW	0xb	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:8	RO	0x0	reserved
7:4	RW	0xa	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x1	esmart_cbcr_gather_en To enable CBCR gather transfer.
2	RW	0x1	esmart_yrgb_gather_en To enable YRGB gather transfer.
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

ESMART0_AXI_CTRL

Address: Operational Base(0x00001800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num esmart outstanding number.
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

ESMART0_REGION0_MST_CTL

Address: Operational Base(0x00001800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region0_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region0_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region0_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239

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Bit	Attr	Reset Value	Description
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

ESMART0_REGION0_MST_YRGB

Address: Operational Base(0x00001800) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

ESMART0_REGION0_MST_CBCR

Address: Operational Base(0x00001800) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address.

ESMART0_REGION0_VIR

Address: Operational Base(0x00001800) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of mst0 uv virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of mst0 yrgb virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

ESMART0_REGION0_ACT_INFO

Address: Operational Base(0x00001800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_act_heigth Win_act_height=(win0_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_height=(win0_vertical size-1)

ESMART0_REGION0_DSP_INFO

Address: Operational Base(0x00001800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width=(horizontal size-1)

ESMART0_REGION0_DSP_OFFSET

Address: Operational Base(0x00001800) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

ESMART0_REGION0_SCL_CTRL

Address: Operational Base(0x00001800) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region0_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART0_REGION0_SCL_FACTOR_YRGB

Address: Operational Base(0x00001800) + offset (0x0034)

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Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART0_REGION0_SCL_OFFSET

Address: Operational Base(0x00001800) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yscl_offset Esmart_region0 vertical scale offset.
7:0	RW	0x00	region0_yrgb_xscl_offset Esmart_region0 horizontal scale offset.

ESMART0_REGION1_MST_CTL

Address: Operational Base(0x00001800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region1_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region1_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region1_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA

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Bit	Attr	Reset Value	Description
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

ESMART0_REGION1_MST_YRGB

Address: Operational Base(0x00001800) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region1 YRGB frame buffer memory start address.

ESMART0_REGION1_MST_CBCR

Address: Operational Base(0x00001800) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region1 CBCR frame buffer memory start address.

ESMART0_REGION1_VIR

Address: Operational Base(0x00001800) + offset (0x004C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of mst1 uv virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of mst1 yrgb virtual width. ARGB888: win1_vir_width RGB888: (win1_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win1_vir_width/2) YUV: ceil(win1_vir_width/4) YUV tile: ceil(win1_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win1_vir_width/4)

ESMART0_REGION1_ACT_INFO

Address: Operational Base(0x00001800) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth Win_act_height=(win1_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_act_width Win_act_height=(win1_vertical size-1)

ESMART0_REGION1_DSP_INFO

Address: Operational Base(0x00001800) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width Dsp_width=(horizontal size-1)

ESMART0_REGION1_DSP_OFFSET

Address: Operational Base(0x00001800) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

ESMART0_REGION1_SCL_CTRL

Address: Operational Base(0x00001800) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region1_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL

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Bit	Attr	Reset Value	Description
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART0_REGION1_SCL_FACTOR_YRGB

Address: Operational Base(0x00001800) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12

Rockchip Confidencial

Bit	Attr	Reset Value	Description
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12

ESMART0_REGION1_SCL_OFFSET

Address: Operational Base(0x00001800) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yscl_offset Esmart_region1 vertical scale offset.
7:0	RW	0x00	region1_yrgb_xscl_offset Esmart_region1 horizontal scale offset.

ESMART0_REGION2_MST_CTL

Address: Operational Base(0x00001800) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region2_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region2_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region2_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

ESMART0_REGION2_MST_YRGB

Address: Operational Base(0x00001800) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region2 YRGB frame buffer memory start address.

ESMART0_REGION2_MST_CBCR

Address: Operational Base(0x00001800) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region2 CBCR frame buffer memory start address.

ESMART0_REGION2_VIR

Address: Operational Base(0x00001800) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of mst2 uv virtual width.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	region2_vir_stride Number of words of mst2 yrgb virtual width. ARGB888: win2_vir_width RGB888: (win2_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win2_vir_width/2) YUV: ceil(win2_vir_width/4) YUV tile: ceil(win2_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win2_vir_width/4)

ESMART0_REGION2_ACT_INFO

Address: Operational Base(0x00001800) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth Win_act_height=(win2_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_act_width Win_act_height=(win2_vertical size-1)

ESMART0_REGION2_DSP_INFO

Address: Operational Base(0x00001800) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width Dsp_width=(horizontal size-1)

ESMART0_REGION2_DSP_OFFSET

Address: Operational Base(0x00001800) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

ESMART0_REGION2_SCL_CTRL

Address: Operational Base(0x00001800) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region2_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL

Rockchip Confidencial

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART0_REGION2_SCL_FACTOR_YRGB

Address: Operational Base(0x00001800) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN2_ACT_INFO[15:0])/(LCDC_WIN2_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN2_ACT_INFO[15:0])/(LCDC_WIN2_DSP_INFO[15:0]))*2^12

Rockchip Confidencial

ESMART0_REGION2_SCL_OFFSET

Address: Operational Base(0x00001800) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yscl_offset Esmart_region2 vertical scale offset.
7:0	RW	0x00	region2_xscl_offset Esmart_region2 horizontal scale offset.

ESMART0_REGION3_MST_CTL

Address: Operational Base(0x00001800) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region3_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region3_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region3_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

ESMART0_REGION3_MST_YRGB

Address: Operational Base(0x00001800) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region3 YRGB frame buffer memory start address.

ESMART0_REGION3_MST_CBCR

Address: Operational Base(0x00001800) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region3 CBCR frame buffer memory start address.

ESMART0_REGION3_VIR

Address: Operational Base(0x00001800) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of mst3 uv virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of mst3 yrgb virtual width. ARGB888: win3_vir_width RGB888: (win3_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win3_vir_width/2) YUV: ceil(win3_vir_width/4) YUV tile: ceil(win3_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win3_vir_width/4)

ESMART0_REGION3_ACT_INFO

Address: Operational Base(0x00001800) + offset (0x00B0)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth Win_act_height=(win3_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_act_width Win_act_height=(win3_vertical size-1)

ESMART0_REGION3_DSP_INFO

Address: Operational Base(0x00001800) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width Dsp_width=(horizontal size-1)

ESMART0_REGION3_DSP_OFFSET

Address: Operational Base(0x00001800) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

ESMART0_REGION3_SCL_CTRL

Address: Operational Base(0x00001800) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region3_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART0_REGION3_SCL_FACTOR_YRGB

Address: Operational Base(0x00001800) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^12

ESMART0_REGION3_SCL_OFFSET

Address: Operational Base(0x00001800) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yscl_offset Esmart_region3 vertical scale offset.
7:0	RW	0x00	region3_xscl_offset Esmart_region3 horizontal scale offset.

ESMART0_KEY_CTRL

Rockchip Confidencial

Address: Operational Base(0x00001800) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

ESMART0_BG_EN

Address: Operational Base(0x00001800) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart Background Red color.
19:10	RW	0x000	esmart_g_value Esmart Background Green color.
9:0	RW	0x000	esmart_b_value Esmart Background Blue color.

3.5.3.8 ESMART1

ESMART1_CTRL0

Address: Operational Base(0x00001A00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:14	RO	0x00000	reserved
13:12	RW	0x0	esmart_scl_num 2'b00: Scale engine0 2'b01: Scale engine1 2'b10: Scale engine2 2'b11: Scale engine3
11:10	RO	0x0	reserved
9	RW	0x0	esmart_endian_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte0,byte1,byte2,byte3}
8	RW	0x0	esmart_mid_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte3,byte1,byte2,byte0}
7:6	RO	0x0	reserved
5	RW	0x0	esmart_8bpp_alpha_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

ESMART1_CTRL1

Address: Operational Base(0x00001A00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold.If esmart empty lb number>=esmart_dma_rreq_thold,dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x3	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x3	esmart_yrgb_gather_num The gather number of YRGB.
19:16	RO	0x0	reserved
15:12	RW	0xb	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:8	RO	0x0	reserved
7:4	RW	0xa	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x1	esmart_cbcr_gather_en To enable CBCR gather transfer.
2	RW	0x1	esmart_yrgb_gather_en To enable YRGB gather transfer.
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

ESMART1_AXI_CTRL

Address: Operational Base(0x00001A00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num esmart outstanding number.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

ESMART1_REGION0_MST_CTL

Address: Operational Base(0x00001A00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region0_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region0_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region0_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

ESMART1_REGION0_MST_YRGB

Address: Operational Base(0x00001A00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

ESMART1_REGION0_MST_CBCR

Address: Operational Base(0x00001A00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address.

ESMART1_REGION0_VIR

Address: Operational Base(0x00001A00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of mst0 uv virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of mst0 yrgb virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

Rockchip Confidencial

ESMART1_REGION0_ACT_INFO

Address: Operational Base(0x00001A00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_act_heigth Win_act_height=(win0_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_height=(win0_vertical size-1)

ESMART1_REGION0_DSP_INFO

Address: Operational Base(0x00001A00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width=(horizontal size-1)

ESMART1_REGION0_DSP_OFFSET

Address: Operational Base(0x00001A00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

ESMART1_REGION0_SCL_CTRL

Address: Operational Base(0x00001A00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region0_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART1_REGION0_SCL_FACTOR_YRGB

Address: Operational Base(0x00001A00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART1_REGION0_SCL_OFFSET

Rockchip Confidencial

Address: Operational Base(0x00001A00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yscl_offset Esmart_region0 vertical scale offset.
7:0	RW	0x00	region0_xscl_offset Esmart_region0 horizontal scale offset.

ESMART1_REGION1_MST_CTL

Address: Operational Base(0x00001A00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region1_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region1_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region1_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

ESMART1_REGION1_MST_YRGB

Address: Operational Base(0x00001A00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region1 YRGB frame buffer memory start address.

ESMART1_REGION1_MST_CBCR

Address: Operational Base(0x00001A00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region1 CBCR frame buffer memory start address.

ESMART1_REGION1_VIR

Address: Operational Base(0x00001A00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of mst1 uv virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of mst1 yrgb virtual width. ARGB888: win1_vir_width RGB888: (win1_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win1_vir_width/2) YUV: ceil(win1_vir_width/4) YUV tile: ceil(win1_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win1_vir_width/4)

ESMART1_REGION1_ACT_INFO

Address: Operational Base(0x00001A00) + offset (0x0050)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth Win_act_height=(win1_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_act_width Win_act_height=(win1_vertical size-1)

ESMART1_REGION1_DSP_INFO

Address: Operational Base(0x00001A00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width Dsp_width=(horizontal size-1)

ESMART1_REGION1_DSP_OFFSET

Address: Operational Base(0x00001A00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

ESMART1_REGION1_SCL_CTRL

Address: Operational Base(0x00001A00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region1_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART1_REGION1_SCL_FACTOR_YRGB

Address: Operational Base(0x00001A00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12

ESMART1_REGION1_SCL_OFFSET

Address: Operational Base(0x00001A00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yscl_offset Esmart_region1 vertical scale offset.
7:0	RW	0x00	region1_xscl_offset Esmart_region1 horizontal scale offset.

ESMART1_REGION2_MST_CTL

Rockchip Confidencial

Address: Operational Base(0x00001A00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region2_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region2_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region2_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

ESMART1_REGION2_MST_YRGB

Address: Operational Base(0x00001A00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region2 YRGB frame buffer memory start address.

ESMART1_REGION2_MST_CBCR

Address: Operational Base(0x00001A00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region2 CBCR frame buffer memory start address.

ESMART1_REGION2_VIR

Address: Operational Base(0x00001A00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of mst2 uv virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of mst2 yrgb virtual width. ARGB888: win2_vir_width RGB888: (win2_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win2_vir_width/2) YUV: ceil(win2_vir_width/4) YUV tile: ceil(win2_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win2_vir_width/4)

ESMART1_REGION2_ACT_INFO

Address: Operational Base(0x00001A00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth Win_act_height=(win2_vertical size-1)
15:13	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region2_act_width Win_act_height=(win2_vertical size-1)

ESMART1_REGION2_DSP_INFO

Address: Operational Base(0x00001A00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width Dsp_width=(horizontal size-1)

ESMART1_REGION2_DSP_OFFSET

Address: Operational Base(0x00001A00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

ESMART1_REGION2_SCL_CTRL

Address: Operational Base(0x00001A00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region2_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART1_REGION2_SCL_FACTOR_YRGB

Address: Operational Base(0x00001A00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN2_ACT_INFO[15:0])/(LCDC_WIN2_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN2_ACT_INFO[15:0])/(LCDC_WIN2_DSP_INFO[15:0]))*2^12

ESMART1_REGION2_SCL_OFFSET

Address: Operational Base(0x00001A00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yscl_offset Esmart_region vertical scale offset.
7:0	RW	0x00	region2_xscl_offset Esmart_region2 horizontal scale offset.

ESMART1_REGION3_MST_CTL

Address: Operational Base(0x00001A00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
23:22	RW	0x0	region3_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region3_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region3_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

ESMART1_REGION3_MST_YRGB

Address: Operational Base(0x00001A00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region3 YRGB frame buffer memory start address.

ESMART1_REGION3_MST_CBCR

Address: Operational Base(0x00001A00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region3 CBCR frame buffer memory start address.

ESMART1_REGION3_VIR

Address: Operational Base(0x00001A00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of mst3 uv virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of mst3 yrgb virtual width. ARGB888: win3_vir_width RGB888: (win3_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win3_vir_width/2) YUV: ceil(win3_vir_width/4) YUV tile: ceil(win3_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win3_vir_width/4)

ESMART1_REGION3_ACT_INFO

Address: Operational Base(0x00001A00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth Win_act_height=(win3_vertical size-1)
15:13	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region3_act_width Win_act_height=(win3_vertical size-1)

ESMART1_REGION3_DSP_INFO

Address: Operational Base(0x00001A00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width Dsp_width=(horizontal size-1)

ESMART1_REGION3_DSP_OFFSET

Address: Operational Base(0x00001A00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

ESMART1_REGION3_SCL_CTRL

Address: Operational Base(0x00001A00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region3_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART1_REGION3_SCL_FACTOR_YRGB

Address: Operational Base(0x00001A00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^12

ESMART1_REGION3_SCL_OFFSET

Address: Operational Base(0x00001A00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yscl_offset Esmart_region3 vertical scale offset.
7:0	RW	0x00	region3_xscl_offset Esmart_region3 horizontal scale offset.

ESMART1_KEY_CTRL

Address: Operational Base(0x00001A00) + offset (0x00D0)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

ESMART1_BG_EN

Address: Operational Base(0x00001A00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart Background Red color.
19:10	RW	0x000	esmart_g_value Esmart Background Green color.
9:0	RW	0x000	esmart_b_value Esmart Background Blue color.

3.5.3.9 ESMART2

ESMART2_CTRL0

Address: Operational Base(0x00001C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:14	RO	0x00000	reserved
13:12	RW	0x0	esmart_scl_num 2'b00: Scale engine0 2'b01: Scale engine1 2'b10: Scale engine2 2'b11: Scale engine3
11:10	RO	0x0	reserved
9	RW	0x0	esmart_endian_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte0,byte1,byte2,byte3}
8	RW	0x0	esmart_mid_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte3,byte1,byte2,byte0}
7:6	RO	0x0	reserved
5	RW	0x0	esmart_8bpp_alpha_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

ESMART2_CTRL1

Address: Operational Base(0x00001C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold.If esmart empty lb number>=esmart_dma_rreq_thold,dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x3	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x3	esmart_yrgb_gather_num The gather number of YRGB.
19:16	RO	0x0	reserved
15:12	RW	0xb	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:8	RO	0x0	reserved
7:4	RW	0xa	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x1	esmart_cbcr_gather_en To enable CBCR gather transfer.
2	RW	0x1	esmart_yrgb_gather_en To enable YRGB gather transfer.
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

ESMART2_AXI_CTRL

Address: Operational Base(0x00001C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num esmart outstanding number.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

ESMART2_REGION0_MST_CTL

Address: Operational Base(0x00001C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region0_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region0_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region0_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

ESMART2_REGION0_MST_YRGB

Address: Operational Base(0x00001C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

ESMART2_REGION0_MST_CBCR

Address: Operational Base(0x00001C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address.

ESMART2_REGION0_VIR

Address: Operational Base(0x00001C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of mst0 uv virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of mst0 yrgb virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

Rockchip Confidencial

ESMART2_REGION0_ACT_INFO

Address: Operational Base(0x00001C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_act_heigth Win_act_height=(win0_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_height=(win0_vertical size-1)

ESMART2_REGION0_DSP_INFO

Address: Operational Base(0x00001C00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width=(horizontal size-1)

ESMART2_REGION0_DSP_OFFSET

Address: Operational Base(0x00001C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

ESMART2_REGION0_SCL_CTRL

Address: Operational Base(0x00001C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region0_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART2_REGION0_SCL_FACTOR_YRGB

Address: Operational Base(0x00001C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART2_REGION0_SCL_OFFSET

Rockchip Confidencial

Address: Operational Base(0x00001C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yscl_offset Esmart_region0 vertical scale offset.
7:0	RW	0x00	region0_xscl_offset Esmart_region0 horizontal scale offset.

ESMART2_REGION1_MST_CTL

Address: Operational Base(0x00001C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region1_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region1_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region1_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

ESMART2_REGION1_MST_YRGB

Address: Operational Base(0x00001C00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region1 YRGB frame buffer memory start address.

ESMART2_REGION1_MST_CBCR

Address: Operational Base(0x00001C00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region1 CBCR frame buffer memory start address.

ESMART2_REGION1_VIR

Address: Operational Base(0x00001C00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of mst1 uv virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of mst1 yrgb virtual width. ARGB888: win1_vir_width RGB888: (win1_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win1_vir_width/2) YUV: ceil(win1_vir_width/4) YUV tile: ceil(win1_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win1_vir_width/4)

ESMART2_REGION1_ACT_INFO

Address: Operational Base(0x00001C00) + offset (0x0050)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth Win_act_height=(win1_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_act_width Win_act_height=(win1_vertical size-1)

ESMART2_REGION1_DSP_INFO

Address: Operational Base(0x00001C00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width Dsp_width=(horizontal size-1)

ESMART2_REGION1_DSP_OFFSET

Address: Operational Base(0x00001C00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

ESMART2_REGION1_SCL_CTRL

Address: Operational Base(0x00001C00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region1_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART2_REGION1_SCL_FACTOR_YRGB

Address: Operational Base(0x00001C00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12

ESMART2_REGION1_SCL_OFFSET

Address: Operational Base(0x00001C00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yscl_offset Esmart_region1 vertical scale offset.
7:0	RW	0x00	region1_xscl_offset Esmart_region1 horizontal scale offset.

ESMART2_REGION2_MST_CTL

Rockchip Confidencial

Address: Operational Base(0x00001C00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region2_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region2_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region2_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

ESMART2_REGION2_MST_YRGB

Address: Operational Base(0x00001C00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region2 YRGB frame buffer memory start address.

ESMART2_REGION2_MST_CBCR

Address: Operational Base(0x00001C00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region2 CBCR frame buffer memory start address.

ESMART2_REGION2_VIR

Address: Operational Base(0x00001C00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of mst2 uv virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of mst2 yrgb virtual width. ARGB888: win2_vir_width RGB888: (win2_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win2_vir_width/2) YUV: ceil(win2_vir_width/4) YUV tile: ceil(win2_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win2_vir_width/4)

ESMART2_REGION2_ACT_INFO

Address: Operational Base(0x00001C00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth Win_act_height=(win2_vertical size-1)
15:13	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region2_act_width Win_act_height=(win2_vertical size-1)

ESMART2_REGION2_DSP_INFO

Address: Operational Base(0x00001C00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width Dsp_width=(horizontal size-1)

ESMART2_REGION2_DSP_OFFSET

Address: Operational Base(0x00001C00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

ESMART2_REGION2_SCL_CTRL

Address: Operational Base(0x00001C00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region2_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART2_REGION2_SCL_FACTOR_YRGB

Address: Operational Base(0x00001C00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN2_ACT_INFO[15:0])/(LCDC_WIN2_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN2_ACT_INFO[15:0])/(LCDC_WIN2_DSP_INFO[15:0]))*2^12

ESMART2_REGION2_SCL_OFFSET

Address: Operational Base(0x00001C00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yscl_offset Esmart_region2 vertical scale offset.
7:0	RW	0x00	region2_xscl_offset Esmart_region2 horizontal scale offset.

ESMART2_REGION3_MST_CTL

Address: Operational Base(0x00001C00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
23:22	RW	0x0	region3_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region3_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region3_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

ESMART2_REGION3_MST_YRGB

Address: Operational Base(0x00001C00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region3 YRGB frame buffer memory start address.

ESMART2_REGION3_MST_CBCR

Address: Operational Base(0x00001C00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region3 CBCR frame buffer memory start address.

ESMART2_REGION3_VIR

Address: Operational Base(0x00001C00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of mst3 uv virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of mst3 yrgb virtual width. ARGB888: win3_vir_width RGB888: (win3_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win3_vir_width/2) YUV: ceil(win3_vir_width/4) YUV tile: ceil(win3_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win3_vir_width/4)

ESMART2_REGION3_ACT_INFO

Address: Operational Base(0x00001C00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth Win_act_height=(win3_vertical size-1)
15:13	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region3_act_width Win_act_height=(win3_vertical size-1)

ESMART2_REGION3_DSP_INFO

Address: Operational Base(0x00001C00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width Dsp_width=(horizontal size-1)

ESMART2_REGION3_DSP_OFFSET

Address: Operational Base(0x00001C00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

ESMART2_REGION3_SCL_CTRL

Address: Operational Base(0x00001C00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region3_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART2_REGION3_SCL_FACTOR_YRGB

Address: Operational Base(0x00001C00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^12

ESMART2_REGION3_SCL_OFFSET

Address: Operational Base(0x00001C00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yscl_offset Esmart_region3 vertical scale offset.
7:0	RW	0x00	region3_xscl_offset Esmart_region3 horizontal scale offset.

ESMART2_KEY_CTRL

Address: Operational Base(0x00001C00) + offset (0x00D0)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

ESMART2_BG_EN

Address: Operational Base(0x00001C00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart Background Red color.
19:10	RW	0x000	esmart_g_value Esmart Background Green color.
9:0	RW	0x000	esmart_b_value Esmart Background Blue color.

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ESMART3_CTRL0

Address: Operational Base(0x00001E00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:14	RO	0x00000	reserved
13:12	RW	0x0	esmart_scl_num 2'b00: Scale engine0 2'b01: Scale engine1 2'b10: Scale engine2 2'b11: Scale engine3
11:10	RO	0x0	reserved
9	RW	0x0	esmart_endian_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte0,byte1,byte2,byte3}
8	RW	0x0	esmart_mid_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte3,byte1,byte2,byte0}
7:6	RO	0x0	reserved
5	RW	0x0	esmart_8bpp_alpha_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

ESMART3_CTRL1

Address: Operational Base(0x00001E00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold.If esmart empty lb number>=esmart_dma_rreq_thold,dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x3	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x3	esmart_yrgb_gather_num The gather number of YRGB.
19:16	RO	0x0	reserved
15:12	RW	0xb	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:8	RO	0x0	reserved
7:4	RW	0xa	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x1	esmart_cbcr_gather_en To enable CBCR gather transfer.
2	RW	0x1	esmart_yrgb_gather_en To enable YRGB gather transfer.
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

ESMART3_AXI_CTRL

Address: Operational Base(0x00001E00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num esmart outstanding number.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

ESMART3_REGION0_MST_CTL

Address: Operational Base(0x00001E00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region0_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region0_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region0_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

ESMART3_REGION0_MST_YRGB

Address: Operational Base(0x00001E00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

ESMART3_REGION0_MST_CBCR

Address: Operational Base(0x00001E00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address.

ESMART3_REGION0_VIR

Address: Operational Base(0x00001E00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of mst0 uv virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of mst0 yrgb virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

Rockchip Confidencial

ESMART3_REGION0_ACT_INFO

Address: Operational Base(0x00001E00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_act_heigth Win_act_height=(win0_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_height=(win0_vertical size-1)

ESMART3_REGION0_DSP_INFO

Address: Operational Base(0x00001E00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width=(horizontal size-1)

ESMART3_REGION0_DSP_OFFSET

Address: Operational Base(0x00001E00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

ESMART3_REGION0_SCL_CTRL

Address: Operational Base(0x00001E00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region0_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART3_REGION0_SCL_FACTOR_YRGB

Address: Operational Base(0x00001E00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART3_REGION0_SCL_OFFSET

Rockchip Confidencial

Address: Operational Base(0x00001E00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yscl_offset Esmart_region0 vertical scale offset.
7:0	RW	0x00	region0_xscl_offset Esmart_region0 horizontal scale offset.

ESMART3_REGION1_MST_CTL

Address: Operational Base(0x00001E00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region1_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region1_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region1_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

ESMART3_REGION1_MST_YRGB

Address: Operational Base(0x00001E00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region1 YRGB frame buffer memory start address.

ESMART3_REGION1_MST_CBCR

Address: Operational Base(0x00001E00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region1 CBCR frame buffer memory start address.

ESMART3_REGION1_VIR

Address: Operational Base(0x00001E00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of mst1 uv virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of mst1 yrgb virtual width. ARGB888: win1_vir_width RGB888: (win1_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win1_vir_width/2) YUV: ceil(win1_vir_width/4) YUV tile: ceil(win1_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win1_vir_width/4)

ESMART3_REGION1_ACT_INFO

Address: Operational Base(0x00001E00) + offset (0x0050)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth Win_act_height=(win1_vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_act_width Win_act_height=(win1_vertical size-1)

ESMART3_REGION1_DSP_INFO

Address: Operational Base(0x00001E00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width Dsp_width=(horizontal size-1)

ESMART3_REGION1_DSP_OFFSET

Address: Operational Base(0x00001E00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

ESMART3_REGION1_SCL_CTRL

Address: Operational Base(0x00001E00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region1_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART3_REGION1_SCL_FACTOR_YRGB

Address: Operational Base(0x00001E00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN1_ACT_INFO[15:0])/(LCDC_WIN1_DSP_INFO[15:0]))*2^12

ESMART3_REGION1_SCL_OFFSET

Address: Operational Base(0x00001E00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yscl_offset Esmart_region1 vertical scale offset.
7:0	RW	0x00	region1_xscl_offset Esmart_region1 horizontal scale offset.

ESMART3_REGION2_MST_CTL

Rockchip Confidencial

Address: Operational Base(0x00001E00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region2_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region2_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region2_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

ESMART3_REGION2_MST_YRGB

Address: Operational Base(0x00001E00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region2 YRGB frame buffer memory start address.

ESMART3_REGION2_MST_CBCR

Address: Operational Base(0x00001E00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region2 CBCR frame buffer memory start address.

ESMART3_REGION2_VIR

Address: Operational Base(0x00001E00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of mst2 uv virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of mst2 yrgb virtual width. ARGB888: win2_vir_width RGB888: (win2_vir_width*3/4)+(win0_vir_width%3) RGB565: ceil(win2_vir_width/2) YUV: ceil(win2_vir_width/4) YUV tile: ceil(win2_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win2_vir_width/4)

ESMART3_REGION2_ACT_INFO

Address: Operational Base(0x00001E00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth Win_act_height=(win2_vertical size-1)
15:13	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region2_act_width Win_act_height=(win2_vertical size-1)

ESMART3_REGION2_DSP_INFO

Address: Operational Base(0x00001E00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width Dsp_width=(horizontal size-1)

ESMART3_REGION2_DSP_OFFSET

Address: Operational Base(0x00001E00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

ESMART3_REGION2_SCL_CTRL

Address: Operational Base(0x00001E00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region2_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART3_REGION2_SCL_FACTOR_YRGB

Address: Operational Base(0x00001E00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0])/(LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN2_ACT_INFO[15:0])/(LCDC_WIN2_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN2_ACT_INFO[15:0])/(LCDC_WIN2_DSP_INFO[15:0]))*2^12

ESMART3_REGION2_SCL_OFFSET

Address: Operational Base(0x00001E00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yscl_offset Esmart_region2 vertical scale offset.
7:0	RW	0x00	region2_xscl_offset Esmart_region2 horizontal scale offset.

ESMART3_REGION3_MST_CTL

Address: Operational Base(0x00001E00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
23:22	RW	0x0	region3_xpre_scl_mode 2'b00: Xgt2 or xavg2 2'b01: Xgt4 or xavg4 Others: Reserved
21	RW	0x0	region3_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region3_xavg_en 1'b0: Disable 1'b1: Enable
19:18	RO	0x0	reserved
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>4,esmart_cbcr_4gt must be enable.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc,bilinear is enable and cbcr_act_height/cbcr_dsp_height>2,esmart_cbcr_2gt must be enable.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>4,esmart_yrgb_4gt must be enable.
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc,bilinear is enable and yrgb_act_height/yrgb_dsp_height>2,esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Others: Reserved
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

ESMART3_REGION3_MST_YRGB

Address: Operational Base(0x00001E00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region3 YRGB frame buffer memory start address.

ESMART3_REGION3_MST_CBCR

Address: Operational Base(0x00001E00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region3 CBCR frame buffer memory start address.

ESMART3_REGION3_VIR

Address: Operational Base(0x00001E00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of mst3 uv virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of mst3 yrgb virtual width. ARGB888: win3_vir_width RGB888: (win3_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win3_vir_width/2) YUV: ceil(win3_vir_width/4) YUV tile: ceil(win3_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win3_vir_width/4)

ESMART3_REGION3_ACT_INFO

Address: Operational Base(0x00001E00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth Win_act_height=(win3_vertical size-1)
15:13	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region3_act_width Win_act_height=(win3_vertical size-1)

ESMART3_REGION3_DSP_INFO

Address: Operational Base(0x00001E00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height Dsp_height=(vertical size-1)
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width Dsp_width=(horizontal size-1)

ESMART3_REGION3_DSP_OFFSET

Address: Operational Base(0x00001E00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

ESMART3_REGION3_SCL_CTRL

Address: Operational Base(0x00001E00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region3_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not ysu_scale When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not ysd_scale
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Others: Not xsu_scale When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Others: Not xsd_scale
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART3_REGION3_SCL_FACTOR_YRGB

Address: Operational Base(0x00001E00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_xsu: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN3_ACT_INFO[15:0])/(LCDC_WIN3_DSP_INFO[15:0]))*2^12

ESMART3_REGION3_SCL_OFFSET

Address: Operational Base(0x00001E00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yscl_offset Esmart_region3 vertical scale offset.
7:0	RW	0x00	region3_xscl_offset Esmart_region3 horizontal scale offset.

ESMART3_KEY_CTRL

Address: Operational Base(0x00001E00) + offset (0x00D0)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

ESMART3_BG_EN

Address: Operational Base(0x00001E00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart Background Red color.
19:10	RW	0x000	esmart_g_value Esmart Background Green color.
9:0	RW	0x000	esmart_b_value Esmart Background Blue color.

3.5.3.11 MMU

VOP3_MMU_DTE_ADDR

Address: Operational Base(0x00007E00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dte_addr Current page table address.

VOP3_MMU_STATUS

Address: Operational Base(0x00007E00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	page_fault_bus_id Index of master responsible for last page fault.
5	RW	0x0	page_fault_is_write The direction of access for last page fault. 1'b0: Read 1'b1: Write
4	RW	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RW	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	page_fault_active MMU page fault mode currently enabled. The mode is enabled by command.

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Bit	Attr	Reset Value	Description
0	RW	0x0	paging_en Paging is enabled. 1'b0: Disable 1'b1: Enable

VOP3_MMU_COMMAND

Address: Operational Base(0x00007E00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd This can be: 3'd0: MMU_ENABLE_PAGING 3'd1: MMU_DISABLE_PAGING 3'd2: MMU_ENABLE_STALL 3'd3: MMU_DISABLE_STALL 3'd4: MMU_ZAP_CACHE 3'd5: MMU_PAGE_FAULT_DONE 3'd6: MMU_FORCE_RESET Others: reserved

VOP3_MMU_PAGE_FAULT_ADDR

Address: Operational Base(0x00007E00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

VOP3_MMU_ZAP_ONE_LINE

Address: Operational Base(0x00007E00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

VOP3_MMU_INT_RAWSTAT

Address: Operational Base(0x00007E00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rawst_bus_error Raw interrupt status of read bus error.
0	RW	0x0	rawst_page_fault Raw interrupt status of page fault.

VOP3_MMU_INT_CLEAR

Address: Operational Base(0x00007E00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	clr_bus_error Clear interrupt of bus error.
0	RW	0x0	clr_page_fault Clear interrupt of page fault.

VOP3_MMU_INT_MASK

Address: Operational Base(0x00007E00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	mask_bus_error Mask interrupt of bus error.
0	RW	0x0	mask_page_fault Mask interrupt of page fault.

VOP3_MMU_INT_STATUS

Address: Operational Base(0x00007E00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	st_bus_error Interrupt status of bus error.
0	RW	0x0	st_page_fault Interrupt status of page fault.

VOP3_MMU_AUTO_GATING

Address: Operational Base(0x00007E00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mmu_cfg_mode 1'b0: Regdone when frame start 1'b1: Regdone immediately
0	RW	0x0	mmu_auto_gating When it is 1'b1,the mmu will auto gating itself.

3.6 Interface Description

Table 3-28 LCDC interface description

Module Pin	Direction	Pad Name	IOMUX Setting
LCDC Interface			
LCDC_DCLK	O	VO_LCDC_CLK/RGMII_CLK_M0/CAM_CLK1_OUT_M1/PDM_CLK0_M1/GPIO4_B7_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[15:12]= 4'h1
LCDC_HSYNC	O	VO_LCDC_HSYNC/I2S1_SDO1_M0/UART9_CTSN_M0/SPI2_CSN1_M0/I2C1_SCL_M1/UART3_TX_M0/GPIO4_B4_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[3:0]= 4'h1
LCDC_VSYNC	O	VO_LCDC_VSYNC/I2S1_SDO2_M0/UART9_RTSN_M0/SPI2_CSN0_M0/I2C1_SDA_M1/UART3_RX_M0/GPIO4_B5_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[7:4]= 4'h1
LCDC_DEN	O	VO_LCDC_DEN/I2S1_SDO3_M0/UART3_CTSN_M0/SPI2_CLK_M0/GPIO4_B6_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[11:8]= 4'h1
LCDC_D23	O	VO_LCDC_D23/RGMII_TXD1_M0/UART6_RTSN_M1/SPI1_MISO_M0/GPIO4_A3_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[15:12]= 4'h1
LCDC_D22	O	VO_LCDC_D22/RGMII_TXD0_M0/UART6_CTSN_M1/SPI1_MOSI_M0/GPIO4_A2_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[11:8]= 4'h1
LCDC_D21	O	VO_LCDC_D21/RGMII_RXCLK_M0/I2S2_LRCK_M1/PWM12_M0/GPIO4_A1_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[7:4]= 4'h1
LCDC_D20	O	VO_LCDC_D20/RGMII_RXD3_M0/UART8_RTSN_M1/SPI1_CSN1_M0/GPIO4_A0_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[3:0]= 4'h1
LCDC_D19	O	VO_LCDC_D19/RGMII_RXD2_M0/UART8_CTSN_M1/SPI1_CSN0_M0/GPIO3_D7_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[15:12] = 4'h1
LCDC_D18	O	VO_LCDC_D18/RGMII_MDIO_M0/UART9_RX_M0/GPIO4_B3_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_L[15:12]= 4'h1
LCDC_D17	O	VO_LCDC_D17/ETH_CLK_25M_OUT_M0/CAM_CLK0_OUT_M1/I2S2_SCLK_M1/PDM_CLK1_M1/GPIO4_B1_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_L[7:4]= 4'h1
LCDC_D16	O	VO_LCDC_D16/RGMII_RXER_M0/UART1_CTSN_M1/PDM_SDI1_M1/UART6_RX_M1/GPIO4_B0_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_L[3:0]= 4'h1
LCDC_D15	O	VO_LCDC_D15/RGMII_TXCLK_M0/I2S2_MCLK_M1/SPI1_CLK_M0/GPIO3_D6_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[11:8]= 4'h1

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Module Pin	Direction	Pad Name	IOMUX Setting
LCDC_D14	O	VO_LCDC_D14/RGMII_TXD3_M0/UART8_RX_M1/I2S2_SDO_M1/GPIO3_D5_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[7:4]= 4'h1
LCDC_D13	O	VO_LCDC_D13/RGMII_TXD2_M0/UART8_TX_M1/I2S2_SDI_M1/GPIO3_D4_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[3:0]= 4'h1
LCDC_D12	O	VO_LCDC_D12/I2S1_SDI3_M0/UART7_RTSN_M0/SPI2_MOSI_M0/I2C2_SDA_M1/GPIO3_D3_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[15:12]= 4'h1
LCDC_D11	O	VO_LCDC_D11/I2S1_SDI2_M0/UART7_CTSN_M0/SPI2_MISO_M0/I2C2_SCL_M1/GPIO3_D2_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[11:8]= 4'h1
LCDC_D10	O	VO_LCDC_D10/I2S1_SDI1_M0/UART4_RX_M0/UART3_RTSN_M0/GPIO3_D1_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[7:4]= 4'h1
LCDC_D9	O	VO_LCDC_D9/RGMII_RXDV_M0/UART1_RTSN_M1/PDM_SDI0_M1/UART6_TX_M1/GPIO4_A7_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H[15:12]= 4'h1
LCDC_D8	O	VO_LCDC_D8/RGMII_RXD1_M0/UART1_RX_M1/PDM_SDI3_M1/I2C3_SDA_M1/GPIO4_A6_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H[11:8]= 4'h1
LCDC_D7	O	VO_LCDC_D7/I2S1_SDI0_M0/UART4_TX_M0/GPIO3_D0_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[3:0]= 4'h1
LCDC_D6	O	VO_LCDC_D6/I2S1_SDO0_M0/UART7_RX_M0/GPIO3_C7_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H[15:12]= 4'h1
LCDC_D5	O	VO_LCDC_D5/I2S1_LRCK_M0/UART4_RTSN_M0/PWM15_M0/GPIO3_C6_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H[11:8]= 4'h1
LCDC_D4	O	VO_LCDC_D4/I2S1_SCLK_M0/UART4_CTSN_M0/PWM14_M0/GPIO3_C5_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H[7:4]= 4'h1
LCDC_D3	O	VO_LCDC_D3/I2S1_MCLK_M0/UART7_TX_M0/GPIO3_C4_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H[3:0]= 4'h1
LCDC_D2	O	VO_LCDC_D2/RGMII_MDC_M0/UART9_TX_M0/GPIO4_B2_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_L[11:8] = 4'h1
LCDC_D1	O	VO_LCDC_D1/RGMII_RXD0_M0/UART1_TX_M1/PDM_SDI2_M1/I2C3_SCL_M1/GPIO4_A5_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H[7:4] = 4'h1
LCDC_D0	O	VO_LCDC_D0/RGMII_TXEN_M0/PWM13_M0/GPIO4_A4_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H[3:0] = 4'h1

3.7 Application Notes

3.7.1 VOP Pixel Clock Configuration

- **dclk**: The clock source of the post-processing module and interface pixel clock, provided by the CRU module in the pd_VOP subsystem.
- **dclk_core**: The operating clock of the scanning timing of the post-processing module.

3.7.1.1 Dclk Frequency Requirements

Because it is necessary to provide clock sources for post-processing modules (dclk_core, dclk) and various output display interfaces (mipi_pixel_clock, lvds_pixel_clock, etc.), it is necessary to ensure that dclk is the highest frequency to meet various interface format rate conversion and frequency division requirements.

3.7.1.2 Interface BT656 dclk and dclk_core Clock Frequency Requirements

Only the BT656 interface needs to down-convert the dclk_core in use.

$$\text{dclk_core} = \text{dclk}/2$$

In order to achieve dclk_core frequency reduction, must be set DSP_CTRL[4] to 1.

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Chapter 4 Raster Graphic Acceleration (RGA2)

4.1 Overview

RGA2 is a separate 2D raster graphic accelerator, use to accelerate basic 2D graphics operations, including: image scaling, rotation, BitBLT, alpha blending.

4.1.1 Features

- **Data format**
  - Input data:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551
    - YUV420/YUV422/YVYU422/YUV422SP10bit/YUV420SP10bit
  - Output data:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551
    - YUV420/YUV422/YUV400/Y4/YVYU422/YVYU420
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average filter
  - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror operation
  - Mirroring and rotation co-operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT
  - A+B=B only BitBLT, A support rotate & scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - Comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- **OSD Automatic Inversion**
  - Supports OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
  - Support SRC0 and OSD overlay
- **Others**
  - Support square mosaic patterns to cover rectangular mosaic areas
  - Support MMU

4.1.2 The Constraints

- YUV420/422-8bit virtual stride need 8byte align, xoff/yoff need 2byte align
- YUV420/422-10bit virtual stride need 16byte align, not support xoff/yoff
- Vertical scale down or bypass && Horizontal bi-cubic scale up src0 width<=2048
- Vertical scale up && Horizontal bi-cubic scale up src0 width<=1928
- Vertical scale down or bypass Horizontal BI-linear scale up src0 width<=4096
- Vertical scale up && Horizontal BI-linear scale up src0 width<=3856

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4.2 Block Diagram

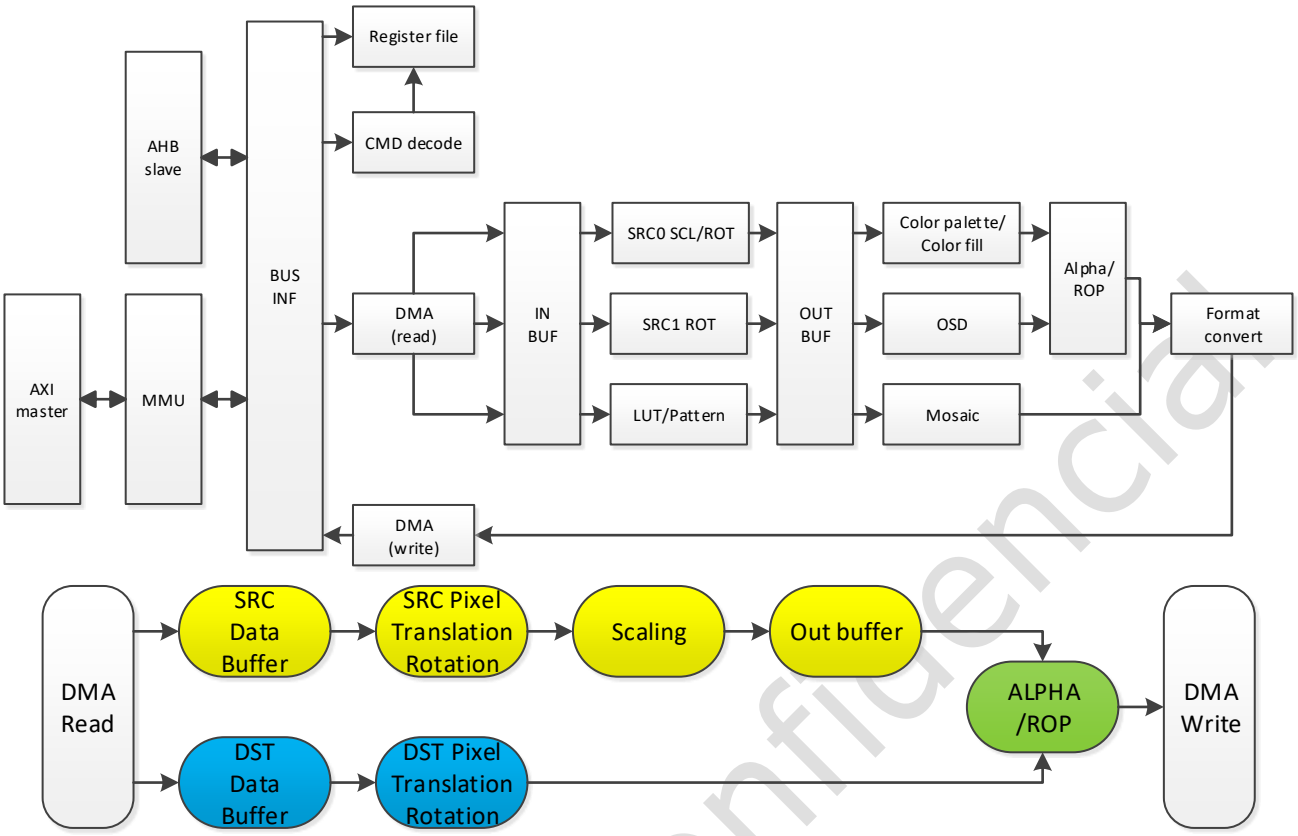

Fig. 4-1 RGA2 Block Diagram

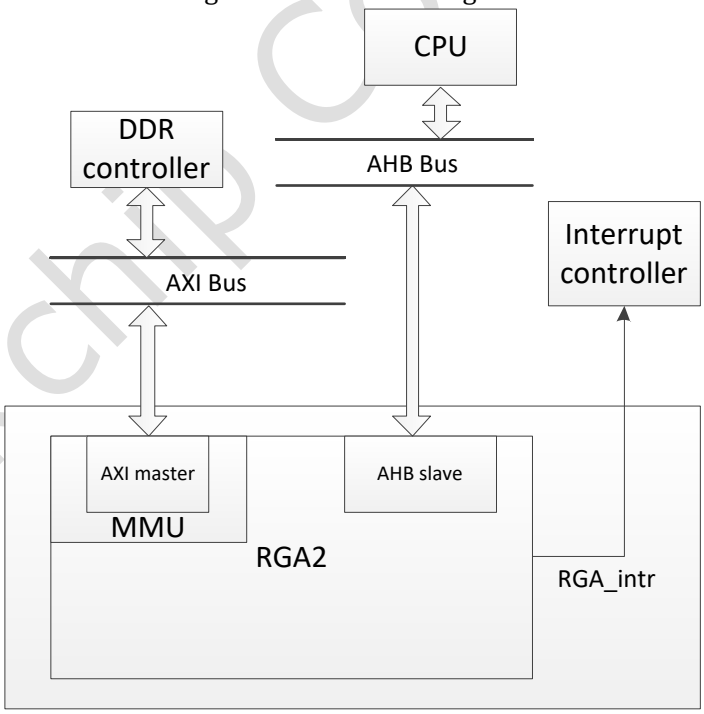

Fig. 4-2 RGA2 in SOC

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4.3 Function Description

4.3.1 Data Format

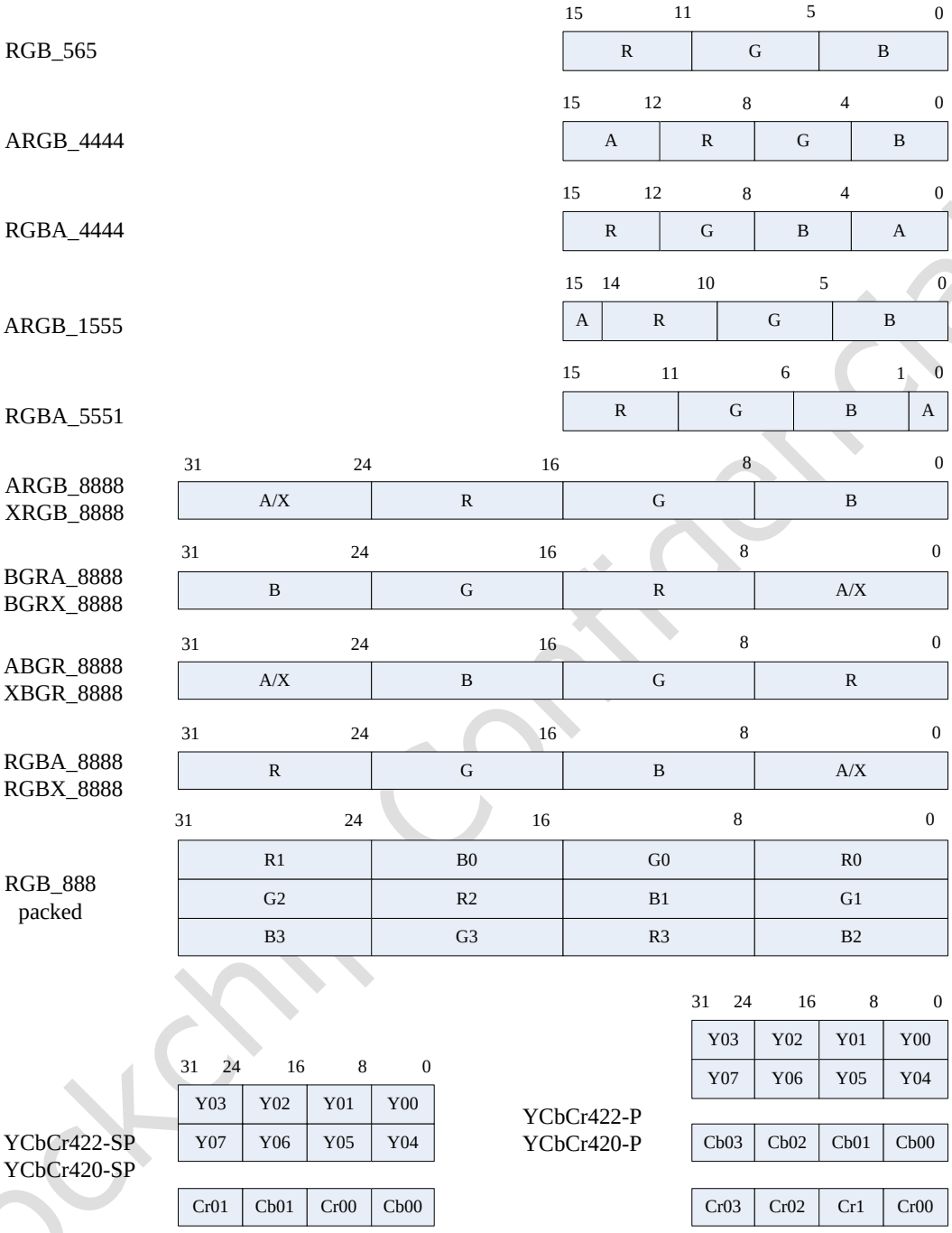

Fig. 4-3 RGA2 Input Data Format

All input data (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888/AUYV8888. The results are converted to the output data format (defined by DST_OUT_FMT).

4.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.

The down-dithering is done using Dither Allegro.

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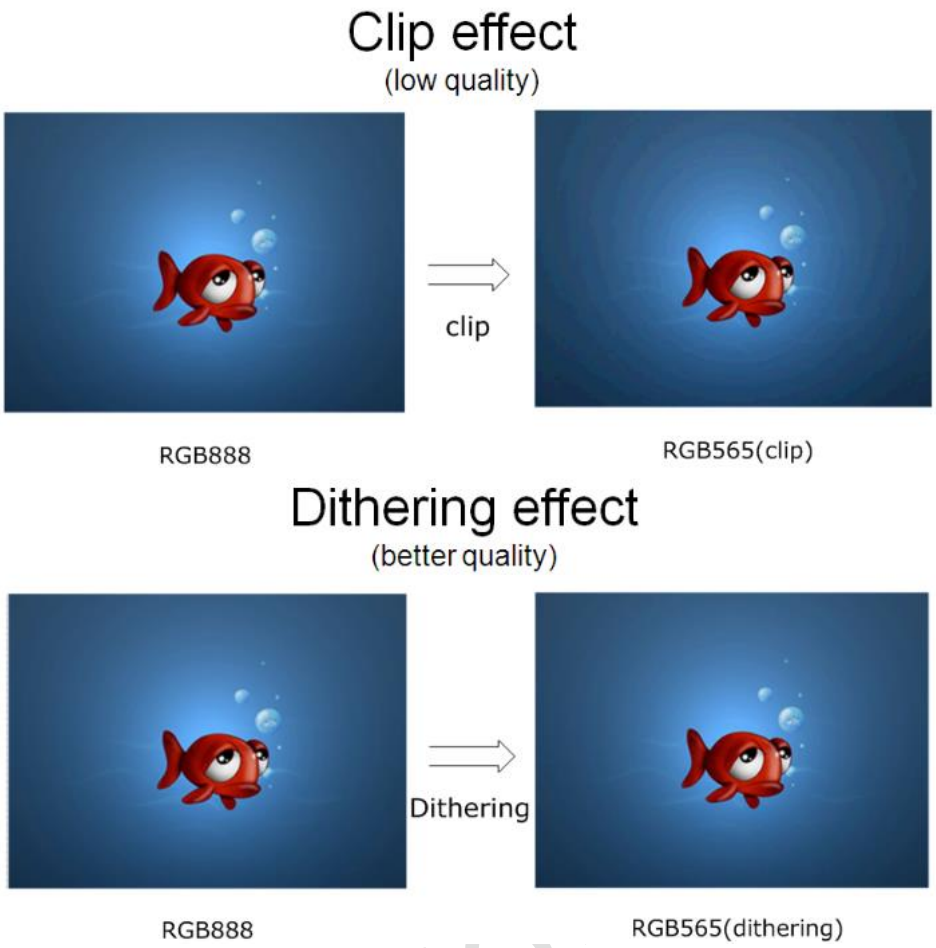
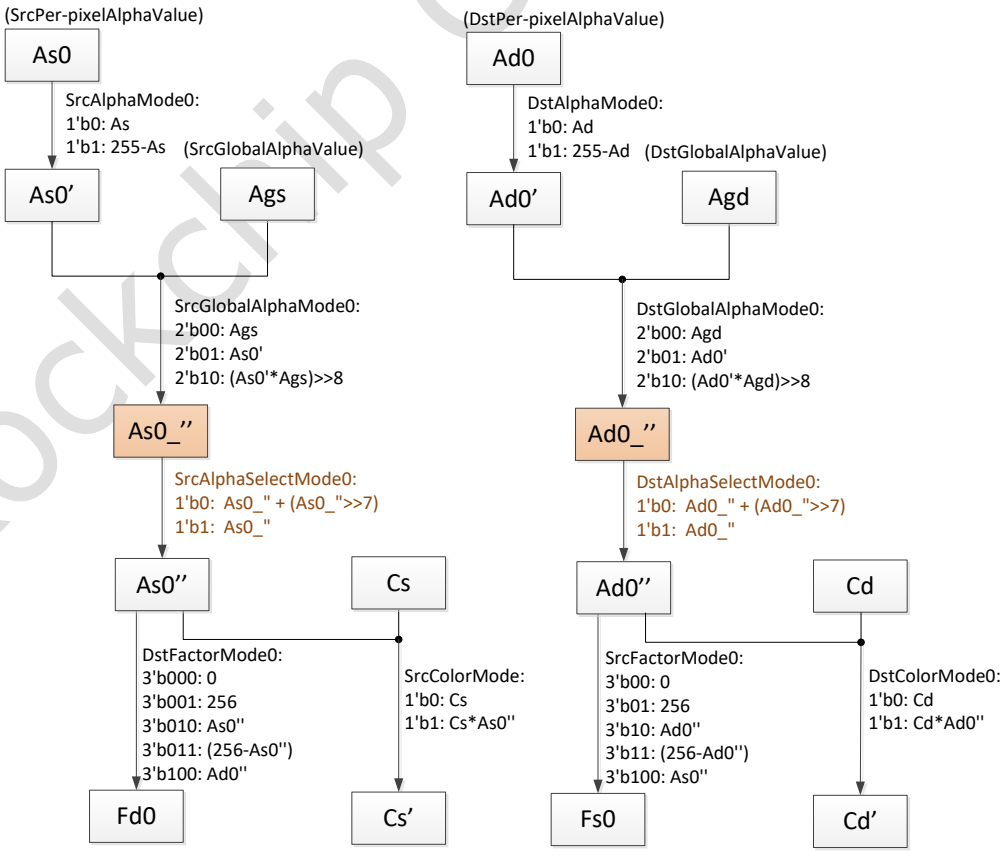


Fig. 4-4 RGA2 Dither effect

4.3.3 Alpha Mode



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')

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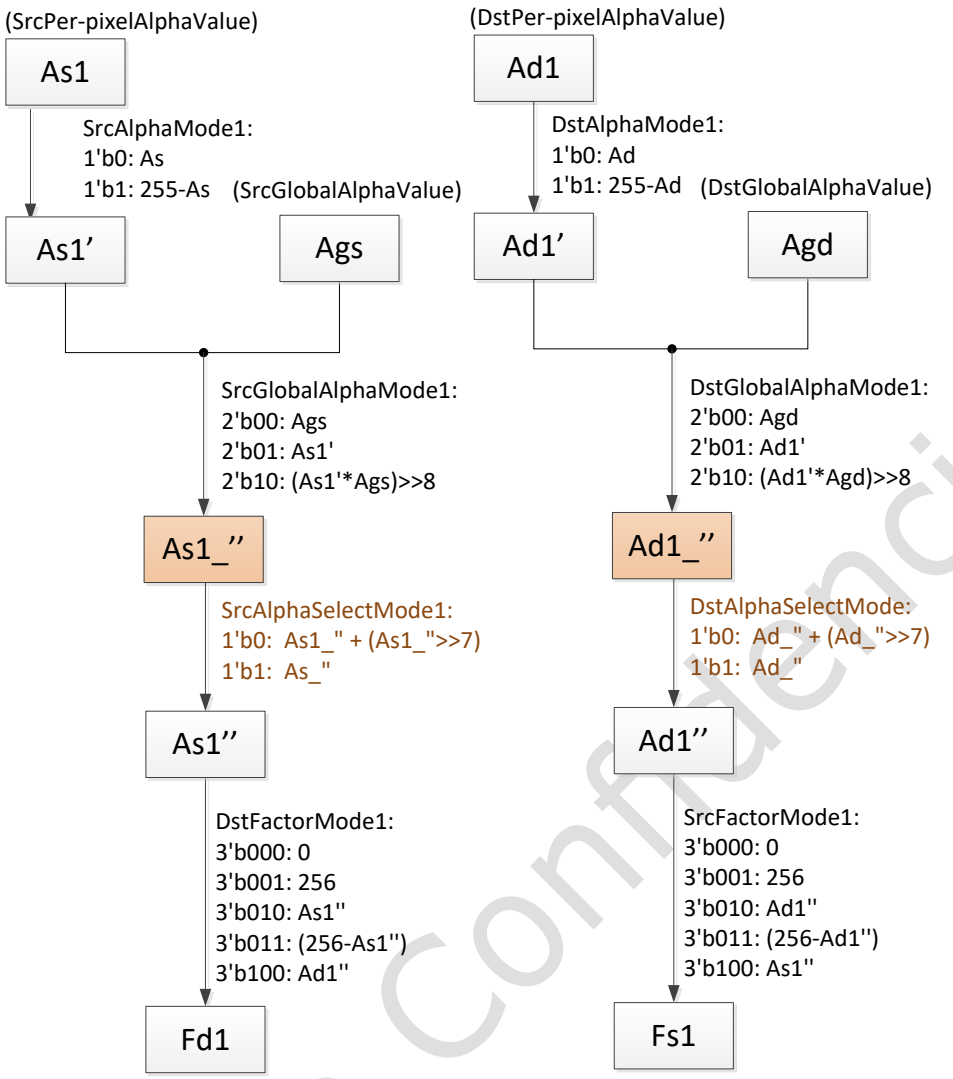

$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \quad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1' – dst alpha'')

Fig. 4-5 alpha mode configure description

4.3.4 Color Fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

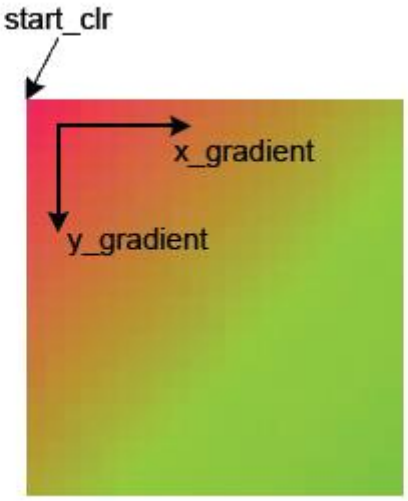

Fig. 4-6 RGA2 Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different coordinate.

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A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;
A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

4.3.5 Scaling

The scaling operation is the image reshaping processing of source image. Scaling is done base on ARGB8888 format.
There are three sampling modes: scale down (Average); scale up(Bi-cubic), scale up(Bi-linear).

4.3.6 OSD Automatic Inversion

Supports unidirectional (vertical or horizontal) OSD bars. Support OSD automatic color inversion and regional brightness statistics. The command of statistics and automatic color inversion can be operated at the same time or separately.
The width of each OSD block supports fixed mode and variable mode. The threshold for whether the OSD inverts color can be configured. The brightness statistics or the inverse color flags of OSD blocks can be read by AHB.This function can be used in dash cams, monitors, players, etc.

Fig. 4-7 RGA2 OSD Figure

4.3.7 Cover Mosaic

The Mosaic function realizes the coverage of the image area, which blurs the specific area.

Fig. 4-8 RGA2 Mosaic Figure

4.4 Register Description

4.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RGA2_SYS_CTRL	0x0000	W	0x00000044	RGA system control register
RGA2_CMD_CTRL	0x0004	W	0x00000000	RGA command control register

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Name	Offset	Size	Reset Value	Description
RGA2_CMD_BASE	0x0008	W	0x00000000	RGA command codes base address register
RGA2_STATUS1	0x000C	W	0x00000000	RGA status register
RGA2_INT	0x0010	W	0x00000000	RGA interrupt register
RGA2_MMU_CTRL0	0x0014	W	0x00000000	RGA MMU control 0 register
RGA2_STATUS2	0x001C	W	0x00000000	RGA status register
RGA2_WORK_CNT	0x0020	W	0x00000000	RGA work counter
RGA2_VERSION_INFO	0x0028	W	0x00000000	RTL version and FPGA version information
RGA2_READ_LINE_CNT_TH	0x0030	W	0x00001FFF	RGA read interrupt line count threshold.
RGA2_WRITE_LINE_CNT_TH	0x0034	W	0x00001FFF	RGA write interrupt line threshold start and step.
RGA2_INT_LINE_CNT	0x0038	W	0x00000000	Read and write line count for interrupt.
RGA2_DST_CSC_00	0x0060	W	0x000000BC	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_01	0x0064	W	0x00000274	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_02	0x0068	W	0x00000040	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF0	0x006C	W	0x00004200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_10	0x0070	W	0x00000798	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_11	0x0074	W	0x000006A4	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_12	0x0078	W	0x000001C0	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF1	0x007C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_20	0x0080	W	0x000001C0	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_21	0x0084	W	0x00000668	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_22	0x0088	W	0x000007D8	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF2	0x008C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_OSD_CUR_FLAGS0	0x0090	W	0x00000000	Cur OSD statistics result
RGA2_OSD_CUR_FLAGS1	0x009C	W	0x00000000	Cur OSD statistics result
RGA2_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA2_SRC_INFO	0x0104	W	0x00000000	RGA source information register
RGA2_SRC_BASE0	0x0108	W	0x00000000	RGA source image Y/RGB base address register
RGA2_SRC_BASE1	0x010C	W	0x00000000	RGA source image Cb/Cbr base address register
RGA2_SRC_BASE2	0x0110	W	0x00000000	RGA source image Cr base address register
RGA2_SRC_BASE3	0x0114	W	0x00000000	RGA source image 1 base address register
RGA2_SRC_VIR_INFO	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number register

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Name	Offset	Size	Reset Value	Description
RGA2_SRC_ACT_INFO	0x011C	W	0x00000000	RGA source image active width/height register
RGA2_SRC_X_FACTOR	0x0120	W	0x00000000	RGA source image horizontal scaling factor
RGA2_OSD_CTRL0	0x0120	W	0x00000000	RGA OSD control register
RGA2_SRC_Y_FACTOR	0x0124	W	0x00000000	RGA source image vertical scaling factor
RGA2_OSD_CTRL1	0x0124	W	0x00000000	RGA OSD control register
RGA2_SRC_BG_COLOR	0x0128	W	0x00000000	RGA source image background color
RGA2_OSD_COLOR0	0x0128	W	0x00000000	OSD color0
RGA2_SRC_FG_COLOR	0x012C	W	0x00000000	RGA source image foreground color
RGA2_OSD_COLOR1	0x012C	W	0x00000000	OSD color1
RGA2_MOSAIC_MODE	0x0130	W	0x00000000	RGA mosaic function mode select.
RGA2_SRC_TR_COLOR0	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_CP_GR_A	0x0130	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_OSD_LAST_FLAGS0	0x0130	W	0x00000000	Flags for cur OSD auto inversion using
RGA2_SRC_TR_COLOR1	0x0134	W	0x00000000	RGA source image transparency color max value
RGA2_CP_GR_B	0x0134	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_OSD_LAST_FLAGS1	0x0134	W	0x00000000	Flags for cur OSD auto inversion using
RGA2_DST_INFO	0x0138	W	0x00000000	RGA destination format register
RGA2_DST_BASE0	0x013C	W	0x00000000	RGA destination image base address 0 register
RGA2_DST_BASE1	0x0140	W	0x00000000	RGA destination image base address 1 register
RGA2_DST_BASE2	0x0144	W	0x00000000	RGA destination image base address 2 register
RGA2_DST_VIR_INFO	0x0148	W	0x00000000	RGA destination image virtual width/height register
RGA2_DST_ACT_INFO	0x014C	W	0x00000000	RGA destination image active width/height register
RGA2_ALPHA_CTRL0	0x0150	W	0x00000000	Alpha control register 0
RGA2_ALPHA_CTRL1	0x0154	W	0x00000000	Register0000 Description
RGA2_FADING_CTRL	0x0158	W	0x00000000	Fading control register
RGA2_PAT_CON	0x015C	W	0x00000000	Pattern size/offset register
RGA2_NN_QUANTIZE_SCALE	0x0160	W	0x00000000	Quantize scale of RGB (2bit integer+8bit fraction, 0~3.99)
RGA2_CP_GR_G	0x0160	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_DST_Y4MAP_LUT0	0x0160	W	0x76543210	Y4MAP LUT REGS from lut0 to lut7
RGA2_OSD_INVERTSION_CAL0	0x0160	W	0x00000000	Used for OSD inversion calculation clip
RGA2_NN_QUANTIZE_OFFSET	0x0164	W	0x00000000	Quantize offset of RGB (1bit signed + 8bit integer)
RGA2_CP_GR_R	0x0164	W	0x00000000	RGA color gradient fill step register (color fill mode)

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Name	Offset	Size	Reset Value	Description
RGA2_DST_Y4MAP_LUT1	0x0164	W	0xFEDCBA98	Y4MAP LUT REGS from lut8 to lut15
RGA2_OSD_INVERTSION_CAL1	0x0164	W	0x00000000	Used for OSD inversion calculation clip
RGA2_MASK_BASE	0x0168	W	0x00000000	RGA mask base address register
RGA2_OSD_ST_LUMA0	0x0400	W	0x00000000	Luminance statistics for the OSD block 0-3
RGA2_OSD_ST_LUMA1	0x0404	W	0x00000000	Luminance statistics for the OSD block 4-7
RGA2_OSD_ST_LUMA2	0x0408	W	0x00000000	Luminance statistics for the OSD block 8-11
RGA2_OSD_ST_LUMA3	0x040C	W	0x00000000	Luminance statistics for the OSD block 12-15
RGA2_OSD_ST_LUMA4	0x0410	W	0x00000000	Luminance statistics for the OSD block 16-19
RGA2_OSD_ST_LUMA5	0x0414	W	0x00000000	Luminance statistics for the OSD block 20-23
RGA2_OSD_ST_LUMA6	0x0418	W	0x00000000	Luminance statistics for the OSD block 24-27
RGA2_OSD_ST_LUMA7	0x041C	W	0x00000000	Luminance statistics for the OSD block 28-31
RGA2_OSD_ST_LUMA8	0x0420	W	0x00000000	Luminance statistics for the OSD block 32-35
RGA2_OSD_ST_LUMA9	0x0424	W	0x00000000	Luminance statistics for the OSD block 36-39
RGA2_OSD_ST_LUMA10	0x0428	W	0x00000000	Luminance statistics for the OSD block 40-43
RGA2_OSD_ST_LUMA11	0x042C	W	0x00000000	Luminance statistics for the OSD block 44-47
RGA2_OSD_ST_LUMA12	0x0430	W	0x00000000	Luminance statistics for the OSD block 48-51
RGA2_OSD_ST_LUMA13	0x0434	W	0x00000000	Luminance statistics for the OSD block 52-55
RGA2_OSD_ST_LUMA14	0x0438	W	0x00000000	Luminance statistics for the OSD block 56-59
RGA2_OSD_ST_LUMA15	0x043C	W	0x00000000	Luminance statistics for the OSD block 60-63
RGA2_DTE_ADDR	0x0F00	W	0x00000000	MMU current page Table address
RGA2_STATUS	0x0F04	W	0x00000000	MMU status register
RGA2_COMMAND	0x0F08	W	0x00000000	MMU command register
RGA2_PAGE_FAULT_ADDR	0x0F0C	W	0x00000000	MMU logical address of last page fault
RGA2_ZAP_ONE_LINE	0x0F10	W	0x00000000	MMU Zap cache line register
RGA2_INT_RAWSTAT	0x0F14	W	0x00000000	MMU raw interrupt status register
RGA2_INT_CLEAR	0x0F18	W	0x00000000	MMU raw interrupt status register
RGA2_INT_MASK	0x0F1C	W	0x00000000	MMU raw interrupt status register
RGA2_INT_STATUS	0x0F20	W	0x00000000	MMU raw interrupt status register
RGA2_AUTO_GATING	0x0F24	W	0x80000000	mmu auto gating

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

4.4.3 Detail Registers Description

RGA2_SYS_CTRL

Address: Operational Base(0xFF440000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	sw_src0yuv420sp_rd_opt_dis SRC0 YUV420SP format read optimization disable bit.
11	RW	0x0	sw_dst_wr_opt_dis AXI write optimization disable bit(If this bit equal to 0, the write data will continuously in one whole burst)
10	W1C	0x0	sys_cmd_continue_p RGA2 read continue pulse, and read commands will continue to be sent.
9	RW	0x0	sw_rd_hold_mode_en RGA read hold mode enable bit, the read command will be holden when RGA raising read line count interrupt.
8	RO	0x0	reserved
7	RW	0x0	sys_rst_handsave_p It would save protect-rstn into initial status if long time dead in protect-rstn status(auto clear into '0').
6	RW	0x1	sw_rst_protect_e Protect-rstn mode enable. It would be ensure all AXI write/read operation into completion status when sw_cclk_sreset_p or sw_aclk_sreset_p valid.
5	RW	0x0	sw_auto_rst It would auto-resetn after one frame finish. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sys_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
3	WO	0x0	sys_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 1'b0: Disable 1'b1: Enable
1	WO	0x0	sw_cmd_mode RGA command mode 1'b0: Slave mode 1'b1: Master mode
0	W1C	0x0	sys_cmd_op_st_p Only used in passive (slave) control mode

RGA2_CMD_CTRL

Address: Operational Base(0xFF440000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop_mode RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to 1.

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Bit	Attr	Reset Value	Description
1	WO	0x0	sys_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total command number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	RW	0x0	sys_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total command number would reset to RGA_INCR_CMD_NUM.

RGA2_CMD_BASE

Address: Operational Base(0xFF440000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cmd_base RGA command codes base address

RGA2_STATUS1

Address: Operational Base(0xFF440000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RO	0x00	reserved
0	RO	0x0	sw_rga_sta RGA engine status 1'b0: Idle 1'b1: Working

RGA2_INT

Address: Operational Base(0xFF440000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	W1C	0x0	sys_intr_line_wr_clr RGA2 write line count interrupt clear pulse.
15	W1C	0x0	sys_intr_line_rd_clr RGA2 read line count interrupt clear pulse.
14	RW	0x0	sw_intr_line_wr_en RGA2 write line count and interrupt enable bit.
13	RW	0x0	sw_intr_line_rd_en RGA read line count and interrupt enable bit.
12	RO	0x0	ro_write_cnt_intr RGA2 write data line count reach threshold interrupt flag.
11	RO	0x0	ro_read_cnt_intr RGA2 read data line count reach threshold interrupt flag.
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_rpp_err_e RPP error interrupt enable
8	RW	0x0	sw_intr_bus_err_e Bus error interrupt enable
7	W1C	0x0	sys_intr_cf_clr Current command finished interrupt clear

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Bit	Attr	Reset Value	Description
6	W1C	0x0	sys_intr_af_clr All command finished interrupt clear
5	W1C	0x0	sys_intr_rpp_err_clr RPP error interrupt clear
4	W1C	0x0	sys_intr_bus_err_clr Bus error interrupt clear
3	RO	0x0	ro_cmd_cur_finish_intr Current command finished interrupt flag
2	RO	0x0	ro_cmd_all_finish_intr All command finished interrupt flag
1	RO	0x0	ro_rpp_error_intr RPP error interrupt flag
0	RO	0x0	ro_bus_error_intr Bus error interrupt flag

RGA2_MMU_CTRL0

Address: Operational Base(0xFF440000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:15	RW	0x0	sw_mmu_qos_num2 RGA DATA QOS number2.
14:12	RW	0x0	sw_mmu_qos_num3 RGA MMU/CMD QOS number3.
11	RW	0x0	sw_qos_en RGA MMU QOS enable bit.
10:9	RW	0x0	sw_els_ch_priority The priority of this channel
8:7	RW	0x0	sw_dst_ch_priority The priority of this channel
6:5	RW	0x0	sw_src1_ch_priority The priority of this channel
4:3	RW	0x0	sw_src_ch_priority The priority of this channel
2:0	RO	0x0	reserved

RGA2_STATUS2

Address: Operational Base(0xFF440000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:11	RO	0x0	rpp_mkram_rready Rpp mkram rready
10:6	RO	0x00	dstrpp_outbuf_rready Dstrpp outbuf rready
5:2	RO	0x0	srcrpp_outbuf_rready Srcrpp outbuf rready
1	RO	0x0	bus_error Bus error status
0	RO	0x0	rpp_error RPP error status

RGA2_WORK_CNT

Address: Operational Base(0xFF440000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:0	RO	0x0000000	sw_work_cnt RGA total working counter

RGA2_VERSION_INFO

Address: Operational Base(0xFF440000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	major Used for IP structure version information
23:20	RW	0x0	minor Big feature change under same structure
19:0	RW	0x00000	svnbuild RTL current SVN number

RGA2_READ_LINE_CNT_TH

Address: Operational Base(0xFF440000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x1fff	sw_intr_line_rd_th RGA read interrupt line count threshold.

RGA2_WRITE_LINE_CNT_TH

Address: Operational Base(0xFF440000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_intr_line_wr_step The threshold step size for RGA2, and the interrupt raising when write count reach very threshold(start + N * step).
15:13	RO	0x0	reserved
12:0	RW	0x1fff	sw_intr_line_wr_start RGA2 write interrupt line count threshold start value.

RGA2_INT_LINE_CNT

Address: Operational Base(0xFF440000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	ro_write_line_cnt RGA write interrupt line count. (Read Only)
15:14	RO	0x0	reserved
13	RO	0x0	ro_dma_cmd_hold RGA raising the dma hold when read interrupt.
12:0	RO	0x0000	ro_read_line_cnt RGA read interrupt line count. (Read Only)

RGA2_DST_CSC_00

Address: Operational Base(0xFF440000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_dst_csc_y_min Dst csc Y channel clip min value
23:16	RW	0x00	sw_dst_csc_y_max Dst csc Y channel clip max value.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x0bc	sw_dst_coe_00 1bit signed+2bit integer+8bit float factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_01

Address: Operational Base(0xFF440000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_dst_csc_uv_min Dst csc UV channel clip min value.
23:16	RW	0x00	sw_dst_csc_uv_max Dst csc UV channel clip max value.
15:11	RO	0x00	reserved
10:0	RW	0x274	sw_dst_coe_01 1bit signed+2bit integer+8bit float factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_02

Address: Operational Base(0xFF440000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x040	sw_dst_coe_02 1bit signed+2bit integer+8bit float factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_OFF0

Address: Operational Base(0xFF440000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x04200	sw_dst_coe_off0 1bit signed+10bit integer+8bit float factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_10

Address: Operational Base(0xFF440000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x798	sw_dst_coe_10 1bit signed+2bit integer+8bit float factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_11

Address: Operational Base(0xFF440000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x6a4	sw_dst_coe_11 1bit signed+2bit integer+8bit float factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_12

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Address: Operational Base(0xFF440000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x1c0	sw_dst_coe_12 1bit signed+2bit integer+8bit float factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_OFF1

Address: Operational Base(0xFF440000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x20200	sw_dst_coe_off1 1bit signed+10bit integer+8bit float factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_20

Address: Operational Base(0xFF440000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x1c0	sw_dst_coe_20 1bit signed+2bit integer+8bit float factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_21

Address: Operational Base(0xFF440000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x668	sw_dst_coe_21 1bit signed+2bit integer+8bit float factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_22

Address: Operational Base(0xFF440000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x7d8	sw_dst_coe_22 1bit signed+2bit integer+8bit float factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_OFF2

Address: Operational Base(0xFF440000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x20200	sw_dst_coe_off2 1bit signed+10bit integer+8bit float factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_OSD_CUR_FLAGS0

Address: Operational Base(0xFF440000) + offset (0x0090)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_cur_osd_flags0 Cur OSD statistics result

RGA2_OSD_CUR_FLAGS1

Address: Operational Base(0xFF440000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_cur_osd_flags1 Cur OSD statistics result

RGA2_MODE_CTRL

Address: Operational Base(0xFF440000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	sw_yin_yout_mode RGA Y in Y out mode enable bit.
9	RW	0x0	sw_mosaic_en RGA Mosaic function enable bit.
8	RW	0x0	sw_osd_en RGA OSD function enable bit.
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 1'b0: Clip 1'b1: Not-clip
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565) for ARGB888 to RGBX/RGB565 color key. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 1'b0: Solid color 1'b1: Pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 1'b0: SRC + DST => DST 1'b1: SRC + SRC1 => DST
2:0	RW	0x0	sw_render_mode RGA 2D render mode 3'b000: Bitblt 3'b001: Color palette 3'b010: Rectangle fill 3'b011: Update palette LUT/pattern ram

RGA2_SRC_INFO

Address: Operational Base(0xFF440000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_src_yuv10_round_e This bit valid when RGA2E/2L support YUV 10bit picture input 1'b0: YUV 10bit to 8bit round disable 1'b1: YUV 10bit to 8bit round enable

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Bit	Attr	Reset Value	Description
27	RW	0x0	sw_src_yuv10_e This bit valid when RGA2E/2L support YUV 10bit picture input. 1'b0: YUV 10bit disable 1'b1: YUV 10bit enable
26	RW	0x0	sw_vsp_mode 1'b0:By-cubic 1'b1:Bi-linear
25:24	RW	0x0	sw_bic_coe_sel SRC BI-cubic scaling coefficient select 2'b00: CATROM 2'b01: MITCHELL 2'b10: HERMITE 2'b11: B-SPLINE
23	RW	0x0	sw_src_dither_up SRC dither up enable 1'b0: Disable 1'b1: Enable
22:19	RW	0x0	sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit
18	RW	0x0	sw_src_trans_mode Source transparency mode 1'b0: Normal stencil test (color key) 1'b1: Inverted stencil test
17:16	RW	0x0	sw_src_vscl_mode SRC vertical scaling mode 2'b00No scaling 2'b01: Down-scaling 2'b10: Up-scaling
15:14	RW	0x0	sw_src_hscl_mode SRC horizontal scaling mode 2'b00No scaling 2'b01: Down-scaling 2'b10: Up-scaling
13:12	RW	0x0	sw_src_mir_mode SRC mirror mode 2'b00: No mirror 2'b01: X mirror 2'b10: Y mirror 2'b11: X mirror + y mirror
11:10	RW	0x0	sw_src_rot_mode SRC rotation mode 2'b00: 0 degree 2'b01: 90 degree 2'b10: 180 degree 2'b11: 270 degree
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 2'b00: Bypass 2'b01: BT.601-range0(limit range) 2'b10: BT.601-range1(full range) 2'b11: BT.709-range0(limit range)

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Bit	Attr	Reset Value	Description
7	RW	0x0	sw_cp_endian Source Color palette endian swap 1'b0: Big endian 1'b1: Little endian
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 1'b0: CrCb 1'b1: CbCr For YVYU422 mode, UV swap 1'b0: YVYU422(U LSB) 1'b1: YUYV422(V LSB)
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 1'b0: BGR 1'b1: RGB For YVYU422 mode, YC swap 1'b0: YVYU422(U LSB) 1'b1: VYUY422(Y LSB)
3:0	RW	0x0	sw_src_fmt Source bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 4'b0111: YVYU422(U LSB) 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P 4'b1100: 1BPP (color palette) 4'b1101: 2BPP (color palette) 4'b1110: 4BPP (color palette) 4'b1111: 8BPP (color palette)

RGA2_SRC_BASE0

Address: Operational Base(0xFF440000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 Source image Y/RGB base address

RGA2_SRC_BASE1

Address: Operational Base(0xFF440000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 Source image Cb base address (YUV422/420-P) Source image Cb/Cr base address (YU,V422/420-SP)

RGA2_SRC_BASE2

Address: Operational Base(0xFF440000) + offset (0x0110)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base2 Source image Cr base address (YUV422/420-P)

RGA2_SRC_BASE3

Address: Operational Base(0xFF440000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base3 Source image 1 RGB base address(source bitblt mode1)

RGA2_SRC_VIR_INFO

Address: Operational Base(0xFF440000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_mask_vir_stride Mask image virtual stride (words)
15	RO	0x0	reserved
14:0	RW	0x0000	sw_src_vir_stride SRC image virtual stride (words)

RGA2_SRC_ACT_INFO

Address: Operational Base(0xFF440000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_src_act_height Source image active height
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_src_act_width Source image active width

RGA2_SRC_X_FACTOR

Address: Operational Base(0xFF440000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor =((SRC_ACT_WIDTH-1)/(DST_ACT_WIDTH-1)) * 65536
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor =(DST_ACT_WIDTH/(SRC_ACT_WIDTH) * 65536 + 1

RGA2_OSD_CTRL0

Address: Operational Base(0xFF440000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_osd_2bpp_mode OSD 2bpp(1bit alpha, 1bit color) format.
29:20	RW	0x000	sw_osd_fix_width If sw_osd_width_mode is fix mode, use this signal. Each real OSD width = (sw_osd_fix_width+1)*2
19:10	RW	0x000	sw_osd_flags_index Cur OSD flags ID
9:4	RW	0x00	sw_osd_blk_num OSD block number

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Bit	Attr	Reset Value	Description
3	RW	0x0	sw_osd_width_mode OSD width mode 1'b0: Each OSD width is fix(use sw_osd_fix_width) 1'b1: Each OSD width is different (use LUT mode to load each OSD width)
2	RW	0x0	sw_osd_ver_mode OSD shape mode 1'b0: OSD is horizontal 1'b1: OSD is vertical
1:0	RW	0x0	sw_osd_mode OSD calculate mode 2'b00: OSD static disable and OSD auto inversion disable 2'b01: OSD static only mode 2'b10: OSD auto inversion only mode 2'b11: OSD static enable and OSD auto inversion enable

RGA2_SRC_Y_FACTOR

Address: Operational Base(0xFF440000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor =((SRC_ACT_ HEIGHT -1)/(DST_ACT_ HEIGHT -1)) * 65536
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor =(DST_ACT_ HEIGHT /(SRC_ACT_ HEIGHT) * 65536 + 1

RGA2_OSD_CTRL1

Address: Operational Base(0xFF440000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	sw_osd_unfix_index Cur OSD unfix width configuration ID
15	RO	0x0	reserved
14	RW	0x0	sw_osd_invert_c_dis OSD auto inversion C/RB channel disable bit
13	RW	0x0	sw_osd_invert_y_dis OSD auto inversion Y/G channel disable bit
12	RW	0x0	sw_osd_invert_a_en OSD auto inversion alpha channel enable bit
11:4	RW	0x00	sw_osd_thresh If cur OSD average luminance > sw_osd_thresh, cur osd flag=1.
3	RW	0x0	sw_osd_auto_invert_mode OSD auto inversion mode 1'b0: OSD auto inversion use (sw_osd_max - DATA) 1'b1: OSD auto inversion use swap (If YUV overlay, UV swap; If RGB overlay, RB swap)
2	RW	0x0	sw_osd_default_color OSD default color mode 1'b0: OSD default color is bright, OSD content will invert when background is bright 1'b1: OSD default color is dark, OSD content will invert when background is dark

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_osd_flag_sel OSD overlay use flags mode 1'b0: OSD overlay use internal data 1'b1: OSD overlay use external data(sw_osd_last_result)
0	RW	0x0	sw_osd_color_sel 1'b0: Select SRC1 data for OSD overlay content 1'b1: Select config data for OSD overlay content

RGA2_SRC_BG_COLOR

Address: Operational Base(0xFF440000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

RGA2_OSD_COLOR0

Address: Operational Base(0xFF440000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_osd2bpp_alpha0 Substitute value for alpha to be 0 when in OSD ARGB2BPP format.
23:0	RW	0x000000	sw_osd_color0 This color will be used when sw_osd_color_sel is 1.

RGA2_SRC_FG_COLOR

Address: Operational Base(0xFF440000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

RGA2_OSD_COLOR1

Address: Operational Base(0xFF440000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_osd2bpp_alpha1 Substitute value for alpha to be 0 when in OSD ARGB2BPP format.
23:0	RW	0x000000	sw_osd_color1 This color will be used when sw_osd_color_sel is 1.

RGA2_MOSAIC_MODE

Address: Operational Base(0xFF440000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	sw_mosaic_mode RGA mosaic function mode select. 3'b000: 8 * 8 pixel 3'b001: 16 * 16 pixel 3'b010: 32 * 32 pixel 3'b011: 64 * 64 pixel 3b100: 128 * 128 pixel Others: Reserved

RGA2_SRC_TR_COLOR0

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Address: Operational Base(0xFF440000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin Source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin Source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin Source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin Source image transparency color R min value

RGA2_CP_GR_A

Address: Operational Base(0xFF440000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

RGA2_OSD_LAST_FLAGS0

Address: Operational Base(0xFF440000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_last_flags0 This signal means sw_osd_last_result[31:0]

RGA2_SRC_TR_COLOR1

Address: Operational Base(0xFF440000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax Source image transparency color A max value
23:16	RW	0x00	sw_src_trans_bmax Source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax Source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax Source image transparency color R max value

RGA2_CP_GR_B

Address: Operational Base(0xFF440000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

RGA2_OSD_LAST_FLAGS1

Address: Operational Base(0xFF440000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_last_flags1 This signal means sw_osd_last_result[63:32]

RGA2_DST_INFO

Address: Operational Base(0xFF440000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RW	0x0	sw_dst_uvvds_mode Destination Cb-Cr down-sampling vertical optimization (valid for YUV420 P/SP format) 1'b0: Optimization enable 1'b1: Optimization disable
26	RW	0x0	sw_dst_nn_quantize_en Destination output RGB quantize calculate 1'b0: Quantize calculate disable 1'b1: Quantize calculate enable
25	RW	0x0	sw_dst_fmt_y4_en Destination output Y channel 4bit and UV 0bit 1'b0: Y4 out disable 1'b1: Y4 out enable
24	RW	0x0	sw_dst_fmt_yuv400_en Destination Cb-Cr output disable (valid for YUV420/2 P/SP format) 1'b0: CbCr output normal 1'b1: CbCr output disable
23	RW	0x0	sw_dst_uvhds_mode Destination Cb-Cr down-sampling horizontal optimization (valid for YUV420/2 P/SP format) 1'b0: Optimization enable 1'b1: Optimization disable
22	RW	0x0	sw_src1_csc_clip Src1 read BGR2YUV Clip mode(RGB from 0~255 clip to 16~235) 1'b0: Clip disable 1'b1: Clip enable
21:20	RW	0x0	sw_src1_csc_mode SRC1 read bitmap RGB2YUV conversion mode 2'b00: Bypass 2'b01: BT.601-range0, BT601_l, Y{00,255}, UV{00,255} 2'b10: BT.601-range1, BT601_f, Y{16,235}, UV{16,240} 2'b11: BT.709,Y{16,235},UV{16,240}
19	RW	0x0	sw_dst_csc_mode_2 sw_dst_csc_mode[2]+sw_dst_csc_mode[1:0]; DST read bitmap CSC(r2y/y2y) conversion mode under sw_dst_csc_mode[2]=1'b0: 3'b1xx: Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0 U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1 V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2 without clip
18	RW	0x0	sw_dst_csc_clip Dst write RGB2YUV Clip mode(RGB from 0~255 clip to 16~235) 1'b1: Clip enable 1'b0: Clip disable
17:16	RW	0x0	sw_dst_csc_mode_01 sw_dst_csc_mode[1:0] under sw_dst_csc_mode[2]=1'b0: DST read bitmap RGB2YUV conversion mode 3'b000: Bypass 3'b001: BT.601-range0,BT601_l,Y{00,255},UV{00,255} 3'b010: BT.601-range1,BT601_f,Y{16,235},UV{16,240} 3'b011: BT.709,Y{16,235},UV{16,240}

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	sw_dither_mode DST dither down bit mode 2'b00: 888 to 666 2'b01: 888 to 565 2'b10: 888 to 555 2'b11: 888 to 444 DST YUV dither down bit mode 2'b00: Y8 to Y4 others:Y8 to Y1
13	RW	0x0	sw_dither_down DST dither down enable 1'b0: Disable 1'b1: Enable
12	RW	0x0	sw_src1_dither_up DST/SRC1 dither up enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	sw_src1_alpha_swap Source 1 bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
10	RW	0x0	sw_src1_rbswap Source 1 bitmap data RB swap 1'b0: BGR 1'b1: RGB
9:7	RW	0x0	sw_src1_fmt Source 1 bitmap data format 3'b000: ABGR888 3'b001: XBGR888 3'b010: BGR packed 3'b100: RGB565 3'b101: ARGB1555 3'b110: ARGB4444
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 1'b0: CrCb 1'b1: CbCr
5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 1'b0: BGR 1'b1: RGB

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 when sw_dst_fmt_yuv400_en=1, YUV420/2 P/SP format will change to YUV400: 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P only RGA2E has yuyv output format feature: 4'b1100: YVYU422(U, LSB) 4'b1101: YVYU420(U, LSB) 4'b1110: VYUY422(Y, LSB) 4'b1111: VYUY420(Y, LSB)

RGA2_DST_BASE0

Address: Operational Base(0xFF440000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 Destination image Y/RGB base address

RGA2_DST_BASE1

Address: Operational Base(0xFF440000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 Destination image Cb/CbCr base address

RGA2_DST_BASE2

Address: Operational Base(0xFF440000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 Destination image Cr base address

RGA2_DST_VIR_INFO

Address: Operational Base(0xFF440000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_src1_vir_stride Source image 1 virtual stride (words)
15	RO	0x0	reserved
14:0	RW	0x0000	sw_dst_vir_stride Destination image virtual stride(words)

RGA2_DST_ACT_INFO

Address: Operational Base(0xFF440000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_dst_act_width Destination image active width

RGA2_ALPHA_CTRL0

Address: Operational Base(0xFF440000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_mask_endian ROP4 mask endian swap 1'b0: Big endian 1'b1: Little endian
19:12	RW	0x00	sw_dst_global_alpha Global alpha value of DST(Agd)
11:4	RW	0x00	sw_src_global_alpha Global alpha value of SRC(Ags) Fading value in fading mod
3:2	RW	0x0	sw_rop_mode ROP mode select 2'b00: ROP 2 2'b01: ROP 3 2'b10: ROP 4
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 1'b0: Alpha 1'b1: ROP
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 1'b0: Disable 1'b1: Enable

RGA2_ALPHA_CTRL1

Address: Operational Base(0xFF440000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 SRC Transparent/opaque of alpha channel (As1) 1'b0: As 1'b1: 255-As
28	RW	0x0	sw_dst_alpha_m1 DST Transparent/opaque of alpha channel (Ad1) 1'b0: Ad 1'b1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha SRC blend mode select of alpha channel (As1_) 2'b00: Ags 2'b01: As1 2'b10: (As1*Ags)>>8 2'b11: reserved
25:24	RW	0x0	sw_dst_blend_m1 Alpha DST blend mode select of alpha channel(Ad1_) 2'b00: Agd 2'b01: Ad1 2'b10: (Ad1*Agd)>>8 2'b11: reserved

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Bit	Attr	Reset Value	Description
23	RW	0x0	sw_src_alpha_cal_m1 Alpha SRC calculate mode of alpha channel(As1) 1'b0: As1= As1_ + (As1_ >>7) 1'b1: As1= As1 _
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha DST calculate mode of alpha channel(Ad1) 1'b0: Ad1= Ad1 + (Ad1_ >>7) 1'b1: Ad1= Ad1_
21:19	RW	0x0	w_src_factor_m1 SRC factor mode of alpha channel(Fs1) 3'b000: 0 3'b001: 256 3'b010: Ad1 3'b011: 256-Ad1 3'b100: As1
18:16	RW	0x0	sw_dst_factor_m1 DST factor mode of alpha channel(Fd1) 3'b000: 0 3'b001: 256 3'b010: As1 3'b011: 256-As1 3'b100: Ad1
15	RW	0x0	sw_src_alpha_m0 Src Transparent/opaque of color channel (As0) 1'b0: As 1'b1: 255-As
14	RW	0x0	sw_dst_alpha_m0 DST Transparent/opaque of color channel (Ad0) 1'b0: Ad 1'b1: 255-Ad
13:12	RW	0x0	sw_src_blend_m0 Alpha SRC blend mode select of color channel (As0_) 2'b00: Ags 2'b01: As0 2'b10: (As0*Ags)>>8 2'b11: Reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha DST blend mode select of color channel(Ad0_) 2'b00: Agd 2'b01: Ad0 2'b10: (Ad0*Agd)>>8 2'b11: Reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha SRC calculate mode of color channel(As0) 1'b0: As0= As0_ + (As0_ >>7) 1'b1: As0= As0 _
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha DST calculate mode of color channel(Ad0) 1'b0: Ad0= Ad0 + (Ad0_ >>7) 1'b1: Ad0= Ad0_

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_src_factor_m0 SRC factor mode of color channel(Fs0) 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0
4:2	RW	0x0	sw_dst_factor_m0 Dst factor mode of color channel(Fd0) 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0
1	RW	0x0	sw_src_color_m0 SRC color select(Cs) 1'b0: Cs 1'b1: Cs * As0
0	RW	0x0	sw_dst_color_m0 SRC color select(Cd) 1'b0: Cd 1'b1: Cd * Ad0

RGA2_FADING_CTRL

Address: Operational Base(0xFF440000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

RGA2_PAT_CON

Address: Operational Base(0xFF440000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

RGA2_NN_QUANTIZE_SCALE

Address: Operational Base(0xFF440000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x000	sw_nn_quantize_scale_b Quantize scale of Blue (2bit integer+8bit fraction, 0--3.99)
19:10	RW	0x000	sw_nn_quantize_scale_g Quantize scale of Green (2bit integer+8bit fraction, 0--3.99)
9:0	RW	0x000	sw_nn_quantize_scale_r Quantize scale of Red (2bit integer+8bit fraction, 0--3.99)

RGA2_CP_GR_G

Address: Operational Base(0xFF440000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_g Y gradient value of Green (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_g X gradient value of Green (signed 8.8)

RGA2_DST_Y4MAP_LUT0

Address: Operational Base(0xFF440000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x76543210	sw_dst_y4map_lut0 Y4 lut from lut0 to lut7

RGA2_OSD_INVERTSION_CAL0

Address: Operational Base(0xFF440000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_osd_maxc Used for OSD inversion calculation C/RB channel clip
23:16	RW	0x00	sw_osd_minc Used for OSD inversion calculation C/RB channel clip
15:8	RW	0x00	sw_osd_maxy Used for OSD inversion calculation Y/G channel clip
7:0	RW	0x00	sw_osd_miny Used for OSD inversion calculation Y/G channel clip

RGA2_NN_QUANTIZE_OFFSET

Address: Operational Base(0xFF440000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	sw_nn_quantize_offset_b Quantize offset of Blue(1bit signed + 8bit integer)
19	RO	0x0	reserved
18:10	RW	0x000	sw_nn_quantize_offset_g Quantize offset of Green (1bit signed + 8bit integer)
9	RO	0x0	reserved
8:0	RW	0x000	sw_nn_quantize_offset_r Quantize offset of Red(1bit signed + 8bit integer)

RGA2_CP_GR_R

Address: Operational Base(0xFF440000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0x0000	sw_gradient_x_r X gradient value of Red(signed 8.8)

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RGA2_DST_Y4MAP_LUT1

Address: Operational Base(0xFF440000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0xfedcba98	sw_dst_y4map_lut1 Y4 lut from lut8 to lut15

RGA2_OSD_INVERTSION_CAL1

Address: Operational Base(0xFF440000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	sw_osd_maxa Used for OSD inversion calculation A channel clip
7:0	RW	0x00	sw_osd_mina Used for OSD inversion calculation A channel clip

RGA2_MASK_BASE

Address: Operational Base(0xFF440000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base Mask base address in ROP4 mode LUT/ pattern load base address

RGA2_OSD_ST_LUMA0

Address: Operational Base(0xFF440000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma3 Luminance statistics for the OSD block 3
23:16	RO	0x00	ro_osd_st_luma2 Luminance statistics for the OSD block 2
15:8	RO	0x00	ro_osd_st_luma1 Luminance statistics for the OSD block 1
7:0	RO	0x00	ro_osd_st_luma0 Luminance statistics for the OSD block 0

RGA2_OSD_ST_LUMA1

Address: Operational Base(0xFF440000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma7 Luminance statistics for the OSD block 7
23:16	RO	0x00	ro_osd_st_luma6 Luminance statistics for the OSD block 6
15:8	RO	0x00	ro_osd_st_luma5 Luminance statistics for the OSD block 5
7:0	RO	0x00	ro_osd_st_luma4 Luminance statistics for the OSD block 4

RGA2_OSD_ST_LUMA2

Address: Operational Base(0xFF440000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma11 Luminance statistics for the OSD block 11
23:16	RO	0x00	ro_osd_st_luma10 Luminance statistics for the OSD block 10
15:8	RO	0x00	ro_osd_st_luma9 Luminance statistics for the OSD block 9

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	ro_osd_st_luma8 Luminance statistics for the OSD block 8

RGA2_OSD_ST_LUMA3

Address: Operational Base(0xFF440000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma15 Luminance statistics for the OSD block 15
23:16	RO	0x00	ro_osd_st_luma14 Luminance statistics for the OSD block 14
15:8	RO	0x00	ro_osd_st_luma13 Luminance statistics for the OSD block 13
7:0	RO	0x00	ro_osd_st_luma12 Luminance statistics for the OSD block 12

RGA2_OSD_ST_LUMA4

Address: Operational Base(0xFF440000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma19 Luminance statistics for the OSD block 19
23:16	RO	0x00	ro_osd_st_luma18 Luminance statistics for the OSD block 18
15:8	RO	0x00	ro_osd_st_luma17 Luminance statistics for the OSD block 17
7:0	RO	0x00	ro_osd_st_luma16 Luminance statistics for the OSD block 16

RGA2_OSD_ST_LUMA5

Address: Operational Base(0xFF440000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma23 Luminance statistics for the OSD block 23
23:16	RO	0x00	ro_osd_st_luma22 Luminance statistics for the OSD block 22
15:8	RO	0x00	ro_osd_st_luma21 Luminance statistics for the OSD block 21
7:0	RO	0x00	ro_osd_st_luma20 Luminance statistics for the OSD block 20

RGA2_OSD_ST_LUMA6

Address: Operational Base(0xFF440000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma27 Luminance statistics for the OSD block 27
23:16	RO	0x00	ro_osd_st_luma26 Luminance statistics for the OSD block 26
15:8	RO	0x00	ro_osd_st_luma25 Luminance statistics for the OSD block 25
7:0	RO	0x00	ro_osd_st_luma24 Luminance statistics for the OSD block 24

RGA2_OSD_ST_LUMA7

Address: Operational Base(0xFF440000) + offset (0x041C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma31 Luminance statistics for the OSD block 31
23:16	RO	0x00	ro_osd_st_luma30 Luminance statistics for the OSD block 30
15:8	RO	0x00	ro_osd_st_luma29 Luminance statistics for the OSD block 29
7:0	RO	0x00	ro_osd_st_luma28 Luminance statistics for the OSD block 28

RGA2_OSD_ST_LUMA8

Address: Operational Base(0xFF440000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma35 Luminance statistics for the OSD block 35
23:16	RO	0x00	ro_osd_st_luma34 Luminance statistics for the OSD block 34
15:8	RO	0x00	ro_osd_st_luma33 Luminance statistics for the OSD block 33
7:0	RO	0x00	ro_osd_st_luma32 Luminance statistics for the OSD block 32

RGA2_OSD_ST_LUMA9

Address: Operational Base(0xFF440000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma39 Luminance statistics for the OSD block 39
23:16	RO	0x00	ro_osd_st_luma38 Luminance statistics for the OSD block 38
15:8	RO	0x00	ro_osd_st_luma37 Luminance statistics for the OSD block 37
7:0	RO	0x00	ro_osd_st_luma36 Luminance statistics for the OSD block 36

RGA2_OSD_ST_LUMA10

Address: Operational Base(0xFF440000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma43 Luminance statistics for the OSD block 43
23:16	RO	0x00	ro_osd_st_luma42 Luminance statistics for the OSD block 42
15:8	RO	0x00	ro_osd_st_luma41 Luminance statistics for the OSD block 41
7:0	RO	0x00	ro_osd_st_luma40 Luminance statistics for the OSD block 40

RGA2_OSD_ST_LUMA11

Address: Operational Base(0xFF440000) + offset (0x042C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma47 Luminance statistics for the OSD block 47
23:16	RO	0x00	ro_osd_st_luma46 Luminance statistics for the OSD block 46
15:8	RO	0x00	ro_osd_st_luma45 Luminance statistics for the OSD block 45

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	ro_osd_st_luma44 Luminance statistics for the OSD block 44

RGA2_OSD_ST_LUMA12

Address: Operational Base(0xFF440000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma51 Luminance statistics for the OSD block 51
23:16	RO	0x00	ro_osd_st_luma50 Luminance statistics for the OSD block 50
15:8	RO	0x00	ro_osd_st_luma49 Luminance statistics for the OSD block 49
7:0	RO	0x00	ro_osd_st_luma48 Luminance statistics for the OSD block 48

RGA2_OSD_ST_LUMA13

Address: Operational Base(0xFF440000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma55 Luminance statistics for the OSD block 55
23:16	RO	0x00	ro_osd_st_luma54 Luminance statistics for the OSD block 54
15:8	RO	0x00	ro_osd_st_luma53 Luminance statistics for the OSD block 53
7:0	RO	0x00	ro_osd_st_luma52 Luminance statistics for the OSD block 52

RGA2_OSD_ST_LUMA14

Address: Operational Base(0xFF440000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma59 Luminance statistics for the OSD block 59
23:16	RO	0x00	ro_osd_st_luma58 Luminance statistics for the OSD block 58
15:8	RO	0x00	ro_osd_st_luma57 Luminance statistics for the OSD block 57
7:0	RO	0x00	ro_osd_st_luma56 Luminance statistics for the OSD block 56

RGA2_OSD_ST_LUMA15

Address: Operational Base(0xFF440000) + offset (0x043C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma63 Luminance statistics for the OSD block 63
23:16	RO	0x00	ro_osd_st_luma62 Luminance statistics for the OSD block 62
15:8	RO	0x00	ro_osd_st_luma61 Luminance statistics for the OSD block 61
7:0	RO	0x00	ro_osd_st_luma60 Luminance statistics for the OSD block 60

RGA2_DTE_ADDR

Address: Operational Base(0xFF440000) + offset (0x0F00)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page Table address

RGA2_STATUS

Address: Operational Base(0xFF440000) + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	page_fault_bus_id Index of master reponsible for last page fault.
5	RO	0x0	page_fault_is_write The direction of access for last page fault 1'b0: Read 1'b1: Write
4	RO	0x0	replay_buffer_empty The MMU replay buffer is empty
3	RO	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses
2	RO	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command
0	RO	0x0	paging_enabled Paging is enabled

RGA2_COMMAND

Address: Operational Base(0xFF440000) + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	mmu_cmd MMU_CMD. This can be 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

RGA2_PAGE_FAULT_ADDR

Address: Operational Base(0xFF440000) + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	page_fault_addr Address of last page fault.

RGA2_ZAP_ONE_LINE

Address: Operational Base(0xFF440000) + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

RGA2_INT_RAWSTAT

Address: Operational Base(0xFF440000) + offset (0x0F14)

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Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

RGA2_INT_CLEAR

Address: Operational Base(0xFF440000) + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	read_bus_error Read bus error
0	WO	0x0	page_fault Page fault

RGA2_INT_MASK

Address: Operational Base(0xFF440000) + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

RGA2_INT_STATUS

Address: Operational Base(0xFF440000) + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	read_bus_error Read bus error
0	RO	0x0	page_fault Page fault

RGA2_AUTO_GATING

Address: Operational Base(0xFF440000) + offset (0x0F24)

Bit	Attr	Reset Value	Description
31	RW	0x1	sw_mmu_old_en mmu old version enable, need set 1.
30:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self.

4.5 Application Notes

4.5.1 Register Partition

There are two types of register in RGA. The first part registers (0x0 - 0xFC) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

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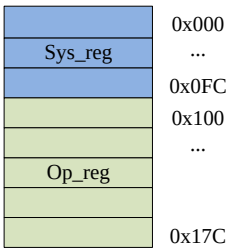

Fig. 4-9 RGA2 software main register-region

4.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In salve mode (RGA_SYS_CTRL[1] = 1'b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA_SYS_CTRL[0] to 1. In master mode (RGA_SYS_CTRL[1] = 1'b1), 2D graphic commands could be run sequentially. After setting command's number to RGA_CMD_CTRL[12:3], writing 1 to RGA_CMD_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.

Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA_CMD_ADDR) and command number (RGA_CMD_CTRL[12:3]) should be set, then write 1 to cmd_line_st (RGA_CMD_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd_incr_num (RGA_CMD_CTRL[12:3]) and cmd_incr_valid (RGA_CMD_CTRL[1]=1'b1).

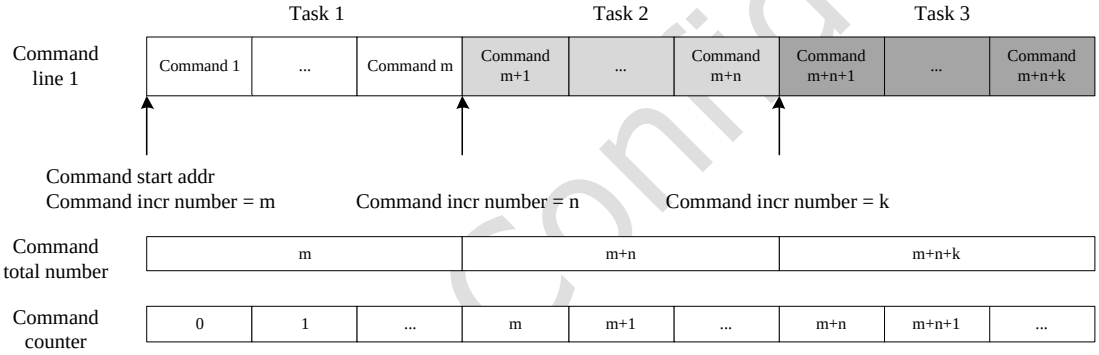

Fig. 4-10 RGA2 command line and command counter

4.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.

In master command mode, user can enable the current_cmd_int (sw_intr_cf), command by command to generate a interrupt at the end point of target command operation.

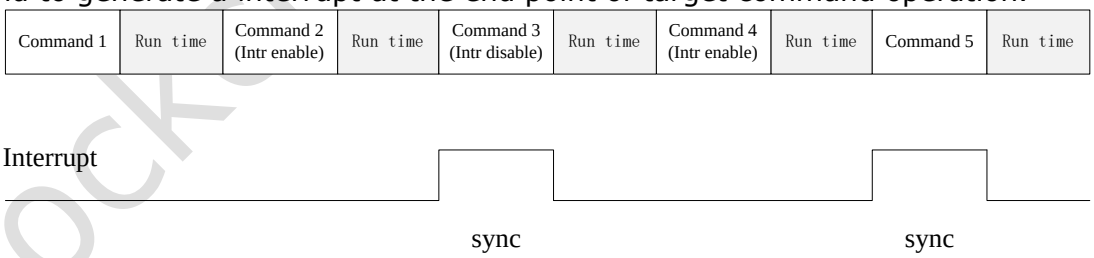

Fig. 4-11 RGA2 command sync generation

4.5.4 Color Palette Application Notes

1. Palette/LUT Load into special RAM in ELS_BUF_CTRL.
2. Color Palette/Pattern interval operations no need to initial LUT/pattern ram if LUT/pattern content no update.

4.5.5 OSD Automatic Inversion Application Notes

1. In horizontal mode, the width must be greater than or equal to the height, and vice versa.
2. Supports up to 64 OSD blocks, and the width of each OSD ranges from 8 to 2048, so that the size of the OSD area supports up to 4096.
3. The format of SRC0 and the format of DST need to be equal.
4. SRC0 sources format support in YUV422 P/SP, YUV420 P/SP.
5. In OSD width variable mode, the maximum supported width is 512.

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6. OSD inverse flags can be configured externally or read from internal storage, and the internal storage supports a maximum of 1024 flags.
7. OSD sources in ARGB2BPP format virtual stride need 32pixel(64bits) align.
8. At least one of the sw_auto_rst or sw_auto_ckg register needs to be closed when using OSD unfix width function.

4.5.6 Some Special Application Constraints

1. The algorithm of vertical scale up: must select BI-cubic algorithm when source picture is smaller or equal to 2k and must select BI-linear when bigger than 2k.
2. The effects that The output's definition is near 2k or 4k may not very well when at the scenario that the vertical side is scale up and the horizontal is scale down within range of 2%(such as:2048x32, 2008x64).
3. At the scenario A+B->C(A means SRC0, B means DST, C means SRC1), the size among the A B C has some constraints:
A's size after scale must be equal to C. C's size must equal to B when A+C is no rotation.
C's rotation (90degree) size must equal to B1 when A+C is rotation 90 degree.

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Chapter 5 USB2.0 Host

5.1 Overview

USB2.0 host controller supports fully USB2.0 functions with one EHCI host controller and one OHCI host controller, and each host controller has one USB port. OHCI host controller only supports full-speed and low-speed mode and is used for full-speed devices and low-speed devices. EHCI only supports high-speed mode and is used for high-speed devices. OHCI host controller and EHCI host controller shares the same USB port, EHCI host controller will auto select the owner (OHCI or EHCI) of this USB port depending on the speed mode of attached devices, when selecting OHCI as owner, OHCI host controller will serve for the attached device; when selecting EHCI as owner, EHCI host controller will serve for the attached device.

USB2.0 Host Controller supports the following features:

- Compatible Specifications
  - Universal Serial Bus Specification, Revision 2.0
  - Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Open Host Controller Interface Specification (OHCI), Revision 1.0a
- Support High-speed (480Mbps), Full-speed (12Mbps) and Low-speed (1.5Mbps)

5.2 Block Diagram

USB2.0 Host Controller is comprised of:

- EHCI Host Controller: Perform High-speed transactions
- OHCI Host Controller: Perform full/low-speed transactions
- Port Routing Control: Select EHCI Host Controller or OHCI Host Controller

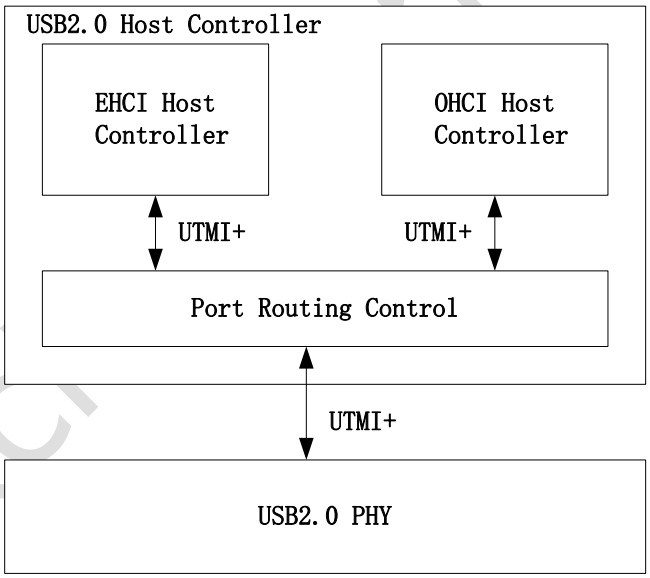

Fig. 5-1USB2.0 Host Controller Block Diagram

5.3 Function Description

5.3.1 EHCI Host Controller

It performs descriptors and data read or write from or to system memory and packs or un-pack USB transactions from or to UTMI+ interface defined in EHCI specification for high-speed data transmission.

5.3.2 OHCI Host Controller

It performs descriptors and data read/write from/to system memory and packs or un-pack USB transactions from or to UTMI+ interface defined in OHCI specification for full-speed or low-speed data transmission.

5.3.3 Port Routing Control

As part of logic in the EHCI host controller, it is used to auto-select EHCI or OHCI host

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controller to serve the attached device depending on the speed of the attached device.

5.4 Register Description

5.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 5-1USB2.0 Host Controller Address Mapping

Base Address[18]	Device	Address Length	Offset Address Range
1'b0	EHCI	256K BYTE	0xfed00000 ~ 0xfed3ffff
1'b1	OHCI	256K BYTE	0xfed40000 ~ 0xfed7ffff

EHCI and OHCI register definitions, please refer to Enhanced Host Controller Interface Specification (EHCI), Revision 1.0 and Open Host Controller Interface Specification (OHCI), Revision 1.0a.

5.5 Interface Description

Table 5-2 USB2.0 PHY Interface Description

Module Pin	Direction	Pad Name	Descriptions
USB1PN	I/O	USB20_HOST1_DM	USB2.0 PHY Host Port PN
USB1PP	I/O	USB20_HOST1_DP	USB2.0 PHY Host Port PP

5.6 Application Notes

5.6.1 Program flow

Please refer to Enhanced Host Controller Interface Specification (EHCI), Revision 1.0 and Open Host Controller Interface Specification (OHCI), Revision 1.0a.

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Chapter 6 USB3 Controller

6.1 Overview

USB3 sub-system include USB3.0 controller and some PHYs. The USB3.0 controller (marked as USB3OTG) can act as static host, static device, USB2.0/3.0 OTG A device or B device basing on the status of input ID from USB2.0 PHY. The controller respectively connect to one USB3.0 PHY and one USB2.0 PHY and can perform data transmission between host and device as host or device for Super-Speed/High-Speed/Full-Speed/Low-Speed.
USB3.0 sub-system supports the following features:

- General Features
  - Compatible Specification
    - Universal Serial Bus 3.0 Specification, Revision 1.0
    - Universal Serial Bus Specification, Revision 2.0
    - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  - Simultaneous IN and OUT transfer for USB3.0, up to 8Gbps bandwidth
  - Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
  - LPM protocol in USB 2.0 and U0, U1, U2, and U3 states for USB 3.0
  - Dynamic FIFO memory allocation for endpoints
  - Keep-Alive feature in LS mode and (micro-)SOFs in HS/FS modes
  - Low MIPS requirement
    - Driver involved only in setting up transfers and high-level error recovery
    - Hardware handles data packing and routing to a specific pipe
- Application Interface Features
  - AHB Slave interface
  - AXI Master interface
    - Programmable burst lengths up to 16
    - Handle fixed burst address alignment
    - Programmable number of outstanding read/write requests up to 16
    - Concurrent read/write to get best performance of USB3.0 duplex operation
- USB3.0 Device Features
  - Up to 10 IN endpoints, including control endpoint 0
  - Up to 6 OUT endpoints, including control endpoint 0
  - Up to 16 endpoint transfer resources, each one for each endpoint
  - Flexible endpoint configuration for multiple applications/USB set-configuration modes
  - Hardware handles ERDY and burst
  - Stream-based bulk endpoints with controller automatically initiating data movement
  - Isochronous endpoints with isochronous data in data buffers
  - Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- USB Class-Specific Device Features
  - Stream support for UASP application
  - Gathering of scattered packet to support Ethernet Over USB
  - Scheduling of multiple Ethernet packets without interrupt
  - Variable FIFO buffer allocation for each endpoint
  - For isochronous applications, scheduling of variable-length payloads for each microframe
  - Microframe precise scheduling for isochronous applications
  - Configurable endpoint type selection and dynamic FIFO allocation to facilitate multi-function/composite device implementation. During set-config or alternate-setting, device resources are reconfigured to meet the configuration or alternate setting requirements.
- USB 3.0 xHCI Host Features

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- Support up to 64 devices
- Support 1 interrupter
- Support 1 USB2.0 port and 1 Super-Speed port
- Support standard or open-source xHCI and class driver

- USB 3.0 Dual-Role Device (DRD) Features
  - Static Device Operation
  - Static Host Operation
  - USB3.0/USB2.0 OTG A device and B device basing on ID
  - Not Support USB3.0/USB2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)
- Miscellaneous Features
  - USB2.0 PHY support Battery Charge detection
  - USB3.0 PHY combos with PCIE

6.2 Block Diagram

USB3 is comprised of:

- Bus Interface: Register Interface/Data and Descriptors DMA management
- SS/HS/FS/LS MAC: USB part logic
- USB2.0 PHY: UTMI+ interface USB2.0 PHY
- USB3.0 PHY: USB3.0 and PCIE combo

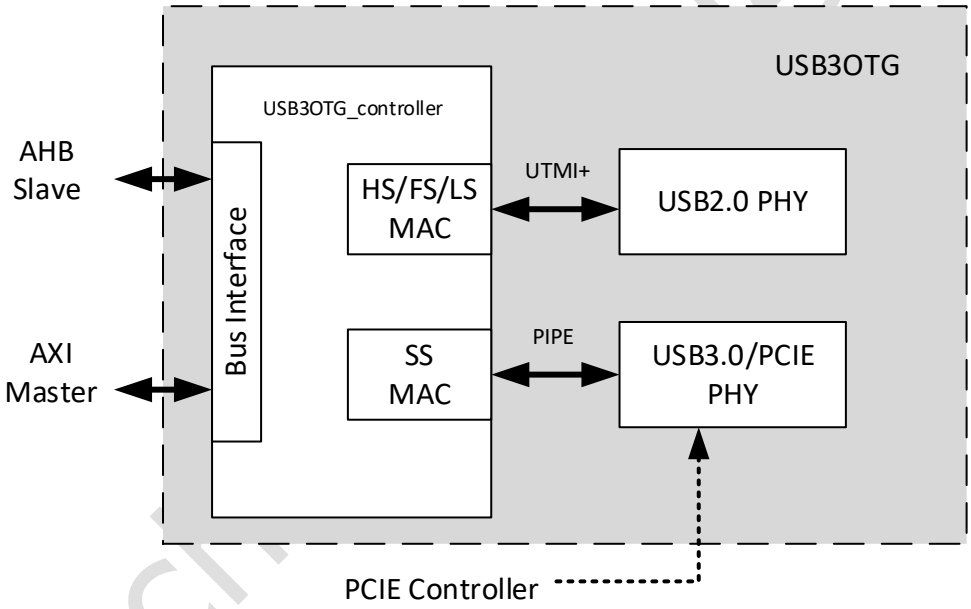

Fig. 6-1 USB3 Block Diagram

6.3 Function Description

USB3OTG can act as static xHCI host controller, static device controller, USB3.0/2.0 OTG A device or B device basing on ID of USB2.0 PHY. As device controller, it can work on either USB2.0 speed or Super-Speed basing on speed of host attached to, and process USB transactions described in the descriptors (read back from external memory by AXI master) to/from UTMI+ interface and Pipe Interface of USB3/ PCIE combo PHY.
As host controller, it can work on USB2.0 speed, Super-Speed or both basing on speed or type of attached device, and process USB transactions described in the descriptors (read back from external memory by AXI master) to/from UTMI+ interface and Pipe Interface of USB3/ PCIE combo PHY.

6.4 Register Description

6.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 6-1 USB3 Address Mapping

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USB3.0 Controller Address Mapping	
Offset Address Range	**Register Type**
0x00000 ~ 0x07FFF	xHCI Registers, see xHCI spec.
0x0C100 ~ 0x0C6FF	Global Registers
0x0C700 ~ 0x0CBFF	Device Controller Registers
0x0CC00 ~ 0x0CFFF	Unused/Reserved
0x40000 ~ 0x7FFFF	Internal RAM0 – Debug Access (256KB)
0x80000 ~ 0xBFFFF	Internal RAM1 – Debug Access (256KB)
0xC0000 ~ 0xFFFFF	Internal RAM2 – Debug Access (256KB)

6.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
USB3OTG_GSBUSCFG0	0xC100	W	0x00000001	Global SoC Bus Configuration Register 0
USB3OTG_GSBUSCFG1	0xC104	W	0x00000300	Global SoC Bus Configuration Register 1
USB3OTG_GTXTHRCFG	0xC108	W	0x00000000	Global Tx Threshold Control Register
USB3OTG_GRXTHRCFG	0xC10C	W	0x00000000	Global Rx Threshold Control Register
USB3OTG_GCTL	0xC110	W	0x13512004	Global Core Control Register
USB3OTG_GSTS	0xC118	W	0x7E800000	Global Status Register
USB3OTG_GUCTL1	0xC11C	W	0x0004018A	Global User Control Register 1
USB3OTG_GSNPSID	0xC120	W	0x5533300A	Global SNPS ID Register
USB3OTG_GGPIO	0xC124	W	0x00000000	Global General Purpose Input/Output Register
USB3OTG_GUID	0xC128	W	0x20190520	Global User ID Register
USB3OTG_GUCTL	0xC12C	W	0x02008010	Global User Control Register
USB3OTG_GBUSERRADDRLO	0xC130	W	0x00000000	Global SoC Bus Error Address Register - Low
USB3OTG_GBUSERRADDRHI	0xC134	W	0x00000000	Global SoC Bus Error Address Register - High
USB3OTG_GPRTBIMAPLO	0xC138	W	0x00000000	Global SS Port to Bus Instance Mapping Register
USB3OTG_GHWPARAMS0	0xC140	W	0x2020400A	Global Hardware Parameters Register 0
USB3OTG_GHWPARAMS1	0xC144	W	0x0120C93B	Global Hardware Parameters Register 1
USB3OTG_GHWPARAMS2	0xC148	W	0x20190520	Global Hardware Parameters Register 2
USB3OTG_GHWPARAMS3	0xC14C	W	0x069CD084	Global Hardware Parameters Register 3
USB3OTG_GHWPARAMS4	0xC150	W	0x47822010	Global Hardware Parameters Register 4
USB3OTG_GHWPARAMS5	0xC154	W	0x04204018	Global Hardware Parameters Register 5
USB3OTG_GHWPARAMS6	0xC158	W	0x09D78020	Global Hardware Parameters Register 6
USB3OTG_GHWPARAMS7	0xC15C	W	0x00000000	Global Hardware Parameters Register 7
USB3OTG_GDBGFIFOSPACE	0xC160	W	0x000A0000	Global Debug Queue/FIFO Space Available Register
USB3OTG_GDBGLNMCC	0xC168	W	0x00000000	Global Debug LNMCC Register
USB3OTG_GDBGBMU	0xC16C	W	0x00000000	Global Debug BMU Register

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Name	Offset	Size	Reset Value	Description
USB3OTG_GDBGLSPMUX	0xC170	W	0x003F0000	Global Debug LSP MUX Register - Device
USB3OTG_GDBGLSP	0xC174	W	0x00000000	Global Debug LSP Register
USB3OTG_GDBGEPINFO0	0xC178	W	0x00000000	Global Debug Endpoint Information Register 0
USB3OTG_GDBGEPINFO1	0xC17C	W	0x00800000	Global Debug Endpoint Information Register 1
USB3OTG_GPRTBIMAP_HSLO	0xC180	W	0x00000000	Global High-Speed Port to Bus Instance Mapping Register - Low
USB3OTG_GPRTBIMAP_FSLO	0xC188	W	0x00000000	Global Full-Speed Port to Bus Instance Mapping Register - Low
USB3OTG_GUSB2PHYCFG0	0xC200	W	0x40102400	Global USB2 PHY Configuration Register 0
USB3OTG_GUSB3PIPECTL0	0xC2C0	W	0x00000000	Global PIPE PHY Configuration Register 0
USB3OTG_GTXFIFOSIZn	0xC300	W	0x00000042	Global Transmit FIFO Size Register n, offset (0xc300 + 4*n), n=0~6
USB3OTG_GRXFIFOSIZn	0xC380	W	0x03340185	Global Receive FIFO Size Register n,
USB3OTG_GEVNTADRLO0	0xC400	W	0x00000000	Global Event Buffer Address (Low) Register 0
USB3OTG_GEVNTADRHI0	0xC404	W	0x00000000	Global Event Buffer Address (High) Register 0
USB3OTG_GEVNTSIZ0	0xC408	W	0x00000000	Global Event Buffer Size Register 0
USB3OTG_GEVNTCOUNT0	0xC40C	W	0x00000000	Global Event Buffer Count Register 0
USB3OTG_GHWPARAMS8	0xC600	W	0x0000047C	Global Hardware Parameters Register 8
USB3OTG_GTXFIFOPRIDEV	0xC610	W	0x00000000	Global Device TX FIFO DMA Priority Register
USB3OTG_GTXFIFOPRIHST	0xC618	W	0x00000000	Global Host TX FIFO DMA Priority Register
USB3OTG_GRXFIFOPRIHST	0xC61C	W	0x00000000	Global Host RX FIFO DMA Priority Register
USB3OTG_GFIFOPRIDBC	0xC620	W	0x00000000	Global Host Debug Capability DMA Priority Register
USB3OTG_GDMAHLRATIO	0xC624	W	0x00000000	Global Host FIFO DMA High-Low Priority Ratio Register
USB3OTG_GFLADJ	0xC630	W	0x00000000	Global Frame Length Adjustment Register
USB3OTG_DCFG	0xC700	W	0x00080000	Device Configuration Register
USB3OTG_DCTL	0xC704	W	0x00F00000	Device Control Register
USB3OTG_DEVTEN	0xC708	W	0x00000000	Device Event Enable Register
USB3OTG_DSTS	0xC70C	W	0x00520000	Device Status Register
USB3OTG_DGCMDPAR	0xC710	W	0x00000000	Device Generic Command Parameter Register
USB3OTG_DGCMD	0xC714	W	0x00000000	Device Generic Command Register
USB3OTG_DALEPENA	0xC720	W	0x00000000	Device Active USB Endpoint Enable Register
USB3OTG_DEPnCMDPAR2	0xC800	W	0x00000000	Device Physical Endpoint-n Command Parameter 2 Register, offset (0xc800 + 4*n), n=0~12

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Name	Offset	Size	Reset Value	Description
USB3OTG_DEPnCMDPAR1	0xC804	W	0x00000000	Device Physical Endpoint-n Command Parameter 1 Register, offset (0xc804 + 4*n), n=0~12
USB3OTG_DEPnCMDPAR0	0xC808	W	0x00000000	Device Physical Endpoint-n Command Parameter 0 Register, offset (0xc808 + 4*n), n=0~12
USB3OTG_DEPnCMD	0xC80C	W	0x00000000	Device Physical Endpoint-n Command Register, offset (0xc80c + 4*n), n=0~12

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

6.4.3 Detail Registers Description

USB3OTG_GSBUSCFG0

Address: Operational Base(0xFE500000) + offset (0xC100)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	datrdreqinfo AXI-cache for Data Read (DatRdReqInfo).
27:24	RW	0x0	desrdreqinfo AXI-cache for Descriptor Read (DesRdReqInfo).
23:20	RW	0x0	datwrreqinfo AXI-cache for Data Write (DatWrReqInfo).
19:16	RW	0x0	deswrreqinfo AXI-cache for Descriptor Write (DesWrReqInfo).
15:12	RO	0x0	reserved
11	RW	0x0	datbigend This bit controls the endian mode for data accesses. 1'b0: Little-endian (default) 1'b1: Big-endian
10	RW	0x0	desbigend This bit controls the endian mode for descriptor accesses. 1'b0: Little-endian (default) 1'b1: Big-endian
9:8	RO	0x0	reserved
7	RW	0x0	incr256brstena If software set this bit to 1, the AXI master uses INCR to do the 256-beat burst.
6	RW	0x0	incr128brstena If software set this bit to 1, the AXI master uses INCR to do the 128-beat burst.
5	RW	0x0	incr64brstena If software set this bit to 1, AXI master uses INCR to do the 64-beat burst.
4	RW	0x0	incr32brstena If software set this bit to 1, the AXI master uses INCR to do the 32-beat burst.
3	RW	0x0	incr16brstena If software set this bit to 1, the AXI master uses INCR to do the 16-beat burst.
2	RW	0x0	incr8brstena If software set this bit to 1, the AXI master uses INCR to do the 8-beat burst.

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Bit	Attr	Reset Value	Description
1	RW	0x0	incr4brstena When this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers.
0	RW	0x1	incrbrstena This bit determines the set of burst lengths the master interface uses. It works in conjunction with the GSBUSCFG0[7:1] enables(INCR256/128/64/32/16/8/4). 0: INCRX burst mode ARLEN/AWLEN do not use INCR. They use only the following burst lengths: 4 (if GSBUSCFG0.INCR4BrstEna = 1); 8 (if GSBUSCFG0.INCR8BrstEna = 1); 16 (if GSBUSCFG0.INCR16BrstEna = 1); 32 (if GSBUSCFG0.INCR32BrstEna = 1); 64 (if GSBUSCFG0.INCR64BrstEna = 1); 128 (if GSBUSCFG0.INCR128BrstEna = 1); 256 (if GSBUSCFG0.INCR256BrstEna = 1); 1: INCR (undefined length) burst mode; ARLEN/AWLEN uses any length less than or equal to the largest-enabled burst length of INCR4/8/16/32/64/128/256. For cache line-aligned applications, this bit is typically set to 0 to ensure that the master interface uses only power-of-2 burst lengths (as enabled via GSBUSCFG0[7:0]).

USB3OTG_GSBUSCFG1

Address: Operational Base(0xFE500000) + offset (0xC104)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	en1kpage 1K Page Boundary Enable. By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	RW	0x3	pipe_trans_limit AXI Pipelined Transfers Burst Request Limit. The field controls the number of outstanding pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 4'h0: 1 request 4'h1: 2 requests 4'h2: 3 requests 4'h3: 4 requests ... 4'hF: 16 requests
7:0	RO	0x00	reserved

USB3OTG_GTXTHRCFG

Address: Operational Base(0xFE500000) + offset (0xC108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RO	0x0	USBTxPktCntSel This field enables/disables the USB transmission multi-packet thresholding: 1'b0: USB transmission multi-packet thresholding is disabled; the core can only start transmission on the USB after the entire packet has been fetched into the corresponding TXFIFO. 1'b1: USB transmission multi-packet thresholding is enabled. The core can only start transmission on the USB after USB Transmit Packet Count amounts of packets for the USB transaction (burst) are already in the corresponding TXFIFO. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	RO	0x0	reserved
27:24	RW	0x0	USBTxPktCnt This field specifies the number of packets that must be in the TXFIFO before the core can start transmission for the corresponding USB transaction (burst). This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15. Note: This field must be less than or equal to the USB Maximum TX Burst Size field.
23:16	RW	0x00	USBMaxTxBurstSize USB Maximum TX Burst Size When USBTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the core can do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. You can program a smaller value to this field to limit the TX burst size that the core can execute. Host mode: It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints. Device mode: This value is not used in device mode, but users need to program a value when using the TX threshold feature to make sure that the value programmed in USBTxPktCnt is less than this value. Valid values are from 1 to 16.
15:0	RO	0x0000	reserved

USB3OTG_GRXTHRCFG

Address: Operational Base(0xFE500000) + offset (0xC10C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	usb_rx_pkt_cntsel USB ReceivePacket Count Enable. This field enables/disables the USB reception multi-packet thresholding: 1'b0: The core can only start reception on the USB when the RX FIFO has space for at least one packet. 1'b1: Not applied. If you are using external buffer control (EBC) feature, disable this mode by setting USBRxPktCntSel to 0.
28:13	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	resvl_socout_spc Space reserved in rx fifo for ISOC OUT. In host mode, this field is not applicable and must be programmed to 0. In device mode, this value represents the amount of space to be reserved for ISOC OUT packets. The value to be programmed should be chosen so as to ensure that non ISOC packets are not completely dropped, If no space needs to be reserved for ISOC OUT packets, program this field to 0. This field is valid only in device mode. The maximum configurable depth of rx fifo is 8192. Therefore, this field is 13 bits wide. For HS/FS, the space reservation is the actual value.

USB3OTG_GCTL

Address: Operational Base(0xFE500000) + offset (0xC110)

Bit	Attr	Reset Value	Description
31:19	RW	0x026a	pwrdnscale Not applied.
18	RW	0x0	masterfiltbypass Master Filter Bypass When this bit is set to 1'b1, all the filters are bypassed. The double synchronizers to mac_clk preceding the filters are also bypassed. For enabling the filters, this bit must be 1'b0.
17	RW	0x0	bypassetaddr Bypass SetAddress in Device Mode. When BYPSSETADDR bit is set, the device core uses the value in the DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, you can use this feature to avoid sending an actual SET ADDRESS control transfer on the USB, and make the device core respond to a new address. Note: You can set this bit for simulation purposes only. In the actual hardware, this bit must be set to 1'b0.
16	RW	0x1	u2rstecn Device controller on USB 2.0 reset checks for receiver termination eight times per attempt if this bit is set to zero, or only once per attempt if the bit is set to one. Note: This bit is applicable only in device mode.
15:14	RW	0x0	frmscldwn This field scales down device view of a SOF/USOF duration. For HS mode: Value of 2'h3 implements interval to be 15.625 us Value of 2'h2 implements interval to be 31.25 us Value of 2'h1 implements interval to be 62.5 us Value of 2'h0 implements interval to be 125us For FS mode, the scale-down value is multiplied by 8. This field also scales down the MaxPacketSize of the IN and OUT bulk endpoint to allow more traffic during simulation. It can only be changed from a non-zero value during simulation. 2'h0: 1024 bytes 2'h1: 512 bytes 2'h2: 256 bytes 2'h3: 128 bytes

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Bit	Attr	Reset Value	Description
13:12	RW	0x2	prtcapdir PRTCAPDIR: Port Capability Direction (PrtCapDir) 2'b01: for Host configurations 2'b10: for Device configurations SW should base on IDDIG input to set usb controller as an OTG 2.0 device with A-device or B-device.
11	RW	0x0	coresoftreset Core Soft Reset (CoreSoftReset) 1'b0: No soft reset; 1'b1: Soft reset to core Clears the interrupts and all the CSRs except the following registers: GCTL; GUCTL; GSTS; GSNPSID; GGPIO; GUID; GUSB2PHYCFGn registers; GUSB3PIPECTLn registers; DCFG; DCTL; DEVTEN; DSTS.
10	RW	0x0	sofitpsync Not applied.
9	RW	0x0	u1u2_timescale Not applied.
8	RW	0x0	debugattach Debug Attach. Not applied.
7:6	RW	0x0	ramclksel RAM Clock Select (RAMClkSel) 2'b00: bus clock 2'b01: pipe clock (Only used in device mode) 2'b10: In device mode, pipe/2 clock. In Host mode, controller switches ram_clk between pipe/2 clock, mac2_clk and bus_clk based on the status of the U2 ports 2'b11: In device mode, selects mac2_clk as ram_clk (when 8-bit UTMI or ULPI used. Not supported in 16-bit UTMI mode); In Host mode, controller switches ram_clk between pipe_clk, mac2_clk and bus_clk based on the status of the U2 ports. In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00.
5:4	RW	0x0	scaledown Scale-Down Mode (ScaleDown) When Scale-Down mode is enabled for simulation, the core uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes: 2'b00: Disables all scale-downs. Actual timing values are used. 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include Speed enumeration, HNP/SRP, and Host mode suspend and resume 2'b10: Enables scale-down of Device mode suspend and resume timing values only. 2'b11: Enables bit 0 and bit 1 scale-down timing values.
3	RW	0x0	disscramble Disable Scrambling (DisScramble) Transmit request to Link Partner on next transition to Recovery or Polling.

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Bit	Attr	Reset Value	Description
2	RW	0x1	u2exit_lfps If this bit is: 1'b0: the link treats 248ns LFPS as a valid U2 exit. 1'b1: the link waits for 8us of LFPS before it detects a valid U2 exit. This bit is added to improve interoperability with a third part host controller. This host controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the device can stay in U2 while ignoring this glitch from the host controller.
1	RO	0x0	gbl_hibernation_en This bit enables hibernation at the global level. If hibernation is not enabled through this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	RW	0x0	dsblclkgtng Disable Clock Gating. This bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset.

USB3OTG_GSTS

Address: Operational Base(0xFE500000) + offset (0xC118)

Bit	Attr	Reset Value	Description
31:20	RO	0x7e8	cbelt Current BELT Value. In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
19:12	RO	0x00	reserved
11	RO	0x0	SSIC_IP Not applied.
10	RO	0x0	OTG_IP OTG Interrupt Pending. This field indicates that there is a pending interrupt pertaining to OTG in OEVT register.
9	RO	0x0	bc_ip Battery Charger Interrupt Pending This field indicates that there is a pending interrupt pertaining to BC in BCEVT register.
8	RO	0x0	adp_ip ADP Interrupt Pending. This field indicates that there is a pending interrupt pertaining to ADP in ADPEVT register.
7	RO	0x0	host_ip Host Interrupt Pending. This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.
6	RO	0x0	device_ip Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.

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Bit	Attr	Reset Value	Description
5	W1C	0x0	csr_timeout When this bit is 1'b1, it indicates that the software performed a write or read to a core register that could not be completed within DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles (default: h1FFFF).
4	W1C	0x0	buserraddrvld us Error Address Valid Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	RO	0x0	reserved
1:0	RO	0x0	curmod Current Mode of Operation.

USB3OTG_GUCTL1

Address: Operational Base(0xFE500000) + offset (0xC11C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	filter_se0_fsls_eop 1'b0: Default behaviour, no change in Linestate check for SE0 detection in FS/LS. 1'b1: Feature enabled, FS/LS SE0 is filtered for 2 clocks for detecting EOP. This bit is applicable for FS/LS operation. If this feature is enabled, then SE0 on the Linestate is validated for 2 consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode: FS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM handshake, the core will ignore single SE0 glitch on the Linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS. Host mode: FS/LS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the core will ignore single SE0 glitch on the Linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if the Linestate has SE0 glitches during transmission. This bit is quasi-static, i.e., should not be changed during device operation.

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Bit	Attr	Reset Value	Description
28	RW	0x0	tx_ipgap_linecheck_dis 1'b0: Default behavior, no change in Linestate check. 1'b1: Feature enable, 2.0 MAC disables Linestate check during HS transmit. This bit is applicable for HS operation of u2mac. If this feature is enabled, then the 2.0 mac operating in HS ignores the UTMI/ULPI Linestate during the transmit of a token (during token-to-token and token-to-data IPGAP). When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the Linestate during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then for device LPM handshake, the core will ignore the Linestate after TX and wait for a fixed clock (40 bit times equivalent) after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap between (tkn to tkn/data) is added by 40 bit times of TXENDDELAY, and linestate is ignored during this 40 bit times delay. Enable this bit if the LineState will not reflect the expected line state (J) during transmission. This bit is quasi-static, i.e., should not be changed during device operation.
27	RW	0x0	dev_trb_out_spr_ind 1'b0: Default behavior, no change in TRB status dword. 1'b1: Feature enable, OUT TRB status indicates Short Packet. This bit is applicable for device mode only (and ignored in host mode). If the device application (SW/HW) wants to know if a short packet was received for an OUT in the TRB status itself, then this feature can be enabled, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the trbstatus, RSVD, SPR,PCM1, bufsize dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, i.e., should not be changed during device operation.
26	RW	0x0	dve_force_20clk_for_30clk Not applied.
25	RW	0x0	p3_in_u2 Not applied.

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Bit	Attr	Reset Value	Description
24	RW	0x0	dev_l1_exit_by_hw 1'b0: Default behavior, disables device L1 hardware exit logic. 1'b1: Feature enabled This bit is applicable for device mode (2.0) only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wkp signaling to resume after going into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This HW remote wake feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control When control transfers are in progress, the LPM will be rejected (NYET response). Only after control transfers are completed (either with ACK/STALL), LPM will be accepted For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote-wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests thru L1. This bit is quasi-static, i.e., should not be changed during device operation.
23:21	RW	0x0	ip_gap_add_on This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC.
20	RW	0x0	dev_lsp_tail_lock_dis 1'b0: Default behaviour, enables device lsp lock logic for tail TRB update. 1'b1: Fix disabled This is a bug fix for STAR 9000716195 that affects the CSP mode for OUT endpoints in device mode. The issue is that tail TRB index is not synchronized with the cache Scratchpad bytecount update. If the fast-forward request comes in-between the bytecount update on a newly fetched TRB and the tail-index write update in TPF, the RDP works on an incorrect tail index and misses the byte count decrement for the newly fetched TRB in the fast-forwarding process. This fix needs to be present all the times.
19	RW	0x0	nak_per_enh_fs 1'b1: Enables performance enhancement for FS async endpoints in the presence of NAKs. 1'b0: Enhancement not applied. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other Full Speed bulk endpoint which is ACKed by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your FullSpeed application. Setting this bit will only control, and is only required for Full Speed transfers.

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Bit	Attr	Reset Value	Description
18	RW	0x1	nak_per_enh_hs 1'b1: Enables performance enhancement for HS async endpoints in the presence of NAKs. 1'b0: Enhancement not applied. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other High Speed bulk endpoint which is ACKed by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your HighSpeed application. Setting this bit will only control, and is only required for High Speed transfers.
17	RW	0x0	parkmode_disbale_ss Not applied.
16	RW	0x0	parkmode_disable_hs This bit is used only in host mode. When this bit is set to 1 all HS bus instances park mode are disabled. To improve performance in park mode, the xHCI scheduler queues in three requests of 4 packets each for High Speed asynchronous endpoints in a micro-frame. But if a device is slow and if it NAKs more than 3 times, then it is rescheduled only in the next micro-frame. This could decrease the performance of a slow device even further. In a few High Speed devices (such as Sandisk Cruzer Blade 4GB VID: 1921, PID: 21863 and Flex Drive VID: 3744, PID: 8552) when an IN request is sent within 900ns of the ACK of the previous packet, these devices send a NAK. When connected to these devices, if required, the software can disable the park mode if you see performance drop in your system. When park mode is disabled, pipelining of multiple packet is disabled and instead one packet at a time is requested by the scheduler. This allows up to 12 NAKs in a micro-frame and improves performance of these slow devices.
15	RW	0x0	parkmod_disavale_fsls This bit is used only in host mode, and is for debug purpose only. When this bit is set to 1 all FS/LS bus instances in park mode disabled.
14:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x1	l1_susp_thrld_en_for_host This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals (see LPM Interface Signals table in the Databook) as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: The HIRD/BESL value used is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: The HIRD/BESL value used is less than the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0.
7:4	RW	0x8	l1_susp_thrld_for_host This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit.
3	RW	0x1	hc_errata_enable Not applied.
2	RW	0x0	hc_parchk_disable Host Parameter Check Disable. When this bit is set to 0 (by default), the xHC checks that the input slot/EP context fields comply to the xHCI Specification. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating PARAMETER ERROR. When the bit is set to 1, the xHC does not perform parameter checks and does not generate PARAMETER ERROR completion code.
1	RW	0x1	ovrld_l1_susp_com If this bit is set, the utmi_l1_suspend_com_n is overloaded with the utmi_sleep_n signal. This bit is usually set if the PHY stops the port clock during L1 sleep condition.
0	RW	0x0	loa_filter_en If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables. Note: This bit is valid only in host mode.

USB3OTG_GSNPSID

Address: Operational Base(0xFE500000) + offset (0xC120)

Bit	Attr	Reset Value	Description
31:0	RO	0x5533300a	snpsid SNPSID[31:16] indicates Core Identification Number. 0x5533 is ASCII for U3 (DWC_usb3). SNPSID[15:0] indicates the release number. Current Release is 3.00a. Software uses this register to configure release-specific features in the driver.

USB3OTG_GGPIO

Address: Operational Base(0xFE500000) + offset (0xC124)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	gpo General Purpose Output This field's value is driven out on the gp_out[15:0] core output port.
15:0	RO	0x0000	gpi General Purpose Input This field's read value reflects the gp_in[15:0] core input value.

USB3OTG_GUID

Address: Operational Base(0xFE500000) + offset (0xC128)

Bit	Attr	Reset Value	Description
31:0	RW	0x20190520	userid Application-programmable ID field.

USB3OTG_GUCTL

Address: Operational Base(0xFE500000) + offset (0xC12C)

Bit	Attr	Reset Value	Description
31:22	RW	0x008	refclkper This field indicates in terms of nano seconds the period of ref_clk. The default value of this register is set to 'h8 (8ns/125 MHz). This field needs to be updated during power-on initialization, if GCTL.SOFITPSYNC or GFLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. The programmable maximum value is 62ns, and the minimum value is 8ns. You must use a reference clock with a period that is an integer multiple, so that ITP can meet the jitter margin of 32ns. The allowable ref_clk frequencies whose period is not integer multiples are 16/17/19.2/24/39.7MHz. This field must not be set to 0 at any time. If you never plan to use this feature, then set this field to 'h8, the default value.
21	RW	0x0	no_extr_di No Extra Delay Between SOF and the First. Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host must wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. 1'b0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. 1'b1: Host doesn't wait after a SOF before it sends the first USB packet.
20:18	RO	0x0	reserved
17	RW	0x0	sprs_ctrl_trans_en Sparse Control Transaction Enable. Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames.

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Bit	Attr	Reset Value	Description
16	RW	0x0	res_bw_hs_esp Reserving 85% Bandwidth for HS Periodic EPs. By default, HC reserves 80% of the bandwidth for periodic EPs. If this bit is set, the bandwidth is relaxed to 85% to accommodate two high speed, high bandwidth ISOC EPs. USB 2.0 required 80% bandwidth allocated for ISOC traffic. If two High-bandwidth ISOC devices (HD Webcams) are connected, and if each requires 1024-bytes X 3 packets per Micro-Frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 payload per Micro-Frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
15	RW	0x1	cm_dev_addr Compliance Mode for Device Address. When this bit is 1'b1, Slot ID may have different value than Device Address if max_slot_enabled < 128. 1'b1: Increment Device Address on each Address Device command. 1'b0: Device Address is equal to Slot ID. The xHCI compliance requires this bit to be set to 1. The 0 mode is for debug purpose only. This allows you to easily identify a device connected to a port in the Lecroy or Eliisys trace during hardware debug. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
14	RW	0x0	usb_host_in_auto_retry_en Host IN Auto Retry. 1'b0: Auto Retry Disabled 1'b1: Auto Retry Enabled Note: This bit is also applicable to the device mode.
13	RW	0x0	en_overlap_chk Not applied.

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Bit	Attr	Reset Value	Description
12	RW	0x0	ext_cap_suppt_en External Extended Capability Support Enable When set, this field enables extended capabilities to be implemented outside the core. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in Debug Capability returns 16. A read to the first DWORD of the last internal extended capability (the "xHCI Supported Protocol Capability for USB 3.0" when the Debug Capability is not enabled) returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability (for example, at address N+16 where N is the address of this DWORD). If enabled, an external address decoder that snoops the xHC slave interface must be implemented. If it sees an access to N+16 or greater, the slave access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer' field. This indicates there are no more capabilities.
11	RW	0x0	insrt_extr_fsbodi Insert Extra Delay Between FS Bulk OUT. Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b0: Host doesn't insert extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. Note: Setting this bit to one will reduce the Bulk OUT transfer performance for most of the FS devices.
10:9	RW	0x0	dtct Device Timeout Coarse Tuning. This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The core first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: 2'b00: 0 usec -> use DTFT value instead 2'b01: 500 usec 2'b10: 1.5 msec 2'b11: 6.5 msec

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Bit	Attr	Reset Value	Description
8:0	RW	0x010	ctft Device Timeout Fine Tuning. This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For the DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. The minimum value of DTFT is 2. For example, if the mac3_clk is 125 MHz clk (8 ns period), this is calculated as follows: (DTFT value) * 256 * (8 ns) Quick Reference: if DTFT = 0x2, 2*256*8 = 4usec timeout if DTFT = 0x5, 5*256*8 = 10usec timeout if DTFT = 0xA, 10*256*8 = 20usec timeout if DTFT = 0x10, 16*256*8 = 32usec timeout if DTFT = 0x19, 25*256*8 = 51usec timeout if DTFT = 0x31, 49*256*8 = 100usec timeout if DTFT = 0x62, 98*256*8 = 200usec timeout

USB3OTG_GBUSERRADDRLO

Address: Operational Base(0xFE500000) + offset (0xC130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	buserraddr Bus Address - Low. This register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core. Note: Only supported in AHB and AXI configurations.

USB3OTG_GBUSERRADDRHI

Address: Operational Base(0xFE500000) + offset (0xC134)

Bit	Attr	Reset Value	Description
31:0	RU	0x00000000	buserraddr Bus Address - High. This register contains the higher 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core. Note: Only supported in AHB and AXI configurations.

USB3OTG_GPRTBIMAPLO

Address: Operational Base(0xFE500000) + offset (0xC138)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	BINUM1 SS USB Instance Number for Port 1 Application-programmable ID field.

USB3OTG_GHWPARAMS0

Address: Operational Base(0xFE500000) + offset (0xC140)

Bit	Attr	Reset Value	Description
31:0	RO	0x2020400a	ghwparams0 Global Hardware Parameters Register 0.

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USB3OTG_GHWPARAMS1

Address: Operational Base(0xFE500000) + offset (0xC144)

Bit	Attr	Reset Value	Description
31:0	RO	0x0120c93b	ghwparams1 Global Hardware Parameters Register 1.

USB3OTG_GHWPARAMS2

Address: Operational Base(0xFE500000) + offset (0xC148)

Bit	Attr	Reset Value	Description
31:0	RO	0x20190520	ghwparams2 Global Hardware Parameters Register 2.

USB3OTG_GHWPARAMS3

Address: Operational Base(0xFE500000) + offset (0xC14C)

Bit	Attr	Reset Value	Description
31:0	RO	0x069cd084	ghwparams3 Global Hardware Parameters Register 3.

USB3OTG_GHWPARAMS4

Address: Operational Base(0xFE500000) + offset (0xC150)

Bit	Attr	Reset Value	Description
31:0	RO	0x47822010	ghwparams4 Global Hardware Parameters Register 4.

USB3OTG_GHWPARAMS5

Address: Operational Base(0xFE500000) + offset (0xC154)

Bit	Attr	Reset Value	Description
31:0	RO	0x04204018	ghwparams5 Global Hardware Parameters Register 5.

USB3OTG_GHWPARAMS6

Address: Operational Base(0xFE500000) + offset (0xC158)

Bit	Attr	Reset Value	Description
31:0	RO	0x09d78020	ghwparams6 Global Hardware Parameters Register 6.

USB3OTG_GHWPARAMS7

Address: Operational Base(0xFE500000) + offset (0xC15C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ghwparams7 Global Hardware Parameters Register 7.

USB3OTG_GDBGFIFOSPACE

Address: Operational Base(0xFE500000) + offset (0xC160)

Bit	Attr	Reset Value	Description
31:16	RO	0x000a	space_available Space Available.
15:9	RO	0x00	reserved
8:0	RW	0x000	fifo_queue_select FIFO/Queue Select (or) Port-Select. FIFO/Queue Select[8:5] indicates the FIFO/Queue Type. FIFO/Queue Select[4:0] indicates the FIFO/Queue Number. Port-Select[3:0] selects the port-number when accessing GDBGLTSSM register.

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USB3OTG_GDBGLNMCC

Address: Operational Base(0xFE500000) + offset (0xC168)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	lnmcc_berc This field indicates the bit error rate information for the port selected in the GDBGFIFOSPACE.PortSelect field. This field is for debug purposes only.

USB3OTG_GDBGBMU

Address: Operational Base(0xFE500000) + offset (0xC16C)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	bmu_bcu BMU_BCU Debug information.
7:4	RO	0x0	bmu_dcu BMU_DCU Debug information.
3:0	RO	0x0	bmu_ccu BMU_CCU Debug information.

USB3OTG_GDBGLSPMUX

Address: Operational Base(0xFE500000) + offset (0xC170)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x3f	logic_analyzer_trace Logic Analyzer Trace Port MUX Select. Currently only bits[21:16] are used. A value of 6'h3F drives "0"s on the logic_analyzer_trace signal. If you plan to OR (instead using a mux) this signal with other trace signals in your system to generate a common trace signal, you can use this feature.
15	RW	0x0	endbc Enable debugging of Debug capability LSP in Host mode. Use HostSelect to select DbC LSP debug information presented in the GDBGLSP register.
14	RO	0x0	reserved
13:8	RW	0x00	hostselect Host LSP Select. Selects the LSP debug information presented in the GDBGLSP register in host mode.
7:4	RW	0x0	devselect Device LSP Select. Selects the LSP debug information presented in the GDBGLSP register in device mode. Or bit[7:4] of HOSTSELECT, Selects the LSP debug information presented in the GDBGLSP register in host mode.
3:0	RW	0x0	epselect Device Endpoint Select. Selects the Endpoint debug information presented in the GDBGEPINFO registers in device mode. Or bit[3:0] of HOSTSELECT, Selects the LSP debug information presented in the GDBGLSP register in host mode.

USB3OTG_GDBGLSP

Address: Operational Base(0xFE500000) + offset (0xC174)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lspdebug LSP Debug Information.

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USB3OTG_GDBGEPINFO0

Address: Operational Base(0xFE500000) + offset (0xC178)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	epdebug Endpoint Debug Information Low 32-bit.

USB3OTG_GDBGEPINFO1

Address: Operational Base(0xFE500000) + offset (0xC17C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00800000	epdebug Endpoint Debug Information High 32-bit.

USB3OTG_GPRTBIMAP_HSLO

Address: Operational Base(0xFE500000) + offset (0xC180)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	binum1 HS USB Instance Number for Port 1. Application-programmable ID field.

USB3OTG_GPRTBIMAP_FSLO

Address: Operational Base(0xFE500000) + offset (0xC188)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	binum1 FS USB Instance Number for Port 1. Application-programmable ID field.

USB3OTG_GUSB2PHYCFG0

Address: Operational Base(0xFE500000) + offset (0xC200)

Bit	Attr	Reset Value	Description
31	RW	0x0	physoftrst UTMI PHY Soft Reset. Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI because ULPI PHYs are reset via their FunctionControl. Reset register, and the core automatically writes to this register when the core is reset (vcc_reset_n, USBCMD.HCRST, DCTL.SoftReset, or GCTL.SoftReset).
30	RW	0x1	u2_freeclk_exists Specifies whether your USB 2.0 PHY provides a free-running PHY clock, which is active when the clock control input is active. If your USB 2.0 PHY provides a free-running PHY clock, it must be connected to the utmi_clk[0] input. The remaining utmi_clk[n] must be connected to the respective port clocks. The core uses the Port-0 clock for generating the internal mac2 clock. 1'b0: USB 2.0 free clock does not exist 1'b1: USB 2.0 free clock exists Note: When the core is configured as device-only, do not set this bit to 1.
29:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:22	RW	0x0	lstrd LS Turnaround Time. This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: 3'h0: 2 bit times 3'h1: 2.5 bit times 3'h2: 3 bit times 3'h3: 3.5 bit times 3'h4: 4 bit times 3'h5: 4.5 bit times 3'h6: 5 bit times 3'h7: 5.5 bit times Note: This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h0 (2 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the Open LS mouse requires 3 bit times of inter-packet gap to work correctly.
21:19	RW	0x2	lsipd LS Inter-Packet Time. This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows: 3'h0: 2 bit times 3'h1: 2.5 bit times 3'h2: 3 bit times 3'h3: 3.5 bit times 3'h4: 4 bit times 3'h5: 4.5 bit times 3'h6: 5 bit times 3'h7: 5.5 bit times Note: This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h2 (3 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly.
18:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13:10	RW	0x9	usbtrdim USB 2.0 Turnaround Time. Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). The following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+/ULPI. If SoC bus clock is less than 60 MHz, and USB turnaround time is not critical, this field can be set to a larger value. Note: This field is valid only in device mode.
9	RW	0x0	xcvrdly Transceiver Delay. Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal (for HS) and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay (of approximately 2.5 us) is introduced from the time when the Transceiver Select is set to 2'b00 (HS) to the time the TxValid is driven to 0 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. Note: If you enable the hibernation feature when the device core comes out of power-off, you must re-initialize this bit with the appropriate value because the core does not save and restore this bit value during hibernation. This bit is valid only in device mode.
8	RW	0x0	enblslpm Enable utmi_sleep_n and utmi_l1_suspend_n. The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the L1 state. 1'b0: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is not transferred to the external PHY. 1'b1: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is transferred to the external PHY. Note: This bit must be set high for Port0 if SNPS PHY is used. In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
7	RO	0x0	physel USB 2.0 High-Speed PHY or USB 1.1 Full-Speed. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY. 1'b1: USB 1.1 full-speed serial transceiver.

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Bit	Attr	Reset Value	Description
6	RW	0x0	suspendusb20 Suspend USB2.0 HS/FS/LS PHY. When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. If it is set to 1, then the application must clear this bit after power-on reset. Application needs to set it to 1 after the core initialization completes. For all other configurations, this bit can be set to 1 during core configuration. Note: In host mode, on reset, this bit is set to 1. Software can override this bit after reset. In device mode, before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. If you issue a command without disabling this bit when the device is in L2 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
5	RO	0x0	reserved
4	RO	0x0	ulpi_utmi_sel ULPI or UTMI+ Select. 1'b0: UTMI+ Interface 1'b1: ULPI Interface
3	RW	0x0	phyif If UTMI+ is selected, the application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. 1'b0: 8 bits 1'b1: 16 bits
2:0	RW	0x0	tout_cal HS/FS Timeout Calibration. The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor; this factor is added to the high-speed/full-speed interpacket timeout duration in the core to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times

USB3OTG_GUSB3PIPECTL0

Address: Operational Base(0xFE500000) + offset (0xC2C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	PHYSoftRst USB3 PHY Soft Reset After setting this bit to 1, the software needs to clear this bit.

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Bit	Attr	Reset Value	Description
30	RW	0x0	HstPrtCmpl This feature tests the PIPE PHY compliance patterns without having to have a test fixture on the USB 3.0 cable. This bit enables placing the SS port link into a compliance state. By default, this bit must be set to 1'b0. In compliance lab testing, the SS port link enters compliance after failing the first polling sequence after power on. Set this bit to 0, when you run compliance tests. The sequence for using this functionality is as follows: 1. Disconnect any plugged in devices. 2. Perform USBCMD.HCRST or power-on-chip reset. 3. Set PORTSC.PP=0. 4. Set GUSB3PIPECTL. HstPrtCmpl=1. This places the link into compliance state. To advance the compliance pattern, follow this sequence (toggle the set GUSB3PIPECTL. HstPrtCmpl): 1. Set GUSB3PIPECTL.HstPrtCmpl=0. 2. Set GUSB3PIPECTL.HstPrtCmpl=1. This advances the link to the next compliance pattern. To exit from the compliance state, perform USBCMD.HCRST or power-on-chip reset.
29	RW	0x0	U2SSInactP3ok 1'b0: During link state U2/SS.Inactive, put PHY in P2 (Default) 1'b1: During link state U2/SS.Inactive, put PHY in P3
28	RW	0x0	DisRxDetP3 Disabled receiver detection in P3 1'b0: If PHY is in P3 and Core needs to perform receiver detection, the core performs receiver detection in P3. (Default) 1'b1: If PHY is in P3 and Core needs to perform receiver detection, the core changes the PHY power state to P2 and then performs receiver detection. After receiver detection, the cores changes PHY power state to P3.
27	RW	0x0	Ux_exit_in_Px 1'b0: The core does U1/U2/U3 exit in PHY power state P0 (default behavior). 1'b1: The core does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively.
26	RW	0x0	ping_enhancement_en Ping Enhancement Enable When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for the downstream port only.
25	RW	0x0	u1u2exitfail_to_recov U1U2exitfail to Recovery When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake.

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Bit	Attr	Reset Value	Description
24	RW	0x0	request_p1p2p3 Always Request P1/P2/P3 for U1/U2/U3 When set, the core always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit (remotely initiated, or locally initiated) happens, the core does not request P1/P2/P3 power state change.
23	RW	0x0	StartRxDetU3RxDet Start Receiver Detection in U3/Rx.Detect (StartRxdetU3RxDet) If DWC_USB3_GUSB3PIPECTL_INIT[22] is set, and the link is in either U3 or Rx.Detect state, the core starts receiver detection on the rising edge of this bit. This can only be used for Downstream ports. This bit must be set to '0' for Upstream ports. This feature must not be enabled for normal operation.
22	RW	0x0	DisRxDetU3RxDet Disable Receiver Detection in U3/Rx.Det When set, the core does not handle receiver detection in either U3 or Rx.Detect states. DWC_USB3_GUSB3PIPECTL_INIT[23] must be used to start receiver detection manually. This bit can only be used for the downstream port. This bit must be set to 0 for Upstream ports. This feature must not be enabled for normal operation. If you have to use this feature, contact SNPS.
21:19	RW	0x0	DelayP1P2P3 Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality.
18	RW	0x0	DELAYP1TRANS DELAYP1TRANS Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. 1'b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0 1'b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIlde and pipe3_RxValid. Note: This bit must be set to '1' for SNPS PHY. It is also used by third-party SS PHY.
17	RO	0x0	reserved
16:15	RW	0x0	DATWIDTH 2'b00: 32 bits 2'b01: 16 bits 2'b10: 8 bits One clock after reset, these bits receive the value seen on the pipe3_DataBusWidth.
14	RW	0x0	AbortRxDetInU2 Abort Rx Detect in U2 (AbortRxDetInU2) When set, and the link state is U2, then the core will abort receiver detection if it receives U2 exit LFPS from the remote link partner. This bit is for the downstream port only.

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Bit	Attr	Reset Value	Description
13	RW	0x0	SkipRxDet Skip Rx Detect: When set, the core skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.
12	RW	0x0	LFPSP0Algn LFPS P0 Align When set: 1. The core deasserts LFPS transmission on the clock edge that it requests Phy power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. 2. The core requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state.
11	RW	0x0	P3P2TranOK P3 P2 Transitions OK (P3P2TranOK) When set, the core transitions directly from Phy power state P2 to P3 or from state P3 to P2. When not set, P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE3 Specification. According to the PIPE3 Specification, any direct transition between P3 and P2 is illegal.
10	RW	0x0	P3ExSigP2 P3 Exit Signal in P2 When this bit is set, the core always changes the PHY power state to P2, before attempting a U3 exit handshake. This bit is used only for some non-SNPS PHYs that cannot do LFPS in P3. Note: This bit is used by third-party SS PHY. It must be set to '0' for SNPS PHY.
9	RW	0x0	LFPSFILTER LFPS Filter When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted.
8	RW	0x0	RX_DETECT_to_Polling_L RX_DETECT to Polling.LFPS Control 1'b0 (Default): Enables a 400us delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. 1'b1: Disables the 400us delay to start Polling LFPS after RX_DETECT. During controller certification with third party PHY it is observed that the PHY is not able to meet the Tx AC common mode voltage active (VTX-CM-ACPP_ACTIVE <100mv) if the link starts polling within 80us from the time rx.detect is performed. To meet this VTX-CM-ACPP_ACTIVE specification, the polling must be delayed further. If the PHY does not have issue then they can set this bit to 1 which allows polling to start within 80us.
7	RO	0x0	reserved
6	RW	0x0	TX_SWING Tx Swing (TxSwing) Refer to the PIPE3 specification.
5:3	RW	0x0	TX_MARGIN Tx Margin[2:0] (TxMargin) Refer to Table 5-3 of the PIPE3 Specification.

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	TX_DE_EPPHASIS Tx Deemphasis The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode.
0	RW	0x0	ELASTIC_BUFFER_MODE Elastic Buffer Mode (ElasticBufferMode) (Refer to Table 5-3 of the PIPE3 specification.)

USB3OTG_GTXFIFOSIZn

Address: Operational Base(0xFE500000) + offset (0xC300)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	txfstaddr_n Transmit FIFOn RAM Start Address. This field contains the memory start address for TxFIFOn in 64-bit words.
15:0	RW	0x0042	txfdep_n TxFIFO Depth. This field contains the depth of TxFIFOn in 64-bit words. Minimum value: 32; Maximum value: 32,768.

USB3OTG_GRXFIFOSIZn

Address: Operational Base(0xFE500000) + offset (0xC380)

Bit	Attr	Reset Value	Description
31:16	RW	0x0334	rxfstaddr_n RxFIFOn RAM Start Address. This field contains the memory start address for RxFIFOn in 64-bit words.
15:0	RW	0x0185	rxfdep_n RxFIFOn RAM Start Address. This field contains the memory start address for RxFIFOn in 64-bit words.

USB3OTG_GEVNTADRLO0

Address: Operational Base(0xFE500000) + offset (0xC400)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	evntadrlo Event Buffer Address. Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

USB3OTG_GEVNTADRHI0

Address: Operational Base(0xFE500000) + offset (0xC404)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	evntadrhi Event Buffer Address. Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

USB3OTG_GEVNTSIZ0

Address: Operational Base(0xFE500000) + offset (0xC408)

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Bit	Attr	Reset Value	Description
31	RW	0x0	evntintrptmask Event Interrupt Mask. When set to '1', this prevents the interrupt from being generated. However, even when the mask is set, the events are queued.
30:16	RO	0x0000	reserved
15:0	RW	0x0000	eventsiz Event Buffer Size in bytes. Holds the size of the Event Buffer in bytes; must be a multiple of four. This is programmed by software once during initialization. The minimum size of the event buffer is 32 bytes.

USB3OTG_GEVNTCOUNT0

Address: Operational Base(0xFE500000) + offset (0xC40C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	evntcount Event Count. When read, returns the number of valid events in the Event Buffer (in bytes). When written, hardware decrements the count by the value written. The interrupt line remains high when count is not 0.

USB3OTG_GHWPARAMS8

Address: Operational Base(0xFE500000) + offset (0xC600)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000047c	ghwparams8_32_0 ghwparams8

USB3OTG_GTXFIFOPRIDEV

Address: Operational Base(0xFE500000) + offset (0xC610)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	gtxfifopridev Device TxFIFO priority. This register specifies the relative DMA priority level among the Device TXFIFOs (one per IN endpoint). Each register bit[n] controls the priority (1: high, 0: low) of each TXFIFO[n]. When multiple TXFIFOs compete for DMA service at a given time (that is, multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. High-priority TXFIFOs are granted access using round-robin arbitration 2. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. When configuring periodic IN endpoints, software must set register bit[n]=1, where n is the TXFIFO assignment. This ensures that the DMA for isochronous or interrupt IN endpoints are prioritized over bulk or control IN endpoints. This register is present only when the core is configured to operate in the device mode. The register size corresponds to the number of Device IN endpoints.

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USB3OTG_GTXFIFOPRIHST

Address: Operational Base(0xFE500000) + offset (0xC618)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	gtxfifoprihst Host TxFIFO priority. This register specifies the relative DMA priority level among the Host TXFIFOs (one per USB bus instance) within the associated speed group (HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of TXFIFO[n] within a speed group. When multiple TXFIFOs compete for DMA service at a given time (i.e., multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (HS/FSLS): a. High-priority TXFIFOs are granted access using round-robin arbitration b. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). 2. The TX DMA arbiter prioritizes the HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the core is configured to operate in the host mode (includes DRD and OTG modes). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 2 USB bus instances (1 HS, and 1 FSLS).

USB3OTG_GRXFIFOPRIHST

Address: Operational Base(0xFE500000) + offset (0xC61C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	grxfifoprihst Host RxFIFO priority This register specifies the relative DMA priority level among the Host RXFIFOs (one per USB bus instance) within the associated speed group (HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of RXFIFO[n] within a speed group. When multiple RXFIFOs compete for DMA service at a given time (i.e., multiple RXQs contain RX DMA requests and their corresponding RXFIFOs have data available), the RX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (HS/FSLS): a. High-priority RXFIFOs are granted access using round-robin arbitration b. Low-priority RXFIFOs are granted access using round-robin arbitration only after high-priority RXFIFOs have no further processing to do (that is, either the RXQs are empty or the corresponding RXFIFOs do not have the required data). 2. The RX DMA arbiter prioritizes the HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the core is configured to operate in the host mode (includes DRD and OTG modes). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 2 USB bus instances (1 HS, and 1 FSLS).

USB3OTG_GFIFOPRIDBC

Address: Operational Base(0xFE500000) + offset (0xC620)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	gfifopridbc Host DbC DMA priority. This register specifies the relative priority of the RXFIFOs and TXFIFOs associated with the DbC mode. It overrides the priority assigned in the corresponding indexes of the Host RXFIFO and TXFIFO DMA priority registers, when the DbC mode is enabled.

USB3OTG_GDMAHLRATIO

Address: Operational Base(0xFE500000) + offset (0xC624)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:8	RW	0x0000	hstrxfifo Host RXFIFO DMA High-Low Priority.
7:5	RO	0x0	reserved
4:0	RW	0x00	hsttxfifo Host TXFIFO DMA High-Low Priority.

USB3OTG_GFLADJ

Address: Operational Base(0xFE500000) + offset (0xC630)

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Bit	Attr	Reset Value	Description
31	RW	0x0	gfladj_refclk_240mhzdecr_pls1 This field indicates that the decrement value that the controller applies for each ref_clk must be GFLADJ_REFCLK_240MHZ_DECR and GFLADJ_REFCLK_240MHZ_DECR +1 alternatively on each ref_clk. Set this bit to a 1 only if GFLADJ_REFCLK_LPM_SEL is set to 1 and the fractional component of 240/ref_frequency is greater than or equal to 0.5. Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = (240/24) = 10 3. GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 0
30:24	RW	0x00	gfladj_refclk_240mhz_decr This field indicates the decrement value that the controller applies for each ref_clk in order to derive a frame timer in terms of a 240-MHz clock. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1. The value is derived as follows: GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/24 = 10
23	RW	0x0	gfladj_refclk_lpm_sel This bit enables the functionality of running SOF counters on the ref_clk. This bit must not be set to 1 if GCTL.SOFITPSYNC bit is set to 1. Similarly, if GFLADJ_REFCLK_LPM_SEL set to 1, GCTL.SOFITPSYNC must not be set to 1. Note that the ref_clk frequencies supported in this mode are 16/17/19.2/20/24/39.7/40 MHz. The utmi_clk[0] signal of the core must be connected to the FREECLK of the PHY. Note: If you set this bit to 1, the GUSB2PHYCFG.U2_FREECLK_EXISTS bit must be set to 0.
22	RO	0x0	reserved
21:8	RW	0x0000	gfladj_refclk_fladj This field indicates the frame length adjustment to be applied when SOF counter is running on the ref_clk. SOF interval when GLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1 or GCTL.SOFITPSYNC is set to 1. The value is derived as follows: FLADJ_REF_CLK_FLADJ=((125000/ref_clk_period_integer)-(125000/ref_clk_period)) * ref_clk_period where: 1. The ref_clk_period_integer is the integer value of the ref_clk period got by truncating the decimal (fractional) value that is programmed in the GUCTL.REF_CLK_PERIOD field. 2. The ref_clk_period is the ref_clk period including the fractional value. Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GLADJ_REFCLK_FLADJ = ((125000/41)-(125000/41.6666))*41.6666 = 2032 (ignoring the fractional value).

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Bit	Attr	Reset Value	Description
7	RW	0x0	gfladj_30mhz_sdbnd_sel This field selects whether to use the input signal fladj_30mhz_reg or the GFLADJ.GFLADJ_30MHZ to adjust the frame length for the SOF. When this bit is set to: 1'b1: the controller uses the register field GFLADJ.GFLADJ_30MHZ value 1'b0: the controller uses the input signal fladj_30mhz_reg value.
6	RO	0x0	reserved
5:0	RW	0x00	gfadj_30mhz This field indicates the value that is used for frame length adjustment instead of considering from the sideband input signal fladj_30mhz_reg. This enables post-silicon frame length adjustment in case the input signal fladj_30mhz_reg is connected to a wrong value or is not valid. For details on how to set this value, refer to section 5.2.4, "Frame Length Adjustment Register (FLADJ)," of the xHCI Specification.

USB3OTG_DCFG

Address: Operational Base(0xFE500000) + offset (0xC700)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	ignstrmpp This bit only affects stream-capable bulk endpoints. Not applied.
22	RW	0x0	lpmcap LPM Capable. Not applied.
21:17	RW	0x04	nump Number of Receive Buffers. Not applied.
16:12	RW	0x00	intrnum Interrupt number. Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts (see DEVT) are generated.
11:10	RO	0x0	reserved
9:3	RW	0x00	devaddr Device Address. The application must perform the following: 1. Program this field after every SetAddress request. 2. Reset this field to zero after USB reset.
2:0	RW	0x0	devspd Device Speed. Indicates the speed at which the application requires the core to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 3'b000: High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 3'b001: Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz)

USB3OTG_DCTL

Address: Operational Base(0xFE500000) + offset (0xC704)

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Bit	Attr	Reset Value	Description
31	RW	0x0	run_stop The software writes 1 to this bit to start the device controller operation. To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: 1. After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. 2. The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared is specified in the Note below. If the software attempts a connect after the soft disconnect or detects a disconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stop bit. 3. When the USB is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller. Note: The following is the minimum duration under various conditions for which the soft disconnect (SftDiscon) bit must be set for the USB host to detect a device disconnect: 10ms: For high-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions); For full-speed/low-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions). To accommodate clock jitter, it is recommended that the application add extra delay to the specified minimum duration.

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Bit	Attr	Reset Value	Description
30	R/W SC	0x0	csftrst Core Soft Reset. Reset all clock domains as follows: 1. This bit clears the interrupts and all the CSRs except GSTS, GSNPSID, GGPIO, GUID, GUSB2PHYCFGn registers, GUSB3PIPECTLn registers, DCFG, DCTL, DEVTEN, and DSTS registers. 2. All module state machines (except the SoC Bus Slave Unit) are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. 3. Any transactions on the SoC bus Master are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the core. This is a self-clearing bit; the core clears this bit after all necessary logic is reset in the core, which may take several clocks depending on the core's current state. Once this bit is cleared, the software must wait at least 3 PHY clocks before accessing the PHY domain (synchronization delay). Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation.
29	RO	0x0	reserved
28:24	RW	0x00	hirdthres HIRD Threshold. The core asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The core asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: 1. HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] 2. HIRD_Thres[4] is set to 1'b1. The core asserts utmi_sleep_n on L1 when one of the following is true: 1. If the HIRD value is less than HIRD_Thres[3:0] or 2. HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation.

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Bit	Attr	Reset Value	Description
23:20	RW	0xf	lpm_nyet_thres LPM NYET Threshold Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. DCFG.LPMCap is 1'b0 - The core always responds with Timeout (that is, no response). DCFG.LPMCap is 1'b1 - The core responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: 1. There are no PID or CRC5 errors in both the EXT token and the LPM token (if not true, inactivity results in a timeout ERROR). 2. No data is pending in the Transmit FIFO and OUT endpoints not in flow controlled state (else NYET). 3. The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0].
19	RW	0x0	keep_connect When 1, this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to 0. The device core disconnects from the host when DCTL.RunStop is set to 0. This bit indicates whether to preserve this behavior (0), or if the core must not disconnect when RunStop is set to 0 (1).
18	RW	0x0	l1_hibernation_en When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core does not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.
17	RW	0x0	crs Controller Restore State. This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to 1, the controller immediately sets DSTS.RSS to 1. When the controller has finished the restore process, it sets DSTS.RSS to 0. Note: When read, this field always returns 0.
16	RW	0x0	css Controller Save State. This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to 1, the controller immediately sets DSTS.SSS to 1. When the controller has finished the save process, it sets DSTS.SSS to 0. Note: When read, this field always returns 0.
15:13	RO	0x0	reserved
12	RW	0x0	initu2ena Not applied.
11	RW	0x0	acceptu2ena Not applied.
10	RW	0x0	initu1ena Not applied.
9	RW	0x0	acceptu1ena Not applied.

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Bit	Attr	Reset Value	Description
8:5	RW	0x0	ulstchngreq Software writes this field to issue a USB state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. In HS/FS/LS mode: Value: Requested USB state transition 8: Remote wakeup request Others: Reserved The Remote wakeup request must be issued 2us after the device goes into suspend state (DSTS[21:18] is 3). Note: After coming out of hibernation, software must write 8 (Recovery) into this field to confirm exit from the suspended state.
4:1	RW	0x0	tstctl Test Control. 4'b000: Test mode disabled 4'b001: Test_J mode 4'b010: Test_K mode 4'b011: Test_SE0_NAK mode 4'b100: Test_Packet mode 4'b101: Test_Force_Enable Others: Reserved
0	RO	0x0	reserved

USB3OTG_DEVTEN

Address: Operational Base(0xFE500000) + offset (0xC708)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	vendevtstrcvden Vendor Device Test LMP Received Event. 1'b0: Disable this event 1'b1: Enable this event
11:10	RO	0x0	reserved
9	RW	0x0	errticerrevten Erratic Error Event Enable. 1'b0: Disable this event 1'b1: Enable this event
8	RO	0x0	reserved
7	RW	0x0	softevten Start of (u)frame Event Enable. 1'b0: Disable this event 1'b1: Enable this event
6	RW	0x0	u3l2l1_susp_en U3/L2-L1 Suspend Event Enable. 1'b0: Disable this event 1'b1: Enable this event
5	RW	0x0	hibernation_req_evt_en Hibernation Request Event Enable. 1'b0: Disable this event 1'b1: Enable this event

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Bit	Attr	Reset Value	Description
4	RW	0x0	wkupevten Resume/Remote Wakeup Detected Event Enable. 1'b0: Disable this event 1'b1: Enable this event
3	RW	0x0	ulstcngen USB State Change Event Enable. 1'b0: Disable this event 1'b1: Enable this event
2	RW	0x0	connectdoneevten Connection Done Event Enable. 1'b0: Disable this event 1'b1: Enable this event
1	RW	0x0	usbrstevten USB Reset Event Enable. 1'b0: Disable this event 1'b1: Enable this event
0	RW	0x0	disconnevten Disconnect Detected Event Enable. 1'b0: Disable this event 1'b1: Enable this event

USB3OTG_DSTS

Address: Operational Base(0xFE500000) + offset (0xC70C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	dcnrd Device Controller Not Ready. The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to 1 and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt.
28:26	RO	0x0	reserved
25	RW	0x0	rss Restore State Status. This bit is similar to the USBSTS.RSS in host mode. When the controller finishes the restore process, it completes the command by setting DSTS.RSS to 0.
24	RO	0x0	sss Save State Status. This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to 0.
23	RO	0x0	coreidle Core Idle. The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero. Note: While testing for Reset values, mask out the read value. This bit represents the changing state of the core and does not hold a static value.

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Bit	Attr	Reset Value	Description
22	RO	0x1	devctrlhlt Device Controller Halted. This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to 0, the core is idle and the lower layer finishes the disconnect process. When Halted=1, the core does not generate Device events. Note: The core does not set this bit to 1 if GEVNTCOUNTn has some valid value. Software needs to acknowledge the events that are generated (by writing to GEVNTCOUNTn) while it is waiting for this bit to be set to 1.
21:18	RO	0x4	usblnkst USB/Link State In SS mode: LTSSM State 4'h0: U0 4'h1: U1 4'h2: U2 4'h3: U3 4'h5: RX_DET 4'h6: SS_INACT 4'h7: POLL 4'h8: RECOV 4'h9: HRESET 4'ha: CMPLY 4'hb: LPBK 4'hf: Resume/Reset In HS/FS/LS mode: 4'h0: On state 4'h2: Sleep (L1) state 4'h3: Suspend (L2) state 4'h4: Disconnected state (Default state) 4'h5: Early Suspend state (valid only when Hibernation is disabled, GCTL[1].GblHibernationEn = 0) 4'he: Reset (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) 4'hf: Resume (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) The link state Resume/Reset indicates that the core received a resume or USB reset request from the host while the link was in hibernation. Software must write 8 (Recovery) to the DCTL.ULStChngReq field to acknowledge the resume/reset request. When Hibernation is enabled, GCTL[1].GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL[31].Run/Stop set to 1 and DSTS[29].DCNRD = 0.
17	RO	0x1	rx_fifo_empty Rx Fifo Empty.
16:3	RO	0x0000	reserved
2:0	RU	0x0	connectspd Connected Speed. Indicates the speed at which the DWC_usb3 core has come up after speed detection through a chirp sequence. 3'b000: High-speed (PHY clock is running at 30 or 60 MHz) 3'b001: Full-speed (PHY clock is running at 30 or 60 MHz)

USB3OTG_DGCMDPAR

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Address: Operational Base(0xFE500000) + offset (0xC710)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the device command parameter. This must be programmed before or along with the device command. The available device commands are listed in DGCMD register.

USB3OTG_DGCMD

Address: Operational Base(0xFE500000) + offset (0xC714)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	cmdstatus Command Status: 1'b1: CmdErr: Indicates that the device controller encountered an error while processing the command. 1'b0: Indicates command success
11:10	RO	0x0	reserved
9	R/WSC	0x0	cmdact Command Active. The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.
8	RW	0x0	cmdioc Command Interrupt on Complete. When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to 1 if the DCTL.RunStop field is 0.
7:0	RW	0x00	cmdtyp Command Type. Specifies the type of command the software driver is requesting the core to perform. 8'h0: Reserved 8'h1: Set Endpoint Configuration - 64 or 96-bit Parameter 8'h2: Set Endpoint Transfer Resource Configuration - 32-bit Parameter 8'h3: Get Endpoint State - No Parameter Needed 8'h4: Clear Stall (see Set Stall) - No Parameter Needed 8'h5: Start Transfer - 64-bit Parameter 8'h6: Update Transfer - No Parameter Needed 8'h7: End Transfer - No Parameter Needed 8'h8 Start New Configuration - No Parameter Needed

USB3OTG_DALEPENA

Address: Operational Base(0xFE500000) + offset (0xC720)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usbactep USB Active Endpoints. This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0~15 and OUT endpoints 0~15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN ... The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints (resources) after USBReset. Hardware clears these bits for all endpoints (other than EP0-OUT and EP0-IN) after detecting a USB reset event. After receiving SetConfiguration and SetInterface requests, the application must program endpoint registers accordingly and set these bits.

USB3OTG_DEPnCMDPAR2

Address: Operational Base(0xFE500000) + offset (0xC800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

USB3OTG_DEPnCMDPAR1

Address: Operational Base(0xFE500000) + offset (0xC804)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command.

USB3OTG_DEPnCMDPAR0

Address: Operational Base(0xFE500000) + offset (0xC808)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 0. It must be programmed before issuing the command.

USB3OTG_DEPnCMD

Address: Operational Base(0xFE500000) + offset (0xC80C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	commandparam Command Parameters or Event Parameters when this register is written: For Start Transfer command: The 16-bit StreamID assigned to this transfer. For Start Transfer command applied to an isochronous endpoint: StartMicroFramNum, Indicates the (micro) frame number to which the first TRB applies. For Update Transfer, End Transfer, and Start New Configuration commands: [22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command. Event Parameters (EventParam), when this register is read.
15:12	RW	0x0	cmdstatus Command Completion Status. The information is in the same format as bits 15:12 of the Endpoint Command Complete event.
11	RW	0x0	hipri_forcerm HighPriority: Only valid for Start Transfer command. ForceRM: Only valid for End Transfer command. ClearPendIN: Only valid for Clear Stall command. Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.
10	RW	0x0	cmdact Command Active. Software sets this bit to 1 to enable the device endpoint controller to execute the generic command. The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
9	RO	0x0	reserved
8	RW	0x0	cmdioc Command Interrupt on Complete. When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to 1 if the DCTL.RunStop field is 0.
7:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	cmdtyp Command Type. Specifies the type of command the software driver is requesting the core to perform. 4'h0: Reserved 4'h1: Set Endpoint Configuration 64 or 96-bit Parameter 4'h2: Set Endpoint Transfer Resource Configuration - 32-bitparameter 4'h3: Get Endpoint State - No Parameter Needed 4'h4: Set Stall - No Parameter Needed 4'h5: Clear Stall (see Set Stall) - No Parameter Needed 4'h6: Start Transfer - 64-bit Parameter 4'h7: Update Transfer - No Parameter Needed 4'h8: End Transfer - No Parameter Needed 4'h9: Start New Configuration - No Parameter Needed

6.5 Interface Description

Table 6-2 USB3OTG Interface Description

Pad Name	Direction	Descriptions
USB20_OTG0_ID	I/O	USB2.0 PHY Mini-Receptacle Identifier
USB20_OTG0_DM	I/O	USB D- Signal
USB20_OTG0_DP	I/O	USB D+ Signal
USB20_OTG0_VBUSDET	I/O	USB2.0 PHY VBUS
USB30_OTG0_SSRXN/PCIE20_RXDN	I/O	Received Differential Data for USB3.0
USB30_OTG0_SSRXP/PCIE20_RXDP	I/O	
USB30_OTG0_SSTXN/PCIE20_TXDN	I/O	Transmitted Different Data for USB3.0
USB30_OTG0_SSTXP/PCIE20_TXDP	I/O	

6.6 Application Notes

6.6.1 USB2PHY Reset Sequence

In USB function mode, the recommended reset sequence is in figure 1-2. The setting can be found in CRU and GRF section, and table 1-3 also lists some information.

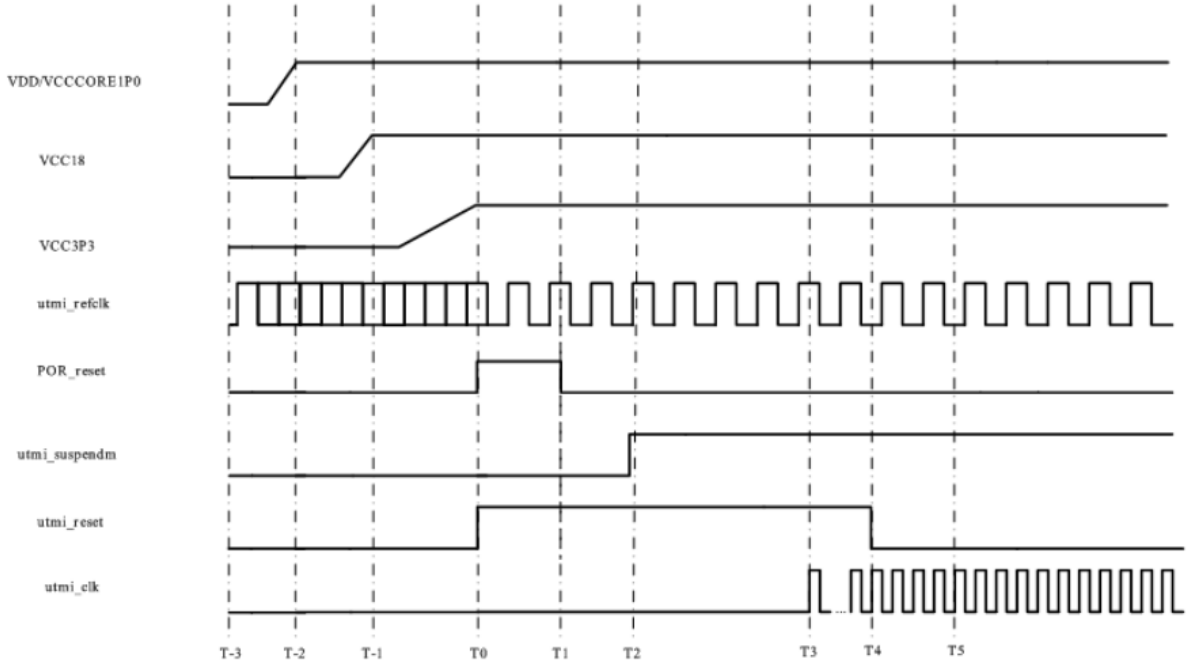

Fig. 6-2 USBPHY reset sequence

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The timing requirements can be found in table 1-3. If the USB PHY need to reset, utmi_reset need to be assert first, then POR_reset can be asserted and pull down utmi_suspend.

Table 6-3 USBPHY reset sequence

Description		Timing
T0 ~ T1	Power has been brought up and utmi_refclk is available POR_reset is set high utmi_suspendm is set low utmi_reset is set high set refclk_sel to 1'b1 or 1'b0.	This timing is SOC /product specific and outside of the control of the PHY. There is no required order for the signals to be set, but the quicker they can be set, and the faster the supplies can reach full value, the less current will leak from the PHY.
T1 ~ T2	POR_reset is set low utmi_suspendm is set low.	At least 10 us.
T2 ~ T3	utmi_suspendm is set high. This allows the PLL to startup.	At least 1 ms.
T3	The PLL has locked utmi_clk has stabilized.	
T4	utmi_clk has stabilized utmi_reset is set low. The PHY is now operational.	At least 10 utmi_clk cycles.
T4 ~ T5	The PHY is now operational.	At least 10ms.
T5	Release the reset of USB controller signal. The PHY is now operational.	

6.6.2 USB3 mode setting

USB3.0 PHY is combo with PCIE, so you must set some GRF to set USB mode (see PIPEPHY_GRF).

- Set GRF_PIPEPHY_ PIPE_CON0[3:2] to 2'b01;
  Set GRF_PIPEPHY_ PIPE_CON3[14:13] to 2'b01;
  Set GRF_PIPEPHY_ PIPE_CON2[1] to 1'b1 to select USB mode.
- Set GRF_PIPEPHY_ PIPE_CON2[12] and [15] to 1'b0. This will select TxElecidle and TxCompliance form controller.

6.6.3 OTG Programming Model

When detect ID change event (see USBPHY_GRF) or VBUS change event (see USBPHY_GRF) after disconnect, it means a USB2.0/3.0 OTG A device or B device may connect, then check status of ID (see USBPHY_GRF). If ID==0, it will work as A device, then follow host programming flow; if ID==1, it will work as B device, then it follows device programming flow.

Note: USB3OTG doesn't support host/device mode swapping through HNP and RSP.

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Chapter 7 PCIe Controller

7.1 Overview

The PCI Express (PCIe) is a high performance, general purpose I/O interconnect defined for a wide variety of future computing and communication platforms. The PCIe designed to be used as a general-purpose serial I/O interconnect in multiple market segments, including desktop, mobile, server, storage, and embedded communications. The PCIe controller implements the three PCI Express protocol layers (Transaction layer, Data Link layer, and the MAC portion of the physical layer). It also implements the application-dependent functionality of the PCI Express Transaction Layer for packet transmission, which is located between application logic and the PCI Express protocol layers.
The PCIe controller is compliant with PCI Express Specifications 1.1, 2.1. The PCIe controller subsystem consists of 1 controller, refer to Block Diagram for details.
PCIe controller subsystem supports the following features:

- Compatible with PCI Express Base Specification Revision 2.1
- Including 1 PCIe controller
  - RC mode only
    - Maximum payload size is 128 bytes
    - 8 ATU inbound regions, 8 ATU outbound regions
    - Up to Gen2 X 1 link when connecting with Combo PIPE PHY
- The following optional features of the specification
  - Alternative Routing-ID Interpretation (ARI)
  - TLP Prefix
  - Dynamic Power Allocation (DPA)
  - L1 Substates (L1SS)
  - PCI Express Active State Power Management (ASPM)
  - PCI Express Advanced Error Reporting (AER) with Multiple Header Logging
- Support Latency Tolerance Reporting (LTR)
- Support Optimized Buffer Flush and Fill (OBFF)
- Internal Datapath Operating at 62.5 MHz, 125 MHz
- Advanced Power and Clock Management
- Internal Address Translation Unit
- Integrated MSI/MSI-X Receiver Module
- RAS DES (Debug, Error Injection, and Statistics)
- ECRC Generation and Checking
- Store-and-forward Queue Modes for Rx TLPs
- Configurable Filtering Rules for Posted, Non-posted, and Completion Traffic
- Configurable BAR Filtering, I/O Filtering, Configuration Filtering and Completion Lookup/Timeout
- Three Application Transmit Clients
- MSI with Per-Vector Masking (PVM), Extended message data for MSI
- MSI-X with Per-Vector Masking (PVM)

7.2 Block Diagram

PCIe is comprised of:

- APB: APB Interface
- AXI_S: AXI Slave Interface
- AXI_M: AXI Master Interface
- AXI_DBI: AXI Slave Interface for configuration
- Client: Client Logic
- CLKRST: Clock and Reset related logic
- Memory: SRAMs and Buffers
- AMBA Bridge: AXI to Core Bridge
- PCIe Core: PCIe Controller Core
- PM: Power Management Unit
- Combo PIPE PHY

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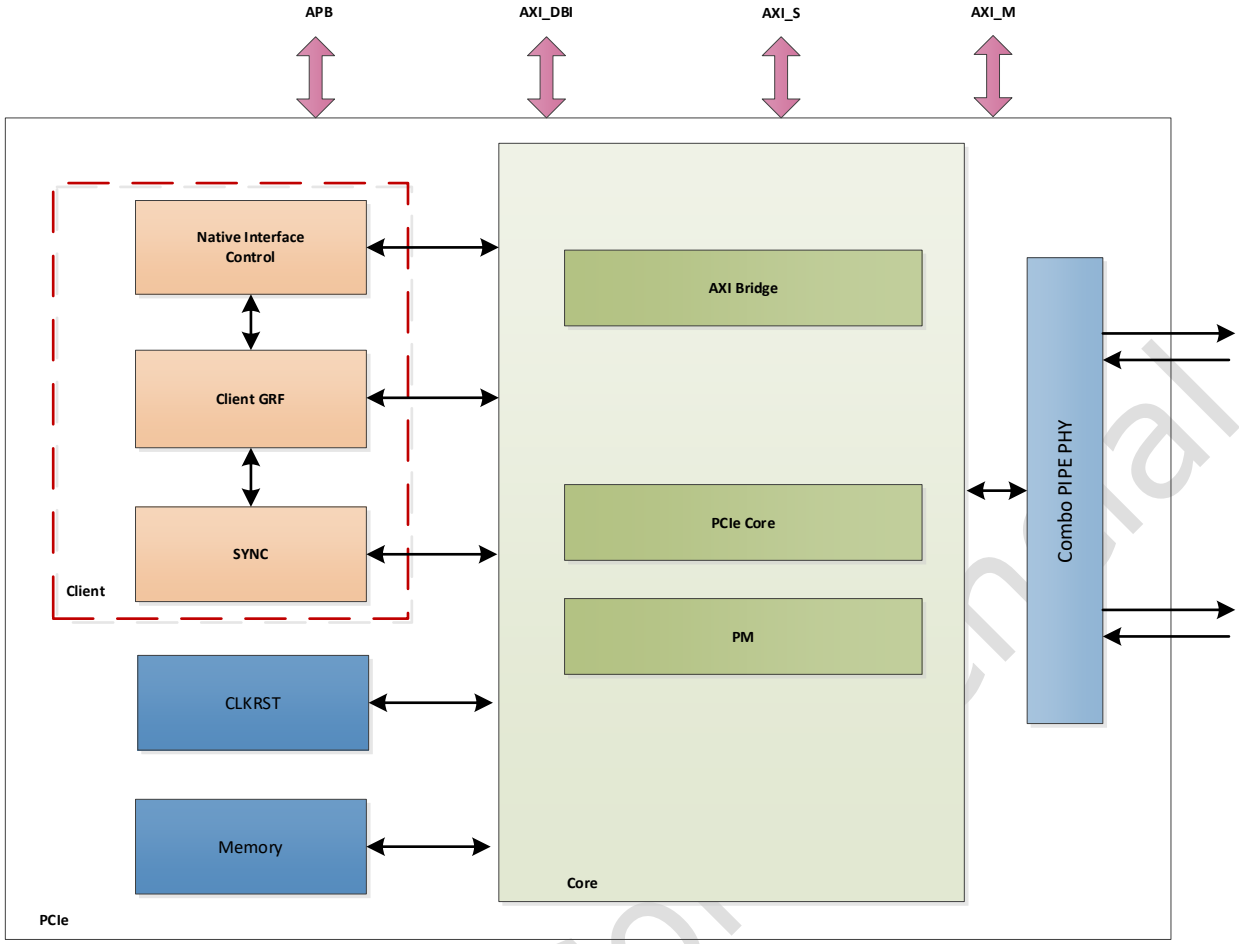

Fig. 7-1 PCIe Block Diagram

Block function description will be discussed in next section.

7.3 Function Description

7.3.1 Application Interface and AXI Bridge

Application Interface is comprised of four standard interfaces: one AXI master interface, two AXI slave interface and one APB interface. These interface bridging capability for directly adding a PCI Express link to an AXI system fabric.

The AXI bridge module acts as a bridge between the standard AXI interfaces and the PCIe controller native interfaces. The bridge interconnects the AXI interfaces within an AXI-embedded system with a remote PCIe link, as either a root complex port or as an endpoint port.

The AXI master interfaces enable a remote PCIe device to read and write to an AXI slave (in System Interface) connected to the AXI bridge. The AXI link slave interface enables an AXI master (in System Interface) to read and write through the AXI bridge to a remote PCIe device. The DBI slave enables an AXI master (in System Interface) to access the controller's registers. The APB enables Application to access the Client registers.

7.3.2 Client

Client Logic Consists of some additional logic used for application to interact with PCIe Controller. For example, applications can access client registers to send/receive PCIe Message, request to enter/exit PM state, deal with interrupts, configure some basic operation mode, read some basic debug information, and so on. For more details, please refer to Client registers description and application notes for more information.

7.3.3 CXPL

PCIe Core deal with the PCIe protocol, and consists of three main modules:

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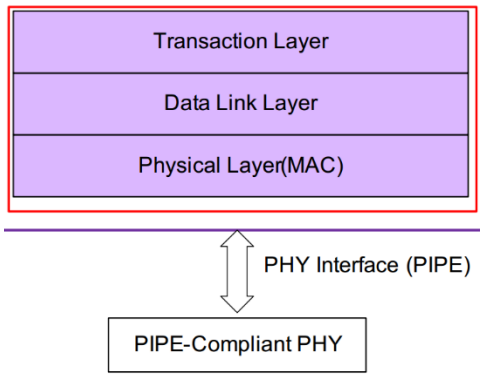

Fig. 7-2 PCIe Core Architecture Overview

The PCIe Core implements the basic functionality for the PCI Express physical, link, and transaction layers. This module implements a large part of the transaction layer logic, all of the data link layer logic, and the MAC portion of the physical layer, including the link training and status state machine (LTSSM). The Core connects to the external PHY through the standard PIPE interface.

7.3.4 PMC

PCIe Controller support PCIe ASPM, L1 Substate and PCI PM. For proper understanding of PCIe Power Management, you should be familiar with Power Management of the PCI Express Base Specification, and PCI-SIG Engineering Change Notice ECN L1 Substates with CLKREQ#. For application details, please refer to Application Notes for more information.

7.3.5 XADM

Transmit Application-Dependent Module (XADM) implements the application-specific functionality of the PCI Express transaction layer for packet transmission. Its functions include:

- TLP Arbitration
- TLP Formation
- Flow Control (FC) Credit checking

The transmit path uses a cut-through architecture. It does not implement transmit buffering/queues (other than the retry buffer). The controller maintains an internal Target Completion Lookup Table to store certain TLP header information from the Rx request.

7.3.6 RADM

Receive Application-Dependent Module (RADM) implements application-specific functionality of the PCI Express transaction layer for packet reception. Its functions include:

- Sorting/filtering of received TLPs. The filtering rules and routing are configurable.
- Buffering and queuing of the received TLPs.
- Routing of received TLP to the controller's receive interfaces.

The RADM maintains a Receive Completion Lookup Table (LUT) for completion tracking and completion-timeout monitoring of Tx non-posted requests. It indicates a timeout when an expected Rx completion does not arrive within the timeout period.

7.3.7 CDM

Configuration-Dependent Module (CDM) implements:

- Standard PCI Express configuration space
- Controller-specific register space (Port Logic Registers)

7.4 Register Description

7.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 7-1 PCIe2 RC G2 Client and Core Register Address Mapping

Base Address	Name	Device	Address Length	Offset Address Range
0xFE000000	PCIe2_1L_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0x3C0000000	PCIe2_1L_DBI	Core	4M BYTE	0x00000 ~ 0x3fffff

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Base Address	Name	Device	Address Length	Offset Address Range
		Register		
0xFC000000	PCIe2_1L_S	PCIe Outbound Memory	32M BYTE	0x0000000~0x1ffffff
0x300000000	PCIe2_1L_S	PCIe Outbound Memory	1G BYTE	0x00000000~0x3fffffff
0xFF500000	PCIe2_1L_APB	Client Register	64K BYTE	0x0000~0xffff

Table 7-2 PCIe 2 RC Core Register Map in RC mode

Offset	Register Block	Description
0x0000	TYPE1_HDR	PCI-Compatible Configuration Space Header Type1
0x0040	PM_CAP	PCI Power Management Capability Structure
0x0050	MSI_CAP	MSI Capability Structure
0x0070	PCIE_CAP	PCI Express Capability Structure
0x00b0	MSIX_CAP	MSI-X Capability Structure
0x0100	AER_CAP	Advanced Error Reporting Capability Structure
0x0148	SPCIE_CAP	Secondary PCI Express Capability Structure
0x0160	L1SUB_CAP	L1 Substates Capability Structure
0x0170	RAS_DES_CAP	RAS D.E.S. Capability Structure
0x0700	PORT_LOGIC	Port Logic
0x100000	PCIE_CAP_DBI2	DBI2 Shadow Block: PF PCI Express Capability Structure
0x1000b0	MSIX_CAP_DBI2	Shadow Block: MSI-X Capability Structure
0x300000	ATU_CAP	ATU Port Logic Structure

7.4.2 PCIe Client Register

7.4.2.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_GENERAL_CON	0x0000	W	0x00000000	General Control Register
PCIE_CLIENT_INTR_STATUS_MSG_RX	0x0004	W	0x00000000	Interrupt Status Register Related to Message Reception
PCIE_CLIENT_INTR_STATUS_LEGACY	0x0008	W	0x00000000	Interrupt Status Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_STATUS_ERR	0x000C	W	0x00000000	Interrupt Status Register Related to Error Detection
PCIE_CLIENT_INTR_STATUS_MISC	0x0010	W	0x00000000	Interrupt Status Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_STATUS_PMC	0x0014	W	0x00000000	Interrupt Status Register Related Power Management Control
PCIE_CLIENT_INTR_MASK_MSG_RX	0x0018	W	0x00007737	Interrupt Mask Register Related to Message Reception
PCIE_CLIENT_INTR_MASK_LEGACY	0x001C	W	0x000000FF	Interrupt Mask Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_MASK_ERR	0x0020	W	0x0000177F	Interrupt Mask Register Related to Error Detection

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Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_INTR_MASK_MISC	0x0024	W	0x0000FFFF	Interrupt Mask Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_MASK_PMC	0x0028	W	0x000001FF	Interrupt Mask Register Related Power Management Control
PCIE_CLIENT_POWER_CON	0x002C	W	0x00000008	Power Management Control Register
PCIE_CLIENT_POWER_STATUS	0x0030	W	0x00000000	Power Management Status Register
PCIE_CLIENT_MSG_GEN_CON	0x0034	W	0x00000000	Message Generation Control Register
PCIE_CLIENT_MSI_GEN_CON	0x0038	W	0x00000000	MSI Generation Control Register
PCIE_CLIENT_MSI_GEN_FNUM_TC	0x0040	W	0x00000000	MSI Function Number and TC set Register
PCIE_CLIENT_RBAR_SIZE_INFO0	0x0044	W	0x00000000	Resizable BAR2 to BAR0 Size Information Register
PCIE_CLIENT_RBAR_SIZE_INFO1	0x0048	W	0x00000000	Resizable BAR5 to BAR3 Size Information Register
PCIE_CLIENT_DMA_HSHAKE_TOGG	0x004C	W	0x00000000	DMA Handshake Toggle Register
PCIE_CLIENT_VEN_MSG_RX_INFO0	0x0050	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_RX_INFO1	0x0054	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_RX_INFO2	0x0058	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_TX_CFG0	0x005C	W	0x00000000	Vendor Message Transmit Configuration Register 0
PCIE_CLIENT_VEN_MSG_TX_CFG1	0x0060	W	0x00000000	Vendor Message Transmit Configuration Register 1
PCIE_CLIENT_VEN_MSG_TX_CFG2	0x0064	W	0x00000000	Vendor Message Transmit Configuration Register 2
PCIE_CLIENT_LTR_MSG_TX_INFO	0x0068	W	0x00000000	LTR Message Transmit Data Register
PCIE_CLIENT_APP_ERR_RPT_INFO0	0x006C	W	0x00000000	Application Error Report Information Register 0
PCIE_CLIENT_APP_ERR_RPT_INFO1	0x0070	W	0x00000000	Application Error Report Information Register 1
PCIE_CLIENT_APP_ERR_RPT_INFO2	0x0074	W	0x00000000	Application Error Report Information Register 2
PCIE_CLIENT_APP_ERR_RPT_INFO3	0x0078	W	0x00000000	Application Error Report Information Register 3
PCIE_CLIENT_APP_ERR_RPT_INFO4	0x007C	W	0x00000000	Application Error Report Information Register 4
PCIE_CLIENT_OBFF_WAKE_ELE_CFG	0x0080	W	0xB4F05064	OBFF Wake Configuration Register
PCIE_CLIENT_OBFF_WAKE_DEBUG	0x0084	W	0x00000000	OBFF Wake Decoder Debug Register
PCIE_CLIENT_RX_CPL_TIME_OUT_INFO	0x0088	W	0x00000000	RX CPL Timeout Information

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Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_TX_CPL_TIME_OUT_INFO0	0x008C	W	0x00000000	TX CPL Timeout Information 0
PCIE_CLIENT_TX_CPL_TIME_OUT_INFO1	0x0090	W	0x00000000	TX CPL Timeout Information 1
PCIE_CLIENT_LOCAL_CRU_CTRL	0x009C	W	0x00000000	Local Clock and Reset Control Register
PCIE_CLIENT_GENERAL_DEBUG_CON	0x0100	W	0x00000000	General Debug Control Register
PCIE_CLIENT_GENERAL_DEBUG_INFO	0x0104	W	0x00000000	General Debug Information Register
PCIE_CLIENT_SLC_DEBUG_INFO_CMN	0x0108	W	0x00000000	Silicon Debug Information Common Register
PCIE_CLIENT_SLC_DEBUG_INFO_LN	0x010C	W	0x00000000	Silicon Debug Information Lane N Register
PCIE_CLIENT_SLC_DEBUG_INFO_V0	0x0114	W	0x00000000	Silicon Debug Information Virtual Channel 0 Register
PCIE_CLIENT_DIAG_STATUS_BUS_SEL	0x0118	W	0x00000000	Diagnostic Status Bus Select Register
PCIE_CLIENT_DIAG_STATUS_BUS_INFO	0x011C	W	0x00000000	Diagnostic Status Bus Information Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_CON	0x0140	W	0x00000000	CDM RASDES Control Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_CMN	0x0144	W	0x00000000	CDM RASDES Information Common Data Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_LN	0x0148	W	0x00000000	Lane N CDM RASDES Information Register
PCIE_CLIENT_CDM_RASDES_TBA_CON	0x0150	W	0x00000000	CDM RASDES TBA Control Register
PCIE_CLIENT_CDM_RASDES_TBA_INFO_CMN	0x0154	W	0x00000000	CDM RASDES TBA Common Information Register
PCIE_CLIENT_HOT_RESET_CTRL	0x0180	W	0x00000000	Hot Reset Control Register
PCIE_CLIENT_INTR_EN_MSG_RX	0x0190	W	0x00007737	Interrupt Enable Register Related to Message Reception
PCIE_CLIENT_INTR_EN_LEGACY	0x0194	W	0x000000FF	Interrupt Enable Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_EN_ERR	0x0198	W	0x0000177F	Interrupt Enable Register Related to Error Detection
PCIE_CLIENT_INTR_EN_MISC	0x019C	W	0x0000FFFF	Interrupt Enable Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_EN_PMC	0x01A0	W	0x000001FF	Interrupt Enable Register Related Power Management Control
PCIE_CLIENT_MSI_INT_RX_VEC	0x01C0	W	0x00000000	MSI Interrupt Vector
PCIE_CLIENT_AXI_MSTR_MISC_CON	0x0200	W	0x00000000	AXI Master Sideband Signals Control Register
PCIE_CLIENT_AXI_SLV_ATU_BYPASS	0x0204	W	0x00000000	Address Translate Unit Bypass set Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR	0x0208	W	0x00000000	AXI Slave Write Address Sideband Signals HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR3	0x020C	W	0x00000000	AXI Slave Write Address Sideband Signals 3rd HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR4	0x0210	W	0x00000000	AXI Slave Write Address Sideband Signals 4th HDR Register

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Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_AXI_SLV_AWMISC_TAG	0x0214	W	0x00000000	AXI Slave Write Request Tag Register
PCIE_CLIENT_AXI_SLV_MISC_INFO	0x0218	W	0x00000000	AXI Slave Read Address and Write Data Sideband Signals Control Register
PCIE_CLIENT_AXI_SLV_AW_TLP_PRFX	0x0220	W	0x00000000	AXI Slave Write TLP Prefix
PCIE_CLIENT_AXI_SLV_AR_TLP_PRFX	0x0224	W	0x00000000	AXI Slave Read TLP Prefix
PCIE_CLIENT_DBI_MISC_CON	0x0270	W	0x00000000	DBI Miscellaneous Control Register
PCIE_CLIENT_PORT_BDF	0x0274	W	0x00000000	Port BDF Register
PCIE_CLIENT_LTSSM_STATUS	0x0300	W	0x00000000	LTSSM Status Register
PCIE_CLIENT_DBG_FIFO_MODE_CON	0x0310	W	0x00000000	Debug FIFO Mode Control Register
PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA0	0x0320	W	0x00000000	Debug FIFO Pattern hit Data Register 0
PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA1	0x0324	W	0x00000000	Debug FIFO Pattern hit Data Register 1
PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA0	0x0328	W	0x00000000	Debug FIFO Transition Pattern hit Data Register 0
PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA1	0x032C	W	0x00000000	Debug FIFO Transition Pattern hit Data Register 1
PCIE_CLIENT_DBG_FIFO_STATUS	0x0350	W	0x00000000	Debug FIFO Status Register
PCIE_CLIENT_CFG_ERR_STATUS	0x0354	W	0x00000000	Configuration Error Status
PCIE_CLIENT_TLP_PRFX_LOG0	0x0380	W	0x00000000	TLP Prefixes Log Register 0
PCIE_CLIENT_TLP_PRFX_LOG1	0x0384	W	0x00000000	TLP Prefixes Log Register 1
PCIE_CLIENT_TLP_PRFX_LOG2	0x0388	W	0x00000000	TLP Prefixes Log Register 2
PCIE_CLIENT_TLP_PRFX_LOG3	0x038C	W	0x00000000	TLP Prefixes Log Register 3
PCIE_CLIENT_CLIENT_VER	0x0800	W	0x00050611	Client Version Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.2.2 Detail Registers Description

PCIE_CLIENT_GENERAL_CON

Address: Operational Base(0xFF500000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	mem_auto_clk_gating_disable Control the memory auto clock gating when it is inactive. 1'b0: Auto gating enable 1'b1: Auto gating disable

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Bit	Attr	Reset Value	Description
13	RW	0x0	link_req_rst_grt_sel Link down reset request grant control select: 1'b1: From client grf GENERAL_CON bit 3 1'b0: From pcie grf PCIE_CON0 bit 2 Reserved after r5p6 (version 50600).
12	R/WSC	0x0	app_hdr_valid Alias "app_err_report" in old client version. One-clock-cycle pulse indicating that the data app_hdr_log, app_err_bus, app_err_func_num, and app_tlp_prfx_log is valid. Set 1 to report application error to controller. It is a self-clear bit to generate a pulse to controller. Application should provide error information in VEN_ERR_INFOx registers before setting this bit.
11	RW	0x0	app_sris_mode SRIS operating mode 1'b0: non-SRIS mode 1'b1: SRIS mode
10	RW	0x0	app_dbi_ro_wr_disable DBI Read-only Write Disable 1'b0: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is read-write. 1'b1: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is forced to 0 and is read-only
9	RW	0x0	tx_lane_flip_en Performs manual lane reversal for transmit lanes. For use whenautomatic lane reversal does not occur because lane 0 is not detected. In most cases, tx_lane_flip_en should be wired to a static value at thechip level. For more information, see 'Lane Reversal and Broken Lanes'. This signal is only used in Conventional PCIe mode. When in M-PCIe mode, mpcie_tx_lane_flip_en is used. 1'b0: Disable 1'b1: Enable
8	RW	0x0	rx_lane_flip_en Performs manual lane reversal for receive lanes. For use when automatic lane reversal does not occur because lane 0 is not detected. In most cases, rx_lane_flip_en should be wired to a static value at the chip level. For more information, see 'Lane Reversal and Broken Lanes'. This signal is only used in Conventional PCIe mode. When in M-PCIe mode, mpcie_rx_lane_flip_en is used. 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	device_type Device/port type. Indicates the specific type of this PCI Express function. It is also used to set the 'Device/Port Type' field of the 'PCI Express Capabilities Register'. The controller uses this input to determine the operating mode of the controller at run time. Defined encodings are: 4'h0: PCI Express endpoint 4'h1: Legacy PCI Express endpoint 4'h4: Root port of PCI Express root complex
3	RW	0x0	link_req_rst_grt Link down reset request grant control. 1'b0: Disable link down reset request grant 1'b1: Enable link down reset request grant Reserved after r5p6(version 50600).

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Bit	Attr	Reset Value	Description
2	RW	0x0	app_ltssm_enable Driven low by your application after cold, warm, or hot reset to hold the LTSSM in the Detect state until your application is ready for the link training to begin. When your application has finished reprogramming the controller configuration registers using the DBI, it asserts app_ltssm_enable to allow the LTSSM to continue link establishment. Can also be used to delay hot resetting of the controller until you have read out any register status.
1	RW	0x0	app_req_retry_en Provides a capability to defer incoming configuration requests until initialization is complete. When app_req_retry_en is asserted, the controller completes incoming configuration requests with a configuration request retry status. Other incoming requests are not affected. When the Readiness Notification mechanism is supported, DRS messaging is blocked when app_req_retry_en=1. When app_req_retry_en=0 and app_drs_ready=1, the controller autonomously transmits a DRS message when the link transitions from DL_Down to DL_Up.
0	R/WSC	0x0	app_init_rst Request from your application to send a hot reset to the upstream port. The hot reset request is sent when a single cycle pulse is applied to this pin. In an upstream port, you should set this input to '0'.

PCIE_CLIENT_INTR_STATUS_MSG_RX

Address: Operational Base(0xFF500000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	W1C	0x0	obff_cpu_active_int Interrupt indicates that the controller received an 'CPU Active' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. One-clock-cycle pulse that indicates that the controller received a 'CPU Active' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.
13	W1C	0x0	obff_obff_int Interrupt indicates that the controller received an 'OBFF' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. if cfg_obff_en is not equal to 2'b11, then radm_msg_obff One-clock-cycle pulse that indicates that the controller received an 'OBFF' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.

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Bit	Attr	Reset Value	Description
12	W1C	0x0	obff_idle_int Interrupt indicates that the controller received an 'IDLE' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. if cfg_obff_en is not equal to 2'b11, then radm_msg_idle One-clock-cycle pulse that indicates that the controller received an 'IDLE' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.
11	RO	0x0	reserved
10	W1C	0x0	pm_turnoff_int Interrupt indicates that the controller received a PME Turnoff message. 1'b0: No interrupt 1'b1: Interrupt EP mode only. radm_pm_turnoff One-clock-cycle pulse that indicates that the controller received a PME Turnoff message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no indication is given for the second message.
9	W1C	0x0	pm_to_ack_int Interrupt indicates that the controller received a PME_TO_Ack message. 1'b0: No interrupt 1'b1: Interrupt RC mode only. radm_pm_to_ackOne-clock-cycle pulse that indicates that the controller received a PME_TO_Ack message. Upstream port: Reserved.
8	W1C	0x0	pm_pme_int Interrupt indicates that the controller received a PM_PME message. 1'b0: No interrupt 1'b1: Interrupt RC mode only. radm_pm_pme One-clock-cycle pulse that indicates that the controller received a PM_PME message.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	W1C	0x0	cfg_pme_msi_int Interrupt that indicates the controller received a cfg_pme_msi pulse. 1'b0: No interrupt 1'b1: Interrupt cfg_pme_msi asserted when all of the following conditions are true: 1. MSI or MSI-X is enabled. 2. The PME Interrupt Enable bit in Root Control register is set to 1. 3. The PME Status bit in Root Status register is set to 1. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
4	RO	0x0	cfg_pme_int Asserted when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0. 2. The PME Interrupt Enable bit in the Root Control register is set to 1. 3. The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.
3	RO	0x0	reserved
2	W1C	0x0	ltr_msg_int Interrupt that indicates the controller received a LTR message. The LTR message information is available in PL_LTR_LATENCY_OFF registers. 1'b0: No interrupt 1'b1: Interrupt radm_msg_ltr One-clock-cycle pulse that indicates that the controller received an LTR message. The controller makes the message header available the radm_msg_payload output. It is also available the app_ltr_latency output. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
1	W1C	0x0	unlock_msg_int Interrupt indicates that the controller received an unlock message. 1'b0: No interrupt 1'b1: Interrupt radm_msg_unlock One-cycle pulse that indicates that the controller received an Unlock message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.

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Bit	Attr	Reset Value	Description
0	W1C	0x0	ven_msg_int Interrupt that indicates radm_vendor_msg One-cycle pulse is received. The message header is available in VEN_MSG_RX_INFO registers. 1'b0: No interrupt 1'b1: Interrupt radm_vendor_msg One-cycle pulse that indicates the controller received a vendor-defined message. The controller makes the message header available the radm_msg_payload output. When FX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then both bits are asserted.

PCIE_CLIENT_INTR_STATUS_LEGACY

Address: Operational Base(0xFF500000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	tx_intd_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTD Message to the upstream device. The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTD Message to the upstream device. The signal deassert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTD Message to the upstream device. EP mode only.
6	RO	0x0	tx_intc_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTC Message to the upstream device. The signal assert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTC Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTC Message to the upstream device. The signal deassert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTC Message to the upstream device. EP mode only.
5	RO	0x0	tx_intb_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTB Message to the upstream device. The signal assert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTB Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTB Message to the upstream device. The signal deassert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTB Message to the upstream device. EP mode only.

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Bit	Attr	Reset Value	Description
4	RO	0x0	tx_inta_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTA Message to the upstream device. The signal assert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTA Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTA Message to the upstream device. The signal deassert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTA Message to the upstream device. EP mode only.
3	RO	0x0	rx_intd_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTD Message from the downstream device. radm_intd_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTD Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTD Message from the downstream device. radm_intd_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTD Message from the downstream device. RC mode only.
2	RO	0x0	rx_intc_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTC Message from the downstream device. radm_intc_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTC Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTC Message from the downstream device. radm_intc_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTC Message from the downstream device. RC mode only.
1	RO	0x0	rx_intb_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTB Message from the downstream device. radm_intb_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTB Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTB Message from the downstream device. radm_intb_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTB Message from the downstream device. RC mode only.

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Bit	Attr	Reset Value	Description
0	RO	0x0	rx_inta_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTA Message from the downstream device. radm_inta_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTA Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTA Message from the downstream device. radm_inta_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTA Message from the downstream device. RC mode only.

PCIE_CLIENT_INTR_STATUS_ERR

Address: Operational Base(0xFF500000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	W1C	0x0	radm_qoverflow_int Pulse radm_qoverflow indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism 1'b0: No interrupt 1'b1: Interrupt
11	RO	0x0	reserved
10	W1C	0x0	f_err_rx_int One-clock-cycle radm_fatal_err pulse that indicates that the controller received an ERR_FATAL message. 1'b0: No interrupt 1'b1: Interrupt RC mode only.
9	W1C	0x0	nf_err_rx_int One-clock-cycle radm_nonfatal_err pulse that indicates that the controller received an ERR_NONFATAL message. 1'b0: No interrupt 1'b1: Interrupt RC mode only.
8	W1C	0x0	cor_err_rx_int One-clock-cycle radm_correctable_err pulse that indicates that the controller received an ERR_COR message. The controller makes the message header available the radm_msg_payload output. 1'b0: No interrupt 1'b1: Interrupt RC mode only.
7	RO	0x0	reserved
6	W1C	0x0	f_err_sent_int cfg_send_f_err indicates Sent Fatal Error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained a fatal error, and that can not be corrected, has been received by the EndPoint. 1'b0: No interrupt 1'b1: Interrupt EP mode only.

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Bit	Attr	Reset Value	Description
5	W1C	0x0	nf_err_sent_int cfg_send_nf_err indicates Sent Non-Fatal Error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained a non-fatal error, and that can not be corrected, has been received by the EndPoint. 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	cor_err_sent_int cfg_send_cor_err indicates sent correctable error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained an error, and that can be corrected, has been received by the EndPoint 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	tx_cpl_timeout_int trgt_cpl_timeout indicates that the application has not generated a completion for an incoming request within the required time interval. Information about the timed-out completion is available the trgt_timeout_* outputs listed later. When a completion timeout occurs, the controller does not clear the corresponding entry from the completion lookup table. The default completion timeout value is approximately 10 ms. 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	rx_cpl_timeout_int radm_cpl_timeout indicates that the completion TLP for a request has not been received within the expected time window. 1'b0: No interrupt 1'b1: Interrupt Can find the timed-out completion information in RX_CPL_TIME_OUT_INFO register.
1	W1C	0x0	aer_rc_err_msi The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: 1. MSI or MSI-X is enabled. 2. A reported error condition causes a bit to be set in the Root Error Status register. 3. The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. RC mode only.
0	RO	0x0	aer_rc_err_int Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred. Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi. RC mode only.

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PCIE_CLIENT_INTR_STATUS_MISC

Address: Operational Base(0xFF500000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ep_elbi_app_int Interrupt generated by ELBI application register access. 1'b0: No interrupt 1'b1: Interrupt
14	RO	0x0	link_eq_req_int Interrupt indicating to your application that the Link Equalization Request bit in the Link Status 2 Register has been set and the Link Equalization Request Interrupt Enable (Link Control 3 Register bit 1) is set. cfg_link_eq_req_int 1'b1: Interrupt 1'b0: No interrupt
13	W1C	0x0	rbar_update_int Indicates that a resizable BAR control register has been updated: 1 bit per Physical function. 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	dpa_sub_upd_int DPA Substate-Updated Indication Signal Bus. The controller asserts "dpa_substate_update" for one core_clk cycle when the Substate Control field of the DPA Control Register has been updated with a new value for the associated function. The controller asserts it when the updated value of the Substate Control field does not match the Substate Status field of the Status Register when the Substate Control Enable bit field of the Status Register is set to "1". Note: Your application logic is required to do the following: 1. Detect the one cycle pulse on the signal for the relevant function. 2. Read the function's substate control register to determine the software's target substate (transition). 3. Read the function's transition latency value, unit, and indicator. Calculate the maximum transition latency for the substate transition. 4. Execute the substate transition and complete it within the maximum transition latency. 5. Update the substate status after completing the transition through a DBI write. The controller updates the substate status during the substate transition if the transition is from a lower power substate to a higher; the status is the higher power substate during the substate transition.
11	RO	0x0	edma_rd_int DMA read channel interrupt. Indicates that the DMA transfer has completed or that an error has occurred. This is a level interrupt. For more information, see 'Interrupts and Error Handling'. 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
10	RO	0x0	edma_wr_int DMA write channel interrupt. Indicates that the DMA transfer has completed or that an error has occurred. This is a level interrupt. For more information, see 'Interrupts and Error Handling'. 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	bw_mgt_msi The controller sets this pin when following conditions are true: 1. MSI or MSI-X is enabled. 2. The Link Bandwidth Management Status register (Link Control Status register bit 14) is updated 3. The Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set. reuse-pragma begin Attr Description This pin is set as a notification when the Link Bandwidth Management Status register (Link Status register bit 14) is updated and the Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set and in addition the msi or msix are enabled. This bit is not applicable to, and is reserved, for endpoint devices and upstream ports of Switches. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.
8	RO	0x0	bw_mgt_int The controller asserts cfg_bw_mgt_int when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0, and 2. The Bandwidth Management Interrupt Enable bit in the Link Control register is set to 1, and 3. The Bandwidth Management Interrupt Status bit in the Link Status register is set to 1. The cfg_bw_mgt_msi output is a pulse signal (only asserted for one clock cycle); but cfg_bw_mgt_int is a level signal. For upstream port: Reserved.
7	W1C	0x0	link_auto_bw_msi The controller sets this pin when following conditions are true: 1. MSI or MSI-X is enabled. 2. The Link Autonomous Bandwidth Status register (Link Status register bit 15) is updated. 3. The Link Autonomous Bandwidth Interrupt Enable (Link Control register bit 11) is set. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.

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Bit	Attr	Reset Value	Description
6	RO	0x0	link_auto_bw_int The controller asserts cfg_link_auto_bw_int when all of the following conditions are true: 1. The INTx assertion disable bit in the Command register is 0, and 2. The Link Autonomous Bandwidth Interrupt Enable bit in the Link Control register is set to 1, and 3. The Link Autonomous Bandwidth Interrupt Status bit in the Link Status register is set to 1. The cfg_link_auto_bw_msi output is a pulse signal (only asserted for one clock cycle); but cfg_link_auto_bw_int is a level signal. For upstream port: Reserved.
5	W1C	0x0	hp_msi The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: 1. MSI or MSI-X is enabled. 2. Hot-Plug interrupts are enabled in the Slot Control register. 3. Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).
4	RO	0x0	hp_int The controller asserts hp_int when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0. 2. Hot-Plug interrupts are enabled in the Slot Control register. 3. Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.
3	W1C	0x0	hp_pme_int The controller asserts hp_pme when all of the following conditions are true: 1. The PME Enable bit in the Power Management Control and Status register is set to 1. 2. Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled.

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Bit	Attr	Reset Value	Description
2	W1C	0x0	link_req_rst_not_int Early version of the link_req_rst_not signal. For more information, see the 'Warm and Hot Resets' section in the Architecture chapter of the Databook. smlh_req_rst_not. 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	dll_link_up_int Data link layer up/down indicator (rdlh_link_up): This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Link is down 1'b1: Link is up
0	W1C	0x0	phy_link_up_int PHY "smlh_link_up" Link up/down indicator. 1'b0: Link is down 1'b1: Link is up

PCIE_CLIENT_INTR_STATUS_PMC

Address: Operational Base(0xFF500000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	W1C	0x0	pm_dstate_update_int Interrupt indicates that the current power management D-state have changed. The current power management D-state of pm_dstate the function: 1. 000b: D0 2. 001b: D1 3. 010b: D2 4. 011b: D3 5. 100b: Uninitialized 6. Other values: Not applicable There are 3 bits of pm_dstate for each configured function. 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	linkst_out_l0s_int Power management is in L0s state. Indicates in L0_STALL state when M-PCIe Interrupt that indicates link has entered L0s state (falling edge detected of pm_linkst_in_l0s in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	linkst_out_l2_int Power management is in L2 state. Interrupt that indicates link has entered L2 state (falling edge detected of pm_linkst_in_l2 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	linkst_out_l1_int Power management is in L1 state. Interrupt that indicates link has entered L1 state (falling edge detected of pm_linkst_in_l1 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
4	W1C	0x0	linkst_out_l1sub_int Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used in DWC_pcie_clkrst.v (see 'Clock Generation and Gating Design Example') to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. Interrupt indicates link has entered L1 substate (falling edge detected of pm_linkst_in_l1sub in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	linkst_in_l0s_int Power management is in L0s state. Indicates in L0_STALL state when M-PCIe Interrupt that indicates link has entered L0s state (rising edge detected of pm_linkst_in_l0s in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	linkst_in_l2_int Power management is in L2 state. Interrupt that indicates link has entered L2 state (rising edge detected of pm_linkst_in_l2 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	linkst_in_l1_int Power management is in L1 state. Interrupt that indicates link has entered L1 state (rising edge detected of pm_linkst_in_l1 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	linkst_in_l1sub_int Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used in (see 'Clock Generation and Gating Design Example') to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. Interrupt indicates link has entered L1 substate (rising edge detected of pm_linkst_in_l1sub in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt

PCIE_CLIENT_INTR_MASK_MSG_RX

Address: Operational Base(0xFF500000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x1	obff_cpu_active_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
13	RW	0x1	obff_obff_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
12	RW	0x1	obff_idle_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RO	0x0	reserved
10	RW	0x1	pm_turnoff_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	pm_to_ack_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
8	RW	0x1	pm_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7:6	RO	0x0	reserved
5	RW	0x1	cfg_pme_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	cfg_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RO	0x0	reserved
2	RW	0x1	ltr_msg_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	unlock_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	ven_msg_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_LEGACY

Address: Operational Base(0xFF500000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x1	tx_intd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	tx_intc_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	tx_intb_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	tx_inta_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	rx_intd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
2	RW	0x1	rx_intc_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	rx_intb_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	rx_inta_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_ERR

Address: Operational Base(0xFF500000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	radm_qoverflow_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RO	0x0	reserved
10	RW	0x1	f_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	nf_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
8	RW	0x1	cor_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7	RO	0x0	reserved
6	RW	0x1	f_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	nf_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	cor_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	tx_cpl_timeout_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
2	RW	0x1	rx_cpl_timeout_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	aer_rc_err_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	aer_rc_err_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_MISC

Address: Operational Base(0xFF500000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	ep_elbi_app_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
14	RW	0x1	link_eq_req_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
13	RW	0x1	rbar_update_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
12	RW	0x1	dpa_sub_upd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RW	0x1	edma_rd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
10	RW	0x1	edma_wr_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	bw_mgt_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
8	RW	0x1	bw_mgt_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7	RW	0x1	link_auto_bw_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	link_auto_bw_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	hp_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	hp_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	hp_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
2	RW	0x1	link_req_rst_not_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	dll_link_up_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	phy_link_up_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_PMC

Address: Operational Base(0xFF500000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	pm_dstate_update_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7	RW	0x1	linkst_out_l0s_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	linkst_out_l2_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	linkst_out_l1_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	linkst_out_l1sub_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	linkst_in_l0s_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
2	RW	0x1	linkst_in_l2_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	linkst_in_l1_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	linkst_in_l1sub_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_POWER_CON

Address: Operational Base(0xFF500000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_req_n_con Valid when clk_req_n_bypass set to 1. 1'b1: Tristate CLKREQ# 1'b0: Pull down CLKREQ#

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Bit	Attr	Reset Value	Description
12	RW	0x0	clk_req_n_bypass 1'b0: clk_req_n does not bypass, CLKREQ# driven by controller 1'b1: clk_req_n bypass, CLKREQ# driven by bit 13 of POWER_CON
11:10	RW	0x0	p2_cpm_disable 2'b00: When phy in P2 power state, enable clock PM for both L1 and L2 2'b01: When phy in P2 power state, enable clock PM for L2 but disable for L1 2'b10: When phy in P2 power state, disable clock PM for L2 but enable for L1 2'b11: When phy in P2 power state, disable clock PM for both L1 and L2 Reserved after r5p6(version 50600).
9	RW	0x0	app_clk_pm_en Clock PM feature enabled by application. Used to inhibit the programming of the Clock PM in Link Control Register. For more information, see 'L1 with Clock PM (L1 with REFCLK removal/PLL Off)'.
8	RW	0x0	sys_aux_pwr_det Auxiliary Power Detected. Used to report to the host software that auxiliary power (Vaux) is present. 1'b0: Auxiliary power is not present 1'b1: Auxiliary power is present
7	RO	0x0	reserved
6	RW	0x0	app_l1sub_disable The application can set this input to 1'b1 to prevent entry to L1 Sub-states. This pin is used to gate the L1 sub-state enable bits from the L1 PM Substates Control 1 Register.
5	RW	0x0	app_xfer_pending Indicates that your application has transfers pending. 1'b1: There are transactions outside the controller that the controller needs to transmit. For EP mode, prevents generation of requests to enter L1. Triggers exit if already in L1. For RC mode, triggers exit if already in L1. 1'b0: There are no transactions outside the controller. Indicates that your application has transfers pending and prevents the controller from entering L1. If the entry into L1 is already in progress, assertion of app_xfer_pending causes an exit from L1. This is a level signal used to inform the controller about the state of external queues and pipeline stages that contain transactions to be transmitted by the controller. The controller uses this information to determine when to enter/exit L1. When this signal is asserted, it indicates that there are transactions outside the controller that the controller needs to transmit. When de-asserted, it indicates that there are no transactions outside the controller. The controller responds to an assertion on this signal as follows: 1. Upstream Ports: Prevents generation of requests to enter L1. Triggers exit if already in L1. 2. Downstream Ports: Triggers exit if already in L1. You can instruct the controller to exit L1 by asserting either or both of app_xfer_pending and app_req_exit_l1. The controller only samples app_req_exit_l1 when the controller is already in the L1 state.

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Bit	Attr	Reset Value	Description
4	R/WSC	0x0	app_req_exit_l1 1'b0: Self clear to generate a pulse to controller. 1'b1: Application request to Exit L1. Application request to Exit L1. Request from your application to exit L1. It is only effective when L1 is enabled.
3	RW	0x1	app_ready_entr_l23 1'b0: Application not ready to enter L23. 1'b1: Application ready to enter L23. Application Ready to Enter L23. Indication from your application that it is ready to enter the L23 state. The app_ready_entr_l23 signal is provided for applications that must control L23 entry (in case certain tasks must be performed before going into L23). The controller delays sending PM_Enter_L23 (in response to PM_Turn_Off) until this signal becomes active. When this signal has been asserted by the application, it must be kept asserted until L2 entry has completed. Hardwire to 1 for applications that do not require this feature. Note: The controller ignores this input in RC mode.
2	R/WSC	0x0	app_req_entr_l1 Application request to Enter L1 ASPM state. 1'b0: Self clear to generate a pulse to controller 1'b1: Application request to enter L1 state Application request to Enter L1 ASPM state. The app_req_entr_l1 signal is for use by applications that need to control L1 entry instead of using the L1 entry timer as defined in the PCI Express Specification. It is only effective when L1 is enabled. The controller latches this request when in L0 or L0s; to be acted upon later. Note: The controller ignores this input in RC mode.
1	R/WSC	0x0	app_pm_xmt_pme Wake Up. If PME is enabled and PME support is configured for current PMCSR D-state asserting this signal (apps_pm_xmt_pme) causes the controller to wake from either L1 or L2 state. When the controller has transitioned back to the L0 state it transmits a PME message and set the PME_Status. Upon receiving the PME message the root complex should clear the PME_Status and change the D-state back to D0.
0	RW	0x0	app_clk_req_n Indicates that the application logic is ready to have reference clock removed. In designs which support reference clock removal through either L1 PM Sub-states or L1 CPM, the application should set this signal to 1'b1 if it supports reference clock removal. If the application does not want to remove reference clock it should set this signal to 1'b0. This signal should be asserted or de-asserted when L1 CPM or L1 Sub-states are being configured, it should not be changed dynamically during L1. Indicates that the application is ready to have reference clock removed. 1'b0: Application does not want to remove reference clock 1'b1: Application is ready to have reference clock removed

PCIE_CLIENT_POWER_STATUS

Address: Operational Base(0xFF500000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28	RO	0x0	pm_clkreq_in Status of wire CLKREQ# GPIO.
27	RO	0x0	pm_clkreq_out Status of CLKREQ# output drive signal.
26	RO	0x0	pm_wake_in Status of wire WAKE# GPIO.
25	RO	0x0	pm_wake_out The wake state of the wake_out 1'b0: Controller is not in wake process or Link already back to L0 1'b1: Controller assert WAKE# signal to request to make link back to L0 EP only.
24	RO	0x0	pm_linkst_in_l0s Power management is in L0s state. 1'b0: Power management is not in L0s. 1'b1: Power management is in L0s.
23	RO	0x0	pm_linkst_in_l2 Power management is in L2 state. 1'b0: Power management is not in L2 1'b1: Power management is in L2
22	RO	0x0	pm_linkst_in_l1 Power management is in L1 state. 1'b0: Power management is not in L1 1'b1: Power management is in L1
21	RO	0x0	pm_linkst_in_l1sub Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used in (see 'Clock Generation and Gating Design Example') to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. 1'b0: Power management is not in L1 substate 1'b1: Power management is in L1 substate
20	RO	0x0	reserved
19:17	RO	0x0	pm_l1sub_state Power management L1 sub-states FSM state. For debugging purposes, not for system operation. 3'b000: L1_U 3'b001: L1_0 3'b010: L1_0_WAIT4_ACK 3'b011: L1_0_WAIT4_CLKREQ 3'b100: L1_N_ENTRY 3'b101: L1_N 3'b110: L1_N_EXIT 3'b111: L1_N_ABORT
16:15	RO	0x0	reserved
14:10	RO	0x00	pm_slave_state Power management slave FSM state. For debugging purposes, not for system operation.
9	RO	0x0	reserved
8:4	RO	0x00	pm_master_state Power management master FSM state. For debugging purposes, not for system operation.

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Bit	Attr	Reset Value	Description
3	RO	0x0	reserved
2:0	RO	0x0	pm_currnt_state Indicates the current power state. For debugging purposes, not for system operation.

PCIE_CLIENT_MSG_GEN_CON

Address: Operational Base(0xFF500000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	R/W SC	0x0	obff_cpu_active_msg_req Request controller to generate a "CPU Active" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
13	R/W SC	0x0	obff_obff_msg_req Request controller to generate a "OBFF" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
12	R/W SC	0x0	obff_idle_msg_req Request controller to generate a "IDLE" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
11:9	RO	0x0	reserved
8	R/W SC	0x0	app_ltr_msg_req Indicates that your application is requesting to send an LTR message. Once asserted, app_ ltr_msg_req must remain asserted until the controller asserts app_ltr_msg_grant. Set to request controller to send a LTR Message. This bit clears automatically when request is granted by controller. Application should put LTR message information ready in LTR_MSG_TX_INFO register before setting this bit.
7:6	RO	0x0	reserved
5	R/W SC	0x0	app_unlock_msg Request from your application to generate an Unlock message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.
4	R/W SC	0x0	apps_pm_xmt_turnoff Request from your application to generate a PM_Turn_Off message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	legacy_int_req When legacy_int_req (sys_int) goes from low to high, the controller generates an Assert_INTx Message. When sys_int goes from high to low, the controller generates a Deassert_INTx Message. There is a separate sys_int input bit for each function in your controller configuration. The Interrupt Pin register for the corresponding function determines which INTx Message the controller generates (INTA, INTB, INTC, or INTD). Legacy and native PCIe devices capable of generating an interrupt must support both Assert_INTx/Deassert_INTx and MSI or MSI-X. sys_int is intended to generate a message that emulates the legacy PCI Interrupts.
0	R/W SC	0x0	ven_msg_req Set to request controller to send a vendor-defined Message. This bit clears automatically when request is granted by controller. Application should put vendor message information ready in VEN_MSG_TX_CFGx registers before setting this bit. Request from your application to send a vendor-defined Message. Once asserted, ven_msg_req must remain asserted until the controller asserts ven_msg_grant.

PCIE_CLIENT_MSI_GEN_CON

Address: Operational Base(0xFF500000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	R/W SC	0x00000000	msi_gen_req 32 bits write only MSI generation request signals. MSB has the highest priority and LSB has the lowest priority. Write 1 to a certain bit request the controller send a MSI interrupt. Software should use MSI capability register to access MSI mask or pending status.

PCIE_CLIENT_MSI_GEN_FNUM_TC

Address: Operational Base(0xFF500000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	ven_msi_tc Traffic Class of the MSI request, valid when ven_msi_req is asserted.
3	RO	0x0	reserved
2:0	RW	0x0	ven_msi_func_num The function number of the MSI request.

PCIE_CLIENT_RBAR_SIZE_INFO0

Address: Operational Base(0xFF500000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	bar2_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RO	0x00	bar1_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
7:6	RO	0x0	reserved
5:0	RO	0x00	bar0_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.

PCIE_CLIENT_RBAR_SIZE_INFO1

Address: Operational Base(0xFF500000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	bar5_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
15:14	RO	0x0	reserved
13:8	RO	0x00	bar4_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
7:6	RO	0x0	reserved
5:0	RO	0x00	bar3_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.

PCIE_CLIENT_DMA_HSHAKE_TOGG

Address: Operational Base(0xFF500000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	dma_rdxfer_done_togg DMA read engine descriptor transfer done toggle signal. One bit for each implemented DMA read channel. After a doorbell command, this signal is de-asserted. When a channel is operating in non-linked list mode this signal does not toggles.
11:8	RO	0x0	dma_wdxfer_done_togg DMA write engine descriptor transfer done toggle signal. One bit for each implemented DMA write channel. After a doorbell command, this signal is de-asserted. When a channel is operating in non-linked list mode this signal does not toggles.
7:4	RW	0x0	app_rdxfer_go_togg DMA read engine descriptor transfer go toggle signal. One bit for each implemented DMA read channel. This signal is ignored whenever a DMA channel operates in non-linked mode.
3:0	RW	0x0	app_wdxfer_go_togg DMA Write engine descriptor transfer go toggle signal. One bit for each implemented DMA write channel. This signal is ignored whenever a DMA channel operates in non-linked mode.

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PCIE_CLIENT_VEN_MSG_RX_INFO0

Address: Operational Base(0xFF500000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	ven_msg_req_id The requester ID of the received Message(radm_msg_req_id). Bit[15:8]: Bus number Bit[7:3]: Device number Bit[2:0]: Function number

PCIE_CLIENT_VEN_MSG_RX_INFO1

Address: Operational Base(0xFF500000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ven_msg_header_l The third double word of the Vendor Defined Message header. Received message header information. When a vendor-defined or ltr message is received (radm_vendor_msg=1 or radm_ltr_msg=1), the controller maps radm_msg_payload to the Rx TLP header dwords as follows: When RX_TLP =1 Bit[31:0] = bytes 12-15 (4th dword), where [7:0] =byte 15 Bit[63:32] = bytes 8-11 (3rd dword)

PCIE_CLIENT_VEN_MSG_RX_INFO2

Address: Operational Base(0xFF500000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ven_msg_header_h The fourth double word of the Vendor Defined Message header. Received message header information. When a vendor-defined or ltr message is received (radm_vendor_msg=1 or radm_ltr_msg=1), the controller maps radm_msg_payload to the Rx TLP header dwords as follows: When RX_TLP =1 Bit[31:0] = bytes 12-15 (4th dword), where [7:0] =byte 15 Bit[63:32] = bytes 8-11 (3rd dword)

PCIE_CLIENT_VEN_MSG_TX_CFG0

Address: Operational Base(0xFF500000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	ven_msg_code The Message Code for the vendor-defined Message TLP.
23:16	RW	0x00	ven_msg_tag Tag for the vendor-defined Message TLP.
15:11	RO	0x00	reserved
10:9	RW	0x0	ven_msg_attr The Attributes field for the vendor-defined Message TLP. bit1: Relaxed ordering. bit0: No snoop.
8	RW	0x0	ven_msg_ep The Poisoned TLP (EP) bit for the vendor-defined Message TLP.
7:5	RW	0x0	ven_msg_tc The Traffic Class field for the vendor-defined Message TLP.
4:0	RW	0x00	ven_msg_type The TYPE field for the vendor-defined Message TLP.

PCIE_CLIENT_VEN_MSG_TX_CFG1

Address: Operational Base(0xFF500000) + offset (0x0060)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ven_msg_data_l The third double word of the Vendor Defined Message header. Third and fourth dwords of the Vendor Defined Message header where: 1. Bytes 8-11 (third header dword) =ven_msg_data[63:32] 2. Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15 For more information, see the 'Endianness' advanced information chapter.

PCIE_CLIENT_VEN_MSG_TX_CFG2

Address: Operational Base(0xFF500000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ven_msg_data_h The fourth double word of the Vendor Defined Message header. Third and fourth dwords of the Vendor Defined Message header where: 1. Bytes 8-11 (third header dword) =ven_msg_data[63:32] 2. Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15 For more information, see the 'Endianness' advanced information chapter.

PCIE_CLIENT_LTR_MSG_TX_INFO

Address: Operational Base(0xFF500000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_ltr_msg_latency LTR message that your application is requesting to send. The message format is defined in the PCI Express Specification.

PCIE_CLIENT_APP_ERR_RPT_INFO0

Address: Operational Base(0xFF500000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log0 The header(bit 0 to bit 31) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO1

Address: Operational Base(0xFF500000) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log1 The header(bit 32 to bit 63) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO2

Address: Operational Base(0xFF500000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log2 The header(bit 64 to bit 95) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO3

Address: Operational Base(0xFF500000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log3 The header (bit 96 to bit 127) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO4

Address: Operational Base(0xFF500000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	app_err_advisory Indicates that your application error is an advisory error. Your application should assert app_err_advisory under either of the following conditions: 1. The controller is configured to mask completion timeout errors, your application is reporting a completion timeout error app_err_bus, and your application intends to resend the request. In such cases the error is an advisory error, as described in PCI Express Specification. When your application does not intend to resend the request, then your application must keep app_err_advisory de-asserted when reporting a completion timeout error. 2. The controller is configured to forward poisoned TLPs to your application and your application is going to treat the poisoned TLP as a normal TLP, as described in PCI Express Specification. Upon receipt of a poisoned TLP, your application must report the error app_err_bus, and either assert app_err_advisory (to indicate an advisory error) or de-assert app_err_advisory (to indicate that your application is dropping the TLP). For more information, see the PCI Express Specification to determine when an application error is an advisory error. 1'b0: Application error is not an advisory error 1'b1: Application error is an advisory error
15:13	RO	0x0	reserved
12:0	RW	0x0000	app_err_bus The type of error that application detected. The controller combines the values err_bus bits with the internally detected error signals to set the corresponding bit in the Un-correctable or Correctable Error Status Registers [0]: Malformed TLP [1]: Receiver Overflow [2]: Unexpected completion [3]: Completer abort [4]: Completion Timeout [5]: Unsupported request [6]: ECRC Check Failed [7]: Poisoned TLP received [8]: AtomicOp Egress Blocked [9]: Un-correctable Internal Error [10]: Corrected Internal Error [11]: TLP Prefix Blocked Error Status: only valid for RC and when CX_NPRFX >0 [12]: ACS Violation: only valid when CX_ACS_ENABLE =1 For more information, see 'Application Error Reporting Interface'.

PCIE_CLIENT_OBFF_WAKE_ELE_CFG

Address: Operational Base(0xFF500000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0xb4	wk_min_f2f_wdt Configure the minimum falling edge to falling edge width. The minimum value Specification define is 700ns. Application set this value equals to wk_min_f2f_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).

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Bit	Attr	Reset Value	Description
23:16	RW	0xf0	wk_max_f2f_wdt Configure the maximum falling edge to falling edge width. The maximum value Specification define is 1000ns. Application set this value equals to wk_max_f2f_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
15:8	RW	0x50	wk_mim_pls_wdt Configure the minimum WAKE# pulse width for both active-inactive-active and inactive-active-inactive pulse. The minimum value Specification define is 300ns. Application set this value equals to wk_mim_pls_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
7:0	RW	0x64	wk_max_pls_wdt Configure the maximum WAKE# pulse width for both active-inactive-active and inactive-active-inactive pulse. The maximum value Specification define is 500ns. Application set this value equals to wk_max_pls_wdt * core_clock_period(8ns in gen1 and 4ns in gen2). Setting this value less than 50% of {wk_max_f2f_wdt * core_clock_period}.

PCIE_CLIENT_OBFF_WAKE_DEBUG

Address: Operational Base(0xFF500000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	obff_wake_dec_err Error state of OBFF decoder FSM, used for debug.
7:4	RO	0x0	obff_wake_dec_state Current state of OBFF decoder FSM, used for debug.
3	RW	0x0	obff_wake_dec_cpu 1'b0: Do not initialize to CPU ACTIVE state 1'b1: Initialize the OBFF decoder to CPU ACTIVE state when obff_wake_dec_init is set
2	RW	0x0	obff_wake_dec_obff 1'b0: Do not initialize to OBFF state 1'b1: Initialize the OBFF decoder to OBFF state when obff_wake_dec_init is set
1	RW	0x0	obff_wake_dec_idle 1'b0: Do not initialize to IDLE state 1'b1: Initialize the OBFF decoder to IDLE state when obff_wake_dec_init is set
0	RW	0x0	obff_wake_dec_init 1'b0: Do not initialize the OBFF decoder 1'b1: Initialize the OBFF decoder

PCIE_CLIENT_RX_CPL_TIME_OUT_INFO

Address: Operational Base(0xFF500000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	radm_timeout_cpl_tag The Tag field of the timeout completion (radm_timeout_cpl_tag).
23:12	RO	0x000	radm_timeout_cpl_len Length (in bytes) of the timeout completion. For a split completion, it indicates the number of bytes remaining to be delivered when the completion timeout (radm_timeout_cpl_len).
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RO	0x0	radm_timeout_cpl_attr The Attributes field of the timeout completion (radm_timeout_cpl_attr).
7	RO	0x0	reserved
6:4	RO	0x0	radm_timeout_cpl_tc The Traffic Class of the timed-out completion (radm_timeout_cpl_tc).
3	RO	0x0	reserved
2:0	RO	0x0	radm_timeout_func_num The function Number of the timed-out completion (radm_timeout_func_num). Function numbering starts at '0'.

PCIE_CLIENT_TX_CPL_TIME_OUT_INFO0

Address: Operational Base(0xFF500000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RO	0x000	trgt_timeout_cpl_len The Length of the timeout completion (trgt_timeout_cpl_len).
11:10	RO	0x0	reserved
9:8	RO	0x0	trgt_timeout_cpl_attr The Attributes value of the timeout completion (trgt_timeout_cpl_attr).
7	RO	0x0	reserved
6:4	RO	0x0	trgt_timeout_cpl_tc The TC of the timeout completion (trgt_timeout_cpl_tc).
3	RO	0x0	reserved
2:0	RO	0x0	trgt_timeout_func_num The function number of the timed-out completion. Function numbering starts at '0' (trgt_timeout_cpl_func_num).

PCIE_CLIENT_TX_CPL_TIME_OUT_INFO1

Address: Operational Base(0xFF500000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	trgt_lookup_empty When this signal is asserted with radm_trgt1_hv, it indicates that the target completion LUT is not full. The application can use this signal to determine a back-pressure mechanism to the controller so that there is not an overflow condition when the number of outstanding non-posted transactions received is more than expected. Your application logic must drive trgt1_radm_halt with the logical OR of your application halt signal and the inverse of this output.
15:8	RO	0x00	trgt_lookup_id The target completion LUT lookup ID for the incoming request TLP. When using the optional target completion lookup table feature, the application must save the lookup ID and assert the same lookup ID client0/1/2_cpl_lookup_id when generating a completion for the request.
7:0	RO	0x00	trgt_timeout_lookup_id The target completion LUT lookup ID of the timeout completion

PCIE_CLIENT_LOCAL_CRU_CTRL

Address: Operational Base(0xFF500000) + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	radm_gate_disable Disable the radm_clk gating in local cru.
12	RW	0x0	aux_gate_disable Disable the aux_clk gating in local cru. Reserved after r5p6 (version 50600)
11	RW	0x0	link_down_gate_disable Disable the link down clock gating in local cru. Reserved after r5p6 (version 50600)
10	RW	0x0	dbi_aclk_gate_disable Disable the dbi_aclk gating in local cru. Reserved after r5p6 (version 50600)
9	RW	0x0	slv_aclk_gate_disable Disable the slv_aclk gating in local cru. Reserved after r5p6 (version 50600)
8	RW	0x0	mstr_aclk_gate_disable Disable the mstr_aclk gating in local cru. Reserved after r5p6 (version 50600)
7:4	RO	0x0	reserved
3	RW	0x0	pcie_pm_phy_req_disable Mask the phy reset request from controller pm. Reserved after r5p6 (version 50600)
2	RW	0x0	pcie_pm_srst_req_disable Mask the sticky reset request from controller pm. Reserved after r5p6 (version 50600)
1	RW	0x0	pcie_pm_nsrst_req_disable Mask the non-sticky reset request from controller pm. Reserved after r5p6 (version 50600)
0	RW	0x0	pcie_pm_crst_req_disable Mask the core reset request from controller pm. Reserved after r5p6 (version 50600)

PCIE_CLIENT_GENERAL_DEBUG_CON

Address: Operational Base(0xFF500000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	sd_hold_ltssm app_ras_des_sd_hold_ltssm Hold and release LTSSM. For as long as this signal is '1', the controller stays in the current LTSSM. 1'b0: Release LTSSM 1'b1: Hold LTSSM

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Bit	Attr	Reset Value	Description
5	RW	0x0	dbg_pba MSIX PBA RAM Debug Mode. Use this input to activate the debug mode and allow direct read/write access to the PBA. You can also use the MSIX_RAM_CTRL_DBG_PBA field in MSIX_RAM_CTRL_OFF to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire array linearly from the base address of the BAR (indicated by the BIR) in function 0. When you assert dbg_table and dbg_pba simultaneously, you can access the traffic class (TC) information bits. For more information, see the Interrupts section in the "Controller Operations" chapter of the Databook.
4	RW	0x0	dbg_table MSIX Table RAM Debug Mode. Use this input to activate the debug mode and allow direct read/write access to the Table. You can also use the MSIX_RAM_CTRL_DBG_TABLE field in MSIX_RAM_CTRL_OFF to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. When you assert dbg_table and dbg_pba simultaneously, you can access the traffic class (TC) information bits. For more information, see the Interrupts section in the "Controller Operations" chapter of the Databook.
3	RO	0x0	reserved
2:0	RW	0x0	diag_ctrl_bus Diagnostic Control Bus 1. x01: Insert LCRC error by inverting the LSB of LCRC 2. x10: Insert ECRC error by inverting the LSB of ECRC 2.1 The rising edge of these two signals ([1:0]) enable the controller to assert an LCRC or ECRC to the packet that it currently being transferred. 2.2 When LCRC or ECRC error packets are transmitted by the controller, the controller asserts diag_status_bus[lcrc_err_asserted] or diag_status_bus[ecrc_err_asserted] to report that the requested action has been completed. This handshake between control and status allows your application to control a specific packet being injected with an CRC or ECRC error. 2.3 The LCRC and ECRC errors are generated by simply inverting the last bit of the LCRC or ECRC value. 3. 1xx: Select Fast Link Mode. 3.1 Sets all internal LTSSM millisecond timers to Fast Mode for speeding up simulation purposes. Forces the LTSSM training (link initialization) to use shorter timeouts and to link up faster. 3.2 The default scaling factor is 1024 for all internal timers. The default scaling factor can be changed using the DEFAULT_FAST_LINK_SCALING_FACTOR parameter or through the FAST_LINK_SCALING_FACTOR field in the TIMER_CTRL_MAX_FUNC_NUM_OFF register. 3.3 Fast Link Mode can also be activated by setting the FAST_LINK_MODE field in the PORT_LINK_CTRL_OFF register. 3.4 For more information, see the "Fast Link Simulation Mode" section in the "Integrating the Controller with the PHY or Application RTL or Verification IP" chapter of the User Guide.

PCIE_CLIENT_GENERAL_DEBUG_INFO

Address: Operational Base(0xFF500000) + offset (0x0104)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	smlh_ltssm_state Current state of the LTSSM.
9	RO	0x0	reserved
8	RO	0x0	radm_q_not_empty Level indicating that the receive queues contain TLP header/data. 1'b0: Receive queues do not contain TLP header/data 1'b1: Receive queues contain TLP header/data
7	RO	0x0	radm_xfer_pending Receive request pending status. Indicates Receive TLP requests are pending, that is, requests sent to the RTRGT1 or RTRGT0 interfaces are awaiting a response from your application. For debugging purposes. 1'b0: Receive TLP requests are not pending 1'b1: Receive TLP requests are pending
6	RO	0x0	edma_xfer_pending eDMA transfer pending status. Indicates eDMA Write or Read Channel transfers are pending, that is, DMA Write or Read Channels have not finished transferring data. For debugging purposes. 1'b0: eDMA DBI transfer not pending 1'b1: eDMA transfer pending
5	RO	0x0	brdg_dbi_xfer_pending AXI Slave DBI transfer pending status. Indicates AXI DBI Slave Read or Write transfers are pending, that is, AXI Slave transfers are awaiting a response from the controller. For debugging purposes. 1'b0: AXI Slave DBI transfer not pending 1'b1: AXI Slave DBI transfer pending
4	RO	0x0	brdg_slv_xfer_pending AXI Slave non-DBI transfer pending status. Indicates AXI non-DBI Slave Read or Write transfers are pending, that is, AXI Slave transfers are awaiting a response from the controller. For debugging purposes. 1'b0: AXI Slave non-DBI transfer not pending 1'b1: AXI Slave non-DBI transfer pending
3	RO	0x0	reserved
2	RO	0x0	radm_idle RADM activity status signal. The controller creates the en_radm_clk_g output by gating this signal with the output of the RADM_CLK_GATING_EN field in the CLOCK_GATING_CTRL_OFF register. For debug purposes only. 1'b0: RADM is not idle in status 1'b1: RADM is in idle status
1	RO	0x0	rdlh_link_up Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Data link layer down 1'b1: Data link layer up
0	RO	0x0	smlh_link_up PHY Link up/down indicator. 1'b0: PHY link is down 1'b1: PHY link is up

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PCIE_CLIENT_SLC_DEBUG_INFO_CMN

Address: Operational Base(0xFF500000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 78 bit of common silicon debug information: 3'b000: Select bit 15 to 0 3'b001: Select bit 31 to 16 3'b010: Select bit 47 to 32 3'b011: Select bit 63 to 48 3'b100: Select bit 79 to 64 Other: Reserved
27:16	RO	0x000	reserved
15:0	RO	0x0000	cdm_ras_des_sd_info_common Common debug signal bus that is used in RAS D.E.S. silicon debug Bit [78]: init_eq_pending_g4: Level: Equalization sequence Gen5 Bit [77:75]: l1sub_state: Level: L1 sub state Bit [74]: init_eq_pending_g4: Level: Equalization sequence Gen4 Bit [73]: init_eq_pending: Level: Equalization sequence Gen3 Bit [72:61]: xdlh_curnt_seqnum [11:0]: Level: Tx TLP SEQ# Bit [60:49]: rdlh_curnt_rx_ack_seqnum[11:0]: Level: Rx ACK SEQ# Bit [48]: rdlh_vc0_initfc2_status: Level: Init-FC Flag2 VC0 Bit [47]: rdlh_vc0_initfc1_status: Level: Init-FC Flag1 VC0 Bit [46:45]: rdlh_dlcntrl_state [1:0]: Level: DLCM Bit [44:37]: latched_ts_nfts[7:0]: Level: Latched NFTS Bit [36:34]: ltssm_powerdown[1:0]: Level: PIPE: Power Down Bit [33:18]: smlh_ltssm_variable [15:0]: Level: LTSSM Variable Bit [17]: pm_pme_resend_flag: Pulse: PME Re-Send flag Bit [16]: smlh_lane_reversed: Level: Lane Reversal Operation Bit [15:9]: rmlh_framing_err_ptr[6:0]: Pulse: 1st Framing Error Pointer Bit [8:5]: pm_slave_state[3:0]: Level: PM Internal State (Slave) Bit [4:0]: pm_master_state[4:0]: Level: PM Internal State (Master)

PCIE_CLIENT_SLC_DEBUG_INFO_LN

Address: Operational Base(0xFF500000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 78 bit of Lane N silicon debug information: 3'b000: Select bit 15 to 0 3'b001: Select bit 31 to 16 3'b010: Select bit 47 to 32 3'b011: Select bit 63 to 48 3'b100: Select bit 79 to 64 Others: Reserved
27:24	RW	0x0	lane_sel cdm_ras_des_sd_info_li source selects 4'h0: Lane 0 4'h1: Lane 1 4'h2: Lane 2 4'h3: Lane 3
23:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	cdm_ras_des_sd_info_li 16 of total 78-bit lane N silicon debug information, selected by bus_select field. [77:76]: eq_convergence_sts [1:0]: Level: Equalization convergence information Gen3 [75]: eqpa_violate_rule_123[2]: Level: Rule C Violation Event Status Gen3 [74]: eqpa_violate_rule_123[1]: Level: Rule B Violation Event Status Gen3 [73]: eqpa_violate_rule_123[0]: Level: Rule A Violation Event Status Gen3 [72]: mac_cdm_ras_des_reject_rtx: Level: Receive Reject Coefficient Event status Gen3 [71:64]: phy_cdm_ras_des_fomfeedback: Level: Current Figure of Merit Gen3 [63:61]: mac_cdm_ras_des_pset_lrx: Level: Current Local Receiver Preset Hint Gen3 [60:55]: mac_cdm_ras_des_coef_ltx[5:0]: Level: Current Local Transmitter Pre Cursor coefficient Gen3 [54:49]: mac_cdm_ras_des_coef_ltx[11:6]: Level: Current Local Transmitter Cursor coefficient Gen3 [48:43]: mac_cdm_ras_des_coef_ltx[17:12]: Level: Current Local Transmitter Post Cursor coefficient Gen3 [42:37]: mac_cdm_ras_des_coef_rtx[5:0]: Level: Current Remote Transmitter Pre Cursor coefficient Gen3 [36:31]: mac_cdm_ras_des_coef_rtx[11:6]: Level: Current Remote Transmitter Cursor coefficient Gen3 [30:25]: mac_cdm_ras_des_coef_rtx[17:12]: Level: Current Remote Transmitter Post Cursor coefficient Gen3 [24:19]: mac_cdm_ras_des_lf: Level: Remote Device LF Gen3 [18:13]: mac_cdm_ras_des_fs: Level: Remote Device FS Gen3 [12:5]: rmlh_deskew_fifo_ptr: Level: Deskew Pointer [4]: mac_phy_rxpolarity: Level: PIPE: RxPolarity [3]: latched_rxdetected: Level: PIPE: Detect Lane [2]: phy_mac_rxvalid_rxburst: Level: PIPE: RxValid/RxBurst [1]: phy_mac_rxelec_rxh8exit: Level: PIPE: RxElecIdle/RxHibern8ExitType1 [0]: mac_phy_txelec_txburst: Level: PIPE: TxElecIdle/TxBurst

PCIE_CLIENT_SLC_DEBUG_INFO_V0

Address: Operational Base(0xFF500000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 240 bit of virtual channel 0 silicon debug information: 4'd0: Select bit 15 to 0 4'd1: Select bit 31 to 16 ... 4'd14: Select bit 239 to bit 224 Other: Reserved
27:16	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	cdm_ras_des_sd_info_vi 16 of total 240-bit l1 silicon debug information, selected by bus_select field. [239:228]: rtlh_fc_allctd_cpld: Level: Credit Allocated (CD) [227:220]: rtlh_fc_allctd_cplh: Level: Credit Allocated (CH) [219:208]: rtlh_fc_allctd_npd: Level: Credit Allocated (ND) [207:200]: rtlh_fc_allctd_nph: Level: Credit Allocated (NH) [199:188]: rtlh_fc_allctd_pd: Level: Credit Allocated (PD) [187:180]: rtlh_fc_allctd_ph: Level: Credit Allocated (PH) [179:168]: rtlh_fc_rcvd_cpld: Level: Credit Received (CD) [167:160]: rtlh_fc_rcvd_cplh: Level: Credit Received (CH) [159:148]: rtlh_fc_rcvd_npd: Level: Credit Received (ND) [147:140]: rtlh_fc_rcvd_nph: Level: Credit Received (NH) [139:128]: rtlh_fc_rcvd_pd: Level: Credit Received (PD) [127:120]: rtlh_fc_rcvd_ph: Level: Credit Received (PH) [119:108]: xadm_fc_limit_cpld: Level: Credit Limit (CD) [107:100]: xadm_fc_limit_cplh: Level: Credit Limit (CH) [99:88]: xadm_fc_limit_npd: Level: Credit Limit (ND) [87:80]: xadm_fc_limit_nph: Level: Credit Limit (NH) [79:68]: xadm_fc_limit_pd: Level: Credit Limit (PD) [67:60]: xadm_fc_limit_ph: Level: Credit Limit (PH) [59:48]: xadm_fc_cnsmd_cpld: Level: Credit Consumed (CD) [47:40]: xadm_fc_cnsmd_cplh: Level: Credit Consumed (CH) [39:28]: xadm_fc_cnsmd_npd: Level: Credit Consumed (ND) [27:20]: xadm_fc_cnsmd_nph: Level: Credit Consumed (NH) [19:8]: xadm_fc_cnsmd_pd: Level: Credit Consumed (PD) [7:0]: xadm_fc_cnsmd_ph: Level: Credit Consumed (PH)

PCIE_CLIENT_DIAG_STATUS_BUS_SEL

Address: Operational Base(0xFF500000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	diag_bus_sel Select the 32bit of total 1024 bit of diag_status_bus that present on register DIAG_STATUS_BUS_INFO. 5'd0: bit 31 to 0 5'd1: bit 63 to 32 ... 5'd31: bit 1023 to 992

PCIE_CLIENT_DIAG_STATUS_BUS_INFO

Address: Operational Base(0xFF500000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	diag_status_bus 32 bit of total 1024-bit width diag_status_bus. Selected by DIAG_STATUS_BUS_SEL register. Contains all the important status signals from each controller module. Debug only.

PCIE_CLIENT_CDM_RASDES_EC_INFO_CON

Address: Operational Base(0xFF500000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	cdm_rasdes_ec_info_lane_sel cdm_ras_des_ec_info_li source selects 4'h0: Lane 0 4'h1: Lane 1 4'h2: Lane 2 4'h3: Lane 3
3:0	RW	0x0	cdm_rasdes_ec_info_con Select the 32bit rasdes_ec_info_cmn 4'd0: Select bit 31 to 0 4'd1: Select bit 63 to 32 ..... Others: Reserved

PCIE_CLIENT_CDM_RASDES_EC_INFO_CMN

Address: Operational Base(0xFF500000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cdm_ras_des_ec_info_common Common event signal bus that is used in RAS D.E.S. event counters

PCIE_CLIENT_CDM_RASDES_EC_INFO_LN

Address: Operational Base(0xFF500000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	cdm_ras_des_ec_info_li Lanei event signal bus that is used in RAS D.E.S. event counters.

PCIE_CLIENT_CDM_RASDES_TBA_CON

Address: Operational Base(0xFF500000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	app_ras_des_tba_ctrl Controls the start/end of time-based analysis. You must only set the pins to the required value for the duration of one clock cycle. This signal must be 2'b00 while the TIMER_START field in TIME_BASED_ANALYSIS_CONTROL_REG register is controlled by the DBI interface or the accesses from the wire side. 2'b00: No action 2'b01: Start 2'b10: End. This setting is only used when the TIME_BASED_DURATION_SELECT field of TIME_BASED_ANALYSIS_CONTROL_REG is set to "manual control". 2'b11: Reserved These pins also set the contents of the TIMER_START field in TIME_BASED_ANALYSIS_CONTROL_REG register.

PCIE_CLIENT_CDM_RASDES_TBA_INFO_CMN

Address: Operational Base(0xFF500000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	cdm_ras_des_tba_info_common Common event signal status bus used in RAS D.E.S. time-based analysis. Indicates the internal signals that are used in the time-based analysis. The results are in TIME_BASED_ANALYSIS_DATA_REG. Each bit indicates the state that the controller stays in. All signals are level sensitive unless otherwise indicated. [6]: smlh_link_in_training: Config/Recovery [5]: pm_in_l12: L1.2 [4]: pm_in_l11: L1.1 [3]: smlh_in_l1: L1 [2]: smlh_in_l0: L0 [1]: smlh_in_rl0s: Rx L0s [0]: smlh_in_l0s: Tx L0s

PCIE_CLIENT_HOT_RESET_CTRL

Address: Operational Base(0xFF500000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	app_ltssm_enable_enhance Set "1" to enable ltssm_enbale enhance mode. In this mode, the host-reset and link-down reset can be optionaly delayed. Available after version 50600.
3	RW	0x0	app_dly2_done Set "1" to end the delaying of the link training after Hot Reset. This bit is self-cleared. Available after version 50600.
2	RW	0x0	app_dly1_done Set "1" to end the delaying of the controller Hot Reset. This bit is self-cleared. Available after version 50600.
1	RW	0x0	app_dly2_en Set "1" to enable delaying the link training after Hot Reset Available after version 50600.
0	RW	0x0	app_dly1_en Set "1" to enable delaying the controller Hot Reset Available after version 50600.

PCIE_CLIENT_INTR_EN_MSG_RX

Address: Operational Base(0xFF500000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	obff_cpu_active_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

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Bit	Attr	Reset Value	Description
13	RW	0x1	obff_obff_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
12	RW	0x1	obff_idle_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RO	0x0	reserved
10	RW	0x1	pm_turnoff_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	pm_to_ack_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	pm_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7:6	RO	0x0	reserved
5	RW	0x1	cfg_pme_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	cfg_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RO	0x0	reserved
2	RW	0x1	ltr_msg_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	unlock_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	ven_msg_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_LEGACY

Address: Operational Base(0xFF500000) + offset (0x0194)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	tx_intd_int_en Reserved
6	RW	0x1	tx_intc_int_en Reserved
5	RW	0x1	tx_intb_int_en Reserved
4	RW	0x1	tx_inta_int_en Reserved
3	RW	0x1	rx_intd_int_en Reserved
2	RW	0x1	rx_intc_int_en Reserved
1	RW	0x1	rx_intb_int_en Reserved
0	RW	0x1	rx_inta_int_en Reserved

PCIE_CLIENT_INTR_EN_ERR

Address: Operational Base(0xFF500000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	radm_qoverflow_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RO	0x0	reserved
10	RW	0x1	f_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	nf_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	cor_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x1	f_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	nf_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	cor_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	tx_cpl_timeout_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
2	RW	0x1	rx_cpl_timeout_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	aer_rc_err_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	aer_rc_err_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_MISC

Address: Operational Base(0xFF500000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	ep_elbi_app_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
14	RW	0x1	link_eq_req_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

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Bit	Attr	Reset Value	Description
13	RW	0x1	rbar_update_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
12	RW	0x1	dpa_sub_upd_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RW	0x1	edma_rd_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
10	RW	0x1	edma_wr_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	bw_mgt_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	bw_mgt_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7	RW	0x1	link_auto_bw_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
6	RW	0x1	link_auto_bw_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	hp_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	hp_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	hp_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

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Bit	Attr	Reset Value	Description
2	RW	0x1	link_req_rst_not_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	dll_link_up_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	phy_link_up_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_PMC

Address: Operational Base(0xFF500000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	pm_dstate_update_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7	RW	0x1	linkst_out_l0s_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
6	RW	0x1	linkst_out_l2_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	linkst_out_l1_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	linkst_out_l1sub_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	linkst_in_l0s_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

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Bit	Attr	Reset Value	Description
2	RW	0x1	linkst_in_l2_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	linkst_in_l1_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	linkst_in_l1sub_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_MSI_INT_RX_VEC

Address: Operational Base(0xFF500000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	msi_ctrl_int_vec DSP AXI MSI Interrupt Vector. Asserted when an MSI interrupt is pending. De-asserted when there is no MSI interrupt pending

PCIE_CLIENT_AXI_MSTR_MISC_CON

Address: Operational Base(0xFF500000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	mstr_rmisc_ep AXI Master Read Response Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of standard AXI interface. For more information, see 'AXI Master Interface Sideband Signals'. All reserved bits must be connected to logic '0'. [1:0]: Reserved [2]: Reserved [6:3]: Reserved [7]: TLP's EP bit [12:8]: Reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	mstr_rmisc_info_cpl_stat AXI Master Read Response selection bus. This bus controls the response sent on the PCIe wire in the case of successful read requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. For more information, see the "Master AXI-to-PCIe Error Mapping" section in the AXI chapter of the Databook. 2'b00: SC (Successful Completion) 2'b01: CA (Completer Abort) 2'b10: UR (Unsupported Request) 2'b11: SC (Successful Completion) Your application must drive the same value on mstr_rmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_rmisc_info_cpl_stat to UR: 1. If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. 2. If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.
1:0	RW	0x0	mstr_bmisc_info_cpl_stat AXI Master Write Response selection bus. This controls the response to be sent on the wire in the case of successful write requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. For more information, see the "Master AXI-to-PCIe Error Mapping" section in the AXI chapter of the Databook. 2'b00: SC (Successful Completion) 2'b01: CA (Completer Abort) 2'b10: UR (Unsupported Request) 2'b11: SC (Successful Completion) Your application must drive the same value on mstr_bmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_bmisc_info_cpl_stat to UR: 1. If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. 2. If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.

PCIE_CLIENT_AXI_SLV_ATU_BYPASS

Address: Operational Base(0xFF500000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	slv_armisc_info_atu_bypass AXI Slave Read Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit. 1'b0: Not bypass 1'b1: AXI slave read address ATU bypass

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Bit	Attr	Reset Value	Description
0	RW	0x0	slv_awmisc_info_atu_bypass AXI Slave Write Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit. 1'b0: Not bypass 1'b1: AXI slave write address ATU bypass

PCIE_CLIENT_AXI_SLV_AWMISC_HDR

Address: Operational Base(0xFF500000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	slv_awmisc_info AXI Slave Write Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more information, see 'AXI Slave Interface Sideband Signals'. You must set all reserved bits to '0'.[4:0]: TLP's TYPE. For more information, see 'I/O and CFG Transaction Handling' [5]: Serialize NP Requests [6]: TLP's EP bit [7]: Reserved [8]: TLP's NS bit [9]: TLP's RO bit [12:10]: TLP's TC bits [20:13]: TLP's MSG code [21]: AXI transaction is a DBI access. This is for SHARED DBI mode only. [24:22]: TLP's Function number. Function numbering starts at '0'. Not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more information, see slv_awmisc_info_func_num. This field is only present when multifunction support (CX_NFUNC > 1) is enabled. For a configuration transfer, you must drive the bus number, device number, function number, and register number onto the address bus as follows: bus_number = addr[31:24] dev_number = addr[23:19] func_number = addr[18:16] ext_reg_number = addr[11:8] reg_number = addr[7:2]

PCIE_CLIENT_AXI_SLV_AWMISC_HDR3

Address: Operational Base(0xFF500000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_hdr_3dw AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.

PCIE_CLIENT_AXI_SLV_AWMISC_HDR4

Address: Operational Base(0xFF500000) + offset (0x0210)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_hdr_4dw AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.

PCIE_CLIENT_AXI_SLV_AWMISC_TAG

Address: Operational Base(0xFF500000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	slv_awmisc_info_p_tag AXI Slave Write Request Tag. Sets the TAG number for output posted requests. It is expected that your application normally sets this to '0' except when generating ATS invalidate requests.

PCIE_CLIENT_AXI_SLV_MISC_INFO

Address: Operational Base(0xFF500000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	slv_wmisc_info_ep AXI Slave Write Data transaction related misc information. This is an optional signal that your application can use to poison write requests. When asserted, the controller sets the Poisoned TLP (EP) bit in the TLP header of the current and subsequent Write Data transactions. It is not a part of the standard AXI interface. For more information, see "AXI Slave Interface Sideband Signals" section in the Databook.
21:0	RW	0x000000	slv_armisc_info AXI Slave Read Transaction Associated Miscellaneous Information. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more information, see 'AXI Slave Interface Sideband Signals'. You must set all reserved bits to '0'. [4:0]: TLP's TYPE [5]: Serialize NP Requests [6]: TLP's EP bit [7]: Reserved [8]: TLP's NS bit [9]: TLP's RO bit [12:10]: TLP's TC bits [20:13]: TLP's MSG code [21]: AXI transaction is a DBI access. This is for SHARED DBI mode only. [24:22]: TLP's function number. Function numbering starts at '0'. Not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more information, see slv_armisc_info_func_num. This field is only present when multifunction support (CX_NFUNC > 1) is enabled. For a configuration transfer, you must drive the bus number, device number, function number, and register number onto the address bus as follows: bus_number = addr[31:24] dev_number = addr[23:19] func_number = addr[18:16] ext_reg_number = addr[11:8] reg_number = addr[7:2]

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PCIE_CLIENT_AXI_SLV_AW_TLP_PRFX

Address: Operational Base(0xFF500000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_tlpprfx AXI Slave Write Request TLP Prefixes. The field [31:0] represents the first prefix to be transmitted. The optional TLP prefixes are implemented as little endian. Using the example of a controller with just one prefix (CX_NPRFX =1), this means that slv_awmisc_info_tlpprfx[31:0] has prefix byte #0 in the lower byte position of the dword slv_awmisc_info_tlpprfx[31:0]. That is, FMT =bits 7:5, and Type =bits 4:0. Your application is responsible for passing Local and End-End prefixes in the correct order for transmission. Local prefixes must precede End-End prefixes. Any parity bits that your application appends (when RAS data protection is enabled) to the most significant bits are routed but not checked by the controller. The controller passes along and appends to the prefix, any protection codes it receives, when datapath protection is enabled. Available after version 50610.

PCIE_CLIENT_AXI_SLV_AR_TLP_PRFX

Address: Operational Base(0xFF500000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	slv_armisc_info_tlpprfx AXI Slave Read Request TLP Prefixes. The field [31:0] represents the first prefix to be transmitted. The optional TLP prefixes are implemented as little endian. Using the example of a controller with just one prefix (CX_NPRFX =1), this means that slv_armisc_info_tlpprfx[31:0] has prefix byte #0 in the lower byte position of the dword slv_armisc_info_tlpprfx[31:0]. That is, FMT =bits 7:5, and Type =bits 4:0. Your application is responsible for passing Local and End-End prefixes in the correct order for transmission. Local prefixes must precede End-End prefixes. Any parity bits that your application appends (when RAS data protection is enabled) to the most significant bits are routed but not checked by the controller. The controller passes along and appends to the prefix, any protection codes it receives, when datapath protection is enabled. Available after version 50610.

PCIE_CLIENT_DBI_MISC_CON

Address: Operational Base(0xFF500000) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	dbi_msix_table_access_ctrl Control the bit 30 of the DBI awaddr. Set 1 to enable access, and shoud clear to 0 when access done.

PCIE_CLIENT_PORT_BDF

Address: Operational Base(0xFF500000) + offset (0x0274)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	app_bus_dev Bus number. Your application must drive this signal to set the bus number in the Requester ID for RC port and Switch DSP port.
7:3	RW	0x00	app_dev_num Device number. Your application must drive this signal to set the device number in the Requester ID for RC port and Switch DSP port.
2:0	RO	0x0	reserved

PCIE_CLIENT_LTSSM_STATUS

Address: Operational Base(0xFF500000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RO	0x0	pm_current_data_rate The current link operating rate. 3'b000: 2.5 GT/s signalling rate 3'b001: 5.0 GT/s signalling rate 3'b010: 8.0 GT/s signalling rate for PCIe mode or ESM data rate0 for ESM mode 3'b011: 16.0 GT/s signalling rate for PCIe mode or ESM data rate1 for ESM mode 3'b100: 32.0 GT/s signalling rate
19:18	RO	0x0	reserved
17	RO	0x0	rdlh_link_up Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Link is down 1'b1: Link is up
16	RO	0x0	smlh_link_up PHY Link up/down indicator: 1'b0: Link is down 1'b1: Link is up
15:11	RO	0x00	reserved
10:8	RO	0x0	l1sub_state Power management L1 sub-states FSM state.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	smlh_ltssm_state smlh_ltssm_state Current state of the LTSSM. Encoding is defined as follows: 6'h00: S_DETECT_QUIET 6'h01: S_DETECT_ACT 6'h02: S_POLL_ACTIVE 6'h03: S_POLL_COMPLIANCE 6'h04: S_POLL_CONFIG 6'h05: S_PRE_DETECT_QUIET 6'h06: S_DETECT_WAIT 6'h07: S_CFG_LINKWD_START 6'h08: S_CFG_LINKWD_ACEPT 6'h09: S_CFG_LANENUM_WAI 6'h0A: S_CFG_LANENUM_ACEPT 6'h0B: S_CFG_COMPLETE 6'h0C: S_CFG_IDLE 6'h0D: S_RCVRY_LOCK 6'h0E: S_RCVRY_SPEED 6'h0F: S_RCVRY_RCVRCFG 6'h10: S_RCVRY_IDLE 6'h11: S_L0 6'h12: S_L0S 6'h13: S_L123_SEND_EIDLE 6'h14: S_L1_IDLE 6'h15: S_L2_IDLE 6'h16: S_L2_WAKE 6'h17: S_DISABLED_ENTRY 6'h18: S_DISABLED_IDLE 6'h19: S_DISABLED 6'h1A: S_LPBK_ENTRY 6'h1B: S_LPBK_ACTIVE 6'h1C: S_LPBK_EXIT 6'h1D: S_LPBK_EXIT_TIMEOUT 6'h1E: S_HOT_RESET_ENTRY 6'h1F: S_HOT_RESET 6'h20: S_RCVRY_EQ0 6'h21: S_RCVRY_EQ1 6'h22: S_RCVRY_EQ2 6'h23: S_RCVRY_EQ3

PCIE_CLIENT_DBG_FIFO_MODE_CON

Address: Operational Base(0xFF500000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	dbg_fifo_hit_mode Hit mode control. Bit0 enable pattern 0 match mode Bit1 enable pattern 1 match mode Bit2 enable pattern 0 transition mode
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	dbg_fifo_mode Debug FIFO store debug status mode 2'b00: Default 2'b01: If hit pattern, disable FIFO write 2'b10: If FIFO full, disable FIFO write 2'b11: Reserved
3	RO	0x0	reserved
2	RW	0x0	dbg_fifo_l1sub_en Debug FIFO enable for L1SS 1'b0: Disable 1'b1: Enable
1	RW	0x0	dbg_fifo_ltssm_en Debug FIFO enable for LTSSM 1'b0: Disable 1'b1: Enable
0	RW	0x0	dbg_fifo_en Debug FIFO enable 1'b0: Disable 1'b1: Enable

PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA0

Address: Operational Base(0xFF500000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ptn_hit_data0 Hit mode data pattern 0

PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA1

Address: Operational Base(0xFF500000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ptn_hit_data1 Hit mode data pattern 1

PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA0

Address: Operational Base(0xFF500000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trn_hit_data0 Transition state data 0

PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA1

Address: Operational Base(0xFF500000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trn_hit_data1 Transition state data 1

PCIE_CLIENT_DBG_FIFO_STATUS

Address: Operational Base(0xFF500000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RO	0x0	dbg_pm_current_data_rate The current link operating rate. 3'b000: 2.5 GT/s signalling rate 3'b001: 5.0 GT/s signalling rate 3'b010: 8.0 GT/s signalling rate for PCIe mode or ESM data rate0 for ESM mode 3'b011: 16.0 GT/s signalling rate for PCIe mode or ESM data rate1 for ESM mode 3'b100: 32.0 GT/s signalling rate Available after version 50610.
19	RO	0x0	reserved
18:16	RO	0x0	dbg_space2empty Debug FIFO space to empty.
15	RO	0x0	reserved
14	RO	0x0	dbg_fifo_wr_overfollow Debug FIFO overfollow flag 1'b0: Not overfollow 1'b1: Overfollow
13	RO	0x0	dbg_fifo_full Debug FIFO full flag 1'b0: Not full 1'b1: Full
12	RO	0x0	dgb_fifo_empty Debug FIFO empty flag 1'b0: Not empty 1'b1: Empty
11	RO	0x0	reserved
10:8	RO	0x0	dbg_fifo_l1sub_state Power management L1 sub-states FSM state.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	dbg_fifo_ltssm_state smlh_ltssm_state Current state of the LTSSM. Encoding is defined as follows: 6'h00: S_DETECT_QUIET 6'h01: S_DETECT_ACT 6'h02: S_POLL_ACTIVE 6'h03: S_POLL_COMPLIANCE 6'h04: S_POLL_CONFIG 6'h05: S_PRE_DETECT_QUIET 6'h06: S_DETECT_WAIT 6'h07: S_CFG_LINKWD_START 6'h08: S_CFG_LINKWD_ACEPT 6'h09: S_CFG_LANENUM_WAI 6'h0A: S_CFG_LANENUM_ACEPT 6'h0B: S_CFG_COMPLETE 6'h0C: S_CFG_IDLE 6'h0D: S_RCVRY_LOCK 6'h0E: S_RCVRY_SPEED 6'h0F: S_RCVRY_RCVRCFG 6'h10: S_RCVRY_IDLE 6'h11: S_L0 6'h12: S_L0S 6'h13: S_L123_SEND_EIDLE 6'h14: S_L1_IDLE 6'h15: S_L2_IDLE 6'h16: S_L2_WAKE 6'h17: S_DISABLED_ENTRY 6'h18: S_DISABLED_IDLE 6'h19: S_DISABLED 6'h1A: S_LPBK_ENTRY 6'h1B: S_LPBK_ACTIVE 6'h1C: S_LPBK_EXIT 6'h1D: S_LPBK_EXIT_TIMEOUT 6'h1E: S_HOT_RESET_ENTRY 6'h1F: S_HOT_RESET 6'h20: S_RCVRY_EQ0 6'h21: S_RCVRY_EQ1 6'h22: S_RCVRY_EQ2 6'h23: S_RCVRY_EQ3

PCIE_CLIENT_CFG_ERR_STATUS

Address: Operational Base(0xFF500000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	cfg_uncor_internal_err_sts Indication from the controller that the controller has detected an Uncorrectable Internal Error.
11	RO	0x0	cfg_rcvr_overflow_err_sts Indication from the controller that the controller has detected an Receiver Overflow Error.
10	RO	0x0	cfg_fc_protocol_err_sts Indication from the controller that the controller has detected an Flow Control Protocol Error.
9	RO	0x0	cfg_mlf_tlp_err_sts Indication from the controller that the controller detected an Malformed TLP Error.

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Bit	Attr	Reset Value	Description
8	RO	0x0	cfg_surprise_down_err_sts Indication from the controller that the controller detected an Surprise Down Error.
7	RO	0x0	cfg_dl_protocol_err_sts Indication from the controller that the controller detected an Data Link Protocol Error.
6	RO	0x0	cfg_ecrc_err_sts Indication from the controller that the controller detected an ECRC Error.
5	RO	0x0	cfg_corrected_internal_err_sts Indication from the controller that the controller detected an Corrected Internal Error.
4	RO	0x0	cfg_replay_number_rollover_err_sts Indication from the controller that the controller detected an REPLAY_NUMBER Rollover Error.
3	RO	0x0	cfg_replay_timer_timeout_err_sts Indication from the controller that the controller detected an Replay Timer Timeout.
2	RO	0x0	cfg_bad_dllp_err_sts Indication from the controller that the controller detected an Bad DLLP Error.
1	RO	0x0	cfg_bad_tlp_err_sts Indication from the controller that the controller detected an Bad TLP Error.
0	RO	0x0	cfg_rcvr_err_sts Indication from the controller that the controller detected an Receiver Error.

PCIE_CLIENT_TLP_PRFX_LOG0

Address: Operational Base(0xFF500000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_0 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG1

Address: Operational Base(0xFF500000) + offset (0x0384)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_1 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG2

Address: Operational Base(0xFF500000) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_2 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG3

Address: Operational Base(0xFF500000) + offset (0x038C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_3 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_CLIENT_VER

Address: Operational Base(0xFF500000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RO	0x00050611	version Client version ID

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7.4.3 Downstream Port Register

7.4.3.1 PCIE_DSP_PF0_TYPE1_HDR

7.4.3.1.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_DEV_ID_VEND_ID_REG	0x0000	W	0x35621D87	This register holds the device ID and vendor ID.
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_STATUS_COMMAND_REG	0x0004	W	0x00100000	This register provides the status and controls the behavior of a function.
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_CLASS_CODE_REV_ID_REG	0x0008	W	0x00000001	This register specifies the class code and revision ID of a function.
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_BIST_HDR_TYPE_LAT_CACHE_LINE_SIZE_REG	0x000C	W	0x00010000	This register provides the status and controls BIST. It also holds information regarding the header layout, latency timer, and cache line size.
PCIE_DSP_PF0_TYPE1_HDR_BAR0_REG	0x0010	W	0x00000000	System software must build a consistent address map before booting the machine to an operating system. This means it has to determine how much memory is in the system, and how much address space the Functions in the system require. After determining this information, system software can map the Functions into reasonable locations and proceed with system boot. In order to do this mapping in a device-independent manner, the base registers for this mapping are placed in the predefined header portion of Configuration Space. It is strongly recommended that power-up firmware/software also support the optional Enhanced Configuration Access Mechanism (ECAM).

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_TYPE1_HDR_BAR1_REG	0x0014	W	0x00000000	System software must build a consistent address map before booting the machine to an operating system. This means it has to determine how much memory is in the system, and how much address space the Functions in the system require. After determining this information, system software can map the Functions into reasonable locations and proceed with system boot. In order to do this mapping in a device-independent manner, the base registers for this mapping are placed in the predefined header portion of Configuration Space. It is strongly recommended that power-up firmware/software also support the optional Enhanced Configuration Access Mechanism (ECAM).
PCIE_DSP_PF0_TYPE1_HDR_SEC_LAT_TIMER_SUB_BUS_SEC_BUS_PRI_BUS_REG	0x0018	W	0x00000000	This register holds information regarding secondary latency timer, subordinate bus number, secondary bus number, and primary bus number.
PCIE_DSP_PF0_TYPE1_HDR_SEC_STAT_IO_LIMIT_IO_BASE_REG	0x001C	W	0x00000000	The I/O Limit and I/O Base registers are optional and define an address range that is used by the bridge to determine when to forward I/O transactions from one interface to the other. If a bridge does not implement an I/O address range, then both the I/O Limit and I/O Base registers must be implemented as read-only registers that return zero when read. If a bridge supports an I/O address range, then these registers must be initialized by configuration software so default states are not specified.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_TYPE1_HDR_MEM_LIMIT_MEM_BASE_REG	0x0020	W	0x00000000	The Memory Limit and Memory Base registers define a memory mapped address range which is used by the bridge to determine when to forward memory transactions from one interface to the other. If there is no prefetchable memory space, and there is no memory-mapped space on the secondary side of the bridge, then the bridge will not forward any memory transactions from the primary bus to the secondary bus and will forward all memory transactions from the secondary bus to the primary bus.
PCIE_DSP_PF0_TYPE1_HDR_PREF_MEM_LIMIT_PREF_MEM_BASE_REG	0x0024	W	0x00010001	The Prefetchable Memory Limit and Prefetchable Memory Base registers must indicate that 64-bit addresses are supported.The Prefetchable Memory Limit and Prefetchable Memory Base registers are optional. They define a prefetchable memory address range which is used by the bridge to determine when to forward memory transactions from one interface to the other (see the PCI-to-PCI Bridge Architecture Specification for additional details).
PCIE_DSP_PF0_TYPE1_HDR_PREF_BASE_UPPER_REG	0x0028	W	0x00000000	The Prefetchable Base Upper 32 Bits register is an optional extension to the Prefetchable Memory Base register.
PCIE_DSP_PF0_TYPE1_HDR_PREF_LIMIT_UPPER_REG	0x002C	W	0x00000000	The Prefetchable Limit Upper 32 Bits register is an optional extension to the Prefetchable Memory Limit register.
PCIE_DSP_PF0_TYPE1_HDR_IO_LIMIT_UPPER_IO_BASE_UPPER_REG	0x0030	W	0x00000000	The I/O Limit Upper 16 Bits and I/O Base Upper 16 Bits registers are optional extensions to the I/O Limit and I/O Base registers.
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_CAP_PTR_REG	0x0034	W	0x00000040	This register is used to point to a linked list of capabilities implemented by a Function.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_EXP_ROM_BASE_REG	0x0038	W	0x00000000	This register is defined to handle the base address and size information for this expansion ROM. The mask for this ROM BAR exists (if implemented) as a shadow register at this address. The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the second register at this address.
PCIE_DSP_PF0_TYPE1_HDR_BRIDGE_CTRL_INT_PIN_INT_LINE_REG	0x003C	W	0x000001FF	This register provides many of the same controls for the secondary interface that are provided by the Command Register for theprimary interface. This register also identifies the legacy interrupt Message(s) a Function uses and communicates interrupt line routing information.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.1.2 Detail Registers Description

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_DEV_ID_VEND_ID_REG

Address: Operational Base(0xFE000000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x3562	DEVICE_ID Device ID. The Device ID register identifies the particular Function. This identifier is allocated by the vendor. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RO	0x1d87	VENDOR_ID Vendor ID. The Vendor ID register identifies the manufacturer of the Function. Valid vendor identifiers are allocated by the PCI-SIG to ensure uniqueness. It is not permitted to populate this register with a value of FFFFh, which is an invalid value for Vendor ID. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_STATUS_COMMAND_REG

Address: Operational Base(0xFE000000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	DETECTED_PARITY_ERROR Detected Parity Error. The bit is set when the Poisoned TLP is received by a Function's primary side.
30	RW	0x0	SIGNALED_SYS_ERROR Signaled System Error.

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Bit	Attr	Reset Value	Description
29	RW	0x0	RCVD_MASTER_ABORT Received Master Abort. This bit is set when a Requester receives a Completion with Unsupported Request Completion status. The bit is set when the Unsupported Request is received by a Function's primary side.
28	RW	0x0	RCVD_TARGET_ABORT Received Target Abort. This bit is set when a Requester receives a Completion with Completer Abort Completion status. The bit is set when the Completer Abort is received by a Function's primary side.
27	RW	0x0	SIGNALED_TARGET_ABORT Signaled Target Abort. This bit is set when a Function completes a Posted or Non-Posted Request as a Completer Abort error. This applies to a Function when the Completer Abort was generated by its primary side.
26:25	RO	0x0	DEV_SEL_TIMING DEVSEL Timing. This field was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires it to 00b.
24	RW	0x0	MASTER_DPE Master Data Parity Error. This bit is set by a Function if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: - Port receives a Poisoned Completion going downstream - Port transmits a Poisoned Request upstream If the Parity Error Response bit is 0b, this bit is never set.
23	RO	0x0	FAST_B2B_CAP Fast Back-to-Back Transactions Capable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
22	RO	0x0	RSVDP_22 Reserved for future use.
21	RO	0x0	FAST_66MHZ_CAP 66 MHz Capable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
20	RO	0x1	CAP_LIST Capabilities List. Indicates the presence of an Extended Capability list item. Since all PCI Express device Functions are required to implement the PCI Express Capability structure, the controller hardwires this bit to 1b.

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Bit	Attr	Reset Value	Description
19	RO	0x0	INT_STATUS Interrupt Status. INTx emulation interrupts forwarded by Functions from the secondary side are not reflected in this bit. Setting the Interrupt Disable bit has no effect on the state of this bit. For Functions that do not generate INTx interrupts, the controller hardwires this bit to 0b.
18:17	RO	0x0	RSVDP_17 Reserved for future use.
16	RO	0x0	reserved
15:11	RO	0x00	RESERV Reserved.
10	RW	0x0	INT_EN Interrupt Disable. Controls the ability of a Function to generate INTx emulation interrupts. Note: - Any INTx emulation interrupts already asserted by the Function must be deasserted when this bit is set. INTx interrupts use virtual wires that must, if asserted, be deasserted using the appropriate Deassert_INTx message(s) when this bit is set. - Only the INTx virtual wire interrupt(s) associated with the Function(s) for which this bit is set are affected. - For Functions that generate INTx interrupts on their own behalf, this bit is required. This bit has no effect on interrupts forwarded from the secondary side. For Functions that do not generate INTx interrupts on their own behalf this bit is optional. If this bit is not implemented, the controller hardwires it to 0b.
9	RO	0x0	RSVDP_9 Reserved for future use.
8	RW	0x0	SERREN SERR# Enable. Note: - The errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control register. - In addition, this bit controls transmission by the primary interface of ERR_NONFATAL and ERR_FATAL error Messages forwarded from the secondary interface. This bit does not affect the transmission of forwarded ERR_COR messages.
7	RO	0x0	IDSEL IDSEL Stepping/Wait Cycle Control. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
6	RW	0x0	PERREN Parity Error Response. This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Status register.

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Bit	Attr	Reset Value	Description
5	RO	0x0	VGAPS VGA Palette Snoop. This bit was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
4	RO	0x0	MWI_EN Memory Write and Invalidate. This bit was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. For PCI Express to PCI/PCI-X Bridges, refer to the PCI Express to PCI/PCI-X Bridge Specification for requirements for this register.
3	RO	0x0	SCO Special Cycle Enable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
2	RW	0x0	BME Bus Master Enable. This bit controls forwarding of Memory or I/O requests by a port in the Upstream direction. When this bit is 0b, Memory and I/O Requests received at a Root Port must be handled as Unsupported Requests (UR) For Non-Posted Requests a Completion with UR completion status must be returned. This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O Requests is not controlled by this bit.
1	RW	0x0	MSE Memory Space Enable. This bit controls a Function's response to Memory Space accesses received on its primary side. You cannot write to this register if your configuration has no MEM BARs; that is, the internal signal has_mem_bar =0. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: !has_mem_bar ? RO : RW
0	RW	0x0	IO_EN IO Space Enable. This bit controls a Function's response to I/O Space accesses received on its primary side. You cannot write to this register if your configuration has no IO BARs; that is, the internal signal has_io_bar =0. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: !has_io_bar ? RO : RW

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_CLASS_CODE_REV_ID_REG

Address: Operational Base(0xFE000000) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	BASE_CLASS_CODE Base Class Code. A code that broadly classifies the type of operation the Function performs. Encodings for base class, are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
23:16	RO	0x00	SUBCLASS_CODE Sub-Class Code. Specifies a base class sub-class, which identifies more specifically the operation of the Function. Encodings for sub-class are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:8	RO	0x00	PROGRAM_INTERFACE Programming Interface. This field identifies a specific register level programming interface (if any) so that device independent software can interact with the Function. Encodings for interface are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
7:0	RO	0x01	REVISION_ID Revision ID. The value of this field specifies a Function specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. The Revision ID should be viewed as a vendor defined extension to the Device ID. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_BIST_HDR_TYPE_LAT_CACHE_LINE_SIZE_REG

Address: Operational Base(0xFE000000) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	BIST BIST. This register is used for control and status of BIST. Functions that do not support BIST must hardwire the register to 00h. A Function whose BIST is invoked must not prevent normal operation of the PCI Express Link. Bit descriptions: - [31]: BIST Capable. When set, this bit indicates that the Function supports BIST. When Clear, the Function does not support BIST. - [30]: Start BIST. If BIST Capable is set, set this bit to invoke BIST. The Function resets the bit when BIST is complete. Software is permitted to fail the device if this bit is not Clear (BIST is not complete) 2 seconds after it had been set. Writing this bit to 0b has no effect. The controller hardwires this bit to 0b if BIST Capable is clear. - [29:28]: Reserved. - [27:24]: Completion Code. This field encodes the status of the most recent test. A value of 0000b means that the Function has passed its test. Non-zero values mean the Function failed. Function-specific failure codes can be encoded in the non-zero values. This field's value is only meaningful when BIST Capable is set and Start BIST is Clear. This field must be hardwired to 0000b if BIST Capable is clear.
23	RO	0x0	MULTI_FUNC Multi-Function Device. Except where stated otherwise, it is recommended that this bit be set if there are multiple Functions, and clear if there is only one Function. Note: This register field is sticky.
22:16	RO	0x01	HEADER_TYPE Header Layout. This field identifies the layout of the second part of the predefined header. The controller uses 000 0001b encoding. The encoding 000 0010b is reserved. This encoding was originally described in the PC Card Standard Electrical Specification and is used in previous versions of the programming model. Careful consideration should be given to any attempt to re-purpose it.
15:8	RO	0x00	LATENCY_MASTER_TIMER Latency Timer. This register is also referred to as Primary Latency Timer. The Latency Timer was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this register to 00h.
7:0	RW	0x00	CACHE_LINE_SIZE Cache Line Size. The Cache Line Size register is programmed by the system firmware or the operating system to system cache line size. However, legacy conventional PCI software may not always be able to program this register correctly especially in the case of Hot-Plug devices. This read-write register is implemented for legacy compatibility purposes but has no effect on any PCI Express device behavior.

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PCIE_DSP_PF0_TYPE1_HDR_BAR0_REG

Address: Operational Base(0xFE000000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR0_START BAR0 Base Address. - Memory Space: Base Address. - IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky.
3	RO	0x0	BAR0_PREFETCH BAR0 Prefetchable. - Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. - IO Space: Not applicable Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.
2:1	RO	0x0	BAR0_TYPE BAR0 Type. - Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. - IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.
0	RO	0x0	BAR0_MEM_IO BAR0 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_BAR1_REG

Address: Operational Base(0xFE000000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR1_START BAR1 Base Address. - Memory Space: Base Address. - IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky.
3	RO	0x0	BAR1_PREFETCH BAR1 Prefetchable. - Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. - IO Space: Not applicable Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.
2:1	RO	0x0	BAR1_TYPE BAR1 Type. - Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. - IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.
0	RO	0x0	BAR1_MEM_IO BAR1 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_SEC_LAT_TIMER_SUB_BUS_SEC_BUS_PRI_BUS_REG

Address: Operational Base(0xFE000000) + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	SEC_LAT_TIMER Secondary Latency Timer. This register does not apply to PCI Express. The controller hardwires it to 00h.
23:16	RW	0x00	SUB_BUS Subordinate Bus Number. The Subordinate Bus Number register is used to record the bus number of the highest numbered PCI bus segment which is behind (or subordinate to) the bridge. Configuration software programs the value in this register. The bridge uses this register in conjunction with the Secondary Bus Number register to determine when to respond to and pass on a Type 1 configuration transaction on the primary interface to the secondary interface.
15:8	RW	0x00	SEC_BUS Secondary Bus Number. The Secondary Bus Number register is used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected. Configuration software programs the value in this register. The bridge uses this register to determine when to respond to and convert a Type 1 configuration transaction on the primary interface into a Type 0 transaction on the secondary interface.
7:0	RW	0x00	PRIM_BUS Primary Bus Number. This register is not used by PCI Express Functions. It is implemented for compatibility with legacy software.

PCIE_DSP_PF0_TYPE1_HDR_SEC_STAT_IO_LIMIT_IO_BASE_REG

Address: Operational Base(0xFE000000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RW	0x0	SEC_STAT_DPE Detected Parity Error. This bit is set by a Function when a Poisoned TLP is received by its secondary side, regardless of the state the Parity Error Response Enable bit in the Bridge Control register.
30	RW	0x0	SEC_STAT_RCVD_SYS_ERR Received System Error. This bit is set when the secondary side of a Function receives an ERR_FATAL or ERR_NONFATAL message.
29	RW	0x0	SEC_STAT_RCVD_MSTR_ABRT Received Master Abort. This bit is set when the secondary side of a Function (for requests initiated by the Type 1 header Function itself) receives a Completion with Unsupported Request Completion status.
28	RW	0x0	SEC_STAT_RCVD_TRGT_ABRT Received Target Abort. This bit is set when the secondary side of a Function (for requests initiated by the Type 1 header Function itself) receives a Completion with Completer Abort Completion status.
27	RW	0x0	SEC_STAT_SIG_TRGT_ABRT Signaled Target Abort. This bit is set when the secondary side of the Function (for Requests completed by the Type 1 header Function itself) completes a Posted or Non-Posted request as a Completer Abort error.

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Bit	Attr	Reset Value	Description
26:25	RO	0x0	RSVDP_25 Reserved for future use.
24	RW	0x0	SEC_STAT_MDPE Master Data Parity Error. This bit is set by a Function if the Parity Error Response Enable bit in the Bridge Control register is set, and either of the following two conditions occurs: - Port receives a Poisoned Completion coming Upstream - Port transmits a Poisoned Request Downstream If the Parity Error Response Enable bit is clear, this bit is never set.
23	RO	0x0	RSVDP_23 Reserved for future use.
22:16	RO	0x00	SEC_STAT_RESERV Reserved.
15:12	RW	0x0	IO_LIMIT I/O Limit Address. These bits correspond to the address[15:12] of IO address range. For the purpose of address decoding, the bridge assumes that the lower 12 address bits, address[11:0], of the I/O limit address (not implemented in the I/O Limit register) are FFFh. The I/O Limit register can be programmed to a smaller value than the I/O Base register, if there are no I/O addresses on the secondary side of the bridge. In this case, the bridge will not forward any I/O transactions from the primary bus to the secondary and will forward all I/O transactions from the secondary bus to the primary bus.
11:9	RO	0x0	IO_RESERV1 Reserved.
8	RO	0x0	IO_DECODE_BIT8 I/O Addressing Encode (IO Limit Address). This bit encodes the IO addressing capability of the bridge. Note: - For 16bit I/O address decoding, the bridge must still perform a full 32-bit decode of the I/O address (that is, check that Address[31:16] are 0000h). In this case, the I/O address range supported by the bridge will be restricted to the first 64 KB of I/O Space (0000 0000h to 0000 FFFFh). - For 16bit I/O address decoding, the bridge assumes that the upper 16 address bits, Address[31:16], of the I/O limit address (not implemented in I/O Limit register) are zero. - For 32bit I/O address decoding, and the I/O Limit Upper 16 Bits hold the upper 16 bits, corresponding to Address[31:16], of the 32-bit Limit address. In this case, system configuration software is permitted to locate the I/O address range supported by the bridge anywhere in the 4-GB I/O Space. - The 4-KB alignment and granularity restrictions still apply when the bridge supports 32-bit I/O addressing. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	IO_BASE I/O Base Address. These bits correspond to the address[15:12] of IO address range. For the purpose of address decoding, the bridge assumes that the lower 12 address bits, address[11:0], of the I/O base address (not implemented in the I/O Base register) are zero.
3:1	RO	0x0	IO_RESERV Reserved.
0	RO	0x0	IO_DECODE I/O Addressing Encode (IO Base Address). This bit encodes the IO addressing capability of the bridge. Note: - For 16bit I/O address decoding, the bridge must still perform a full 32-bit decode of the I/O address (that is, check that Address[31:16] are 0000h). In this case, the I/O address range supported by the bridge will be restricted to the first 64 KB of I/O Space (0000 0000h to 0000 FFFFh). - For 16bit I/O address decoding, the bridge assumes that the upper 16 address bits, Address[31:16], of the I/O limit address (not implemented in I/O Limit register) are zero. - For 32bit I/O address decoding, and the I/O Limit Upper 16 Bits hold the upper 16 bits, corresponding to Address[31:16], of the 32-bit Limit address. In this case, system configuration software is permitted to locate the I/O address range supported by the bridge anywhere in the 4-GB I/O Space. - The 4-KB alignment and granularity restrictions still apply when the bridge supports 32-bit I/O addressing. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

PCIE_DSP_PF0_TYPE1_HDR_MEM_LIMIT_MEM_BASE_REG

Address: Operational Base(0xFE000000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	MEM_LIMIT Memory Limit Address. These bits correspond to the upper 12 address bits, Address[31:20], of 32-bit addresses. For the purpose of address decoding, the bridge assumes that the lower 20 address bits, Address[19:0], of the memory limit address (not implemented in the Memory Limit register) are F FFFFh. The Memory Limit register must be programmed to a smaller value than the Memory Base register if there is no memory-mapped address space on the secondary side of the bridge.
19:16	RO	0x0	MEM_LIMIT_RESERV Reserved.
15:4	RW	0x000	MEM_BASE Memory Base Address. These bits correspond to the upper 12 address bits, Address[31:20], of 32-bit addresses. For the purpose of address decoding, the bridge assumes that the lower 20 address bits, Address[19:0], of the memory base address (not implemented in the Memory Base register) are zero.
3:0	RO	0x0	MEM_BASE_RESERV Reserved.

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PCIE_DSP_PF0_TYPE1_HDR_PREF_MEM_LIMIT_PREF_MEM_BASE_REG

Address: Operational Base(0xFE000000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	PREF_MEM_LIMIT Prefetchable Memory Limit Address. - If the Prefetchable Memory Limit register indicates support for 32-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read-only register that returns zero when read. - If the Prefetchable Memory Limit registers indicate support for 64-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read/write register which must be initialized by configuration software. - If a 64-bit prefetchable memory address range is supported, the Prefetchable Limit Upper 32 Bits register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit limit addresses which specify the prefetchable memory address range.
19:17	RO	0x0	PREF_RESERV1 Reserved.
16	RO	0x1	PREF_MEM_LIMIT_DECODE Prefetchable Memory Limit Decode. This bit encodes whether or not the bridge supports 64-bit addresses. Note: This bit is a copy of the PREF_MEM_DECODE bit and always reflects the current value of that bit.
15:4	RW	0x000	PREF_MEM_BASE Prefetchable Memory Base Address. - If the Prefetchable Memory Base register indicates support for 32-bit addressing, then the Prefetchable Base Upper 32 Bits register is implemented as a read-only register that returns zero when read. - If the Prefetchable Memory Base register indicates support for 64-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read/write register which must be initialized by configuration software. - If a 64-bit prefetchable memory address range is supported, the Prefetchable Base Upper 32 Bits register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range.
3:1	RO	0x0	PREF_RESERV Reserved.
0	RO	0x1	PREF_MEM_DECODE Prefetchable Memory Base Decode. This bit encodes whether or not the bridge supports 64-bit addresses. Note: By default the bit is set to 1'b1 indicating that 64-bit addresses are supported. If the bridge only supports 32-bit prefetchable memory address range, or if there is no prefetchable memory address range, then the configuration parameter MEM_DECODE_64_0 must be changed to 0. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_PREF_BASE_UPPER_REG

Address: Operational Base(0xFE000000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PREF_MEM_BASE_UPPER Prefetchable Base Upper 32 Bit. - If the Prefetchable Memory Base register indicates support for 32-bit addressing, then this register is implemented as read-only register that returns zero when read. - If the Prefetchable Memory Base register indicate support for 64-bit addressing, then this register is implemented as read/write register which must be initialized by configuration software. - This register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PREF_MEM_LIMIT_PREF_MEM_BASE_REG.PREF_MEM_DECODE ? RW : RO

PCIE_DSP_PF0_TYPE1_HDR_PREF_LIMIT_UPPER_REG

Address: Operational Base(0xFE000000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PREF_MEM_LIMIT_UPPER Prefetchable Limit Upper 32 Bit. - If the Prefetchable Memory Limit register indicate support for 64-bit addressing, then this register is implemented as read/write register which must be initialized by configuration software. - This register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PREF_MEM_LIMIT_PREF_MEM_BASE_REG.PREF_MEM_DECODE ? RW : RO

PCIE_DSP_PF0_TYPE1_HDR_IO_LIMIT_UPPER_IO_BASE_UPPER_REG

Address: Operational Base(0xFE000000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	IO_LIMIT_UPPER I/O Limit Upper 16 Bits. - If the I/O Limit register indicates support for 16-bit I/O address decoding, then this register is implemented as a read-only register which return zero when read. - If the I/O Limit register indicates support for 32-bit I/O addressing, then this register must be initialized by configuration software. - If 32-bit I/O address decoding is supported, this register specifies the upper 16 bits, corresponding to Address[31:16], of the 32-bit limit address, that specify the I/O address range. - See the PCI-to-PCI Bridge Architecture Specification for additional details). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: SEC_STAT_IO_LIMIT_IO_BASE_REG.IO_DECODE ? RW : RO

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	IO_BASE_UPPER I/O Base Upper 16 Bits. - If the I/O Base register indicates support for 16-bit I/O address decoding, then this register is implemented as a read-only register which return zero when read. - If the I/O base register indicates support for 32-bit I/O addressing, then this register must be initialized by configuration software. - If 32-bit I/O address decoding is supported, this register specifies the upper 16 bits, corresponding to Address[31:16], of the 32-bit base address, that specify the I/O address range. - See the PCI-to-PCI Bridge Architecture Specification for additional details. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: SEC_STAT_IO_LIMIT_IO_BASE_REG.IO_DECODE ? RW : RO

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_CAP_PTR_REG

Address: Operational Base(0xFE000000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7:0	RO	0x40	CAP_POINTER Capabilities Pointer. This register is used to point to a linked list of capabilities implemented by this Function. Since all PCI Express Functions are required to implement the PCI Express Capability structure, this register must point to a valid capability structure and either this structure is the PCI Express Capability structure, or a subsequent list item points to the PCI Express Capability structure. The bottom two bits are Reserved and must be set to 00b. Software must mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_EXP_ROM_BASE_REG

Address: Operational Base(0xFE000000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	EXP_ROM_BASE_ADDRESS Expansion ROM Base Address. Upper 21 bits of the Expansion ROM base address. The number of bits (out of these 21) that a Function actually implements depends on how much address space the Function requires. The mask for this ROM BAR exists (if implemented) as a shadow register at this address. The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the second register at this address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	RSVDP_8 Reserved for future use.
7:4	RW	0x0	ROM_BAR_VALIDATION_DETAILS Expansion ROM Validation Details. The field contains optional, implementation-specific details associated with Expansion ROM Validation. - If validation is in progress (Expansion ROM Validation Status is 001b), non-zero values of this field represent implementation-specific indications of the phase of the validation progress (e.g., 50% complete). The value 0000b indicates that no validation progress information is provided. - If validation is completed (Expansion ROM Validation Status 010b to 111b inclusive), non-zero values in this field represent additional implementation-specific information. The value 0000b indicates that no information is provided. - When validation is supported and this field is not implemented, this field must be hardwired to 0000b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1 && DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
3:1	RW	0x0	ROM_BAR_VALIDATION_STATUS Expansion ROM Validation Status. When this field is non-zero, it indicates the status of hardware validation of the Expansion ROM contents. - If the Function does not support validation, this field must be hardwired to 000b. - It is optional whether an implementation is capable of returning Validation Status values 011b, 101b, 110b, or 111b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1 && DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
0	RW	0x0	ROM_BAR_ENABLE Expansion ROM Enable. This bit controls whether or not the Function accepts accesses to its expansion ROM. The Memory Space Enable bit in the Command register has precedence over the Expansion ROM Enable bit. A Function must claim accesses to its expansion ROM only if both the Memory Space Enable bit and the Expansion ROM Enable bit are set. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R

PCIE_DSP_PF0_TYPE1_HDR_BRIDGE_CTRL_INT_PIN_INT_LINE_REG

Address: Operational Base(0xFE000000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	BRIDGE_CTRL_RESERV Reserved.

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Bit	Attr	Reset Value	Description
22	RW	0x0	SBR Secondary Bus Reset. Setting this bit triggers a hot reset on the corresponding PCI Express Port. Software must ensure a minimum reset duration (Trst) as defined in the PCI Local Bus Specification. Software and systems must honor first-access-following-reset timing requirements, unless the Readiness Notifications mechanism is used or if the Immediate Readiness bit in the relevant Function's Status Register register is set. Port configuration registers must not be changed, except as required to update Port status.
21	RO	0x0	MSTR_ABORT_MODE Master Abort Mode. This bit was originally described in the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
20	RO	0x0	VGA_16B_DEC VGA 16 bit decode. This bit only has meaning if VGA Enable bit is set. This bit enables system configuration software to select between 10-bit and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary. For Functions that do not support VGA, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R

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Bit	Attr	Reset Value	Description
19	RO	0x0	VGA_EN VGA Enable. Modifies the response by the bridge to VGA compatible addresses. If the VGA Enable bit is set, the bridge will positively decode and forward the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): - Memory accesses in the range 000A 0000h to 000B FFFFh - I/O addresses in the first 64 KB of the I/O address space (Address[31:16] are 0000h) where Address[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases determined by the setting of VGA 16-bit Decode) If the VGA Enable bit is set, forwarding of these accesses is independent of the I/O address range and memory address ranges defined by the I/O Base and Limit registers, the Memory Base and Limit registers, and the Prefetchable Memory Base and Limit registers of the bridge. (Forwarding of these accesses is also independent of the setting of the ISA Enable bit (in the Bridge Control register) when the VGA Enable bit is set. Forwarding of these accesses is qualified by the I/O Space Enable and Memory Space Enable bits in the Command register.) For Functions that do not support VGA, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
18	RW	0x0	ISA_EN ISA Enable. Modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions will be forwarded if they address the last 768 bytes in each 1-KB block.
17	RW	0x0	SERR_EN SERR# Enable. This bit controls forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary.
16	RW	0x0	PERE Parity Error Response Enable. This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Secondary Status register.
15:8	RO	0x01	INT_PIN Reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RW	0xff	INT_LINE Reserved

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7.4.3.2 PCIE_DSP_PF0_PM_CAP

7.4.3.2.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PM_CAP_CAP_ID_NXT_PTR_REG	0x0000	W	0xDFC35001	This register provides information refarding the Power Management Capabilities.
PCIE_DSP_PF0_PM_CAP_CON_STATUS_REG	0x0004	W	0x00000008	This register is used to manage the PCI function's power management state as well as to enable/monitor PMEs.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.2.2 Detail Registers Description

PCIE_DSP_PF0_PM_CAP_CAP_ID_NXT_PTR_REG

Address: Operational Base(0xFE000040) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x1b	PME_SUPPORT PME_Support. This 5-bit field indicates the power states in which the function may generate a PME and/or forward PME messages. A value of 0b for any bit indicates that the function is not capable of asserting PME while in that power state. - bit(27) X XXX1b - PME can be generated from D0 - bit(28) X XX1Xb - PME can be generated from D1 - bit(29) X X1XXb - PME can be generated from D2 - bit(30) X 1XXXb - PME can be generated from D3hot - bit(31) 1 XXXXb - PME can be generated from D3cold Bit 31 (PME can be asserted from D3cold) represents a special case. Functions that set this bit require some sort of auxiliary power source. Implementation specific mechanisms are recommended to validate that the power source is available before setting this bit. Each bit that corresponds to a supported D-state must be set for PCI-PCI Bridge structures representing Ports on Root Complexes/Switches to indicate that the Bridge will forward PME Messages. Bit 31 must only be set if the Port is still able to forward PME Messages when main power is not available. The read value from this field is the write value && (sys_aux_pwr_det, 1'b1, D2_SUPPORT, D1_SUPPORT, 1'b1), where D1_SUPPORT and D2_SUPPORT are fields in this register. The reset value PME_SUPPORT_n && (sys_aux_pwr_det, 1'b1, D2_SUPPORT, D1_SUPPORT, 1'b1), where PME_SUPPORT_n is a configuration parameter. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
26	RO	0x1	D2_SUPPORT D2_Support. If this bit is set, this function supports the D2 Power Management state. Functions that do not support D2 must always return a value of 0b for this bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
25	RO	0x1	D1_SUPPORT D1_Support. If this bit is set, this function supports the D1 Power Management state. Functions that do not support D1 must always return a value of 0b for this bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
24:22	RO	0x7	AUX_CURR Aux_Current. This 3 bit field reports the Vaux auxiliary current requirements for the function. If this function implements the Data Register, the controller hardwires this field to 000b. If PME_Support is 0 xxxxb (PME assertion from D3cold is not supported), the controller hardwires this field to 0000b. For functions where PME_Support is 1 xxxxb (PME assertion from D3cold is supported), and which do not implement the Data field, the encodings defined in Values: apply: Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
21	RO	0x0	DSI Device Specific Initialization. The DSI bit indicates whether special initialization of this function is required. When set, indicates that the function requires a device specific initialization sequence following a transition to the D0uninitialized state. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
20	RO	0x0	reserved
19	RO	0x0	PME_CLK PME Clock. Does not apply to PCI Express, the controller hardwires it to 0b. Note: This register field is sticky.
18:16	RO	0x3	PM_SPEC_VER Version. This field provides the Power Management specification version. The controller hardwires this field to 011b for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0>. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:8	RO	0x50	PM_NEXT_POINTER Next Capability Pointer. This field provides an offset into the function's configuration space pointing to the location of next item in the capabilities list. If there are no additional items in the capabilities list, this field is set to 00h. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RO	0x01	PM_CAP_ID Capability ID. This field returns 01h to indicate that this is the PCI Power Management Capability. Each function may have only one item in its capability list with Capability ID set to 01h.

PCIE_DSP_PF0_PM_CAP_CON_STATUS_REG

Address: Operational Base(0xFE000040) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DATA_REG_ADD_INFO Data. This field is used to report the state dependent data requested by the Data_Select field. The value of this field is scaled by the value reported by the Data_Scale field.
23	RO	0x0	BUS_PWR_CLK_CON_EN Bus Power/Clock Control Enable. If this field is set, Bus Power/Clock Control is Enable.
22	RO	0x0	B2_B3_SUPPORT B2B3 Support for D3hot. If this field is set, B2B3 support for D3hot is available.
21:16	RO	0x00	RSVDP_16 Reserved for future use.
15	RW	0x0	PME_STATUS PME_Status. This bit is set when the function normally generates a PME signal. The value of this bit is not affected by the value of the PME_En bit. If PME_Support bit 31 of the Power Management Capabilities register is clear, this bit is permitted to be hardwired to 0b. Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this register value is not modified by Conventional Reset or FLR. Note: This register field is sticky.
14:13	RO	0x0	DATA_SCALE Data_Scale. This field indicates the scaling factor to be used when interpreting the value of the Data field. The value and meaning of this field varies depending on which data value has been selected by the Data_Select field. For more details, see 7.5.2.3 section of PCI Express Base Specification.
12:9	RO	0x0	DATA_SELECT Data_Select. This 4-bit field is used to select which data is to be reported through the Data and Data_Scale field. If the Data field is not implemented, this field must be hardwired to 0000b.

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Bit	Attr	Reset Value	Description
8	RW	0x0	PME_ENABLE PME_En. - When set, the function is permitted to generate a PME. - When clear, the function is not permitted to generate a PME. If PME_Support is 1 xxxxb (PME generation from D3cold) or the function consumes Aux power and Aux power is available this bit is RWS and the bit is not modified by Conventional Reset or FLR. If PME_Support is 0 xxxxb, this field is not sticky (RW). If PME_Support is 0 0000b, the controller hardwires this bit to 0b. Note: This register field is sticky.
7:4	RO	0x0	RSVDP_4 Reserved for future use.
3	RO	0x1	NO_SOFT_RST No_Soft_Reset. This bit indicates the state of the function after writing the PowerState field to transition the function from D3hot to D0. - When set, this transition preserves internal function state. The function is in D0Active and no additional software intervention is required. - When clear, this transition results in undefined internal function state. Regardless of this bit, functions that transition from D3hot to D0 by Fundamental Reset will return to D0Uninitialized with only PME context preserved if PME is supported and enabled. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
2	RO	0x0	RSVDP_2 Reserved for future use.
1:0	RW	0x0	POWER_STATE PowerState. This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. You can write to this register; however, the read-back value is the actual power state, not the write value. If you attempt to write an unsupported, optional state to this field, the write operation completes normally; however, the data is discarded and no state change occurs. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

7.4.3.3 PCIE_DSP_PF0_MSI_CAP

7.4.3.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_MSI_CAP_PCI_MSI_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x008A7005	This register holds MSI Capability Header information and controls the MSI behaviour.
PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_04H_REG	0x0004	W	0x00000000	This register holds the system specified message address for an MSI transaction.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_08H_REG	0x0008	W	0x00000000	For a function that supports a 32-bit message address, - bits[31:16] of this register represent the Extended Message Data, and - bits[15:0] of this register represent the Message DataFor a function that supports a 64-bit message address (bit 23 in PCI_MSI_CAP_ID_NEXT_CTRL_REG register set), this register represents the Message Upper Address Register for MSI (Offset 08h). It specifies the Message Upper Address (System-specified message upper address). This register is required for PCI Express Endpoints and is optional for other function types. If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register (if non-zero) specify the upper 32-bits of a 64-bit message address (Address[63:32]). If the contents of this register are zero, the Function uses the 32 bit address specified by the Message Address register.
PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_0CH_REG	0x000C	W	0x00000000	For a function that supports a 32-bit message address, this register contains the Mask Bits when the Per-Vector Masking Capable bit (bit 24 of PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set.For a function that supports a 64-bit message address, this register contains Message Data.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.3.2 Detail Registers Description

PCIE_DSP_PF0_MSI_CAP_PCI_MSI_CAP_ID_NEXT_CTRL_REG

Address: Operational Base(0xFE000050) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.

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Bit	Attr	Reset Value	Description
26	RW	0x0	PCI_MSI_EXT_DATA_EN Extended Message Data Enable. - If set, the function is enabled to provide Extended Message Data. - If clear, the function is not enabled to provide Extended Message Data. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_MSI_EXT_DATA_CAP ? RW : RO
25	RO	0x0	PCI_MSI_EXT_DATA_CAP Extended Message Data Capable. - If set, the function is capable of providing Extended Message Data. - If clear, the function does not support providing Extended Message Data. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
24	RO	0x0	PCI_PVM_SUPPORT Per-Vector Masking Capable. - If set, the function supports MSI Per-Vector Masking. - If clear, the function does not support MSI Per-Vector Masking.
23	RO	0x1	PCI_MSI_64_BIT_ADDR_CAP 64 bit address capable. - If set, the function is capable of sending a 64-bit message address. - If clear, the function is not capable of sending a 64-bit message address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
22:20	RW	0x0	PCI_MSI_MULTIPLE_MSG_EN Multiple Message Enable. Software writes to this field to indicate the number of allocated vectors (equal to or less than the number of requested vectors). The number of allocated vectors is aligned to a power of two. If a function requests four vectors (indicated by a Multiple Message Capable encoding of 010b), system software can allocate either four, two, or one vector by writing a 010b, 001b, or 000b to this field, respectively. When MSI is enabled, a function will be allocated at least 1 vector. All encodings other than the defined encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

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Bit	Attr	Reset Value	Description
19:17	RO	0x5	PCI_MSI_MULTIPLE_MSG_CAP Multiple Message Capable. System software reads this field to determine the number of requested vectors. The number of requested vectors must be aligned to a power of two (if a function requires three vectors, it requests four by initializing this field to 010b). All encodings other than the defined encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
16	RW	0x0	PCI_MSI_ENABLE MSI Enable. - If set and the MSI-X Enable bit in the MSI-X Message Control register is clear, the function is permitted to use MSI to request service and is prohibited from using INTx interrupts. System configuration software sets this bit to enable MSI. A device driver is prohibited from writing this bit to mask a function's service request. For more details on control of INTx interrupts, see section 7.5.1.1 of PCI Express Base Specification. - If clear, the function is prohibited from using MSI to request service. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
15:8	RO	0x70	PCI_MSI_CAP_NEXT_OFFSET Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RO	0x05	PCI_MSI_CAP_ID Capability ID. Indicates the MSI Capability structure. This field returns a Capability ID of 05h indicating that this is an MSI Capability structure.

PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_04H_REG

Address: Operational Base(0xFE000050) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	PCI_MSI_CAP_OFF_04H Message Address - System-specified message address. If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG register) is set, the contents of this field specify the DWORD-aligned address (Address[31:02]) for the MSI transaction. Address[1:0] are set to 00b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
1:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_08H_REG

Address: Operational Base(0xFE000050) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PCI_MSI_CAP_OFF_0AH For a function that supports a 32-bit message address, this field contains Extended Message Data (System-specified message data). For the MSI Capability structures without per-vector masking, it must be implemented if the Extended Message Data Capable bit is set; otherwise, it is outside the MSI Capability structure and undefined. For the MSI Capability structures with Per-vector Masking, it must be implemented if the Extended Message Data Capable bit is set; otherwise, it is RsvdP. If the Extended Message Data Enable bit (bit 26 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the DWORD Memory Write transaction uses Extended Message Data for the upper 16 bits; otherwise, it uses 0000h for the upper 16 bits. For a function that supports a 64-bit message address, it contains upper 16 bits of the Message Upper Address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PCI_MSI_64_BIT_ADDR_CAP || `DEFAULT_EXT_MSI_DATA_CAPABLE ? R/W : R
15:0	RW	0x0000	PCI_MSI_CAP_OFF_08H For a function that supports a 32-bit message address, this field contains Message Data (System-specified message data). If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the function sends a DWORD Memory Write transaction using Message Data for the lower 16 bits. All 4 Byte Enables are set. The Multiple Message Enable field (bits 22:20 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010b indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000b, the Function is not permitted to modify the message data. For a function that supports a 64-bit message address, it contains lower 16 bits of the Message Upper Address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_0CH_REG

Address: Operational Base(0xFE000050) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PCI_MSI_CAP_OFF_0EH For a function that supports a 32-bit message address, this field contains the upper Mask Bits when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For a function that supports a 64-bit message address, this field contains Message Data (System-specified message data). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: (!MSI_64_EN && MSI_PVM_EN_VALUE) ? RW: MSI_64_EN && DEFAULT_EXT_MSI_DATA_CAPABLE ? RW : RO

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	PCI_MSI_CAP_OFF_0CH For a function that supports a 32-bit message address, this field contains the lower Mask Bits when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For a function that supports a 64-bit message address, this field contains Message Data (System-specified message data). If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the function sends a DWORD Memory Write transaction using Message Data for the lower 16 bits. All 4 Byte Enables are set. The Multiple Message Enable field (bits 22:20 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010b indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000b, the Function is not permitted to modify the message data. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PCI_MSI_64_BIT_ADDR_CAP || MSI_PVM_EN ? R/W : R

7.4.3.4 PCIE_DSP_PF0_PCIE_CAP

7.4.3.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PCIE_CAP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	0x0000	W	0x0042B010	This is the PCI Express Capabilities, ID, and Next Pointer Register.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES_REG	0x0004	W	0x00008000	The Device Capabilities register identifies PCI Express device function specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS	0x0008	W	0x00102010	This register controls PCI Express device specific parameters and provides information about PCI Express device (function) specific parameters.
PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES_REG	0x000C	W	0x0072AC13	The Link Capabilities register identifies PCI Express Link specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG	0x0010	W	0x10110000	This register controls and provides information about PCI Express Link specific parameters.
PCIE_DSP_PF0_PCIE_CAP_SLOT_CAPABILITIES_REG	0x0014	W	0x00000000	The Slot Capabilities register identifies PCI Express slot specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS	0x0018	W	0x004003C0	This register controls and provides information about PCI Express Slot specific parameters.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG	0x001C	W	0x00010000	This register controls PCI Express Root Complex specific parameters and identifies PCI Express Root Port specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_ROOT_STATUS_REG	0x0020	W	0x00000000	The Root Status register provides information about PCI Express device specific parameters.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES2_REG	0x0024	W	0x000C0C10	This register identifies PCI Express device specific capabilities; in addition to the Device Capabilities Register.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG	0x0028	W	0x00000000	This register controls PCI Express device specific parameters and provides information about PCI Express device (function) specific parameters; in addition to the Device Control and Device Status Register.
PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES2_REG	0x002C	W	0x0000000E	This register identifies PCI Express Link specific capabilities; in addition to the Link Capabilities Register.
PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG	0x0030	W	0x00010003	This register controls and provides information about PCI Express Link specific parameters; in addition to the Link Control and Link Status Register.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.4.2 Detail Registers Description

PCIE_DSP_PF0_PCIE_CAP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG

Address: Operational Base(0xFE000070) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30	RO	0x0	RSVD Reserved.

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Bit	Attr	Reset Value	Description
29:25	RO	0x00	PCIE_INT_MSG_NUM PCIE Interrupt Message Number. Interrupt Message Number. This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
24	RO	0x0	PCIE_SLOT_IMP Slot Implemented. When set, this bit indicates that the Link associated with this Port is connected to a slot (as compared to being connected to a system-integrated device or being disabled). This bit is valid for Downstream Ports. This bit is undefined for Upstream Ports. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
23:20	RO	0x4	PCIE_DEV_PORT_TYPE Device/Port Type. Indicates the specific type of this PCI Express function. Note: Different functions in a Multi-Function Device can generally be of different types. Defined encodings for functions that implement a Type 00h PCI Configuration Space header are: Defined encodings for functions that implement a Type 01h PCI Configuration Space header are: All other encodings are Reserved. Note: Different Endpoint types have notably different requirements in Section 1.3.2 of PCI Express Base Specification regarding I/O resources, Extended Configuration Space, and other capabilities.

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Bit	Attr	Reset Value	Description
19:16	RO	0x2	PCIE_CAP_REG Capability Version. Indicates PCI-SIG defined PCI Express Capability structure version number. A version of the specification that changes the PCI Express Capability structure in a way that is not otherwise identifiable (for example, through a new Capability field) is permitted to increment this field. All such changes to the PCI Express Capability structure must be software-compatible. Software must check for Capability Version numbers that are greater than or equal to the highest number defined when the software is written, as functions reporting any such Capability Version numbers will contain a PCI Express Capability structure that is compatible with that piece of software. The controller hardwires this field to 2h for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0. Note: This register field is sticky.
15:8	RO	0xb0	PCIE_CAP_NEXT_PTR Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RO	0x10	PCIE_CAP_ID Capability ID. Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES_REG

Address: Operational Base(0xFE000070) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15	RO	0x1	PCIE_CAP_ROLE_BASED_ERR_REPORT Role-Based Error Reporting. When set, this bit indicates that the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be set by all functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
14:6	RO	0x000	RSVDP_6 Reserved for future use.

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Bit	Attr	Reset Value	Description
5	RO	0x0	PCIE_CAP_EXT_TAG_SUPP Extended Tag Field Supported. This bit, in combination with the 10-Bit Tag Requester Supported bit in the Device Capabilities 2 register, indicates the maximum supported size of the Tag field as a Requester. This bit must be set if the 10-Bit Tag Requester Supported bit is set. Note: 8-bit Tag field generation must be enabled by the Extended Tag Field Enable bit in the Device Control register of the Requester Function before 8-bit Tags can be generated by the Requester. See Section 2.2.6.2 of PCI Express Base Specification for interactions with enabling the use of 10-Bit Tags. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
4:3	RO	0x0	PCIE_CAP_PHANTOM_FUNC_SUPPORT Phantom Functions Supported. This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers (called Phantom Functions) with the Tag identifier (see Section 2.2.6.2 of PCI Express Base Specification for a description of Tag Extensions). With every Function in an ARI Device, the Phantom Functions Supported field must be set to 00b. The remainder of this field description applies only to non-ARI Multi-Function Devices. This field indicates the number of most significant bits of the Function Number portion of Requester ID that are logically combined with the Tag identifier. Note: Phantom Function support for the function must be enabled by the Phantom Functions Enable field in the Device Control register before the Function is permitted to use the Function Number field in the Requester ID for Phantom Functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
2:0	RO	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE Max_Payload_Size Supported. This field indicates the maximum payload size that the function can support for TLPs. All encodings other than the defined encodings are reserved. The functions of a Multi-Function Device are permitted to report different values for this field. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS

Address: Operational Base(0xFE000070) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	RSVDP_22 Reserved for future use.

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Bit	Attr	Reset Value	Description
21	RO	0x0	PCIE_CAP_TRANS_PENDING Transactions Pending. Root and Switch Ports: The controller hardwires this bit to 0b.
20	RO	0x1	PCIE_CAP_AUX_POWER_DETECTED AUX Power Detected. Functions that require Aux power report this bit as set if Aux power is detected by the function. This bit is derived by sampling the sys_aux_pwr_det input.
19	RW	0x0	PCIE_CAP_UNSUPPORTED_REQ_DETECTED Unsupported Request Detected. This bit indicates that the function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function Device, each function indicates status of errors as perceived by the respective function.
18	RW	0x0	PCIE_CAP_FATAL_ERR_DETECTED Fatal Error Detected. This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.
17	RW	0x0	PCIE_CAP_NON_FATAL_ERR_DETECTED Non-Fatal Error Detected. This bit indicates status of Non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.
16	RW	0x0	PCIE_CAP_CORR_ERR_DETECTED Correctable Error Detected. This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Correctable Error Mask register.
15	RO	0x0	reserved
14:12	RW	0x2	PCIE_CAP_MAX_READ_REQ_SIZE Max_Read_Request_Size. This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For functions that do not generate Read Requests larger than 128 bytes and functions that do not generate Read Requests on their own behalf, the controller implements this field as Read Only (RO) with a value of 000b.

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Bit	Attr	Reset Value	Description
11	RO	0x0	PCIE_CAP_EN_NO_SNOOP Enable No Snoop. If this bit is set, the function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency (see section 2.2.6.5 in PCI Express Base Specification). Note: Setting this bit to 1b should not cause a function to set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a function is only permitted to set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. The controller hardwires this bit 0b if a function would never set the No Snoop attribute in transactions it initiates. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
10	RW	0x0	PCIE_CAP_AUX_POWER_PM_EN Aux Power PM Enable. This bit is derived by sampling the sys_aux_pwr_det input. When set this bit, enables a function to draw Aux power independent of PME Aux power. Functions that require Aux power on legacy operating systems should continue to indicate PME Aux power requirements. Aux power is allocated as requested in the Aux_Current field of the Power Management Capabilities register (PMC), independent of the PME_En bit in the Power Management Control/Status register (PMCSR). For Multi-Function devices, a component is allowed to draw Aux power if at least one of the functions has this bit set. Note: Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this bit is not modified by Conventional Reset. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9	RO	0x0	PCIE_CAP_PHANTOM_FUNC_EN Phantom Functions Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, - If this bit is set, it enables a function to use unclaimed functions as Phantom functions to extend the number of outstanding transaction identifiers - If this bit is clear, the function is not allowed to use Phantom functions For more details, see section 2.2.6.2 of PCI Express Base Specification. Software should not change the value of this bit while the function has outstanding Non-Posted Requests; otherwise, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_PHANTOM_FUNC_SUPPORT ? RW : RO
8	RO	0x0	PCIE_CAP_EXT_TAG_EN Extended Tag Field Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, - If the Extended Tag Field Enable bit is set, the function is permitted to use an 8-bit Tag field as a Requester - If the Extended Tag Field Enable bit is clear, the Function is restricted to a 5-bit Tag field See section 2.2.6.2 of PCI Express Base Specification for required behavior when the 10-Bit Tag Requester Enable bit is set. If software changes the value of the Extended Tag Field Enable bit while the function has outstanding Non-Posted Requests, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_EXT_TAG_SUPP ? RW : RO

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE_CS Max_Payload_Size. This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported field (PCIE_CAP_MAX_PAYLOAD_SIZE) in the Device Capabilities (DEVICE_CAPABILITIES_REG) register (for more details, see section 7.5.3.3 of PCI Express Base Specification). This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For Functions that support only the 128-byte max payload size, the controller hardwires this field to 000b. System software is not required to program the same value for this field for all the Functions of a Multi-Function device (for more details, see section 2.2.2 of PCI Express Base Specification). For ARI Devices, Max_Payload_Size is determined solely by the setting in Function0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
4	RW	0x1	PCIE_CAP_EN_REL_ORDER Enable Relaxed Ordering. If this bit is set, the function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering (for more details, see section 2.2.6.4 and section 2.4 of PCI Express Base Specification). For a function that never sets the Relaxed Ordering attribute in transactions it initiates as a Requester, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
3	RW	0x0	PCIE_CAP_UNSUPPORT_REQ_REP_EN Unsupported Request Reporting Enable. This bit, in conjunction with other bits, controls the signaling of Unsupported Request Errors by sending error Messages (for more details, see section 6.2.5 and section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each Function from point-of-view of the respective Function.
2	RW	0x0	PCIE_CAP_FATAL_ERR_REPORT_EN Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_FATAL Messages (for more details, see section 6.2.5 and section 6.2.6 of of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL Message is generated.

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Bit	Attr	Reset Value	Description
1	RW	0x0	PCIE_CAP_NON_FATAL_ERR_REPORT_EN Non-Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages (for more details, see section 6.2.5 and Section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each function from point-of-view of the respective Function. For a Root Port, the reporting of Non-fatal errors is internal to the root. No external ERR_NONFATAL Message is generated.
0	RW	0x0	PCIE_CAP_CORR_ERR_REPORT_EN Correctable Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_COR Messages (for more details, see section 6.2.5, section 6.2.6, and section 6.2.10.2 of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR Message is generated.

PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES_REG

Address: Operational Base(0xFE000070) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	PCIE_CAP_PORT_NUM Port Number. This field indicates the PCI Express Port number for the given PCI Express Link. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RO	0x1	PCIE_CAP_ASPM_OPT_COMPLIANCE ASPM Optionality Compliance. This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
21	RO	0x1	PCIE_CAP_LINK_BW_NOT_CAP Link Bandwidth Notification Capability. A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This capability is required for all Root Ports and Switch Downstream Ports supporting Links wider than x1 and/or multiple Link speeds. This field is not applicable and is Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
20	RO	0x1	PCIE_CAP_DLL_ACTIVE_REP_CAP Data Link Layer Link Active Reporting Capable. For a Downstream Port, the controller hardwires this bit to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable bit of the Slot Capabilities register) or a Downstream Port that supports Link speeds greater than 5.0 GT/s, the controller hardwires this bit to 1b. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b.
19	RO	0x0	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP Surprise Down Error Reporting Capable. For a Downstream Port, this bit must be set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
18	RO	0x0	PCIE_CAP_CLOCK_POWER_MAN Clock Power Management. For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a Multi-Function device associated with an Upstream Port, each Function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the Multi-Function device indicate a 1b in this bit. For ARI Devices, all Functions must indicate the same value in this bit. For Downstream Ports, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
17:15	RO	0x5	PCIE_CAP_L1_EXIT_LATENCY L1 Exit Latency. This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from ASPM L1 to L0. If ASPM L1 is not supported, the value is undefined. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
14:12	RO	0x2	PCIE_CAP_L0S_EXIT_LATENCY L0s Exit Latency. This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. If L0s is not supported, the value is undefined; however, see the Implementation Note "Potential Issues With Legacy Software When L0s is Not Supported" in section 5.4.1.1 of PCI Express Base Specification for the recommended value. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
11:10	RO	0x3	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT Active State Power Management (ASPM) Support. This field indicates the level of ASPM supported on the given PCI Express Link. For more details on ASPM support requirements, see section 5.4.1 of PCI Express Base Specification. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9:4	RO	0x01	PCIE_CAP_MAX_LINK_WIDTH Maximum Link Width. This field indicates the maximum Link width (xN - corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. All encodings other than the defined encodings are reserved. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
3:0	RO	0x3	PCIE_CAP_MAX_LINK_SPEED Max Link Speed. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. All encodings other than the defined encodings are reserved. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG

Address: Operational Base(0xFE000070) + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	PCIE_CAP_LINK_AUTO_BW_STATUS Link Autonomous Bandwidth Status. This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b.

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Bit	Attr	Reset Value	Description
30	RW	0x0	PCIE_CAP_LINK_BW_MAN_STATUS Link Bandwidth Management Status. This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit. Note: This bit is set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. The default value of this bit is 0b. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG.
29	RO	0x0	PCIE_CAP_DLL_ACTIVE Data Link Layer Link Active. This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the Data Link Layer Link Active Reporting Capable bit is 1b. Otherwise, the controller hardwires it to 0b.
28	RO	0x1	PCIE_CAP_SLOT_CLK_CONFIG Slot Clock Configuration. This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference clock on the connector, this bit must be clear. For a Multi-Function Device, each Function must report the same value for this bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
27	RO	0x0	PCIE_CAP_LINK_TRAINING Link Training. This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches, and the controller hardwires it to 0b.
26	RO	0x0	RSVDP_26 Reserved for future use.
25:20	RO	0x01	PCIE_CAP_NEGO_LINK_WIDTH Negotiated Link Width. This field indicates the negotiated width of the given PCI Express Link. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up.

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Bit	Attr	Reset Value	Description
19:16	RO	0x1	PCIE_CAP_LINK_SPEED Current Link Speed. This field indicates the negotiated Link speed of the given PCI Express Link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up.
15:14	RW	0x0	PCIE_CAP_DRS_SIGNALING_CONTROL DRS Signaling Control. Indicates the mechanism used to report reception of a DRS message. Must be implemented for Downstream Ports with the DRS Supported bit Set in the Link Capabilities 2 Register. Encodings are: If DRS Supported is set, receiving a DRS Message will set DRS Message Received in the Link Status 2 Register but will otherwise have no effect If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, and either MSI or MSI-X is enabled, an MSI or MSI-X interrupt is generated using the vector in Interrupt Message Number (section 7.5.3.2) If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, the Port must send an FRS Message Upstream with the FRS Reason field set to DRS Message Received. Behavior is undefined if this field is set to 10b and the FRS Supported bit in the Device Capabilities 2 Register is Clear. Behavior is undefined if this field is set to 11b. For Downstream Ports with the DRS Supported bit clear in the Link Capabilities 2 register, the controller hardwires this field to 00b. This field is Reserved for Upstream Ports. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES2_REG.DRS_SUPPORTED ? RW : RO
13:12	RO	0x0	RSVDP_12 Reserved for future use.
11	RW	0x0	PCIE_CAP_LINK_AUTO_BW_INT_EN Link Autonomous Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO

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Bit	Attr	Reset Value	Description
10	RW	0x0	PCIE_CAP_LINK_BW_MAN_INT_EN Link Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO
9	RW	0x0	PCIE_CAP_HW_AUTO_WIDTH_DISABLE Hardware Autonomous Width Disable. When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. For components that do not implement the ability autonomously to change Link width, the ciontroller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

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Bit	Attr	Reset Value	Description
8	RW	0x0	PCIE_CAP_EN_CLK_POWER_MAN Enable Clock Power Management. Applicable only for Upstream Ports and with form factors that support a "Clock Request" (CLKREQ#) mechanism, this bit operates as follows: For a non-ARI Multi-Function Device, power-management-configuration software must only Set this bit if all Functions of the Multi-Function Device indicate a 1b in the Clock Power Management bit of the Link Capabilities register. The component is permitted to use the CLKREQ# signal to power manage Link clock only if this bit is Set for all Functions. For ARI Devices, Clock Power Management is enabled solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. The CLKREQ# signal may also be controlled via the L1 PM Substates mechanism. Such control is not affected by the setting of this bit. For Downstream Ports and components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities register), the controller hardwires this bit to 0b. The write value is gated with the PCIE_CAP_CLOCK_POWER_MAN field in LINK_CAPABILITIES_REG. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_CLOCK_POWER_MAN ? RWS : ROS Note: This register field is sticky.
7	RW	0x0	PCIE_CAP_EXTENDED_SYNCH Extended Synch. When set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state (see section 4.2.4.5 of PCI Express Base Specification) and when in the Recovery state (see section 4.2.6.4.1 of PCI Express Base Specification). This mode provides external devices (for example, logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. For Multi-Function devices if any function has this bit set, then the component must transmit the additional Ordered Sets when exiting L0s or when in Recovery.

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Bit	Attr	Reset Value	Description
6	RW	0x0	PCIE_CAP_COMMON_CLK_CONFIG Common Clock Configuration. When set, this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0b indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. For non-ARI Multi-Function Devices, software must program the same value for this bit in all Functions. If not all functions are Set, then the component must as a whole assume that its reference clock is not common with the Upstream component. For ARI Devices, Common Clock Configuration is determined solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies. After changing the value in this bit in both components on a Link, software must trigger the Link to retrain by writing a 1b to the Retrain Link bit of the Downstream Port.
5	RW	0x0	PCIE_CAP_RETRAIN_LINK Retrain Link. A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. If the LTSSM is already in Recovery or Configuration, re-entering Recovery is permitted but not required. If the Port is in DPC when a write of 1b to this bit occurs, the result is undefined. Reads of this bit always return 0b. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. This bit is not applicable and is Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. This bit always returns 0b when read. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description

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Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_LINK_DISABLE Link Disable. This bit disables the Link by directing the LTSSM to the Disabled state when set; this bit is Reserved on Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. After clearing this bit, software must honor timing requirements defined in Section 6.6.1 with respect to the first Configuration Read following a Conventional Reset. In a DSP that supports crosslink, the controller gates the write value with the CROSS_LINK_EN field in PORT_LINK_CTRL_OFF. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: CX_CROSSLINK_ENABLE=1 && PORT_LINK_CTRL_OFF.CROSS_LINK_EN=1||CX_CROSSLINK_ENABLE=0 && dsp=1? RW : RO
3	RO	0x0	PCIE_CAP_RCB Read Completion Boundary (RCB). Root Ports: Indicates the RCB value for the Root Port. Refer to section 2.3.1.1 of PCI Express Base Specification for the definition of the parameter RCB. The controller hardwires this bit for a Root Port and returns its RCB support capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
2	RO	0x0	RSVDP_2 Reserved for future use.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	PCIE_CAP_ACTIVE_STATE_LINK_PM_CONTROL Active State Power Management (ASPM) Control. This field controls the level of ASPM enabled on the given PCI Express Link. See section 5.4.1.3 of PCI Express Base Specification for requirements on when and how to enable ASPM. Note: "L0s Entry Enabled" enables the Transmitter to enter L0s. If L0s is supported, the Receiver must be capable of entering L0s even when the Transmitter is disabled from entering L0s (00b or 10b). ASPM L1 must be enabled by software in the Upstream component on a Link prior to enabling ASPM L1 in the Downstream component on that Link. When disabling ASPM L1, software must disable ASPM L1 in the Downstream component on a Link prior to disabling ASPM L1 in the Upstream component on that Link. ASPM L1 must only be enabled on the Downstream component if both components on a Link support ASPM L1. For Multi-Function Devices (including ARI Devices), it is recommended that software program the same value for this field in all Functions. For non-ARI Multi-Function Devices, only capabilities enabled in all Functions are enabled for the component as a whole. For ARI Devices, ASPM Control is determined solely by the setting in Function0, regardless of Function 0's D-state. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Software must not enable L0s in either direction on a given Link unless components on both sides of the Link each support L0s; otherwise, the result is undefined.

PCIE_DSP_PF0_PCIE_CAP_SLOT_CAPABILITIES_REG

Address: Operational Base(0xFE000070) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	PCIE_CAP_PHY_SLOT_NUM Physical Slot Number. This field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to zero for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
18	RO	0x0	PCIE_CAP_NO_CMD_CPL_SUPPORT No Command Completed Support. When set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set if the hot-plug capable Port is able to accept writes to all fields of the Slot Control register without delay between successive writes. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
17	RO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK Electromechanical Interlock Present. When set, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
16:15	RO	0x0	PCIE_CAP_SLOT_POWER_LIMIT_SCALE Slot Power Limit Scale. Specifies the scale used for the Slot Power Limit Value (for more details, see Section 6.9 of PCI Express Base Specification). This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 00b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
14:7	RO	0x00	PCIE_CAP_SLOT_POWER_LIMIT_VALUE Slot Power Limit Value. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot (for more detais, see Section 6.9 of PCI Express Base Specification) or by other means to the adapter. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b (1.0x) and Slot Power Limit Value exceeds EFh, the alternative encodings defined in Values: are used. Value F3h to FFh are Reserved for Slot Power Limit values above 300 W. This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 0000 0000b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
6	RO	0x0	PCIE_CAP_HOT_PLUG_CAPABLE Hot-Plug Capable. When set, this bit indicates that this slot is capable of supporting hot-plug operations. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
5	RO	0x0	PCIE_CAP_HOT_PLUG_SURPRISE Hot-Plug Surprise. When set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
4	RO	0x0	PCIE_CAP_POWER_INDICATOR Power Indicator Present. When set, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
3	RO	0x0	PCIE_CAP_ATTENTION_INDICATOR Attention Indicator Present. When set, this bit indicates that an Attention Indicator is electrically controlled by the chassis. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
2	RO	0x0	PCIE_CAP_MRL_SENSOR MRL Sensor Present. When set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
1	RO	0x0	PCIE_CAP_POWER_CONTROLLER Power Controller Present. When set, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter (depending on form factor). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
0	RO	0x0	PCIE_CAP_ATTENTION_INDICATOR_BUTTON Attention Button Present. When set, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

PCIE_DSP_PF0_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS

Address: Operational Base(0xFE000070) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	RSVDP_25 Reserved for future use.
24	RW	0x0	PCIE_CAP_DLL_STATE_CHANGED Data Link Layer State Changed. This bit is set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active bit of the Link Status register to determine if the Link is active before initiating configuration cycles to the hot plugged device.
23	RO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_STATUS Electromechanical Interlock Status. If an Electromechanical Interlock is implemented, this bit indicates the status of the Electromechanical Interlock.

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Bit	Attr	Reset Value	Description
22	RO	0x1	PCIE_CAP_PRESENCE_DETECT_STATE Presence Detect State. This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. This bit must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), the controller hardwires this bit to 1b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
21	RO	0x0	PCIE_CAP_MRL_SENSOR_STATE MRL Sensor State. This bit reports the status of the MRL sensor if implemented. Encodings are define as above.
20	RW	0x0	PCIE_CAP_CMD_CPLD Command Completed. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. If Command Completed notification is not supported, the controller hardwires this bit to 0b.
19	RW	0x0	PCIE_CAP_PRESENCE_DETECTED_CHANGED Presence Detect Changed. This bit is set when the value reported in the Presence Detect State bit is changed.
18	RW	0x0	PCIE_CAP_MRL_SENSOR_CHANGED MRL Sensor Changed. If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.
17	RW	0x0	PCIE_CAP_POWER_FAULT_DETECTED Power Fault Detected. If a Power Controller that supports power fault detection is implemented, this bit issSet when the Power Controller detects a power fault at this slot. Note: Depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.

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Bit	Attr	Reset Value	Description
16	RW	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED Attention Button Pressed. If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.
15:14	RO	0x0	RSVDP_14 Reserved for future use.
13	RO	0x0	reserved
12	RW	0x0	PCIE_CAP_DLL_STATE_CHANGED_EN Data Link Layer State Changed Enable. If the Data Link Layer Link Active Reporting capability is 1b, this bit enables software notification when Data Link Layer Link Active bit is changed. If the Data Link Layer Link Active Reporting Capable bit is 0b, this bit is permitted to be read-only with a value of 0b.
11	WO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_CTRL Electromechanical Interlock Control. If an Electromechanical Interlock is implemented, a write of 1b to this bit causes the state of the interlock to toggle. A write of 0b to this bit has no effect. A read of this bit always returns a 0b.
10	RW	0x0	PCIE_CAP_POWER_CONTROLLER_CTRL Power Controller Control. If a Power Controller is implemented, this bit when written sets the power state of the slot per the defined encodings. Reads of this bit must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write, if required to, without waiting for the previous command to complete in which case the read value is undefined. Note: In some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. If the Power Controller Present bit in the Slot Capabilities register is clear, then writes to this bit have no effect and the read value of this bit is undefined.
9:8	RW	0x3	PCIE_CAP_POWER_INDICATOR_CTRL Power Indicator Control. If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Power Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b.

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Bit	Attr	Reset Value	Description
7:6	RW	0x3	PCIE_CAP_ATTENTION_INDICATOR_CTRL Attention Indicator Control. If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Attention Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b.
5	RW	0x0	PCIE_CAP_HOT_PLUG_INT_EN Hot-Plug Interrupt Enable. When set, this bit enables generation of an interrupt on enabled hot-plug events. If the Hot Plug Capable bit in the Slot Capabilities register is clear, this bit is permitted to be read-only with a value of 0b.
4	RW	0x0	PCIE_CAP_CMD_CPL_INT_EN Command Completed Interrupt Enable. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), when set, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, the controller hardwires this bit must to 0b. Write value is gated with PCIE_CAP_NO_CMD_CPL_SUPPORT field in SLOT_CAPABILITIES_REG. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: SLOT_CAPABILITIES_REG.PCIE_CAP_NO_CMD_CPL_SUPPORT ? RO : RW
3	RW	0x0	PCIE_CAP_PRESENCE_DETECT_CHANGE_EN Presence Detect Changed Enable. When set, this bit enables software notification on a presence detect changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Hot-Plug Capable bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b.
2	RW	0x0	PCIE_CAP_MRL_SENSOR_CHANGED_EN MRL Sensor Changed Enable. When set, this bit enables software notification on a MRL sensor changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the MRL Sensor Present bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b.
1	RW	0x0	PCIE_CAP_POWER_FAULT_DETECTED_EN Power Fault Detected Enable. When set, this bit enables software notification on a power fault event (for more details, see Section 6.7.3 of PCI Express Base Specification). If a Power Controller that supports power fault detection is not implemented, this bit is permitted to be read-only with a value of 0b.

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Bit	Attr	Reset Value	Description
0	RW	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED_EN Attention Button Pressed Enable. When set to 1b, this bit enables software notification on an attention button pressed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Attention Button Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b.

PCIE_DSP_PF0_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG

Address: Operational Base(0xFE000070) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	RSVDP_17 Reserved for future use.
16	RO	0x1	PCIE_CAP_CRS_SW_VISIBILITY CRS Software Visibility Capable. When set, this bit indicates that the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W (Sticky) else R (Sticky) Note: This register field is sticky.
15:5	RO	0x000	RSVDP_5 Reserved for future use.
4	RW	0x0	PCIE_CAP_CRS_SW_VISIBILITY_EN CRS Software Visibility Enable. When set, this bit enables the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). For Root Ports that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: ROOT_CONTROL_ROOT_CAPABILITIES_REG.PCIE_CAP_CRS_SW_VISIBILITY ? RW : RO
3	RW	0x0	PCIE_CAP_PME_INT_EN PME Interrupt Enable. When set, this bit enables PME interrupt generation upon receipt of a PME Message as reflected in the PME Status bit (for more details, see Table 7-29 of PCI Express Base Specification). A PME interrupt is also generated if the PME Status bit is set when this bit is changed from clear to set.
2	RW	0x0	PCIE_CAP_SYS_ERR_ON_FATAL_ERR_EN System Error on Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Fatal error (ERR_FATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.

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Bit	Attr	Reset Value	Description
1	RW	0x0	PCIE_CAP_SYS_ERR_ON_NON_FATAL_ERR_EN System Error on Non-Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Non-fatal error (ERR_NONFATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.
0	RW	0x0	PCIE_CAP_SYS_ERR_ON_CORR_ERR_EN System Error on Correctable Error Enable. If set, this bit indicates that a System Error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.

PCIE_DSP_PF0_PCIE_CAP_ROOT_STATUS_REG

Address: Operational Base(0xFE000070) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	RSVDP_18 Reserved for future use.
17	RO	0x0	PCIE_CAP_PME_PENDING PME Pending. This bit indicates that another PME is pending when the PME Status bit is s et. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the PME Requester ID field appropriately. The PME Pending bit is cleared by hardware if no more PMEs are pending.
16	RW	0x0	PCIE_CAP_PME_STATUS PME Status. This bit indicates that PME was asserted by the PME Requester indicated in the PME Requester ID field. Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1b.
15:0	RO	0x0000	PCIE_CAP_PME_REQ_ID PME Requester ID. This field indicates the PCI Requester ID of the last PME Requester. This field is only valid when the PME Status bit is set.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES2_REG

Address: Operational Base(0xFE000070) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	RSVDP_24 Reserved for future use.
23:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19:18	RO	0x3	PCIE_CAP_OBFF_SUPPORT OBFF Supported. This field indicates if OBFF is supported and, if so, what signaling mechanism is used. The value reported in this field must indicate support for WAKE# signaling only if: - for a Downstream Port, driving the WAKE# signal for OBFF is supported and the connector or component connected Downstream is known to receive that same WAKE# signal - for an Upstream Port, receiving the WAKE# signal for OBFF is supported and, if the component is on an add-in-card, that the component is connected to the WAKE# signal on theconnector. Root Ports, Switch Ports, and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this field. For Bridges and Ports that do not implement this capability, the controller hardwires this field to 00b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky.
17	RO	0x0	PCIE_CAP2_10_BIT_TAG_REQ_SUPPORT 10-Bit Tag Requester Supported. If this bit is set, the Function supports 10-Bit Tag Requester capability; otherwise, the Function does not. This bit must not be set if the 10-Bit Tag Completer Supported bit is clear. Note: 10-Bit Tag field generation must be enabled by the 10-Bit Tag Requester Enable bit in the Device Control 2 register of the Requester Function before 10-Bit Tags can be generated by the Requester. For more details, see section 2.2.6.2. of PCI Express Base Specification.
16	RO	0x0	PCIE_CAP2_10_BIT_TAG_COMP_SUPPORT 10-Bit Tag Completer Supported. If this bit is set, the Function supports 10-Bit Tag Completer capability; otherwise, the Function does not. For more details, see section 2.2.6.2. of PCI Express Base Specification.
15:14	RO	0x0	reserved
13	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_1 TPH Completer Supported Bit 1.
12	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_0 TPH Completer Supported Bit 0. Value of this bit along with TPH Completer Supported Bit 1 indicates Completer support for TPH or Extended TPH. Applicable only to Root Ports and Endpoints. For all other Functions, this field is Reserved. For more details, see section 6.17 of PCI Express Base Specification.

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Bit	Attr	Reset Value	Description
11	RO	0x1	PCIE_CAP_LTR_SUPP LTR Mechanism Supported. A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. Root Ports, Switches and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this bit. For Bridges and other Functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky.
10	RO	0x1	PCIE_CAP_NO_RO_EN_PR2PR_PAR No RO-enabled PR-PR Passing. If this bit is set, the routing element never carries out the passing permitted by Table 2-39 of PCI Express Base Specification entry A2b that is associated with the Relaxed Ordering Attribute field being Set. This bit applies only for Switches and RCs that support peer-to-peer traffic between Root Ports. This bit applies only to Posted Requests being forwarded through the Switch or RC and does not apply to traffic originating or terminating within the Switch or RC itself. All Ports on a Switch or RC must report the same value for this bit. For all other functions, this bit must be 0b.
9	RO	0x0	PCIE_CAP_128_CAS_CPL_SUPP 128-bit CAS Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. This bit must be set to 1b if the Function supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification.
8	RO	0x0	PCIE_CAP_64_ATOMIC_CPL_SUPP 64-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification.
7	RO	0x0	PCIE_CAP_32_ATOMIC_CPL_SUPP 32-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification.
6	RO	0x0	PCIE_CAP_ATOMIC_ROUTING_SUPP AtomicOp Routing Supported. Applicable only to Switch Upstream Ports, Switch Downstream Ports, and Root Ports; must be 0b for other Function types. This bit must be set to 1b if the Port supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification.

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Bit	Attr	Reset Value	Description
5	RO	0x0	PCIE_CAP_ARI_FORWARD_SUPPORT ARI Forwarding Supported. Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. For more details, see section 6.13 of PCI Express Base Specification.
4	RO	0x1	PCIE_CAP_CPL_TIMEOUT_DISABLE_SUPPORT Completion Timeout Disable Supported. A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports. For all other Functions this field is Reserved and the controller hardwires this bit to 0b.
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_RANGE Completion Timeout Ranges Supported. This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and must be hardwired to 0000b. Four time value ranges are defined: - Range A: 50 us to 10 ms - Range B: 10 ms to 250 ms - Range C: 250 ms to 4 s - Range D: 4 s to 64 s Bits are set according to the list below to show timeout value ranges supported. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG

Address: Operational Base(0xFE000070) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	PCIE_CAP_OBFF_EN OBFF Enable. This field enables the OBFF mechanism and selects the signaling method. For more details on these encodings, see section 6.19 of PCI Express Base Specification. This field is required for all Ports that support the OBFF Capability. For a Multi-Function Device associated with an Upstream Port of a Device that implements OBFF, the field in Function 0 is of type RW, and only Function 0 controls the Component's behavior. In all other Functions of that Device, this field is of type RsvdP. Ports that do not implement OBFF are permitted to hardwire this field to 00b Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_OBFF_SUPPORT) then R/W else R
12:11	RO	0x0	reserved
10	RW	0x0	PCIE_CAP_LTR_EN LTR Mechanism Enable. When set to 1b, this bit enables Upstream Ports to send LTR messages and Downstream Ports to process LTR Messages. For a Multi-Function Device associated with an Upstream Port of a device that implements LTR, the bit in Function 0 is RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is RsvdP. Functions that do not implement the LTR mechanism are permitted to hardwire this bit to 0b. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. The write value is gated with the PCIE_CAP_LTR_SUPP field of DEVICE_CAPABILITIES2_REG. Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_LTR_SUPP) then R/W else R
9:6	RO	0x0	reserved
5	RO	0x0	PCIE_CAP_ARI_FORWARD_SUPPORT_CS ARI Forwarding Enable. When set, the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. For more details, see Section 6.13 of PCI Express Base Specification. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

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Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_CPL_TIMEOUT_DISABLE Completion Timeout Disable. When set, this bit disables the Completion Timeout mechanism. This bit is required for all Functions that support the Completion Timeout Disable Capability. Functions that do not support this optional capability are permitted to hardwire this bit to 0b Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding Requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding Requests. If this is done, it is permitted to base the start time for each Request on either the time this bit was cleared or the time each Request was issued.
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_VALUE Completion Timeout Value. In device Functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and controller hardwires it to 0000b. A Function that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50 us to 50 ms. Functions that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Ranges Supported field. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms. Values available if Range A (50 us to 10 ms) programmability range is supported: Values available if Range B (10 ms to 250 ms) programmability range is supported: Values available if Range C (250 ms to 4 s) programmability range is supported: Values available if the Range D (4 s to 64 s) programmability range is supported: Software is permitted to change the value in this field at any time. For Requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding Requests, and is permitted to base the start time for each Request either on when this value was changed or on when each request was issued. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES2_REG

Address: Operational Base(0xFE000070) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RO	0x00	RSVDP_25 Reserved for future use.

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Bit	Attr	Reset Value	Description
24:23	RO	0x0	reserved
22:9	RO	0x0000	RSVDP_9 Reserved for future use.
8	RO	0x0	PCIE_CAP_CROSS_LINK_SUPPORT Crosslink Supported. When set to 1b, this bit indicates that the associated Port supports crosslinks (for more details, see section 4.2.6.3.1 of PCI Express Base Specification). When set to 0b on a Port that supports Link speeds of 8.0 GT/s or higher, this bit indicates that the associated Port does not support crosslinks. When set to 0b on a Port that only supports Link speeds of 2.5 GT/s or 5.0 GT/s, this bit provides no information regarding the Port's level of crosslink support. It is recommended that this bit be Set in any Port that supports crosslinks even though doing so is only required for Ports that also support operating at 8.0 GT/s or higher Link speeds. Note: Software should use this bit when referencing fields whose definition depends on whether or not the Port supports crosslinks (for more details, see section 7.7.3.4 of PCI Express Base Specification). Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions.
7:1	RO	0x07	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR Supported Link Speeds Vector. This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. For more details, see section 8.2.1 of PCI Express Base Specification. Bit definitions within this field are: - Bit 0 2.5 GT/s - Bit 1 5.0 GT/s - Bit 2 8.0 GT/s - Bit 3 16.0 GT/s - Bit 4 32.0 GT/s - Bits 6:5 RsvdP Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions. This field has a default of (PCIE_CAP_MAX_LINK_SPEED == 0101) ? 0011111: (PCIE_CAP_MAX_LINK_SPEED == 0100) ? 0001111 : (PCIE_CAP_MAX_LINK_SPEED == 0011) ? 0000111 : (PCIE_CAP_MAX_LINK_SPEED == 0010) ? 0000011 : 0000001 where PCIE_CAP_MAX_LINK_SPEED is a field in the LINK_CAPABILITIES_REG register.
0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG

Address: Operational Base(0xFE000070) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RO	0x0	RSVDP_26 Reserved for future use.
25:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	PCIE_CAP_LINK_EQ_REQ Link Equalization Request 8.0 GT/s. This bit is set by hardware to request the 8.0 GT/s Link equalization process to be performed on the Link. For more details, see sections 4.2.3 and 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
20	RO	0x0	PCIE_CAP_EQ_CPL_P3 EEqualization 8.0 GT/s Phase 3 Successful. When set to 1b, this bit indicates that Phase 3 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
19	RO	0x0	PCIE_CAP_EQ_CPL_P2 Equalization 8.0 GT/s Phase 2 Successful. When set to 1b, this bit indicates that Phase 2 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
18	RO	0x0	PCIE_CAP_EQ_CPL_P1 Equalization 8.0 GT/s Phase 1 Successful. When set to 1b, this bit indicates that Phase 1 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
17	RO	0x0	PCIE_CAP_EQ_CPL Equalization 8.0 GT/s Complete. When set to 1b, this bit indicates that the Transmitter Equalization procedure at the 8.0 GT/s data rate has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
16	RO	0x1	PCIE_CAP_CURR_DEEMPHASIS Current De-emphasis Level. When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For components that support speeds greater than 2.5 GT/s, Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions of the Port. In M-PCIe mode this register is always 0x0. In C-PCIe mode, its contents are derived by sampling the PIPE.
15:12	RW	0x0	PCIE_CAP_COMPLIANCE_PRESET Compliance Preset/De-emphasis. - For 8.0 GT/s and higher Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. The encodings are defined in section 4.2.3.2 of PCI Express Base Specification. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. - For 5.0 GT/s Data Rate: This field sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. - When the Link is operating at 2.5 GT/s, the setting of this field has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this field to 0000b. - For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. - This field is intended for debug and compliance testing purposes. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
11	RW	0x0	PCIE_CAP_COMPLIANCE_SOS Compliance SOS. When set to 1b, the LTSSM is required to send SKP Ordered Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
10	RW	0x0	PCIE_CAP_ENTER_MODIFIED_COMPLIANCE Enter Modified Compliance. When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
9:7	RW	0x0	PCIE_CAP_TX_MARGIN Transmit Margin, This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see Chapter 4 of PCI Express Base Specification for details of how the Transmitter voltage level is determined in various states). - 001b-111b: As defined in Section 8.3.4 not all encodings are required to be implemented. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 000b. This field is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: This register field is sticky.
6	RO	0x0	PCIE_CAP_SEL_DEEMPHASIS Selectable De-emphasis. When the Link is operating at 5.0 GT/s speed, this bit is used to control the transmit de-emphasis of the link in specific situations. For more details, see section 4.2.6 of PCI Express Base Specification. When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5	RW	0x0	PCIE_CAP_HW_AUTO_SPEED_DISABLE Hardware Autonomous Speed Disable. When set, this bit disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
4	RW	0x0	PCIE_CAP_ENTER_COMPLIANCE Enter Compliance. Software is permitted to force a Link to enter Compliance mode (at the speed indicated in the Target Link Speed field and the de-emphasis/preset level indicated by the Compliance Preset/De-emphasis field) by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x3	PCIE_CAP_TARGET_LINK_SPEED Target Link Speed. For Downstream Ports, this field sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the desired target Link speed. All encodings other than the defined encodings are reserved. If a value is written to this field that does not correspond to a supported speed (as indicated by the Supported Link Speeds Vector), the result is undefined. If either of the Enter Compliance or Enter Modified Compliance bits are implemented, then this field must also be implemented. The default value of this field is the highest Link speed supported by the component (as reported in the Max Link Speed field of the Link Capabilities register) unless the corresponding platform/form factor requires a different default value. For both Upstream and Downstream Ports, this field is used to set the target compliance mode speed when software is using the Enter Compliance bit to force a Link into compliance mode. For Upstream Ports, if the Enter Compliance bit is Clear, this field is permitted to have no effect. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0000b. In M-PCIe mode, the contents of this field are derived from other registers. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

7.4.3.5 PCIE_DSP_PF0_MSIX_CAP

7.4.3.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_MSIX_CAP_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x00000011	This Register holds MSI-X Capability ID, Next Capability pointer. It also controls the MSI-X behaviour.
PCIE_DSP_PF0_MSIX_CAP_MSIX_TABLE_OFFSET_REG	0x0004	W	0x00000000	This register provides Table BIR and MSI-x Table offset select.
PCIE_DSP_PF0_MSIX_CAP_MSIX_PBA_OFFSET_REG	0x0008	W	0x00000010	This register provides PBA Offset and PBA BIR value.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.5.2 Detail Registers Description

PCIE_DSP_PF0_MSIX_CAP_PCI_MSIX_CAP_ID_NEXT_CTRL_REG

Address: Operational Base(0xFE0000B0) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31	RW	0x0	PCI_MSIX_ENABLE MSI-X Enable. If Set and the MSI Enable bit in the MSI Message Control Register for MSI is Clear, the Function is permitted to use MSI-X to request service and is prohibited from using INTx interrupts (if implemented). System configuration software Sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a Function's service request. If Clear, the Function is prohibited from using MSI-X to request service.
30	RW	0x0	PCI_MSIX_FUNCTION_MASK Function Mask. If Set, all of the vectors associated with the Function are masked, regardless of their per-vector Mask bit values. If Clear, each vector's Mask bit determines whether the vector is masked or not. Setting or Clearing the MSI-X Function Mask bit has no effect on the value of the per-vector Mask bits. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
29:27	RO	0x0	RSVDP_27 Reserved for future use.
26:16	RO	0x000	PCI_MSIX_TABLE_SIZE MSI-X Table Size. System software reads this field to determine the MSI-X Table Size N, which is encoded as N-1. For example, a returned value of 000 0000 0011b indicates a table size of 4. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table Size" (PCI_MSIX_TABLE_SIZE field in SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_TABLE_SIZE field in the PF PCI_MSIX_CAP_ID_NEXT_CTRL_REG register. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
15:8	RO	0x00	PCI_MSIX_CAP_NEXT_OFFSET MSI-X Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RO	0x11	PCI_MSIX_CAP_ID MSI-X Capability ID. This field indicates the MSI-X Capability structure. This field must return a Capability ID of 11h indicating that this is an MSI-X Capability structure.

PCIE_DSP_PF0_MSIX_CAP_MSIX_TABLE_OFFSET_REG

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Address: Operational Base(0xFE0000B0) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	PCI_MSIX_TABLE_OFFSET MSI-X Table Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table Offset" (PCI_MSIX_TABLE_OFFSET field in SHADOW_MSIX_TABLE_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_TABLE_OFFSET field in the PF MSIX_TABLE_OFFSET_REG register. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
2:0	RO	0x0	PCI_MSIX_BIR MSI-X Table BAR Indicator Register Field. This field indicates which one of a Function's Base Address Registers, located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X Table into Memory Space. All encodings other than the defined encodings are reserved. For a 64-bit Base Address Register, the Table BIR indicates the lower DWORD. For Functions with Type 1 Configuration Space headers, BIR values 2 through 5 are also Reserved. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table BAR Indicator Register" (PCI_MSIX_BIR field in SHADOW_MSIX_TABLE_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_BIR field in the PF MSIX_TABLE_OFFSET_REG register. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_MSIX_CAP_MSIX_PBA_OFFSET_REG

Address: Operational Base(0xFE0000B0) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:3	RO	0x00000002	PCI_MSIX_PBA_OFFSET MSI-X PBA Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. SRIOV Note: All VFs in a single PF have the same value for "MSI-X PBA Offset" (PCI_MSIX_PBA_OFFSET field in SHADOW_MSIX_PBA_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_PBA_OFFSET field in the PF MSIX_PBA_OFFSET_REG register. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
2:0	RO	0x0	PCI_MSIX_PBA_BIR MSI-X PBA BIR. This field indicates which one of a Function's Base Address Registers, located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the Table BIR. SRIOV Note: All VFs in a single PF have the same value for "MSI-X PBA BIR" (PCI_MSIX_PBA_BIR field in SHADOW_MSIX_PBA_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_PBA_BIR field in the PF MSIX_PBA_OFFSET_REG register. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

7.4.3.6 PCIE_DSP_PF0_AER_CAP

7.4.3.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_AER_EXT_CAP_HDR_OFF	0x0000	W	0x14820001	Advanced Error Reporting Extended Capability Header provides information about Capability ID, Version, and next offset.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_STATUS_OFF	0x0004	W	0x00000000	The Uncorrectable Error Status Register (Offset 04h) indicates error detection status of individual errors on a PCI Express device Function.An individual error status bit that is Set indicates that a particular error was detected; software may clear an error status by writing a 1b to the respective bit.Register bits not implemented by the Function are hardwired to 0b.
PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_MASK_OFF	0x0008	W	0x00400000	The Uncorrectable Error Mask Register controls reporting of individual errors by the device Function to the PCI Express Root Complex through a PCI Express error Message.A masked error (respective bit Set in the mask register) is not recorded or reported in the Header Log, TLP Prefix Log, or First Error Pointer, and is not reported to the PCI Express Root Complex by this Function.There is a mask bit per error bit of the Uncorrectable Error Status register. Register fields for bits not implemented by the Function are hardwired to 0b.
PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_SEV_OFF	0x000C	W	0x00462030	The Uncorrectable Error Severity Register controls whether an individual error is reported as a Non-fatal or Fatal error.An error is reported as fatal when the corresponding error bit in the severity register is Set. If the bit is Clear, the corresponding error is considered non-fatal.
PCIE_DSP_PF0_AER_CAP_CORR_ERR_STATUS_OFF	0x0010	W	0x00000000	The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device Function.When an individual error status bit is Set, it indicates that a particular error occurred; software may clear an error status by writing a 1b to the respective bit.Register bits not implemented by the Function are hardwired to 0b by the controller.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_CORR_ERR_MASK_OFF	0x0014	W	0x0000E000	The Correctable Error Mask Register controls reporting of individual correctable errors by this Function to the PCI Express Root Complex through a PCI Express error Message.A masked error (respective bit Set in the mask register) is not reported to the PCI Express Root Complex by this Function.There is a mask bit per error bit in the Correctable Error Status register. Register fields for bits not implemented by the Function are hardwired to 0b by the controller.
PCIE_DSP_PF0_AER_CAP_ADV_ERR_CAP_CTRL_OFF	0x0018	W	0x000000A0	Advanced Error Capabilities and Control Register provides information whether the individual capability is supported or not. If the capability is supported then it is enabled or not.
PCIE_DSP_PF0_AER_CAP_HDR_LOG_0_OFF	0x001C	W	0x00000000	The Header Log Register 0 contains the header for the TLP corresponding to a detected error; The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in the specification. Therefore, byte 0 of the header is located in byte 3 of the Header Log Register 0, byte 1 of the header is in byte 2 of the Header Log Register 0, and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_HDR_LOG_1_OFF	0x0020	W	0x00000000	The Header Log Register 1 contains the header for the TLP corresponding to a detected error; The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in the specification. Therefore, byte 0 of the header is located in byte 3 of the Header Log Register 1, byte 1 of the header is in byte 2 of the Header Log Register 1 and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information.
PCIE_DSP_PF0_AER_CAP_HDR_LOG_2_OFF	0x0024	W	0x00000000	The Header Log Register 2 contains the header for the TLP corresponding to a detected error; The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in the specification. Therefore, byte 0 of the header is located in byte 3 of the Header Log Register 2, byte 1 of the header is in byte 2 of the Header Log Register 2 and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_HDR_LOG_3_OFF	0x0028	W	0x00000000	The Header Log Register 3 contains the header for the TLP corresponding to a detected error; The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in the specification. Therefore, byte 0 of the header is located in byte 3 of the Header Log Register 3, byte 1 of the header is in byte 2 of the Header Log Register 3 and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information.
PCIE_DSP_PF0_AER_CAP_ROOT_ERR_CMD_OFF	0x002C	W	0x00000000	The Root Error Command Register allows further control of Root Complex response to Correctable, Non-Fatal, and Fatal error Messages than the basic Root Complex capability to generatesystem errors in response to error Messages.
PCIE_DSP_PF0_AER_CAP_ROOT_ERR_STATUS_OFF	0x0030	W	0x48000000	The Root Error Status Register reports status of error Messages (ERR_COR, ERR_NONFATAL, and ERR_FATAL) received by the Root Port, and of errors detected by the Root Port itself(The Root Port had sent an error Message to itself).In order to update this register, error Messages received by the Root Port and/or internally generated error Messages must be enabled for i°transmissioni± by the primary interface of the Root Port.
PCIE_DSP_PF0_AER_CAP_ERR_SRC_ID_OFF	0x0034	W	0x00000000	The Error Source Identification Register identifies the source (Requester ID) of first correctable and uncorrectable (Non-fatal/Fatal) errors reported in the Root Error Status Register.This register is updated regardless of the settings of the Root Control register and the Root Error Command Register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_1_OFF	0x0038	W	0x00000000	The First TLP Prefix Log Register contains the first End-End TLP Prefix from the TLP corresponding to the detected error. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set.The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described. Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth. The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero by controller.If the End-End TLP Prefix Supported bit is Clear, the TLP Prefix Log Register is not required to be implemented.
PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_2_OFF	0x003C	W	0x00000000	The Second TLP Prefix Log Register contains the second End-End TLP Prefix from the TLP corresponding to the detected error. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set.The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described. Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth. The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero by controller.If the End-End TLP Prefix Supported bit is Clear, the TLP Prefix Log Register is not required to be implemented.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_3_OFF	0x0040	W	0x00000000	The Third TLP Prefix Log Register contains the third End-End TLP Prefix from the TLP corresponding to the detected error. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set.The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described. Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth. The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero by controller.If the End-End TLP Prefix Supported bit is Clear, the TLP Prefix Log Register is not required to be implemented.
PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_4_OFF	0x0044	W	0x00000000	The Fourth TLP Prefix Log Register contains the fourth End-End TLP Prefix from the TLP corresponding to the detected error. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set.The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described.Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth. The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero by controller.If the End-End TLP Prefix Supported bit is Clear, the TLP Prefix Log Register is not required to be implemented.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.6.2 Detail Registers Description

PCIE_DSP_PF0_AER_CAP_AER_EXT_CAP_HDR_OFF

Address: Operational Base(0xFE000100) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:20	RO	0x148	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
19:16	RO	0x2	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field must be 2h if the End-End TLP Prefix Supported bit is set and must be 1h or 2h otherwise. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RO	0x0001	CAP_ID AER Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Advanced Error Reporting Capability is 0001h. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_STATUS_OFF

Address: Operational Base(0xFE000100) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.
26:24	RO	0x0	reserved
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RW	0x0	INTERNAL_ERR_STATUS Uncorrectable Internal Error Status. This field gives status of the Uncorrectable Internal Error. The controller sets this bit when your application asserts app_err_bus[9]. It does not set this bit when it detects internal uncorrectable internal errors such as parity and ECC failures. You should use the outputs from these errors to drive the app_err_bus[9] input. For more details, see the "Data Integrity (Wire, Datapath, and RAM Protection)" section in the Databook. Note: This register field is sticky.
21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20	RW	0x0	UNSUPPORTED_REQ_ERR_STATUS Unsupported Request Error Status. This field represents status of Unsupported Request Error. Note: This register field is sticky.
19	RW	0x0	ECRC_ERR_STATUS ECRC Error Status. This field represents status of ECRC Error. Note: If CX_ECRC_ENABLE=0 the register field always reads 0. Note: This register field is sticky.
18	RW	0x0	MALF_TLP_ERR_STATUS Malformed TLP Status. This field represents status of Malformed TLP. Note: This register field is sticky.
17	RW	0x0	REC_OVERFLOW_ERR_STATUS Receiver Overflow Status. Status bit for Receiver Overflow. Note: This register field is sticky.
16	RW	0x0	UNEXP_CMPLT_ERR_STATUS Unexpected Completion Status. Status bit for Unexpected Completion. Note: This register field is sticky.
15	RW	0x0	CMPLT_ABORT_ERR_STATUS Completer Abort Status. Status bit for Completer Abort. Note: This register field is sticky.
14	RW	0x0	CMPLT_TIMEOUT_ERR_STATUS Completion Timeout Status. Status for Completion Timeout. Note: This register field is sticky.
13	RW	0x0	FC_PROTOCOL_ERR_STATUS Flow Control Protocol Error Status. Status bit for Flow Control Protocol Error. Note: This register field is sticky.
12	RW	0x0	POIS_TLP_ERR_STATUS Poisoned TLP Status. Status bit for Poisoned TLP. Note: This register field is sticky.
11:6	RO	0x00	RSVDP_6 Reserved for future use.
5	RW	0x0	SURPRISE_DOWN_ERR_STATUS Surprise Down Error Status (Optional). Status bit for Surprise Down Error. Note: This register field is sticky.
4	RW	0x0	DL_PROTOCOL_ERR_STATUS Data Link Protocol Error Status. Status bit for Data Link Protocol Error. Note: This register field is sticky.
3:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_MASK_OFF

Address: Operational Base(0xFE000100) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.

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Bit	Attr	Reset Value	Description
26:24	RO	0x0	reserved
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RW	0x1	INTERNAL_ERR_MASK Uncorrectable Internal Error Mask (Optional). Mask bit for Uncorrectable Internal Error. Note: This register field is sticky.
21	RO	0x0	reserved
20	RW	0x0	UNSUPPORTED_REQ_ERR_MASK Unsupported Request Error Mask. Mask bit for Unsupported Request Error. Note: This register field is sticky.
19	RW	0x0	ECRC_ERR_MASK ECRC Error Mask (Optional). Mask bit for ECRC Error. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
18	RW	0x0	MALF_TLP_ERR_MASK Malformed TLP Mask. Mask bit for Malformed TLP. Note: This register field is sticky.
17	RW	0x0	REC_OVERFLOW_ERR_MASK Receiver Overflow Mask (Optional). This field represents Receiver Overflow Mask. Note: This register field is sticky.
16	RW	0x0	UNEXP_CMPLT_ERR_MASK Unexpected Completion Mask. Mask bit for Unexpected Completion Error. Note: This register field is sticky.
15	RW	0x0	CMPLT_ABORT_ERR_MASK Completer Abort Error Mask (Optional). Mask bit for Completer Abort Error. Note: This register field is sticky.
14	RW	0x0	CMPLT_TIMEOUT_ERR_MASK Completion Timeout Error Mask. Mask bit for Completion Timeout Error. Note: This register field is sticky.
13	RW	0x0	FC_PROTOCOL_ERR_MASK Flow Control Protocol Error Mask. Mask bit for Flow Control Protocol Error. Note: This register field is sticky.
12	RW	0x0	POIS_TLP_ERR_MASK Poisoned TLP Error Mask. Mask bit for Poisoned TLP Error. Note: This register field is sticky.
11:6	RO	0x00	RSVDP_6 Reserved for future use.

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Bit	Attr	Reset Value	Description
5	RO	0x0	SURPRISE_DOWN_ERR_MASK Surprise Down Error Mask. Mask bit for Surprise Down Error. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP ? RW : RO Note: This register field is sticky.
4	RW	0x0	DL_PROTOCOL_ERR_MASK Data Link Protocol Error Mask. This field informs whether Data Link Protocol Error is masked or not. Note: This register field is sticky.
3:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_SEV_OFF

Address: Operational Base(0xFE000100) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.
26:24	RO	0x0	reserved
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RW	0x1	INTERNAL_ERR_SEVERITY Uncorrectable Internal Error Severity (Optional). Severity bit for Uncorrectable Internal Error. Note: This register field is sticky.
21	RO	0x0	reserved
20	RW	0x0	UNSUPPORTED_REQ_ERR_SEVERITY Unsupported Request Error Severity. Severity bit for Unsupported Request Error. Note: This register field is sticky.
19	RW	0x0	ECRC_ERR_SEVERITY ECRC Error Severity (Optional). Severity bit for ECRC Error. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
18	RW	0x1	MALF_TLP_ERR_SEVERITY Malformed TLP Severity. Severity bit for Malformed TLP. Note: This register field is sticky.
17	RW	0x1	REC_OVERFLOW_ERR_SEVERITY Receiver Overflow Error Severity (Optional). Severity bit for Receiver Overflow Error. Note: This register field is sticky.
16	RW	0x0	UNEXP_CMPLT_ERR_SEVERITY Unexpected Completion Error Severity. Severity bit for Unexpected Completion Error. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15	RW	0x0	CMPLT_ABORT_ERR_SEVERITY Completer Abort Error Severity (Optional). Severity bit for Completer Abort Error. Note: This register field is sticky.
14	RW	0x0	CMPLT_TIMEOUT_ERR_SEVERITY Completion Timeout Error Severity. Severity bit for Completion Timeout Error. Note: This register field is sticky.
13	RW	0x1	FC_PROTOCOL_ERR_SEVERITY Flow Control Protocol Error Severity (Optional). Severity bit for Flow Control Protocol Error. Note: This register field is sticky.
12	RW	0x0	POIS_TLP_ERR_SEVERITY Poisoned TLP Severity. Severity bit for Poisoned TLP. Note: This register field is sticky.
11:6	RO	0x00	RSVDP_6 Reserved for future use.
5	RO	0x1	SURPRISE_DOWN_ERR_SVRITY Surprise Down Error Severity (Optional). Severity bit for Surprise Down Error. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP ? RW : RO Note: This register field is sticky.
4	RW	0x1	DL_PROTOCOL_ERR_SEVERITY Data Link Protocol Error Severity. Severity bit for Data Link Protocol Error. Note: This register field is sticky.
3:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_AER_CAP_CORR_ERR_STATUS_OFF

Address: Operational Base(0xFE000100) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15	RW	0x0	HEADER_LOG_OVERFLOW_STATUS Header Log Overflow Error Status (Optional). This field provides status of Header Log Overflow Error. Note: This register field is sticky.
14	RW	0x0	CORRECTED_INT_ERR_STATUS Corrected Internal Error Status (Optional). This field provides status of Corrected Internal Error. Note: This register field is sticky.
13	RW	0x0	ADVISORY_NON_FATAL_ERR_STATUS Advisory Non-Fatal Error Status. Status bit for Advisory Non-Fatal Error. Note: This register field is sticky.
12	RW	0x0	RPL_TIMER_TIMEOUT_STATUS Replay Timer Timeout Status. Status bit for Replay Timer Timeout. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
11:9	RO	0x0	RSVDP_9 Reserved for future use.
8	RW	0x0	REPLAY_NO_ROLEOVER_STATUS REPLAY_NUM Rollover Status. Status bit for REPLAY_NUM Rollover. Note: This register field is sticky.
7	RW	0x0	BAD_DLLP_STATUS Bad DLLP Status. Status bit for Bad DLLP. Note: This register field is sticky.
6	RW	0x0	BAD_TLP_STATUS Bad TLP Status. Status bit for Bad TLP. Note: This register field is sticky.
5:1	RO	0x00	RSVDP_1 Reserved for future use.
0	RW	0x0	RX_ERR_STATUS Receiver Error Status (Optional). This field provides status of Receiver Error. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_CORR_ERR_MASK_OFF

Address: Operational Base(0xFE000100) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15	RW	0x1	HEADER_LOG_OVERFLOW_MASK Header Log Overflow Error Mask (Optional). Masking bit for Header Log Overflow Error. Note: This register field is sticky.
14	RW	0x1	CORRECTED_INT_ERR_MASK Corrected Internal Error Mask (Optional). Masking bit for Corrected Internal Error Mask. Note: This register field is sticky.
13	RW	0x1	ADVISORY_NON_FATAL_ERR_MASK Advisory Non-Fatal Error Mask. Masking bit for Advisory Non-Fatal Error. Note: This register field is sticky.
12	RW	0x0	RPL_TIMER_TIMEOUT_MASK Replay Timer Timeout Mask. Masking bit for Replay Timer Timeout. Note: This register field is sticky.
11:9	RO	0x0	RSVDP_9 Reserved for future use.
8	RW	0x0	REPLAY_NO_ROLEOVER_MASK REPLAY_NUM Rollover Mask. Masking bit for REPLAY_NUM Rollover. Note: This register field is sticky.
7	RW	0x0	BAD_DLLP_MASK Bad DLLP Mask. Masking bit for Bad DLLP. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
6	RW	0x0	BAD_TLP_MASK Bad TLP Mask. Masking bit for Bad TLP. Note: This register field is sticky.
5:1	RO	0x00	RSVDP_1 Reserved for future use.
0	RW	0x0	RX_ERR_MASK Receiver Error Mask (Optional). Masking bit for Receiver Error. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_ADV_ERR_CAP_CTRL_OFF

Address: Operational Base(0xFE000100) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	RSVDP_13 Reserved for future use.
12	RO	0x0	CTO_PRFX_HDR_LOG_CAP TLP Prefix Log Present. If Set, this bit indicates that the Function records the prefix/header of Request TLPs that experience a Completion Timeout error.
11	RO	0x0	reserved
10	RO	0x0	MULTIPLE_HEADER_EN Multiple Header Recording Enable. When Set, this bit enables the Function to record more than one error header. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.
9	RO	0x0	MULTIPLE_HEADER_CAP Multiple Header Recording Capable. If Set, this bit indicates that the Function is capable of recording more than one error header. Note: This register field is sticky.
8	RW	0x0	ECRC_CHECK_EN ECRC Check Enable. When Set, ECRC checking is enabled. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: This register field is sticky.
7	RO	0x1	ECRC_CHECK_CAP ECRC Check Capable. If Set, this bit indicates that the Function is capable of checking ECRC. Note: This register field is sticky.
6	RW	0x0	ECRC_GEN_EN ECRC Generation Enable. When Set, ECRC generation is enabled. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5	RO	0x1	ECRC_GEN_CAP ECRC Generation Capable. If Set, this bit indicates that the Function is capable of generating ECRC. Note: This register field is sticky.
4:0	RO	0x00	FIRST_ERR_POINTER First Error Pointer. The First Error Pointer is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_HDR_LOG_0_OFF

Address: Operational Base(0xFE000100) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	FIRST_DWORD_FOURTH_BYTE Byte 3 of Header log register of First 32-bit Data Word. This field represents fourth byte of First DW of Header. Note: This register field is sticky.
23:16	RO	0x00	FIRST_DWORD_THIRD_BYTE Byte 2 of Header log register of First 32-bit Data Word. This field represents third byte of First DW of Header. Note: This register field is sticky.
15:8	RO	0x00	FIRST_DWORD_SECOND_BYTE Byte 1 of Header log register of First 32-bit Data Word. This field represents second byte of First DW of Header. Note: This register field is sticky.
7:0	RO	0x00	FIRST_DWORD_FIRST_BYTE Byte 0 of Header log register of First 32-bit Data Word. This field represents first byte of First DW of Header. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_HDR_LOG_1_OFF

Address: Operational Base(0xFE000100) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	SECOND_DWORD_FOURTH_BYTE Byte 3 of Header log register of Second 32-bit Data Word. This field represents fourth byte of Second DW of Header. Note: This register field is sticky.
23:16	RO	0x00	SECOND_DWORD_THIRD_BYTE Byte 2 of Header log register of Second 32-bit Data Word. This field represents third byte of Second DW of Header. Note: This register field is sticky.
15:8	RO	0x00	SECOND_DWORD_SECOND_BYTE Byte 1 of Header log register of Second 32-bit Data Word. This field represents second byte of Second DW of Header. Note: This register field is sticky.
7:0	RO	0x00	SECOND_DWORD_FIRST_BYTE Byte 0 of Header log register of Second 32-bit Data Word. This field represents first byte of Second DW of Header. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_HDR_LOG_2_OFF

Address: Operational Base(0xFE000100) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	THIRD_DWORD_FOURTH_BYTE Byte 3 of Header log register of Third 32-bit Data Word. This field represents fourth byte of Third DW of Header. Note: This register field is sticky.
23:16	RO	0x00	THIRD_DWORD_THIRD_BYTE Byte 2 of Header log register of Third 32-bit Data Word. This field represents third byte of Third DW of Header. Note: This register field is sticky.
15:8	RO	0x00	THIRD_DWORD_SECOND_BYTE Byte 1 of Header log register of Third 32-bit Data Word. This field represents second byte of Third DW of Header. Note: This register field is sticky.
7:0	RO	0x00	THIRD_DWORD_FIRST_BYTE Byte 0 of Header log register of Third 32-bit Data Word. This field represents first byte of Third DW of Header. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_HDR_LOG_3_OFF

Address: Operational Base(0xFE000100) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	FOURTH_DWORD_FOURTH_BYTE Byte 3 of Header log register of Fourth 32-bit Data Word. This field represents fourth byte of Fourth DW of Header. Note: This register field is sticky.
23:16	RO	0x00	FOURTH_DWORD_THIRD_BYTE Byte 2 of Header log register of Fourth 32-bit Data Word. This field represents third byte of Fourth DW of Header. Note: This register field is sticky.
15:8	RO	0x00	FOURTH_DWORD_SECOND_BYTE Byte 1 of Header log register of Fourth 32-bit Data Word. This field represents second byte of Fourth DW of Header. Note: This register field is sticky.
7:0	RO	0x00	FOURTH_DWORD_FIRST_BYTE Byte 0 of Header log register of Fourth 32-bit Data Word. This field represents first byte of Fourth DW of Header. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_ROOT_ERR_CMD_OFF

Address: Operational Base(0xFE000100) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	RSVDP_3 Reserved for future use.
2	RW	0x0	FATAL_ERR_REPORTING_EN Fatal Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a Fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs.

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Bit	Attr	Reset Value	Description
1	RW	0x0	NON_FATAL_ERR_REPORTING_EN Non-Fatal Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a Non-fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs.
0	RW	0x0	CORR_ERR_REPORTING_EN Correctable Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a correctable error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs (Root Complex integrated Endpoint).

PCIE_DSP_PF0_AER_CAP_ROOT_ERR_STATUS_OFF

Address: Operational Base(0xFE000100) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x09	ADV_ERR_INT_MSG_NUM Advanced Error Interrupt Message Number. This register indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability. For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. For MSI-X, the value in this register indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If MSI-X is enabled, the value in this register must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this register must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this register is undefined. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
26:7	RO	0x00000	RSVDP_7 Reserved for future use.
6	RW	0x0	FATAL_ERR_MSG_RX One or more Fatal Error Messages Received. Set when one or more Fatal Uncorrectable error Messages have been received. Note: This register field is sticky.
5	RW	0x0	NON_FATAL_ERR_MSG_RX One or more Non-Fatal Error Messages Received. Set when one or more Non-Fatal Uncorrectable error Messages have been received. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
4	RW	0x0	FIRST_UNCORR_FATAL First Uncorrectable Error is Fatal. Set when the first Uncorrectable error Message received is for a Fatal error. Note: This register field is sticky.
3	RW	0x0	MUL_ERR_FATAL_NON_FATAL_RX Multiple Fatal or Non-Fatal Errors Received. Set when either a Fatal or a Non-fatal error is received and ERR_FATAL_NON_FATAL_RX is already Set. Note: This register field is sticky.
2	RW	0x0	ERR_FATAL_NON_FATAL_RX Fatal or Non-Fatal Error Received. Set when either a Fatal or a Non-fatal error Message is received and this bit is not already Set. Note: This register field is sticky.
1	RW	0x0	MUL_ERR_COR_RX Multiple Correctable Errors Received. Set when a Correctable error Message is received and ERR_COR_RX is already Set. Note: This register field is sticky.
0	RW	0x0	ERR_COR_RX Correctable Error Received. Set when a Correctable error Message is received and this bit is not already Set. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_ERR_SRC_ID_OFF

Address: Operational Base(0xFE000100) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ERR_FATAL_NON_FATAL_SOURCE_ID Source of Fatal/Non-Fatal Error. Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received bit is not already set. Note: This register field is sticky.
15:0	RO	0x0000	ERR_COR_SOURCE_ID Source of Correctable Error. Loaded with the Requester ID indicated in the received ERR_COR Message when the ERR_COR Received bit is not already set. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_1_OFF

Address: Operational Base(0xFE000100) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_1_FOURTH_BYTE Byte 3 of Error TLP Prefix Log 1. This field contains fourth byte of First DW of TLP Prefix. Note: This register field is sticky.
23:16	RO	0x00	CFG_TLP_PFX_LOG_1_THIRD_BYTE Byte 2 of Error TLP Prefix Log 1. This field contains third byte of First DW of TLP Prefix. Note: This register field is sticky.
15:8	RO	0x00	CFG_TLP_PFX_LOG_1_SECOND_BYTE Byte 1 of Error TLP Prefix Log 1. This field contains second byte of First DW of TLP Prefix. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	CFG_TLP_PFX_LOG_1_FIRST_BYTE Byte 0 of Error TLP Prefix Log 1. This field contains first byte of First DW of TLP Prefix. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_2_OFF

Address: Operational Base(0xFE000100) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_2_FOURTH_BYTE Byte 3 Error TLP Prefix Log 2. This field contains fourth byte of Second DW of TLP Prefix. Note: This register field is sticky.
23:16	RO	0x00	CFG_TLP_PFX_LOG_2_THIRD_BYTE Byte 2 Error TLP Prefix Log 2. This field contains third byte of Second DW of TLP Prefix. Note: This register field is sticky.
15:8	RO	0x00	CFG_TLP_PFX_LOG_2_SECOND_BYTE Byte 1 Error TLP Prefix Log 2. This field contains second byte of Second DW of TLP Prefix. Note: This register field is sticky.
7:0	RO	0x00	CFG_TLP_PFX_LOG_2_FIRST_BYTE Byte 0 Error TLP Prefix Log 2. This field contains first byte of Second DW of TLP Prefix. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_3_OFF

Address: Operational Base(0xFE000100) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_3_FOURTH_BYTE Byte 3 Error TLP Prefix Log 3. This field contains fourth byte of Third DW of TLP Prefix. Note: This register field is sticky.
23:16	RO	0x00	CFG_TLP_PFX_LOG_3_THIRD_BYTE Byte 2 Error TLP Prefix Log 3. This field contains third byte of Third DW of TLP Prefix. Note: This register field is sticky.
15:8	RO	0x00	CFG_TLP_PFX_LOG_3_SECOND_BYTE Byte 1 Error TLP Prefix Log 3. This field contains second byte of Third DW of TLP Prefix. Note: This register field is sticky.
7:0	RO	0x00	CFG_TLP_PFX_LOG_3_FIRST_BYTE Byte 0 Error TLP Prefix Log 3. This field contains first byte of Third DW of TLP Prefix. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_4_OFF

Address: Operational Base(0xFE000100) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_4_FOURTH_BYTE Byte 3 Error TLP Prefix Log 4. This field contains fourth byte of Fourth DW of TLP Prefix. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
23:16	RO	0x00	CFG_TLP_PFX_LOG_4_THIRD_BYTE Byte 2 Error TLP Prefix Log 4. This field contains third byte of Fourth DW of TLP Prefix. Note: This register field is sticky.
15:8	RO	0x00	CFG_TLP_PFX_LOG_4_SECOND_BYTE Byte 1 Error TLP Prefix Log 4. This field contains second byte of Fourth DW of TLP Prefix. Note: This register field is sticky.
7:0	RO	0x00	CFG_TLP_PFX_LOG_4_FIRST_BYTE Byte 0 Error TLP Prefix Log 4. This field contains first byte of Fourth DW of TLP Prefix. Note: This register field is sticky.

7.4.3.7 PCIE_DSP_PF0_SPCIE_CAP

7.4.3.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_SPCIE_CAP_SPCIE_CAP_HEADER_REG	0x0000	W	0x16010019	This Register provides Capability Id, Capability Version, and next Offset of SPCIE Structure.
PCIE_DSP_PF0_SPCIE_CAP_LINK_CONTROL3_REG	0x0004	W	0x00000000	This Register controls equilization and equilization interrupt.
PCIE_DSP_PF0_SPCIE_CAP_LANE_ERR_STATUS_REG	0x0008	W	0x00000000	This Register contains Lane Error Status Bits per Lane.
PCIE_DSP_PF0_SPCIE_CAP_SPCIE_CAP_OFF_0CH_REG	0x000C	W	0x00007F7F	This register provides Transmitter Preset and Receiver Preset Hint for Downstream Port and Upstream Port.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.7.2 Detail Registers Description

PCIE_DSP_PF0_SPCIE_CAP_SPCIE_CAP_HEADER_REG

Address: Operational Base(0xFE000148) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x160	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
19:16	RO	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0019	EXTENDED_CAP_ID Secondary PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_SPCIE_CAP_LINK_CONTROL3_REG

Address: Operational Base(0xFE000148) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	RSVDP_2 Reserved for future use.
1	RW	0x0	EQ_REQ_INT_EN Link Equalization Request Interrupt Enable. This bit is RW for Downstream Ports and for Upstream Ports when Crosslink Supported is 1b. This bit is not applicable and is RsvdP for Upstream Ports when the Crosslink Supported bit is 0b. If the Port does not support 8.0 GT/s, this bit is permitted to be hardwired to 0b by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
0	RW	0x0	PERFORM_EQ Perform Equalization. This bit is RW for Downstream Ports and for Upstream Ports when Crosslink Supported is 1b. This bit is not applicable and is RsvdP for Upstream Ports when the Crosslink Supported bit is 0b. If the Port does not support 8.0 GT/s, this bit is permitted to be hardwired to 0b by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_SPCIE_CAP_LANE_ERR_STATUS_REG

Address: Operational Base(0xFE000148) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	RSVDP_LANE_ERR_STATUS Reserved for future use.
0	RW	0x0	LANE_ERR_STATUS Lane Error Status Bits per Lane. Each bit indicates if the corresponding Lane detected a Lane-based error. A value of 1b indicates that a Lane based-error was detected on the corresponding Lane Number. For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ. For Ports that do not support 8.0 GT/s and do not set these bits based on 8b/10b errors , this field is permitted to be hardwired to 0 by the controller. Note: This register field is sticky.

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PCIE_DSP_PF0_SPCIE_CAP_SPCIE_CAP_OFF_0CH_REG

Address: Operational Base(0xFE000148) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30:24	RO	0x00	reserved
23	RO	0x0	RSVDP_23 Reserved for future use.
22:16	RO	0x00	reserved
15	RO	0x0	RSVDP_15 Reserved for future use.
14:12	RO	0x7	USP_RX_PRESET_HINT0 Upstream Port 8.0 GT/s Receiver Preset Hint 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 0 value sent or received during 8.0 GT/s Link Equalization. - Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field represents the value sent on Lane 0 during 8.0 GT/s equalization. - Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. - Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky)

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Bit	Attr	Reset Value	Description
11:8	RO	0xf	USP_TX_PRESET0 Upstream Port 8.0 GT/s Transmitter Preset 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 0 value sent or received during 8.0 GT/s Link Equalization. - Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. - Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. - Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky)
7	RO	0x0	RSVDP_7 Reserved for future use.
6:4	RO	0x7	DSP_RX_PRESET_HINT0 Downstream Port 8.0 GT/s Receiver Preset Hint 0. Receiver preset hint 0 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky)
3:0	RO	0xf	DSP_TX_PRESET0 Downstream Port 8.0 GT/s Transmitter Preset 0. Transmitter preset 0 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky)

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7.4.3.8 PCIE_DSP_PF0_L1SUB_CAP

7.4.3.8.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CAP_HEADER_REG	0x0000	W	0x1701001E	L1 Substates Extended Capability Header provides capability ID, capability version and next offset value for L1 Substates.
PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CAPABILITY_REG	0x0004	W	0x00280A1F	This register provides extended capability of L1 Substates.
PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CONTROL1_REG	0x0008	W	0x00000A00	This register Controls that the individual extended capability is enabled or not.
PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CONTROL2_REG	0x000C	W	0x00000028	This register Controls that the individual extended capability is enabled or not.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.8.2 Detail Registers Description

PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CAP_HEADER_REG

Address: Operational Base(0xFE000160) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x170	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h, if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
19:16	RO	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is depends on version of the specification. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RO	0x001e	EXTENDED_CAP_ID L1SUB Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 PM Substates is 001Eh. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

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PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CAPABILITY_REG

Address: Operational Base(0xFE000160) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	RSVDP_24 Reserved for future use.
23:19	RW	0x05	PWR_ON_VALUE_SUPPORT Port T Power On Value. Along with the Port T_POWER_ON_SCALE field in the L1 PM Substates Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON_SCALE field in the L1 PM Substates Capabilities register. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP
18	RO	0x0	RSVDP_18 Reserved for future use.
17:16	RW	0x0	PWR_ON_SCALE_SUPPORT Port T Power On Scale. Specifies the scale used for the Port T_POWER_ON_VALUE field in the L1 PM Substates Capabilities register. Range of values are given below. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP
15:8	RW	0x0a	COMM_MODE_SUPPORT Port Common Mode Restore Time. Time (in us) required for this Port to re-establish common mode. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP
7:5	RO	0x0	RSVDP_5 Reserved for future use.

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Bit	Attr	Reset Value	Description
4	RW	0x1	L1_PMSUB_SUPPORT L1 PM Substates ECN Supported. When Set this field indicates that this Port supports L1 PM Substates. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)
3	RW	0x1	L1_1_ASPM_SUPPORT ASPM L11 Supported. When Set this field indicates that ASPM L1.1 is supported. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)
2	RW	0x1	L1_2_ASPM_SUPPORT ASPM L12 Supported. When Set this field indicates that ASPM L1.2 is supported. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)
1	RW	0x1	L1_1_PCIPM_SUPPORT PCI-PM L11 Supported. When Set this field indicates that PCI-PM L1.1 is supported, and must be Set by all Ports implementing L1 PM Substates. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)
0	RW	0x1	L1_2_PCIPM_SUPPORT PCI-PM L12 Supported. When Set this field indicates that PCI-PM L1.2 is supported. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)

PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CONTROL1_REG

Address: Operational Base(0xFE000160) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	L1_2_TH_SCA LTR L12 Threshold Scale. This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. Hardware operation is undefined if software writes a Not-Permitted value to this field. Required for all Ports Ports for which the ASPM L12 Supported bit is Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP
28:26	RO	0x0	RSVDP_26 Reserved for future use.

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	L1_2_TH_VAL LTR L12 Threshold Value. Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled). Required for all Ports for which the ASPM L12 Supported bit is Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP
15:8	RW	0x0a	T_COMMON_MODE Common Mode Restore Time. Sets value of TCOMMONMODE (in us), which must be used by the Downstream Ports for timing the re-establishment of common mode. This field is of type RsvdP for Upstream Ports. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RW : RSVDP
7:4	RO	0x0	RSVDP_4 Reserved for future use.
3	RW	0x0	L1_1_ASPM_EN ASPM L11 Enable. When Set this field, enables ASPM L1.1. For Ports for which the ASPM L1.1 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set.
2	RW	0x0	L1_2_ASPM_EN ASPM L12 Enable. When Set this field, enables ASPM L1.2. For Ports for which the ASPM L1.2 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set.
1	RW	0x0	L1_1_PCIPM_EN PCI-PM L11 Enable. When Set this field, enables PCI-PM L1.1. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set.

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Bit	Attr	Reset Value	Description
0	RW	0x0	L1_2_PCIPM_EN PCI-PM L12 Enable. When Set this field, enables PCI-PM L1.2. For Ports for which the PCI-PM L1.2 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set.

PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CONTROL2_REG

Address: Operational Base(0xFE000160) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7:3	RW	0x05	T_POWER_ON_VALUE T Power On Value. Along with the T_POWER_ON_SCALE sets the minimum amount of time (in us) that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON_SCALE field. Required for all Ports that support L1.2, otherwise this field is of type RsvdP.This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are set. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP
2	RO	0x0	RSVDP_2 Reserved for future use.
1:0	RW	0x0	T_POWER_ON_SCALE T Power On Scale. Specifies the scale used for T_POWER_ON_VALUE. Range of values are given below. Required for all Ports that support L1.2, otherwise this field is of type RsvdP. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are set.Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP

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7.4.3.9 PCIE_DSP_PF0_RAS_DES_CAP

7.4.3.9.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_RAS_DES_CAP_HEADER_REG	0x0000	W	0x0001000B	The Vendor-Specific Extended Capability (VSEC Capability) is an optional Extended Capability that is permitted to be implemented by any PCI Express Function or RCRB. This Register contains Capability Id, Capability Version and Next Offset value for Vendor-Specific Extended Capability.
PCIE_DSP_PF0_RAS_DES_CAP_VENDOR_SPECIFIC_HEADER_REG	0x0004	W	0x10040002	This Register field provides VSEC Length, VSEC ID and VSEC Rev(Version Number).Vendor-specific software must qualify the associated Vendor ID of the PCI Express Function or RCRB before attempting to interpret the values in the VSEC ID or VSEC Rev fields.
PCIE_DSP_PF0_RAS_DES_CAP_EVENT_COUNTER_CONTROL_REG	0x0008	W	0x00000000	This is a viewport control register. - Setting the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register determine the Event Counter data returned by the EVENT_COUNTER_DATA_REG viewport register. - Setting the EVENT_COUNTER_ENABLE field in this register enables the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. - Setting the EVENT_COUNTER_CLEAR field in this register clears the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. - Reading the EVENT_COUNTER_STATUS field in this register returns the Enable status of the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EVENT_COUNTER_DATA_REG	0x000C	W	0x00000000	This viewport register returns the data selected by the following fields: - EVENT_COUNTER_EVENT_SELECT in EVENT_COUNTER_CONTROL_REG - EVENT_COUNTER_LANE_SELECT in EVENT_COUNTER_CONTROL_REG For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_CONTROL_REG	0x0010	W	0x00000100	Used for controlling the measurement of RX/TX data throughput and time spent in each low-power LTSSM state. For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_DATA_REG	0x0014	W	0x00000000	Contains the measurement results of RX/TX data throughput and time spent in each low-power LTSSM state. This viewport register returns the data selected by the TIME_BASED_REPORT_SELECT field in TIME_BASED_ANALYSIS_CONTROL_REG.For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_DATA_63_32_REG	0x0018	W	0x00000000	This viewport register returns the data selected by the TIME_BASED_REPORT_SELECT field in TIME_BASED_ANALYSIS_CONTROL_REG.For more details, see the "Reliability, Availability, and Serviceability (RAS)" section in the "Controller Operations" chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ_ENABLE_REG	0x0030	W	0x00000000	Each type of error insertion is enabled by the corresponding bit in this register. The specific injection controls for each type of error are defined in the following registers: - 0: CRC Error: EINJ0_CRC_REG - 1: Sequence Number Error: EINJ1_SEQNUM_REG - 2: DLLP Error: EINJ2_DLLP_REG - 3: Symbol DataK Mask Error or Sync Header Error: EINJ3_SYMBOL_REG - 4: FC Credit Update Error: EINJ4_FC_REG - 5: TLP Duplicate/Nullify Error: EINJ5_SP_TLP_REG - 6: Specific TLP Error: EINJ6_COMPARE_*_REG/EINJ6_CHANGE_*_REG/EINJ6_TLP_REGAfter the errors have been inserted by controller, it will clear each bit here. For more details, see the RAS DES section in the Core Operations chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ0_CRC_REG	0x0034	W	0x00000000	Controls the insertion of errors into the CRC, and parity of ordered sets for the selected type of the packets as follows: - LCRC. Bad TLP will be detected at the receiver side; receiver responds with NAK DLLP; Data Link Retry starts. - 16-bit CRC of ACK/NAK DLLPs. Bad DLLP occurs at the receiver side; Replay NUM Rollover occurs. - 16-bit CRC of UpdateFC DLLPs. Error insertion continues for the specific time; LTSSM transitions to the Recovery state because of the UpdateFC timeout (if the timeout is implemented at the receiver of the UpdateFCs). - ECRC. If ECRC check is enabled, ECRC error is detected at the receiver side. - FCRC. Framing error will be detected, TLP is discarded, and the LTSSM transitions to Recovery state. - Parity of TSOS. Error insertion continues for the specific time; LTSSM Recovery/Configuration timeout will occur. - Parity of SKPOS. Lane error will be detected at the receiver side.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ1_SEQNUM_REG	0x0038	W	0x00000000	Controls the sequence number of the specific TLPs and ACK/NAK DLLPs.Data Link Protocol Error will be detected at the Rx side of ACK/NAL DLLPs when one of these conditions is true: - ((NEXT_TRANSMIT_SEQ -1) - AckNak_Seq_Num) mod 4096 > 2048 - (AckNak_Seq_Num - ACKD_SEQ) mod 4096 >= 2048TLP is treated as Duplicate TLP at the Rx side when all these conditions are true: - Sequence Number != NEXT_RCV_SEQ - (NEXT_RCV_SEQ - Sequence Number) mod 4096 <= 2048TLP is treated as Bad TLP at the Rx side when all these conditions are true: - Sequence Number != NEXT_RCV_SEQ and - (NEXT_RCV_SEQ - Sequence Number) mod 4096 > 2048

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ2_DLLP_REG	0x003C	W	0x00000000	Controls the transmission of DLLPs and inserts the following errors: - If "ACK/NAK DLLP's transmission block" is selected, replay timeout error will occur at the transmitter of the TLPs and then Data Link Retry will occur. - If "Update FC DLLP's transmission block" is selected, LTSSM will transition to the Recovery state because of the UpdateFC timeout (if the timeout is implemented at the receiver of the UpdateFCs). - If "Always Transmission for NAK DLLP" is selected, Data Link Retry will occur at the transmitter of the TLPs. Furthermore, Replay NUM Rollover will occur when the transmitter has been requested four times to send the TLP with the same sequence number.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ3_SYMBOL_REG	0x0040	W	0x00000000	When 8b/10b encoding is used, this register controls error insertion into the special (K code) symbols. - If TS1/TS2/FTS/E-Idle/SKP is selected, it affects whole of the ordered set. It might cause timeout of the LTSSM. - If END/EDB/STP/SDP is selected, TLP/DLLP will be discarded at the receiver side. When 128b/130b encoding is used, this register controls error insertion into the sync-header.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ4_FC_REG	0x0044	W	0x00000000	Controls error insertion into the credit value in the UpdateFCs. It is possible to insert errors for any of the following types: - Posted TLP Header credit - Non-Posted TLP Header credit - Completion TLP Header credit - Posted TLP Data credit - Non-Posted TLP Data credit - Completion TLP Data credit. These errors are not correctable while error insertion is enabled. Receiver buffer overflow error might occur.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ5_SP_TLP_REG	0x0048	W	0x00000000	Controls the generation of specified TLPs. Correctable errors will occur which will be fixed by the PCIe protocol. - For Duplicate TLP, the controller initiates Data Link Retry by handling ACK DLLP as NAK DLLP. These TLPs will be duplicate TLPs at the receiver side. - For Nullified TLP, the TLPs that the controller transmits are changed into nullified TLPs and the original TLPs are stored in the retry buffer. The receiver of these TLPs will detect the lack of seq# and send NAK DLLP at the next TLP. Then the original TLPs are sent from retry buffer and the data controls are recovered. For 128 bit controller or more than 128 bit, the controller inserts errors the number of times of EINJ5_COUNT but doesn't ensure that the errors are continuously inserted into TLPs.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H0_REG	0x004C	W	0x00000000	Program this register for the 1st DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW0[7:0], TLP_DW0[15:8], TLP_DW0[23:16], TLP_DW0[31:24] The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. The type and number of errors are specified by the EINJ6_TLP_REG register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H1_REG	0x0050	W	0x00000000	Program this register for the 2nd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW1[7:0], TLP_DW1[15:8], TLP_DW1[23:16], TLP_DW1[31:24] The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. The type and number of errors are specified by the EINJ6_TLP_REG register.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H2_REG	0x0054	W	0x00000000	Program this register for the 3rd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW2[7:0], TLP_DW2[15:8], TLP_DW2[23:16], TLP_DW2[31:24] The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. The type and number of errors are specified by the EINJ6_TLP_REG register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H3_REG	0x0058	W	0x00000000	Program this register for the 4th DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW3[7:0], TLP_DW3[15:8], TLP_DW3[23:16], TLP_DW3[31:24] The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. The type and number of errors are specified by the EINJ6_TLP_REG register.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H0_REG	0x005C	W	0x00000000	Program this register for the 1st DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW0[7:0], TLP_DW0[15:8], TLP_DW0[23:16], TLP_DW0[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H1_REG	0x0060	W	0x00000000	Program this register for the 2nd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW1[7:0], TLP_DW1[15:8], TLP_DW1[23:16], TLP_DW1[31:24] The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. The type and number of errors are specified by the EINJ6_TLP_REG register.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H2_REG	0x0064	W	0x00000000	Program this register for the 3rd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW2[7:0], TLP_DW2[15:8], TLP_DW2[23:16], TLP_DW2[31:24] The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. The type and number of errors are specified by the EINJ6_TLP_REG register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H3_REG	0x0068	W	0x00000000	Program this register for the 4th DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW3[7:0], TLP_DW3[15:8], TLP_DW3[23:16], TLP_DW3[31:24] The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. The type and number of errors are specified by the EINJ6_TLP_REG register.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H0_REG	0x006C	W	0x00000000	Program this register for the 1st DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW0[7:0], TLP_DW0[15:8], TLP_DW0[23:16], TLP_DW0[31:24] The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register. Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H1_REG	0x0070	W	0x00000000	Program this register for the 2nd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW1[7:0], TLP_DW1[15:8], TLP_DW1[23:16], TLP_DW1[31:24] The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register. Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H2_REG	0x0074	W	0x00000000	Program this register for the 3rd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW2[7:0], TLP_DW2[15:8], TLP_DW2[23:16], TLP_DW2[31:24] The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register. Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H3_REG	0x0078	W	0x00000000	Program this register for the 4th DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW3[7:0], TLP_DW3[15:8], TLP_DW3[23:16], TLP_DW3[31:24] The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register. Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H0_REG	0x007C	W	0x00000000	Program this register for the 1st DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW0[7:0], TLP_DW0[15:8], TLP_DW0[23:16], TLP_DW0[31:24] The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register. Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H1_REG	0x0080	W	0x00000000	Program this register for the 2nd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW1[7:0], TLP_DW1[15:8], TLP_DW1[23:16], TLP_DW1[31:24] The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register. Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H2_REG	0x0084	W	0x00000000	Program this register for the 3rd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW2[7:0], TLP_DW2[15:8], TLP_DW2[23:16], TLP_DW2[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register. Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H3_REG	0x0088	W	0x00000000	Program this register for the 4th DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register. Bits [31:0] = TLP_DW3[7:0], TLP_DW3[15:8], TLP_DW3[23:16], TLP_DW3[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register. Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_TLP_REG	0x008C	W	0x00000000	The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. The type and number of errors are specified by the this register. The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the this register. Only applies when EINJ6_INVERTED_CONTROL in this register =0.The TLP into that errors are injected will not arrive at the transaction layer of the remote device when all of the following conditions are true. - Using 128b/130b encoding - Injecting errors into TLP Length field / TLP digest bit

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_SD_CONTROL1_REG	0x00A0	W	0x00000000	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_CONTROL2_REG	0x00A4	W	0x00000000	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L1LANE_REG	0x00B0	W	0x00180000	This viewport register returns the data selected by the following field: - LANE_SELECT in SD_STATUS_L1LANE_REGFor more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L1LTSSM_REG	0x00B4	W	0x00000200	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_PM_REG	0x00B8	W	0x00000000	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L2_REG	0x00BC	W	0x00FFF000	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L3FC_REG	0x00C0	W	0x00000000	The CREDIT_DATA[0/1] fields in this viewport register return the data for the VC and TLP Type selected by the following fields: - CREDIT_SEL_VC - CREDIT_SEL_CREDIT_TYPE - CREDIT_SEL_TLP_TYPE - CREDIT_SEL_HD. For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L3_REG	0x00C4	W	0x00000000	Silicon Debug Status(Layer3).For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL1_REG	0x00D0	W	0x00000000	This is a viewport control register. Setting the EQ_RATE_SEL and EQ_LANE_SEL fields in this register determine the per-lane Silicon Debug EQ Status data returned by the SD_EQ_STATUS[1/2/3] viewport registers. For more details, see the RAS DES section in the Core Operations chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL2_REG	0x00D4	W	0x00000000	This viewport register returns the value for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register. For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL3_REG	0x00D8	W	0x00000000	This viewport register returns the value for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register. For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS1_REG	0x00E0	W	0x00000000	This viewport register returns the first of three words of Silicon Debug EQ Status data for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register. The following fields are available when Equalization finished unsuccessfully(EQ_CONVERGENCE_INFO=2). - EQ_RULEA_VIOLATION - EQ_RULEB_VIOLATION - EQ_RULEC_VIOLATION - EQ_REJECT_EVENT. For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS2_REG	0x00E4	W	0x00000000	This viewport register returns the second of three words of Silicon Debug EQ Status data for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register. Each field is available when Equalization finished successfully(EQ_CONVERGENCE_INFO=1).For more details, see the RAS DES section in the Core Operations chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS3_REG	0x00E8	W	0x00000000	This viewport register returns the third of three words of Silicon Debug EQ Status data for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register. Each field is available when Equalization finished successfully(EQ_CONVERGENCE_INFO=1).For more details, see the RAS DES section in the Core Operations chapter of the Databook.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.9.2 Detail Registers Description

PCIE_DSP_PF0_RAS_DES_CAP_RAS_DES_CAP_HEADER_REG

Address: Operational Base(0xFE000170) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
19:16	RO	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Value of this field is depends on the version of the specification. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RO	0x000b	EXTENDED_CAP_ID PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Vendor-Specific Extended Capability is 000Bh. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_VENDOR_SPECIFIC_HEADER_REG

Address: Operational Base(0xFE000170) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:20	RO	0x100	VSEC_LENGTH VSEC Length. This field indicates the number of bytes in the entire VSEC structure, including the Vendor-Specific Extended Capability Header, the Vendor-Specific Header, and the vendor-specific registers.
19:16	RO	0x4	VSEC_REV VSEC Rev. This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field.
15:0	RO	0x0002	VSEC_ID VSEC ID. This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field.

PCIE_DSP_PF0_RAS_DES_CAP_EVENT_COUNTER_CONTROL_REG

Address: Operational Base(0xFE000170) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	RSVDP_28 Reserved for future use.
27:16	RW	0x000	EVENT_COUNTER_EVENT_SELECT Event Counter Data Select. This field in conjunction with the EVENT_COUNTER_LANE_SELECT field indexes the Event Counter data returned by the EVENT_COUNTER_DATA_REG register. - 27-24: Group number(4-bit: 0..0x7) - 23-16: Event number(8-bit: 0..0x13) within the Group - .. For detailed definitions of Group number and Event number, see the RAS DES chapter in the Databook. Note: This register field is sticky.
15:12	RO	0x0	RSVDP_12 Reserved for future use.
11:8	RW	0x0	EVENT_COUNTER_LANE_SELECT Event Counter Lane Select. This field in conjunction with EVENT_COUNTER_EVENT_SELECT indexes the Event Counter data returned by the EVENT_COUNTER_DATA_REG register. Note: This register field is sticky.
7	RO	0x0	EVENT_COUNTER_STATUS Event Counter Status. This register returns the current value of the Event Counter selected by the following fields: - EVENT_COUNTER_EVENT_SELECT - EVENT_COUNTER_LANE_SELECT Note: This register field is sticky.
6:5	RO	0x0	RSVDP_5 Reserved for future use.

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Bit	Attr	Reset Value	Description
4:2	WO	0x0	EVENT_COUNTER_ENABLE Event Counter Enable. Enables/disables the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. By default, all event counters are disabled. You can enable/disable a specific Event Counter by writing the 'per event off' or 'per event on' codes. You can enable/disable all event counters by writing the 'all on' or 'all off' codes. The read value is always '0'. For other values no change.
1:0	WO	0x0	EVENT_COUNTER_CLEAR Event Counter Clear. Clears the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. You can clear the value of a specific Event Counter by writing the 'per clear' code and you can clear all event counters at once by writing the 'all clear' code. The read value is always '0'. Other values are reserved.

PCIE_DSP_PF0_RAS_DES_CAP_EVENT_COUNTER_DATA_REG

Address: Operational Base(0xFE000170) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EVENT_COUNTER_DATA Event Counter Data. This register returns the data selected by the following fields: - EVENT_COUNTER_EVENT_SELECT in EVENT_COUNTER_CONTROL_REG Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_CONTROL_REG

Address: Operational Base(0xFE000170) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	TIME_BASED_REPORT_SELECT Time-based Report Select. Selects what type of data is measured for the selected duration (TIME_BASED_DURATION_SELECT), and returned in TIME_BASED_ANALYSIS_DATA. Each type of data is measured using one of three types of units: - Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. Total time in ps is [Value of TIME_BASED_ANALYSIS_DATA returned when TIME_BASED_REPORT_SELECT=0x00] * TIME_BASED_ANALYSIS_DATA. Values 0-4 and 7-8 correspond to Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. - Aux_clk Cycles. Total time in ps is [Period of platform specific clock] * TIME_BASED_ANALYSIS_DATA. Values 5, 6, and 9 correspond to aux_clk Cycles. - Core_clk Cycles for 20GT/s, 25GT/s (CCIX ESM data rate). Total time in ps is [Value of TIME_BASED_ANALYSIS_DATA returned when TIME_BASED_REPORT_SELECT=0x10] * TIME_BASED_ANALYSIS_DATA. Values 10-14 and 17-18 correspond to Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. - Data Bytes. Actual amount of bytes is 16 * TIME_BASED_ANALYSIS_DATA. Values 20-23 correspond to data bytes. All encodings other than the defined encodings are reserved. Note: This register field is sticky.
23:16	RO	0x00	RSVDP_16 Reserved for future use.
15:8	RW	0x01	TIME_BASED_DURATION_SELECT Time-based Duration Select. Selects the duration of time-based analysis. When "manual control" is selected and TIMER_START is set to '1', this analysis never stops until TIMER_STOP is set to '0'. All encodings other than the defined encodings are reserved. Note: This register field is sticky.
7:1	RO	0x00	RSVDP_1 Reserved for future use.
0	RW	0x0	TIMER_START Timer Start. This bit will be cleared automatically when the measurement is finished. Note: The app_ras_des_tba_ctrl input also sets the contents of this field and controls the measurement start/stop. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_DATA_REG

Address: Operational Base(0xFE000170) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TIME_BASED_ANALYSIS_DATA Time Based Analysis Data. This register returns the data selected by the TIME_BASED_REPORT_SELECT field in TIME_BASED_ANALYSIS_CONTROL_REG. The results are cleared when next measurement starts. Note: This register field is sticky.

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PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_DATA_63_32_REG

Address: Operational Base(0xFE000170) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TIME_BASED_ANALYSIS_DATA_63_32 Upper 32 bits of Time Based Analysis Data. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ_ENABLE_REG

Address: Operational Base(0xFE000170) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	RSVDP_7 Reserved for future use.
6	RW	0x0	ERROR_INJECTION6_ENABLE Error Injection6 Enable (Specific TLP Error). Enables insertion of errors into the packets that you select. You can set this bit to '1' when you have disabled RAS datapath protection (DP) by setting CX_RASDP = CX_RASDP_RAM_PROT =0. You can set this bit to '1' when you have disabled the address translation by setting ADDR_TRANSLATION_SUPPORT_EN=0. For more details, see the EINJ6_COMPARE_*_REG/EINJ6_CHANGE_*_REG/EINJ6_TLP_REG registers. Note: This register field is sticky.
5	RW	0x0	ERROR_INJECTION5_ENABLE Error Injection5 Enable (TLP Duplicate/Nullify Error). Enables insertion of duplicate/nullified TLPs. For more details, see the EINJ5_SP_TLP_REG register. Note: This register field is sticky.
4	RW	0x0	ERROR_INJECTION4_ENABLE Error Injection4 Enable (FC Credit Update Error). Enables insertion of errors into UpdateFCs. For more details, see the EINJ4_FC_REG register. Note: This register field is sticky.
3	RW	0x0	ERROR_INJECTION3_ENABLE Error Injection3 Enable (Symbol DataK Mask Error or Sync Header Error). Enables DataK masking of special symbols or the breaking of the sync header. For more details, see the EINJ3_SYMBOL_REG register. Note: This register field is sticky.
2	RW	0x0	ERROR_INJECTION2_ENABLE Error Injection2 Enable (DLLP Error). Enables insertion of DLLP errors. For more details, see the EINJ2_DLLP_REG register. Note: This register field is sticky.
1	RW	0x0	ERROR_INJECTION1_ENABLE Error Injection1 Enable (Sequence Number Error). Enables insertion of errors into sequence numbers. For more details, see the EINJ1_SEQNUM_REG register. Note: This register field is sticky.
0	RW	0x0	ERROR_INJECTION0_ENABLE Error Injection0 Enable (CRC Error). Enables insertion of errors into various CRC. For more details, see the EINJ0_CRC_REG register. Note: This register field is sticky.

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PCIE_DSP_PF0_RAS_DES_CAP_EINJ0_CRC_REG

Address: Operational Base(0xFE000170) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	RSVDP_12 Reserved for future use.
11:8	RW	0x0	EINJ0_CRC_TYPE Error injection type. Selects the type of CRC error to be inserted. All encodings other than the defined encodings are reserved. Note: This register field is sticky.
7:0	RW	0x00	EINJ0_COUNT Error injection count. Indicates the number of errors. This register is decremented when the errors have been inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION0_ENABLE in EINJ_ENABLE_REG returns 0b. - If the counter value is 0x00 and ERROR_INJECTION0_ENABLE=1, the errors are inserted until ERROR_INJECTION0_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ1_SEQNUM_REG

Address: Operational Base(0xFE000170) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	RSVDP_29 Reserved for future use.
28:16	RW	0x0000	EINJ1_BAD_SEQNUM Bad sequence number. Indicates the value to add/subtract from the naturally-assigned sequence numbers. This value is represented by two's complement. For example: - Set Type, SEQ# and Count -- EINJ1_SEQNUM_TYPE =0 (Insert errors into new TLPs) -- EINJ1_BAD_SEQNUM =0x1FFD (represents -3) -- EINJ1_COUNT =1 - Enable Error Injection -- ERROR_INJECTION1_ENABLE =1 - Send a TLP From the Core's Application Interface -- Assume SEQ#5 is given to the TLP. - The SEQ# is Changed to #2 by the Error Injection Function in Layer2. -- 5 + (-3) = 2 - The TLP with SEQ#2 is Transmitted to PCIe Link. Note: This register field is sticky.
15:9	RO	0x00	RSVDP_9 Reserved for future use.
8	RW	0x0	EINJ1_SEQNUM_TYPE Sequence number type. Selects the type of sequence number. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	EINJ1_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION1_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION1_ENABLE=1, the errors are inserted until ERROR_INJECTION1_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ2_DLLP_REG

Address: Operational Base(0xFE000170) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	RSVDP_10 Reserved for future use.
9:8	RW	0x0	EINJ2_DLLP_TYPE DLLP Type. Selects the type of DLLP errors to be inserted. Note: This register field is sticky.
7:0	RW	0x00	EINJ2_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and the error is inserted, ERROR_INJECTION2_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION2_ENABLE =1, the errors are inserted until ERROR_INJECTION2_ENABLE is set to '0'. This register is affected only when EINJ2_DLLP_TYPE =2'10b. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ3_SYMBOL_REG

Address: Operational Base(0xFE000170) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	RSVDP_11 Reserved for future use.
10:8	RW	0x0	EINJ3_SYMBOL_TYPE Error Type. 8b/10b encoding - Mask K symbol. It is not supported to insert errors into the first ordered-set after exiting from TxElecIdle when CX_FREQ_STEP_EN has been enabled. All encodings other than the defined encodings are reserved. Note: This register field is sticky.
7:0	RW	0x00	EINJ3_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION3_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION3_ENABLE =1, the errors are inserted until ERROR_INJECTION3_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ4_FC_REG

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Address: Operational Base(0xFE000170) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	RSVDP_29 Reserved for future use.
28:16	RW	0x0000	EINJ4_BAD_UPDFC_VALUE Bad update-FC credit value. Indicates the value to add/subtract from the UpdateFC credit. This value is represented by two's complement. Note: This register field is sticky.
15	RO	0x0	RSVDP_15 Reserved for future use.
14:12	RW	0x0	EINJ4_VC_NUMBER VC Number. Indicates target VC Number. Note: This register field is sticky.
11	RO	0x0	RSVDP_11 Reserved for future use.
10:8	RW	0x0	EINJ4_UPDFC_TYPE Update-FC type. Selects the credit type. Note: This register field is sticky.
7:0	RW	0x00	EINJ4_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION4_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION4_ENABLE =1, the errors are inserted until ERROR_INJECTION4_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ5_SP_TLP_REG

Address: Operational Base(0xFE000170) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	RSVDP_9 Reserved for future use.
8	RW	0x0	EINJ5_SPECIFIED_TLP Specified TLP. Selects the specified TLP to be inserted. Note: This register field is sticky.
7:0	RW	0x00	EINJ5_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION5_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION5_ENABLE =1, the errors are inserted until ERROR_INJECTION5_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H0_REG

Address: Operational Base(0xFE000170) + offset (0x004C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H0 Packet Compare Point: 1st DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H1_REG

Address: Operational Base(0xFE000170) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H1 Packet Compare Point: 2nd DWORD. Specifies which Tx TLP header DWORD#1 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H2_REG

Address: Operational Base(0xFE000170) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H2 Packet Compare Point: 3rd DWORD. Specifies which Tx TLP header DWORD#2 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H3_REG

Address: Operational Base(0xFE000170) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H3 Packet Compare Point: 4th DWORD. Specifies which Tx TLP header DWORD#3 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H0_REG

Address: Operational Base(0xFE000170) + offset (0x005C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H0 Packet Compare Value: 1st DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H1_REG

Address: Operational Base(0xFE000170) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H1 Packet Compare Value: 2nd DWORD. Specifies the value to compare against Tx the TLP header DWORD#1 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H2_REG

Address: Operational Base(0xFE000170) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H2 Packet Compare Value: 3rd DWORD. Specifies the value to compare against Tx the TLP header DWORD#2 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H3_REG

Address: Operational Base(0xFE000170) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H3 Packet Compare Value: 4th DWORD. Specifies the value to compare against Tx the TLP header DWORD#3 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H0_REG

Address: Operational Base(0xFE000170) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H0 Packet Change Point: 1st DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H1_REG

Address: Operational Base(0xFE000170) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H1 Packet Change Point: 2nd DWORD. Specifies which Tx TLP header DWORD#1 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H2_REG

Address: Operational Base(0xFE000170) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H2 Packet Change Point: 3rd DWORD. Specifies which Tx TLP header DWORD#2 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H3_REG

Address: Operational Base(0xFE000170) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H3 Packet Change Point: 4th DWORD. Specifies which Tx TLP header DWORD#3 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H0_REG

Address: Operational Base(0xFE000170) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H0 Packet Change Value: 1st DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H1_REG

Address: Operational Base(0xFE000170) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H1 Packet Change Value: 2nd DWORD. Specifies replacement values for the Tx TLP header DWORD#1 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H2_REG

Address: Operational Base(0xFE000170) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H2 Packet Change Value: 3rd DWORD. Specifies replacement values for the Tx TLP header DWORD#2 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H3_REG

Address: Operational Base(0xFE000170) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H3 Packet Change Value: 4th DWORD. Specifies replacement values for the Tx TLP header DWORD#3 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_TLP_REG

Address: Operational Base(0xFE000170) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	RSVDP_12 Reserved for future use.
11:9	RW	0x0	EINJ6_PACKET_TYPE Packet type. Selects the TLP packets to inject errors into. All encodings other than the specified encodings are reserved. Note: This register field is sticky.
8	RW	0x0	EINJ6_INVERTED_CONTROL Inverted Error Injection Control. Encoded values given as above. Note: This register field is sticky.
7:0	RW	0x00	EINJ6_COUNT Error Injection Count. Indicates the number of errors to insert. This counter is decremented while errors are inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION6_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION6_ENABLE=1, errors are inserted until ERROR_INJECTION6_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_CONTROL1_REG

Address: Operational Base(0xFE000170) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	RSVDP_24 Reserved for future use.

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Bit	Attr	Reset Value	Description
23:22	RW	0x0	LOW_POWER_INTERVAL Low Power Entry Interval Time. Interval Time that the controller starts monitoring RXELECIDLE signal after L0s/L1/L2 entry. You should set the value according to the latency from receiving EIOS to, RXELECIDLE assertion at the PHY. Note: This register field is sticky.
21:20	RW	0x0	TX_EIOS_NUM Number of Tx EIOS. This register sets the number of transmit EIOS for L0s/L1 entry and Disable/Loopback/Hot-reset exit. The controller selects the greater value between this register and the value defined by the PCI-SIG specification. Note: This register field is sticky.
19:17	RO	0x0	RSVDP_17 Reserved for future use.
16	RW	0x0	FORCE_DETECT_LANE_EN Force Detect Lane Enable. Note: This register field is sticky.
15:0	RW	0x0000	FORCE_DETECT_LANE Force Detect Lane. When the FORCE_DETECT_LANE_EN field is set, the controller ignores receiver detection from PHY during LTSSM Detect state and uses this value instead. Value represents lane number. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_CONTROL2_REG

Address: Operational Base(0xFE000170) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	RSVDP_17 Reserved for future use.
16	RW	0x0	FRAMING_ERR_RECOVERY_DISABLE Framing Error Recovery Disable. This bit disables a transition to Recovery state when a Framing Error is occurred. Note: This register field is sticky.
15:11	RO	0x00	RSVDP_11 Reserved for future use.
10	RW	0x0	DIRECT_LPBKSLV_TO_EXIT Direct Loopback Slave To Exit. Note: This register field is sticky.
9	RW	0x0	DIRECT_POLCOMP_TO_DETECT Direct Polling.Compliance to Detect. Note: This register field is sticky.
8	RW	0x0	DIRECT_RECIDLE_TO_CONFIG Direct Recovery.Idle to Configuration. Note: This register field is sticky.
7:3	RO	0x00	RSVDP_3 Reserved for future use.
2	RW	0x0	NOACK_FORCE_LINKDOWN Force LinkDown. Note: This register field is sticky.
1	WO	0x0	RECOVERY_REQUEST Recovery Request.

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Bit	Attr	Reset Value	Description
0	RW	0x0	HOLD_LTSSM Hold and Release LTSSM. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L1LANE_REG

Address: Operational Base(0xFE000170) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DESKEW_POINTER Deskew Pointer. Indicates Deskew pointer of internal Deskew buffer of selected lane number(LANE_SELECT). Note: This register field is sticky.
23:21	RO	0x0	RSVDP_21 Reserved for future use.
20	RO	0x1	PIPE_TXELECIDLE PIPE:TxElecIdle. Indicates PIPE TXELECIDLE signal of selected lane number(LANE_SELECT). Note: This register field is sticky.
19	RO	0x1	PIPE_RXELECIDLE PIPE:RxElecIdle. Indicates PIPE RXELECIDLE signal of selected lane number(LANE_SELECT). Note: This register field is sticky.
18	RO	0x0	PIPE_RXVALID PIPE:RxValid. Indicates PIPE RXVALID signal of selected lane number(LANE_SELECT). Note: This register field is sticky.
17	RO	0x0	PIPE_DETECT_LANE PIPE:Detect Lane. Indicates whether PHY indicates receiver detection or not on selected lane number(LANE_SELECT). Note: This register field is sticky.
16	RO	0x0	PIPE_RXPOLARITY PIPE:RxPolarity. Indicates PIPE RXPOLARITY signal of selected lane number(LANE_SELECT). Note: This register field is sticky.
15:4	RO	0x000	RSVDP_4 Reserved for future use.
3:0	RW	0x0	LANE_SELECT Lane Select. Lane Select register for Silicon Debug Status Register of Layer1-PerLane. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L1LTSSM_REG

Address: Operational Base(0xFE000170) + offset (0x00B4)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	LTSSM_VARIABLE LTSSM Variable. Indicates internal LTSSM variables defined in the PCI Express Base Specification. For other value idle_to_rlock_transitioned. Note: This register field is sticky.
15	RO	0x0	LANE_REVERSAL Lane Reversal Operation. Receiver detected lane reversal. This field is only valid in the L0 LTSSM state. Note: This register field is sticky.
14:11	RO	0x0	RSVDP_11 Reserved for future use.
10:8	RO	0x2	PIPE_POWER_DOWN PIPE:PowerDown. Indicates PIPE PowerDown signal. Note: This register field is sticky.
7	RW	0x0	FRAMING_ERR Framing Error. Indicates Framing Error detection status. Note: This register field is sticky.
6:0	RO	0x00	FRAMING_ERR_PTR First Framing Error Pointer. Identifies the first Framing Error using the following encoding. The field contents are only valid value when FRAMING_ERR =1. - Received Unexpected Framing Token (Values 01h to 06h) - Received Unexpected STP Token (Values 11h to 13h) - Received Unexpected Block (Values 21h to 2Eh) All encodings other than the defined encodings are reserved. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_PM_REG

Address: Operational Base(0xFE000170) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	RSVDP_24 Reserved for future use.
23:16	RO	0x00	LATCHED_NFTS Latched N_FTS. Indicates the value of N_FTS in the received TS Ordered Sets from the Link Partner. Note: This register field is sticky.
15:13	RO	0x0	L1SUB_STATE L1Sub State. Indicates internal state machine of L1Sub state. Note: This register field is sticky.
12	RW	0x0	PME_RESEND_FLAG PME Re-send flag. When the DUT sends a PM_PME message TLP, the DUT sets PME_Status bit. If host software does not clear PME_Status bit for 100ms(+50%/-5%), the DUT resends the PM_PME Message. This bit indicates that a PM_PME was resent. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
11:8	RO	0x0	INTERNAL_PM_SSTATE Internal PM State(Slave). Indicates internal state machine of Power Management Slave controller. Note: This register field is sticky.
7:5	RO	0x0	RSVDP_5 Reserved for future use.
4:0	RO	0x00	INTERNAL_PM_MSTATE Internal PM State(Master). Indicates internal state machine of Power Management Master controller. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L2_REG

Address: Operational Base(0xFE000170) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	RSVDP_28 Reserved for future use.
27	RO	0x0	FC_INIT2 FC_INIT2. Indicates the controller is in FC_INIT2(VC0) state. Note: This register field is sticky.
26	RO	0x0	FC_INIT1 FC_INIT1. Indicates the controller is in FC_INIT1(VC0) state. Note: This register field is sticky.
25:24	RO	0x0	DLCMSM DLCMSM. Indicates the current DLCMSM. Note: This register field is sticky.
23:12	RO	0xfff	RX_ACK_SEQ_NO Tx Ack Sequence Number. Indicates ACKD_SEQ which is updated by receiving ACK/NAK DLLP. Note: This register field is sticky.
11:0	RO	0x000	TX_TLP_SEQ_NO Tx Tlp Sequence Number. Indicates next transmit sequence number for transmit TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L3FC_REG

Address: Operational Base(0xFE000170) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	CREDIT_DATA1 Credit Data1. Current FC credit data selected by the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields. - Rx: Credit Allocated Value - Tx: Credit Limit Value. This value is valid when DLCMSM=0x3(DL_ACTIVE). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
19:8	RO	0x000	CREDIT_DATA0 Credit Data0. Current FC credit data selected by the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields. - Rx: Credit Received Value - Tx: Credit Consumed Value Note: This register field is sticky.
7	RO	0x0	RSVDP_7 Reserved for future use.
6	RW	0x0	CREDIT_SEL_HD Credit Select(HeaderData). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, and CREDIT_SEL_TLP_TYPE viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky.
5:4	RW	0x0	CREDIT_SEL_TLP_TYPE Credit Select(TLP Type). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky.
3	RW	0x0	CREDIT_SEL_CREDIT_TYPE Credit Select(Credit Type). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky.
2:0	RW	0x0	CREDIT_SEL_VC Credit Select(VC). This field in conjunction with the CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L3_REG

Address: Operational Base(0xFE000170) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7	RW	0x0	MFTLP_STATUS Malformed TLP Status. Indicates malformed TLP has occurred. Note: This register field is sticky.
6:0	RO	0x00	MFTLP_POINTER First Malformed TLP Error Pointer. Indicates the element of the received first malformed TLP. This pointer is validated by MFTLP_STATUS. All encodings other than the defined encodings are reserved. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL1_REG

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Address: Operational Base(0xFE000170) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	FOM_TARGET FOM Target. Indicates figure of merit target criteria value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2). This field is only valid when GEN3_EQ_FB_MODE is 0001b(Figure Of Merit). Note: This register field is sticky.
23	RW	0x0	FOM_TARGET_ENABLE FOM Target Enable. Enables the FOM_TARGET fields. Note: This register field is sticky.
22:18	RO	0x00	RSVDP_18 Reserved for future use.
17:16	RW	0x0	EVAL_INTERVAL_TIME Eval Interval Time. Indicates interval time of RxEqEval assertion. This field is used for EQ Master(DSP in EQ Phase3/USP in EQ Phase2). Note: This register field is sticky.
15:10	RO	0x00	RSVDP_10 Reserved for future use.
9:8	RW	0x0	EXT_EQ_TIMEOUT Extends EQ Phase2/3 Timeout. This field is used when the LTSSM is in Recovery.EQ2/3. When this field is set, the value of EQ2/3 timeout is extended. Note: This register field is sticky.
7:6	RO	0x0	RSVDP_6 Reserved for future use.
5:4	RW	0x0	EQ_RATE_SEL EQ Status Rate Select. Setting this field in conjunction with the EQ_LANE_SEL field determines the per-lane Silicon Debug EQ Status data returned by the SD_EQ_CONTROL[2/3] and SD_EQ_STATUS[1/2/3] viewport registers. Note: This register field is sticky.
3:0	RW	0x0	EQ_LANE_SEL EQ Status Lane Select. Setting this field in conjunction with the EQ_RATE_SEL field determines the per-lane Silicon Debug EQ Status data returned by the SD_EQ_CONTROL[2/3] and SD_EQ_STATUS[1/2/3] viewport registers. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL2_REG

Address: Operational Base(0xFE000170) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30	RW	0x0	FORCE_LOCAL_TX_PRESET_ENABLE Force Local Transmitter Preset Enable. Enables the FORCE_LOCAL_TX_PRESET field. If select rate in the EQ_RATE_SEL field is 32.0GT/s Speed, this feature is not available. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
29	RW	0x0	FORCE_LOCAL_RX_HINT_ENABLE Force Local Receiver Preset Hint Enable. Enables the FORCE_LOCAL_RX_HINT field. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky.
28	RW	0x0	FORCE_LOCAL_TX_COEF_ENABLE Force Local Transmitter Coefficient Enable. Enables the following fields: - FORCE_LOCAL_TX_PRE_CURSOR - FORCE_LOCAL_TX_CURSOR - FORCE_LOCAL_TX_POST_CURSOR Note: This register field is sticky.
27:24	RW	0x0	FORCE_LOCAL_TX_PRESET Force Local Transmitter Preset. Indicates initial preset value of USP in EQ Slave(EQ Phase2) instead of receiving EQ TS2. If select rate in the EQ_RATE_SEL field is 32.0GT/s Speed, this feature is not available. Note: This register field is sticky.
23:21	RO	0x0	RSVDP_21 Reserved for future use.
20:18	RW	0x0	FORCE_LOCAL_RX_HINT Force Local Receiver Preset Hint. Indicates the RxPresetHint value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of received or set value. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky.
17:12	RW	0x00	FORCE_LOCAL_TX_POST_CURSOR Force Local Transmitter Post-Cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky.
11:6	RW	0x00	FORCE_LOCAL_TX_CURSOR Force Local Transmitter Cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky.
5:0	RW	0x00	FORCE_LOCAL_TX_PRE_CURSOR Force Local Transmitter Pre-cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL3_REG

Address: Operational Base(0xFE000170) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	RSVDP_29 Reserved for future use.

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Bit	Attr	Reset Value	Description
28	RW	0x0	FORCE_REMOTE_TX_COEF_ENABLE Force Remote Transmitter Coefficient Enable. Enables the following fields: - FORCE_REMOTE_TX_PRE_CURSOR - FORCE_REMOTE_TX_CURSOR - FORCE_REMOTE_TX_POST_CURSOR This function can only be used when GEN3_EQ_FB_MODE = 0000b(Direction Change) Note: This register field is sticky.
27:18	RO	0x000	RSVDP_18 Reserved for future use.
17:12	RW	0x00	FORCE_REMOTE_TX_POST_CURSOR Force Remote Transmitter Post-Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky.
11:6	RW	0x00	FORCE_REMOTE_TX_CURSOR Force Remote Transmitter Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky.
5:0	RW	0x00	FORCE_REMOTE_TX_PRE_CURSOR Force Remote Transmitter Pre-Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS1_REG

Address: Operational Base(0xFE000170) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7	RO	0x0	EQ_REJECT_EVENT EQ Reject Event. Indicates that the controller receives two consecutive TS1 OS w/Reject=1b during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.
6	RO	0x0	EQ_RULEC_VIOLATION EQ Rule C Violation. Indicates that coefficients rule C violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rule C correspond to the rules c) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5	RO	0x0	EQ_RULEB_VIOLATION EQ Rule B Violation. Indicates that coefficients rule B violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rules B correspond to the rules b) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.
4	RO	0x0	EQ_RULEA_VIOLATION EQ Rule A Violation. Indicates that coefficients rule A violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rules A correspond to the rules a) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.
3	RO	0x0	RSVDP_3 Reserved for future use.
2:1	RO	0x0	EQ_CONVERGENCE_INFO EQ Convergence Info. Indicates equalization convergence information. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.
0	RO	0x0	EQ_SEQUENCE EQ Sequence. Indicates that the controller is starting the equalization sequence. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS2_REG

Address: Operational Base(0xFE000170) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EQ_LOCAL_FOM_VALUE EQ Local Figure of Merit. Indicates Local maximum Figure of Merit value. Note: This register field is sticky.
23:21	RO	0x0	RSVDP_21 Reserved for future use.
20:18	RO	0x0	EQ_LOCAL_RX_HINT EQ Local Receiver Preset Hint. Indicates Local Receiver Preset Hint value. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky.
17:12	RO	0x00	EQ_LOCAL_POST_CURSOR EQ Local Post-Cursor. Indicates Local post cursor coefficient value. Note: This register field is sticky.
11:6	RO	0x00	EQ_LOCAL_CURSOR EQ Local Cursor. Indicates Local cursor coefficient value. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	EQ_LOCAL_PRE_CURSOR EQ Local Pre-Cursor. Indicates Local pre cursor coefficient value. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS3_REG

Address: Operational Base(0xFE000170) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	RSVDP_30 Reserved for future use.
29:24	RO	0x00	EQ_REMOTE_FS EQ Remote FS. Indicates Remote FS value. Note: This register field is sticky.
23:18	RO	0x00	EQ_REMOTE_LF EQ Remote LF. Indicates Remote LF value. Note: This register field is sticky.
17:12	RO	0x00	EQ_REMOTE_POST_CURSOR EQ Remote Post-Cursor. Indicates Remote post cursor coefficient value. Note: This register field is sticky.
11:6	RO	0x00	EQ_REMOTE_CURSOR EQ Remote Cursor. Indicates Remote cursor coefficient value. Note: This register field is sticky.
5:0	RO	0x00	EQ_REMOTE_PRE_CURSOR EQ Remote Pre-Cursor. Indicates Remote pre cursor coefficient value. Note: This register field is sticky.

7.4.3.10 PCIE_DSP_PF0_PORT_LOGIC

7.4.3.10.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_ACK_LATENCY_TIMER_OFF	0x0000	W	0x0C23040B	This register holds the ack latency timer limit and replay timer limit values.
PCIE_DSP_PF0_PORT_LOGIC_VENDOR_SPEC_DLLP_OFF	0x0004	W	0xFFFFFFFF	This register holds the vendor specific DLLP.
PCIE_DSP_PF0_PORT_LOGIC_PORT_FORCE_OFF	0x0008	W	0x00000004	This register can be used for testing and debugging the link.
PCIE_DSP_PF0_PORT_LOGIC_ACK_F_ASPM_CTRL_OFF	0x000C	W	0x1BFFFF00	This register is used to control ack frequency and L0-L1 ASPM behaviour.
PCIE_DSP_PF0_PORT_LOGIC_PORT_LINK_CTRL_OFF	0x0010	W	0x00010120	Using this register you can control the port link behaviour.
PCIE_DSP_PF0_PORT_LOGIC_LANE_SKEW_OFF	0x0014	W	0x00000000	This register is used to control the lane skew behaviour.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_TIMER_CTRL_MAX_FUNC_NUM_OFF	0x0018	W	0x00018000	This register holds the ack frequency, latency, replay, fast link scaling timers, and max function number values.
PCIE_DSP_PF0_PORT_LOGIC_SYMBOL_TIMER_FILTER_1_OFF	0x001C	W	0x00000140	The Filter Mask 1 Register modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" section. In each case, '0' applies the associated filtering rule and '1' masks the associated filtering rule.
PCIE_DSP_PF0_PORT_LOGIC_FILTER_MASK_2_OFF	0x0020	W	0x00000000	This register modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" section. In each case, '0' applies the associated filtering rule and '1' masks the associated filtering rule.
PCIE_DSP_PF0_PORT_LOGIC_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF	0x0024	W	0x00000001	This register controls multiple outbound decomposed NP subRequests operation.
PCIE_DSP_PF0_PORT_LOGIC_PL_DEBUG0_OFF	0x0028	W	0x00000000	This register holds cxpl_debug_info[31:0].
PCIE_DSP_PF0_PORT_LOGIC_PL_DEBUG1_OFF	0x002C	W	0x00000000	This register holds cxpl_debug_info[63:32].
PCIE_DSP_PF0_PORT_LOGIC_TX_P_FC_CREDIT_STATUS_OFF	0x0030	W	0x00000000	This register provides transmit posted FC credit status.
PCIE_DSP_PF0_PORT_LOGIC_TX_NP_FC_CREDIT_STATUS_OFF	0x0034	W	0x00000000	This register provides the transmit Non-Posted FC credit status.
PCIE_DSP_PF0_PORT_LOGIC_TX_CPL_FC_CREDIT_STATUS_OFF	0x0038	W	0x00000000	This register provides transmit completion FC credit status.
PCIE_DSP_PF0_PORT_LOGIC_QUEUE_STATUS_OFF	0x003C	W	0x00000000	This register provides the queue status.
PCIE_DSP_PF0_PORT_LOGIC_VC_TX_ARBI_1_OFF	0x0040	W	0x0000000F	This register is used for setting the WRR weights for VC0 - VC3.
PCIE_DSP_PF0_PORT_LOGIC_VC_TX_ARBI_2_OFF	0x0044	W	0x00000000	This register is used for setting the WRR weights for VC4 - VC7.
PCIE_DSP_PF0_PORT_LOGIC_VC0_P_RX_Q_CTRL_OFF	0x0048	W	0x45217038	This register controls segmented-buffer VC0 posted receive queue operation.
PCIE_DSP_PF0_PORT_LOGIC_VC0_NP_RX_Q_CTRL_OFF	0x004C	W	0x05217005	This register controls the segmented-buffer VC0 non-posted receive queue operation.
PCIE_DSP_PF0_PORT_LOGIC_VC0_CPL_RX_Q_CTRL_OFF	0x0050	W	0x05200000	This register controls the segmented-buffer VC0 completion receive queue operation.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_GEN2_CTRL_OFF	0x010C	W	0x000001FF	This register controls various functions of the controller related to link training, lane reversal, and equalization.
PCIE_DSP_PF0_PORT_LOGIC_PHY_STATUS_OFF	0x0110	W	0x00000000	Memory mapped register from phy_cfg_status GPIO input pins.
PCIE_DSP_PF0_PORT_LOGIC_PHY_CONTROL_OFF	0x0114	W	0x00000000	Memory mapped register to cfg_phy_control GPIO output pins.
PCIE_DSP_PF0_PORT_LOGIC_TRGT_MAP_CTRL_OFF	0x011C	W	0x0000007F	This register controls the target map.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_ADDR_OFF	0x0120	W	0x00000000	This register holds the integrated MSI reception module address.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_UPPER_ADDR_OFF	0x0124	W	0x00000000	This register holds the integrated MSI reception module upper address.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_EN_OFF	0x0128	W	0x00000000	This register enables integrated MSI reception module interrupt0.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_MASK_OFF	0x012C	W	0x00000000	This register provides information regarding the MSI Interrupt0 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_STATUS_OFF	0x0130	W	0x00000000	This register provides the MSI Interrupt0 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_EN_OFF	0x0134	W	0x00000000	This register enables integrated MSI reception module interrupt1.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_MASK_OFF	0x0138	W	0x00000000	This register provides information regarding the MSI Interrupt1 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_STATUS_OFF	0x013C	W	0x00000000	This register provides the MSI Interrupt1 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_EN_OFF	0x0140	W	0x00000000	This register enables integrated MSI reception module interrupt2.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_MASK_OFF	0x0144	W	0x00000000	This register provides information regarding the MSI Interrupt2 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_STATUS_OFF	0x0148	W	0x00000000	This register provides the MSI Interrupt2 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_EN_OFF	0x014C	W	0x00000000	This register enables integrated MSI reception module interrupt3.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_MASK_OFF	0x0150	W	0x00000000	This register provides information regarding the MSI Interrupt3 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_STATUS_OFF	0x0154	W	0x00000000	This register provides the MSI Interrupt3 status.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_EN_OFF	0x0158	W	0x00000000	This register enables integrated MSI reception module interrupt4.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_MASK_OFF	0x015C	W	0x00000000	This register provides information regarding the MSI Interrupt4 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_STATUS_OFF	0x0160	W	0x00000000	This register provides the MSI Interrupt4 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_EN_OFF	0x0164	W	0x00000000	This register enables integrated MSI reception module interrupt5.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_MASK_OFF	0x0168	W	0x00000000	This register provides information regarding the MSI Interrupt5 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_STATUS_OFF	0x016C	W	0x00000000	This register provides the MSI Interrupt5 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_EN_OFF	0x0170	W	0x00000000	This register enables integrated MSI reception module interrupt6.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_MASK_OFF	0x0174	W	0x00000000	This register provides information regarding the MSI Interrupt6 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_STATUS_OFF	0x0178	W	0x00000000	This register provides the MSI Interrupt6 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_EN_OFF	0x017C	W	0x00000000	This register enables integrated MSI reception module interrupt7.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_MASK_OFF	0x0180	W	0x00000000	This register provides information regarding the MSI Interrupt7 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_STATUS_OFF	0x0184	W	0x00000000	This register provides the MSI Interrupt7 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_GPIO_IO_OFF	0x0188	W	0x00000000	The contents of this register drive the top-level GPIO msi_ctrl_io[31:0].
PCIE_DSP_PF0_PORT_LOGIC_CLOCK_GATING_CTRL_OFF	0x018C	W	0x00000003	This register enables you to disable dynamic clock gating. By default, dynamic clock gating is on, allowing the controller to autonomously enable and disable its clocks. The clock gating is performed in the clock and reset module, DWC_pcie_clk_rst.v, and is initiated by the controllers clock enable signals. The following modules support dynamic clock gating: - AXI Bridge - RADM

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_GEN3_RELATED_OFF	0x0190	W	0x00002001	There is no Gen3-specific N_FTS field. The N_FTS field in the "Link Width and Speed Change Control Register" is used for both Gen2 and Gen3 speed modes. There is no Gen3-specific "Directed Speed Change" field. The "Directed Speed Change" field in the "Link Width and Speed Change Control Register" is used to change to Gen2 or Gen3 speed. A speed change to Gen3 occurs if (1) the "Directed Speed Change" field is set to '1' and (2) the "Target Link Speed" field in the Link Control 2 Register is set to Gen3. Gen3 support is advertised by both sides of the link during link training.
PCIE_DSP_PF0_PORT_LOGIC_GEN3_EQ_CONTROL_OFF	0x01A8	W	0x04059F61	This register controls equalization for Phase2 in an upstream port (USP), or Phase3 in a downstream port (DSP).
PCIE_DSP_PF0_PORT_LOGIC_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF	0x01AC	W	0x00000040	Equalization controls to be used in Phase2 (USP) or Phase 3 (DSP), when you set the Feedback Mode in "Gen3 EQ Control Register" to "Direction Change." These fields allow control over the initial starting point for the search of optimal coefficient settings, and allow control over the criteria used to determine when the optimal settings have been achieved. The values are applied to all the lanes.
PCIE_DSP_PF0_PORT_LOGIC_ORDER_RULE_CTRL_OFF	0x01B4	W	0x00000000	This register controls the order rule.
PCIE_DSP_PF0_PORT_LOGIC_PIPE_LOOPBACK_CONTROL_OFF	0x01B8	W	0x00000001	This register controls the PIPE Loopback.
PCIE_DSP_PF0_PORT_LOGIC_MISC_CONTROL_1_OFF	0x01BC	W	0x000BFF40	This is the DBI Read-Only write enable register.
PCIE_DSP_PF0_PORT_LOGIC_MULTI_LANE_CONTROL_OFF	0x01C0	W	0x00000000	Used when upsizing or downsizing the link width through Configuration state without bringing the link down. For more details, see the "Link Establishment" section in the "ControllerOperations" chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_PHY_INTEROP_CTRL_OFF	0x01C4	W	0x0001E001	This register controls the PHY interoperability.
PCIE_DSP_PF0_PORT_LOGIC_TRGT_CPL_LUT_DELETE_ENTRY_OFF	0x01C8	W	0x00000000	Using this register, you can delete one entry in the target completion LUT. You should only use this register when you know that your application will never send the completion because of an FLR or any other reason. Note: The target completion LUT (and associated target completion timeout event) is watching for completions (from your application on XALI0/1/2 or AXI master read channel) corresponding to previously received non-posted requests from the PCIe wire.
PCIE_DSP_PF0_PORT_LOGIC_LINK_FLUSH_CONTROL_OFF	0x01CC	W	0xFF000001	This register controls link reset request flush behaviour.
PCIE_DSP_PF0_PORT_LOGIC_AMBA_ERROR_RESPONSE_DEFAULT_OFF	0x01D0	W	0x00009C00	This register holds the AXI bridge slave error responses.
PCIE_DSP_PF0_PORT_LOGIC_AMBA_LINK_TIMEOUT_OFF	0x01D4	W	0x00000032	If your application AXI master issues outbound requests to the AXI bridge slave interface before the PCIe link is operational, the controller starts a "flush" timer. The timeout value of the timer is set by this register. If the timer times out before the PCIe link is operational, the bridge TX request queues are flushed. For more details, see the "AXI Bridge Initialization, Clocking and Reset" section in the AXI chapter of the Databook.
PCIE_DSP_PF0_PORT_LOGIC_AMBA_ORDERING_CTRL_OFF	0x01D8	W	0x00000000	This register controls the AXI Bridge Ordering.
PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_1_OFF	0x01E0	W	0x00000000	This register controls the ACE cache coherency operation.
PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_2_OFF	0x01E4	W	0x00000000	This register controls the ACE cache coherency operation.
PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_3_OFF	0x01E8	W	0x00000000	This register controls the ACE cache coherency operation.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_AXI_MSTR_MSG_ADDR_LOW_OFF	0x01F0	W	0x00000000	Lower 20 bits of the programmable AXI address to which Messages coming from wire are mapped. Bits [11:0] of the register are tied to zero for the address to be 4k-aligned. In previous releases, the third and fourth DWORDs of a message (Msg/MsgD) TLP header were delivered though the AXI master address bus (mstr_awaddr). These DWORDS are now supplied through the mstr_awmisc_info_hdr_34dw[63:0] output; and the value on mstr_awaddr is driven to the value you have programmed into the AXI_MSTR_MSG_ADDR_LOW_OFF and AXI_MSTR_MSG_ADDR_HIGH_OFF registers.
PCIE_DSP_PF0_PORT_LOGIC_AXI_MSTR_MSG_ADDR_HIGH_OFF	0x01F4	W	0x00000000	Upper 32 bits of the programmable AXI address to which Messages coming from wire are mapped.
PCIE_DSP_PF0_PORT_LOGIC_PCIE_VERSION_NUMBER_OFF	0x01F8	W	0x3536302A	The version number is given in hex format. You should convert each pair of hex characters to ASCII to interpret. Using 4.70a (GA) as an example: - VERSION_NUMBER = 0x3437302a which translates to 470* - VERSION_TYPE = 0x67612a2a which translates to ga**Using 4.70a-ea01 as an example: - VERSION_NUMBER = 0x3437302a which translates to 470* - VERSION_TYPE = 0x65613031 which translates to ea01GA is a general release available on www.designware.comEA is an early release available on a per-customer basis.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_PCIE_VERSION_TYPE_OFF	0x01FC	W	0x6C703035	The type is given in hex format. You should convert each pair of hex characters to ASCII to interpret. Using 4.70a (GA) as an example: - VERSION_NUMBER = 0x3437302a which translates to 470* - VERSION_TYPE = 0x67612a2a which translates to ga**Using 4.70a-ea01 as an example: - VERSION_NUMBER = 0x3437302a which translates to 470* - VERSION_TYPE = 0x65613031 which translates to ea01GA is a general release available on www.designware.comEA is an early release available on a per-customer basis.
PCIE_DSP_PF0_PORT_LOGIC_PL_APP_BUS_DEV_NUM_STATUS_OFF	0x0410	W	0x00000000	This register reflects the application driven bus and device number.
PCIE_DSP_PF0_PORT_LOGIC_PCIPM_TRAFFIC_CTRL_OFF	0x041C	W	0x00000000	This register provides control over TLP Traffic during Non-D0 States.
PCIE_DSP_PF0_PORT_LOGIC_PL_LTR_LATENCY_OFF	0x0430	W	0x00000000	The function of this register field (and all other fields in this register) differs between an upstream port and a downstream port. For an upstream port, the register fields capture the corresponding fields in the LTR messages that are transmitted by the port. For a downstream port, the register fields capture the corresponding fields in the LTR messages that are received by the port. The full content of the register is reflected on the app_ltr_latency[31:0] output.
PCIE_DSP_PF0_PORT_LOGIC_AUX_CLK_FREQ_OFF	0x0440	W	0x00000018	This register controls the auxiliary clock frequency.
PCIE_DSP_PF0_PORT_LOGIC_L1_SUBSTATES_OFF	0x0444	W	0x000000D2	This register holds L1 substates timing information.
PCIE_DSP_PF0_PORT_LOGIC_POWERDOWN_CTRL_STATUS_OFF	0x0448	W	0x00000220	This is the Powerdown Control and Status register.
PCIE_DSP_PF0_PORT_LOGIC_PIPE_RELATED_OFF	0x0490	W	0x00000000	This register controls the PIPE's capability, control, and status parameters.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.10.2 Detail Registers Description

PCIE_DSP_PF0_PORT_LOGIC_ACK_LATENCY_TIMER_OFF

Address: Operational Base(0xFE000700) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0c23	REPLAY_TIME_LIMIT Replay Timer Limit. The replay timer expires when it reaches this limit. The controller initiates a replay upon reception of a NAK or when the replay timer expires. For more details, see "Transmit Replay" in the Databook. - You can modify the effective timer limit through the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. - After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-4, 3-5, and 3-6 of the PCI Express Base Specification. - If there is a change in the payload size or link speed, the controller overrides any value that you have written to this register field, and resets the field back to the specification-defined value. The controller does not change the value in the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register.
15:0	RW	0x040b	ROUND_TRIP_LATENCY_TIME_LIMIT Ack Latency Timer Limit. The Ack latency timer expires when it reaches this limit. For more details, see "ACK/NAK Scheduling" in the Databook. - You can modify the effective timer limit through the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. - After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-7, 3-8, and 3-9 of the PCI Express Base Specification. - The limit must reflect the round trip latency from requester to completer. - If there is a change in the payload size or link width, the controller overrides any value that you have written to this register field, and resets the field back to the specification-defined value. The controller does not change the value in the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register.

PCIE_DSP_PF0_PORT_LOGIC_VENDOR_SPEC_DLLP_OFF

Address: Operational Base(0xFE000700) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	VENDOR_SPEC_DLLP Vendor Specific DLLP Register. You can use this register to send a specific PCI Express DLLP. Your application can write 8-bit DLLP Type and 24-bit Payload data into this register, and set the VENDOR_SPECIFIC_DLLP_REQ field of the PORT_LINK_CTRL_OFF, to send the DLLP. - Bits[7:0]: DLLP Type - Bits[31:8]: Vendor Defined Payload (24 bits) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PORT_FORCE_OFF

Address: Operational Base(0xFE000700) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	RSVDP_24 Reserved for future use.

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Bit	Attr	Reset Value	Description
23	RW	0x0	DO_DESKEW_FOR_SRIS Use the transitions from TS2 to Logical Idle Symbol, SKP OS to Logical Idle Symbol, EIEOS to Logical Idle Symbol, and FTS Sequence to SKP OS to do deskew instead of using received SKP OS or TS1 to TS2 transition if DO_DESKEW_FOR_SRIS is set to '1'. Note: This register field is sticky.
22	RW	0x0	SUPPORT_PART_LANES_RXEI_EXIT Support LTSSM transition from Polling.Active to Polling.Config based on Rx 8 TSs on any lanes which are Rx EI exit too from base spec after 24ms timeout. This prevents some lanes detected but not Rx EI exit and LTSSM cannot move to Polling.Config. You must set the parameter CX_AUTO_LANE_FLIP_CTRL_EN true for the auto lanes reversal. Note: This register field is sticky.
21:16	RW	0x00	LINK_STATE Forced LTSSM State. The LTSSM state that the controller is forced to when you set the FORCE_EN bit (Force Link). LTSSM state encoding is defined by the lts_state variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky.
15	WO	0x0	FORCE_EN Force Link. The controller supports a testing and debug capability to allow your software to force the LTSSM state machine into a specific state, and to force the controller to transmit a specific Link Command. Asserting this bit triggers the following actions: - Forces the LTSSM to the state specified by the Forced LTSSM State field. - Forces the controller to transmit the command specified by the Forced Link Command field. This is a self-clearing register field. Reading from this register field always returns a '0'.
14:12	RO	0x0	RSVDP_12 Reserved for future use.
11:8	RW	0x0	FORCED_LTSSM Forced Link Command. The link command that the controller is forced to transmit when you set FORCE_EN bit (Force Link). Link command encoding is defined by the ltssm_cmd variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky.
7:0	RW	0x04	LINK_NUM Link Number. Not used for endpoint. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_ACK_F_ASPM_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30	RW	0x0	ENTER_ASPM ASPM L1 Entry Control. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
29:27	RW	0x3	L1_ENTRANCE_LATENCY L1 Entrance Latency. Note: Programming this timer with a value greater that 32us has no effect unless extended sync is used, or all of the credits are infinite. Note: This register field is sticky.
26:24	RW	0x3	L0S_ENTRANCE_LATENCY L0s Entrance Latency. Note: This register field is sticky.
23:16	RW	0xff	COMMON_CLK_N_FTS Common Clock N_FTS. This is the N_FTS when common clock is used. The number of Fast Training Sequence ordered sets to be transmitted when transitioning from L0s to L0. This field is only writable (sticky) when all of the following configuration parameter equations are true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
15:8	RW	0xff	ACK_N_FTS The number of Fast Training Sequence(N_FTS) ordered sets to be transmitted when transitioning from L0s to L0. Note: This register field is sticky.
7:0	RW	0x00	ACK_FREQ Ack Frequency. The controller accumulates the number of pending ACKs specified here (up to 255) before scheduling an ACK DLLP. - 0: Indicates that this Ack Frequency Counter feature is turned off. The controller generates a low-priority ACK request for every TLP that it receives. The controller waits until the ACK Latency Timer expires, then converts the current low-priority ACK request to a high-priority ACK request and schedules the DLLP for transmission to the remote link partner. - 1-255: Indicates that the controller will schedule a high-priority ACK after receiving this number of TLPs. It might schedule the ACK before receiving this number of TLPs if the ACK Latency Timer expires, but never later. For a typical system, you do not have to modify the default setting. For more details, see "ACK/NAK Scheduling" in the Databook. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PORT_LINK_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	RSVDP_28 Reserved for future use.

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Bit	Attr	Reset Value	Description
27	RW	0x0	TRANSMIT_LANE_REVERSALE_ENABLE TRANSMIT_LANE_REVERSALE_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
26	RW	0x0	EXTENDED_SYNCH EXTENDED_SYNCH is an internally reserved field. Do not use. Note: This register field is sticky.
25	RW	0x0	CORRUPT_LCRC_ENABLE CORRUPT_LCRC_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
24	RW	0x0	BEACON_ENABLE BEACON_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
23:22	RO	0x0	reserved
21:16	RW	0x01	LINK_CAPABLE Link Mode Enable. Sets the number of lanes in the link that you want to connect to the link partner. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Predetermined Number of Lanes" field of the "Link Width and Speed Change Control Register". For more information, see "How to Tie Off Unused Lanes". For information on upsizing and downsizing the link width, see "Link Establishment". Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
15:12	RO	0x0	RSVDP_12 Reserved for future use.
11:8	RW	0x1	LINK_RATE LINK_RATE is an internally reserved field. Do not use. Note: This register field is sticky.
7	RW	0x0	FAST_LINK_MODE Fast Link Mode. Sets all internal LTSSM millisecond timers to Fast Mode for speeding up simulation. Forces the LTSSM training (link initialization) to use shorter time-outs and to link up faster. - The default scaling factor can be changed using the DEFAULT_FAST_LINK_SCALING_FACTOR parameter or through the FAST_LINK_SCALING_FACTOR field in the TIMER_CTRL_MAX_FUNC_NUM_OFF register. - Fast Link Mode can also be activated by setting the diag_ctrl_bus[2] pin to '1'. For more details, see the "Fast Link Simulation Mode" section in the "Integrating the Controller with the PHY or Application RTL or Verification IP" chapter of the User Guide. Note: This register field is sticky.
6	RW	0x0	LINK_DISABLE LINK_DISABLE is an internally reserved field. Do not use. Note: This register field is sticky.
5	RW	0x1	DLL_LINK_EN DLL Link Enable. Note: This register field is sticky.
4	RO	0x0	RSVDP_4 Reserved for future use.

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Bit	Attr	Reset Value	Description
3	RW	0x0	RESET_ASSERT Reset Assert. Triggers a recovery and forces the LTSSM to the hot reset state (downstream port only). Note: This register field is sticky.
2	RW	0x0	LOOPBACK_ENABLE Loopback Enable. Turns on loopback. For more details, see "Loopback" in the Databook. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
1	RW	0x0	SCRAMBLE_DISABLE Scramble Disable. Turns off data scrambling. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
0	RW	0x0	VENDOR_SPECIFIC_DLLP_REQ Vendor Specific DLLP Request.Reading from this self-clearing register field always returns a '0'.

PCIE_DSP_PF0_PORT_LOGIC_LANE_SKEW_OFF

Address: Operational Base(0xFE000700) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	DISABLE_LANE_TO_LANE_DESKEW Disable Lane-to-Lane Deskew. Causes the controller to disable the internal Lane-to-Lane deskew logic. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
30:27	RW	0x0	IMPLEMENT_NUM_LANES Implementation-specific Number of Lanes. Set the implementation-specific number of lanes. The number of lanes to be used when in Loopback Master. The number of lanes programmed must be equal to or less than the valid number of lanes set in LINK_CAPABLE field. You must configure this field before initiating Loopback by writing in the LOOPBACK_ENABLE field. The controller will transition from Loopback.Entry to Loopback.Active after receiving two consecutive TS1 Ordered Sets with the Loopback bit asserted on the implementation specific number of lanes configured in this field. Note: This register field is sticky.
26	RW	0x0	ELASTIC_BUFFER_MODE Selects Elasticity Buffer operating mode: Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
25	RW	0x0	ACK_NAK_DISABLE Ack/Nak Disable. Prevents the controller from sending ACK and NAK DLLPs. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
24	RW	0x0	FLOW_CTRL_DISABLE Flow Control Disable. Prevents the controller from sending FC DLLPs. Note: This register field is sticky.
23:0	RW	0x000000	INSERT_LANE_SKEW INSERT_LANE_SKEW is an internally reserved field. Do not use. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_TIMER_CTRL_MAX_FUNC_NUM_OFF

Address: Operational Base(0xFE000700) + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30:29	RW	0x0	FAST_LINK_SCALING_FACTOR Fast Link Timer Scaling Factor. Sets the scaling factor of LTSSM timer when FAST_LINK_MODE field in PORT_LINK_CTRL_OFF is set to '1'. Default is set by the hidden configuration parameter DEFAULT_FAST_LINK_SCALING_FACTOR which defaults to '0'. Note: This register field is sticky.
28:24	RW	0x00	UPDATE_FREQ_TIMER UPDATE_FREQ_TIMER is an internally reserved field. Do not use. Note: This register field is sticky.
23:19	RW	0x00	TIMER_MOD_ACK_NAK Ack Latency Timer Modifier. Increases the timer value for the Ack latency timer in increments of 64 clock cycles. A value of '0' represents no modification to the timer value. For more details, see the ROUND_TRIP_LATENCY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. Note: This register field is sticky.
18:14	RW	0x06	TIMER_MOD_REPLAY_TIMER Replay Timer Limit Modifier. Increases the time-out value for the replay timer in increments of 64 clock cycles at Gen1 or Gen2 speed, and in increments of 256 clock cycles at Gen3 speed. A value of '0' represents no modification to the timer limit. For more details, see the REPLAY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. At Gen3 speed, the controller automatically changes the value of this field to DEFAULT_GEN3_REPLAY_ADJ. Note: This register field is sticky.
13:8	RO	0x00	RSVDP_8 Reserved for future use.
7:0	RW	0x00	MAX_FUNC_NUM Maximum function number that can be used in a request. Configuration requests targeted at function numbers above this value are returned with UR (unsupported request). Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_SYMBOL_TIMER_FILTER_1_OFF

Address: Operational Base(0xFE000700) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	MASK_RADM_1 Filter Mask 1. The Filter Mask 1 Register modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" section. In each case, '0' applies the associated filtering rule and '1' masks the associated filtering

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Bit	Attr	Reset Value	Description
			rule. [31]: CX_FLT_MASK_RC_CFG_DISCARD - 0: For RADM RC filter to not allow CFG transaction being received - 1: For RADM RC filter to allow CFG transaction being received [30]: CX_FLT_MASK_RC_IO_DISCARD - 0: For RADM RC filter to not allow IO transaction being received - 1: For RADM RC filter to allow IO transaction being received [29]: CX_FLT_MASK_MSG_DROP - 0: Drop MSG TLP (except for Vendor MSG). Send decoded message on the SII. - 1: Do not Drop MSG (except for Vendor MSG). Send message TLPs to your application on TRGT1 and send decoded message on the SII. - The default for this bit is the inverse of FLT_DROP_MSG. That is, if FLT_DROP_MSG =1, then the default of this bit is '0' (drop message TLPs). This bit only controls message TLPs other than Vendor MSGs. Vendor MSGs are controlled by Filter Mask Register 2, bits [1:0]. The controller never passes ATS Invalidate messages to the SII interface regardless of this filter rule setting. The controller passes all ATS Invalidate messages to TRGT1 (or AXI bridge master), as they are too big for the SII. [28]: CX_FLT_MASK_CPL_ECRC_DISCARD - Only used when completion queue is advertised with infinite credits and is in store-and-forward mode. - 0: Discard completions with ECRC errors - 1: Allow completions with ECRC errors to be passed up - Reserved field for SW. [27]: CX_FLT_MASK_ECRC_DISCARD - 0: Discard TLPs with ECRC errors - 1: Allow TLPs with ECRC errors to be passed up [26]: CX_FLT_MASK_CPL_LEN_MATCH - 0: Enforce length match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err - 1: Mask length match for completions [25]: CX_FLT_MASK_CPL_ATTR_MATCH - 0: Enforce attribute match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask attribute match for completions [24]: CX_FLT_MASK_CPL_TC_MATCH - 0: Enforce Traffic Class match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask Traffic Class match for completions [23]: CX_FLT_MASK_CPL_FUNC_MATCH - 0: Enforce function match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask function match for completions [22]: CX_FLT_MASK_CPL_REQID_MATCH - 0: Enforce Req. Id match for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca

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Bit	Attr	Reset Value	Description
			- 1: Mask Req. Id match for completions [21]: CX_FLT_MASK_CPL_TAGERR_MATCH - 0: Enforce Tag Error Rules for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask Tag Error Rules for completions [20]: CX_FLT_MASK_LOCKED_RD_AS_UR - 0: Treat locked Read TLPs as UR for EP; Supported for RC - 1: Treat locked Read TLPs as Supported for EP; UR for RC [19]: CX_FLT_MASK_CFG_TYPE1_REQ_AS_UR - 0: Treat CFG type1 TLPs as UR for EP; Supported for RC - 1: Treat CFG type1 TLPs as Supported for EP; UR for RC - When CX_SRIOV_ENABLE is set then this bit is set to allow the filter to process Type 1 Config requests if the EP consumes more than one bus number. [18]: CX_FLT_MASK_UR_OUTSIDE_BAR - 0: Treat out-of-bar TLPs as UR - 1: Do not treat out-of-bar TLPs as UR [17]: CX_FLT_MASK_UR_POIS - 0: Treat poisoned request TLPs as UR - 1: Do not treat poisoned request TLPs as UR - The native controller always passes poisoned completions to your application except when you are using the DMA read channel. [16]: CX_FLT_MASK_UR_FUNC_MISMATCH - 0: Treat Function MisMatched TLPs as UR - 1: Do not treat Function MisMatched TLPs as UR Note: This register field is sticky.
15	RW	0x0	DISABLE_FC_WD_TIMER Disable FC Watchdog Timer. Note: This register field is sticky.
14:11	RW	0x0	EIDLE_TIMER EIDLE_TIMER is an internally reserved field. Do not use. Note: This register field is sticky.
10:0	RW	0x140	SKP_INT_VAL SKP Interval Value. The number of symbol times to wait between transmitting SKP ordered sets. The controller waits the number of symbol times in this register plus 1, between transmitting SKP ordered sets. Your application must program this register accordingly. For example, if 1536 were programmed into this register (in a 250 MHz controller), then the controller actually transmits SKP ordered sets once every 1537 symbol times. The value programmed to this register is actually clock ticks and not symbol times. In a 125 MHz controller, programming the value programmed to this register should be scaled down by a factor of 2 (because one clock tick =two symbol times in this case). Note: This value is not used at Gen3 speed; the skip interval is hardcoded to 370 blocks. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_FILTER_MASK_2_OFF

Address: Operational Base(0xFE000700) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MASK_RADM_2 Filter Mask 2. This field modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" in the Databook. In each case, '0' applies the associated filtering rule and '1' masks the associated filtering rule. [31:10]: Reserved [9]: CX_FLT_MASK_CPL_IN_LUT_CHECK - 0: Disable masking of checking if the tag of CPL is registered in LUT - 1: Enable masking of checking if the tag of CPL is registered in LUT [8]: CX_FLT_MASK_POIS_ERROR_REPORTING - 0: Disable masking of error reporting for Poisoned TLPs - 1: Enable masking of error reporting for Poisoned TLPs [7]: CX_FLT_MASK_PRS_DROP - 0: Allow PRS message to pass through - 1: Drop PRS Messages silently - This bit is ignored when the CX_FLT_MASK_MSG_DROP bit in the MASK_RADM_1 field of the SYMBOL_TIMER_FILTER_1_OFF register is set to '1'. [6]: CX_FLT_UNMASK_TD - 0: Disable unmask TD bit if CX_STRIP_ECRC_ENABLE - 1: Enable unmask TD bit if CX_STRIP_ECRC_ENABLE [5]: CX_FLT_UNMASK_UR_POIS_TRGT0 - 0: Disable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination - 1: Enable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination [4]: CX_FLT_MASK_LN_VENMSG1_DROP - 0: Allow LN message to pass through - 1: Drop LN Messages silently [3]: CX_FLT_MASK_HANDLE_FLUSH - 0: Disable controller Filter to handle flush request - 1: Enable controller Filter to handle flush request [2]: CX_FLT_MASK_DABORT_4UCPL - 0: Enable DLLP abort for unexpected completion - 1: Do not enable DLLP abort for unexpected completion [1]: CX_FLT_MASK_VENMSG1_DROP - 0: Vendor MSG Type 1 dropped silently - 1: Vendor MSG Type 1 not dropped [0]: CX_FLT_MASK_VENMSG0_DROP - 0: Vendor MSG Type 0 dropped with UR error reporting - 1: Vendor MSG Type 0 not dropped Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	RSVDP_1 Reserved for future use.

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Bit	Attr	Reset Value	Description
0	RW	0x1	OB_RD_SPLIT_BURST_EN Enable AMBA Multiple Outbound Decomposed NP SubRequests. You should not clear this register unless your application master is requesting an amount of read data greater than Max_Read_Request_Size, and the remote device (or switch) is reordering completions that have different tags. For more details, see "AXI Bridge Ordering" in the AXI chapter of the Databook. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PL_DEBUG0_OFF

Address: Operational Base(0xFE000700) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DEB_REG_0 The value on cxpl_debug_info[31:0].

PCIE_DSP_PF0_PORT_LOGIC_PL_DEBUG1_OFF

Address: Operational Base(0xFE000700) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DEB_REG_1 The value on cxpl_debug_info[63:32].

PCIE_DSP_PF0_PORT_LOGIC_TX_P_FC_CREDIT_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	RSVDP_TX_P_FC_CREDIT_STATUS Reserved for future use.
19:12	RO	0x00	TX_P_HEADER_FC_CREDIT Transmit Posted Header FC Credits. - The posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

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Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_P_DATA_FC_CREDIT Transmit Posted Data FC Credits. - The posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PCIE_DSP_PF0_PORT_LOGIC_TX_NP_FC_CREDIT_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	RSVDP_TX_NP_FC_CREDIT_STATUS Reserved for future use.
19:12	RO	0x00	TX_NP_HEADER_FC_CREDIT Transmit Non-Posted Header FC Credits. - The non-posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].
11:0	RO	0x000	TX_NP_DATA_FC_CREDIT Transmit Non-Posted Data FC Credits. - The non-posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PCIE_DSP_PF0_PORT_LOGIC_TX_CPL_FC_CREDIT_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	RSVDP_TX_CPL_FC_CREDIT_STATUS Reserved for future use.

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Bit	Attr	Reset Value	Description
19:12	RO	0x00	TX_CPL_HEADER_FC_CREDIT Transmit Completion Header FC Credits. - The Completion Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].
11:0	RO	0x000	TX_CPL_DATA_FC_CREDIT Transmit Completion Data FC Credits. - The Completion Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PCIE_DSP_PF0_PORT_LOGIC_QUEUE_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RW	0x0	TIMER_MOD_FLOW_CONTROL_EN FC Latency Timer Override Enable. Note: This register field is sticky.
30:29	RO	0x0	RSVDP_29 Reserved for future use.
28:16	RW	0x0000	TIMER_MOD_FLOW_CONTROL FC Latency Timer Override Value. When you set the "FC Latency Timer Override Enable" in this register, the value in this field will override the FC latency timer value that the controller calculates according to the PCIe specification. For more details, see "Flow Control" in the Databook. Note: This register field is sticky.
15:14	RO	0x0	reserved
13	RO	0x0	RX_SERIALIZATION_Q_NON_EMPTY Receive Serialization Queue Not Empty.
12:4	RO	0x000	RSVDP_4 Reserved for future use.
3	RW	0x0	RX_QUEUE_OVERFLOW Receive Credit Queue Overflow.
2	RO	0x0	RX_QUEUE_NON_EMPTY Receive Credit Queue Not Empty.
1	RO	0x0	TX_RETRY_BUFFER_NE Transmit Retry Buffer Not Empty.

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Bit	Attr	Reset Value	Description
0	RO	0x0	RX_TLP_FC_CREDIT_NON_RETURN Received TLP FC Credits Not Returned.

PCIE_DSP_PF0_PORT_LOGIC_VC_TX_ARBI_1_OFF

Address: Operational Base(0xFE000700) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	WRR_WEIGHT_VC_3 WRR Weight for VC3. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
23:16	RO	0x00	WRR_WEIGHT_VC_2 WRR Weight for VC2. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
15:8	RO	0x00	WRR_WEIGHT_VC_1 WRR Weight for VC1. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
7:0	RO	0x0f	WRR_WEIGHT_VC_0 WRR Weight for VC0. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R

PCIE_DSP_PF0_PORT_LOGIC_VC_TX_ARBI_2_OFF

Address: Operational Base(0xFE000700) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	WRR_WEIGHT_VC_7 WRR Weight for VC7. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
23:16	RO	0x00	WRR_WEIGHT_VC_6 WRR Weight for VC6. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
15:8	RO	0x00	WRR_WEIGHT_VC_5 WRR Weight for VC5. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
7:0	RO	0x00	WRR_WEIGHT_VC_4 WRR Weight for VC4. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R

PCIE_DSP_PF0_PORT_LOGIC_VC0_P_RX_Q_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x0048)

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Bit	Attr	Reset Value	Description
31	RW	0x0	VC_ORDERING_RX_Q VC Ordering for Receive Queues. Determines the VC ordering rule for the receive queues, used only in the segmented-buffer configuration: Note: This register field is sticky.
30	RW	0x1	TLP_TYPE_ORDERING_VC0 TLP Type Ordering for VC0. Determines the TLP type ordering rule for VC0 receive queues, used only in the segmented-buffer configuration: Note: This register field is sticky.
29:28	RW	0x0	RESERVED5 Reserved. Note: This register field is sticky.
27:26	RW	0x1	VC0_P_DATA_SCALE VC0 Scale Posted Data Credits. Note: This register field is sticky.
25:24	RW	0x1	VC0_P_HDR_SCALE VC0 Scale Posted Header Credits. Note: This register field is sticky.
23:21	RW	0x1	VC0_P_TLP_Q_MODE Reserved. Note: This register field is sticky.
20	RW	0x0	RESERVED4 Reserved. Note: This register field is sticky.
19:12	RO	0x17	VC0_P_HEADER_CREDIT VC0 Posted Header Credits. The number of initial posted header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.
11:0	RO	0x038	VC0_P_DATA_CREDIT VC0 Posted Data Credits. The number of initial posted data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_VC0_NP_RX_Q_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RESERVED7 Reserved. Note: This register field is sticky.
27:26	RW	0x1	VC0_NP_DATA_SCALE VC0 Scale Non-Posted Data Credits. Note: This register field is sticky.
25:24	RW	0x1	VC0_NP_HDR_SCALE VC0 Scale Non-Posted Header Credits. Note: This register field is sticky.
23:21	RW	0x1	VC0_NP_TLP_Q_MODE Reserved. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	RESERVED6 Reserved. Note: This register field is sticky.
19:12	RO	0x17	VC0_NP_HEADER_CREDIT VC0 Non-Posted Header Credits. The number of initial non-posted header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.
11:0	RO	0x005	VC0_NP_DATA_CREDIT VC0 Non-Posted Data Credits. The number of initial non-posted data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_VC0_CPL_RX_Q_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RESERVED9 Reserved. Note: This register field is sticky.
27:26	RW	0x1	VC0_CPL_DATA_SCALE VC0 Scale CPL Data Credits. Note: This register field is sticky.
25:24	RW	0x1	VC0_CPL_HDR_SCALE VC0 Scale CPL Header Credits. Note: This register field is sticky.
23:21	RW	0x1	VC0_CPL_TLP_Q_MODE Reserved. Note: This register field is sticky.
20	RW	0x0	RESERVED8 Reserved. Note: This register field is sticky.
19:12	RO	0x00	VC0_CPL_HEADER_CREDIT VC0 Completion Header Credits. The number of initial Completion header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.
11:0	RO	0x000	VC0_CPL_DATA_CREDIT VC0 Completion Data Credits. The number of initial Completion data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_GEN2_CTRL_OFF

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Address: Operational Base(0xFE000700) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	SELECTABLE_DEEMPH_BIT_MUX The selectable deemphasis bit (Symbol 4 bit 6) of the transmitted TS2 Ordered Sets for DSP in Recovery.RcvrCfg state is muxed between the Selectable De-emphasis field in the Link Control 2 register and the value requested by USP in Recovery.RcvrLock state through Tx TS1s from USP. Note: This register field is sticky.
22	RW	0x0	SELECT_DEEMPH_VAR_MUX The select_deemphasis variable for DSP on entry to Recovery.RcvrCfg state is muxed between the Selectable De-emphasis field in the Link Control 2 register and the value requested by the Upstream Port in the eight consecutive TS1 Ordered Sets it received. Note: This register field is sticky.
21	RW	0x0	GEN1_EI_INFERENCE Electrical Idle Inference Mode at Gen1 Rate. Programmable mode to determine inferred electrical idle (EI) in Recovery.Speed or Loopback.Active (as slave) state at Gen1 speed by looking for a '1' value on RxElecIdle instead of looking for a '0' on RxValid. If the PHY fails to deassert the RxValid signal in Recovery.Speed or Loopback.Active (because of corrupted EIOS for example), then EI cannot be inferred successfully in the controller by just detecting the condition RxValid=0. Note: This register field is sticky.
20	RW	0x0	SEL_DEEMPHASIS Used to set the de-emphasis level for upstream ports. This bit selects the level of de-emphasis the link operates at. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
19	RW	0x0	CONFIG_TX_COMP_RX Config Tx Compliance Receive Bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
18	RW	0x0	CONFIG_PHY_TX_CHANGE Config PHY Tx Swing. Controls the PHY transmitter voltage swing level. The controller drives the mac_phy_txswing output from this register bit field. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
17	RW	0x0	DIRECT_SPEED_CHANGE Directed Speed Change.When the speed change occurs, the controller will clear the contents of this field; and a read to this field by your software will return a '0'. To manually initiate the speed change: - Write to LINK_CONTROL2_LINK_STATUS2_REG.PCIE_CAP_TARGET_LINK_SPEED in the local device - Deassert this field - Assert this field If you set the default of this field using the DEFAULT_GEN2_SPEED_CHANGE configuration parameter to '1', then the speed change is initiated automatically after link up, and the controller clears the contents of this field. If you want to prevent this automatic speed change, then write a lower speed value to the Target Link Speed field of the Link Control 2 register (LINK_CONTROL2_LINK_STATUS2_OFF.PCIE_CAP_TARGET_LINK_SPEED) through the DBI before link up. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
16	RW	0x0	AUTO_LANE_FLIP_CTRL_EN Enable Auto flipping of the lanes. You must set the CX_AUTO_LANE_FLIP_CTRL_EN configuration parameter to include the hardware for this feature in the controller. For more details, see the 'Lane Reversal' appendix in the Databook. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
15:13	RW	0x0	PRE_DET_LANE Predetermined Lane for Auto Flip. This field defines which physical lane is connected to logical Lane0 by the flip operation performed in Detect. This field is used to restrict the receiver detect procedure to a particular lane when the default detect and polling procedure performed on all lanes cannot be successful. A notable example of when it is useful to program this field to a value different from the default, is when a lane is asymmetrically broken, that is, it is detected in Detect LTSSM state but it cannot exit Electrical Idle in Polling LTSSM state. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
12:8	RW	0x01	NUM_OF_LANES Predetermined Number of Lanes. Defines the number of lanes which are connected and not bad. Used to limit the effective link width to ignore 'broken" or "unused" lanes that detect a receiver. Indicates the number of lanes to check for exit from Electrical Idle in Polling.Active and L2.Idle. It is possible that the LTSSM might detect a receiver on a bad or broken lane during the Detect Substate. However, it is also possible that such a lane might also fail to exit Electrical Idle and therefore prevent a valid link from being configured. This value is referred to as the "Predetermined Number of Lanes" in section 4.2.6.2.1 of the PCI Express Base Specification. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Link Mode Enable" field of PORT_LINK_CTRL_OFF. The value in this register is normally the same as the encoded value in PORT_LINK_CTRL_OFF. If you find that one of your used lanes is bad then you must reduce the value in this register. For more information, see "How to Tie Off Unused Lanes" in the Databook. For information on upsizing and downsizing the link width, see "Link Establishment" in the Databook. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
7:0	RW	0xff	FAST_TRAINING_SEQ Sets the Number of Fast Training Sequences (N_FTS) that the controller advertises as its N_FTS during Gen2 or Gen3 link training. This value is used to inform the link partner about the PHY's ability to recover synchronization after a low power state. The number should be provided by the PHY vendor. Do not set N_FTS to zero; doing so can cause the LTSSM to go into the recovery state when exiting from L0s. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PHY_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PHY_STATUS PHY Status. Data received directly from the phy_cfg_status bus. These is a GPIO register reflecting the values on the static phy_cfg_status input signals. The usage is left completely to the user and does not in any way influence controller functionality. You can use it for any static sideband status signalling requirements that you have for your PHY. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PHY_CONTROL_OFF

Address: Operational Base(0xFE000700) + offset (0x0114)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PHY_CONTROL PHY Control. Data sent directly to the cfg_phy_control bus. This is a GPIO register driving the values on the static cfg_phy_control output signals, and does not in any way influence controller functionality. It can be used for any static sideband control signaling requirements that you have for your PHY. Usage of this register and the associated GPIO bus is RESERVED when the controller is connected to a Synopsys PHY. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_TRGT_MAP_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	TARGET_MAP_RESERVED_21_31 Reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky)
20:16	RW	0x00	TARGET_MAP_INDEX The number of the PF Function on which the Target Values are set. This register does not respect the Byte Enable setting, any write will affect all register bits.
15:13	RO	0x0	TARGET_MAP_RESERVED_13_15 Reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky)
12:7	RO	0x00	reserved
6	RW	0x1	TARGET_MAP_ROM Target Value for the ROM page of the PF Function selected by the index number. This register does not respect the Byte Enable setting, any write will affect all register bits.
5:0	RW	0x3f	TARGET_MAP_PF Target Values for each BAR on the PF Function selected by the index number. This register does not respect the Byte Enable setting, any write will affect all register bits.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_ADDR_OFF

Address: Operational Base(0xFE000700) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_ADDR Integrated MSI Reception Module Address. System specified address for MSI memory write transaction termination. Within the AXI Bridge, every received Memory Write request is examined to see if it targets the MSI Address that has been specified in this register; and also to see if it satisfies the definition of an MSI interrupt request. When these conditions are satisfied the Memory Write request is marked as an MSI request. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_UPPER_ADDR_OFF

Address: Operational Base(0xFE000700) + offset (0x0124)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_UPPER_ADDR Integrated MSI Reception Module Upper Address. System specified upper address for MSI memory write transaction termination. Allows functions to support a 64-bit MSI address. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_EN_OFF

Address: Operational Base(0xFE000700) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_0_EN MSI Interrupt0 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_MASK_OFF

Address: Operational Base(0xFE000700) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_0_MASK MSI Interrupt0 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_0_STATUS MSI Interrupt0 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_EN_OFF

Address: Operational Base(0xFE000700) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_1_EN MSI Interrupt1 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_MASK_OFF

Address: Operational Base(0xFE000700) + offset (0x0138)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_1_MASK MSI Interrupt1 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_1_STATUS MSI Interrupt1 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_EN_OFF

Address: Operational Base(0xFE000700) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_2_EN MSI Interrupt2 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_MASK_OFF

Address: Operational Base(0xFE000700) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_2_MASK MSI Interrupt2 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_2_STATUS MSI Interrupt2 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_EN_OFF

Address: Operational Base(0xFE000700) + offset (0x014C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_3_EN MSI Interrupt3 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_MASK_OFF

Address: Operational Base(0xFE000700) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_3_MASK MSI Interrupt3 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_3_STATUS MSI Interrupt3 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_EN_OFF

Address: Operational Base(0xFE000700) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_4_EN MSI Interrupt4 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_MASK_OFF

Address: Operational Base(0xFE000700) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_4_MASK MSI Interrupt4 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0160)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_4_STATUS MSI Interrupt4 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_EN_OFF

Address: Operational Base(0xFE000700) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_5_EN MSI Interrupt5 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_MASK_OFF

Address: Operational Base(0xFE000700) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_5_MASK MSI Interrupt5 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_5_STATUS MSI Interrupt5 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_EN_OFF

Address: Operational Base(0xFE000700) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_6_EN MSI Interrupt6 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_MASK_OFF

Address: Operational Base(0xFE000700) + offset (0x0174)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_6_MASK MSI Interrupt6 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_6_STATUS MSI Interrupt6 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_EN_OFF

Address: Operational Base(0xFE000700) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_7_EN MSI Interrupt7 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_MASK_OFF

Address: Operational Base(0xFE000700) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_7_MASK MSI Interrupt7 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_7_STATUS MSI Interrupt7 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_GPIO_IO_OFF

Address: Operational Base(0xFE000700) + offset (0x0188)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_GPIO_REG MSI GPIO Register. The contents of this register drive the top-level GPIO msi_ctrl_io[31:0]. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_CLOCK_GATING_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	RSVDP_2 Reserved for future use.
1	RW	0x1	AXI_CLK_GATING_EN AXI Clock Gating Enable. This register enables the AXI Bridge to autonomously enable and disable the AXI Master clock, the AXI Slave clock and the AXI DBI slave clock. The DWC_pcie_clk_rst.v module provides the gated clock, mstr_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, mstr_aclk_active, is asserted. For the AXI Slave this module provides the gated clock, slv_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, slv_aclk_active, is asserted. If the AXI DBI Slave is enabled (DBI_4SLAVE_POPULATED=1) the module provides the gated clock, dbi_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, dbi_aclk_active, is asserted. The controller de-asserts the clock enable signals when the respective AXI Master/Slave interfaces are idle. Note: This register field is sticky.
0	RW	0x1	RADM_CLK_GATING_EN RADM Clock Gating Enable. This register, if set, enables the RADM to autonomously enable and disable its clock. The DWC_pcie_clk_rst.v module provides the gated clock, radm_clk_g, to the RADM and is enabled when the controllers clock enable signal, en_radm_clk_g, is asserted. The RADM clock is a gated version of the controller clock, core_clk. The controller de-asserts en_radm_clk_g when there is no Rx traffic, Rx queues and pre/post-queue pipelines are empty, RADM completion LUT is empty, and there are no FLR actions pending. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_GEN3_RELATED_OFF

Address: Operational Base(0xFE000700) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	RSVDP_26 Reserved for future use.
25:24	RO	0x0	reserved
23	RW	0x0	GEN3_EQ_INVREQ_EVAL_DIFF_DISABLE Eq InvalidRequest and RxEqEval Different Time Assertion Disable. Disable the assertion of Eq InvalidRequest and RxEqEval at different time. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
22:21	RO	0x0	reserved
20:19	RO	0x0	RSVDP_19 Reserved for future use.

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Bit	Attr	Reset Value	Description
18	RW	0x0	GEN3_DC_BALANCE_DISABLE DC Balance Disable. Disable DC Balance feature. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
17	RW	0x0	GEN3_DLLP_XMT_DELAY_DISABLE DLLP Transmission Delay Disable. Disable delay transmission of DLLPs before equalization. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
16	RW	0x0	GEN3_EQUALIZATION_DISABLE Equalization Disable. Disable equalization feature. This bit cannot be changed once the LTSSM starts link training. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
15:14	RO	0x0	RSVDP_14 Reserved for future use.
13	RW	0x1	RXEQ_RGRDLESS_RXTS When set to '1', the controller as Gen3 EQ master asserts RxEqEval to instruct the PHY to do Rx adaptation and evaluation after a 500ns timeout from a new preset request. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description Note: This register field is sticky.
12	RW	0x0	RXEQ_PH01_EN Rx Equalization Phase 0/Phase 1 Hold Enable. When this bit is set the upstream port holds phase 0 (the downstream port holds phase 1) for 10ms. Holding phase 0 or phase 1 can be used to allow sufficient time for Rx Equalization to be performed by the PHY. This bit is used during Virtex-7 Gen3 equalization. The programmable bits [RXEQ_PH01_EN, EQ_PHASE_2_3] can be used to obtain the following variations of the equalization procedure: Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
11	RW	0x0	EQ_REDO Equalization Redo Disable. Disable autonomous mechanism for requesting to redo the equalization process. The received presets or coefficients mismatch in Recovery.RcvrLock after Recovery EQ phases causes the EQ redo requests. If the EQ redo is infinite or you do not want eq requests and redo, setting this bit to 1 will stop the EQ requests and EQ redo so that the link can go ahead to L0 state for packet trasmissions. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
10	RW	0x0	EQ_EIEOS_CNT Equalization EIEOS Count Reset Disable. Disable requesting reset of EIEOS count during equalization. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
9	RW	0x0	EQ_PHASE_2_3 Equalization Phase 2 and Phase 3 Disable. This applies to downstream ports only. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description Note: This register field is sticky.
8	RW	0x0	DISABLE_SCRAMBLER_GEN_3 Disable Scrambler for Gen3 and Gen4 Data Rate. The Gen3 and Gen4 scrambler/descrambler within the controller needs to be disabled when the scrambling function is implemented outside of the controller (for example within the PHY). Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
7:2	RO	0x00	RSVDP_2 Reserved for future use.
1	RW	0x0	NO_SEED_VALUE_CHANGE If this bit is set to 1, the seed value of LFSR for scrambler at Gen3 rate does not change after LinkUp = 1. This bit takes effect only when CX_AUTO_LANE_FLIP_CTRL_EN is supported. This feature requires both sides of the link support it. Note: this register is shared for Gen3 and Gen4/Gen5 data rates. Note: This register field is sticky.
0	RW	0x1	GEN3_ZRXDC_NONCOMPL Gen3 Receiver Impedance ZRX-DC Not Compliant. Receivers that operate at 8.0 GT/s with an impedance other than the range defined by the ZRX-DC parameter for 2.5 GT/s (40-60 Ohms) must meet additional behavior requirements in the following LTSSM states: Polling, Rx_L0s, L1, L2, and Disabled. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rates. Note: This register field is sticky.

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PCIE_DSP_PF0_PORT_LOGIC_GEN3_EQ_CONTROL_OFF

Address: Operational Base(0xFE000700) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.
26	RW	0x1	GEN3_REQ_SEND_CONSEC_EIEOS_FOR_PSET_MAP Request controller to send back-to-back EIEOS in Recovery.RcvrLock state until presets to coefficients mapping is complete. Note: Gen3 and Gen4 share the same register bit and have the same feature. Note: This register field is sticky.
25	RW	0x0	GEN3_EQ_PSET_REQ_AS_COEF GEN3_EQ_PSET_REQ_AS_COEF is an internally reserved field. Do not use. Note: This register field is sticky.
24	RW	0x0	GEN3_EQ_FOM_INC_INITIAL_EVAL Include Initial FOM. Include or not the FOM feedback from the initial preset evaluation performed in the EQ Master, when finding the highest FOM among all preset evaluations. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
23:8	RW	0x059f	GEN3_EQ_PSET_REQ_VEC Preset Request Vector. Requesting of Presets during the initial part of the EQ Master Phase. Encoding scheme is as follows: Bit [15:0] =0x0: No preset is requested and evaluated in EQ Master Phase. Bit [i] =1: "Preset=i" is requested and evaluated in EQ Master Phase. - 0000000000000000: No preset be requested and evaluated in EQ Master Phase - 000000xxxxxxxxx1: Preset 0 is requested and evaluated in EQ Master Phase - 000000xxxxxxxx1x: Preset 1 is requested and evaluated in EQ Master Phase - 000000xxxxxxx1xx: Preset 2 is requested and evaluated in EQ Master Phase - 000000xxxxxx1xxx: Preset 3 is requested and evaluated in EQ Master Phase - 000000xxxxx1xxxx: Preset 4 is requested and evaluated in EQ Master Phase - 000000xxxx1xxxxx: Preset 5 is requested and evaluated in EQ Master Phase - 000000xxx1xxxxxx: Preset 6 is requested and evaluated in EQ Master Phase - 000000xx1xxxxxxx: Preset 7 is requested and evaluated in EQ Master Phase - 000000x1xxxxxxxx: Preset 8 is requested and evaluated in EQ Master Phase

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Bit	Attr	Reset Value	Description
			- 00000x1xxxxxxxxx: Preset 9 is requested and evaluated in EQ Master Phase - 000001xxxxxxxxxx: Preset 10 is requested and evaluated in EQ Master Phase - All other encodings: Reserved Note: You must contact your PHY vendor to ensure 24 ms timeout does not occur in presets requests in EQ master phase, that is, you must set a proper value to the GEN3_EQ_PSET_REQ_VEC register so that the EQ tunning for Figure of Merit in the EQ master phase completes before 24 ms timeout. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
7	RO	0x0	RSVDP_7 Reserved for future use.
6	RW	0x1	GEN3_LOWER_RATE_EQ_REDO_ENABLE Support EQ redo and lower rate change. Note: Gen3 and Gen4 share the same register bit and have the same feature. Note: This register field is sticky.
5	RW	0x1	GEN3_EQ_EVAL_2MS_DISABLE Phase2_3 2 ms Timeout Disable. Determine behavior in Phase2 for USP (Phase3 if DSP) when the PHY does not respond within 2ms to the assertion of RxEqEval. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
4	RW	0x0	GEN3_EQ_PHASE23_EXIT_MODE Behavior After 24 ms Timeout (when optimal settings are not found). For a USP: Determine next LTSSM state from Phase2 after 24ms Timeout - 0: Recovery.Speed - 1: Recovery.Equalization.Phase3 When optimal settings are not found then: - Equalization Phase 2 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 - Equalization Phase 2 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 - Equalization Phase 2 Complete status bit is set in the "Link

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Bit	Attr	Reset Value	Description
			Status Register 2" For a DSP: Determine next LTSSM state from Phase3 after 24ms Timeout - 0: Recovery.Speed - 1: Recovery.Equalization.RcvrLock When optimal settings are not found then: - Equalization Phase 3 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 - Equalization Phase 3 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 - Equalization Phase 3 Complete status bit is set in the "Link Status Register 2" Note: GEN3_EQ_PHASE23_EXIT_MODE = 1 affects Direction Change feed back mode. EQ requests for Figure Of Merit mode complete before 24 ms timeout. Please see GEN3_EQ_PSET_REQ_VEC Register for more. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
3:0	RW	0x1	GEN3_EQ_FB_MODE Feedback Mode. Other values are reserved. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is a shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF

Address: Operational Base(0xFE000700) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	RSVDP_18 Reserved for future use.
17:14	RW	0x0	GEN3_EQ_FMDC_MAX_POST_CUSROR_DELTA Convergence Window Aperture for C+1. Post-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data

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Bit	Attr	Reset Value	Description
			rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
13:10	RW	0x0	GEN3_EQ_FMDC_MAX_PRE_CUSROR_DELTA Convergence Window Aperture for C-1. Pre-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
9:5	RW	0x02	GEN3_EQ_FMDC_N_EVALS Convergence Window Depth. Number of consecutive evaluations considered in Phase 2/3 when determining if optimal coefficients have been found. Allowed range: 0,1,2,..16 up to a maximum of CX_GEN3_EQ_COEFQ_DEPTH. When set to 0, EQ Master is performed without sending any requests to the remote partner in Phase 2 for USP and Phase 3 for DSP. Therefore, the remote partner will not change its transmitter coefficients and will move to the next state. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
4:0	RW	0x00	GEN3_EQ_FMDC_T_MIN_PHASE23 Minimum Time (in ms) To Remain in EQ Master Phase. The LTSSM stays in EQ Master phase for at least this amount of time, before starting to check for convergence of the coefficients. Allowed values 0,1,...,24. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_ORDER_RULE_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15:8	RW	0x00	CPL_PASS_P Completion Passing Posted Ordering Rule Control. Determines if CPL can pass halted P queue.
7:0	RW	0x00	NP_PASS_P Non-Posted Passing Posted Ordering Rule Control. Determines if NP can pass halted P queue.

PCIE_DSP_PF0_PORT_LOGIC_PIPE_LOOPBACK_CONTROL_OFF

Address: Operational Base(0xFE000700) + offset (0x01B8)

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Bit	Attr	Reset Value	Description
31	RW	0x0	PIPE_LOOPBACK PIPE Loopback Enable. Indicates RMMI Loopback if M-PCIe. Note: This register field is sticky.
30:27	RO	0x0	RSVDP_27 Reserved for future use.
26:24	WO	0x0	RXSTATUS_VALUE RXSTATUS_VALUE is an internally reserved field. Do not use.
23:22	RO	0x0	RSVDP_22 Reserved for future use.
21:16	RW	0x00	RXSTATUS_LANE RXSTATUS_LANE is an internally reserved field. Do not use. Note: This register field is sticky.
15:0	RW	0x0001	LPBK_RXVALID LPBK_RXVALID is an internally reserved field. Do not use. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MISC_CONTROL_1_OFF

Address: Operational Base(0xFE000700) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	RSVDP_23 Reserved for future use.
22	RW	0x0	PORT_LOGIC_WR_DISABLE Disable port logic register write from wire side. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
21	RW	0x0	P2P_ERR_RPT_CTRL Determines whether to enable Peer to Peer (P2P) error reporting. Note: This register field is sticky.
20	RW	0x0	P2P_TRACK_CPL_TO_REG Determines whether to track completion of transmitted Non-Posted TLPs in P2P mode. Note: This register field is sticky.
19:18	RW	0x2	TARGET_ABOVE_CONFIG_LIMIT_REG Configuration requests with an address greater than CONFIG_LIMIT_REG are directed to either ELBI or TRGT1 interface based on the setting of this field. This field can have the following values: Note: This register field is sticky.
17:8	RW	0x3ff	CONFIG_LIMIT_REG Configuration requests are directed either to CDM or ELBI/RTRGT1 based on the value of this field. - Configuration requests with an address less CONFIG_LIMIT_REG are directed to the CDM - Configuration requests with an address greater than CONFIG_LIMIT_REG are directed to either ELBI or TRGT1 interface based on the setting of TARGET_ABOVE_CONFIG_LIMIT_REG field. Your application must set a proper value for this field based on your extended configuration registers. For more details, see the "CDM/ELBI Register Space Access Through CFG Request" in "Register Module, LBC, and DBI" section in the "Controller Operations" chapter of the Databook. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7	RW	0x0	CFG_TLP_BYPASS_EN_REG Setting of this field defines how to decide the destination of Configuration requests. Note: When app_req_retry_en is asserted, the setting of this field is ignored. Note: This register field is sticky.
6	RW	0x1	CPLQ_MNG_EN This field enables the Completion Queue Management feature. Note: This register field is sticky.
5	RW	0x0	ARI_DEVICE_NUMBER When ARI is enabled, this field enables use of the device ID. Note: This register field is sticky.
4	RW	0x0	DISABLE_AUTO_LTR_CLR_MSG Disable the autonomous generation of LTR clear message in upstream port. This field can have the following values: For more details, see "Latency Tolerance Reporting (LTR) Message Generation [EP Mode]" in "Message Generation" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky.
3	RW	0x0	SIMPLIFIED_REPLAY_TIMER Enables Simplified Replay Timer (Gen4). For more details, see "Transmit Replay" in "Transmit TLP Processing" section in the "Controller Operations" chapter of the Databook. Simplified Replay Timer can have the following Values: - A value from 24,000 to 31,000 Symbol Times when Extended Synch is 0b. - A value from 80,000 to 100,000 Symbol Times when Extended Synch is 1b. The Simplified Replay Timer value must not be changed while the link is in use. Note: This register field is sticky.
2	RW	0x0	UR_CA_MASK_4_TRGT1 When this field is set to '1', the controller suppresses error logging, error message generation, and CPL generation for non-posted requests TLPs (with UR filtering status) forwarded to your application (that is, when DEFAULT_TARGET =1). For more details, see "Advanced Error Handling For Received TLPs" chapter of the Databook. Note: This register field is sticky.
1	RW	0x0	DEFAULT_TARGET Default target for an IO or MEM request with UR/CA/CRS received. Based on the value of this field the controller either drops or forwards these requests to your application. For more details, see "ECRC Handling" and "Request TLP Routing Rules" in "Receive Routing" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky.
0	RW	0x0	DBI_RO_WR_EN Write to RO Registers Using DBI. For more details, see "Writing to Read-Only Registers" in "Register Module, LBC, and DBI" section in the "Controller Operations" chapter of the Databook. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MULTI_LANE_CONTROL_OFF

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Address: Operational Base(0xFE000700) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7	RW	0x0	UPCONFIGURE_SUPPORT Upconfigure Support. The controller sends this value as the Link Upconfigure Capability in TS2 Ordered Sets in Configuration.Complete state. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
6	RW	0x0	DIRECT_LINK_WIDTH_CHANGE Directed Link Width Change. - If the upconfigure_capable variable is '1' and the PCIE_CAP_HW_AUTO_WIDTH_DISABLE bit in LINK_CONTROL_LINK_STATUS_REG is '0', the controller starts upconfigure or autonomous width downsizing (to the TARGET_LINK_WIDTH value) in the Configuration state. - If TARGET_LINK_WIDTH value is 0x0, the controller does not start upconfigure or autonomous width downsizing in the Configuration state. The controller self-clears this field when the controller accepts this request. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
5:0	RW	0x00	TARGET_LINK_WIDTH Target Link Width. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_PORT_LOGIC_PHY_INTEROP_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	RSVDP_18 Reserved for future use.
17:12	RW	0x1e	PHY_RST_TIMER Decide how many aux clock cycles the PHY reset lasts (0 to 63 aux clock cycles). Note: This register field is sticky.
11	RO	0x0	reserved
10	RW	0x0	L1_CLK_SEL L1 Clock control bit. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9	RW	0x0	L1_NOWAIT_P1 L1 entry control bit. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
8	RW	0x0	L1SUB_EXIT_MODE L1 Exit Control Using phy_mac_pclkack_n. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. If PCLK as PHY input is selected, you should not write to this field and change the default value since PCLK as PHY input doesn't support any value other than the default. Note: This register field is sticky.
7	RO	0x0	RSVDP_7 Reserved for future use.
6:0	RW	0x01	RXSTANDBY_CONTROL Rxstandby Control. Bits 0..5 determine if the controller asserts the RxStandby signal (mac_phy_rxstandby) in the indicated condition. Bit 6 enables the controller to perform the RxStandby/RxStandbyStatus handshake. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. - [0]: Rx EIOS and subsequent T TX-IDLE-MIN - [1]: Rate Change - [2]: Inactive lane for upconfigure/downconfigure - [3]: PowerDown=P1orP2 - [4]: RxL0s.Idle - [5]: EI Infer in L0 - [6]: Execute RxStandby/RxStandbyStatus Handshake Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_TRGT_CPL_LUT_DELETE_ENTRY_OFF

Address: Operational Base(0xFE000700) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31	WO	0x0	DELETE_EN This is a one-shot bit. This is a self-clearing register field. Reading from this register field always returns a '0'.
30:0	RW	0x00000000	LOOK_UP_ID This number selects one entry to delete of the TRGT_CPL_LUT.

PCIE_DSP_PF0_PORT_LOGIC_LINK_FLUSH_CONTROL_OFF

Address: Operational Base(0xFE000700) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	RSVD_I_8 This is an internally reserved field. Do not use. Note: This register field is sticky.
23:1	RO	0x000000	RSVDP_1 Reserved for future use.

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Bit	Attr	Reset Value	Description
0	RW	0x1	AUTO_FLUSH_EN Enables automatic flushing of pending requests before sending the reset request to the application logic to reset the PCIe controller and the AXI Bridge. The flushing process is initiated if any of the following events occur: - Hot reset request. A downstream port (DSP) can "hot reset" an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. - Warm (Soft) reset request. Generated when exiting from D3 to D0 and cfg_pm_no_soft_rst=0. - Link down reset request. A high to low transition on smlh_req_rst_not indicates the link has gone down and the controller is requesting a reset. If you disable automatic flushing, your application is responsible for resetting the PCIe controller and the AXI Bridge. For more details, see "Warm and Hot Resets" section in the Architecture chapter of the Databook. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AMBA_ERROR_RESPONSE_DEFAULT_OFF

Address: Operational Base(0xFE000700) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15:10	RW	0x27	AMBA_ERROR_RESPONSE_MAP AXI Slave Response Error Map. Allows you to selectively map the errors received from the PCIe completion (for non-posted requests) to the AXI slave responses, slv_rresp or slv_bresp. The recommended setting is SLVERR. CRS is always mapped to OKAY. - [0] -- 0: UR (unsupported request) -> DECERR -- 1: UR (unsupported request) -> SLVERR - [1] -- 0: CRS (configuration retry status) -> DECERR -- 1: CRS (configuration retry status) -> SLVERR - [2] -- 0: CA (completer abort) -> DECERR -- 1: CA (completer abort) -> SLVERR - [3]: RESERVED (0x0) - [4]: RESERVED (0x0) - [5] -- 0: Completion Timeout -> DECERR -- 1: Completion Timeout -> SLVERR. The AXI bridge internally drops (processes internally but not passed to your application) a completion that has been marked by the Rx filter as UC or MLF, and does not pass its status directly down to the slave interface. It waits for a timeout and then signals "Completion Timeout" to the slave interface. The controller sets the AXI slave read databus to 0xFFFF for all error responses. Note: This register field is sticky.
9:5	RO	0x00	RSVDP_5 Reserved for future use.

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	AMBA_ERROR_RESPONSE_CRS CRS Slave Error Response Mapping. Determines the AXI slave response for CRS completions. For more details, see "Error Handling" in the AXI chapter of the Databook. Note: This register field is sticky.
2	RW	0x0	AMBA_ERROR_RESPONSE_VENDORID Vendor ID Non-existent Slave Error Response Mapping. Determines the AXI slave response for errors on reads to non-existent Vendor ID register. For more details, see "Error Handling" in the AXI chapter of the Databook. Note: This register field is sticky.
1	RO	0x0	RSVDP_1 Reserved for future use.
0	RW	0x0	AMBA_ERROR_RESPONSE_GLOBAL Global Slave Error Response Mapping. Determines the AXI slave response for all error scenarios on non-posted requests. For more details, see "Error Handling" in the AXI chapter of the Databook. The error response mapping is not applicable to Non-existent Vendor ID register reads. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AMBA_LINK_TIMEOUT_OFF

Address: Operational Base(0xFE000700) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	RSVDP_9 Reserved for future use.
8	RW	0x0	LINK_TIMEOUT_ENABLE_DEFAULT Disable Flush. Note: This register field is sticky.
7:0	RW	0x32	LINK_TIMEOUT_PERIOD_DEFAULT Timeout Value (ms). The timer will timeout and then flush the bridge TX request queues after this amount of time. The timer counts when there are pending outbound AXI slave interface requests and the PCIe TX link is not transmitting any of these requests. The timer is clocked by core_clk. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AMBA_ORDERING_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7	RW	0x0	AX_MSTR_ZEROLREAD_FW AXI Master Zero Length Read Forward to the application. The DW PCIe controller AXI bridge is able to terminate in order with the Posted transactions the zero length read, implementing the PCIe express flush semantics of the Posted transactions.
6:5	RO	0x0	RSVDP_5 Reserved for future use.

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	AX_MSTR_ORDR_P_EVENT_SEL AXI Master Posted Ordering Event Selector. This field selects how the master interface determines when a P write is completed when enforcing the PCIe ordering rule, "NP must not pass P" at the AXI Master Interface. The AXI protocol does not support ordering between channels. Therefore, NP reads can pass P on your AXI bus fabric. This can result in an ordering violation when the read overtakes a P that is going to the same address. Therefore, the bridge master does not issue any NP requests until all outstanding P writes reach their destination. It does this by waiting for the all of the write responses on the B channel. This can affect the performance of the master read channel. For scenarios where the interconnect serializes the AXI master "AW", "W" and "AR" channels, you can increase the performance by reducing the need to wait until the complete Posted transaction has effectively reached the application slave. Note: This setting will not affect: - MSI interrupt catcher and P data ordering. This is always driven by the B'last event. - DMA read engine TLP ordering. This is always driven by the B'last event. - NP write transactions which are always serialized with P write transactions.
2	RO	0x0	RSVDP_2 Reserved for future use.
1	RW	0x0	AX_SNP_EN AXI Serialize Non-Posted Requests Enable. This field enables the AXI Bridge to serialize same ID Non-Posted Read/Write Requests on the wire. Serialization implies one outstanding same ID NP Read or Write on the wire and used to avoid AXI RAR and WAW hazards at the remote link partner. For more details, see the "Optional Serialization of AXI Slave Non-posted Requests" section in the AXI chapter of the Databook.
0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_1_OFF

Address: Operational Base(0xFE000700) + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_LOW_ADDR Boundary Lower Address For Memory Type. Bits [31:0] of dword-aligned address of the boundary for Memory type. The two lower address LSBs are '00'. Addresses up to but not including this value are in the lower address space region; addresses equal or greater than this value are in the upper address space region. Note: This register field is sticky.
1	RO	0x0	RSVDP_1 Reserved for future use.
0	RW	0x0	CFG_MEMTYPE_VALUE Sets the memory type for the lower and upper parts of the address space: Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_2_OFF

Address: Operational Base(0xFE000700) + offset (0x01E4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_HIGH_ADDR Boundary Upper Address For Memory Type. Bits [63:32] of the 64-bit dword-aligned address of the boundary for Memory type. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_3_OFF

Address: Operational Base(0xFE000700) + offset (0x01E8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	CFG_MSTR_AWCACHE_VALUE Master Write CACHE Signal Value. Value of the individual bits in mstr_awcache when CFG_MSTR_AWCACHE_MODE is '1'. Note: Not applicable to message requests; for message requests the value of mstr_awcache is always '0000'. Note: This register field is sticky.
26:23	RO	0x0	reserved
22:19	RW	0x0	CFG_MSTR_ARCACHE_VALUE Master Read CACHE Signal Value. Value of the individual bits in mstr_arcache when CFG_MSTR_ARCACHE_MODE is '1'. Note: This register field is sticky.
18:15	RO	0x0	reserved
14:11	RW	0x0	CFG_MSTR_AWCACHE_MODE Master Write CACHE Signal Behavior. Defines how the individual bits in mstr_awcache are controlled. Note: for message requests the value of mstr_awcache is always "0000" regardless of the value of this bit. Note: This register field is sticky.
10:7	RO	0x0	reserved
6:3	RW	0x0	CFG_MSTR_ARCACHE_MODE Master Read CACHE Signal Behavior. Defines how the individual bits in mstr_arcache are controlled. Note: This register field is sticky.
2:0	RO	0x0	reserved

PCIE_DSP_PF0_PORT_LOGIC_AXI_MSTR_MSG_ADDR_LOW_OFF

Address: Operational Base(0xFE000700) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	CFG_AXIMSTR_MSG_ADDR_LOW Lower 20-bits of the programmable AXI address for Messages. Note: This register field is sticky.
11:0	RO	0x000	CFG_AXIMSTR_MSG_ADDR_LOW_RESERVED Reserved for future use. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AXI_MSTR_MSG_ADDR_HIGH_OFF

Address: Operational Base(0xFE000700) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_AXIMSTR_MSG_ADDR_HIGH Upper 32 bits of the programmable AXI address for Messages. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PCIE_VERSION_NUMBER_OFF

Address: Operational Base(0xFE000700) + offset (0x01F8)

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Bit	Attr	Reset Value	Description
31:0	RO	0x3536302a	VERSION_NUMBER Version Number.

PCIE_DSP_PF0_PORT_LOGIC_PCIE_VERSION_TYPE_OFF

Address: Operational Base(0xFE000700) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x6c703035	VERSION_TYPE Version Type.

PCIE_DSP_PF0_PORT_LOGIC_PL_APP_BUS_DEV_NUM_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15:8	RO	0x00	RC_DSW_BUS_NUM This field reflects the value of bus number driven on app_bus_num input signal by your application. Note: This register field is sticky.
7:3	RO	0x00	RC_DSW_DEV_NUM This field reflects the value of device number driven on app_device_num input signal by your application. Note: This register field is sticky.
2:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_PORT_LOGIC_PCIPM_TRAFFIC_CTRL_OFF

Address: Operational Base(0xFE000700) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7:4	RO	0x0	PCIPM_RESERVED_4_7 Reserved. Note: This register field is sticky.
3	RW	0x0	PCIPM_NEW_TLP_CLIENT2_BLOCKED This field indicates that all TLPs transmitted by Client 2 interface are blocked during non-D0 states. Note: This register field is sticky.
2	RW	0x0	PCIPM_NEW_TLP_CLIENT1_BLOCKED This field indicates that all TLPs transmitted by Client 1 interface are blocked during non-D0 states. Note: This register field is sticky.
1	RW	0x0	PCIPM_NEW_TLP_CLIENT0_BLOCKED This field indicates that all TLPs transmitted by Client 0 interface are blocked during non-D0 states. Note: This register field is sticky.
0	RW	0x0	PCIPM_VDM_TRAFFIC_BLOCKED This field indicates that VDM Message TLPs are blocked during non-D0 states. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PL_LTR_LATENCY_OFF

Address: Operational Base(0xFE000700) + offset (0x0430)

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Bit	Attr	Reset Value	Description
31	RW	0x0	NO_SNOOP_LATENCY_REQUIRE No Snoop Latency Requirement. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
30:29	RO	0x0	RSVDP_29 Reserved for future use.
28:26	RW	0x0	NO_SNOOP_LATENCY_SCALE No Snoop Latency Scale. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
25:16	RW	0x000	NO_SNOOP_LATENCY_VALUE No Snoop Latency Value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
15	RW	0x0	SNOOP_LATENCY_REQUIRE Snoop Latency Requirement. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
14:13	RO	0x0	RSVDP_13 Reserved for future use.
12:10	RW	0x0	SNOOP_LATENCY_SCALE Snoop Latency Scale. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
9:0	RW	0x000	SNOOP_LATENCY_VALUE Snoop Latency Value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_PORT_LOGIC_AUX_CLK_FREQ_OFF

Address: Operational Base(0xFE000700) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	RSVDP_10 Reserved for future use.
9:0	RW	0x018	AUX_CLK_FREQ The aux_clk frequency in MHz. This value is used to provide a 1 us reference for counting time during low-power states with aux_clk when the PHY has removed the pipe_clk. Frequencies lower than 1 MHz are possible but with a loss of accuracy in the time counted. If the actual frequency (f) of aux_clk does not exactly match the programmed frequency (f_prog), then there is an error in the time counted by the controller that can be expressed in percentage as: err% = (f_prog/f-1)*100. For example if f=2.5 MHz and f_prog=3 MHz, then err% =(3/2.5-1)*100 =20%, meaning that the time counted by the controller on aux_clk will be 20% greater than the time in us programmed in the corresponding time register (for example T_POWER_ON). Note: This register field is sticky.

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PCIE_DSP_PF0_PORT_LOGIC_L1_SUBSTATES_OFF

Address: Operational Base(0xFE000700) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	RSVDP_9 Reserved for future use.
8	RW	0x0	L1SUB_LOW_POWER_CLOCK_SWITCH_MODE If the bit is set to 1'b1 the controller will delay the switching of aux_clk to the slow platform clock until it detects that the link partner has de-asserted CLKREQ#. Note: This register field is sticky.
7:6	RW	0x3	L1SUB_T_PCLKACK Max delay (in 1us units) between a MAC request to remove the clock on mac_phy_pclkreq_n and a PHY response on phy_mac_pclkack_n. If the PHY does not respond within this time the request is aborted. Range is 1..4 Note: This register field is sticky.
5:2	RW	0x4	L1SUB_T_L1_2 Duration (in 1us units) of L1.2. Range is 1..16. Note: This register field is sticky.
1:0	RW	0x2	L1SUB_T_POWER_OFF Duration (in 1us units) of L1.2.Entry. Range is 1..4. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_POWERDOWN_CTRL_STATUS_OFF

Address: Operational Base(0xFE000700) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	RSVDP_12 Reserved for future use.
11:8	RO	0x2	POWERDOWN_PHY_POWERDOWN This field represents the Powerdown value that has been acknowledged by the PHY. It is updated with the value of Powerdown driven by the controller, when the PHY has returned the Phystatus acknowledgment for the Powerdown transition.
7:4	RO	0x2	POWERDOWN_MAC_POWERDOWN This field represents the Powerdown value driven by the controller to the PHY.
3:2	RO	0x0	RSVDP_2 Reserved for future use.
1	RW	0x0	POWERDOWN_VMAIN_ACK Set this bit to 1 if you do not want to perform the handshake with the power-switch after PERST# assertion. By default the controller will perform the handshake with the power-switch if L1 power gating is enabled Note: This register field is sticky.
0	WO	0x0	POWERDOWN_FORCE This field is a one shot field. This field could be used for debug purposes in event that the P2 Powerdown transition does not complete. It will allow the controller to proceed with the transition to the P1 Powerdown state. This field always reads back as 1'b0.

PCIE_DSP_PF0_PORT_LOGIC_PIPE_RELATED_OFF

Address: Operational Base(0xFE000700) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	RSVDP_9 Reserved for future use.

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Bit	Attr	Reset Value	Description
8	RW	0x0	PIPE_GARBAGE_DATA_MODE PIPE Garbage Data Mode. - RxValid is deasserted - a valid RxStartBlock is received at 128b/130b encoding - a valid COM symbol is received at 8b/10b encoding Note: This register field is sticky.
7:0	RO	0x00	reserved

7.4.3.11 PCIE_DSP_PF0_PCIE_CAP_DBI2

7.4.3.11.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PCIE_CAP_DBI2_SHADOW_LINK_CAPABILITIES_REG	0x000C	W	0x0073EC13	This is a 7-bit register at the same address as LINK_CAPABILITIES_REG, and it only exists when one or more of the following expressions are true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCYThe register has only two fields in RTL. All of the other fields here do not exist in RTL and accesses to them are redirected to the corresponding fields in the parent register (LINK_CAPABILITIES_REG).They are modeled here to make the shadow register (model) 32 bits wide which is a tool requirement.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.11.2 Detail Registers Description

PCIE_DSP_PF0_PCIE_CAP_DBI2_SHADOW_LINK_CAPABILITIES_REG

Address: Operational Base(0xFE100070) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	PCIE_CAP_PORT_NUM Shadow Port Number. This field indicates the PCI Express Port number for the given PCI Express Link. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RO	0x1	PCIE_CAP_ASPM_OPT_COMPLIANCE Shadow ASPM Optionality Compliance. This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification

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Bit	Attr	Reset Value	Description
			will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
21	RO	0x1	PCIE_CAP_LINK_BW_NOT_CAP Shadow Link Bandwidth Notification Capable. A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This capability is required for all Root Ports and Switch Downstream Ports supporting Links wider than x1 and/or multiple Link speeds. This field is not applicable and is Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
20	RO	0x1	PCIE_CAP_DLL_ACTIVE_REP_CAP Shadow Data Link Layer Link Active Reporting Capable. For a Downstream Port, the controller hardwires this bit to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable bit of the Slot Capabilities register) or a Downstream Port that supports Link speeds greater than 5.0 GT/s, the controller hardwires this bit to 1b. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b.
19	RO	0x0	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP Shadow Surprise Down Error Reporting Capable. For a Downstream Port, this bit must be set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Note: This register field is sticky.
18	RO	0x0	PCIE_CAP_CLOCK_POWER_MAN Shadow Clock Power Management. For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a Multi-Function device associated with an Upstream Port, each Function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the Multi-Function device indicate

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Bit	Attr	Reset Value	Description
			a 1b in this bit. For ARI Devices, all Functions must indicate the same value in this bit. For Downstream Ports, the controller hardwires this bit to 0b. Note: This register field is sticky.
17:15	RO	0x7	SHADOW_PCIE_CAP_L1_EXIT_LATENCY Shadow L1 Exit Latency. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R - Dbi2: R/W
14:12	RO	0x6	SHADOW_PCIE_CAP_L0S_EXIT_LATENCY Shadow L0s Exit Latency. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access.

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Bit	Attr	Reset Value	Description
			- Dbi: R - Dbi2: R/W
11:10	RO	0x3	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT Shadow Level of ASPM (Active State Power Management) Support. This field indicates the level of ASPM supported on the given PCI Express Link. For more details on ASPM support requirements, see section 5.4.1 of PCI Express Base Specification. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
9:4	RO	0x01	PCIE_CAP_MAX_LINK_WIDTH Shadow Maximum Link Width. This field indicates the maximum Link width (xN - corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. All encodings other than the defined encodings are reserved. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
3:0	RO	0x3	PCIE_CAP_MAX_LINK_SPEED Shadow Maximum Link Speed. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. All encodings other than the defined encodings are reserved. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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7.4.3.12 PCIE_DSP_PF0_MSIX_CAP_DBI2

7.4.3.12.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x00000000	This is the shadow register of the MSI-X Capability ID, Next Pointer, and Control Register.
PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_MSIX_TABLE_OFFSET_REG	0x0004	W	0x00000000	This register provides Table BIR and MSI-x Table offset select.
PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_MSIX_PBA_OFFSET_REG	0x0008	W	0x00000010	This register provides PBA Offset and PBA BIR value.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.12.2 Detail Registers Description

PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG

Address: Operational Base(0xFE1000B0) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	PCI_MSIX_RESERVED1 reserved field 1 in the shadow register. Note: This register field is sticky.
26:16	RO	0x000	PCI_MSIX_TABLE_SIZE MSI-X Table Size in the shadow register. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
15:0	RO	0x0000	PCI_MSIX_RESERVED0 reserved field 0 in the shadow register. Note: This register field is sticky.

PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_MSIX_TABLE_OFFSET_REG

Address: Operational Base(0xFE1000B0) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	PCI_MSIX_TABLE_OFFSET MSI-X Table Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky.
2:0	RO	0x0	PCI_MSIX_BIR MSI-X Table BAR Indicator Register Field. This field indicates which one of a Function's Base Address Registers, located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X Table into Memory Space. All encodings other than the defined encodings are reserved.

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Bit	Attr	Reset Value	Description
			For a 64-bit Base Address Register, the Table BIR indicates the lower DWORD. For Functions with Type 1 Configuration Space headers, BIR values 2 through 5 are also Reserved. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_MSIX_PBA_OFFSET_REG

Address: Operational Base(0xFE1000B0) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000002	PCI_MSIX_PBA_OFFSET MSI-X PBA Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky.
2:0	RO	0x0	PCI_MSIX_PBA_BIR MSI-X PBA BIR. This field indicates which one of a Function's Base Address Registers, located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the Table BIR. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky.

7.4.3.13 PCIE_DSP_PF0_ATU_CAP

7.4.3.13.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_0	0x0000	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_0	0x0004	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_0	0x0008	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_0	0x000C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_0	0x0010	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_0	0x0014	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_0	0x0018	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_0	0x0020	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_0	0x0100	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_0	0x0104	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_0	0x0108	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_0	0x010C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_0	0x0110	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_0	0x0114	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_0	0x0118	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_0	0x0120	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_1	0x0200	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_1	0x0204	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_1	0x0208	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_1	0x020C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_1	0x0210	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_1	0x0214	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_1	0x0218	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_1	0x0220	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_1	0x0300	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_1	0x0304	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_1	0x0308	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_1	0x030C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_1	0x0310	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_1	0x0314	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_1	0x0318	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_1	0x0320	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_2	0x0400	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_2	0x0404	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_2	0x0408	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_2	0x040C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_2	0x0410	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_2	0x0414	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_2	0x0418	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_2	0x0420	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_2	0x0500	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_2	0x0504	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_2	0x0508	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_2	0x050C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_2	0x0510	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_2	0x0514	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_2	0x0518	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_2	0x0520	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_3	0x0600	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_3	0x0604	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_3	0x0608	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_3	0x060C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_3	0x0610	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_3	0x0614	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_3	0x0618	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_3	0x0620	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_3	0x0700	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_3	0x0704	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_3	0x0708	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_3	0x070C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_3	0x0710	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_3	0x0714	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_3	0x0718	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_3	0x0720	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_4	0x0800	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_4	0x0804	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_4	0x0808	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_4	0x080C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_4	0x0810	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_4	0x0814	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_4	0x0818	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_4	0x0820	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_4	0x0900	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_4	0x0904	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_4	0x0908	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_4	0x090C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_4	0x0910	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_4	0x0914	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_4	0x0918	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_4	0x0920	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_5	0x0A00	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_5	0x0A04	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_5	0x0A08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_5	0x0A0C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_5	0x0A10	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_5	0x0A14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_5	0x0A18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_5	0x0A20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_5	0x0B00	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_5	0x0B04	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_5	0x0B08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_5	0x0B0C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_5	0x0B10	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_5	0x0B14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_5	0x0B18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_5	0x0B20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_6	0x0C00	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_6	0x0C04	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_6	0x0C08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_6	0x0C0C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_6	0x0C10	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_6	0x0C14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_6	0x0C18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_6	0x0C20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_6	0x0D00	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_6	0x0D04	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_6	0x0D08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_6	0x0D0C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_6	0x0D10	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_6	0x0D14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_6	0x0D18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_6	0x0D20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_7	0x0E00	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_7	0x0E04	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_7	0x0E08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_7	0x0E0C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_7	0x0E10	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_7	0x0E14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_7	0x0E18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_7	0x0E20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_7	0x0F00	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_7	0x0F04	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_7	0x0F08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_7	0x0F0C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_7	0x0F10	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_7	0x0F14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_7	0x0F18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_7	0x0F20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3.13.2 Detail Registers Description

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are defined as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0xFE300000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

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PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

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PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_0

Address: Operational Base(0xFE300000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated.

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Bit	Attr	Reset Value	Description
			Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_0

Address: Operational Base(0xFE300000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0200)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration

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Bit	Attr	Reset Value	Description
			space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are defined as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0xFE300000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_1

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Address: Operational Base(0xFE300000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.

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Bit	Attr	Reset Value	Description
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

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PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_1

Address: Operational Base(0xFE300000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

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PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_1

Address: Operational Base(0xFE300000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are defined as above. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1.

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Bit	Attr	Reset Value	Description
			Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0xFE300000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0414)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as

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Bit	Attr	Reset Value	Description
			address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_2

Address: Operational Base(0xFE300000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0510)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0514)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0518)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_2

Address: Operational Base(0xFE300000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are defined as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in

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Bit	Attr	Reset Value	Description
			IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0xFE300000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.

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Bit	Attr	Reset Value	Description
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

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PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_3

Address: Operational Base(0xFE300000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated.

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Bit	Attr	Reset Value	Description
			Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0714)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0718)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_3

Address: Operational Base(0xFE300000) + offset (0x0720)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0800)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration

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Bit	Attr	Reset Value	Description
			space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are defined as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0xFE300000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_4

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Address: Operational Base(0xFE300000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.

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Bit	Attr	Reset Value	Description
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0900)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0904)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0908)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

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PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_4

Address: Operational Base(0xFE300000) + offset (0x090C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0910)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated.

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Bit	Attr	Reset Value	Description
			Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0914)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0918)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_4

Address: Operational Base(0xFE300000) + offset (0x0920)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0A00)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration

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Bit	Attr	Reset Value	Description
			space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_5

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Address: Operational Base(0xFE300000) + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0A14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0A20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.

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Bit	Attr	Reset Value	Description
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0B04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

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PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated.

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Bit	Attr	Reset Value	Description
			Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_5

Address: Operational Base(0xFE300000) + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0C00)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration

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Bit	Attr	Reset Value	Description
			space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are defined as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD.

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Bit	Attr	Reset Value	Description
			Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0C18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'

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Bit	Attr	Reset Value	Description
			Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

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PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated.

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Bit	Attr	Reset Value	Description
			Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_6

Address: Operational Base(0xFE300000) + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0E00)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0E04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration

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Bit	Attr	Reset Value	Description
			space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are defined as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_7

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Address: Operational Base(0xFE300000) + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0E14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.

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Bit	Attr	Reset Value	Description
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0F04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

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PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: 0000b: 0 (Default; legacy Single Address Location mode) 0001b: 4 0010b: 8 0011b: 16 0100b: 32 0101b: 64 0110b: 128 0111b: 256 1000b: 512 1001b: 1024 1010b: 2048 1011b: 4096 1100b: 8192 1101b: rsvd. 1110b: rsvd. 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated.

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Bit	Attr	Reset Value	Description
			Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_7

Address: Operational Base(0xFE300000) + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

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7.5 Interface Description

Table 7-3 PCIe IO Usage Model

Signal name	Direction	IO Attribute
WAKEN	I/O	Open Drain, pull up
PERSTN	I/O	pull down
BUTTONRSTN	I	pull down
CLKREQN	I/O	Open Drain, pull up

Table 7-4 PCIe 2 RC G2 Interface Description

Module Pin	Dir	Group	Pin Name	IOMUX Setting
pcie_perst_n	I	M0	I2C2_SCL_M0/PCIE20_PERSTN_M0/GPIO0_B5_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_H[7:4] = 4'h2
		M1	I2S0_SDO3_M0/I2S0_SDI1_M0/PDM_SDI1_M0/PCIE20_PERSTN_M1/GPIO3_B0_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_L[3:0] = 4'h4
pcie_wake_in/out	I/O	M0	I2C2_SDA_M0/PCIE20_WAKEN_M0/GPIO0_B6_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_H[11:8] = 4'h2
		M1	I2S0_SDO2_M0/I2S0_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEN_M1/UART5_RX_M1/GPIO3_A7_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_H[15:12] = 4'h4
pcie_button_n	I	M0	CLK_32K_IN/CLK0_32K_OUT/PCIE20_BUTTONRSTN/GPIO0_B0_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_L[3:0] = 4'h3
pcie_clkreq_in/out_n	I/O	M0	PCIE20_CLKREQN_M0/GPIO0_A6_d	GPIO0_IOC_GPIO0A_IOMUX_SEL_H[11:8] = 4'h1
		M1	I2S0_SDO1_M0/I2S0_SDI3_M0/PDM_CLK0_M0/PCIE20_CLKREQN_M1/UART5_TX_M1/GPIO3_A6_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_H[11:8] = 4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

7.6 Application Notes

7.6.1 Clock and Reset

7.6.1.1 Clock Overview

The PCIe module uses multiple clock domains, it consists of system bus clocks (APB and AXI), Core function clock, PIPE interface clock, Power management clock, and PCIe PHY reference clock.

Table 7-5 Clock Overview

Clock Name	Note
pclk/core_clk/pipe_clk	PIPE and Core clock from PHY PLL generated
mstr_aclk	AXI master clock
slv_aclk	AXI slave clock
dbi_aclk	DBI AXI slave clock
aux_clk	Low power clock(24MHz)
apb_clk	APB slave clock for Client

The system bus clock is generated from SOC main PLL internally, please refer to the relative CRU for details. System bus clock gating is handled automatically by PCIe controller

Core function clock is derived from the PIPE interface clock output from the PCIe PHY. In specific low power state, core function clock is gated and switch to Power management clock automatically. After power up, if the PHY is not ready(phystatus is not de-assert), accessing the core through AXI slave will be held until it is ready.

The PHY TX PLL generates PIPE interface clock from the platform reference clock. The PCIe link Training and transaction is completely dependent upon availability of this clock.

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Application should not initiate transactions before ensuring that the PHY PLL is locked.
The Power management clock which should be fixed with 24MHz driven by crystal input clock. The PCIe controller uses this clock for counting time during L1 substates. You must program the frequency of this clock into the L1_SUBSTATES_OFF register with a value of 24MHz to count real time.
Many PCIe connections, especially backplane connections, require a synchronous reference clock between the two link partners. To achieve this a common clock source, referred to as REFCLK in the PCI Express Card Electromechanical Specification, should be used by both ends of the PCIe link.

7.6.1.2 PCIe PHY Reference Clock

The PHY usually use the external dedicated 100M differential clock as reference clock, the clock should be compatible with the CEM specification.
For low BOM cost usage, In RC mode, PCIe PHY can use internal single-ended clock which can be configured to 24Mhz(Combo PHY), 100Mhz(Combo PHY). Meanwhile, In Combo PHY mode, PCIe PHY can provide differential clock output for system application. The source of differential clock output can be select from internal single-ended clock or PHY TX PLL.

7.6.1.3 Reset Overview

7.6.1.3.1 Power-On Reset

The power-on reset is used as Cold reset of the PCIe. The entire module is reset when power-on reset is asserted and generate a phy_rst_n to reset the PHY link. After de-assertion of the power-on reset, the PCIe PHY and PCIe Core function reset keeps until the software release. Software should finish PCIe PHY initialization before de-asserting the power-on reset. The power-on reset is controlled by CRU, the power-on reset is keep asserted until the software de-assert the reset request.

7.6.1.3.2 System reset

The PCIe Controller has the following distinct resets, all of these are configurable through software driver. This section describes the function of each of the reset inputs.

- button_rst_n: Button reset from board if related IO has been used. section for more information. This reset has an equal functionality with power-on reset.
- perst_n: This reset works as Warm Reset of PCIe if related IO has been used. Please refer to 错误!未找到引用源。 section for more information.
- core_rst_n: This is the main reset for the PCIe Controller. It resets all the logic in the core running in the CORE_CLK(partial of PCLK) domain, except for the PMC module. It keeps reset with power-up reset by default. It also should be asserted when Hot Reset or link down reset occurs, but Application software can delay core_rst_n been asserted until system is ready to do core reset. This delayed reset operation will be discussed in next section.
- AXI Reset: All three AXI interface has its own reset input: mstr_aresetn, slv_aresetn, dbi_resetn. Each resets all logic in the specific AXI clock domain. Typically, these resets are be asserted whenever core_rst_n is asserted. Application software shall have the knowledge of choosing an appropriate time to drive this reset to avoid times when a transaction is in flight.
- non_sticky_rst_n: Resets all non-sticky bit registers in the configuration register space.
- sticky_rst_n : Resets all sticky bit registers in the configuration register space.
- pwr_rst_n: Resets the PMC module and resets all registers in the PM clock domain, including sticky bits. It is the power-on reset.
- phy_rst_n: output reset signal to reset the PCIe PHY. This reset asserted along with Cold Reset, Warm Reset, Hot Reset.

7.6.1.3.3 Hot Reset and Link-Down Reset

A downstream port (DSP) can hot reset an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. Eventually, the DSP and USP assert link_req_rst_not to request external logic to reset them. Alternatively, during normal operation, the link might fail and go down. After this link-down event, the controller requests the reset module to hot-reset the controller. There is no difference in the handling of a link-down reset or a hot reset.
Hot Reset or Link-down reset cannot be activated before no transaction is appending on system bus. Application software must confirm that system bus is in IDLE state then let the

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reset operation go on.
To prevent your application from hanging when the controller is reset, the controller must cleanly terminate all transactions that are still in-progress. In AXI configurations with a segmented-buffer Rx queue architecture, the controller automatically executes this process before asserting link_req_rst_not. To disable automatic flushing, set the AUTO_FLUSH_EN field in LINK_FLUSH_CONTROL_OFF to '0'.

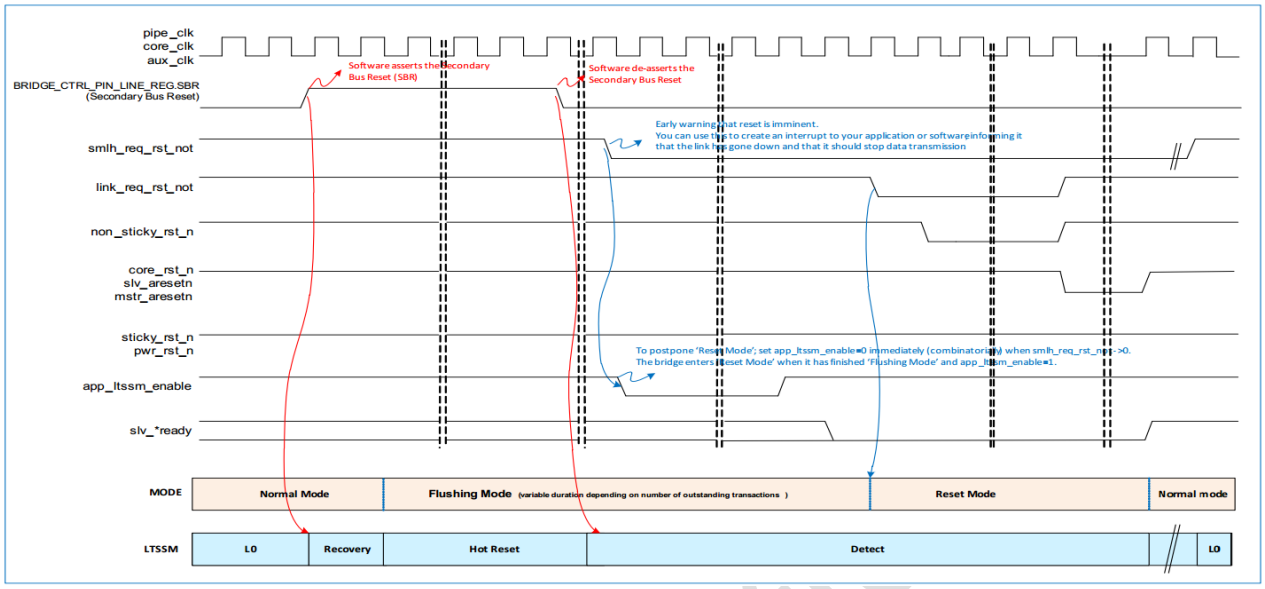

Fig. 7-3 Delaying the PCIe Hot Reset

Figure above illustrates the timing of handling Hot Reset. When Hot Reset or Link-down reset occurs, controller will assert smlh_req_rst_not as an early warning. This warning is an interrupt bit in Client Register group(link_req_rst_not_int). If you want to delay the reset of the controller so that it continues to accept and terminate slave requests, or to read out some register status through the DBI, you must set app_ltssm_enable =0 immediately (combinatorially) after smlh_req_rst_not ->0, as shown in above, this can be achieved by enable the app_dly1_en, app_ltssm_enable will be de-asserted immediately to disable the LTSSM. Then the Hot Reset process is holding on, software then should set the PCIe BIU in IDLE state. This delay will be end-up by asserting app_dly1_done.

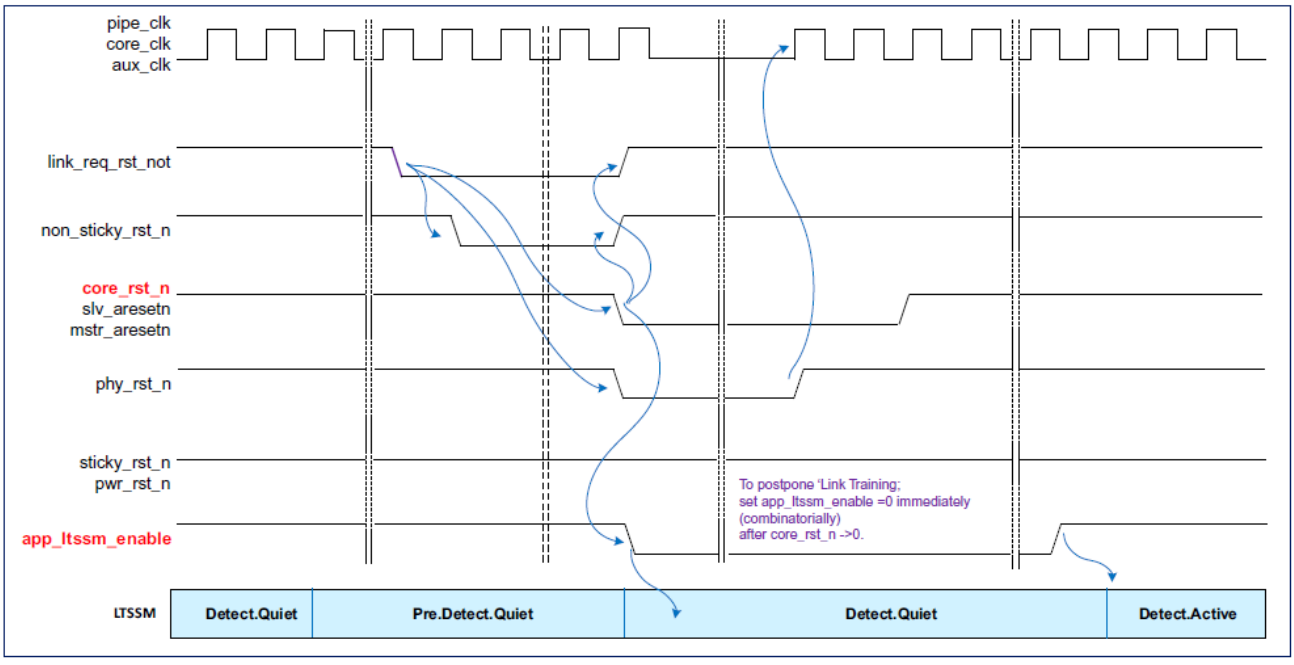

Fig. 7-4 Delaying the Link Training After Hot Reset

If you want to delay link re-establishment (after reset) so that you can reprogram some registers through DBI, you must set app_ltssm_enable =0 immediately after core_rst_n as shown in above. This can be achieved by enable the app_dly2_en, and end-up the delay by assert app_dly2_done.

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To be compatible with old version client design, the app_ltssm_enable_enhance is a new way to control the glue behavior of the app_ltssm_enable. It's advised set app_ltssm_enable_enhance to "1" when the version >= 0x50600. The mechanisms of delaying the Hot reset are available only in app_ltssm_enable_enhance mode.

7.6.2 Initialization

7.6.2.1 Initialization Sequence for RC Mode

The initialization sequence for RC mode is as follows:

1. Configure the IO for CLKREQ# and WAKE# signals. Configure the optional signals button_rst_n and perst_n if they are used. Please refer to section 错误!未找到引用源。 for details.
2. De-assert the PCIe 3.0 PHY PMA output clamp(pcie30_clamp_n) if PCIe 3.0 PHY used.
3. If want to change the default pcie30_phy_mode or other critical configurations that need to be followed by phy_reset, please assert pcie30_phy_resetn
4. Configure the CRU registers to provide appropriate reference clock to PCIe PHY if internal reference used. Check all the CRU control registers, such as PLL/DIV/CKG(clock gating), to make sure the reference and other clock is working normally. Please refer to CRU Chapter for more information.
5. Configure Combo PIPE PHY or PCIe 3.0 PHY General Register File, to set PHY working mode, control the unused PIPE signals and initialize the PHY, the source of the reference or output the differential reference clock.
6. De-assert the PCIe 3.0 pcie30_phy_resetn if necessary
7. Sometimes, it is also necessary to configure the PHY internal register to adjust some analog trim.
8. De-assert the power-up reset of PCIe Controller. Delay some time or wait PLL lock if the PLL lock flag is accessible.
9. Set the app_ltssm_enable_enhance to enable enhance control mode of app_ltssm_enable
10. Initialize the device_type as Root Complex. You can program Client and controller registers before Link training start if necessary. Link training can be initialed by setting ltssm_enable bit in register PCIE_CLIENT_GENERAL_CON to 1. Link training success will set phy_link_up_int to 1. And if data flow initialization success, dll_link_up_int interrupt status bit will be set to 1. These two bits can be polled in LTSSM_STATUS or GENERAL_DEBUG_INFO, besides, it can be informed by interrupt optionally. The controller tries to linkup at maximum Link width/speed, if you want to resize or change speed, please refer to internal application document about speed changing and lane resizing. It is strongly recommended that set direct_speed_change bit to 1 in PL_GEN2_CTRL_OFF before link training.
11. Software emulation and initialization.
12. Writes to Bus Master Enable (BME), Memory Space Enable (MSE), then application can start application traffic generation.

7.6.2.2 Tie Off Unused Lanes

N/A

It is automatically implemented by hardware.

7.6.3 Address Translation

The controller uses the internal Address Translation Unit(iATU) to implement a local address translation scheme that replaces the TLP address and TLP header fields in the current TLP request header.

The iAUT has several inbound Address Translation regions and several outbound Address Translation regions. The minimum size of an Address Translation Region is 64k and the maximum size of an Address Translation Region is 4G.

7.6.3.1 Outbound Features

Address translation is used for mapping different address ranges to different memory spaces supported by your application. A typical example maps your application memory space to PCI memory space. The ATU also supports type translation. Without address translation, your application address is passed unmodified to the TLPs directly through the Tx application interface. You can program the iATU to implement your own outbound address translation scheme. The outbound features are as follows:

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- Address Match mode operation for MEM and I/O, CFG, and MSG TLPs. No translation for completions.
- Supports type translation through TLP type header field replacement for MEM or I/O types to MSG/CFG types.
- Programmable TLP header field replacement. Including TYPE, TC, AT, ATTR, MSG-Code, TH, PH, ST.
- Multiple (up to 16) address regions programmable for location and size.
- Programmable enable/disable per region.
- Automatic FMT field translation between three DWORDs and four DWORDs for 64-bit addresses.
- Invert Address Matching mode to translate accesses outside of a successful address match.
- Configuration Shift mode. Optimizes the memory footprint of CFG accesses destined for the Rx application interface in a multifunction device.
- Response code which defines the completion status to return for accesses matching a region.
- Supports regions from 64 KB to 4 GB in size.
- Payload Inhibit marks all TLPs as having no payload data.
- Header Substitution replaces bytes 8 to 11 (for 3 DWORD header) or bytes 12 to 15 (for 4 DWORD header), inclusive, of the outbound TLP header.
- Tag Substitution of the outbound TLP tag field.
- Function number bypass mode to allow function number information to be supplied from your application transmit interface while translating the address and other attributes of the TLP.
- DMA bypass mode to allow TLPs which are initiated by the embedded DMA engine, to pass through the iATU untranslated.

7.6.3.2 Outbound Basic Operation

The address field of each request MEM and I/O TLP is checked to see if it falls into any of the enabled address regions defined by the Start and End addresses as defined in the figure below. When an address match is found, then the TLP address field is modified as follows:

Translated Address = Original Address - Base Address + Target Address

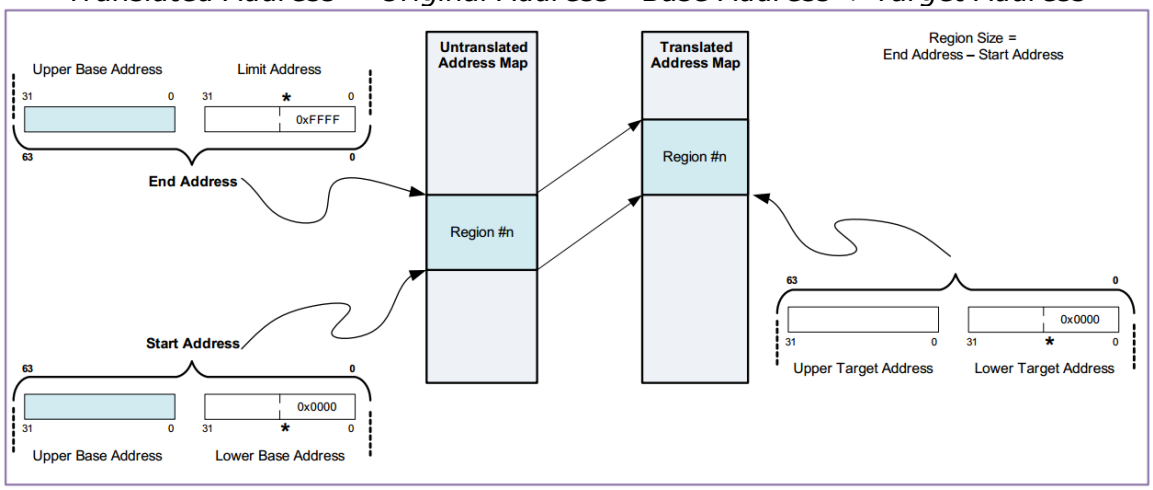

Fig. 7-5 PCIe Hot Reset Control Structure

The TYPE, TC, AT, TH, PH, ST, Function Number, and ATTR header fields are replaced with the corresponding fields in the IATU_REGION_CTRL_1_OFF_OUTBOUND_0 register. When your application address field matches more than one of the CX_ATU_NUM_OUTBOUND_REGIONS address regions, then the first (from lowest number 0) enabled region to be matched is used. For details on what happens when there is no address match, see “No Address Match Result”. This operational mode (called Address Match Mode) is always used for outbound translation.

The minimum size of an address translation region is 64KB. So, the lower 16 bits of the Base, Limit, and Target registers are zero and all address regions are aligned on 64 KB boundaries.

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7.6.3.3 Outbound Detailed Operation

7.6.3.3.1 RID BDF Number Replacement

When there is a successful address match on an outbound TLP, then the function number used in generating the function part of the requester ID field of the TLP is taken from the 3-bit Function Number field of the IATU_REGION_CTRL_1_OFF_OUTBOUND_iregister. The value in this field must be 0x0 unless multifunction operation in the controller is enabled. To override this behavior, use the "Function Number Translation Bypass Feature" described later.

7.6.3.3.2 iATU Outbound MSG Handling

The iATU supports TYPE translation/conversion of MEM and I/O TLPs to Msg/MsgD TLPs. This supports applications that are unable to directly generate Msg/MsgD TLPs. When there is a successful address match on an outbound MEM TLP, and the translated TLP type field is MSG (that is, the type field of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i register is 10xxx), then the message code field of the TLP is set to the value in the Message Code field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_iregister.A Memory Write with an effective length of '0' is converted to Msg and all other MWr TLPs are converted to MsgD.

7.6.3.3.3 MEM-CFG Type Translation

The iATU supports translation of I/O and MEM TLPs to CFG TLPs. This is useful for applications that are unable to generate CFG TLPs. The 16-bit BDF is located at bits [31:16] of the translated address where:

Translated Address = Original Address - Base Address + Target Address

As an example:

Original Address[31:16] = {13h0,function_no[2:0]}
Base Address[31:16] = 16h0
Target Address[31:16] = {bus_no[7:0],device_no[4:0],3h0}

then:

Translated Address[31:16] = BDF ={bus_no[7:0], device_no[4:0], function_no[2:0]}

To handle eight functions (as the previous example indicates), you should use a 19-bit wide region size. For CFG transactions created directly by your application (asopposed to the iATU), you must ensure that the BDF field does not match any programmed iATU address region or else unintentional type translation could occur.

7.6.3.3.4 CFG Shift Feature

This feature is enabled by setting the CFG_SHIFT_MODE field the IATU_REGION_CTRL_2_OFF_OUTBOUND_0 register. The iATU uses bits [27:12] of the original address to form bits [31:16] (BDF location) of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space.

7.6.3.3.5 FMT Translation

The iATU automatically sets the TLP format field for three DWORDs when it detects all zeros in the upper 32 bits of the translated address. Otherwise, it sets it to four DWORDs when it detects a 64-bit address (that is, when there is a '1' in the upper 32 bits of the translated address). When the original address and the translated address are of different format, the iATU ensures that the TLP header size matches the translated address format.

7.6.3.3.6 Invert Feature

In normal operation an address match on an outbound TLP occurs when the untranslated address is in the region bounded by the base address and limit address. When the invert feature is activated, an address match occurs when the untranslated address is not in the region bounded by the base address and limit address. This feature is activated by setting the Invert field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_iregister.

7.6.3.3.7 DMA Bypass Feature

When you do not want the iATU to translate outbound requests that are generated by the DMA, you must implement one of the following approaches:

- Ensure that the combination of DMA channel address programming and iATU control register programming causes no translation of DMA traffic to be done in the iATU.
- Activate the DMA bypass mode to allow request TLPs which are initiated by the

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embedded DMA controller to pass through the iATU untranslated. You can activate the DMA bypass mode by setting the DMA Bypass field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_i register to 1.

7.6.3.3.8 Function Number Translation Bypass Feature

In this mode the function number of the translated TLP is taken from your application transmit interface and not from the Function Number field of the REGION_CTRL_1_OFF_OUTBOUND_i register. You can activate the function number bypass mode by setting the Function Number Translation Bypass Enable field in the IATU_REGION_CTRL_2_OFF_OUTBOUND_i to '1'.

7.6.3.3.9 General Bypass

Application can program PCIE_CLIENT_AXI_SLV_ATU_BYPASS register to do general ATU bypassing. Note that you should make sure that there is no transfer pending before you program this register.

7.6.3.3.10 Header Substitution (Tx)

When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. The expected usage scenario is for Vendor Defined Msg/MsgD and ATS transactions over the AXI bridge which is normally inefficient requiring a very large iATU region. Enabled using the HEADER_SUBSTITUTE_EN field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i.

7.6.3.3.11 Tag Substitution (Tx)

When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Enabled using the TAG_SUBSTITUTE_EN field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i.

Your application must not attempt to perform TAG substitution for outgoing non-posted TLPs.

Note: If the iATU is programmed to allow a TLP to be matched to more than one iATU outbound regions, the Function Number Translation Bypass field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_i register should be same for every region where that TLP can be matched.

7.6.3.4 Outbound Programming Example

Define Outbound Region 1 as:

64 KB I/O region from 0x80000000_d000000to 0x80000000_d000ffff, to be mapped to 0x00010000in the PCIe I/O space.

1. Setup the Region Base and Limit Address Registers.
   Write 0xd0000000to Address {0x208} to set the Lower Base Address.
   Write 0x80000000to Address {0x20C} to set the Upper Base Address.
   Write 0xd000ffff to Address {0x210} to set the Limit Address.
2. Setup the Target Address Registers.
   Write 0x00010000to Address {0x214} to set the Lower Target Address.
   Write 0x00000000to Address {0x218} to set the Upper Target Address.
3. Configure the region through the Region Control 1 Register.
   Write 0x00000002to Address {0x200} to define the type of the region to be I/O.
4. Enable the region.
   Write 0x80000000to Address {0x204} to enable the region.

7.6.3.5 Inbound Features

Address translation is used for mapping different address ranges to different memory spaces supported by your application. A typical example maps your application memory space to PCI memory space. The iATU supports type translation. Without address translation, your application address is passed from the TLPs directly through the AXI application interface. You can program the iATU to implement your own inbound address translation scheme without external logic.

- Programmable Match mode operation for MEM, I/O, CFG, and MSG TLPs. No translation

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for completions.
- Selectable BAR Match mode operation for I/O and MEM TLPs:
  - TLPs destined for the internal CDM (or ELBI) in an upstream port are not translated.
  - TLPs that are not error-free (ECRC, malformed and so on) are not translated.
- Programmable TLP header field matching:
  - TYPE/TD/TC/AT/ATTR/MSG-Code/TH/PH/ST
  - Function Number
- Multiple address regions programmable for location and size.
- Programmable enable/disable per region.
- Automatic FMT field translation between three DWORDs and four DWORDs for 64-bit addresses.
- Invert Address Matching mode to translate accesses outside of a successful address match.
- ECAM Configuration Shift mode to allow a 256 MB CFG1 space to be located anywhere in the 64-bit address space.
- Supports regions from 64 KB to 4 GB in size.
- Single Address Location to allow all TLPs to be translated to a single address location.
- Msg Type Match Mode to allow matching of any TLP of type Message.

7.6.3.6 Inbound Basic Operation

7.6.3.6.1 Overview

The following translation rules and limitations apply:
- When there is no match, then the address is untranslated. In addition
- TLPs destined for the internal registers in an upstream port are not translated.
- TLPs that are not error-free (ECRC, malformed and so on) are not translated.
- Address translation of all TLP types (MEM, I/O, CFG, and MSG) except completion is supported in Address Match mode. In BAR Match mode, only translation of I/O and MEM is supported.

The setting of the MATCH_MODE field in IATU_REGION_CTRL_2_OFF_INBOUND_0 determines how iATU inbound matching is done for each TLP type.

Table 7-6 Determination of Match Mode

TLP Type	MATCH_MODE =0	MATCH_MODE =1
MEM or I/O	Address Match Mode	BAR Match Mode
CFG0	Routing ID Match Mode	Accept Mode
MSG/MSGD	Address Match Mode	Vendor ID Match Mode

7.6.3.6.2 I/O and MEM Match Modes

Inbound address translation for I/O and MEM TLPs operates in one of two matching modes as determined by the "Inbound Match Mode" field in the IATU_REGION_CTRL_2_OFF_INBOUND_0 register.

Address Match Mode:

The operation is similar to "Outbound Basic Operation (Address Match Mode)". The address field of each request TLP is checked to see if it falls into any of the enabled address regions. When an address match is found then the TLP address field is modified as follows:

Address = Address - Base Address + Target Address

BAR Match Mode:

Looking for an address match is a two-step process.
1. The standard internal PCI Express BAR Matching Mechanism checks if the address field of any MEM and I/O request TLP falls into any address region defined by the enabled BAR addresses and masks.
2. When a matched BAR is found, then the iATU compares the BAR ID to the BAR Number field in the IATU_REGION_CTRL_2_OFF_INBOUND_0 register for all enabled regions. Figure below provides more details on inbound translation in BAR Match Mode.

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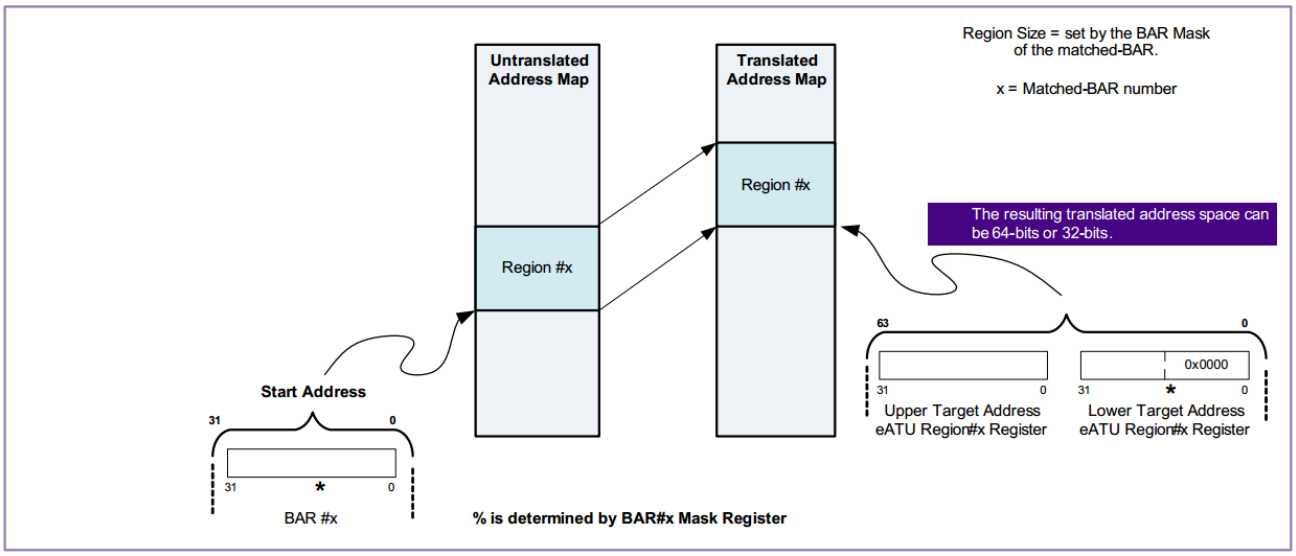

Fig. 7-6 Inbound BAR Match Mode

7.6.3.7 Inbound Detailed Operation

7.6.3.7.1 Single Address Location

When enabled and region address is matched, the TLPs can be translated to a single address location as determined by the target address register of the iATU region. This feature can be enabled using the SINGLE_ADDR_LOC_TRANS_EN field in IATU_REGION_CTRL_2_OFF_INBOUND_i. This feature is useful for translating messages on AXI bridge.

7.6.3.7.2 CFG Handling (Upstream Port)

The controller normally routes CFG TLPs (to the internal CDM or ELBI) without translation. The iATU only translates CFG0 TLPs that the controller has routed to the TRGT1. Inbound address translation for CFG0 TLPs operates in one of two matching modes as determined by the Inbound CFG0 Match Mode field in the IATU_REGION_CTRL_2_OFF_INBOUND_i register.

Accept Mode

The controller always accepts CFG0 TLPs even when the CFG bus number does not match the current bus number of the device. This mode follows that behavior. The routing ID of received CFG0 TLPs are ignored when determining a match.

Routing ID Match Mode

The operation is similar to "Outbound Basic Operation (Address Match Mode)". The routing ID of the inbound CFG0 TLP must fall within the Base and Limit of the defined iATU region for matching to proceed. The iATU interprets the routing ID (Bytes1 8-11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM and I/O transactions.

CFG Shift Feature

Inbound CFG transactions routed to the Rx application interface can exist anywhere in address space, because the PCIe controller filter processes the routing ID (BDF) as bits [31:16] of an address. This BDF changes according on the PCIe bus topology. A compressor feature (CFG Shift Feature) can be enabled by setting the CFG Shift bit in the IATU_REGION_CTRL_2_OFF_INBOUND_i register. Bits [15:12] of the third DWORD1 of CFG TLPs are reserved. The compressor feature uses this fact to reduce the memory requirement. This shifts/maps the BDF (bits [31:16] of the third header DWORD, which would be matched against the Base and Limit addresses) of the incoming CfgRd0/CfgWr0 down to bits [27:12] of the translated address.

7.6.3.7.3 Optional Matching Fields

In address and BAR match modes, a successful address/BAR match can be optionally gated by successful matching of the following programmable TLP header fields (per region):

- TYPE/TD/TC/AT/ATTR/TH/PH/ST
- MSG Code (MSG TLPs only)
- Function number (MEM, I/O, or CFG TLPs only)
- Virtual function number (MEM or I/O TLPs only)

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For each of the previous fields in the IATU_REGION_CTRL_1_OFF_INBOUND_i register, there is an associated Match Enable bit in the IATU_REGION_CTRL_2_OFF_INBOUND_i register. Address translation only proceeds when compares on all enabled field are successful.

7.6.3.7.4 Response Code Feature

When the Response Code field of the IATU_REGION_CTRL_REG_2_INBOUND_i register is set to a value other than 00, the controller uses it to determine the completion status field of completion TLPs sent in response to successfully match non-posted TLPs. This can be set to unsupported request (UR) or completer abort (CA). When the error response field is set to 2b00, then the normal receive filter response for this TLP is used.

7.6.3.7.5 Inbound MSG Handling

Inbound message (Msg/MsgD) transactions can use one of two matching modes:

Address Match Mode

The third and fourth header DWORDs are treated as an address and are compared against the iATU Region Base and Limit Address registers. For vendor defined messages this allows specific messages to be filtered into memory at the target address. The Upper Base address should be set to BDF and Vendor ID. The Lower Base address can be used as a filter for specific messages.

Vendor ID Match Mode

This mode is relevant for ID-routed vendor defined messages. The iATU ignores the routing ID (BDF) in bits [31:16] of the third DWORD of the TLP header1 but compares it against the vendor ID in bits [15:0] of the third DWORD of the TLP header (bytes1 10 and 11). This allows vendor defined messages to be filtered against specific vendor IDs without needing to know the BDF number which might vary depending on the PCI topology. Bits [15:0] of the Region Upper Base register should be programmed with the required vendor ID as follows:

Region Upper Base [15:8] =byte 10

Region Upper Base [7:0] =byte 11

The lower base and limit register should be programmed to translate TLPs based on vendor-specific information in the fourth DWORD of the TLP header.

7.6.3.7.6 Msg Type Match Mode

Inbound message (Msg/MsgD) transactions can also use Msg Type Matching mode. When this mode is enabled and Single Address Location is enabled, the iATU matches Msg TLP Type field with TYPE field of IATU_REGION_CTRL_1_OFF_INBOUND_i register.

If Fuzzy Type Match Mode is also enabled, then any Msg received will be matched (that is, Msg Type's sub-field r[2:0], which specifies the Message routing mechanism, is ignored). The Message should be consumed by your application before the next message arrives as all messages go to the same address.

If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN is set for any region, then you must ensure that the same TLP cannot be matched in any other region where SINGLE_ADDRESS_LOCATION_TRANSLATE_EN is not set. If this happens radm_trgt1_hdr_uppr_bytes could have incorrect data.

7.6.3.7.7 Fuzzy Type Match Mode

When enabled, the iATU relaxes the matching of the TLP type field against the expected type field so that:

- CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1.
- MWr, MRd and MRdLk TLPs are seen as identical.
- The routing field of MsgD TLPs is ignored.
- Atomic Ops TLPs-FetchAdd, Swap, and CAS are seen as identical.

For example, CFG0 in the type of field in the IATU_REGION_CTRL_1_OFF_INBOUND_i register matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. To enable this feature, set the Fuzzy Type Match Mode bit of the IATU_REGION_CTRL_OFF_2_INBOUND_i register.

7.6.3.7.8 FMT Translation

The iATU automatically sets the TLP format field for three DWORDs when it detects all zeroed in the upper 32 bits of the translated address. Otherwise, it sets it to four DWORDs when it detects a 64-bit address (when there is a 1 in the upper 32 bits of the translated

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address). When the original address and the translated address are of a different format then the iATU ensures that the TLP header size matches the translated address format.

7.6.3.7.9 Invert Feature

Normally an address match on an inbound TLP occurs when the untranslated address is in the region bounded by the Base address and Limit address. When the Invert feature is activated, an address match occurs when the untranslated address is not in the region bounded by the Base address and Limit address. This feature is activated by setting the Invert field of the IATU_REGION_CTRL_OFF_2_INBOUND_i register.

7.6.3.8 Inbound Programming Example

You must not update the iATU registers while operations are in progress on the AXI bridge slave interface.

Example 1:

Define Inbound Region 2 as: MEM region matching BAR4 (BAR match mode) mapping to 0x8000_0000_2000_0000 in your application memory space

1. Setup the Target Address Registers.
   Write 0x20000000 to Address {0x508} to set the Lower Target Address.
   Write 0x80000000 to Address {0x50C} to set the Upper Target Address.
2. Configure the region through the Region Control 1 Register.
   Write 0x00000000 to Address {0x500} to define the type of the region to be MEM.
3. Enable the region for BAR Match Mode.
   Write 0xC0000400 to Address {0x504} to enable the region for BAR match mode for BAR#4.

Example 2:

MEM region matching TLPs with addresses in the range 0x00010000 to 0x0005ffff mapped to 0x2000_0000 - 0x2004_ffff in your application memory space.

1. Setup the Region Base and Limit Address Registers.
   Write 0x00010000 to Address {0x108} to set the Lower Base Address.
   Write 0x00000000 to Address {0x10C} to set the Upper Base Address.
   Write 0x0005ffff to Address {0x110} to set the Limit Address
2. Setup the Target Address Registers.
   Write 0x20000000 to Address {0x114} to set the Lower Target Address.
   Write 0x10000000 to Address {0x118} to set the Upper Target Address.
3. Configure the region through the Region Control 1 Register.
   Write 0x00000000 to Address {0x100} to define the type of the region to be MEM.
4. Enable the region.
   Write 0x80000000 to Address {0x104} to enable the region in address match mode

7.6.4 PCIe Message Handling

This section describes the processing of messages through the controller. For a proper understanding of messages, you should be familiar with Section 2.2.8, "Message Request Rules" of the PCI Express Base Specification, Revision 3.0.

7.6.4.1 Message Generation

These are three methods to generate PCIe Messages:

- Specific MSG interface
  You can use PCIE_CLIENT_MSG_GEN_CON register to generate messages such as:
  - Vendor-Defined Message
  - Legacy PCI Interrupt Message
  - PME_Turn_Off message
  - Unlock message
  - LTR Message
  - OBFF Message

  Refer to register description for more details.
- AXI bridge
  In this method, you should program the PCIE_CLIENT_AXI_SLV_AWMISC_HDR PCIE_CLIENT_AXI_SLV_AWMISC_HDR3 and PCIE_CLIENT_AXI_SLV_AWMISC_HDR4 registers to set these parameters:
  slv_awmisc_info [4:0] =MSG
  slv_awmisc_info [20:13] = message code

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slv_awmisc_tag [5:0] = tag
slv_awmisc_info_hdr_[3|4]dw = 3rd and 4th TLP header DWORD
Then you can send zero length memory write (slv_awstrb=0) to generate the message. You must not program registers mentioned above when there are normal transfers pending on AXI slave interface. And should set these registers in normal value when you want to send MWr TLP. This method is not recommended because of these limitations.

- AXI bridge and iATU
  Program related client register fields as follows:
  slv_awmisc_info[4:0] =MEM
  slv_awmisc_info_hdr_[3|4]dw = 3rd and 4th TLP header DWORD
  Then iATU needs to be configured to to translate MWr to Msg TLPs. Refer to "Address Translation" for more details. This method is not recommended because that it needs additional iATU resources.

7.6.4.2 Message Reception

PCIe controller use pcie_msg_int interrupt to indicate the reception of PCIe Message. Application can poll to PCIE_CLIENT_INTR_STATUS_MSG_RX register to check the status of Message reception. Refer to register information for details.

7.6.5 PCIe Power Management

7.6.5.1 Overview

The controller supports two categories of PM operations to control the device state (D-state) and link state. For a proper understanding of PCIe Power management you should be familiar with Section 5, "Power Management" of the PCI Express Base Specification, Revision 3.0.

Software PCI Compatible PM (PCI-PM)

- D-state PM of Function. The host software can direct the function to enter any of the D1, D2, or D3 low-power states. It does this by writing to the Power Management Control and Status Register (PMCSR) in the PCI-PM capability structure.
- D-state PM of Link. Link states are not visible to PCI-PM legacy compatible software and are derived from the power management D-states of the components connected to that link. The action of changing the D-state in the PMCSR indirectly causes a change in the link power state. The L1 state is entered whenever all functions of a USP on a link are programmed to a non-D0 state. The entry into L2 and L3 states is initiated by the DSP.

PCIe PM Mechanisms

- Active State PM (ASPM). When the USP is in L0 and detects idleness on the link for a specific amount of time, it automatically transitions the link to the L0s or L1 (optional) power state.
- L1 Substates. This is an optional PCIe feature that enables components on a link to further reduce idle power consumption while the link is in L1, including almost complete removal of power for the high speed PHY circuits.

7.6.5.2 L0s Operation

L0s is a low-power state enabled by ASPM. ASPM controls entry into L0s for the transmitter. The remote device controls entry into L0s for the receiver.

7.6.5.2.1 L0s Entry

All of these conditions must be met:

- ASPM L0s is enabled through the ASPM Control field in the Link Control register.
- L0s entry conditions as defined in Section 5.4.1.1.1, "Entry into the L0s State" of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L0S_ENTRANCE_LATENCY field in ACK_F_ASPM_CTRL_OFF).
- No higher stage of power-down requested.

7.6.5.2.2 L0s Exit

Any of these conditions can be met:

- A DLLP or TLP is pending to be sent.
- L1 entry conditions as defined in Section 5.4.1.2.1, "Entry into the L1 State" of the PCI Express Base Specification, Revision 3.0, are satisfied.
- PCIe link partner requests to enter into link recovery.

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7.6.5.3 L1 Operation (Non-substates)

The following topic will be discussed in this section: L1 (ASPM/PM) Entry and Exit Conditions and L1 Clock PM (L1 with REFCLK removal/PLL Off) Entry and Exit Conditions.

7.6.5.3.1 L1 (ASPM/PM) Entry

L1 is a low-power state enabled either by ASPM (L1-ASPM) or by the software changing the D-state (L1-PM). The L1 state is a bi-directional link low-power state and both link partners must negotiate to go to this state.

The L1-ASPM entry negotiation handshake uses PM_Active_State_Request_L1 DLLPs, PM_Request_Ack DLLPs, and PM_Active_State_Nak MSG TLPs. Refer to PCIe Basic Specification for more information.

There are three scenarios that cause the controller to enter L1 under ASPM conditions.

Scenario 1: L1 Idle Timeout in L0s

All of these conditions must be met in the USP:

- ASPM L1 and L0s are enabled through the ASPM Control field in the Link Control register.
- The ENTER_ASPMfield of ACK_F_ASPM_CTRL_OFFis set to ‘0’ and the link state is L0s for both link partners, or the ENTER_ASPMfield of ACK_F_ASPM_CTRL_OFFis set to ‘1’.
- L1 entry conditions as defined in Section 5.4.1.2.1, “Entry into the L1 State” of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L1_ENTRANCE_LATENCYfield in ACK_F_ASPM_CTRL_OFF).
- No higher stage of power-down requested.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller
- There are no pending requests at the AXI slave interface, that is, slv_a*valid must be 0.
- There are no pending DMA transfers.

Scenario 2: L1 Idle Timeout in L0

All of these conditions must be met in the USP:

- ASPM L1 is enabled and L0s is not enabled through the ASPM Control field in the Link Control register.
- Link state is L0.
- L1 entry conditions as defined in Section 5.4.1.2.1, “Entry into the L1 State” of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L1_ENTRANCE_LATENCYfield in ACK_F_ASPM_CTRL_OFF).
- No higher stage of power down-requested.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller.
- There are no pending requests at the AXI slave interface, that is, slv_a*valid must be 0.
- There are no pending DMA transfers.

Scenario 3: Application Controlled (USP only)

All of these conditions must be met in the USP:

- ASPM L1 is enabled through the ASPM Control field in the Link Control register.
- Your application writes 1 to the app_req_entr_l1 field in PCIE_CLIENT_POWER_CON register.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller.
- There are no pending requests at the AXI slave interface, that is, slv_a*validmust be 0.
- There are no pending DMA transfers.

L1-PM Entry

The power management state of a link is determined bythe D-state of theUSP.When you change the device state of the USP to D1, D2, or D3hot by writing to the PMCSR, the controller must initiate a link state transition to L1.

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An USP application asserting the app_xfer_pending field does not prevent L1-PM entry, but will cause immediate exit from L1-PM.

7.6.5.3.2 L1-PM/L1-ASPM Exit

Any of these conditions are met:

- A DLLP or TLP is pending to be sent.
- Your application asserts the app_req_exit_l1 field.
- Link partner is requesting exit from L1.
- Your application asserts the app_xfer_pending field.
- Your application asserts the app_pm_xmt_pme field.

When the USP is programmed with capability to support PME; it sends a PME message to the RC which calls the PM software to transition the USP to the D0 state. Therefore, you should only use app_pm_xmt_pme for L1-PM exit.

- PM software (RC) requests a higher stage of power-down by writing to the PMCSR in the USP.
- Your application (USP) requests transmission of VDM, MSI/MSIX, or LTR message. Legacy interrupt is not included.
- Your application (DSP) requests transmission of Unlock message.
- Your application is requesting to send traffic by asserting or slv_a*valid.
- Your application doorbells a DMA read or write channel, or DMA controller is requesting data.
- Your application (DSP) initiates link disable, or link retrain (by setting PCIE_CAP_LINK_DISABLE or PCIE_CAP_RETRAIN_LINK field in LINK_CONTROL_LINK_STATUS_REG to 1).
- Your application (DSP) initiates hot reset by either:
  - setting RESET_ASSERT field in PORT_LINK_CTRL_OFF to 1, or
  - setting SBR field in BRIDGE_CTRL_INT_PIN_INT_LINE_REG to 1, or
  - toggling app_init_rst field in PCIE_CLIENT_GENERAL_CON.
- Your application requests a speed change (by setting DIRECT_SPEED_CHANGE field in GEN2_CTRL_OFF to 1).
- Your application requests link width change (by setting DIRECT_LINK_WIDTH_CHANGE field in MULTI_LANE_CONTROL_OFF is set to 1).

7.6.5.3.3 L1 Clock PM

For an USP, host software uses the Enable Clock Power Management bit in the Link Control register to enable this feature. For a DSP, this register bit is hard coded to '0' and cannot be used to control this behavior. Your application can use the app_clk_pm_en input to dynamically control whether to execute L1 with or without Clock PM.

- The Support Clock Power Management bit in the Link Capabilities register must be set. For downstream ports it is hardcoded to 0, for upstream ports it can be accessed through the DBI.
- The Enable Clock Power Management bit in the Link Control register must be set.
- You must set the app_clk_pm_en field to 1. The controller only samples app_clk_pm_en when L1 is entered.

L1 with Clock PM and L1 substates work orthogonal to each other. L1 with Clock PM uses the mac_phy_pclkreq_n[0]signaling, and L1 substates uses the mac_phy_pclkreq_n[1]signaling. However, L1 substates takes precedence over Clock PM within the cores PM state machine.

7.6.5.4 L1 Substate

The L1 substates are applicable in both the ASPM and PCI-PM L1 link states. L1 substates management utilizes a per-link sideband signal called CLKREQ#.

- During L1 substates it is assumed that core_clk is turned off and that aux_clk is active. It is required that your application switches aux_clk to a low frequency free running clock on entry into L1.
- The controller uses aux_clk for counting time during L1 substates. You must program the frequency of this clock into the L1_SUBSTATES_OFF register with a value in the range 1...1000MHz to count real time. Frequencies lower than 1 MHz are possible, but with a loss of accuracy in the time counted.
- When the electrical idle detection circuitry is disabled, it is assumed that the PHY holds

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the signal phy_mac_rxelecidle to 1.

After the link has entered L1 through the normal L1 negotiation, the USP can initiate the sequence for entering the target L1 substate (L1.1 or L1.2) by tri-stating its CLKREQ# output buffer. The entry sequence can only proceed if the DSP is also tri-stating its CLKREQ# output buffer, resulting in the bidirectional CLKREQ# signal being pulled up to 1. Otherwise CLKREQ# will remain asserted at 0 and the link state will stay in L1. The exit sequence can be initiated by either port by asserting CLKREQ# to 0. For each port there are two cases to consider, the first where the exit is initiated locally, the second where the exit is initiated remotely. L1 substates management utilizes a per-link sideband signal called CLKREQ#.

7.6.5.4.1 L1 Substates Software Control

When the controller enters L1, the target L1 substate depends on several programming bits:

- PM Control/Status Register
  - USP: The current D-state
  - DSP: The DLLP type that was used by USP to request L1
- L1 Substates Control 1 Register
  - ASPM PM L1.1 Enabled
  - ASPM PM L1.2 Enabled
  - PCI PM L1.1 Enabled
  - PCI PM L1.2 Enabled

After the USP controller enters L1, it uses the D-state of the device to determine if L1 was entered in ASPM mode or PCI-PM mode.

After the DSP controller enters L1, it uses the USPs DLLPL1 request type to determine if L1 was entered in ASPM mode or PCI-PM mode. The next tables show the target L1 substate as a function of the relevant programming bits.

Table 7-7 Target L1 Substate as a Function of Software Controls (USP)

D-State	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
!D0	-	-	-	0	0	L1
!D0	-	-	-	1	0	L1.1
!D0	-	-	-	-	1	L1.2
D0	0	0	-	-	-	L1
D0	1	0	-	-	-	L1.1
D0	0	1	0	-	-	L1
D0	1	1	0	-	-	L1.1
D0	-	1	1	-	-	L1.2

Table 7-8 Target L1 Substate as a Function of Software Controls (DSP)

DLLP Receive	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
PM_Enter_L1	-	-	-	0	0	L1
	-	-	-	1	0	L1.1
	-	-	-	-	1	L1.2
PM_Active_State_Request_L1	0	0	-	-	-	L1
	1	0	-	-	-	L1.1
	0	1	0	-	-	L1
	1	1	0	-	-	L1.1
	-	1	1	-	-	L1.2

The Reported LTR is the maximum of the snoop/no snoop latency values embedded in LTR messages transmitted by the upstream ports or received by the downstream port. The

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controller stores these values in the port logic LTR Latency Register (LTR_LATENCY_OFF). When the requirement bit in the message is 0, the latency value is considered infinite (that is, the check with the threshold always pass).

7.6.5.4.2 L1 Substates Entry and Exit

PCIe link entered L1 substate automatically if related enable bit is set and LTSSM already in L1 state, refer to section L1 Substates Software Control for details.

L1 substates Exit can be triggered locally or Remotely. For locally initiated exit, refer to section L1-PM/L1-ASPM Exit. Remotely initiated exit begins when CLKREQ# is asserted by remote PCIe partner.

7.6.5.5 L2 and L3 Power Down Entry and Exit

L2/L3 entry is initiated after the RC calls power management software to initiate the removal of power and clocks. USPs of devices in D0, D1, D2, and D3hot must respond to the receipt of a PME_Turn_Off MSG TLP by transmitting a PME_TO_Ack MSG TLP. The device must then request a link transition to L2/L3_Ready. L2/L3_Ready is a bi-directional link power down state. If your application is not ready to be shut down, it must keep the app_ready_entr_l23 field de-asserted.

L2/L3 Entry

All of these conditions must be met:

- PME_Turn_Off/PME_TO_Ack handshake has been completed.
- Your USP application is ready to be turned off; app_ready_entr_l23=1.
- After sending the PME_TO_Ack, the USP initiates the L2/L3 Ready transition protocol by sending the PM_Enter_L23 DLLP. The RC responds with the PM_Request_Ack.

L2/L3 Exit

Any of these conditions can be met:

- When the USP is programmed with capability to support PME, your application can assert the apps_pm_xmt_pme field to request the controller to wake up. The USP then sends a PM_PME MSG TLP to the RC which calls the PM software to transition the USP out of the D3 state.
- Device is programmed with capability to support PME and your application requests the controller to wake up by triggering a native hot-plug event.
- Link partner is requesting exit from L2/L3.

7.6.5.6 Dynamic Power Allocation (DPA)

The DPA capability enables software to actively manage and optimize function power usage when in the D0 state. DPA is not applicable to power states D1-D3.

For details on how your application interacts with the controller, see the description of the dpa_sub_upd_int field in PCIE_CLIENT_INTR_STATUS_MISC register.

7.6.6 PCIe Interrupt

The PCIe provides several types of interrupts to system interrupt controller. They can be divided into MSI/MSI-X, PCIe Error interrupt, PCIe Message Receive interrupt, PCIe Legacy interrupt, PCIe System interrupt and PCIe Power Management Interrupt etc. When operating as RC, the PCIe is capable of handling both MSI/MSI-X and legacy interrupts. This is because when operating as RC it should be able to service both PCIe end points as well as legacy endpoints. It is capable of generating MSI or Legacy interrupt if the PCIe is configured as EP. Notes that PCIe EP component can't generate both Legacy and MSI/MSI-X interrupt. It is either one or the other. The interrupt type an EP generates is configured during configuration time.

Interrupt status and mask bits are located in client register group, some interrupts are handled by client register directly, but some interrupts are generated by events deep into controller and software should clear the root cause to serve the interrupt events. For more information, refer to the register description.

The pcie_edma_wr/rd_int is more efficient than service by pcie_sys_int, it is available depends on Chip ID.

Table 7-9 PCIe Interrupt Table

System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
pcie_sys_int	PCIe System	phy_link_up_int	RC & EP

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System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
	Interrupt	dll_link_up_int	RC & EP
		link_req_rst_not_int	RC & EP
		hp_pme_int	RC
		hp_int	RC
		hp_msi	RC
		link_auto_bw_int	RC
		link_auto_bw_msi	RC
		bw_mgt_int	RC
		bw_mgt_msi	RC
		edma_wr_int	RC & EP
		edma_rd_int	RC & EP
		dpa_sub_upd_int	EP
		rbar_updata_int	EP
		link_eq_req_int	RC & EP
		ep_elbi_app_int	EP
pcie_legacy_int	PCIe Legacy interrupt	rx_inta_int	RC
		rx_intb_int	RC
		rx_intc_int	RC
		rx_intd_int	RC
		tx_inta_int	EP
		tx_intb_int	EP
		tx_intc_int	EP
		tx_intd_int	EP
pcie_msg_rx_int	PCIe message received interrupt	ven_msg_int	RC & EP
		unlock_msg_int	EP
		ltr_msg_int	RC
		cfg_pme_int	RC
		cfg_pme_msi_int	RC
		pm_pme_int	RC
		pm_to_ack_int	RC
		pm_turnoff_int	EP
		obff_idle_int	EP
		obff_obff_int	EP
		obff_cpu_active_int	EP
pcie_err_int	PCIe Error interrupt	aer_rc_err_int	RC
		aer_rc_err_msi	RC
		rx_cpl_timeout_int	RC & EP
		tx_cpl_timeout_int	RC & EP
		cor_err_sent_int	EP
		nf_err_sent_int	EP
		f_err_sent_int	EP
		cor_err_rx_int	RC
		nf_err_rx_int	RC
		f_err_rx_int	RC
		radm_qoverflow_int	RC & EP
pcie_pmc_int	PCIe Power Management interrupt	linkst_in_l1sub_int	RC & EP
		linkst_in_l1_int	RC & EP
		linkst_in_l2_int	RC & EP
		linkst_in_l0s_int	RC & EP
		linkst_out_l1sub_int	RC & EP
		linkst_out_l1_int	RC & EP
		linkst_out_l2_int	RC & EP

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System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
		linkst_out_l0s_int	RC & EP
		pm_dstate_update_int	EP
pcie_msi_ctrl_int	MSI/MSI-X	message signaled interrupt	RC
pcie_msi_ctrl_int_vec[7:0]	MSI/MSI-X	message signaled interrupt	RC

7.7 Appendix

7.7.1 LTSSM Code

S_DETECT_QUIET	6'h00
S_DETECT_ACT	6'h01
S_POLL_ACTIVE	6'h02
S_POLL_COMPLIANCE	6'h03
S_POLL_CONFIG	6'h04
S_PRE_DETECT_QUIET	6'h05
S_DETECT_WAIT	6'h06
S_CFG_LINKWD_START	6'h07
S_CFG_LINKWD_ACEPT	6'h08
S_CFG_LANENUM_WAIT	6'h09
S_CFG_LANENUM_ACEPT	6'h0A
S_CFG_COMPLETE	6'h0B
S_CFG_IDLE	6'h0C
S_RCVRY_LOCK	6'h0D
S_RCVRY_SPEED	6'h0E
S_RCVRY_RCVRCFG	6'h0F
S_RCVRY_IDLE	6'h10
S_RCVRY_EQ0	6'h20
S_RCVRY_EQ1	6'h21
S_RCVRY_EQ2	6'h22
S_RCVRY_EQ3	6'h23
S_L0	6'h11
S_L0S	6'h12
S_L123_SEND_EIDLE	6'h13
S_L1_IDLE	6'h14
S_L2_IDLE	6'h15
S_L2_WAKE	6'h16
S_DISABLED_ENTRY	6'h17
S_DISABLED_IDLE	6'h18
S_DISABLED	6'h19
S_LPBK_ENTRY	6'h1A
S_LPBK_ACTIVE	6'h1B
S_LPBK_EXIT	6'h1C
S_LPBK_EXIT_TIMEOUT	6'h1D
S_HOT_RESET_ENTRY	6'h1E
S_HOT_RESET	6'h1F

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Chapter 8 Gigabit Media Access Controller (GMAC)

8.1 Overview

GMAC(Gigabit Media Access Controller) we name it GMAC Controller in the charpter, also named it GMAC0.
GMAC Controller provides a complete Ethernet interface from processor to a Reduced Media Independent Interface (RMII) and Reduced Gigabit Media Independent Interface (RGMII) compliant Ethernet PHY.
It have DMAC controller.The DMA controller efficiently moves packet data from microprocessor's RAM, formats the data for an IEEE 802.3-2002 compliant packet and transmits the data to an Ethernet Physical Interface (PHY). It also efficiently moves packet data from RXFIFO to microprocessor's RAM.

8.1.1 GMAC Features

8.1.1.1 GMAC Tx and Rx Common Features

- (GMAC) Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
- (GMAC) Supports 10/100-Mbps data transfer rates with the RMII interfaces
- (GMAC) Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support (based on implementation-specific whitepapers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
  - (GMAC)Packet bursting and packet extension in 1000 Mbps half-duplex operation
- (GMAC) Standard IEEE 802.3az-2010 for Energy Efficient Ethernet in Reduced Gigabit MediaIndependent Interface (RGMII) PHYs
- (GMAC) 64-bit data transfer interface on the application side
- (GMAC) Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- (GMAC) Media clock generation and recovery
- (GMAC) MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

8.1.1.2 GMAC Tx Features

- (GMAC)Preamble and start of packet data (SFD) insertion
- (GMAC)Separate 32-bit status for each packet transmitted from the application
- (GMAC)Automatic CRC and pad generation controllable on a per-packet basis
- (GMAC)Programmable packet length to support Standard or Jumbo Ethernet packets with up to16 KB of size
- (GMAC)Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- (GMAC)IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flowcontrol input transitions from assertion to de-assertion (in full-duplex mode)
- (GMAC)Frame Preemption for MAC Tx

8.1.1.3 GMAC Rx Features

- (GMAC)Automatic Pad and CRC Stripping options
- (GMAC)Option to disable Automatic CRC checking
- (GMAC)Preamble and SFD deletion
- (GMAC)Separate 112-bit or 128-bit status
- (GMAC)Programmable watchdog timeout limit
- (GMAC)IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- (GMAC)Frame Preemption for MAC Rx

8.1.2 MTL Features

8.1.2.1 MTL Tx and Rx Common Features

- (GMAC) 32-bit, 64-bit, or 128-bit Transaction Layer block (bridges the application and the MAC)
- (GMAC) Data transfers executed using simple FIFO protocol
- (GMAC) Synchronization for all clocks in the design (Transmit, Receive, and Application clocks)
- (GMAC) Programmable burst length, up to half the size of the MTL Rx queue or Tx

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queue size, to support burst data transfer in the GMAC-MTL configuration
- (GMAC) Programmable threshold capability for each queue (default of 64 bytes)

8.1.2.2 MTL Tx Features
- (GMAC) Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- (GMAC) Programmable queue size in configurations with multiple queues. Each queue size can be programmed in terms of 256 bytes
- (GMAC) Automatic retransmission of collision packets in half-duplex mode
- (GMAC) Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- (GMAC) Disabling of Data Memory RAM chip-select when inactive to reduce power consumption

8.1.2.3 MTL Rx Features
- (GMAC) Rx queue sizes in the Receive path is 32 KB
- (GMAC) Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in Store-and-Forward mode) in GMAC-MTL configuration
- P(GMAC) programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- (GMAC) Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- (GMAC) Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level

8.1.3 DMA Block Features
- (GMAC)64-bit data transfers
- (GMAC)Separate DMA channel in the Transmit path for each queue in MTL
- (GMAC)Single or multiple DMA channels for any number of queues in MTL Receive path
- (GMAC)Fully synchronous design operating on a single application clock (except for CSR module, when a separate CSR clock is configured)
- (GMAC)Byte-aligned addressing for data buffer support
- (GMAC)Dual-buffer (ring) descriptor support
- (GMAC)Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- (GMAC)Comprehensive status reporting for normal operation and transfers with errors
- (GMAC)Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- (GMAC)Programmable interrupt options for different operational conditions
- (GMAC)Per-packet Transmit or Receive Complete Interrupt control
- (GMAC)Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- (GMAC)Start and Stop modes
- (GMAC)Separate ports for host CSR access and host data interface
- (GMAC)support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO)
- (GMAC)Selectable number of Tx DMA channels with TSO/USO feature enabled
- (GMAC)Programmable control for Transmit Descriptor posted writes to improve the throughput
- (GMAC)Sideband signals to control starting and stopping of DMA channels

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8.2 Block Diagram

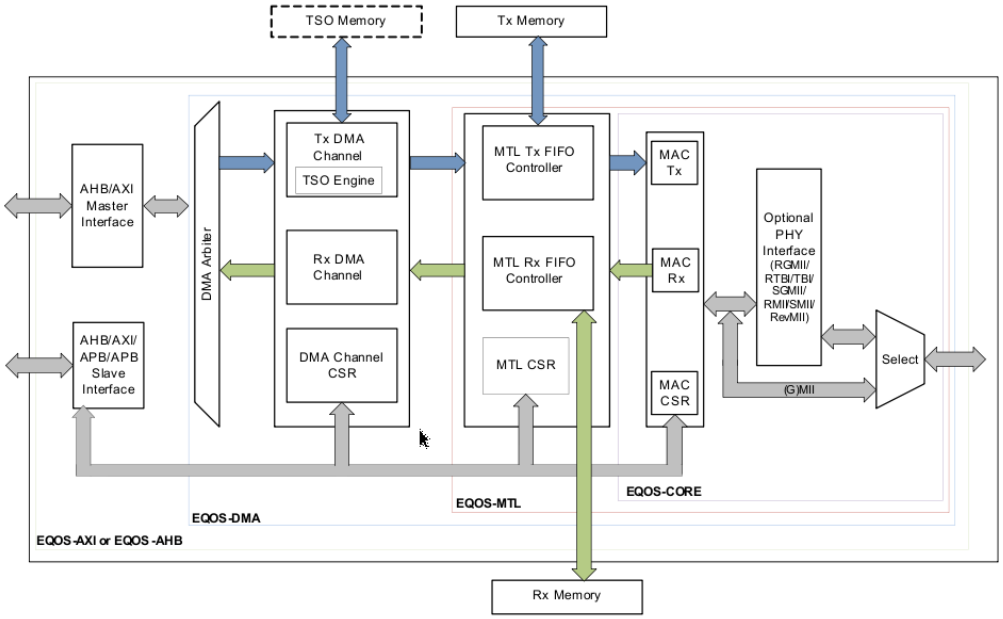

Fig. 8-1GMAC Block Diagram

The GMAC is broken up into multiple separate functional units. These blocks are interconnected in the MAC module. The block diagram shows the general flow of data and control signals between these blocks.

The GMAC transfers data to system memory through the AXI master interface. The host CPU uses the APB Slave interface to access the GMAC subsystem's control and status registers (CSRs).

The GMAC supports the PHY interfaces of reduced GMII (RGMII) and reduced MII (RMII).

The Transmit FIFO (Tx FIFO) buffers data read from system memory by the DMA before transmission by the GMAC Core. Similarly, the Receive FIFO (Rx FIFO) stores the Ethernet frames received from the line until they are transferred to system memory by the DMA. These are asynchronous FIFOs, as they also transfer the data between the application clock and the GMAC line clocks.

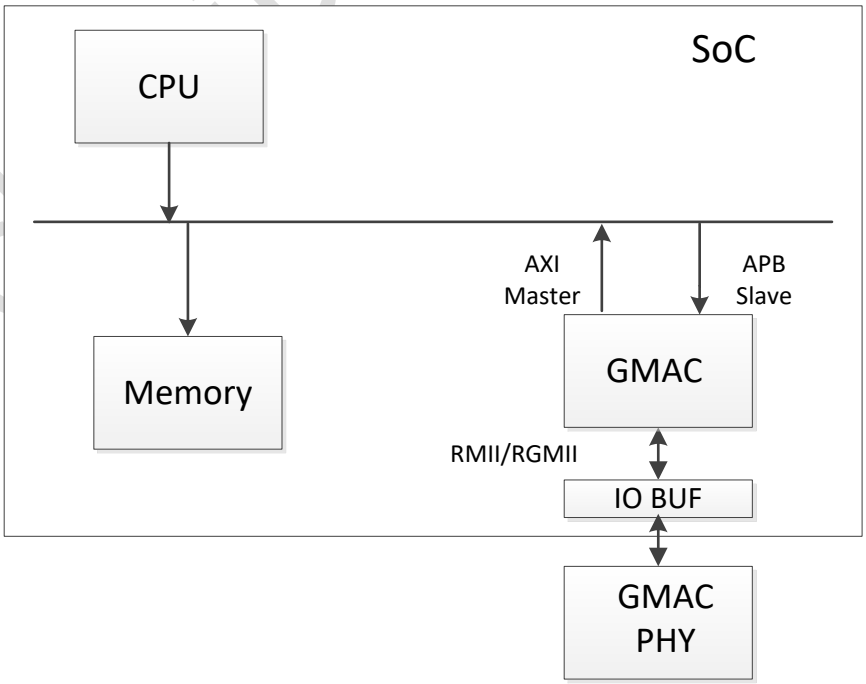

Fig. 8-2 GMAC in SOC

GMAC Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces and Supports 10/100-Mbps data transfer rates with the RMII interfaces.

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8.3 Function Description

8.3.1 Frame Structure

Data frames transmitted shall have the frame format shown in the following figure.

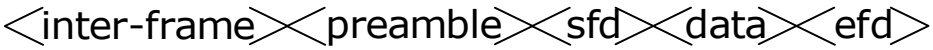

Fig. 8-3 Frame Format

The preamble <preamble> begins a frame transmission. The bit value of the preamble field consists of 7 octets with the following bit values:
10101010 10101010 10101010 10101010 10101010 10101010 10101010
The SFD (start frame delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value is 10101011.The data in a well formed frame shall consist of N octet's data.

8.3.1.1 RMII Interface timing diagram

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. In devices incorporating multiple MAC or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port - a 62.5% decrease in pin count.
The RMII module is instantiated between the GMAC and the PHY. This helps translation of the MAC's MII into the RMII. The RMII block has the following characteristics:
Supports 10-Mbps and 100-Mbps operating rates. It does not support 1000-Mbps operation. Two clock references are sourced externally or CRU, providing independent, 2-bit wide transmit and receive paths.

8.3.1.2 Transmit Bit Ordering

Each nibble from the MII must be transmitted on the RMII a di-bit at a time with the order of di-bit transmission shown in the following figure. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

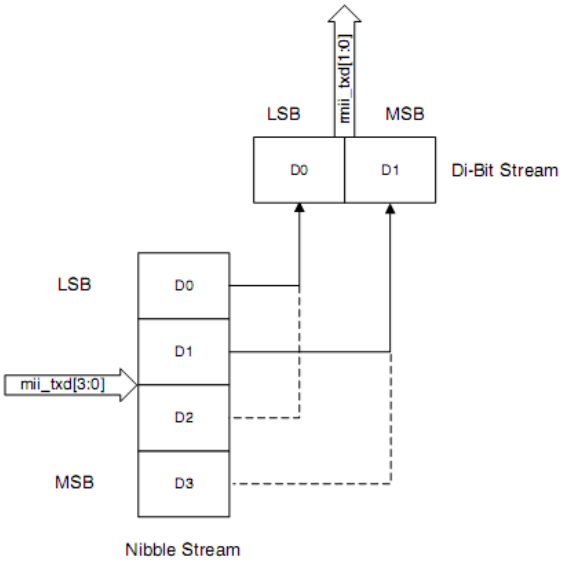

Fig. 8-4 RMII Transmission Bit Ordering

8.3.1.3 RMII Transmit Timing Diagrams

The following figures show MII-to-RMII transaction timing. The clk_rmii_i (REF_CLK) frequency is 50MHz in RMII interface. In 10Mb/s mode, as the REF_CLK frequency is 10 times as the data rate, the value on rmii_txd_o[1:0] (TXD[1:0]) shall be valid such that TXD[1:0] may be sampled every 10th cycle, regard-less of the starting cycle within the group and yield the correct frame data.

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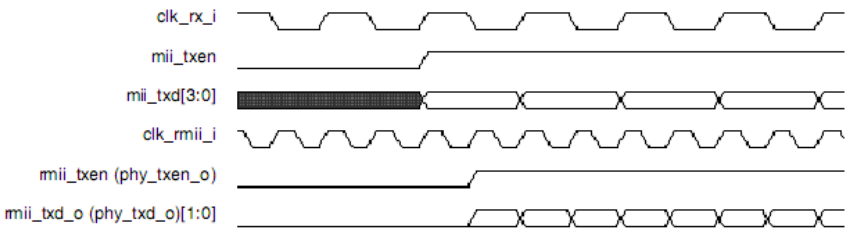

Fig. 8-5 Start of MII and RMII Transmission in 100-Mbps Mode

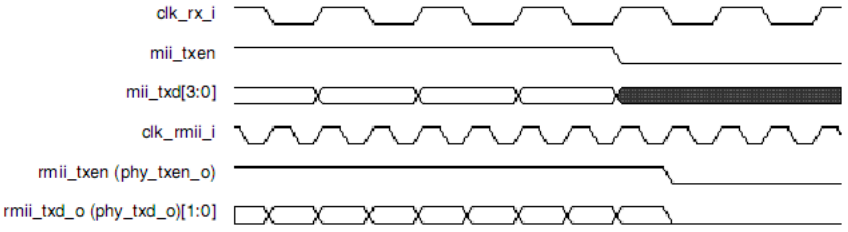

Fig. 8-6 End of MII and RMII Transmission in 100-Mbps Mode

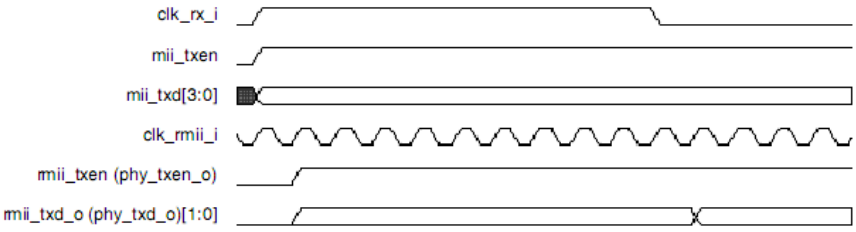

Fig. 8-7 Start of MII and RMII Transmission in 10-Mbps Mode

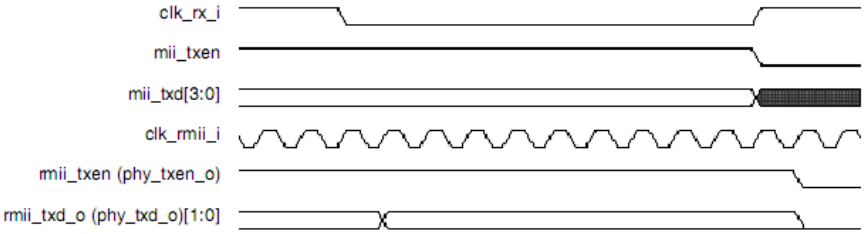

Fig. 8-8 End of MII and RMII Transmission in 10-Mbps Mode

8.3.1.4 Receive Bit Ordering

Each nibble is transmitted to the MII from the di-bit received from the RMII in the nibble transmission order shown in the following figure. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

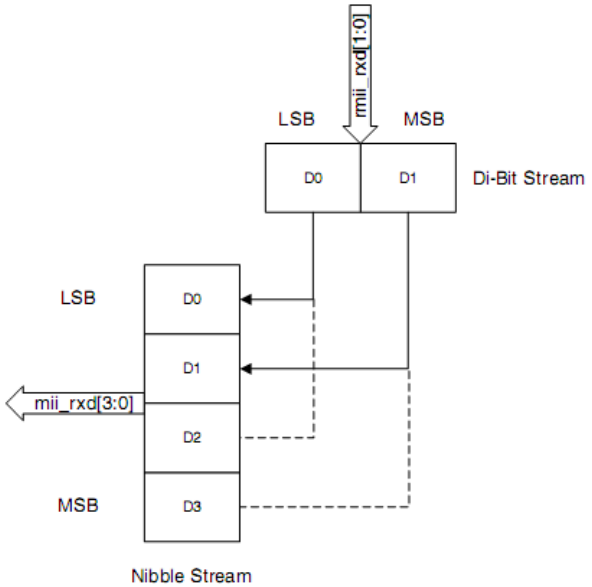

Fig. 8-9 RMII Receive Bit Ordering

8.3.1.5 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) specification reduces the pin

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count of the interconnection between the GMAC 10/100/1000 controller and the PHY for GMII and MII interfaces. To achieve this, the data path and control signals are reduced and multiplexed together with both the edges of the transmission and receive clocks. For gigabit operation the clocks operate at 125 MHz; for 10/100 operation, the clock rates are 2.5 MHz/25 MHz.

In the GMAC 10/100/1000 controller, the RGMII module is instantiated between the GMAC core's GMII and the PHY to translate the control and data signals between the GMII and RGMII protocols.

The RGMII block has the following characteristics:

- Supports 10-Mbps, 100-Mbps, and 1000-Mbps operation rates
- For the RGMII block, no extra clock is required because both the edges of the incoming clocks are used
- The RGMII block extracts the in-band (link speed, duplex mode and link status) status signals from the PHY and provides them to the GMAC core logic for link detection

8.3.2 Station Management Agent

The application can access the PHY registers through the Station Management Agent (SMA) module. SMA is a two-wire Station Management interface (MIM).

For MIM accesses, the maximum operating frequency of the MDC (gmii_mdc_o) is 2.5 MHz, as specified in the IEEE 802.3. In the GMAC core, the gmii_mdc_o clock is derived from the application clock or clk_csr_i, using a divider-counter. The divide factor depends on the clock range setting (CR field) in the MAC_MDIO_Address register Select the clock divide factor as mentioned in the description of CR field of MAC_MDIO_Address register, to meet IEEE specifications. However, if your system supports higher clock frequencies on the MIM interface, there is a provision to select a different divider.

The MDIO frame structure is as follows:

Table 8-1 MDIO Clause 45 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b00
OPCODE	■ 2'b00 ■ 2'b01 ■ 2'b10 ■ 2'b11
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address select for one of 32 devices
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	16-bit value: For an address cycle (OPCODE = 2'b00), this frame contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, this field contains the data to be written to the register. For read or post-read increment address frames, this field contains the contents of the register read from the PHY. ■ In address and data write cycles, the GMAC drives the MDIO line during the transfer of these 16 bits. ■ In read and post-read increment address cycles, the PHY drives the MDIO line during the transfer of these 16 bits.

The frame structure for Clause 22 frames is also supported. The C45E bit in the MAC_MDIO_Address register can be programmed to enable Clause 22 or Clause 45 mode of operation. Table.1-2 shows the Clause 22 frame format.

Table 8-2 MDIO Clause 22 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o

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Field	Description
	signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b01
OPCODE	■ 2'b01 :Write ■ 2'b10 :Read
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address to select the register within each MMD
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	Any 16-bit value: ■ In a write operation, the GMAC drives MDIO ■ In read operation, the PHY drives MDIO

In addition to normal read and write operations, the SMA also supports post-read increment address while operating in Clause 45 mode.

8.3.3 Power Management and Energy Efficient Ethernet

The GMAC supports the following techniques to save power.

- Magic Packet
- Remote Wakeup
- Energy Efficient Ethernet

The Magic Packet and Remove Wakeup techniques are used to save power in the host system when it is idle (Sleep mode) and has to be woken up only at the reception of specific packets from the Ethernet network. In the Sleep mode, the power to the host logic along with majority of the GMAC (except the MAC receiver logic), can be shut down. On receiving the specific packets from the network, the MAC provides the trigger to restore the power to the host system and come back to normal state.

The Energy Efficient Ethernet (EEE) mode is compliant with the IEEE 802.3az-2010 standard. It is primarily targeted to save power in the Ethernet port when there is no traffic on the line. In this mode, the host indicates to the far-end that it does not have any packets to transmit for near future and puts the transmitter port (MAC Controller, PCS and PHY layers) into low-power mode. Similarly, the Receiver port can also be put into low-power mode when the far-end host indicates that it does not have any traffic to transfer. This allows significant saving of power in the Ethernet port (mainly in the PHY) with intermittent and bursty traffic profile. The triggering of entry and exit out of the EEE mode is controlled by the MAC and is supported within the GMAC.

Simultaneous operation of the EEE mode along with any or both the other power saving modes is also supported in GMAC.

8.3.4 TCP/IP Segmentation Offload (TSO) Engine

Only the GMAC Controller has this function.

The TCP Segmentation Offload (TSO) engine is useful in offloading the TCP segmentation functions to the hardware.

It also supports UDP Segmentation Offload (USO) in which the UDP payload is segmented in the hardware. There are no sequencing/ordering controls available or updated in the segments, so it can be used in point to point applications in which out of order packets are not expected by the receiver. The description and flow of TSO mentioned in this section is same as USO, any deviation is provided as notes.

In the TCP segmentation offload (TSO) feature, the DMA splits a large TCP packet into multiple small packets and passes these packets to the MTL Tx Queue.

8.3.5 MAC Management Counters

The GMAC supports storing the statistics about the received and transmitted packets in registers that are accessible through the application.

The counters in the MAC Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted packets. The

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register set includes a control register for controlling the behavior of the registers, two status registers containing interrupts generated (receive and transmit), and Interrupt Enable registers (receive and transmit). These registers are accessible from the Application through the MAC Control Interface (MCI). Each register is 32-bits wide. The write data is qualified with the corresponding mci_be_i signals. Therefore, non-32-bit accesses are allowed as long as the address is word-aligned. The MMCs are accessed using transactions, in the same way the CSR address space is accessed.
The MMC counters are free running. There is no separate enable for the counters to start. If a particular MMC counter is present in the RTL, it starts counting when corresponding packet is received or transmitted. The Receive MMC counters are updated for packets that are passed by the Address Filter (AFM) block. The statistics of packets, dropped by the AFM module, are not updated unless they are runt packets of less than 6 bytes (DA bytes are not received fully). To get statistics of all packets, set Bit 0 in the “MAC_Packet_Filter” register.
The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet packets.

8.4 Register Description

8.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GMAC_MAC_Configuration	0x0000	W	0x00008000	The MAC Configuration Register establishes the operating mode of the MAC
GMAC_MAC_Ext_Configuration	0x0004	W	0x00000000	The MAC Extended Configuration Register establishes the operating mode of the MAC
GMAC_MAC_Packet_Filter	0x0008	W	0x00000000	The MAC Packet Filter register contains the filter controls for receiving packets
GMAC_MAC_Watchdog_Timeout	0x000C	W	0x00000000	The Watchdog Timeout register controls the watchdog timeout for received packets
GMAC_MAC_Hash_Table_Reg0	0x0010	W	0x00000000	The Hash Table Register 0 contains the first 32 bits of the hash table
GMAC_MAC_Hash_Table_Reg1	0x0014	W	0x00000000	The Hash Table Register 1 contains the second 32 bits of the hash table
GMAC_MAC_VLAN_Tag	0x0050	W	0x00000000	The VLAN Tag register identifies the IEEE 802.1Q VLAN type packets
GMAC_MAC_VLAN_Hash_Table	0x0058	W	0x00000000	When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag
GMAC_MAC_Q0_Tx_Flow_Ctrl	0x0070	W	0x00000000	The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC
GMAC_MAC_Rx_Flow_Ctrl	0x0090	W	0x00000000	The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_Interrupt_Status	0x00B0	W	0x00000000	The Interrupt Status register contains the status of interrupts
GMAC_MAC_Interrupt_Enable	0x00B4	W	0x00000000	The Interrupt Enable register contains the masks for generating the interrupts
GMAC_MAC_Rx_Tx_Status	0x00B8	W	0x00000000	The Receive Transmit Status register contains the Receive and Transmit Error status
GMAC_MAC_PMT_Control_Status	0x00C0	W	0x00000000	The PMT Control and Status Register
GMAC_MAC_RWK_Packet_Filter	0x00C4	W	0x00000000	The Remote Wakeup Filter registers are implemented as 8, 16, or 32 indirect access registers (wkuppktfilter_reg#i) based on whether 4, 8, or 16 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC_RWK_Packet_Filter register
GMAC_MAC_LPI_Control_Status	0x00D0	W	0x00000000	The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read
GMAC_MAC_LPI_Timers_Control	0x00D4	W	0x03E80000	The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission
GMAC_MAC_LPI_Entry_Timer	0x00D8	W	0x00000000	This register controls the Tx LPI entry timer. This counter is enabled only when bit[20](LPITE) bit of MAC_LPI_Control_Status is set to 1
GMAC_MAC_1US_Tic_Counter	0x00DC	W	0x00000063	This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially
GMAC_MAC_PHYIF_Control_Status	0x00F8	W	0x00000000	The PHY Interface Control and Status register indicates the status signals received by the SGMII, RGMII, or SMII interface (selected at reset) from the PHY. This register is optional
GMAC_MAC_Version	0x0110	W	0x00004051	The version register identifies the version of the DWC_ether_qos
GMAC_MAC_Debug	0x0114	W	0x00000000	The Debug register provides the debug status of various MAC blocks

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_HW_Feature0	0x011C	W	0x400123E3	This register indicates the presence of first set of the optional features or functions
GMAC_MAC_HW_Feature1	0x0120	W	0x010E41A7	This register indicates the presence of second set of the optional features or functions
GMAC_MAC_HW_Feature2	0x0124	W	0x10000000	This register indicates the presence of third set of the optional features or functions
GMAC_MAC_HW_Feature3	0x0128	W	0x00000000	This register indicates the presence of fourth set the optional features or functions
GMAC_MAC_MDIO_Address	0x0200	W	0x00000000	The MDIO Address register controls the management cycles to external PHY through a management interface
GMAC_MAC_MDIO_Data	0x0204	W	0x00000000	The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address
GMAC_MAC_ARP_Address	0x0210	W	0x00000000	The ARP Address register contains the IPv4 Destination Address of the MAC
GMAC_MAC_CSR_SW_Ctrl	0x0230	W	0x00000000	This register contains SW programmable controls for changing the CSR access response and status bits clearing
GMAC_MAC_Ext_Cfg1	0x0238	W	0x00000002	This register contains Split mode control field and offset field for Split Header feature
GMAC_MAC_Address0_High	0x0300	W	0x0000FFFF	The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station
GMAC_MAC_Address0_Low	0x0304	W	0xFFFFFFFF	The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station
GMAC_MMC_Control	0x0700	W	0x00000000	This register establishes the operating mode of MMC
GMAC_MMC_Rx_Interrupt	0x0704	W	0x00000000	Maintains the interrupts generated from all Receive statistics counters
GMAC_MMC_Tx_Interrupt	0x0708	W	0x00000000	Maintains the interrupts generated from all Transmit statistics counters
GMAC_MMC_Rx_Interrupt_Mask	0x070C	W	0x00000000	This register maintains the masks for interrupts generated from all Receive statistics counters
GMAC_MMC_Tx_Interrupt_Mask	0x0710	W	0x00000000	This register maintains the masks for interrupts generated from all Transmit statistics counters

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Name	Offset	Size	Reset Value	Description
GMAC_Tx_Octet_Count_Good_Bad	0x0714	W	0x00000000	This register provides the number of bytes transmitted by the DWC_ether_qos, exclusive of preamble and retried bytes, in good and bad packets
GMAC_Tx_Packet_Count_Good_Bad	0x0718	W	0x00000000	This register provides the number of good and bad packets, exclusive of retried packets
GMAC_Tx_Underflow_Error_Packets	0x0748	W	0x00000000	This register provides the number of packets aborted because of packets underflow error
GMAC_Tx_Carrier_Error_Packets	0x0760	W	0x00000000	This register provides the number of packets aborted because of carrier sense error (no carrier or loss of carrier)
GMAC_Tx_Octet_Count_Good	0x0764	W	0x00000000	This register provides the number of bytes exclusive of preamble, only in good packets
GMAC_Tx_Packet_Count_Good	0x0768	W	0x00000000	This register provides the number of good packets transmitted by DWC_ether_qos
GMAC_Tx_Pause_Packets	0x0770	W	0x00000000	This register provides the number of good Pause packets by DWC_ether_qos
GMAC_Rx_Packets_Count_Good_Bad	0x0780	W	0x00000000	This register provides the number of good and bad packets received by DWC_ether_qos
GMAC_Rx_Octet_Count_Good_Bad	0x0784	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, in good and bad packets
GMAC_Rx_Octet_Count_Good	0x0788	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, only in good packets
GMAC_Rx_Multicast_Packets_Good	0x0790	W	0x00000000	This register provides the number of good multicast packets received by DWC_ether_qos
GMAC_Rx_CRC_Error_Packets	0x0794	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with CRC error
GMAC_Rx_Length_Error_Packets	0x07C8	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with length error (Length Type field not equal to packet size), for all packets with valid length field
GMAC_Rx_Pause_Packets	0x07D0	W	0x00000000	This register provides the number of good and valid Pause packets received by DWC_ether_qos
GMAC_Rx_FIFO_Overflow_Packets	0x07D4	W	0x00000000	This register provides the number of missed received packets because of FIFO overflow

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Name	Offset	Size	Reset Value	Description
GMAC_MMC_IPC_Rx_Interrupt_Mask	0x0800	W	0x00000000	This register maintains the mask for the interrupt generated from the receive IPC statistic counters
GMAC_MMC_IPC_Rx_Interrupt	0x0808	W	0x00000000	This register maintains the interrupt that the receive IPC statistic counters generate
GMAC_RxIPv4_Good_Packets	0x0810	W	0x00000000	This register provides the number of good IPv4 datagrams received by DWC_ether_qos with the TCP, UDP, or ICMP payload
GMAC_RxIPv4_Header_Error_Packets	0x0814	W	0x00000000	This register provides the number of IPv4 datagrams received by DWC_ether_qos with header (checksum, length, or version mismatch) errors
GMAC_RxIPv6_Good_Packets	0x0824	W	0x00000000	This register provides the number of good IPv6 datagrams received by DWC_ether_qos
GMAC_RxIPv6_Header_Error_Packets	0x0828	W	0x00000000	This register provides the number of IPv6 datagrams received by DWC_ether_qos with header (length or version mismatch) errors
GMAC_RxUDP_Error_Packets	0x0834	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose UDP payload has a checksum error
GMAC_RxTCP_Error_Packets	0x083C	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose TCP payload has a checksum error
GMAC_RxICMP_Error_Packets	0x0844	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose ICMP payload has a checksum error
GMAC_RxIPv4_Header_Error_Octets	0x0854	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv4 data_grams with header errors (checksum, length, version mismatch)
GMAC_RxIPv6_Header_Error_Octets	0x0868	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv6 data_grams with header errors (length, version mismatch)
GMAC_RxUDP_Error_Octets	0x0874	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a UDP segment that had checksum errors
GMAC_RxTCP_Error_Octets	0x087C	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a TCP segment that had checksum errors

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Name	Offset	Size	Reset Value	Description
GMAC_RxICMP_Error_Octets	0x0884	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a good ICMP segment
GMAC_MTL_Operation_Mode	0x0C00	W	0x00000000	The Operation Mode register establishes the Transmit and Receive operating modes and commands
GMAC_MTL_DBG_CTL	0x0C08	W	0x00000000	The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access
GMAC_MTL_DBG_STS	0x0C0C	W	0x02000000	The FIFO Debug Status register contains the status of FIFO debug access
GMAC_MTL_FIFO_Debug_Data	0x0C10	W	0x00000000	The FIFO Debug Data register contains the data to be written to or read from the FIFOs
GMAC_MTL_Interrupt_Status	0x0C20	W	0x00000000	The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC
GMAC_MTL_TxQ0_Operation_Mode	0x0D00	W	0x00000000	The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands
GMAC_MTL_TxQ0_Underflow	0x0D04	W	0x00000000	The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush
GMAC_MTL_TxQ0_Debug	0x0D08	W	0x00000000	The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue
GMAC_MTL_Q0_Interrupt_Ctrl_Status	0x0D2C	W	0x00000000	This register contains the interrupt enable and status bits for the queue 0 interrupts
GMAC_MTL_RxQ0_Operation_Mode	0x0D30	W	0x00000000	The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command
GMAC_MTL_RxQ0_Miss_Pkt_Ovf_Cnt	0x0D34	W	0x00000000	The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow
GMAC_MTL_RxQ0_Debug	0x0D38	W	0x00000000	The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_Mode	0x1000	W	0x00000000	The Bus Mode register establishes the bus operating modes for the DMA
GMAC_DMA_SysBus_Mode	0x1004	W	0x00010000	The System Bus mode register controls the behavior of the AHB or AXI master
GMAC_DMA_Interrupt_Status	0x1008	W	0x00000000	The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC
GMAC_DMA_Debug_Status0	0x100C	W	0x00000000	The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose
GMAC_AXI_LPI_Entry_Interval	0x1040	W	0x00000000	This register is used to control the AXI LPI entry interval
GMAC_DMA_CH0_Control	0x1100	W	0x00000000	The register specifies the MSS value for segmentation, length to skip between two descriptors, and 8xPBL mode
GMAC_DMA_CH0_Tx_Control	0x1104	W	0x00000000	The register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights
GMAC_DMA_CH0_Rx_Control	0x1108	W	0x00000000	The DMA Channel0 Receive Control register controls the Rx features such as PBL, buffer size, and extended status
GMAC_DMA_CH0_TxDesc_List_HAddress	0x1110	W	0x00000000	The Channel0 Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list
GMAC_DMA_CH0_TxDesc_List_Address	0x1114	W	0x00000000	The Channel0 Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list
GMAC_DMA_CH0_RxDesc_List_HAaddress	0x1118	W	0x00000000	The Channel0 Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list
GMAC_DMA_CH0_RxDesc_List_Address	0x111C	W	0x00000000	The Channel0 Rx Descriptor List Address register points the DMA to the start of Receive descriptor list
GMAC_DMA_CH0_TxDesc_Tail_Pointer	0x1120	W	0x00000000	The Channel0 Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH0_RxDesc_Tail_Pointer	0x1128	W	0x00000000	The Channel0 Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_TxDesc_Ring_Length	0x112C	W	0x00000000	The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring
GMAC_DMA_CH0_RxDesc_Ring_Length	0x1130	W	0x00000000	The Channel0 Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring
GMAC_DMA_CH0_Interrupt_Enable	0x1134	W	0x00000000	The Channel0 Interrupt Enable register enables the interrupts reported by the Status register
GMAC_DMA_CH0_Rx_Interrupt_Watchdog_Timer	0x1138	W	0x00000000	The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA
GMAC_DMA_CH0_Current_App_TxDesc	0x1144	W	0x00000000	The Channel0 Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA
GMAC_DMA_CH0_Current_App_RxDesc	0x114C	W	0x00000000	The Channel0 Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA
GMAC_DMA_CH0_Curren_App_TxBuffer_H	0x1150	W	0x00000000	The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA
GMAC_DMA_CH0_Current_App_TxBuffer	0x1154	W	0x00000000	The Channel0 Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA
GMAC_DMA_CH0_Current_App_RxBuffer_H	0x1158	W	0x00000000	The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA
GMAC_DMA_CH0_Current_App_RxBuffer	0x115C	W	0x00000000	The Channel0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA
GMAC_DMA_CH0_Status	0x1160	W	0x00000000	The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA
GMAC_DMA_CH0_Miss_Frame_Cnt	0x1164	W	0x00000000	This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH$i_Rx_Control register

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_RX_ERI_Cnt	0x1168	W	0x00000000	The DMA_CH0_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

8.4.2 Detail Registers Description

GMAC_MAC_Configuration

Address: Operational Base(0xFFA80000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	ARPEN ARP Offload Enable When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. Values: 1'b0: ARP Offload is disabled 1'b1: ARP Offload is enabled
30:28	RO	0x0	reserved
27	RW	0x0	IPC Checksum Offload When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled.The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. Values: 1'b0: IP header/payload checksum checking is disabled 1'b1: IP header/payload checksum checking is enabled
26:24	RW	0x0	IPG Inter-Packet Gap These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. Values: 3'b000: 96 bit times IPG 3'b001: 88 bit times IPG 3'b010: 80 bit times IPG 3'b011: 72 bit times IPG 3'b100: 64 bit times IPG 3'b101: 56 bit times IPG

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Bit	Attr	Reset Value	Description
			3'b110: 48 bit times IPG 3'b111: 40 bit times IPG
23	RW	0x0	GPSLCE Giant Packet Size Limit Control Enable When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet). The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. Values: 1'b0: Giant Packet Size Limit Control is disabled 1'b1: Giant Packet Size Limit Control is enabled
22	RW	0x0	S2KP IEEE 802.3as Support for 2K Packets When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. Values: 1'b0: Support upto 2K packet is disabled 1'b1: Support upto 2K packet is Enabled
21	RW	0x0	CST CRC stripping for Type packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. Note: For information about how the settings of the ACS bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bits. Values: 1'b0: CRC stripping for Type packets is disabled 1'b1: CRC stripping for Type packets is enabled
20	RW	0x0	ACS Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field.When this bit is reset, the MAC passes all incoming packets to the application, without any modification. Note: For information about how the settings of CST bit and this

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Bit	Attr	Reset Value	Description
			bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bit. Values: 1'b0: Automatic Pad or CRC Stripping is disabled 1'b1: Automatic Pad or CRC Stripping is enabled
19	RW	0x0	WD Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. Values: 1'b0: Watchdog is enabled 1'b1: Watchdog is disabled
18:17	RO	0x0	reserved
16	RW	0x0	JE Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. Values: 1'b0: Jumbo packet is disabled 1'b1: Jumbo packet is enabled
15	RW	0x1	PS Port Select This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). The mac_speed_o[1] signal reflects the value of this bit. Values: 1'b0: For 1000 or 2500 Mbps operations 1'b1: For 10 or 100 Mbps operations
14	RO	0x0	reserved
13	RW	0x0	DM Duplex Mode When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. Values: 1'b0: Half-duplex mode 1'b1: Full-duplex mode
12	RW	0x0	LM Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. Values: 1'b0: Loopback is disabled 1'b1: Loopback is enabled
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	DCRS Disable Carrier Sense During Transmission When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. Values: 1'b0: Enable Carrier Sense During Transmission 1'b1: Disable Carrier Sense During Transmission
8	RW	0x0	DR Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status.When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. Values: 1'b0: Enable Retry 1'b1: Disable Retry
7	RO	0x0	reserved
6:5	RW	0x0	BL Back-Off Limit The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. Values: 2'b00: k = min(n,10) 2'b01: k = min(n,8) 2'b10: k = min(n,4) 2'b11: k = min(n,1)
4	RW	0x0	DC Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the

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Bit	Attr	Reset Value	Description
			MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. Values: 1'b0: Deferral check function is disabled 1'b1: Deferral check function is enabled
3:2	RW	0x0	PRELEN Preamble Length for Transmit packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. Values: 2'b00: 7 bytes of preamble 2'b01: 5 bytes of preamble 2'b10: 3 bytes of preamble 2'b11: Reserved
1	RO	0x0	reserved
0	RW	0x0	RE Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. Values: 1'b0: Receiver is disabled 1'b1: Receiver is enabled

GMAC_MAC_Ext_Configuration

Address: Operational Base(0xFFA80000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	EIPG Extended Inter-Packet Gap The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times

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Bit	Attr	Reset Value	Description
24	RW	0x0	EIPGEN Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. Values: 1'b0: Extended Inter-Packet Gap is disabled 1'b1: Extended Inter-Packet Gap is enabled
23	RO	0x0	reserved
22:20	RW	0x0	HDSMS Maximum Size for Splitting the Header Data These bits indicate the maximum header size allowed for splitting the header data in the received packet. Values: 0x0 (64BYTES): Maximum Size for Splitting the Header Data is 64 bytes 0x1 (128BYTES): Maximum Size for Splitting the Header Data is 128 bytes 0x2 (256BYTES): Maximum Size for Splitting the Header Data is 256 bytes 0x3 (512BYTES): Maximum Size for Splitting the Header Data is 512 bytes 0x4 (1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes 0x5 (RSVD): Reserved
19	RO	0x0	reserved
18	RW	0x0	USP Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. Values: 1'b0: Unicast Slow Protocol Packet Detection is disabled 1'b1: Unicast Slow Protocol Packet Detection is enabled
17	RW	0x0	SPEN Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. Values: 1'b0: Slow Protocol Detection is disabled

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Bit	Attr	Reset Value	Description
			1'b1: Slow Protocol Detection is enabled
16	RW	0x0	DCRCC Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. Values: 1'b0: CRC Checking is enabled 1'b1: CRC Checking is disabled
15:14	RO	0x0	reserved
13:0	RW	0x0000	GPSL Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

GMAC_MAC_Packet_Filter

Address: Operational Base(0xFFA80000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	RA Receive All When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled 0x1 (ENABLE): Receive All is enabled
30:17	RO	0x0000	reserved
16	RW	0x0	VTFE VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. Values: 1'b0: VLAN Tag Filter is disabled 1'b1: VLAN Tag Filter is enabled
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	HPF Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. Values: 1'b0: Hash or Perfect Filter is disabled 2'b1: Hash or Perfect Filter is enabled
9:8	RO	0x0	reserved
7:6	RW	0x0	PCF Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets). Values: 2'b00: MAC filters all control packets from reaching the application 2'b01: MAC forwards all control packets except Pause packets to the application even if they fail the Address filter 2'b10: MAC forwards all control packets to the application even if they fail the Address filter 2'b11: MAC forwards the control packets that pass the Address filter
5	RW	0x0	DBF Disable Broadcast Packets When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. Values: 1'b0: Enable Broadcast Packets 1'b1: Disable Broadcast Packets
4	RW	0x0	PM Pass All Multicast When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. Values: 1'b0: Pass All Multicast is disabled 1'b1: Pass All Multicast is enabled
3	RW	0x0	DAIF DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. Values: 1'b0: DA Inverse Filtering is disabled 1'b1: DA Inverse Filtering is enabled

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Bit	Attr	Reset Value	Description
2	RW	0x0	HMC Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. Values: 1'b0: Hash Multicast is disabled 1'b1: Hash Multicast is enabled
1:0	RO	0x0	reserved

GMAC_MAC_Watchdog_Timeout

Address: Operational Base(0xFFA80000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	PWE Programmable Watchdog Enable When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. Values: 1'b0: Programmable Watchdog is disabled 1'b1: Programmable Watchdog is enabled
7:4	RO	0x0	reserved
3:0	RW	0x0	WTO Watchdog Timeout When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. Values: 4'b0000: 2 KB 4'b0001: 3 KB 4'b0010: 4 KB 4'b0011: 5 KB 4'b0100: 6 KB 4'b0101: 7 KB 4'b0110: 8 KB 4'b0111: 9 KB 4'b1000: 10 KB 4'b1001: 11 KB 4'b1010: 12 KB 4'b1011: 13 KB 4'b1100: 14 KB 4'b1101: 15 KB 4'b1110: 16383 Bytes 4'b1111: Reserved

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GMAC_MAC_Hash_Table_Reg0

Address: Operational Base(0xFFA80000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT31T0 MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determine the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way: 1. Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32). 2. Perform bitwise reversal for the value obtained in Step 1. 3. Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_Hash_Table_Reg1

Address: Operational Base(0xFFA80000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT63T32 MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table.

GMAC_MAC_VLAN_Tag

Address: Operational Base(0xFFA80000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	EVLRXS Enable VLAN Tag in Rx status When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. Values: 1'b0: VLAN Tag in Rx status is disabled 1'b1: VLAN Tag in Rx status is enabled
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:21	RW	0x0	EVLS Enable VLAN Tag Stripping on Receive This field indicates the stripping operation on the outer VLAN Tag in received packet. Values: 2'b00: Do not strip 2'b01: Strip if VLAN filter passes 2'b10: Strip if VLAN filter fails 2'b11: Always strip
20	RW	0x0	DOVLTC Disable VLAN Type Check When this bit is set, the MAC does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. Values: 1'b0: VLAN Type Check is enabled 1'b1: VLAN Type Check is disabled
19	RW	0x0	ERSVLM Enable Receive S-VLAN Match When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for filtering or matching. Values: 1'b0: Receive S-VLAN Match is disabled 1'b1: Receive S-VLAN Match is enabled
18	RW	0x0	ESVL Enable S-VLAN When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. Values: 1'b0: S-VLAN is disabled 1'b1: S-VLAN is enabled
17	RW	0x0	VTIM VLAN Tag Inverse Match Enable When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. Values: 1'b0: VLAN Tag Inverse Match is disabled 1'b1: VLAN Tag Inverse Match is enabled
16	RW	0x0	ETV Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. Similarly, when enabled, only 12 bits of the VLAN tag in the received packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for

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Bit	Attr	Reset Value	Description
			comparison and VLAN hash filtering. Values: 1'b0: 12-Bit VLAN Tag Comparison is disabled 1'b1: 12-Bit VLAN Tag Comparison is enabled
15:0	RW	0x0000	VL VLAN Tag Identifier for Receive Packets This field contains the 802.1Q VLAN tag to identify the VLAN packets. This VLAN tag identifier is compared to the 15th and 16th bytes of the packets being received for VLAN packets. The following list describes the bits of this field: 1. Bits[15:13]: User Priority 2. Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) 3. Bits[11:0]: VLAN Identifier (VID) field of VLAN tag When the ETV bit is set, only the VID is used for comparison. If this field ([11:0] if ETV is set) is all zeros, the MAC does not check the 15th and 16th bytes for VLAN tag comparison and declares all packets with Type field value of 0x8100 or 0x88a8 as VLAN packets.

GMAC_MAC_VLAN_Hash_Table

Address: Operational Base(0xFFA80000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	VLHT VLAN Hash Table This field contains the 16-bit VLAN Hash Table. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. When ETV bit of MAC_VLAN_Tag register is set, the upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. When ETV bit of MAC_VLAN_Tag register is reset, the ones-complement of upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. For example, when ETV bit is set a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table, whereas when ETV bit is reset a hash value of 4b'1000 selects Bit 7 of the VLAN Hash table. The hash value of the destination address is calculated in the following way: 1.Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3). 2.Perform bitwise reversal for the value obtained in step 1. 3.Take the upper four bits from the value obtained in step 2. If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] (in little-endian mode) or Bits[7:0] (in big-endian mode) of this register are written. 1.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_Q0_Tx_Flow_Ctrl

Address: Operational Base(0xFFA80000) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PT Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	RO	0x00	reserved
7	RW	0x0	DZPQ Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. Values: 1'b0: Zero-Quanta Pause packet generation is enabled 1'b1: Zero-Quanta Pause packet generation is disabled
6:2	RO	0x00	reserved
1	RW	0x0	TFE Transmit Flow Control Enable Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. Values: 1'b0: Transmit Flow Control is disabled 1'b1: Transmit Flow Control is enabled
0	RW	0x0	FCB_BPA Flow Control Busy or Backpressure Activate This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

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Bit	Attr	Reset Value	Description
			Values: 1'b0: Flow Control Busy or Backpressure Acti_vate is disabled 1'b1: Flow Control Busy or Backpressure Acti_vate is enabled

GMAC_MAC_Rx_Flow_Ctrl

Address: Operational Base(0xFFA80000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	UP Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. Values: 1'b0: Unicast Pause Packet Detect disabled 1'b1: Unicast Pause Packet Detect enabled
0	RW	0x0	RFE Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. Values: 1'b0: Receive Flow Control is disabled 1'b1: Receive Flow Control is enabled

GMAC_MAC_Interrupt_Status

Address: Operational Base(0xFFA80000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	MDIOIS MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: MDIO Interrupt status not active 1'b1: MDIO Interrupt status active
17:15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RO	0x0	RXSTSIS Receive Status Interrupt This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Receive Interrupt status not active 1'b1: Receive Interrupt status active
13	RO	0x0	TXSTSIS Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: 1. Excessive Collision (EXCOL) 2. Late Collision (LCOL) 3. Excessive Deferral (EXDEF) 4. Loss of Carrier (LCARR) 5. No Carrier (NCARR) 6. Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Transmit Interrupt status not active 1'b1: Transmit Interrupt status active
12	RO	0x0	reserved
11	RO	0x0	MMCRXIPIS MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. Values: 1'b0: MMC Receive Checksum Offload Inter_rupt status not active 1'b1: MMC Receive Checksum Offload Interrupt status active
10	RO	0x0	MMCTXIS MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Transmit Interrupt status not active 1'b1: MMC Transmit Interrupt status active

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Bit	Attr	Reset Value	Description
9	RO	0x0	MMCRXIS MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Receive Interrupt status not active 1'b1: MMC Receive Interrupt status active
8	RO	0x0	MMCIS MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Interrupt status not active 1'b1: MMC Interrupt status active
7:6	RO	0x0	reserved
5	RO	0x0	LPIIS LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 0x0 (INACTIVE): LPI Interrupt status not active 0x1 (ACTIVE): LPI Interrupt status active
4	RO	0x0	PMTIS PMT Interrupt Status This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. Values: 1'b0: PMT Interrupt status not active 1'b1: PMT Interrupt status active
3	RO	0x0	PHYIS PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: PHY Interrupt not detected 1'b1: PHY Interrupt detected
2:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	RGSMIIIS RGMII or SMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. Values: 0x0 (INACTIVE): RGMII or SMII Interrupt Status is not active 0x1 (ACTIVE): RGMII or SMII Interrupt Status is active

GMAC_MAC_Interrupt_Enable

Address: Operational Base(0xFFA80000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	MDIOIE MDIO Interrupt Enable When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. Values: 1'b0: MDIO Interrupt is disabled 1'b1: MDIO Interrupt is enabled
17:15	RO	0x0	reserved
14	RW	0x0	RXSTSIE Receive Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Receive Status Interrupt is disabled 1'b1: Receive Status Interrupt is enabled
13	RW	0x0	TXSTSIE Transmit Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Timestamp Status Interrupt is disabled 1'b1: Timestamp Status Interrupt is enabled
12:6	RO	0x00	reserved
5	RW	0x0	LPIIE LPI Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. Values: 0x0 (DISABLE): LPI Interrupt is disabled 0x1 (ENABLE): LPI Interrupt is enabled

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Bit	Attr	Reset Value	Description
4	RW	0x0	PMTIE PMT Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. Values: 1'b0: PMT Interrupt is disabled 1'b1: PMT Interrupt is enabled
3	RW	0x0	PHYIE PHY Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. Values: 1'b0: PHY Interrupt is disabled 1'b1: PHY Interrupt is enabled
2:1	RO	0x0	reserved
0	RW	0x0	RGSMIIIE RGMII or SMII Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. Values: 0x0 (DISABLE): RGMII or SMII Interrupt is disabled 0x1 (ENABLE): RGMII or SMII Interrupt is enabled

GMAC_MAC_Rx_Tx_Status

Address: Operational Base(0xFFA80000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	RWT Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No receive watchdog timeout 1'b1: Receive watchdog timed out
7:5	RO	0x0	reserved
4	RO	0x0	LCOL Late Collision When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values:

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Bit	Attr	Reset Value	Description
			1'b0: No collision 1'b1: Late collision is sensed
3	RO	0x0	EXDEF Excessive Deferral When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Excessive deferral 1'b1: Excessive deferral
2	RO	0x0	LCARR Loss of Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: Loss of carrier
1	RO	0x0	NCARR No Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: No carrier
0	RO	0x0	TJT Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Transmit Jabber Timeout 1'b1: Transmit Jabber Timeout occurr

GMAC_MAC_PMT_Control_Status

Address: Operational Base(0xFFA80000) + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31	RW	0x0	RWKFILTRST Remote Wake-Up Packet Filter Register Pointer Reset When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-Up Packet Filter Register Pointer is not Reset 1'b1: Remote Wake-Up Packet Filter Register Pointer is Reset
30:29	RO	0x0	reserved
28:24	RO	0x00	RWKPTR Remote Wake-up FIFO Pointer This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	RO	0x0000	reserved
10	RW	0x0	RWKPFE Remote Wake-up Packet Forwarding Enable When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-up Packet Forwarding is disabled 1'b1: Remote Wake-up Packet Forwarding is enabled
9	RW	0x0	GLBLUCAST Global Unicast When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. Values: 1'b0: Global unicast is disabled 1'b1: Global unicast is enabled
8:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RO	0x0	RWKPRCVD Remote Wake-Up Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Remote wake-up packet is received 1'b1: Remote wake-up packet is received
5	RO	0x0	MGKPRCVD Magic Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Magic packet is received 1'b1: Magic packet is received
4:3	RO	0x0	reserved
2	RW	0x0	RWKPKTEN Remote Wake-Up Packet Enable When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. Values: 1'b0: Remote wake-up packet is disabled 1'b1: Remote wake-up packet is enabled
1	RW	0x0	MGKPKTEN Magic Packet Enable When this bit is set, a power management event is generated when the MAC receives a magic packet. Values: 1'b0: Magic Packet is disabled 1'b1: Magic Packet is enabled
0	RW	0x0	PWRDWN Power Down When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Power down is disabled 1'b1: Power down is enabled

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GMAC_MAC_RWK_Packet_Filter

Address: Operational Base(0xFFA80000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	WKUPFRMFTR(cont.) (4) If filters chained by And_Previous bit setting have complementary programming, then a frame may never pass the AND chained filter. For example, if Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 1 Address_Type bit is set (bit 3 in Filter 1 command is set) indicating multicast detection and Filter 2 Address_Type bit is reset (bit 3 in Filter 2 command is reset) indicating unicast detection or vice versa, a remote wakeup frame does not pass the AND chained filter as a remote wakeup frame cannot be of both unicast and multicast address type. 4. Bit 0 is the enable for filter i. If Bit 0 is not set, filter i is disabled. Filter i Byte Mask: The filter i byte mask register defines the bytes of the packet that are examined by filter i (0, 1, 2, 3, .., 15) to determine whether or not a packet is a wake-up packet. 1. The MSB (31st bit) must be zero. 2. Bit j[30:0] is the byte mask. 3. If Bit j (byte number) of the byte mask is set, the CRC block processes the Filter i Offset + j of the incoming packet; otherwise Filter i Offset + j is ignored. Filter i Offset: The filter i offset register defines the offset (within the packet) from which the filter i examines the packets. 1. This 8-bit pattern-offset is the offset for the filter i first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet. Filter i CRC-16: The filter i CRC-16 register contains the CRC-16 value calculated from the pattern and the byte mask programmed in the Remote Wakeup filter register. 1. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1 2. Each mask, used in the hash function calculation, is compared with a 16-bit value associated with that mask. Each filter has the following: (1)32-bit Mask: Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC16 calculation. (2) 8-bit Offset Pointer: Specifies the byte to start the CRC-16 computation. The pointer and the mask are used together to locate the bytes to be used in the CRC-16 calculations.

GMAC_MAC_LPI_Control_Status

Address: Operational Base(0xFFA80000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	LPITCSE LPI Tx Clock Stop Enable When this bit is set, the MAC asserts sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode to indicate that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not assert sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. Values: 0x0 (DISABLE): LPI Tx Clock Stop is disabled 0x1 (ENABLE): LPI Tx Clock Stop is enabled
20	RW	0x0	LPIATE LPI Timer Enable This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. Values: 0x0 (DISABLE): LPI Timer is disabled 0x1 (ENABLE): LPI Timer is enabled
19	RW	0x0	LPITXA LPI Tx Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the GMAC-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode.When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. Values: 0x0 (DISABLE): LPI Tx Automate is disabled 0x1 (ENABLE): LPI Tx Automate is enabled

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Bit	Attr	Reset Value	Description
18	RW	0x0	PLSEN PHY Link Status Enable This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. Values: 0x0 (DISABLE): PHY Link Status is disabled 0x1 (ENABLE): PHY Link Status is enabled
17	RW	0x0	PLS PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. Values: 0x0 (DISABLE): link is down 0x1 (ENABLE): link is okay (UP)
16	RW	0x0	LPIEN LPI Enable When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. Values: 0x0 (DISABLE): LPI state is disabled 0x1 (ENABLE): LPI state is enabled
15:10	RO	0x00	reserved
9	RO	0x0	RLPIST Receive LPI State When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. Values: 0x0 (INACTIVE): Receive LPI state not detected 0x1 (ACTIVE): Receive LPI state detected
8	RO	0x0	TLPIST Transmit LPI State When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. Values: 0x0 (INACTIVE): Transmit LPI state not detected 0x1 (ACTIVE): Transmit LPI state detected
7:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3	RO	0x0	RLPIEX Receive LPI Exit When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. Values: 0x0 (INACTIVE): Receive LPI exit not detected 0x1 (ACTIVE): Receive LPI exit detected
2	RO	0x0	RLPIEN Receive LPI Entry When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. Values: 0x0 (INACTIVE): Receive LPI entry not detected 0x1 (ACTIVE): Receive LPI entry detected
1	RO	0x0	TLPIEX Transmit LPI Exit When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Values: 0x0 (INACTIVE): Transmit LPI exit not detected 0x1 (ACTIVE): Transmit LPI exit detected
0	RO	0x0	TLPIEN Transmit LPI Entry When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Values: 0x0 (INACTIVE): Transmit LPI entry not detected 0x1 (ACTIVE): Transmit LPI entry detected

GMAC_MAC_LPI_Timers_Control

Address: Operational Base(0xFFA80000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x3e8	LST LPI LS Timer This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	RW	0x0000	TWT LPI TW Timer This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

GMAC_MAC_LPI_Entry_Timer

Address: Operational Base(0xFFA80000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:3	RW	0x00000	LPIET LPI Entry Timer This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	RO	0x0	reserved

GMAC_MAC_1US_Tic_Counter

Address: Operational Base(0xFFA80000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x063	TIC_1US_CNTR 1US TIC Counter The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example, if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

GMAC_MAC_PHYIF_Control_Status

Address: Operational Base(0xFFA80000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RO	0x0	LNKSTS Link Status This bit indicates whether the link is up (1'b1) or down (1'b0). Values: 0x0 (INACTIVE): Link down 0x1 (ACTIVE): Link up

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Bit	Attr	Reset Value	Description
18:17	RO	0x0	LNKSPEED Link Speed This bit indicates the current speed of the link. Bit 2 is reserved when the MAC is configured for the SMII PHY interface. Values: 0x0 (2500K): 2.5 MHz 0x1 (25M): 25 MHz 0x2 (125M): 125 MHz 0x3 (RSVD): Reserved
16	RO	0x0	LNKMOD Link Mode This bit indicates the current mode of operation of the link. Values: 0x0 (HDUPLX): Half-duplex mode 0x1 (FDUPLX): Full-duplex mode
15:2	RO	0x0000	reserved
1	RW	0x0	LUD Link Up or Down This bit indicates whether the link is up or down during transmission of configuration in the RGMII, SGMII, or SMII interface. Values: 0x0 (LINKDOWN): Link down 0x1 (LINKUP): Link up
0	RW	0x0	TC Transmit Configuration in RGMII, SGMII, or SMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: "Reduced Gigabit Media Independent Interface" "Serial Media Independent Interface" "Serial Gigabit Media Independent Interface" Values: 0x0 (DISABLE): Disable Transmit Configuration in RGMII, SGMII, or SMII 0x1 (ENABLE): Enable Transmit Configuration in RGMII, SGMII, or SMII

GMAC_MAC_Version

Address: Operational Base(0xFFA80000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x40	USERVER User-defined Version
7:0	RW	0x51	RKVER Rockchip-defined Version

GMAC_MAC_Debug

Address: Operational Base(0xFFA80000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
18:17	RO	0x0	TFCSTS MAC Transmit Packet Controller Status This field indicates the state of the MAC Transmit Packet Controller module. Values: 2'b00: Idle state 2'b01: Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over 2'b10: Generating and transmitting a Pause control packet (in full-duplex mode) 2'b11: Transferring input packet for transmission
16	RO	0x0	TPESTS MAC GMII or MII Transmit Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. Values: 1'b0: MAC GMII or MII Transmit Protocol Engine Status not detected 1'b1: MAC GMII or MII Transmit Protocol Engine Status detected
15:3	RO	0x0000	reserved
2:1	RO	0x0	RFCFCSTS MAC Receive Packet Controller FIFO Status When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	RO	0x0	RPESTS MAC GMII or MII Receive Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. Values: 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected

GMAC_MAC_HW_Feature0

Address: Operational Base(0xFFA80000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:28	RO	0x4	ACTPHYSEL Active PHY Selected When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. Values: 4'b0000: GMII or MII 4'b0001: RGMII 4'b0010: SGMII 4'b0011: TBI 4'b0100: RMII 4'b0101: RTBI 4'b0110: SMII 4'b0111: RevMII

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Bit	Attr	Reset Value	Description
27	RO	0x0	SAVLANINS Source Address or VLAN Insertion Enable This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected. Values: 1'b0: Source Address or VLAN Insertion Enable option is not selected 1'b1: Source Address or VLAN Insertion Enable option is selected
26:25	RO	0x0	TSSTSSEL Timestamp System Time Source This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 2'b00: Internal 2'b01: External 2'b10: Both 2'b11: Reserved
24	RO	0x0	reserved
23	RO	0x0	MACADR32SEL MAC Addresses 32-63 Selected This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected. Values: 1'b0: MAC Addresses 32-63 Select option is not selected 1'b1: MAC Addresses 32-63 Select option is selected
22:18	RO	0x00	ADDMACADRSEL MAC Addresses 1-31 Selected This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option.
17	RO	0x0	reserved
16	RO	0x1	RXCOESEL Receive Checksum Offload Enabled This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected. Values: 1'b0: Receive Checksum Offload Enable option is not selected 1'b1: Receive Checksum Offload Enable option is selected
15:14	RO	0x0	reserved
13	RO	0x1	EEESEL Energy Efficient Ethernet Enabled This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected. Values: 1'b0: Energy Efficient Ethernet Enable option is not selected 1'b1: Energy Efficient Ethernet Enable option is selected
12	RO	0x0	TSSEL IEEE 1588-2008 Timestamp Enabled This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 1'b0: IEEE 1588-2008 Timestamp Enable option is not selected. 1'b1: IEEE 1588-2008 Timestamp Enable option is selected.
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RO	0x1	ARPOFFSEL ARP Offload Enabled This bit is set to 1 when the Enable IPv4 ARP Offload option is selected. Values: 1'b0: ARP Offload Enable option is not selected 1'b1: ARP Offload Enable option is selected
8	RO	0x1	MMCSEL RMON Module Enable This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected. Values: 1'b0: RMON Module Enable option is not selected 1'b1: RMON Module Enable option is selected
7	RO	0x1	MGKSEL PMT Magic Packet Enable This bit is set to 1 when the Enable Magic Packet Detection option is selected. Values: 1'b0: PMT Magic Packet Enable option is not selected 1'b1: PMT Magic Packet Enable option is selected
6	RO	0x1	RWKSEL PMT Remote Wake-up Packet Enable This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected. Values: 1'b0: PMT Remote Wake-up Packet Enable option is not selected 1'b1: PMT Remote Wake-up Packet Enable option is selected
5	RO	0x1	SMASEL SMA (MDIO) Interface This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected. Values: 1'b0: SMA (MDIO) Interface not selected 1'b1: SMA (MDIO) Interface selected
4	RO	0x0	VLHASH VLAN Hash Filter Selected This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected. Values: 1'b0: VLAN Hash Filter not selected 1'b1: VLAN Hash Filter selected
3	RO	0x0	PCSSEL PCS Registers (TBI, SGMII, or RTBI PHY interface) This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected. Values: 1'b0: No PCS Registers (TBI, SGMII, or RTBI PHY interface) 1'b1: PCS Registers (TBI, SGMII, or RTBI PHY interface)
2	RO	0x0	HDSEL Half-duplex Support This bit is set to 1 when the half-duplex mode is selected. Values: 1'b0: No Half-duplex support 1'b1: Half-duplex support

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Bit	Attr	Reset Value	Description
1	RO	0x1	GMIISEL 1000 Mbps Support This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation. Values: 1'b0: No 1000 Mbps support 1'b1: 1000 Mbps support
0	RO	0x1	MIISEL 10 or 100 Mbps Support This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation. Values: 1'b0: No 10 or 100 Mbps support 1'b1: 10 or 100 Mbps support

GMAC_MAC_HW_Feature1

Address: Operational Base(0xFFA80000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RO	0x0	L3L4FNUM Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters: Values: 4'b0000: No L3 or L4 Filter 4'b0001: 1 L3 or L4 Filter 4'b0010: 2 L3 or L4 Filters 4'b0011: 3 L3 or L4 Filters 4'b0100: 4 L3 or L4 Filters 4'b0101: 5 L3 or L4 Filters 4'b0110: 6 L3 or L4 Filters 4'b0111: 7 L3 or L4 Filters 4'b1000: 8 L3 or L4 Filters
26	RO	0x0	reserved
25:24	RO	0x1	HASHTBLSZ Hash Table Size This field indicates the size of the hash table: Values: 2'b00: No hash table 2'b01: 64 2'b10: 128 2'b11: 256
23	RO	0x0	POUOST One Step for PTP over UDP/IP Feature Enable This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. Values: 1'b0: One Step for PTP over UDP/IP Feature is not selected 1'b1: One Step for PTP over UDP/IP Feature is selected
22	RO	0x0	reserved
21	RO	0x0	RAVSEL Rx Side Only AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. Values: 1'b0: Rx Side Only AV Feature is not selected 1'b1: Rx Side Only AV Feature is selected

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Bit	Attr	Reset Value	Description
20	RO	0x0	AVSEL AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option is selected. Values: 1'b0: AV Feature is not selected 1'b1: AV Feature is selected
19	RO	0x1	DBGMEMA DMA Debug Registers Enable This bit is set to 1 when the Debug Mode Enable option is selected. Values: 1'b0: DMA Debug Registers option is not selected 1'b1: DMA Debug Registers option is selected
18	RO	0x1	TSOEN TCP Segmentation Offload Enable This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected. Values: 1'b0: TCP Segmentation Offload Feature is not selected 1'b1: TCP Segmentation Offload Feature is selected
17	RO	0x1	SPHEN Split Header Feature Enable This bit is set to 1 when the Enable Split Header Structure option is selected. Values: 1'b0: Split Header Feature is not selected 1'b1: Split Header Feature is selected
16	RO	0x0	DCBEN DCB Feature Enable This bit is set to 1 when the Enable Data Center Bridging option is selected. Values: 1'b0: DCB Feature is not selected 1'b1: DCB Feature is selected
15:14	RO	0x1	ADDR64 Address Width This field indicates the configured address width: Values: 2'b00: 32 2'b01: 40 2'b10: 48 2'b11: Reserved
13	RO	0x0	reserved
12	RO	0x0	PTOEN PTP Offload Enable This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. Values: 1'b0: PTP Offload feature is not selected 1'b1: PTP Offload feature is selected

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Bit	Attr	Reset Value	Description
11	RO	0x0	OSTEN One-Step Timestamping Enable This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. Values: 1'b0: One-Step Timestamping feature is not selected 1'b1: One-Step Timestamping feature is selected
10:6	RO	0x06	TXFIFOSIZE MTL Transmit FIFO Size This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: Values: 0x0 (128B): 128 bytes 0x1 (256B): 256 bytes 0x2 (512B): 512 bytes 0x3 (1024B): 1024 bytes 0x4 (2048B): 2048 bytes 0x5 (4096B): 4096 bytes 0x6 (8192B): 8192 bytes 0x7 (16384B): 16384 bytes 0x8 (32KB): 32 KB 0x9 (64KB): 64 KB 0xa (128KB): 128 KB 0xb (RSVD): Reserved
5	RO	0x1	SPRAM Single Port RAM Enable This bit is set to 1 when the Use single port RAM Feature is selected. Values: 1'b0: Single Port RAM feature is not selected 1'b1: Single Port RAM feature is selected
4:0	RO	0x07	RXFIFOSIZE MTL Receive FIFO Size This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: Values: 5'b00000: 128 bytes 5'b00001: 256 bytes 5'b00010: 512 bytes 5'b00011: 1024 bytes 5'b00100: 2048 bytes 5'b00101: 4096 bytes 5'b00110: 8192 bytes 5'b00111: 16384 bytes 5'b01000: 32 KB 5'b01001: 64 KB 5'b01010: 128 KB 5'b01011: 256 KB 5'b01100: Reserved

GMAC_MAC_HW_Feature2

Address: Operational Base(0xFFA80000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:28	RO	0x1	AUXSNAPNUM Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs: Values: 3'b000: No auxiliary input 3'b001: 1 auxiliary input 3'b010: 2 auxiliary input 3'b011: 3 auxiliary input 3'b100: 4 auxiliary input 3'b101: Reserved
27	RO	0x0	reserved
26:24	RO	0x0	PPSOUTNUM Number of PPS Outputs This field indicates the number of PPS outputs: Values: 3'b000: No PPS output 3'b001: 1 PPS output 3'b010: 2 PPS output 3'b011: 3 PPS output 3'b100: 4 PPS output 3'b101: Reserved
23:22	RO	0x0	reserved
21:18	RO	0x0	TXCHCNT Number of DMA Transmit Channels This field indicates the number of DMA Transmit channels: Values: 4'b0000: 1 MTL Tx Channel 4'b0001: 2 MTL Tx Channels 4'b0010: 3 MTL Tx Channels 4'b0011: 4 MTL Tx Channels 4'b0100: 5 MTL Tx Channels 4'b0101: 6 MTL Tx Channels 4'b0110: 7 MTL Tx Channels 4'b0111: 8 MTL Tx Channels
17:16	RO	0x0	reserved
15:12	RO	0x0	RXCHCNT Number of DMA Receive Channels This field indicates the number of DMA Receive channels: Values: 4'b0000: 1 MTL Rx Channel 4'b0001: 2 MTL Rx Channels 4'b0010: 3 MTL Rx Channels 4'b0011: 4 MTL Rx Channels 4'b0100: 5 MTL Rx Channels 4'b0101: 6 MTL Rx Channels 4'b0110: 7 MTL Rx Channels 4'b0111: 8 MTL Rx Channels
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:6	RO	0x0	TXQCNT Number of MTL Transmit Queues This field indicates the number of MTL Transmit queues: Values: 4'b0000: 1 MTL Tx Queue 4'b0001: 2 MTL Tx Queues 4'b0010: 3 MTL Tx Queues 4'b0011: 4 MTL Tx Queues 4'b0100: 5 MTL Tx Queues 4'b0101: 6 MTL Tx Queues 4'b0110: 7 MTL Tx Queues 4'b0111: 8 MTL Tx Queues
5:4	RO	0x0	reserved
3:0	RO	0x0	RXQCNT Number of MTL Receive Queues This field indicates the number of MTL Receive queues: Values: 4'b0000: 1 MTL Rx Queue 4'b0001: 2 MTL Rx Queues 4'b0010: 3 MTL Rx Queues 4'b0011: 4 MTL Rx Queues 4'b0100: 5 MTL Rx Queues 4'b0101: 6 MTL Rx Queues 4'b0110: 7 MTL Rx Queues 4'b0111: 8 MTL Rx Queues

GMAC_MAC_HW_Feature3

Address: Operational Base(0xFFA80000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RO	0x0	ASP Automotive Safety Package Following are the encoding for the different Safety features. Values: 2'b00: No Safety features selected 2'b01: Only "ECC protection for external memory" feature is selected 2'b10: All the Automotive Safety features are selected without the "Parity Port Enable for external inter_face" feature 2'b11: All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature
27	RO	0x0	TBSSEL Time Based Scheduling Enable This bit is set to 1 when the Time Based Scheduling feature is selected. Values: 1'b0: Time Based Scheduling Enable feature is not selected 1'b1: Time Based Scheduling Enable feature is selected
26	RO	0x0	FPESEL Frame Preemption Enable This bit is set to 1 when the Enable Frame preemption feature is selected. Values: 1'b0: Frame Preemption Enable feature is not selected 1'b1: Frame Preemption Enable feature is selected
25:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:20	RO	0x0	ESTWID Width of the Time Interval field in the Gate Control List This field indicates the width of the Configured Time Interval Field. Values: 2'b00: Width not configured 2'b01: 16 2'b10: 20 2'b11: 24
19:17	RW	0x0	ESTDEP Depth of the Gate Control List This field indicates the depth of Gate Control list expressed as Log2(DWC_GMAC_EST_DEP)-5. Values: 3'b000: No Depth configured 3'b001: 64 3'b010: 128 3'b011: 256 3'b100: 512 3'b101: 1024 3'b110: Reserved
16	RO	0x0	ESTSEL Enhancements to Scheduling Traffic Enable This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. Values: 1'b0: Enable Enhancements to Scheduling Traffic feature is not selected 1'b1: Enable Enhancements to Scheduling Traffic feature is selected
15	RO	0x0	reserved
14:13	RO	0x0	FRPES Flexible Receive Parser Table Entries size This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. Values: 2'b00: 64 Entries 2'b01: 128 Entries 2'b10: 256 Entries 2'b11: Reserved
12:11	RO	0x0	FRPBS Flexible Receive Parser Buffer size This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. Values: 2'b00: 64 Bytes 2'b01: 128 Bytes 2'b10: 256 Bytes 2'b11: Reserved
10:6	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
5	RO	0x0	DVLAN Double VLAN Tag Processing Selected This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. Values: 1'b0: Double VLAN option is not selected 1'b1: Double VLAN option is selected
4	RO	0x0	CBTISEL Queue/Channel based VLAN tag insertion on Tx Enable This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. Values: 1'b0: Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected 1'b1: Enable Queue/Channel based VLAN tag insertion on Tx feature is selected
3	RO	0x0	reserved
2:0	RO	0x0	NRVF Number of Extended VLAN Tag Filters Enabled This field indicates the Number of Extended VLAN Tag Filters selected: Values: 3'b000: No Extended Rx VLAN Filters 3'b001: 4 Extended Rx VLAN Filters 3'b010: 8 Extended Rx VLAN Filters 3'b011: 16 Extended Rx VLAN Filters 3'b100: 24 Extended Rx VLAN Filters 3'b101: 32 Extended Rx VLAN Filters 3'b110: Reserved

GMAC_MAC_MDIO_Address

Address: Operational Base(0xFFA80000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	PSE Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. Values: 1'b0: Preamble Suppression disabled 1'b1: Preamble Suppression enabled

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Bit	Attr	Reset Value	Description
26	RW	0x0	BTB Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. Values: 1'b0: Back to Back transactions disabled 1'b1: Back to Back transactions enabled
25:21	RW	0x00	PA Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. For RevMII, this field gives the PHY Address of the RevMII module. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	RW	0x00	RDA Register/Device Address These bits select the PHY register in selected Clause 22 PHY device. For RevMII, these bits select the CSR register in the RevMII Registers set. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	RO	0x0	reserved
14:12	RW	0x0	NTC Number of Trailing Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.
11:8	RW	0x0	CR CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: 4'b0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 4'b0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 4'b0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 4'b0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 4'b0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 4'b0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 4'b0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 4'b0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5

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Bit	Attr	Reset Value	Description
			MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: 4'b1000: CSR clock/4 4'b1001: CSR clock/6 4'b1010: CSR clock/8 4'b1011: CSR clock/10 4'b1100: CSR clock/12 4'b1101: CSR clock/14 4'b1110: CSR clock/16 4'b1111: CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface.
7:5	RO	0x0	reserved
4	RW	0x0	SKAP Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. Values: 1'b0: Skip Address Packet is disabled 1'b1: Skip Address Packet is enabled
3	RW	0x0	GOC_1 GMII Operation Command 1 This bit is higher bit of the operation command to the PHY or RevMII, GOC_1 and GOC_O is encoded as follows: 2'b00: Reserved 2'b01: Write 2'b10: Post Read Increment Address for Clause 45 PHY 2'b11: Read When Clause 22 PHY or RevMII is enabled, only Write and Read commands are valid. Values: 1'b0: GMII Operation Command 1 is disabled 1'b1: GMII Operation Command 1 is enabled
2	RW	0x0	GOC_0 GMII Operation Command 0 This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. When only RevMII is selected in configuration this bit is read-only and tied to 1. Values: 1'b0: GMII Operation Command 0 is disabled 1'b1: GMII Operation Command 0 is enabled
1	RW	0x0	C45E Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. Values: 1'b0: Clause 45 PHY is disabled 1'b1: Clause 45 PHY is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	GB GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: GMII Busy is disabled 1'b1: GMII Busy is enabled

GMAC_MAC_MDIO_Data

Address: Operational Base(0xFFA80000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	RA Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	RW	0x0000	GD GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

GMAC_MAC_ARP_Address

Address: Operational Base(0xFFA80000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARPPA ARP Protocol Address This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

GMAC_MAC_CSR_SW_Ctrl

Address: Operational Base(0xFFA80000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	RCWE Register Clear on Write 1 Enable When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. Values: 1'b0: Register Clear on Write 1 is disabled 1'b1: Register Clear on Write 1 is enabled

GMAC_MAC_Ext_Cfg1

Address: Operational Base(0xFFA80000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	SPLM Split Mode These bits indicate the mode of splitting the incoming Rx packets. They are Values: 0x0 (L3L4): Split at L3/L4 header 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped 0x3 (RSVD): Reserved
7	RO	0x0	reserved
6:0	RW	0x02	SPLOFST Split Offset These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

GMAC_MAC_Address0_High

Address: Operational Base(0xFFA80000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31	RO	0x0	AE Address Enable This bit is always set to 1. Values: 1'b0: This bit must be always set to 1 1'b1: This bit is always set to 1
30:16	RO	0x0000	reserved
15:0	RW	0xffff	ADDRHI MAC Address0[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_Address0_Low

Address: Operational Base(0xFFA80000) + offset (0x0304)

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Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	ADDRLO MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MMC_Control

Address: Operational Base(0xFFA80000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	UCDBC Update MMC Counters for Dropped Broadcast Packets Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. Values: 1'b0: Update MMC Counters for Dropped Broadcast Packets is disabled 1'b1: Update MMC Counters for Dropped Broadcast Packets is enabled
7:6	RO	0x0	reserved
5	RW	0x0	CNTPRSTLVL Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. Values: 1'b0: Full-Half Preset is disabled 1'b1: Full-Half Preset is enabled
4	RW	0x0	CNTPRST Counters Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters Preset is disabled 1'b1: Counters Preset is enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	CNTFREEZ MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. Values: 1'b0: MMC Counter Freeze is disabled 1'b1: MMC Counter Freeze is enabled
2	RW	0x0	RSTONRD Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. Values: 1'b0: Reset on Read is disabled 1'b1: Reset on Read is enabled
1	RW	0x0	CNTSTOPRO Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value. Values: 1'b0: Counter Stop Rollover is disabled 1'b1: Counter Stop Rollover is enabled
0	RW	0x0	CNTRST Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters are not reset 1'b1: All counters are reset

GMAC_MMC_Rx_Interrupt

Address: Operational Base(0xFFA80000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	RXFOVPIS MMC Receive FIFO Overflow Packet Counter Interrupt Status This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
20	RO	0x0	RXPAUSPIS MMC Receive Pause Packet Counter Interrupt Status This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Pause Packet Counter Inter_rupt Status detected
19	RO	0x0	reserved
18	RO	0x0	RXLENERPIS MMC Receive Length Error Packet Counter Interrupt Status This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive Length Error Packet Counter Interrupt Status detected
17:6	RO	0x000	reserved
5	RO	0x0	RXCRCERPIS MMC Receive CRC Error Packet Counter Interrupt Status This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Status not detecte 1'b1: MMC Receive CRC Error Packet Counter Interrupt Status detected
4	RO	0x0	RXMCGPIS MMC Receive Multicast Good Packet Counter Interrupt Status This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Status detected
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RO	0x0	RXGOCTIS MMC Receive Good Octet Counter Interrupt Status This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Octet Counter Interrupt Status detected
1	RO	0x0	RXGBOCTIS MMC Receive Good Bad Octet Counter Interrupt Status This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Octet Counter Interrupt Status detected
0	RO	0x0	RXGBPKTIS MMC Receive Good Bad Packet Counter Interrupt Status This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Packet Counter Interrupt Status detected

GMAC_MMC_Tx_Interrupt

Address: Operational Base(0xFFA80000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RO	0x0	TXPAUSPIS MMC Transmit Pause Packet Counter Interrupt Status This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected
22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21	RO	0x0	TXGPKTIS MMC Transmit Good Packet Counter Interrupt Status This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Packet Counter Interrupt Status detected
20	RO	0x0	TXGOCTIS MMC Transmit Good Octet Counter Interrupt Status This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Octet Counter Interrupt Status detected
19	RO	0x0	TXCARERPIS MMC Transmit Carrier Error Packet Counter Interrupt Status This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Status detected
18:14	RO	0x00	reserved
13	RO	0x0	TXUFLOWERPIS MMC Transmit Underflow Error Packet Counter Interrupt Status This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Status detected
12:2	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x0	TXGBPKTIS MMC Transmit Good Bad Packet Counter Interrupt Status This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Status detected
0	RO	0x0	TXGBOCTIS MMC Transmit Good Bad Octet Counter Interrupt Status This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Status detected

GMAC_MMC_Rx_Interrupt_Mask

Address: Operational Base(0xFFA80000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	RXFOVPIM MMC Receive FIFO Overflow Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled
20:19	RO	0x0	reserved
18	RW	0x0	RXLENERPIM MMC Receive Length Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Length Error Packet Counter Interrupt Mask is enabled
17:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	RXPAUSPIM MMC Receive Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled
9:6	RO	0x0	reserved
5	RW	0x0	RXCRCERPIM MMC Receive CRC Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive CRC Error Packet Counter Interrupt Mask is enabled
4	RW	0x0	RXMCGPIM MMC Receive Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled
3	RO	0x0	reserved
2	RW	0x0	RXGOCTIM MMC Receive Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Octet Counter Interrupt Mask is enabled
1	RW	0x0	RXGBOCTIM MMC Receive Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Octet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	RXGBPKTIM MMC Receive Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Packet Counter Interrupt Mask is enabled

GMAC_MMC_Tx_Interrupt_Mask

Address: Operational Base(0xFFA80000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	TXPAUSPIM MMC Transmit Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled
22	RO	0x0	reserved
21	RW	0x0	TXGPKTIM MMC Transmit Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Packet Counter Interrupt Mask is enabled
20	RW	0x0	TXGOCTIM MMC Transmit Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Octet Counter Interrupt Mask is enabled
19	RW	0x0	TXCARERPIM MMC Transmit Carrier Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
18:14	RO	0x00	reserved
13	RW	0x0	TXUFLOWERPIM MMC Transmit Underflow Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled
12:2	RO	0x000	reserved
1	RW	0x0	TXGBPKTIM MMC Transmit Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled
0	RW	0x0	TXGBOCTIM MMC Transmit Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled

GMAC_Tx_Octet_Count_Good_Bad

Address: Operational Base(0xFFA80000) + offset (0x0714)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTGB Tx Octet Count Good Bad This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

GMAC_Tx_Packet_Count_Good_Bad

Address: Operational Base(0xFFA80000) + offset (0x0718)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTGB Tx Packet Count Good Bad This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

GMAC_Tx_Underflow_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x0748)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXUNDRFLW Tx Underflow Error Packets This field indicates the number of packets aborted because of packets underflow error.

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GMAC_Tx_Carrier_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x0760)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXCARR Tx Carrier Error Packets This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

GMAC_Tx_Octet_Count_Good

Address: Operational Base(0xFFA80000) + offset (0x0764)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTG Tx Octet Count Good This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

GMAC_Tx_Packet_Count_Good

Address: Operational Base(0xFFA80000) + offset (0x0768)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTG Tx Packet Count Good This field indicates the number of good packets transmitted.

GMAC_Tx_Pause_Packets

Address: Operational Base(0xFFA80000) + offset (0x0770)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPAUSE Tx Pause Packets This field indicates the number of good Pause packets transmitted.

GMAC_Rx_Packets_Count_Good_Bad

Address: Operational Base(0xFFA80000) + offset (0x0780)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPKTGB Rx Packets Count Good Bad This field indicates the number of good and bad packets received.

GMAC_Rx_Octet_Count_Good_Bad

Address: Operational Base(0xFFA80000) + offset (0x0784)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTGB Rx Octet Count Good Bad This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

GMAC_Rx_Octet_Count_Good

Address: Operational Base(0xFFA80000) + offset (0x0788)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTG Rx Octet Count Good This field indicates the number of bytes received, exclusive of preamble, only in good packets.

GMAC_Rx_Multicast_Packets_Good

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Address: Operational Base(0xFFA80000) + offset (0x0790)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXMCASTG Rx Multicast Packets Good This field indicates the number of good multicast packets received.

GMAC_Rx_CRC_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x0794)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXCRCERR Rx CRC Error Packets This field indicates the number of packets received with CRC error.

GMAC_Rx_Length_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXLENERR Rx Length Error Packets This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

GMAC_Rx_Pause_Packets

Address: Operational Base(0xFFA80000) + offset (0x07D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPAUSEPKT Rx Pause Packets This field indicates the number of good and valid Pause packets received.

GMAC_Rx_FIFO_Overflow_Packets

Address: Operational Base(0xFFA80000) + offset (0x07D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXFIFOOVFL Rx FIFO Overflow Packets This field indicates the number of missed received packets because of FIFO overflow.

GMAC_MMC_IPC_Rx_Interrupt_Mask

Address: Operational Base(0xFFA80000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	RXICMPEROIM MMC Receive ICMP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled
28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RW	0x0	RXTCPEROIM MMC Receive TCP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Octet Counter Interrupt Mask is enabled
26	RO	0x0	reserved
25	RW	0x0	RXUDPEROIM MMC Receive UDP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Octet Counter Interrupt Mask is enabled
24:23	RO	0x0	reserved
22	RW	0x0	RXIPV6HEROIM MMC Receive IPV6 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Value: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled
21:18	RO	0x0	reserved
17	RW	0x0	RXIPV4HEROIM MMC Receive IPV4 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled
16:14	RO	0x0	reserved
13	RW	0x0	RXICMPERPIM MMC Receive ICMP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled
12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	RXTCPERPIM MMC Receive TCP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Packet Counter Interrupt Mask is enabled
10	RO	0x0	reserved
9	RW	0x0	RXUDPERPIM MMC Receive UDP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Packet Counter Interrupt Mask is enabled
8:7	RO	0x0	reserved
6	RW	0x0	RXIPV6HERPIM MMC Receive IPV6 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled
5	RW	0x0	RXIPV6GPIM MMC Receive IPV6 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled
4:2	RO	0x0	reserved
1	RW	0x0	RXIPV4HERPIM MMC Receive IPV4 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	RXIPV4GPIM MMC Receive IPV4 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Mask is disable 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled

GMAC_MMC_IPC_Rx_Interrupt

Address: Operational Base(0xFFA80000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	RXICMPEROIS MMC Receive ICMP Error Octet Counter Interrupt Status This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Status detected
28	RO	0x0	reserved
27	RO	0x0	RXTCPEROIS MMC Receive TCP Error Octet Counter Interrupt Status This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Octet Counter Interrupt Status detected
26	RO	0x0	reserved
25	RO	0x0	RXUDPEROIS MMC Receive UDP Error Octet Counter Interrupt Status This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Octet Counter Interrupt Status detected
24:23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22	RO	0x0	RXIPV6HEROIS MMC Receive IPV6 Header Error Octet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected
21:18	RO	0x0	reserved
17	RO	0x0	RXIPV4HEROIS MMC Receive IPV4 Header Error Octet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected
16:14	RO	0x0	reserved
13	RO	0x0	RXICMPERPIS MMC Receive ICMP Error Packet Counter Interrupt Status This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Status detected
12	RO	0x0	reserved
11	RO	0x0	RXTCPERPIS MMC Receive TCP Error Packet Counter Interrupt Status This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Packet Counter Interrupt Status detected
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RO	0x0	RXUDPERPIS MMC Receive UDP Error Packet Counter Interrupt Status This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Packet Counter Interrupt Status detected
8:7	RO	0x0	reserved
6	RO	0x0	RXIPV6HERPIS MMC Receive IPV6 Header Error Packet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected
5	RO	0x0	RXIPV6GPIS MMC Receive IPV6 Good Packet Counter Interrupt Status This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Status detected
4:2	RO	0x0	reserved
1	RO	0x0	RXIPV4HERPIS MMC Receive IPV4 Header Error Packet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
0	RO	0x0	RXIPV4GPIS MMC Receive IPV4 Good Packet Counter Interrupt Status This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Status detected

GMAC_RxIPv4_Good_Packets

Address: Operational Base(0xFFA80000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4GDPKT RxIPv4 Good Packets This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RxIPv4_Header_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERRPKT RxIPv4 Header Error Packets This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

GMAC_RxIPv6_Good_Packets

Address: Operational Base(0xFFA80000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6GDPKT RxIPv6 Good Packets This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RxIPv6_Header_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x0828)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERRPKT RxIPv6 Header Error Packets This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

GMAC_RxUDP_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x0834)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERRPKT RxUDP Error Packets This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

GMAC_RxTCP_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x083C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERRPKT RxTCP Error Packets This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

GMAC_RxICMP_Error_Packets

Address: Operational Base(0xFFA80000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERRPKT RxICMP Error Packets This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

GMAC_RxIPv4_Header_Error_Octets

Address: Operational Base(0xFFA80000) + offset (0x0854)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERROCT RxIPv4 Header Error Octets This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RxIPv6_Header_Error_Octets

Address: Operational Base(0xFFA80000) + offset (0x0868)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERROCT RxIPv6 Header Error Octets This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RxUDP_Error_Octets

Address: Operational Base(0xFFA80000) + offset (0x0874)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERROCT RxUDP Error Octets This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RxTCP_Error_Octets

Address: Operational Base(0xFFA80000) + offset (0x087C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERROCT RxTCP Error Octets This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RxICMP_Error_Octets

Address: Operational Base(0xFFA80000) + offset (0x0884)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERROCT RxICMP Error Octets This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_MTL_Operation_Mode

Address: Operational Base(0xFFA80000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	CNTCLR Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Counters are not reset 0x1 (ENABLE): All counters are reset
8	RW	0x0	CNTPRST Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Counters are not reset 0x1 (ENABLE): All counters are reset
7:2	RO	0x00	reserved
1	RW	0x0	DTXSTS Drop Transmit Status When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. Values: 0x0 (DISABLE): Drop Transmit Status is disabled 0x1 (ENABLE): Drop Transmit Status is enabled
0	RO	0x0	reserved

GMAC_MTL_DBG_CTL

Address: Operational Base(0xFFA80000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	STSIE Transmit Status Available Interrupt Status Enable When this bit is set, an interrupt is generated when Transmit status is available in slave mode. Values: 1'b0: Transmit Packet Available Interrupt Status is disabled 1'b1: Transmit Packet Available Interrupt Status is enabled

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Bit	Attr	Reset Value	Description
14	RW	0x0	PKTIE Receive Packet Available Interrupt Status Enable When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. Values: 1'b0: Receive Packet Available Interrupt Status is disabled 1'b1: Receive Packet Available Interrupt Status is enabled
13:12	RW	0x0	FIFOSEL FIFO Selected for Access This field indicates the FIFO selected for debug access: Values: 2'b00: Tx FIFO 2'b01: Tx Status FIFO (only read access when SLVMOD is set) 2'b10: TSO FIFO (cannot be accessed when SLVMOD is set) 2'b11: Rx FIFO
11	RW	0x0	FIFOWREN FIFO Write Enable When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Write is disabled 1'b1: FIFO Write is enabled
10	RW	0x0	FIFORDEN FIFO Read Enable When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Read is disabled 1'b1: FIFO Read is enabled
9	RW	0x0	RSTSEL Reset Pointers of Selected FIFO When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset Pointers of Selected FIFO is disabled 1'b1: Reset Pointers of Selected FIFO is enabled

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Bit	Attr	Reset Value	Description
8	RW	0x0	RSTALL Reset All Pointers When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset All Pointers is disabled 1'b1: Reset All Pointers is enabled
7	RO	0x0	reserved
6:5	RW	0x0	PKTSTATE Encoded Packet State This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
4	RO	0x0	reserved
3:2	RW	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid
1	RW	0x0	DBGMOD Debug Mode Access to FIFO When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: 1. Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO 2. Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: 1. Write access to the Tx FIFO 2. Read access to the Rx FIFO and Tx Status FIFO Values: 1'b0: Debug Mode Access to FIFO is disabled 1'b1: Debug Mode Access to FIFO is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	FDBGEN FIFO Debug Access Enable When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. Values: 1'b0: FIFO Debug Access is disabled 1'b1: FIFO Debug Access is enabled

GMAC_MTL_DBG_STS

Address: Operational Base(0xFFA80000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00400	LOCR Remaining Locations in the FIFO Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively. Reset: In single Tx Queue configurations, (DWC_GMAC_TXFIFO_SIZE/(DWC_GMAC_DATAWIDTH/8)), Otherwise 0000H.
14:10	RO	0x00	reserved
9	RW	0x0	STSI Transmit Status Available Interrupt Status When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Transmit Status Available Interrupt Status not detected 1'b1: Transmit Status Available Interrupt Status detected
8	RW	0x0	PKTI Receive Packet Available Interrupt Status When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Receive Packet Available Interrupt Status not detected 1'b1: Receive Packet Available Interrupt Status detected
7:5	RO	0x0	reserved
4:3	RO	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid

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Bit	Attr	Reset Value	Description
2:1	RO	0x0	PKTSTATE Encoded Packet State This field is used to get the control or status information of the selected FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
0	RO	0x0	FIFOBUSY FIFO Busy When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: 1. All other fields of this register 2. All fields of the MTL_FIFO_Debug_Data register Values: 1'b0: FIFO Busy not detected 1'b1: FIFO Busy detected

GMAC_MTL_FIFO_Debug_Data

Address: Operational Base(0xFFA80000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FDBGDATA FIFO Debug Data During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

GMAC_MTL_Interrupt_Status

Address: Operational Base(0xFFA80000) + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	DBGIS Debug Interrupt status This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Debug Interrupt status not detected 1'b1: Debug Interrupt status detected
16:1	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	Q0IS Queue 0 Interrupt status This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Queue 0 Interrupt status not detected 1'b1: Queue 0 Interrupt status detected

GMAC_MTL_TxQ0_Operation_Mode

Address: Operational Base(0xFFA80000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	TTC Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. Values: 3'b000: 32 bytes 3'b001: 64 bytes 3'b010: 96 bytes 3'b011: 128 bytes 3'b100: 192 bytes 3'b101: 256 bytes 3'b110: 384 bytes 3'b111: 512 bytes
3:2	RO	0x0	reserved
1	RW	0x0	TSF Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. Values: 1'b0: Transmit Store and Forward is disabled 1'b1: Transmit Store and Forward is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	FTQ Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flush Transmit Queue is disabled 1'b1: Flush Transmit Queue is enabled

GMAC_MTL_TxQ0_Underflow

Address: Operational Base(0xFFA80000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RO	0x0	UFCNTOVF Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow not detected for Underflow Packet Counter 1'b1: Overflow detected for Underflow Packet Counter
10:0	RO	0x000	UFFRMCNT Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_TxQ0_Debug

Address: Operational Base(0xFFA80000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RO	0x0	STXSTSF Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue.When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:16	RO	0x0	PTXQ Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	RO	0x000	reserved
5	RO	0x0	TXSTSFSTS MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. Values: 1'b0: MTL Tx Status FIFO Full status is not detected 1'b1: MTL Tx Status FIFO Full status is detected
4	RO	0x0	TXQSTS MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. Values: 1'b0: MTL Tx Queue Not Empty status is not detected 1'b1: MTL Tx Queue Not Empty status is detected
3	RO	0x0	TWCSTS MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. Values: 1'b0: MTL Tx Queue Write Controller status is not detected 1'b1: MTL Tx Queue Write Controller status is detected
2:1	RO	0x0	TRCSTS MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller: Values: 2'b00: Idle state 2'b01: Read state (transferring data to the MAC transmitter) 2'b10: Waiting for pending Tx Status from the MAC transmitter 2'b11: Flushing the Tx queue because of the Packet Abort request from the MAC
0	RO	0x0	TXQPAUSED Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: 1. Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled 2. Reception of 802.3x Pause packet when PFC is disabled Values: 1'b0: Transmit Queue in Pause status is not detected 1'b1: Transmit Queue in Pause status is detected

GMAC_MTL_Q0_Interrupt_Ctrl_Status

Address: Operational Base(0xFFA80000) + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	RXOIE Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. Values: 1'b0: Receive Queue Overflow Interrupt is disabled 1'b1: Receive Queue Overflow Interrupt is enabled
23:17	RO	0x00	reserved
16	RW	0x0	RXOVFIS Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Receive Queue Overflow Interrupt Status not detected 1'b1: Receive Queue Overflow Interrupt Status detected
15:9	RO	0x00	reserved
8	RW	0x0	TXUIE Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. Values: 1'b0: Transmit Queue Underflow Interrupt Status is disabled 1'b1: Transmit Queue Underflow Interrupt Status is enabled
7:1	RO	0x00	reserved
0	RW	0x0	TXUNFIS Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Transmit Queue Underflow Interrupt Status not detected 1'b1: Transmit Queue Underflow Interrupt Status detected

GMAC_MTL_RxQ0_Operation_Mode

Address: Operational Base(0xFFA80000) + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:14	RW	0x0	RFD Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ...

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Bit	Attr	Reset Value	Description
			62: Full minus 32 KB, that is, FULL 32 KB 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:12	RO	0x0	reserved
11:8	RW	0x0	RFA Threshold for Activating Flow Control (in half-duplex and full-duplex) These bits control the threshold (fill-level of Rx queue) at which the flow control is activated:For more information on encoding for this field, see RFD.
7	RW	0x0	EHFC Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. Values: 1'b0: Hardware Flow Control is disabled 1'b1: Hardware Flow Control is enabled
6	RW	0x0	DIS_TCP_EF Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. Values: 1'b0: Dropping of TCP/IP Checksum Error Packets is enabled 1'b1: Dropping of TCP/IP Checksum Error Packets is disabled
5	RW	0x0	RSF Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. Values: 1'b0: Receive Queue Store and Forward is disabled 1'b1: Receive Queue Store and Forward is enabled

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Bit	Attr	Reset Value	Description
4	RW	0x0	FEP Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA. Values: 1'b0: Forward Error Packets is disabled 1'b1: Forward Error Packets is enabled
3	RW	0x0	FUP Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. Values: 1'b0: Forward Undersized Good Packets is disabled 1'b1: Forward Undersized Good Packets is enabled
2	RO	0x0	reserved
1:0	RW	0x0	RTC Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.

GMAC_MTL_RxQ0_Miss_Pkt_Ovf_Cnt

Address: Operational Base(0xFFA80000) + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	MISCNTOVF Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Missed Packet Counter overflow not detected 1'b1: Missed Packet Counter overflow detected

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Bit	Attr	Reset Value	Description
26:16	RO	0x000	MISPKTCNT Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is incremented each time the application issues ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. In GMAC-DMA, GMAC-AXI, and GMAC-AHB configurations, This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	RO	0x0	reserved
11	RO	0x0	OVFCNTOVF Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow Counter overflow not detected 1'b1: Overflow Counter overflow detected
10:0	RO	0x000	OVFPKTCNT Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_RxQ0_Debug

Address: Operational Base(0xFFA80000) + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	PRXQ Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	RO	0x000	reserved
5:4	RO	0x0	RXQSTS MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue: Values: 2'b00: Rx Queue empty 2'b01: Rx Queue fill-level below flow-control deactivate threshold 2'b10: Rx Queue fill-level above flow-control activate threshold 2'b11: Rx Queue full
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:1	RO	0x0	RRCSTS MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller: Values: 2'b00: Idle state 2'b01: Reading packet data 2'b10: Reading packet status (or timestamp) 2'b11: Flushing the packet data and status
0	RO	0x0	RWCSTS MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. Values: 1'b0: MTL Rx Queue Write Controller Active Status not detected 1'b1: MTL Rx Queue Write Controller Active Status detected

GMAC_DMA_Mode

Address: Operational Base(0xFFA80000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	INTM Interrupt Mode This field defines the interrupt mode of DWC_ether_qos. The behavior of the following outputs changes depending on the following settings: 1. sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) 2. sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) 3. sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. 2'b00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corre_sponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. 2'b01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b11: Reserved Values: 2'b00: See above description 2'b01: See above description 2'b10: See above description 2'b11: Reserved
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	DSPW Descriptor Posted Write When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. Values: 1'b0: Descriptor Posted Write is disabled 1'b1: Descriptor Posted Write is enabled
7:1	RO	0x00	reserved
0	RW	0x0	SWR Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all DWC_ether_qos clock domains. Before reprogramming any DWC_ether_qos register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Software Reset is disabled 1'b1: Software Reset is enabled

GMAC_DMA_SysBus_Mode

Address: Operational Base(0xFFA80000) + offset (0x1004)

Bit	Attr	Reset Value	Description
31	RW	0x0	EN_LPI Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode supported by the GMAC-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. Values: 1'b0: Low Power Interface (LPI) is disabled 1'b1: Low Power Interface (LPI) is enabled
30	RW	0x0	LPI_XIT_PKT Unlock on Magic Packet or Remote Wake-Up Packet When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. Values: 1'b0: Unlock on Magic Packet or Remote Wake-Up Packet is disabled 1'b1: Unlock on Magic Packet or Remote Wake-Up Packet is enabled

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Bit	Attr	Reset Value	Description
29:26	RO	0x0	reserved
25:24	RW	0x0	WR_OSR_LMT AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Note: 1. Bit 26 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ = 4 2. Bit 27 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ!= 16
23:19	RO	0x00	reserved
18:16	RW	0x1	RD_OSR_LMT AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1 Note: 1. Bit 18 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ = 4 2. Bit 19 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ!= 16
15:13	RO	0x0	reserved
12	RW	0x0	AAL Address-Aligned Beats When this bit is set to 1, the GMAC-AXI or GMAC-AHB master performs address-aligned burst transfers on Read and Write channels. Values: 1'b0: Address-Aligned Beats is disabled 1'b1: Address-Aligned Beats is enabled
11	RW	0x0	EAME Enhanced Address Mode Enable. When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration. Values: 0x0 (DISABLE): Enhanced Address Mode is disabled 0x1 (ENABLE): Enhanced Address Mode is enabled
10	RW	0x0	AALE Automatic AXI LPI enable When set to 1, enables the AXI master to enter into LPI state when there is no activity in the DWC_ether_qos for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. Values: 1'b0: Automatic AXI LPI is disabled 1'b1: Automatic AXI LPI is enabled
9:4	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	BLEN16 AXI Burst Length 16 When this bit is set to 1 or the FB bit is set to 0, the GMAC-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 16
2	RW	0x0	BLEN8 AXI Burst Length 8 When this bit is set to 1 or the FB bit is set to 0, the GMAC-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 8
1	RW	0x0	BLEN4 AXI Burst Length 4 When this bit is set to 1 or the FB bit is set to 0, the GMAC-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 4
0	RW	0x0	FB Fixed Burst Length When this bit is set to 1, the GMAC-AXI master initiates burst transfers of specified lengths as given below. 1. Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field 2. Burst transfers of length 1 When this bit is set to 0, the GMAC-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. Values: 1'b0: Fixed Burst Length is disabled 1'b1: Fixed Burst Length is enabled

GMAC_DMA_Interrupt_Status

Address: Operational Base(0xFFA80000) + offset (0x1008)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	MACIS MAC Interrupt Status This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. Values: 1'b0: MAC Interrupt Status not detected 1'b1: MAC Interrupt Status detected

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Bit	Attr	Reset Value	Description
16	RO	0x0	MTLIS MTL Interrupt Status This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. Values: 1'b0: MTL Interrupt Status not detected 1'b1: MTL Interrupt Status detected
15:1	RO	0x0000	reserved
0	RO	0x0	DC0IS DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. Values: 1'b0: DMA Channel 0 Interrupt Status not detected 1'b1: DMA Channel 0 Interrupt Status detected

GMAC_DMA_Debug_Status0

Address: Operational Base(0xFFA80000) + offset (0x100C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	TPS0 DMA Channel 0 Transmit Process State This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Transmit Command issued) 4'b0001: Running (Fetching Tx Transfer Descriptor) 4'b0010: Running (Waiting for status) 4'b0011: Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 4'b0100: Timestamp write state 4'b0101: Reserved for future use 4'b0110: Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 4'b0111: Running (Closing Tx Descriptor)
11:8	RO	0x0	RPS0 DMA Channel 0 Receive Process State This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Receive Command issued) 4'b0001: Running (Fetching Rx Transfer Descriptor) 4'b0010: Reserved for future use 4'b0011: Running (Waiting for Rx packet) 4'b0100: Suspended (Rx Descriptor Unavailable) 4'b0101: Running (Closing the Rx Descriptor) 4'b0110: Timestamp write state 4'b0111: Running (Transferring the received packet data from the Rx buffer to the system memory)
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x0	AXRHSTS AXI Master Read Channel Status When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. Values: 1'b0: AXI Master Read Channel Status not detected 1'b1: AXI Master Read Channel Status detected
0	RO	0x0	AXWHSTS AXI Master Write Channel or AHB Master Status GMAC-AXI Configuration: When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. GMAC-AHB Configuration: When high, this bit indicates that the AHB master FSMs are in the non-idle state. Values: 1'b0: AXI Master Write Channel or AHB Master Status not detected 1'b1: AXI Master Write Channel or AHB Master Status detected

GMAC_AXI_LPI_Entry_Interval

Address: Operational Base(0xFFA80000) + offset (0x1040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	LPIEI LPI Entry Interval Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the DWC_ether_qos to enter into the AXI low power state. 0 indicates 64 clock cycles.

GMAC_DMA_CH0_Control

Address: Operational Base(0xFFA80000) + offset (0x1100)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	SPH Split Headers When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. Values: 0x0 (DISABLE): Split Headers feature is disabled 0x1 (ENABLE): Split Headers feature is enabled
23:21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20:18	RW	0x0	DSL Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	RO	0x0	reserved
16	RW	0x0	PBLx8 8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH0_Tx_Control and Bits[21:16] in DMA_CH0_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled 0x1 (ENABLE): 8xPBL mode is enabled
15:14	RO	0x0	reserved
13:0	RW	0x0000	MSS Maximum Segment Size This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

GMAC_DMA_CH0_Tx_Control

Address: Operational Base(0xFFA80000) + offset (0x1104)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	TxPBL Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.

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Bit	Attr	Reset Value	Description
15	RW	0x0	IPBL Ignore PBL Requirement When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled 0x1 (ENABLE): Ignore PBL Requirement is enabled
14:13	RW	0x0	TSE_MODE TSE Mode 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. 11: Reserved 0x0 (TSO_USO): TSO/USO 0x1 (UFOWC): UFO with Checksum 0x2 (UFOWOC): UFO without Checksum 0x3 (RSVD): Reserved
12	RW	0x0	TSE TCP Segmentation Enabled When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled 0x1 (ENABLE): TCP Segmentation is enabled
11:5	RO	0x00	reserved
4	RW	0x0	OSF Operate on Second Packet When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled 0x1 (ENABLE): Operate on Second Packet enabled
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	ST Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. 2.The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command 0x1 (START): Start Transmission Command

GMAC_DMA_CH0_Rx_Control

Address: Operational Base(0xFFA80000) + offset (0x1108)

Bit	Attr	Reset Value	Description
31	RW	0x0	RPF Rx Packet Flush When this bit is set to 1, then DWC_ether_qos automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the DWC_ether_qos not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This may in turn cause head-of-line blocking in the corresponding RxQueue. 0x0 (DISABLE): Rx Packet Flush is disabled 0x1 (ENABLE): Rx Packet Flush is enabled
30:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x00	RxPBL Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RO	0x0	reserved
14:4	RW	0x000	RBSZ_13_y Receive Buffer size High RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_3_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_3_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	RO	0x0	RBSZ_3_0 Receive Buffer size Low RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_3_0. The RBSZ_3_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO)

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Bit	Attr	Reset Value	Description
0	RW	0x0	SR Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. 2.The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive 0x1 (START): Start Receive

GMAC_DMA_CH0_TxDesc_List_HAddress

Address: Operational Base(0xFFA80000) + offset (0x1110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	TDESHA Start of Transmit List This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

GMAC_DMA_CH0_TxDesc_List_Address

Address: Operational Base(0xFFA80000) + offset (0x1114)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDESLA Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_RxDesc_List_HAaddress

Address: Operational Base(0xFFA80000) + offset (0x1118)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	RDESHA Start of Receive List This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

GMAC_DMA_CH0_RxDesc_List_Address

Address: Operational Base(0xFFA80000) + offset (0x111C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDESLA Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_TxDesc_Tail_Pointer

Address: Operational Base(0xFFA80000) + offset (0x1120)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDTP Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_RxDesc_Tail_Pointer

Address: Operational Base(0xFFA80000) + offset (0x1128)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDRT Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_TxDesc_Ring_Length

Address: Operational Base(0xFFA80000) + offset (0x112C)

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Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	TDRL Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. we recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH0_RxDesc_Ring_Length

Address: Operational Base(0xFFA80000) + offset (0x1130)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	RDRL Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, you can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH0_Interrupt_Enable

Address: Operational Base(0xFFA80000) + offset (0x1134)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	NIE Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled 0x1 (ENABLE): Normal Interrupt Summary is enabled
14	RW	0x0	AIE Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 1: Transmit Process Stopped Bit 7: Rx Buffer Unavailable Bit 8: Receive Process Stopped Bit 9: Receive Watchdog Timeout Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled 0x1 (ENABLE): Abnormal Interrupt Summary is enabled

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Bit	Attr	Reset Value	Description
13	RW	0x0	CDEE Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled 0x1 (ENABLE): Context Descriptor Error is enabled
12	RW	0x0	FBEE Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled 0x1 (ENABLE): Fatal Bus Error is enabled
11	RW	0x0	ERIE Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled 0x1 (ENABLE): Early Receive Interrupt is enabled
10	RW	0x0	ETIE Early Transmit Interrupt Enable When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled 0x1 (ENABLE): Early Transmit Interrupt is enabled
9	RW	0x0	RWTE Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled 0x1 (ENABLE): Receive Watchdog Timeout is enabled
8	RW	0x0	RSE Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.
7	RW	0x0	RBUE Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled 0x1 (ENABLE): Receive Buffer Unavailable is enabled
6	RW	0x0	RIE Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled 0x1 (ENABLE): Receive Interrupt is enabled
5:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	TBUE Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled 0x1 (ENABLE): Transmit Buffer Unavailable is enabled
1	RW	0x0	TXSE Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled 0x1 (ENABLE): Transmit Stopped is enabled
0	RW	0x0	TIE Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled 0x1 (ENABLE): Transmit Interrupt is enabled

GMAC_DMA_CH0_Rx_Interrupt_Watchdog_Timer

Address: Operational Base(0xFFA80000) + offset (0x1138)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	RWTU Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. 2'b00: 256 2'b01: 512 2'b10: 1024 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	RO	0x00	reserved
7:0	RW	0x00	RWT Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH0_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

GMAC_DMA_CH0_Current_App_TxDesc

Address: Operational Base(0xFFA80000) + offset (0x1144)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTDESAPTR Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_Current_App_RxDesc

Address: Operational Base(0xFFA80000) + offset (0x114C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRDESAPTR Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_Curren_App_TxBuffer_H

Address: Operational Base(0xFFA80000) + offset (0x1150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURTBUFAPTRH Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_Current_App_TxBuffer

Address: Operational Base(0xFFA80000) + offset (0x1154)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTBUFAPTR Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_Current_App_RxBuffer_H

Address: Operational Base(0xFFA80000) + offset (0x1158)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURRBUFAPTRH Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_Current_App_RxBuffer

Address: Operational Base(0xFFA80000) + offset (0x115C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRBUFAPTR Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_Status

Address: Operational Base(0xFFA80000) + offset (0x1160)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:19	RO	0x0	REB Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 21 1'b1: Error during data transfer by Rx DMA 1'b0: No Error during data transfer by Rx DMA 2.Bit 20 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 19 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	RO	0x0	TEB Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 18 1'b1: Error during data transfer by Tx DMA 1'b0: No Error during data transfer by Tx DMA 2.Bit 17 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 16 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	RW	0x0	NIS Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected 0x1 (ACTIVE): Normal Interrupt Summary status detected

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Bit	Attr	Reset Value	Description
14	RW	0x0	AIS Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 1: Transmit Process Stopped Bit 7: Receive Buffer Unavailable Bit 8: Receive Process Stopped Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected 0x1 (ACTIVE): Abnormal Interrupt Summary status
13	RW	0x0	CDE Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected 0x1 (ACTIVE): Context Descriptor Error status detected
12	RW	0x0	FBE Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected 0x1 (ACTIVE): Fatal Bus Error status detected
11	RW	0x0	ERI Early Receive Interrupt This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected 0x1 (ACTIVE): Early Receive Interrupt status detected

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Bit	Attr	Reset Value	Description
10	RW	0x0	ETI Early Transmit Interrupt This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected 0x1 (ACTIVE): Early Transmit Interrupt status detected
9	RO	0x0	reserved
8	RW	0x0	RPS Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected 0x1 (ACTIVE): Receive Process Stopped status detected
7	RW	0x0	RBU Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected 0x1 (ACTIVE): Receive Buffer Unavailable status detected
6	RW	0x0	RI Receive Interrupt This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected 0x1 (ACTIVE): Receive Interrupt status detected
5:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	TBU Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected 0x1 (ACTIVE): Transmit Buffer Unavailable status
1	RW	0x0	TPS Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected 0x1 (ACTIVE): Transmit Process Stopped status detected
0	RW	0x0	TI Transmit Interrupt This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected 0x1 (ACTIVE): Transmit Interrupt status detected

GMAC_DMA_CH0_Miss_Frame_Cnt

Address: Operational Base(0xFFA80000) + offset (0x1164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	MFC0 Overflow status of the MFC Counter When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred 0x1 (ACTIVE): Miss Frame Counter overflow occurred
14:11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RO	0x000	MFC Dropped Packet Counters This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programming RPF field in DMA_CH0_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_DMA_CH0_RX_ERI_Cnt

Address: Operational Base(0xFFA80000) + offset (0x1168)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ECNT ERI Counter When ERIC bit of DMA_CH0_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter will get reset at the start of new packet.

8.5 Interface Description

Table 8-3 GMAC Interface M0

Module Pin	Dir.	Pad Name	IOMUX Setting
RMII/RGMII interface			
gmac_mclkinoutm0	I/O	VO_LCDC_CLK/RGMII_CLK_M0/CAM_CLK1_OUT_M1/PDM_CLK0_M1/GPIO4_B7_d	GPIO4B_IOMUX_SEL_H[14:12]=3'h2
gmac_rxclkm0	I	VO_LCDC_D21/RGMII_RXCLK_M0/I2S2_LRCK_M1/PWM12_M0/GPIO4_A1_d	GPIO4A_IOMUX_SEL_L[6:4]=3'h2
gmac_rxdvcrsm0	I	VO_LCDC_D9/RGMII_RXDV_M0/UART1_RTSN_M1/PDM_SDI0_M1/UART6_TX_M1/GPIO4_A7_d	GPIO4A_IOMUX_SEL_H[14:12]=3'h2
gmac_rxerm0	I	VO_LCDC_D16/RGMII_RXER_M0/UART1_CTSN_M1/PDM_SDI1_M1/UART6_RX_M1/GPIO4_B0_d	GPIO4B_IOMUX_SEL_L[2:0]=3'h2
gmac_rxd0m0	I	VO_LCDC_D1/RGMII_RXD0_M0/UART1_TX_M1/PDM_SDI2_M1/I2C3_SCL_M1/GPIO4_A5_d	GPIO4A_IOMUX_SEL_H[6:4]=3'h2
gmac_rxd1m0	I	VO_LCDC_D8/RGMII_RXD1_M0/UART1_RX_M1/PDM_SDI3_M1/I2C3_SDA_M1/GPIO4_A6_d	GPIO4A_IOMUX_SEL_H[10:8]=3'h2
gmac_rxd2m0	I	VO_LCDC_D19/RGMII_RXD2_M0/UART8_CTSN_M1/SPI1_CSN0_M0/GPIO3_D7_d	GPIO3D_IOMUX_SEL_H[14:12]=3'h2
gmac_rxd3m0	I	VO_LCDC_D20/RGMII_RXD3_M0/UART8_RTSN_M1/SPI1_CSN1_M0/GPIO4_A0_d	GPIO4A_IOMUX_SEL_L[2:0]=3'h2
gmac_txclkm0	O	VO_LCDC_D15/RGMII_TXCLK_M0/I2S2_MCLK_M1/SPI1_CLK_M0/GPIO3_D6_d	GPIO3D_IOMUX_SEL_H[10:8]=3'h2
gmac_txenm0	O	VO_LCDC_D0/RGMII_TXEN_M0/PWM13_M0/GPIO4_A4_d	GPIO4A_IOMUX_SEL_H[2:0]=3'h2
gmac_txd0m0	O	VO_LCDC_D22/RGMII_TXD0_M0/UART6_CTSN_M1/SPI1_MOSI_M0/GPIO4_A2_d	GPIO4A_IOMUX_SEL_L[10:8]=3'h2
gmac_txd1m0	O	VO_LCDC_D23/RGMII_TXD1_M0/UART6_RTSN_M1/SPI1_MISO_M0/GPIO4_A3_d	GPIO4A_IOMUX_SEL_L[14:12]=3'h2
gmac_txd2m0	O	VO_LCDC_D13/RGMII_TXD2_M0/UART8_TX_M1/I2S2_SDI_M1/GPIO3_D4_d	GPIO3D_IOMUX_SEL_H[2:0]=3'h2
gmac_txd3m0	O	VO_LCDC_D14/RGMII_TXD3_M0/UART8_RX_M1/I2S2_SDO_M1/GPIO3_D5_d	GPIO3D_IOMUX_SEL_H[6:4]=3'h2
gmac_refclkm0	O	VO_LCDC_D17/ETH_CLK_25M_OUT_M0/CAM_CLK0_OUT_M1/I2S2_SCLK_M1/PDM_CLK1_M1/GPIO4_B1_d	GPIO4B_IOMUX_SEL_L[6:4]=3'h2
Management interface			
gmac_mdcm0	O	VO_LCDC_D2/RGMII_MDC_M0/UART9_TX_M0/GPIO4_B2_d	GPIO4B_IOMUX_SEL_L[10:8]=3'h2
gmac_mdiom0	I/O	VO_LCDC_D18/RGMII_MDIO_M0/UART9_RX_M0/GPIO4_B3_d	GPIO4B_IOMUX_SEL_L[14:12]=3'h2

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Table 8-4 GMAC Interface M1

Module Pin	Dir.	Pad Name	IOMUX Setting
RMII/RGMII interface			
gmac_mclkinoutm1	I/O	I2S2_SCLK_M0/RGMII_CLK_M1/UART4_RX_M1/SPI2_CSN1_M1/RMII_CLK/GPIO1_D5_d	GPIO1D_IOMUX_SEL_H[6:4]=3'h2
gmac_rxclkm1	I	SDMMC1_CLK/RGMII_RXCLK_M1/I2S0_MCLK_M1/PWM1_M1/GPIO1_C6_d	GPIO1C_IOMUX_SEL_H[10:8]=3'h2
gmac_rxdvcrsm1	I	I2S2_LRCK_M0/RGMII_RXDV_M1/UART4_TX_M1/SPI2_CSN0_M1/RMII_RXDV_CRS/GPIO1_D6_d	GPIO1D_IOMUX_SEL_H[10:8]=3'h2
gmac_rxerm1	I	I2S2_SDI_M0/RGMII_RXER_M1/UART4_CTSN_M1/SPI2_MISO_M1/PWM15_M1/RMII_RXER/GPIO2_A0_d	GPIO2A_IOMUX_SEL_L[2:0]=3'h2
gmac_rxd0m1	I	UART1_CTSN_M0/RGMII_RXD0_M1/I2S0_SDI3_M1/PWM7_M1/RMII_RXD0/GPIO1_D4_d	GPIO1D_IOMUX_SEL_H[2:0]=3'h2
gmac_rxd1m1	I	I2S2_SDO_M0/RGMII_RXD1_M1/UART4_RTSN_M1/SPI2_MOSI_M1/PWM14_M1/RMII_RXD1/GPIO1_D7_d	GPIO1D_IOMUX_SEL_H[14:12]=3'h2
gmac_rxd2m1	I	SDMMC1_D3/RGMII_RXD2_M1/I2S0_LRCK_M1/PWM11_M1/GPIO1_C4_d	GPIO1C_IOMUX_SEL_H[2:0]=3'h2
gmac_rxd3m1	I	SDMMC1_CMD/RGMII_RXD3_M1/I2S0_SCLK_M1/PWM0_M1/GPIO1_C5_d	GPIO1C_IOMUX_SEL_H[6:4]=3'h2
gmac_txclkm1	O	SDMMC1_D2/RGMII_TXCLK_M1/I2S0_SDO0_M1/PWM10_M1/GPIO1_C3_d	GPIO1C_IOMUX_SEL_L[14:12]=3'h2
gmac_txenm1	O	UART1_RTSN_M0/RGMII_TXEN_M1/I2S0_SDI2_M1/PWM6_M1/RMII_TXEN/GPIO1_D3_d	GPIO1D_IOMUX_SEL_L[14:12]=3'h2
gmac_txd0m1	O	UART1_RX_M0/RGMII_TXD0_M1/I2S0_SDO1_M1/PWM4_M1/RMII_TXD0/GPIO1_D1_d	GPIO1D_IOMUX_SEL_L[6:4]=3'h2
gmac_txd1m1	O	UART1_TX_M0/RGMII_TXD1_M1/I2S0_SDO2_M1/PWM5_M1/RMII_TXD1/GPIO1_D2_d	GPIO1D_IOMUX_SEL_L[10:8]=3'h2
gmac_txd2m1	O	SDMMC1_D0/RGMII_TXD2_M1/I2S0_SDI0_M1/PWM8_M1/GPIO1_C1_d	GPIO1C_IOMUX_SEL_L[6:4]=3'h2
gmac_txd3m1	O	SDMMC1_D1/RGMII_TXD3_M1/I2S0_SDI1_M1/PWM9_M1/GPIO1_C2_d	GPIO1C_IOMUX_SEL_L[10:8]=3'h2
gmac_refclkm1	O	I2S2_MCLK_M0/ETH_CLK_25M_OUT_M1/CLK1_32K_OUT/SPI2_CLK_M1/I2S0_SDO3_M1/GPIO2_A1_d	GPIO2A_IOMUX_SEL_L[6:4]=3'h2
Management interface			
gmac_mdcm1	O	SDMMC1_PWREN/RGMII_MDC_M1/PWM2_M1/I2C5_SCL_M1/RMII_MDC/GPIO1_C7_d	GPIO1C_IOMUX_SEL_H[14:12]=3'h2
gmac_mdiom1	I/O	SDMMC1_DETN/RGMII_MDIO_M1/PWM3_M1/I2C5_SDA_M1/RMII_MDIO/GPIO1_D0_d	GPIO1D_IOMUX_SEL_L[2:0]=3'h2

8.6 Application Note

8.6.1 GMAC Descriptors

The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention. The DMA is designed for packet-oriented data transfers such as packets in Ethernet. The DMA controller can be programmed tointerrupt the application CPU for situations such as Packet Transmit and Receive Transfer completion, and other normal or error conditions.

The DMA and the application communicate through the following two data structures:

- Control and Status registers (CSR)
- Descriptor lists and data buffers

The base address of each list is written to the respective Tx Descriptor List Address register and Rx Descriptor List Address register. The descriptor list is forward linked and the next descriptor is always considered at a fixed offset to the current one. The offset is controlled by the DSL field of DMA_Ch[n]_Control register. The number of descriptors in the list is programmed in the respective Tx (or Rx) Descriptor Ring Length register. Once the DMA processes the last descriptor in the list, it automatically jumps back to the descriptor in the List Address register to create a descriptor ring.

The descriptor lists reside in the physical memory address space of the application. Each descriptor can point to a maximum of two buffers in the system memory. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.

A data buffer resides in the application physical memory space and consists of an entire packet or part of a packet but cannot exceed a single packet. Buffers contain only data. Buffer status is maintained in the descriptor. Data chaining refers to packets that span

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multiple data buffers. However, a single descriptor cannot span multiple packets. The DMA skips to the data buffer of next packet when EOP is detected.
The GMAC supports the following two types of descriptors:

- Normal Descriptor: Normal descriptors are used for packet data and to provide control information applicable to the packets to be transmitted
- Context Descriptor: Context descriptors are used to provide control information applicable to the packet to be transmitted

The GMAC supports the ring structure for the DMA descriptor.

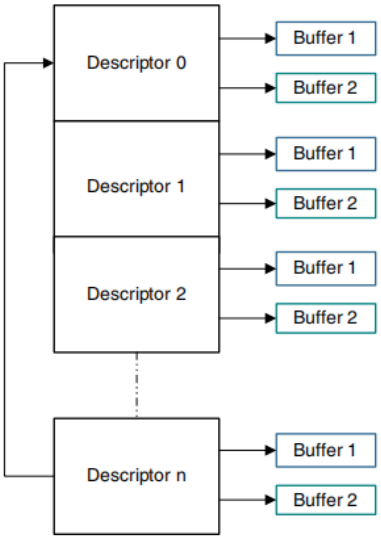

Fig. 8-10 Descriptor Ring Structure

In Ring structure, descriptors are separated by the Word, DWord, or LWord number programmed in the DSL field of the DMA_CH#_Control register. The application needs to program the total ring length, that is, the total number of descriptors in ring span in the following registers of a DMA channel:

- Transmit Descriptor Ring Length Register (DMA_CH#_TxDesc_Ring_Length)
- Receive Descriptor Ring Length Register (DMA_CH#_RxDesc_Ring_Length)

The Descriptor Tail Pointer Register contains the pointer to the descriptor address (N). The base address and the current descriptor pointer decide the address of the current descriptor that the DMA can process.
The descriptors up to one location less than the one indicated by the descriptor tail pointer (N – 1) are owned by the DMA. The DMA continues to process the descriptors until the following condition occurs:

Current Descriptor Pointer == Descriptor Tail Pointer

The DMA goes into the Suspend mode when this condition occurs. The application must perform a write to the Descriptor Tail pointer register and update the tail pointer so that the following condition is true:

Current Descriptor Pointer < Descriptor Tail Pointer

The DMA automatically wraps around the base address when the end of ring is reached. For descriptors owned by the application, the OWN bit of DES3 is reset to 0. For descriptors owned by the DMA, the OWN bit is set to 1. If the application has only one descriptor in the beginning, the application sets the last descriptor address (tail pointer) to Descriptor Base Address + 1. The DMA processes the first descriptor and then waits for the application to advance the tail pointer.

8.6.2 GMAC Transmit Descriptors

The DMA in GMAC requires at least one descriptor for a transmit packet. In addition to two buffers, two byte-count buffers, and two address pointers, the transmit descriptor has control fields which can be used to control the MAC operation on per-transmit packet basis. The Transmit Normal descriptor has two formats: Read format and Write-Back format.

8.6.3 GMAC Transmit Normal Descriptor (Read Format)

Table 8-4 TDES0 Normal Descriptor (Read Format)

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Bit	Name	Description
31:0	BUF1AP	Buffer 1 Address Pointer or TSO Header Address Pointer These bits indicate the physical address of Buffer 1. These bits indicate the TSO Header Address pointer when the following bits are set: ■ TSE bit of TDES3 ■ FD bit of TDES3

Table 8-5 TDES1 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF2AP	Buffer 2 or Buffer 1 Address Pointer This bit indicates the physical address of Buffer 2 when a descriptor ring structure is used. There is no limitation for the buffer address alignment. In 40- or 48-bit addressing mode, these bits indicate the most-significant 8- or 16- bits of the Buffer 1 Address Pointer.

Table 8-6 TDES2 Normal Descriptor (Read Format)

Bit	Name	Description
31	IOC	Interrupt on Completion This bit controls the setting of TI and ETI status bits in the DMA_CH#_Status register. When ETIC = 1 and TDES2[LD] = 0, this bit sets the ETI bit. When TDES3[LD] = 1, this bit sets the TI status bit.
30	TTSE/TMWD	Transmit Timestamp Enable or External TSO Memory Write Enable This bit enables the IEEE1588 time stamping for Transmit packet referenced by the descriptor, if TSE bit is not set. If TSE bit is set and external TSO memory is enabled, setting this bit disables external TSO memory writing for this packet.
29:16	B2L	Buffer 2 Length The driver sets this field. When set, this field indicates Buffer 2 length
15:14	VTIR	VLAN Tag Insertion or Replacement These bits request the MAC to perform VLAN tagging or untagging before transmitting the packets. The application must set the CRC Pad Control bits appropriately when VLAN Tag Insertion, Replacement, or Deletion is enabled for the packet. The following list describes the values of these bits: ■ 2'b00: Do not add a VLAN tag. ■ 2'b01: Remove the VLAN tag from the packets before transmission. This option should be used only with the VLAN packets. ■ 2'b10: Insert a VLAN tag with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the VLAN tag in packets with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. This option should be used only with the VLAN packets. These bits are valid when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core
13:0	HL or	Header Length or Buffer 1 Length

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Bit	Name	Description
	B1L	For Header length only bits [9:0] are taken. The size 13:0 is applicable only when interpreting buffer 1 length. If the TCP Segmentation Offload feature is enabled through the TSE bit of TDES3, this field is equal to the header length. When the TSE bit is set in TDES3, the header length includes the length in bytes from Ethernet Source address till the end of the TCP header. The maximum header length supported for TSO feature is 1023 bytes. The maximum header length supported for TSO feature is 1023 bytes. If the TCP Segmentation Offload feature is not enabled, this field is equal to Buffer 1 length.

Table 8-7 TDES3 Normal Descriptor (Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:26	CPC	CRC Pad Control This field controls the CRC and Pad Insertion for Tx packet. This field is valid only when the first descriptor bit (TDES3[29]) is set. The following list describes the values of Bits[27:26]: ■ 2'b00: CRC and Pad Insertion. The MAC appends the cyclic redundancy check (CRC) at the end of the transmitted packet of length greater than or equal to 60 bytes. The MAC automatically appends padding and CRC to a packet with length less than 60 bytes. ■ 2'b01: CRC Insertion (Disable Pad Insertion). The MAC appends the CRC at the end of the transmitted packet but it does not append padding. The application should ensure that the padding bytes are present in the packet being transferred from the Transmit Buffer, that is, the packet being transferred from the Transmit Buffer is of length greater than or equal to 60 bytes. ■ 2'b10: Disable CRC Insertion. The MAC does not append the CRC at the end of the transmitted packet. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. ■ 2'b11: CRC Replacement. The MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer.

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Bit	Name	Description
		This field is valid only for the first descriptor. Note: When the TSE bit is set, the MAC ignores this field because the CRC and pad insertion is always done for segmentation.
25:23	SAIC	SA Insertion Control These bits request the MAC to add or replace the Source Address field in the Ethernet packet with the value given in the MAC Address 0 register. The application must set the CRC Pad Control bits appropriately when SA Insertion Control is enabled for the packet. Bit 25 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement. The following list describes the values of Bits[24:23]: ■ 2'b00: Do not include the source address ■ 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. ■ 2'b10: Replace the source address. For reliabletransmission, the application must provide frames with source addresses. ■ 2'b11: Reserved These bits are valid in the GMAC-DMA, GMAC-AXI, and GMAC-AHB configurations when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core and when the First Segment control bit (TDES3 [29]) is set. This field is valid only for the first descriptor.
22:19	SLOTNUM or THL	SLOTNUM: Slot Number Control Bits in AV Mode These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES0 or TDES1. When the Transmit descriptor is fetched, the DMA compares the slot number value in this field with the slot interval maintained in the RSN field DMA_CH#_Slot_Function_Control_Status. It fetches the data from the buffers only if a value matches. These bits are valid only for the AV channels. THL: TCP/UDP Header Length If the TSE bit is set, this field contains the length of the TCP/UDP header. The minimum value of this field must be 5 for TCP header. The value must be equal to 2 for UDP header. This field is valid only for the first descriptor.
18	TSE	TCP Segmentation Enable When this bit is set, the DMA performs the TCP/UDP segmentation or UDP fragmentation for a packet depending on the TSE_MODE[1:0] bit of the DMA_CH(#i)_Tx_Control Register. This bit is valid only if the FD bit is set.
17:16	CIC/TPL	Checksum Insertion Control or TCP Payload Length These bits control the checksum calculation and insertion. The following list describes the bit encoding: ■ 2'b00: Checksum Insertion Disabled. ■ 2'b01: Only IP header checksum calculation and insertion are enabled.

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Bit	Name	Description
		■ 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. ■ 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit TCP/IP Checksum Offload option is selected and the TSE bit is reset. When the TSE bit is set, this field contains the upper bits [17:16] of the TCP Payload (or IP Payload for UDP fragmentation). This allows the TCP/UDP packet length field to be spanned across TDES3[17:0] to provide 256 KB packet length support. This field is valid only for the first descriptor.
15	TPL	Reserved or TCP Payload Length When the TSE bit is reset, this bit is reserved. When the TSE bit is set, this is Bit 15 of the TCP payload length [17:0]. This field is valid only when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected while configuring the core.
14:0	FL/TPL	Frame Length or TCP Payload Length This field is equal to the length of the packet to be transmitted in bytes. When the TSE bit is not set, this field is equal to the total length of the packet to be transmitted: Ethernet Header Length + TCP /IP Header Length – Preamble Length – SFD Length + Ethernet Payload Length When the TSE bit is set, this field is equal to the lower 15 bits of the TCP payload length in case of segmentation and IP payload in case of UDP fragmentation. In case of segmentation, this length does not includeEthernet header or TCP/UDP/IP header length. In case of fragmentation, this length does not include Ethernet header and IP header. When DWRR/WFQ algorithm is NOTenabled, value written into this field is not used when TSE = 0.

8.6.4 GMAC Transmit Normal Descriptor (Write-back Format)

The write-back format of the Transmit Descriptor includes timestamp low, timestamp high, OWN, and Status bits. The write-back format is applicable only for the last descriptor of the corresponding packet. The LD bit (TDES3[28]) is set in the descriptor where the DMA writes back the status and timestamp information for the corresponding Transmit packet. this format is only applicable to the last descriptor of a packet.

Table 8-8 TDES0 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for the corresponding Transmit packet. The DMA writes the timestamp only if TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and the Timestamp status (TTSS) bit is set

Table 8-9 TDES1 Normal Descriptor (Write-Back Format)

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Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High The DMA updates this field with the most significant 32 bits of the timestamp captured for corresponding transmit packet. The DMA writes the timestamp only if the TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

Table 8-10 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	Rsvd	Reserved

Table 8-11 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:24	Rsvd	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location after the first descriptor for a packet ■ All 1s ■ CTXT, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status register. Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:18	Rsvd	Reserved
17	TTSS	Tx Timestamp Status This status bit indicates that a timestamp has been captured for the corresponding transmit packet. When this bit is set, TDES0 and TDES1 have timestamp values that were captured for the Transmit packet. This field is

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Bit	Name	Description
		valid only when the Last Segment control bit (TDES3 [28]) in a descriptor is set. This bit is valid only when IEEE1588 timestamping feature is enabled; otherwise, it is reserved.
16	EUE	ECC Uncorrectable Error Status Indicates the ECC uncorrectable error in the TSO memory. Note: Uncorrectable error in Transmit FIFO memory is reported with (Bit 13) FF = 1. This is because, all such packets are flushed by GMAC.
15	ES	Error Summary This bit indicates the logical OR of the following bits: ■ TDES3[0]: IP Header Error ■ TDES3[14]: Jabber Timeout ■ TDES3[13]: Packet Flush ■ TDES3[12]: Payload Checksum Error ■ TDES3[11]: Loss of Carrier ■ TDES3[10]: No Carrier ■ TDES3[9]: Late Collision ■ TDES3[8]: Excessive Collision ■ TDES3[3]: Excessive Deferral ■ TDES3[2]: Underflow Error This bit is also set when EUE (bit 16) is set
14	JT	Jabber Timeout This bit indicates that the MAC transmitter has experienced a jabber time-out. This bit is set only when the JD bit of the MAC_Configuration register is not set.
13	PF	Packet Flushed This bit indicates that the DMA or MTL flushed the packet because of a software flush command given by the CPU.
12	PCE	Payload Checksum Error This bit indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either because of insufficient bytes, as indicated by the Payload Length field of the IP Header or the MTL starting to forward the packet to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet packet being transmitted to avoid deadlock, the MTL starts forwarding the packet when the FIFO is full, even in the store-and-forward mode. This error can also occur when Bus Error is detected during packet transfer. When the Full Checksum Offload engine is not enabled, this bit is reserved.
11	LoC	Loss of Carrier This bit indicates that Loss of Carrier occurred during packet transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during packet transmission). This is valid only for the packets transmitted without collision and when the MAC operates in the half-duplex mode.
10	NC	No Carrier This bit indicates that the carrier sense signal form the PHY was not asserted during transmission.

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Bit	Name	Description
9	LC	Late Collision This bit indicates that packet transmission was aborted because a collision occurred after the collision window (64 byte times including Preamble in MII mode and 512 byte times including Preamble and Carrier Extension in GMII mode). This bit is not valid if Underflow Error is set.
8	EC	Excessive Collision This bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after first collision and the transmission of the packet is aborted.
7:4	CC	Collision Count This 4-bit counter value indicates the number of collisions occurred before the packet was transmitted. The count is not valid when the EC bit is set.
3	ED	Excessive Deferral This bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000 Mbps mode or Jumbo Packet enabled mode) if DC bit is set in the MAC_Configuration register. When TBS is enabled in full duplex mode and this bit is set, it indicates that the frame has been dropped after the expiry time has reached.
2	UF	Underflow Error This bit indicates that the MAC aborted the packet because the data arrived late from the system memory. The underflow error can occur because of either of the following conditions: ■ The DMA encountered an empty Transmit Buffer while transmitting the packet ■ The application filled the MTL Tx FIFO slower than the MAC transmit rate The transmission process enter the suspended state and sets the underflow bit corresponding to a queue in the MTL_Interrupt_Status register.
1	DB	Deferred Bit This bit indicates that the MAC deferred before transmitting because of presence of carrier. This bit is valid only in the half-duplex mode.
0	IHE	IP Header Error When IP Header Error is set, this bit indicates that the Checksum Offload engine detected an IP header error. This bit is valid only when Tx Checksum Offload is enabled. Otherwise, it is reserved. If COE detects an IP header error, it still inserts an IPv4 header checksum if the Ethernet Type field indicates an IPv4 payload. In full duplex mode, when EST/Qbv is enabled and this bit is set, it indicates the frame drop status due to Frame Size error or Schedule Error.

8.6.5 GMAC Transmit Context Descriptor

The context descriptor is used to provide the timestamps for one-step timestamp correction, VLAN Tag ID for VLAN insertion feature. The Transmit Context descriptor can be provided any time before a packet descriptor. The context is valid for the current packet and subsequent packets. The context descriptor is used to provide the timestamps for one-

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step timestamp correction and VLAN Tag ID for VLAN insertion feature. Write back is done on a context descriptor only to reset the OWN bit.

Table 8-12 TDES0 Context Descriptor

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low For one-step correction, the driver can provide the lower 32 bits of timestamp in this descriptor word. The DMA uses this value as the low word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 8-13 TDES1 Context Descriptor

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High For one-step correction, the driver can provide the upper 32 bits of timestamp in this descriptor. The DMA uses this value as the high word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 8-14 TDES2 Context Descriptor

Bit	Name	Description
31:16	IVT	Inner VLAN Tag When the IVLTV bit of TDES3 context descriptor is set and the TCMSSV and OSTC bits of TDES3 context descriptor are reset, TDES2[31:16] contains the inner VLAN Tag to be inserted in the subsequent Transmit packets.
15:14	Rsvd	Reserved
13:0	MSS	Maximum Segment Size When the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected, the driver can provide maximum segment size in this field. This segment size is used while segmenting the TCP/IP payload. This field is valid only if the TCMSSV bit of TDES3 context descriptor is set and the OSTC bit of the TDES3 context descriptor is reset.

Table 8-15 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit immediately after the read.
30	CTXT	Context Type This bit should be set to 1'b1 for Context descriptor.
29:28	Rsvd	Reserved
27	OSTC	One-Step Timestamp Correction Enable When this bit is set, the DMA performs a one-step timestamp correction with reference to the timestamp values provided in TDES0 and TDES1.
26	TCMSSV	One-Step Timestamp Correction Input or MSS Valid When this bit and the OSTC bit are set, it indicates that the Timestamp Correction input provided in TDES0 and TDES1 is valid. When the OSTC bit is reset and this bit and the TSE bit of TDES3 are set in subsequent normal descriptor, it indicates that the MSS input in TDES2 is valid.

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Bit	Name	Description
25:24	Rsvd	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect.The DMA sets this bit during write-back while closing the context descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location before the first descriptor for a packet ■ All 1s ■ CD, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status Register. Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:20	Rsvd	Reserved
19:18	IVTIR	Inner VLAN Tag Insert or Replace When this bit is set, these bits request the MAC to perform Inner VLAN tagging or un-tagging before transmitting the packets. If the packet is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits: ■ 2'b00: Do not add the inner VLAN tag. ■ 2'b01: Remove the inner VLAN tag from the packets before transmission. This option should be used only with the VLAN frames. ■ 2'b10: Insert an inner VLAN tag with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the inner VLAN tag in packets with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. This option should be used only with the VLAN frames. These bits are valid when the Enable SA and VLAN Insertion on Tx and Enable Double VLAN Processing options are selected.
17	IVLTV	Inner VLAN Tag Valid When this bit is set, it indicates that the IVT field of TDES2 is valid.
16	VLTV	VLAN Tag Valid When this bit is set, it indicates that the VT field of TDES3 is valid.
15:0	VT	VLAN Tag This field contains the VLAN Tag to be inserted or replaced in the packet. This field is used as VLAN Tag only when the VLTI bit of the MAC_VLAN_Incl register is reset.

8.6.6 GMAC Receive Descriptors

The DMA in GMAC attempts to read a descriptor only if the Tail Pointer is different from the Base Pointer or current pointer. It is recommended to have a descriptor ring with a length

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that can accommodate at least two complete packets received by the MAC. Otherwise, the performance of the DMA is impacted greatly because of the unavailability of the descriptors. In such situations, the RxFIFO in MTL becomes full and starts dropping packets.

The following Receive Descriptors are present:

- Normal descriptors
- Context descriptors

All RX descriptors are prepared by the software and given to the DMA as "Normal" Descriptors with the content as shown in Receive Normal Descriptor (Read Format). The DMA reads this descriptor and after transferring a received packet (or part of) to the buffers indicated by the descriptor, the Rx DMA will close the descriptor with the corresponding packet status. The format of this status is given in the "Receive Normal Descriptor (Write-Back Format)". For some packets, the normal descriptor bits are not enough to write the complete status. For such packets, the RX DMA writes the extended status to the next descriptor (without processing or using the Buffers/ Pointers embedded in that descriptor). The format and content of the descriptor write back is described in "Receive Context Descriptor".

8.6.7 GMAC Receive Normal Descriptors(Read Format)

Table 8-16 TDES0 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	BUF1AP	Header or Buffer 1 Address Pointer When the SPH bit of Control register of a channel is reset, these bits indicate the physical address of Buffer 1. When the SPH bit is set, these bits indicate the physical address of Header Buffer where the Rx DMA writes the L2/L3/L4 header bytes of the received packet. The application can program a byte-aligned address for this buffer which means that the LS bits of this field can be non-zero. However, while transferring the start of packet, the DMA performs a Write operation with RDES0[1:0] (or RDES0[2:0]/[3:0] in case of 64-/128-bit configuration) as zero. However, the packet data is shifted as per actual offset as given by buffer address pointer. If the address pointer points to a buffer where the middle or last part of the packet is stored, the DMA ignores the offset address and writes to the full location as indicated by the data-width.

Table 8-17 TDES1 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 8-18 TDES2 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 8-19 TDES3 Normal Descriptor(Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the

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Bit	Name	Description
		application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	IOC	Interrupt Enabled on Completion When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor.
29:26	Rsvd	Reserved
25	BUF2V	Buffer 2 Address Valid When this bit is set, it indicates to the DMA that the buffer 2 address specified in RDES2 is valid. The application must set this bit so that the DMA can use the address, to which the Buffer 2 address in RDES2 is pointing, to write received packet data.
24	BUF1V	Buffer 1 Address Valid When set, this indicates to the DMA that the buffer 1 address specified in RDES1 is valid. The application must set this value if the address pointed to by Buffer 1 address in RDES1 can be used by the DMA to write received packet data.
23:0	Rsvd	Reserved

8.6.8 GMAC Receive Normal Descriptors(Write-Back Format)

Table 8-20 TDES0 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	IVT	Inner VLAN Tag This field contains the Inner VLAN tag of the received packet if the RS0V bit of RDES3 is set. This is valid only when Double VLAN tag processing and VLAN tag stripping are enabled.
15:0	OVT	Outer VLAN Tag This field contains the Outer VLAN tag of the received packet if the RS0V bit of RDES3 is set.

Table 8-21 TDES1 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	OPC	OAM Sub-Type Code, or MAC Control Packet opcode OAM Sub-Type Code If Bits[18:16] of RDES3 are set to 3'b111, this field contains the OAM sub-type and code fields. MAC Control Packet opcode If Bits[18:16] of RDES3 are set to 3'b110, this field contains the MAC Control packet opcode field.
15	TD	Timestamp Dropped This bit indicates that the timestamp was captured for this packet but it got dropped in the MTL Rx FIFO because of overflow. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
14	TSA	Timestamp Available When Timestamp is present, this bit indicates that the timestamp value is available in a context descriptor word 2 (RDES2) and word 1(RDES1). This is valid only when the Last Descriptor bit (RDES3 [28]) is set. The context descriptor is written in the next descriptor just after the last normal descriptor for a packet.
13	PV	PTP Version

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Bit	Name	Description
		This bit indicates that the received PTP message has the IEEE 1588 version 2 format. When this bit is reset, it indicates the IEEE 1588 version 1 format. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
12	PFT	PTP Packet Type This bit indicates that the PTP message is sent directly over Ethernet. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
11:8	PMT	PTP Message Type These bits are encoded to give the type of the message received: ■ 0000: No PTP message received ■ 0001: SYNC (all clock types) ■ 0010: Follow_Up (all clock types) ■ 0011: Delay_Req (all clock types) ■ 0100: Delay_Resp (all clock types) ■ 0101: Pdelay_Req (in peer-to-peer transparent clock) ■ 0110: Pdelay_Resp (in peer-to-peer transparent clock) ■ 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) ■ 1000: Announce ■ 1001: Management ■ 1010: Signaling ■ 1011–1110: Reserved ■ 1111: PTP packet with Reserved message type These bits are available only when you select the Timestamp feature.
7	IPCE	IP Payload Error When this bit is set, it indicates either of the following: ■ The 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) calculated by the MAC does not match the corresponding checksum field in the received segment. ■ The TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. ■ The TCP, UDP, or ICMP segment length is less than minimum allowed segment length for TCP, UDP, or ICMP. Bit 15 (ES) of RDES3 is not set when this bit is set.
6	IPCB	IP Checksum Bypassed This bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
5	IPV6	IPv6 header Present This bit indicates that an IPV6 header is detected. When the Enable Split Header Feature option is selected and the SPH bit of Control Register of a channel is set, the IPV6 header is available in the header buffer area to which RDES0 is pointing.
4	IPV4	IPV4 Header Present This bit indicates that an IPV4 header is detected. When the SPH bit of RDES3 is set, the IPV4 header is available in the header buffer area to which RDES0 is pointing.
3	IPHE	IP Header Error When this bit is set, it indicates either of the following:

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Bit	Name	Description
		■ The 16-bit IPv4 header checksum calculated by the MAC does not match the received checksum bytes. ■ The IP datagram version is not consistent with the Ethernet Type value. ■ Ethernet packet does not have the expected number of IP header bytes. This bit is valid when either Bit 5 or Bit 4 is set. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
2:0	PT	Payload Type These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE): ■ 3'b000: Unknown type or IP/AV payload not processed ■ 3'b001: UDP ■ 3'b010: TCP ■ 3'b011: ICMP ■ 3'b110: AV Tagged Data Packet ■ 3'b111: AV Tagged Control Packet ■ 3'b101: AV Untagged Control Packet ■ 3'b100: IGMP if IPV4 Header Present bit is set else DCB (LLDP) Control Packet If the COE does not process the payload of an IP datagram because there is an IP header error or fragmented IP, it sets these bits to 3'b000.

Table 8-22 TDES2 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:29	L3L4FM	Layer 3 and Layer 4 Filter Number Matched These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received packet: ■ 000: Filter 0 ■ 001: Filter 1 ■ 010: Filter 2 ■ 011: Filter 3 ■ 100: Filter 4 ■ 101: Filter 5 ■ 110: Filter 6 ■ 111: Filter 7 This field is valid only when Bit 28 or Bit 27 is set high. When more than one filter matches, these bits give the number of lowest filter. Note: This status is not available when Flexible RX Parser is enabled.
28	L4FM	Layer 4 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true: ■ Layer 3 fields are not enabled and all enabled Layer 4 fields match ■ All enabled Layer 3 and Layer 4 filter fields match When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.

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Bit	Name	Description
27	L3FM	Layer 3 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true: ■ All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed ■ All enabled filter fields match When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.
26:19	MADRM	MAC Address Match or Hash Value When the HF bit is reset, this field contains the MAC address register number that matched the Destination address of the received packet. This field is valid only if the DAF bit is reset. When the HF bit is set, this field contains the hash value computed by the MAC. A packet passes the hash filter when the bit corresponding to the hash value is set in the hash filter register. Note: This status is not available when Flexible RX Parser is enabled.
18	HF	Hash Filter Status When this bit is set, it indicates that the packet passed the MAC address hash filter. Bits[26:19] indicate the hashvalue. Note: This status is not available when Flexible RX Parser is enabled.
17	DAF/RXPI	Destination Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the DA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet parsing is incomplete (RXPI) due to ECC error. Note: When this bit is set, ES bit of RDES3 is also set.
16	SAF/RXPD	SA Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the SA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet is dropped (RXPD) by the parser. Note: When this bit is set, ES bit of RDES3 is also set.
15	OTS	VLAN Filter Status When set, this bit indicates that the VLAN Tag of the received packed passed the VLAN filter. This bit is valid only when DWC_GMAC_ERVFE is not enabled. If DWC_GMAC_ERVFE is enabled, the bit is redefined as Outer VLAN Tag Filter Status (OTS). This bit is valid for both Single and Double VLAN Tagged frames.
14	ITS	Inner VLAN Tag Filter Status (ITS) This bit is valid only when DWC_GMAC_ERVFE is enabled. This bit is valid only for Double VLAN Tagged frames, when Double VLAN Processing is enabled. For more information, see the Filter Status topic.

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Bit	Name	Description
13:11	Rsvd	Reserved
10	ARPNR	ARP Reply Not Generated When this bit is set, it indicates that the MAC did not generate the ARP Reply for received ARP Request packet. This bit is set when the MAC is busy transmitting ARP reply to earlier ARP request (only one ARP request is processed at a time). This bit is reserved when the Enable IPv4 ARP Offload option is not selected.
9:0	HL	L3/L4 Header Length This field contains the length of the header of the packet split by the MAC at L3 or L4 header. boundary as identified by the MAC receiver. This field is valid only when the first descriptor bit is set (FD = 1). The header data is written to the Buffer 1 address of corresponding descriptor. If header length is zero, this field is not valid. It implies that the MAC did not identify and split the header. This field is valid when the Enable Split Header Feature option is selected.

Table 8-23 TDES3 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context type descriptor. The DMA writes 1'b0 to this bit for normal receive descriptor. When CTXT and FD bits are used together, {CTXT, FD} ■ 2'b00: Intermediate Descriptor ■ 2'b01: First Descriptor ■ 2'b10: Reserved ■ 2'b11: Descriptor Error (due to all 1s) Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	FD	First Descriptor When this bit is set, it indicates that this descriptor contains the first buffer of the packet. If the size of the first buffer is 0, the second buffer contains the beginning of the packet. If the size of the second buffer is also 0, the next descriptor contains the beginning of the packet. See the CTXT bit description for details of using the CTXT bit and FD bit together.
28	LD	Last Descriptor

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Bit	Name	Description
		When this bit is set, it indicates that the buffers to which this descriptor is pointing are the last buffers of the packet.
27	RS2V	Receive Status RDES2 Valid When this bit is set, it indicates that the status in RDES2 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
26	RS1V	Receive Status RDES1 Valid When this bit is set, it indicates that the status in RDES1 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
25	RS0V	Receive Status RDES0 Valid When this bit is set, it indicates that the status in RDES0 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
24	CE	CRC Error When this bit is set, it indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received packet. This field is valid only when the LD bit of RDES3 is set.
23	GP	Giant Packet When this bit is set, it indicates that the packet length exceeds the specified maximum Ethernet size of 1518, 1522, or 2000 bytes (9018 or 9022 bytes if jumbo packet enable is set). Note: Giant packet indicates only the packet length. It does not cause any packet truncation.
22	RWT	Receive Watchdog Timeout When this bit is set, it indicates that the Receive Watchdog Timer has expired while receiving the current packet. The current packet is truncated after watchdog timeout.
21	OE	Overflow Error When this bit is set, it indicates that the received packet is damaged because of buffer overflow in Rx FIFO. Note: This bit is set only when the DMA transfers a partial packet to the application. This happens only when the Rx FIFO is operating in the threshold mode. In thestore-and-forward mode, all partial packets are dropped completely in Rx FIFO.
20	RE	Receive Error When this bit is set, it indicates that the gmii_rxer_i signal is asserted while the gmii_rxdv_i signal is asserted during packet reception. This error also includes carrier extension error in the GMII and half-duplex mode. Error can be of less or no extension, or error (rxd!= 0f) during extension.
19	DE	Dribble Bit Error When this bit is set, it indicates that the received packet has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.
18:16	LT	Length/Type Field This field indicates if the packet received is a length packet or a type packet. The encoding of the 3 bits is as follows: ■ 3'b000: The packet is a length packet ■ 3'b001: The packet is a type packet. ■ 3'b011: The packet is a ARP Request packet type

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Bit	Name	Description
		■ 3'b100: The packet is a type packet with VLAN Tag ■ 3'b101: The packet is a type packet with Double VLAN Tag ■ 3'b110: The packet is a MAC Control packet type ■ 3'b111: The packet is a OAM packet type ■ 3'b010: Reserved
15	ES	Error Summary When this bit is set, it indicates the logical OR of the following bits: ■ RDES3[24]: CRC Error ■ RDES3[19]: Dribble Error ■ RDES3[20]: Receive Error ■ RDES3[22]: Watchdog Timeout ■ RDES3[21]: Overflow Error ■ RDES3[23]: Giant Packet ■ RDES2[17]: Destination Address Filter Fail, when Flexible RX Parser is enabled ■ RDES2[16]: SA Address Filter Fail, when Flexible RX Parser is enabled This field is valid only when the LD bit of RDES3 is set.
14	PL	Packet Length These bits indicate the byte length of the received packet that was transferred to system memory (including CRC). This field is valid when the LD bit of RDES3 is set and Overflow Error bits are reset. The packet length also includes the two bytes appended to the Ethernet packet when IP checksum calculation is enabled and the received packet is not a MAC control packet. This field is valid when the LD bit of RDES3 is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current packet.

8.6.9 GMAC Receive Context Descriptor

This descriptor is read-only for the application. Only the DMA can write to this descriptor. The context descriptor provides information about the extended status related to the last received packet. The Bit 30 of RDES3 indicates the context type descriptor.

Table 8-24 TDES0 Context Descriptor

Bit	Name	Description
31:0	RSTL	Receive Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for corresponding Receive packet. When this field and the RTSH field of RDES1 show all-ones value, the timestamp must be considered as corrupt.

Table 8-25 TDES1 Context Descriptor

Bit	Name	Description
31:0	RSTH	Receive Packet Timestamp High The DMA updates this field with most significant 32 bits of the timestamp captured for corresponding receive packet. When this field and the RTSL field of RDES0 show all-ones value, the timestamp must be considered as corrupt.

Table 8-26 TDES2 Context Descriptor

Bit	Name	Description
31:0	Rsvd	Reserved

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Table 8-27 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context descriptor. The DMA writes 1'b1 to this bit for context descriptor. DMA writes 2'b11 to indicate adescriptor error due to all 1s. When CTXT and DE bits are used together, {CTXT, DE} ■ 2'b00: Reserved ■ 2'b01: Reserved ■ 2'b10: Context Descriptor ■ 2'b11: Descriptor Error Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	DE	Descriptor Error See the CTXT bit description for details of using theDE bit along with CTXT bit.
28:0	Rsvd	Reserved

8.6.10 GMAC Programming Guide

8.6.10.1 Initializing DMA

Complete the following steps to initialize the DMA:
1. Provide a software reset. This resets all of the MAC internal registers and logic (bit-0 of DMA_Mode).
2. Wait for the completion of the reset process (poll bit 0 of the DMA_Mode, which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the DMA_SysBus_Mode register:
a. AAL
b. Fixed burst or undefined burst
c. Burst mode values in case of AHB bus interface, OSR_LMT in case of AXI bus interface.
d. If fixed length value is enabled, select the maximum burst length possible on the AXI Bus (bits [7:1])
4. Create a descriptor list for transmit and receive. In addition, ensure that the descriptors are owned by DMA (set bit 31 of descriptor TDES3/RDES3). For more information about descriptors, see section "Descriptors".
5. Program the Transmit and Receive Ring length registers (DMA_CH(#i)_TxDesc_Ring_Length (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Ring_Length (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1)). The ring length programmed must be at least 4.
6. Initialize receive and transmit descriptor list address with the base address of the transmit and receive descriptor (DMA_CH(#i)_TxDesc_List_Address (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1), DMA_CH(#i)_RxDesc_List_Address (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1)). Also, program transmit and receive tail pointer

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registers indicating to the DMA about the available descriptors (DMA_CH(#i)_TxDesc_Tail_Pointer (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Tail_Pointer (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1)).
7. Program the settings of the following registers for the parameters like maximum burst-length (PBL) initiated by DMA, descriptor skip lengths, OSP in case of TxDMA, RBSZ in case of RxDMA, and so on:

- DMA_CH(#i)_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_RX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1)

8. Enable the interrupts by programming the DMA_CH(#i)_Interrupt_Enable (for i = 0; i <=
DWC_GMAC_NUM_DMA_TX_CH-1) register.
9. Start the Receive and Transmit DMAs by setting SR (bit 0) of theDMA_CH(#i)_RX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1) and ST (bit 0) of the DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1)register.
10. Repeat steps 4 to 9 for all the Tx DMA and Rx DMA channels selected in the hardware.

8.6.10.2 Initializing MTL Registers

The Transaction Layer (MTL) registers must be initialized to establish the transmit and receive operating modes and commands.
Complete the following steps to initialize the MTL registers:
1. Program the Tx Scheduling (SCHALG) and Receive Arbitration Algorithm (RAA) fields in MTL_Operation_Mode to initialize the MTL operation in case of multiple Tx and Rx queues.
2. Program the Receive Queue to DMA mapping in MTL_RxQ_DMA_Map0 andMTL_RxQ_DMA_Map1 registers.
3. Program the following fields to initialize the mode of operation in the MTL_TxQ0_Operation_Mode register.
a. Transmit Store And Forward (TSF) or Transmit Threshold Control (TTC) in case of threshold mode
b. Transmit Queue Enable (TXQEN) to value 2'b10 to enable Transmit Queue0
c. Transmit Queue Size (TQS)
4. Program the following fields to initialize the mode of operation in the MTL_RxQ0_Operation_Mode register:
a. Receive Store and Forward (RSF) or RTC in case of Threshold mode
b. Flow Control Activation and De-activation thresholds for MTL Receive FIFO (RFA and RFD)
c. Error Packet and undersized good Packet forwarding enable (FEP and FUP)
d. Receive Queue Size (RQS)
5. Repeat previous two steps for all MTL Tx and Rx queues selected in the configuration.

8.6.10.3 Initializing MAC

The MAC configuration registers establish the operating mode of the MAC. These registers must be initialized before initializing the DMA.
The following MAC Initialization operations can be performed after DMA initialization. If the MAC initialization is completed before the DMA is configured, enable the MAC receiver (last step in the following sequence) only after the DMA is active. Otherwise, received frames fill the Rx FIFO and overflow.
1. Provide the MAC address registers: MAC_Address0_High and MAC_Address0_Low. If more than one MAC address is enabled in your configuration, program the MAC addresses appropriately.
2. Program the following fields to set the appropriate filters for the incoming frames in the MAC_Packet_Filter register:
a. Receive All
b. Promiscuous mode
c. Hash or Perfect Filter
d. Unicast, multicast, broadcast, and control frames filter settings
3. Program the following fields for proper flow control in the MAC_Q0_Tx_Flow_Ctrlregister:
a. Pause time and other Pause frame control bits

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b. Transmit Flow control bits
c. Flow Control Busy
4. Program the MAC_Interrupt_Enable register, as required, and if applicable, for your configuration.
5. Program the appropriate fields in the MAC_Configuration register. For ex: Inter-packet gap while transmission and jabber disable.
6. Set bit 0 and 1 in MAC_Configuration registers to start the MAC transmitter and receiver.

8.6.10.4 Performing Normal Receive and Transmit Operation

During normal operation of the GMAC, normal and transmit interrupts are read, descriptors polled, the DMA is suspended (if it does not own descriptors), and values of current host transmitter or receiver descriptor pointers are read for debugging.
For normal operation, complete the following steps:
1. For normal transmit and receive interrupts, read the interrupt status. Then, poll the descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).
2. Set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
3. If the descriptors are not owned by the DMA (or no descriptor is available), the DMA goes into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and writing the descriptor tail pointer to Tx/Rx tail pointer register (DMA_CH[n]_TxDesc_Tail_Pointer and DMA_CH[n]_RxDesc_Tail_Pointer).
4. The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (DMA_CH[n]_Current_App_TxDesc andDMA_CH[n]_Current_App_RxDesc).
5. The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (Register DMA_CH[n]_Current_App_TxBuffer and DMA_CH[n]_Current_App_RxBuffer)

8.6.10.5 Stopping and Starting Transmission

Complete the following steps to pause the transmission for some time.
1. Disable the Transmit DMA (if applicable) by clearing Bit 0 (ST) of DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1) Register.
2. Wait for any previous frame transmissions to complete. You can check this by reading the appropriate bits of MTL_TxQ0_Debug Register (TRCSTS is not 01 and TXQSTS=0).
3. Disable the MAC transmitter and MAC receiver by clearing Bit (RE) and Bit 1(TE) of the MAC_Configuration Register.
4. Disable the Receive DMA (if applicable), after making sure that the data in the Rx FIFO is transferred to the system memory (by reading the appropriate bits of MTL_TxQ0_Debug Register, PRXQ=0 and RXQSTS=00).
5. Make sure that both Tx Queue and Rx Queue are empty (TXQSTS is 0 inMTL_TxQ0_Debug Register and RXQSTS is 0 in MTL_RxQ0_Debug Register).
6. To restart the operation, first start the DMAs, and then enable the MAC Transmitter and Receiver.

8.6.10.6 Initialization Guidelines for System Time Generation

You can enable the timestamp feature by setting Bit 0 of the MAC_Timestamp_Control Register. However, it is essential that the timestamp counter be initialized after this bit is set. Complete the following steps during GMAC initialization:
1. Mask the Timestamp Trigger interrupt by clearing the bit 16 of MAC_Interrupt_Enable Register.
2. Set Bit 0 of MAC_Timestamp_Control Register to enable timestamping.
3. Program MAC_Sub_Second_Increment Register based on the PTP clock frequency.
4. If you are using the Fine Correction approach, program MAC_Timestamp_Addend and set Bit 5 of MAC_Timestamp_Control Register.
5. Poll the MAC_Timestamp_Control Register until Bit 5 is cleared.
6. Program Bit 1 of MAC_Timestamp_Control Register to select the Fine Update method (if required).
7. Program MAC_System_Time_Seconds_Update Register andMAC_System_Time_Nanoseconds_Update Register with the appropriate time value.

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8. Set Bit 2 in MAC_Timestamp_Control Register.
The timestamp counter starts operation as soon as it is initialized with the value written in the Timestamp Update registers. If one-step timestamping is enabled
a. To enable one-step timestamping, program Bit 27 of the TDES3 Context Descriptor.
b. Program registers MAC_Timestamp_Ingress_Asym_Corr andMAC_Timestamp_Egress_Asym_Corr to update the correction field in PDelay_Req PTP messages.
9. Enable the MAC receiver and transmitter for proper timestamping.

8.6.10.7 Coarse Correction Method

To synchronize or update the system time in one process (coarse correction method), complete the following steps:
1. Set the offset (positive or negative) in the Timestamp Updateregisters(MAC_System_Time_Seconds_Update andMAC_System_Time_Nanoseconds_Update).
2. Set Bit 3 (TSUPDT) of MAC_Timestamp_Control Register. The value in the Timestamp Update registers is added to or subtracted from the system time when the TSUPDT bit is cleared.

8.6.10.8 Programming Guidelines for TSO

The TCP Segmentation Offload (TSO) engine is used to offload the TCP segmentation functions to the hardware. To program the TSO, set the TSE bit to enable TCP packet segmentation, and program descriptor fields to enable TSO for the current packet. Complete the following steps to program TSO:
1. Program the TSE bit of corresponding DMA_CH[n]_Tx_Control register to enable TCP packet segmentation in that DMA.
2. In addition to the normal transfer descriptor setting, the following descriptor fields must be programmed to enable TSO for the current packet:
a. Enable TSE in Bit 18 of TDES3
b. Program the length of the un-segmented TCP/IP packet payload in bits [17:0] of TDES3 and the TCP header in bits [22:19] of TDES3.
c. Program the maximum size of the segment in MSS of DMA_CH[n]_Control register or MSS in the context descriptor. If MSS field is programmed in both DMA_CH[n]_Control register and in the context descriptor, the latest software programmed sequence is considered.
3. The header of the unsegmented TCP/IP packet should be in Buffer 1 of the first descriptor and this buffer must not hold any payload bytes. The payload is allocated to Buffer 2 and the buffers of the subsequent descriptors.

8.6.11 GMAC Clock Architecture

In RMII mode, reference clock and TX/RX clock can be from CRU or external OSC as following figure.

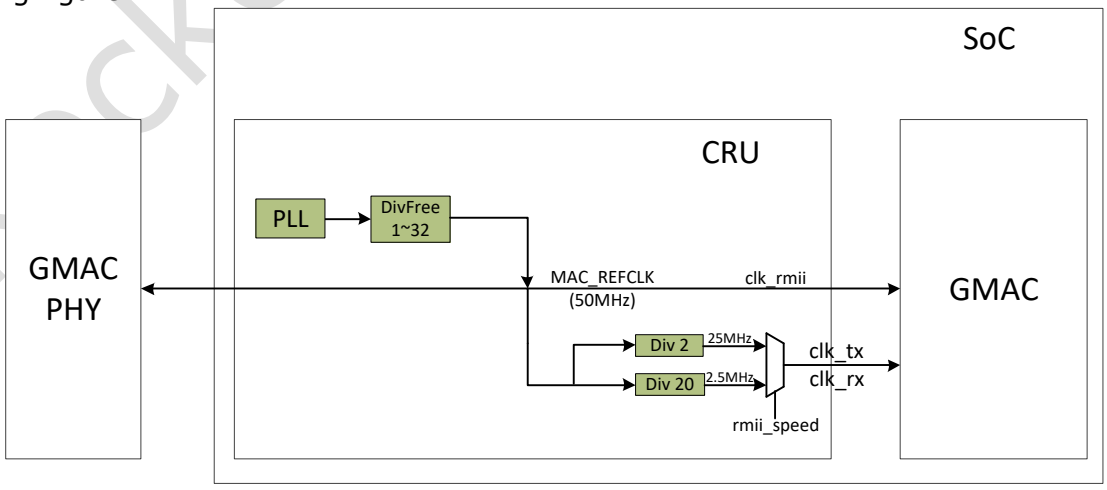

Fig. 8-11 RMII Clock Architecture When Clock Source From CRU

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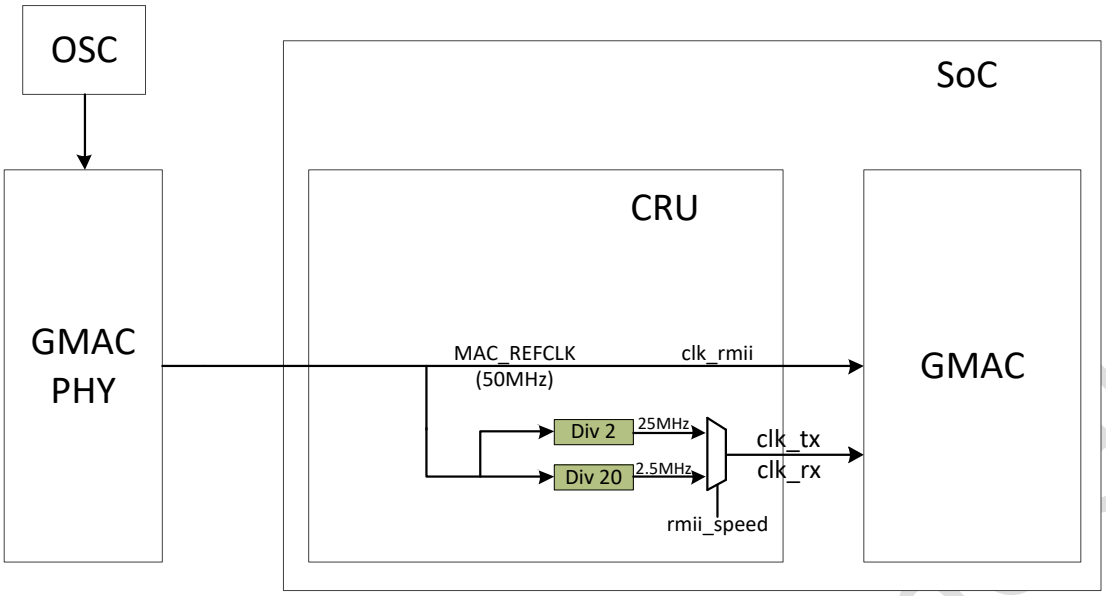

Fig. 8-12 RMII Clock Architecture When Clock Source From External OSC

In RGMII mode, clock architecture only supports that TX clock source is from CRU as following figure. In order to dynamically adjust the timing between TX/RX clocks with data, delay line is integrated in TX and RX clock path.

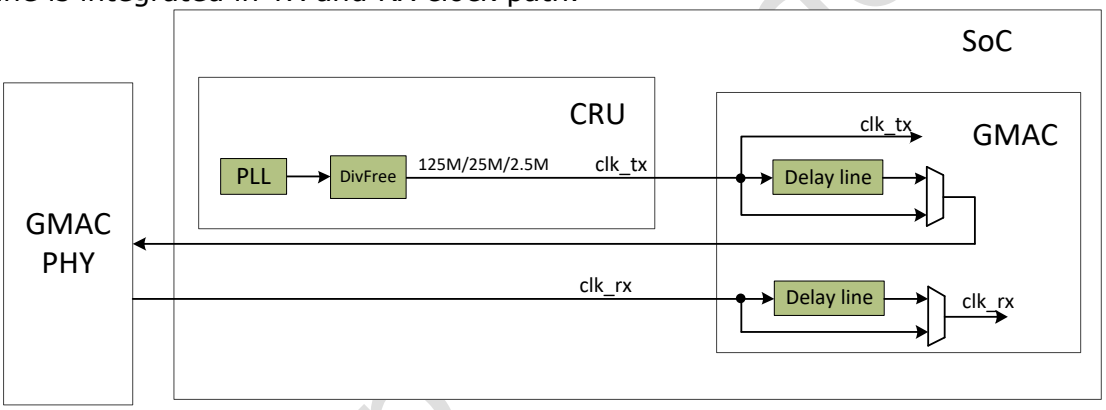

Fig. 8-13 RGMII Clock Architecture When Clock Source From CRU

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Chapter 9 RMII-Only Media Access Controller (MAC100)

9.1 Overview

RMII-Only Media Access Controller in this charpter, we named it MAC100 Controller. We also named it GMAC1 or MAC1 in some applications.
MAC100 Controller provides only an Ethernet interface from processor to a Reduced Media Independent Interface(RMII).
They each have DMAC controller.The DMA controller efficiently moves packet data from microprocessor's RAM, formats the data for an IEEE 802.3-2002 compliant packet and transmits the data to an Ethernet Physical Interface (PHY). It also efficiently moves packet data from RXFIFO to microprocessor's RAM.

9.1.1 Features

Every feature item has been marked that whether it belong to EQOS or MAC100 or both of them.

9.1.1.1 Tx and Rx Common Features

- Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
- Supports 10/100-Mbps data transfer rates with the RMII interfaces
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support (based on implementation-specific whitepapers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
  - Packet bursting and packet extension in 1000 Mbps half-duplex operation
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet in Reduced Gigabit Media Independent Interface (RGMII) PHYs
- 64-bit data transfer interface on the application side
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- Media clock generation and recovery
- MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

9.1.1.2 Tx Features

- Preamble and start of packet data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-packet basis
- Programmable packet length to support Standard or Jumbo Ethernet packets with up to16 KB of size
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flowcontrol input transitions from assertion to de-assertion (in full-duplex mode)
- Frame Preemption for MAC Tx

9.1.1.3 Rx Features

- Automatic Pad and CRC Stripping options
- Option to disable Automatic CRC checking
- Preamble and SFD deletion
- Separate 112-bit or 128-bit status
- Programmable watchdog timeout limit
- IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- Frame Preemption for MAC Rx

9.1.2 MTL Features

9.1.2.1 MTL Tx and Rx Common Features

- 32-bit, 64-bit, or 128-bit Transaction Layer block (bridges the application and the MAC)
- Data transfers executed using simple FIFO protocol
- Synchronization for all clocks in the design (Transmit, Receive, and Application clocks)
- Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size.

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- Programmable threshold capability for each queue (default of 64 bytes)

9.1.2.2 MTL Tx Features

- Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- Programmable queue size in configurations with multiple queues. Each queue size can be programmed in terms of 256 bytes
- Automatic retransmission of collision packets in half-duplex mode
- Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- Disabling of Data Memory RAM chip-select when inactive to reduce power consumption

9.1.2.3 MTL Rx Features

- Rx queue sizes in the Receive path is 32 KB
- Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in Store-and-Forward mode) in EQOS-MTL configuration
- Programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level

9.1.3 DMA Block Features

- 64-bit data transfers
- Separate DMA channel in the Transmit path for each queue in MTL
- Single or multiple DMA channels for any number of queues in MTL Receive path
- Fully synchronous design operating on a single application clock (except for CSR module, when a separate CSR clock is configured)
- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) descriptor support
- Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-packet Transmit or Receive Complete Interrupt control
- Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- Start and Stop modes
- Separate ports for host CSR access and host data interface
- support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO)
- Selectable number of Tx DMA channels with TSO/USO feature enabled
- Programmable control for Transmit Descriptor posted writes to improve the throughput
- Sideband signals to control starting and stopping of DMA channels

9.2 Block Diagram

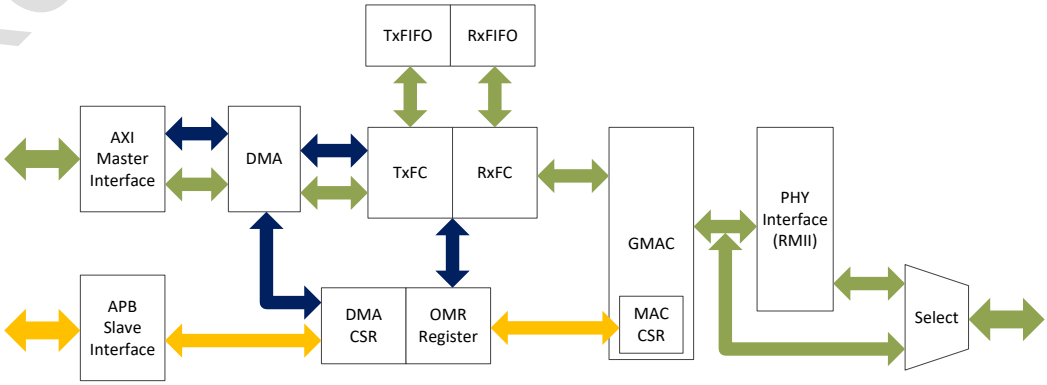

Fig. 9-1MAC100 Architecture

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The MAC is broken up into multiple separate functional units. These blocks are interconnected in the MAC module. The block diagram shows the general flow of data and control signals between these blocks.
The MAC transfers data to system memory through the AXI master interface. The host CPU uses the APB Slave interface to access the MAC subsystem's control and status registers (CSRs).
The MAC supports the PHY interfaces of reduced MII (RMII).
The Transmit FIFO (Tx FIFO) buffers data read from system memory by the DMA before transmission by the MAC Core. Similarly, the Receive FIFO (Rx FIFO) stores the Ethernet frames received from the line until they are transferred to system memory by the DMA. These are asynchronous FIFOs, as they also transfer the data between the application clock and the MAC line clocks.

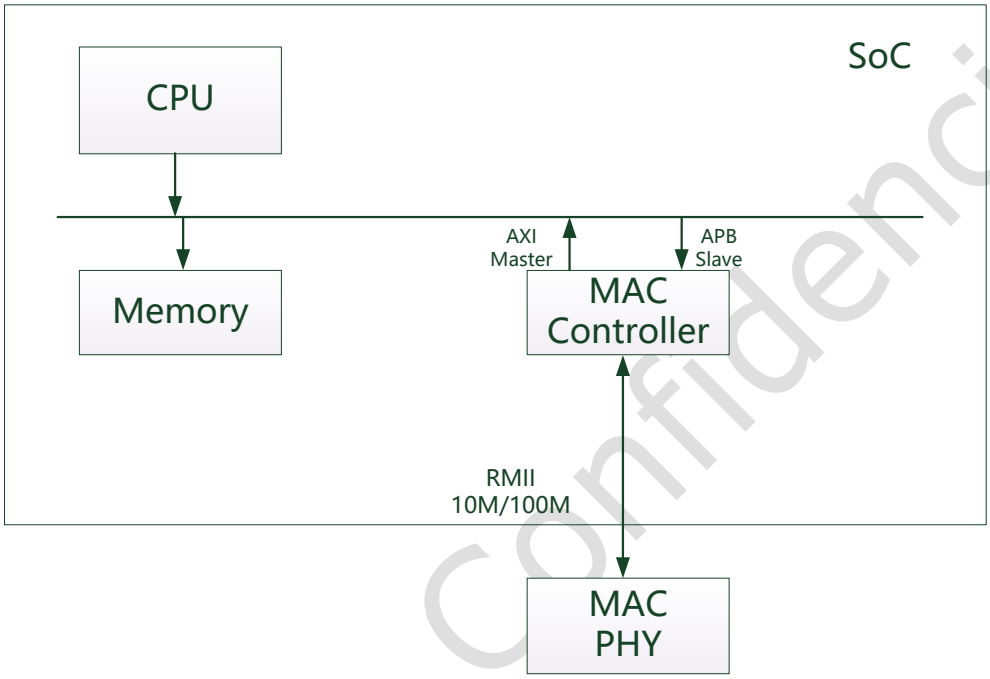

Fig. 9-2MACBlock Diagram

The MAC controller named MAC2IO:

- MAC2IO Supports 10/100-Mbps data transfer rates with the RMII interfaces

9.3 Function Description

9.3.1 Frame Structure

Data frames transmitted shall have the frame format shown in the following figure.

Fig. 9-3MAC100Frame Structure

The preamble <preamble> begins a frame transmission. The bit value of the preamble field consists of 7 octets with the following bit values:
10101010 10101010 10101010 10101010 10101010 10101010 10101010
The SFD (start frame delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value is 10101011.
The data in a well formed frame shall consist of N octet's data.

9.3.2 RMII Interface timing diagram

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. In devices incorporating multiple MAC100 or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port - a 62.5% decrease in pin count.
The RMII module is instantiated between the MAC100 and the PHY. This helps translation of the MAC100's MII into the RMII. The RMII block has the following characteristics:

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- Supports 10-Mbps and 100-Mbps operating rates. It does not support 1000-Mbps operation.
- Two clock references are sourced externally or CRU, providing independent, 2-bit wide transmit and receive paths.

Transmit Bit Ordering

Each nibble from the MII must be transmitted on the RMII a di-bit at a time with the order of di-bit transmission shown in the following figure. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

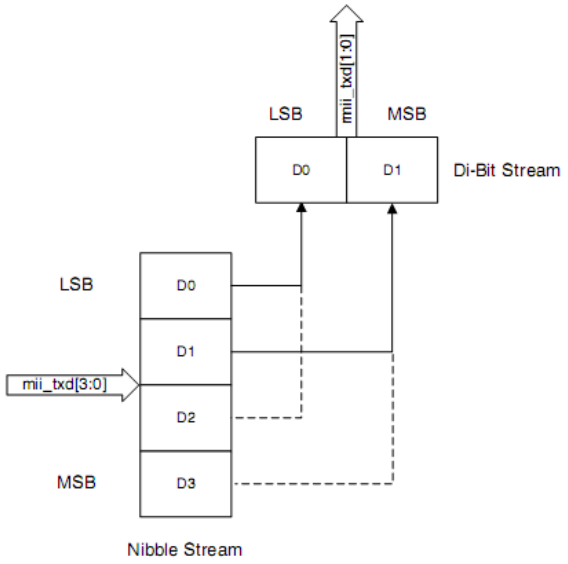

Fig. 9-4 RMII transmission bit ordering

RMII Transmit Timing Diagrams

The following figures show MII-to-RMII transaction timing. The clk_rmii_i (REF_CLK) frequency is 50MHz in RMII interface. In 10Mb/s mode, as the REF_CLK frequency is 10 times as the data rate, the value on rmii_txd_o[1:0] (TXD[1:0]) shall be valid such that TXD[1:0] may be sampled every 10th cycle, regard-less of the starting cycle within the group and yield the correct frame data.

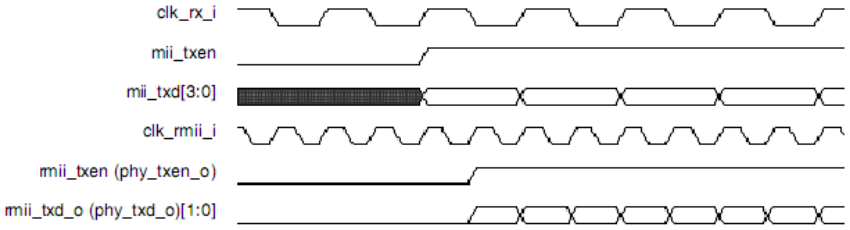

Fig. 9-5Start of MII and RMII transmission in 100-Mbps mode

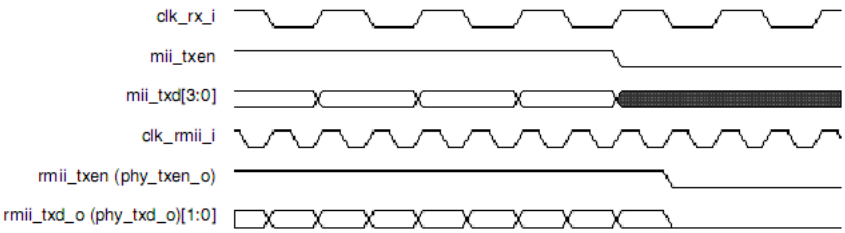

Fig. 9-6End of MII and RMII Transmission in 100-Mbps Mode

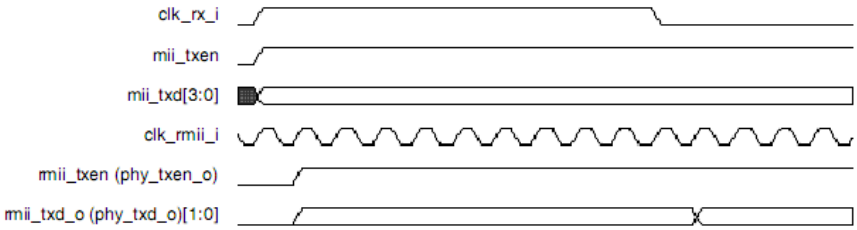

Fig. 9-7Start of MII and RMII Transmission in 10-Mbps Mode

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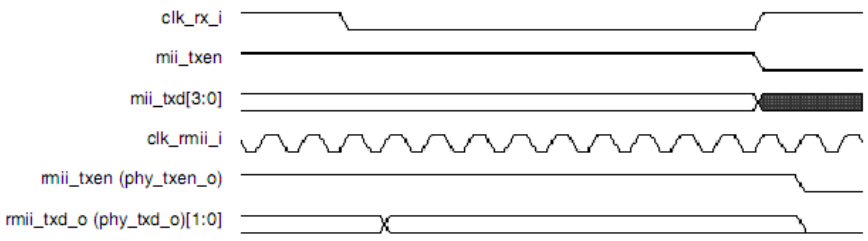

Fig. 9-8End of MII and RMII Transmission in 10-Mbps Mode

Receive Bit Ordering

Each nibble is transmitted to the MII from the di-bit received from the RMII in the nibble transmission order shown in the following figure. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

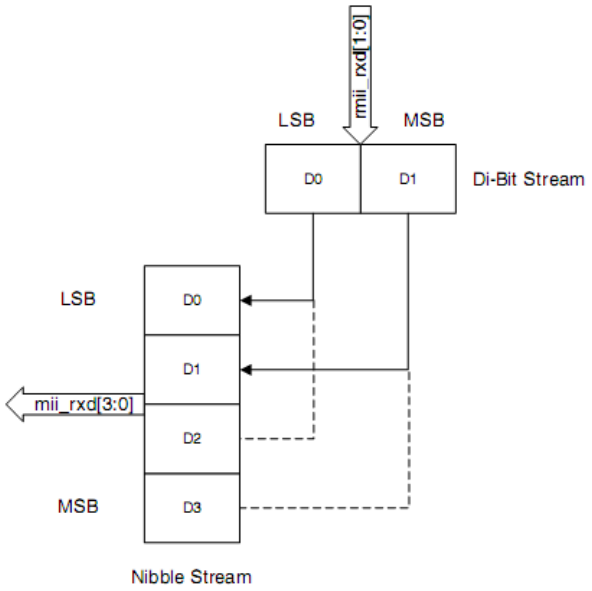

Fig. 9-9RMII receive bit ordering

9.3.3 Management Interface

The MAC100 management interface provides a simple, two-wire, serial interface to connect the MAC100 and a managed PHY, for the purposes of controlling the PHY and gathering status from the PHY. The management interface consists of a pair of signals that transport the management information across the MII bus: MDIO and MDC.

The MAC100 initiates the management write/read operation. The clock gmii_mdc_o(MDC) is a divided clock from the application clock pclk_MAC100. The divide factor depends on the clock range setting in the GMII address register. Clock range is set as follows:

Selection	pclk_MAC100	MDC Clock
0000	60-100 MHz	pclk_MAC100/42
0001	100-150 MHz	pclk_MAC100/62
0010	20-35 MHz	pclk_MAC100/16
0011	35-60 MHz	pclk_MAC100/26
0100	150-250 MHz	pclk_MAC100/102
0101	250-300 MHz	pclk_MAC100/124
0110, 0111	Reserved	

The MDC is the derivative of the application clock pclk_MAC100. The management operation is performed through the gmii_mdi_i, gmii_mdo_o and gmii_mdo_o_e signals. A three-state buffer is implemented in the PAD.

The frame structure on the MDIO line is shown below.

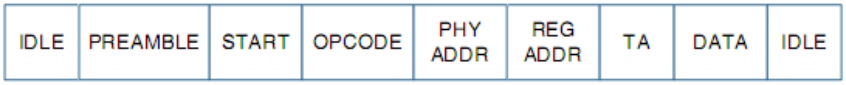

Fig. 9-10 MDIO frame structure

IDLE: The mdio line is three-state; there is no clock on gmii_mdc_o
PREAMBLE: 32 continuous bits of value 1
START: Start-of-frame is 2'b01

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OPCODE: 2'b10 for read and 2'b01 for write
PHY ADDR: 5-bit address select for one of 32 PHYs
REG ADDR: Register address in the selected PHY
TA: Turnaround is 2'bZ0 for read and 2'b10 for Write
DATA: Any 16-bit value. In a write operation, the MAC100 drives mdio; in a read operation, PHY drives it.

9.3.4 Power Management Block

Power management (PMT) supports the reception of network (remote) wake-up frames and Magic Packet frames. PMT does not perform the clock gate function, but generates interrupts for wake-up frames and Magic Packets received by the MAC100. The PMT block sits on the receiver path of the MAC100 and is enabled with remote wake-up frame enable and Magic Packet enable. These enables are in the PMT control and status register and are programmed by the application.

When the power down mode is enabled in the PMT, then all received frames are dropped by the core and they are not forwarded to the application. The core comes out of the power down mode only when either a Magic Packet or a Remote Wake-up frame is received and the corresponding detection is enabled.

Remote Wake-Up Frame Detection

When the MAC100 is in sleep mode and the remote wake-up bit is enabled in register MAC100_PMT_CTRL_STA (0x002C), normal operation is resumed after receiving a remote wake-up frame. The application writes all eight wake-up filter registers, by performing a sequential write to address (0028). The application enables remote wake-up by writing a 1 to bit 2 of the register MAC100_PMT_CTRL_STA.

PMT supports four programmable filters that allow support of different receive frame patterns. If the incoming frame passes the address filtering of Filter Command, and if Filter CRC-16 matches the incoming examined pattern, then the wake-up frame is received. Filter_offset (minimum value 12, which refers to the 13th byte of the frame) determines the offset from which the frame is to be examined. Filter Byte Mask determines which bytes of the frame must be examined. The thirty-first bit of Byte Mask must be set to zero.

The remote wake-up CRC block determines the CRC value that is compared with Filter CRC-16. The wake-up frame is checked only for length error, FCS error, dribble bit error, GMII error, collision, and to ensure that it is not a runt frame. Even if the wake-up frame is more than 512 bytes long, if the frame has a valid CRC value, it is considered valid. Wake-up frame detection is updated in the register MAC100_PMT_CTRL_STA for every remote Wake-up frame received. A PMT interrupt to the application triggers a read to the MAC100_PMT_CTRL_STA register to determine reception of a wake-up frame.

Magic Packet Detection

The Magic Packet frame is based on a method that uses Advanced Micro Device's Magic Packet technology to power up the sleeping device on the network. The MAC100 receives a specific packet of information, called a Magic Packet, addressed to the node on the network.

Only Magic Packets that are addressed to the device or a broadcast address will be checked to determine whether they meet the wake-up requirements. Magic Packets that pass the address filtering (unicast or broadcast) will be checked to determine whether they meet the remote Wake-on-LAN data format of 6 bytes of all ones followed by a MAC100 Address appearing 16 times.

The application enables Magic Packet wake-up by writing a 1 to Bit 1 of the register MAC100_PMT_CTRL_STA. The PMT block constantly monitors each frame addressed to the node for a specific Magic Packet pattern. Each frame received is checked for a 48'hFF_FF_FF_FF_FF_FF pattern following the destination and source address field. The PMT block then checks the frame for 16 repetitions of the MAC100 address without any breaks or interruptions. In case of a break in the 16 repetitions of the address, the 48'hFF_FF_FF_FF_FF_FF pattern is scanned for again in the incoming frame. The 16 repetitions can be anywhere in the frame, but must be preceded by the synchronization stream (48'hFF_FF_FF_FF_FF_FF). The device will also accept a multicast frame, as long as the 16 duplications of the MAC100 address are detected.

If the MAC100 address of a node is 48'h00_11_22_33_44_55, then the MAC100 scans for

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the data sequence:
Destination Address Source Address ……. FF FFFFFFFFF
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
…CRC
Magic Packet detection is updated in the PMT Control and Status register for Magic Packet received. A PMT interrupt to the Application triggers a read to the PMT CSR to determine whether a Magic Packet frame has been received.

9.3.5 Management Counters

The counters in the MAC100 Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted frames. These include a control register for controlling the behavior of the registers, two 32-bit registers containing interrupts generated (receive and transmit), and two 32-bit registers containing masks for the Interrupt register (receive and transmit). These registers are accessible from the Application through the MAC100 Control Interface (MCI). Non-32-bit accesses are allowed as long as the address is word-aligned.
The organization of these registers is shown in Register Description. The MMCs are accessed using transactions, in the same way the CSR address space is accessed. The Register Description in this chapter describe the various counters and list the address for each of the statistics counters. This address will be used for Read/Write accesses to the desired transmit/receive counter.
The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet frames.

9.4 Register Description

9.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
MAC100_MAC_CONF	0x0000	W	0x00000000	This is the operation mode register for the MAC
MAC100_MAC_FRM_FILT	0x0004	W	0x00000000	Contains the frame filtering controls
MAC100_HASH_TAB_HI	0x0008	W	0x00000000	Contains the higher 32 bits of the Multicast Hash table. This register is present only when the Hash filter function is selected in coreConsultant
MAC100_HASH_TAB_LO	0x000C	W	0x00000000	Contains the lower 32 bits of the Multicast Hash table. This register is present only when the Hash filter function is selected in coreConsultant
MAC100_GMII_ADDR	0x0010	W	0x00000000	Controls the management cycles to an external PHY
MAC100_GMII_DATA	0x0014	W	0x00000000	Contains the data to be written to or read from the PHY register
MAC100_FLOW_CTRL	0x0018	W	0x00000000	Controls the generation of control frames
MAC100_VLAN_TAG	0x001C	W	0x00000000	Identifies IEEE 802.1Q VLAN type frames

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Name	Offset	Size	Reset Value	Description
MAC100_DEBUG	0x0024	W	0x00000000	This debug register gives the status of all the main modules of the transmit and receive data-paths and the FIFOs. An all-zero status indicates that the MAC core is in idle state (and FIFOs are empty) and no activity is going on in the data-paths.
MAC100_PMT_CTRL_STA	0x002C	W	0x00000000	PMT Control and Status
MAC100_INT_STATUS	0x0038	W	0x00000000	Contains the interrupt status
MAC100_INT_MASK	0x003C	W	0x00000000	Contains the masks for generating the interrupts
MAC100_MAC_ADDR0_HI	0x0040	W	0x0000FFFF	Contains the higher 16 bits of the first MAC address
MAC100_MAC_ADDR0_LO	0x0044	W	0xFFFFFFFF	Contains the lower 32 bits of the first MAC address
MAC100_AN_CTRL	0x00C0	W	0x00000000	Enables and/or restarts auto-negotiation. It also enables PCS loopback
MAC100_AN_STATUS	0x00C4	W	0x00000008	Indicates the link and auto-negotiation status
MAC100_AN_ADV	0x00C8	W	0x000001E0	This register is configured before auto-negotiation begins. It contains the advertised ability of the GMAC.
MAC100_AN_LINK_PART_AB	0x00CC	W	0x00000000	Contains the advertised ability of the link partner. Its value is valid after successful completion of auto-negotiation or when a new base page has been received (indicated in the Auto-Negotiation Expansion Register)
MAC100_AN_EXP	0x00D0	W	0x00000000	Indicates whether a new base page has been received from the link partner
MAC100_INTF_MODE_STA	0x00D8	W	0x00000000	Indicates the status signals received from the PHY through the RGMII interface
MAC100_MMC_CTRL	0x0100	W	0x00000000	The MMC Control register establishes the operating mode of the management counters
MAC100_MMC_RX_INTR	0x0104	W	0x00000000	The MMC Receive Interrupt register maintains the interrupts generated when the receive statistic counters reach half their maximum values (0x8000_0000), and when they cross their maximum values (0xFFFF_FFFF). When Counter Stop Rollover is set, then interrupts are set but the counter remains at all-ones. The MMC Receive Interrupt register is a 32-bit wide register. An interrupt bit is cleared when the respective MMC counter that

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Name	Offset	Size	Reset Value	Description
				caused the interrupt is read. The least significant byte lane (bits[7:0]) of the respective counter must be read in order to clear the interrupt bit.
MAC100_MMC_TX_INTR	0x0108	W	0x00000000	The MMC Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000), and when they cross their maximum values (0xFFFF_FFFF). When Counter Stop Rollover is set, then interrupts are set but the counter remains at all-ones. The MMC Transmit Interrupt register is a 32-bit wide register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (bits[7:0]) of the respective counter must be read in order to clear the interrupt bit.
MAC100_MMC_RX_INT_MSK	0x010C	W	0x00000000	The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when receive statistic counters reach half their maximum value, and when they reach their maximum values.
MAC100_MMC_TX_INT_MSK	0x0110	W	0x00000000	The MMC Transmit Interrupt Mask register maintains the masks for the interrupts generated when transmit statistic counters reach half their maximum value, and when they reach their maximum values.
MAC100_MMC_TXOCTETCNT_GB	0x0114	W	0x00000000	
MAC100_MMC_TXFRMCNT_GB	0x0118	W	0x00000000	
MAC100_MMC_TXUNDFLWERR	0x0148	W	0x00000000	
MAC100_MMC_TXCARERR	0x0160	W	0x00000000	
MAC100_MMC_TXOCTETCNT_G	0x0164	W	0x00000000	
MAC100_MMC_TXFRMCNT_G	0x0168	W	0x00000000	
MAC100_MMC_RXFRMCNT_GB	0x0180	W	0x00000000	
MAC100_MMC_RXOCTETCNT_GB	0x0184	W	0x00000000	

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Name	Offset	Size	Reset Value	Description
MAC100_MMC_RXOCTETCNT_G	0x0188	W	0x00000000	
MAC100_MMC_RXMCFRMCNT_G	0x0190	W	0x00000000	
MAC100_MMC_RXCRCERR	0x0194	W	0x00000000	
MAC100_MMC_RXLENERR	0x01C8	W	0x00000000	
MAC100_MMC_RXFIFOOVRFLW	0x01D4	W	0x00000000	
MAC100_MMC_IPC_INT_MSK	0x0200	W	0x00000000	The MMC Receive Checksum Offload Interrupt Mask register maintains the masks for the interrupts generated when the receive IPC (Checksum Offload) statistic counters reach half their maximum value, and when they reach their maximum values.
MAC100_MMC_IPC_INTR	0x0208	W	0x00000000	The MMC Receive Checksum Offload Interrupt register maintains the interrupts generated when receive IPC statistic counters reach half their maximum values (0x8000_0000), and when they cross their maximum values (0xFFFF_FFFF). When Counter Stop Rollover is set, then interrupts are set but the counter remains at all-ones. When the MMC IPC counter that caused the interrupt is read, its corresponding interrupt bit is cleared. The counters least-significant byte lane (bits[7:0]) must be read to clear the interrupt bit.
MAC100_MMC_RXIPV4GFRM	0x0210	W	0x00000000	
MAC100_MMC_RXIPV4HDERRFRM	0x0214	W	0x00000000	
MAC100_MMC_RXIPV6GFRM	0x0224	W	0x00000000	
MAC100_MMC_RXIPV6HDERRFRM	0x0228	W	0x00000000	
MAC100_MMC_RXUDPERRFRM	0x0234	W	0x00000000	
MAC100_MMC_RXTCPERRFRM	0x023C	W	0x00000000	
MAC100_MMC_RXICMPERRFRM	0x0244	W	0x00000000	
MAC100_MMC_RXIPV4HDERROCT	0x0254	W	0x00000000	
MAC100_MMC_RXIPV6HDERROCT	0x0268	W	0x00000000	
MAC100_MMC_RXUDPERROCT	0x0274	W	0x00000000	

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Name	Offset	Size	Reset Value	Description
MAC100_MMC_RXTCPERROCT	0x027C	W	0x00000000	
MAC100_MMC_RXICMPERROCT	0x0284	W	0x00000000	
MAC100_BUS_MODE	0x1000	W	0x00020101	Controls the Host Interface Mode
MAC100_TX_POLL_DEMAND	0x1004	W	0x00000000	Used by the host to instruct the DMA to poll the Transmit Descriptor List
MAC100_RX_POLL_DEMAND	0x1008	W	0x00000000	Used by the Host to instruct the DMA to poll the Receive Descriptor list
MAC100_RX_DESC_LIST_ADDR	0x100C	W	0x00000000	Points the DMA to the start of the Receive Descriptor list
MAC100_TX_DESC_LIST_ADDR	0x1010	W	0x00000000	Points the DMA to the start of the Transmit Descriptor List
MAC100_STATUS	0x1014	W	0x00000000	The Software driver (application) reads this register during interrupt service routine or polling to determine the status of the DMA
MAC100_OP_MODE	0x1018	W	0x00000000	Establishes the Receive and Transmit operating modes and command
MAC100_INT_ENA	0x101C	W	0x00000000	Enables the interrupts reported by the Status Register
MAC100_OVERFLOW_CNT	0x1020	W	0x00000000	Contains the counters for discarded frames because no host Receive Descriptor was available, and discarded frames because of Receive FIFO Overflow
MAC100_REC_INT_WDT_TIMER	0x1024	W	0x00000000	Watchdog time-out for Receive Interrupt (RI) from DMA
MAC100_AXI_BUS_MODE	0x1028	W	0x00110001	Controls AXI Master behavior (mainly controls burst splitting and number of outstanding requests)
MAC100_AXI_STATUS	0x102C	W	0x00000000	Gives the idle status of the AXI master's read/write channels
MAC100_CUR_HOST_TX_DESC	0x1048	W	0x00000000	Points to the start of current Transmit Descriptor read by the DMA
MAC100_CUR_HOST_RX_DESC	0x104C	W	0x00000000	Points to the start of current Receive Descriptor read by the DMA
MAC100_CUR_HOST_TX_BUF_ADDR	0x1050	W	0x00000000	Points to the current Transmit Buffer address read by the DMA
MAC100_CUR_HOST_RX_BUF_ADDR	0x1054	W	0x00000000	Points to the current Receive Buffer address read by the DMA

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.2 Detail Registers Description

MAC100_MAC_CONF

Address: Operational Base(0xFFB30000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	TC When set, this bit enables the transmission of duplex mode, link speed, and link up/down information to the PHY in the RGMII ports. When this bit is reset, no such information is driven to the PHY.
23	RW	0x0	WD When this bit is set, the GMAC disables the watchdog timer on the receiver, and can receive frames of up to 16,384 bytes. When this bit is reset, the GMAC allows no more than 2,048 bytes (10,240 if JE is set high) of the frame being received and cuts off any bytes received after that.
22	RW	0x0	JD When this bit is set, the GMAC disables the jabber timer on the transmitter, and can transfer frames of up to 16,384 bytes. When this bit is reset, the GMAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission.
21	RW	0x0	BE When this bit is set, the GMAC allows frame bursting during transmission in GMII Half-Duplex mode.
20	RO	0x0	reserved
19:17	RW	0x0	IFG These bits control the minimum IFG between frames during transmission. 3'b000: 96 bit times 3'b001: 88 bit times 3'b010: 80 bit times ... 3'b111: 40 bit times
16	RW	0x0	DCRS When set high, this bit makes the MAC transmitter ignore the (G)MII CRS signal during frame transmission in Half-Duplex mode. This request results in no errors generated due to Loss of Carrier or No Carrier during such transmission. When this bit is low, the MAC transmitter generates such errors due to Carrier Sense and will even abort the transmissions.
15	RW	0x0	PS Selects between GMII and MII: 1'b0: GMII (1000 Mbps) 1'b1: MII (10/100 Mbps)
14	RW	0x0	FES Indicates the speed in Fast Ethernet (MII) mode: 1'b0: 10 Mbps 1'b1: 100 Mbps
13	RW	0x0	DO When this bit is set, the GMAC disables the reception of frames when the gmii_txen_o is asserted in Half-Duplex mode. When this bit is reset, the GMAC receives all packets that are given by the PHY while transmitting.
12	RW	0x0	LM When this bit is set, the GMAC operates in loopback mode at GMII/MII. The (G)MII Receive clock input (clk_rx_i) is required for the loopback to work properly, as the Transmit clock is not looped-back internally.

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Bit	Attr	Reset Value	Description
11	RW	0x0	DM When this bit is set, the GMAC operates in a Full-Duplex mode where it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in Full-Duplex-only configuration.
10	RW	0x0	IPC When this bit is set, the GMAC calculates the 16-bit one's complement of the one's complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25-26 or 29-30 (VLAN-tagged) of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The GMAC core also appends the 16-bit checksum calculated for the IP header datagram payload (bytes after the IPv4 header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected). When this bit is reset, this function is disabled. When Type 2 COE is selected, this bit, when set, enables IPv4 checksum checking for received frame payloads TCP/UDP/ICMP headers. When this bit is reset, the COE function in the receiver is disabled and the corresponding PCE and IP HCE status bits are always cleared.
9	RW	0x0	DR When this bit is set, the GMAC will attempt only 1 transmission. When a collision occurs on the GMII/MII, the GMAC will ignore the current frame transmission and report a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the GMAC will attempt retries based on the settings of BL.
8	RW	0x0	LUD Indicates whether the link is up or down during the transmission of configuration in RGMII interface: 1'b0: Link Down 1'b1: Link Up
7	RW	0x0	ACS When this bit is set, the GMAC strips the Pad/FCS field on incoming frames only if the length's field value is less than or equal to 1,500 bytes. All received frames with length field greater than or equal to 1,501 bytes are passed to the application without stripping the Pad/FCS field. When this bit is reset, the GMAC will pass all incoming frames to the Host unmodified.
6:5	RW	0x0	BL The Back-Off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) the GMAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only to Half-Duplex mode and is reserved (RO) in Full-Duplex-only configuration. 2'b00: k = min (n, 10) 2'b01: k = min (n, 8) 2'b10: k = min (n, 4) 2'b11: k = min (n, 1), Where n = retransmission attempt. The random integer r takes the value in the range 0 = r < 2^k

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Bit	Attr	Reset Value	Description
4	RW	0x0	DC When this bit is set, the deferral check function is enabled in the GMAC. The GMAC will issue a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status when the transmit state machine is deferred for more than 24,288 bit times in 10/100-Mbps mode. If the Core is configured for 1000 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but is prevented because of an active CRS (carrier sense) signal on the GMII/MII. Defer time is not cumulative. If the transmitter defers for 10,000 bit times, then transmits, collides, backs off, and then has to defer again after completion of back-off, the deferral timer resets to 0 and restarts. When this bit is reset, the deferral check function is disabled and the GMAC defers until the CRS signal goes inactive.
3	RW	0x0	TE When this bit is set, the transmit state machine of the GMAC is enabled for transmission on the GMII/MII. When this bit is reset, the GMAC transmit state machine is disabled after the completion of the transmission of the current frame, and will not transmit any further frames.
2	RW	0x0	RE When this bit is set, the receiver state machine of the GMAC is enabled for receiving frames from the GMII/MII. When this bit is reset, the GMAC receive state machine is disabled after the completion of the reception of the current frame, and will not receive any further frames from the GMII/MII.
1:0	RO	0x0	reserved

MAC100_MAC_FRM_FILT

Address: Operational Base(0xFFB30000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	RA When this bit is set, the GMAC Receiver module passes to the Application all frames received irrespective of whether they pass the address filter. The result of the SA/DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes to the Application only those frames that pass the SA/DA address filter.
30:11	RO	0x00000	reserved
10	RW	0x0	HPF When set, this bit configures the address filter to pass a frame if it matches either the perfect filtering or the hash filtering as set by HMC or HUC bits. When low and if the HUC/HMC bit is set, the frame is passed only if it matches the Hash filter.
9	RW	0x0	SAF The GMAC core compares the SA field of the received frames with the values programmed in the enabled SA registers. If the comparison matches, then the SAMatch bit of RxStatus Word is set high. When this bit is set high and the SA filter fails, the GMAC drops the frame. When this bit is reset, then the GMAC Core forwards the received frame to the application and with the updated SA Match bit of the RxStatus depending on the SA address comparison.

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Bit	Attr	Reset Value	Description
8	RW	0x0	SAIF When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers will be marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers will be marked as failing the SA Address filter.
7:6	RW	0x0	PCF These bits control the forwarding of all control frames (including unicast and multicast PAUSE frames). Note that the processing of PAUSE control frames depends only on RFE of Register GMAC_FLOW_CTRL[2]. 2'b00: GMAC filters all control frames from reaching the application. 2'b01: GMAC forwards all control frames except PAUSE control frames to application even if they fail the Address filter. 2'b10: GMAC forwards all control frames to application even if they fail the Address Filter. 2'b11: GMAC forwards control frames that pass the Address Filter.
5	RW	0x0	DBF When this bit is set, the AFM module filters all incoming broadcast frames. When this bit is reset, the AFM module passes all received broadcast frames.
4	RW	0x0	PM When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address field is '1') are passed. When reset, filtering of multicast frame depends on HMC bit.
3	RW	0x0	DAIF When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed.
2	RW	0x0	HMC When set, MAC performs destination address filtering of received multicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for multicast frames, that is, it compares the DA field with the values programmed in DA registers.
1	RW	0x0	HUC When set, MAC performs destination address filtering of unicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for unicast frames, that is, it compares the DA field with the values programmed in DA registers.
0	RW	0x0	PR When this bit is set, the Address Filter module passes all incoming frames regardless of its destination or source address. The SA/DA Filter Fails status bits of the Receive Status Word will always be cleared when PR is set.

MAC100_HASH_TAB_HI

Address: Operational Base(0xFFB30000) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HTH This field contains the upper 32 bits of Hash table

MAC100_HASH_TAB_LO

Address: Operational Base(0xFFB30000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HTL This field contains the lower 32 bits of Hash table

MAC100_GMII_ADDR

Address: Operational Base(0xFFB30000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x00	PA This field tells which of the 32 possible PHY devices are being accessed
10:6	RW	0x00	GR These bits select the desired GMII register in the selected PHY device
5:2	RW	0x0	CR The APB Clock Range selection determines the frequency of the MDC clock as per the pclk_gmac frequency used in your design. The suggested range of pclk_gmac frequency applicable for each value below (when Bit[5] = 0) ensures that the MDC clock is approximately between the frequency range 1.0 MHz - 2.5 MHz. Selection pclk_gmac MDC Clock 0000 60-100 MHz pclk_gmac/42 0001 100-150 MHz pclk_gmac/62 0010 20-35 MHz pclk_gmac/16 0011 35-60 MHz pclk_gmac/26 0100 150-250 MHz pclk_gmac/102 0101 250-300 MHz pclk_gmac/124 0110, 0111 Reserved When bit 5 is set, you can achieve MDC clock of frequency higher than the IEEE 802.3 specified frequency limit of 2.5 MHz and program a clock divider of lower value. For example, when pclk_gmac is of frequency 100 MHz and you program these bits as "1010", then the resultant MDC clock will be of 12.5 MHz which is outside the limit of IEEE 802.3 specified range. Please program the values given below only if the interfacing chips supports faster MDC clocks. Selection MDC Clock 1000 pclk_gmac/4 1001 pclk_gmac/6 1010 pclk_gmac/8 1011 pclk_gmac/10 1100 pclk_gmac/12 1101 pclk_gmac/14 1110 pclk_gmac/16 1111 pclk_gmac/18
1	RW	0x0	GW When set, this bit tells the PHY that this will be a Write operation using register GMAC_GMII_DATA. If this bit is not set, this will be a Read operation, placing the data in register GMAC_GMII_DATA.

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Bit	Attr	Reset Value	Description
0	W1C	0x0	GB This bit should read a logic 0 before writing to Register GMII_ADDR and Register GMII_DATA. This bit must also be set to 0 during a Write to Register GMII_ADDR. During a PHY register access, this bit will be set to 1'b1 by the Application to indicate that a Read or Write access is in progress. Register GMII_DATA (GMII Data) should be kept valid until this bit is cleared by the GMAC during a PHY Write operation. The Register GMII_DATA is invalid until this bit is cleared by the GMAC during a PHY Read operation. The Register GMII_ADDR (GMII Address) should not be written to until this bit is cleared.

MAC100_GMII_DATA

Address: Operational Base(0xFFB30000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	GD This contains the 16-bit data value read from the PHY after a Management Read operation or the 16-bit data value to be written to the PHY before a Management Write operation.

MAC100_FLOW_CTRL

Address: Operational Base(0xFFB30000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PT This field holds the value to be used in the Pause Time field in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least 4 clock cycles in the destination clock domain.
15:8	RO	0x00	reserved
7	RW	0x0	DZPQ When set, this bit disables the automatic generation of Zero-Quanta Pause Control frames on the de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i/mti_flowctrl_i). When this bit is reset, normal operation with automatic Zero-Quanta Pause Control frame generation is enabled.
6	RO	0x0	reserved
5:4	RW	0x0	PLT This field configures the threshold of the PAUSE timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of PAUSE Frame. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot-times), and PLT = 01, then a second PAUSE frame is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot-times after the first PAUSE frame is transmitted. Selection Threshold 00 Pause time minus 4 slot times 01 Pause time minus 28 slot times 10 Pause time minus 144 slot times 11 Pause time minus 256 slot times Slot time is defined as time taken to transmit 512 bits (64 bytes) on the GMII/MII interface.

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Bit	Attr	Reset Value	Description
3	RW	0x0	UP When this bit is set, the GMAC will detect the Pause frames with the station's unicast address specified in MAC Address0 High Register and MAC Address0 Low Register, in addition to the detecting Pause frames with the unique multicast address. When this bit is reset, the GMAC will detect only a Pause frame with the unique multicast address specified in the 802.3x standard.
2	RW	0x0	RFE When this bit is set, the GMAC will decode the received Pause frame and disable its transmitter for a specified (Pause Time) time. When this bit is reset, the decode function of the Pause frame is disabled.
1	RW	0x0	TFE In Full-Duplex mode, when this bit is set, the GMAC enables the flow control operation to transmit Pause frames. When this bit is reset, the flow control operation in the GMAC is disabled, and the GMAC will not transmit any Pause frames. In Half-Duplex mode, when this bit is set, the GMAC enables the back-pressure operation. When this bit is reset, the backpressure feature is disabled.
0	RW	0x0	FCB_BPA This bit initiates a Pause Control frame in Full-Duplex mode and activates the backpressure function in Half-Duplex mode if TFE bit is set. In Full-Duplex mode, this bit should be read as 1'b0 before writing to the register GMAC_FLOW_CTRL. To initiate a pause control frame, the application must set this bit to 1'b1. During a transfer of the control frame, this bit will continue to be set to signify that a frame transmission is in progress. After the completion of Pause control frame transmission, the GMAC will reset this bit to 1'b0. The register GMAC_FLOW_CTRL should not be written to until this bit is cleared. In Half-Duplex mode, when this bit is set (and TFE is set), then backpressure is asserted by the GMAC Core. During backpressure, when the GMAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically OR'ed with the mti_flowctrl_i input signal for the backpressure function.

MAC100_VLAN_TAG

Address: Operational Base(0xFFB30000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	ETV When this bit is set, a 12-bit VLAN identifier, rather than the complete 16-bit VLAN tag, is used for comparison and filtering. Bits[11:0] of the VLAN tag are compared with the corresponding field in the received VLAN-tagged frame. When this bit is reset, all 16 bits of the received VLAN frame's fifteenth and sixteenth bytes are used for comparison.
15:0	RW	0x0000	VL This contains the 802.1Q VLAN tag to identify VLAN frames, and is compared to the fifteenth and sixteenth bytes of the frames being received for VLAN frames. Bits[15:13] are the User Priority, Bit[12] is the Canonical Format Indicator (CFI) and bits[11:0] are the VLAN tag's VLAN Identifier (VID) field. When the ETV bit is

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Bit	Attr	Reset Value	Description
			set, only the VID (Bits[11:0]) is used for comparison. If VL (VL[11:0] if ETV is set) is all zeros, the GMAC does not check the fifteenth and sixteenth bytes for VLAN tag comparison, and declares all frames with a Type field value of 0x8100 to be VLAN frames.

MAC100_DEBUG

Address: Operational Base(0xFFB30000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	TFIFO3 When high, it indicates that the MTL TxStatus FIFO is full and hence the MTL will not be accepting any more frames for transmission.
24	RW	0x0	TFIFO2 When high, it indicates that the MTL TxFIFO is not empty and has some data left for transmission.
23	RO	0x0	reserved
22	RW	0x0	TFIFO1 When high, it indicates that the MTL TxFIFO Write Controller is active and transferring data to the TxFIFO.
21:20	RW	0x0	TFIFOSTA This indicates the state of the TxFIFO read Controller: 2'b00: IDLE state 2'b01: READ state (transferring data to MAC transmitter) 2'b10: Waiting for TxStatus from MAC transmitter 2'b11: Writing the received TxStatus or flushing the TxFIFO
19	RW	0x0	PAUSE When high, it indicates that the MAC transmitter is in PAUSE condition (in full-duplex only) and hence will not schedule any frame for transmission
18:17	RW	0x0	TSAT This indicates the state of the MAC Transmit Frame Controller module: 2'b00: IDLE 2'b01: Waiting for Status of previous frame or IFG/backoff period to be over 2'b10: Generating and transmitting a PAUSE control frame (in full duplex mode) 2'b11: Transferring input frame for transmission
16	RW	0x0	TACT When high, it indicates that the MAC GMII/MII transmit protocol engine is actively transmitting data and not in IDLE state.
15:10	RO	0x00	reserved
9:8	RW	0x0	RFIFO This gives the status of the RxFIFO Fill-level: 2'b00: RxFIFO Empty 2'b01: RxFIFO fill-level below flow-control de-activate threshold 2'b10: RxFIFO fill-level above flow-control activate threshold 2'b11: RxFIFO Full
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	RFIFORD It gives the state of the RxFIFO read Controller: 2'b00: IDLE state 2'b01: Reading frame data 2'b10: Reading frame status (or time-stamp) 2'b11: Flushing the frame data and Status
4	RW	0x0	RFIFOWR When high, it indicates that the MTL RxFIFO Write Controller is active and transferring a received frame to the FIFO.
3	RO	0x0	reserved
2:1	RW	0x0	ACT When high, it indicates the active state of the small FIFO Read and Write controllers respectively of the MAC receive Frame Controller module
0	RW	0x0	RDB When high, it indicates that the MAC GMII/MII receive protocol engine is actively receiving data and not in IDLE state.

MAC100_PMT_CTRL_STA

Address: Operational Base(0xFFB30000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	W1C	0x0	WFFRPR When set, resets the Remote Wake-up Frame Filter register pointer to 3'b000. It is automatically cleared after 1 clock cycle.
30:10	RO	0x000000	reserved
9	RW	0x0	GU When set, enables any unicast packet filtered by the GMAC (DAF) address recognition to be a wake-up frame.
8:7	RO	0x0	reserved
6	RC	0x0	WFR When set, this bit indicates the power management event was generated due to reception of a wake-up frame. This bit is cleared by a read into this register.
5	RC	0x0	MPR When set, this bit indicates the power management event was generated by the reception of a Magic Packet. This bit is cleared by a read into this register.
4:3	RO	0x0	reserved
2	RW	0x0	WFE When set, enables generation of a power management event due to wake-up frame reception.
1	RW	0x0	MPE When set, enables generation of a power management event due to Magic Packet reception.
0	R/WSC	0x0	PD When set, all received frames will be dropped. This bit is cleared automatically when a magic packet or Wake-Up frame is received, and Power-Down mode is disabled. Frames received after this bit is cleared are forwarded to the application. This bit must only be set when either the Magic Packet Enable or Wake-Up Frame Enable bit is set high.

MAC100_INT_STATUS

Address: Operational Base(0xFFB30000) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	MRCOIS This bit is set high whenever an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.
6	RO	0x0	MTIS This bit is set high whenever an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is only valid when the optional MMC module is selected during configuration.
5	RO	0x0	MRIS This bit is set high whenever an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is only valid when the optional MMC module is selected during configuration.
4	RO	0x0	MIS This bit is set high whenever any of bits 7:5 is set high and cleared only when all of these bits are low. This bit is valid only when the optional MMC module is selected during configuration.
3	RO	0x0	PIS This bit is set whenever a Magic packet or Wake-on-LAN frame is received in Power-Down mode). This bit is cleared when both bits[6:5] are cleared due to a read operation to the register GMAC_PMT_CTRL_STA.
2:1	RO	0x0	reserved
0	RO	0x0	RIS This bit is set due to any change in value of the Link Status of RGMII interface. This bit is cleared when the user makes a read operation the RGMII Status register.

MAC100_INT_MASK

Address: Operational Base(0xFFB30000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	PIM This bit when set, will disable the assertion of the interrupt signal due to the setting of PMT Interrupt Status bit in Register GMAC_INT_STATUS.
2:1	RO	0x0	reserved
0	RW	0x0	RIM This bit when set, will disable the assertion of the interrupt signal due to the setting of RGMII Interrupt Status bit in Register GMAC_INT_STATUS.

MAC100_MAC_ADDR0_HI

Address: Operational Base(0xFFB30000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	A47_A32 This field contains the upper 16 bits (47:32) of the 6-byte first MAC address. This is used by the MAC for filtering for received frames and for inserting the MAC address in the Transmit Flow Control (PAUSE) Frames.

MAC100_MAC_ADDR0_LO

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Address: Operational Base(0xFFB30000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	A31_A0 This field contains the lower 32 bits of the 6-byte first MAC address. This is used by the MAC for filtering for received frames and for inserting the MAC address in the Transmit Flow Control (PAUSE) Frames.

MAC100_AN_CTRL

Address: Operational Base(0xFFB30000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ANE When set, will enable the GMAC to perform auto-negotiation with the link partner. Clearing this bit will disable auto-negotiation.
11:10	RO	0x0	reserved
9	R/W SC	0x0	RAN When set, will cause auto-negotiation to restart if the ANE is set. This bit is self-clearing after auto-negotiation starts. This bit should be cleared for normal operation.
8:0	RO	0x000	reserved

MAC100_AN_STATUS

Address: Operational Base(0xFFB30000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ANC When set, this bit indicates that the auto-negotiation process is completed. This bit is cleared when auto-negotiation is reinitiated.
4	RO	0x0	reserved
3	RO	0x1	ANA This bit is always high, because the GMAC supports auto-negotiation.
2	R/W SC	0x0	LS When set, this bit indicates that the link is up. When cleared, this bit indicates that the link is down.
1:0	RO	0x0	reserved

MAC100_AN_ADV

Address: Operational Base(0xFFB30000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	NP This bit is tied to low, because the GMAC does not support the next page.
14	RO	0x0	reserved
13:12	RW	0x0	RFE These 2 bits provide a remote fault encoding, indicating to a link partner that a fault or error condition has occurred.
11:9	RO	0x0	reserved
8:7	RW	0x3	PSE These 2 bits provide an encoding for the PAUSE bits, indicating that the GMAC is capable of configuring the PAUSE function as defined in IEEE 802.3x.

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Bit	Attr	Reset Value	Description
6	RW	0x1	HD This bit, when set high, indicates that the GMAC supports Half-Duplex. This bit is tied to low (and RO) when the GMAC is configured for Full-Duplex-only operation.
5	RW	0x1	FD This bit, when set high, indicates that the GMAC supports Full-Duplex.
4:0	RO	0x00	reserved

MAC100_AN_LINK_PART_AB

Address: Operational Base(0xFFB30000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	NP When set, this bit indicates that more next page information is available. When cleared, this bit indicates that next page exchange is not desired.
14	RO	0x0	ACK When set, this bit is used by the auto-negotiation function to indicate that the link partner has successfully received the GMAC's base page. When cleared, it indicates that a successful receipt of the base page has not been achieved.
13:12	RO	0x0	RFE These 2 bits provide a remote fault encoding, indicating a fault or error condition of the link partner.
11:9	RO	0x0	reserved
8:7	RO	0x0	PSE These 2 bits provide an encoding for the PAUSE bits, indicating that the link partner's capability of configuring the PAUSE function as defined in IEEE 802.3x.
6	RO	0x0	HD When set, this bit indicates that the link partner has the ability to operate in Half-Duplex mode. When cleared, the link partner does not have the ability to operate in Half-Duplex mode.
5	RO	0x0	FD When set, this bit indicates that the link partner has the ability to operate in Full-Duplex mode. When cleared, the link partner does not have the ability to operate in Full-Duplex mode.
4:0	RO	0x00	reserved

MAC100_AN_EXP

Address: Operational Base(0xFFB30000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	NPA This bit is tied to low, because the GMAC does not support next page function.
1	RO	0x0	NPR When set, this bit indicates that a new page has been received by the GMAC. This bit will be cleared when read.
0	RO	0x0	reserved

MAC100_INTF_MODE_STA

Address: Operational Base(0xFFB30000) + offset (0x00D8)

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Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	LST Indicates whether the link is up (1'b1) or down (1'b0)
2:1	RO	0x0	LSD Indicates the current speed of the link: 2'b00: 2.5 MHz 2'b01: 25 MHz 2'b10: 125 MHz
0	RW	0x0	LM Indicates the current mode of operation of the link: 1'b0: Half-Duplex mode 1'b1: Full-Duplex mode

MAC100_MMC_CTRL

Address: Operational Base(0xFFB30000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	FHP When low and bit4 is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (half - 2K Bytes) and all frame-counters gets preset to 0x7FFF_FFF0 (half - 16) When high and bit4 is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (full - 2K Bytes) and all frame-counters gets preset to 0xFFFF_FFF0 (full - 16)
4	R/W SC	0x0	CP When set, all counters will be initialized or preset to almost full or almost half as per Bit5 above. This bit will be cleared automatically after 1 clock cycle. This bit along with bit5 is useful for debugging and testing the assertion of interrupts due to MMC counter becoming half-full or full.
3	RW	0x0	MCF When set, this bit freezes all the MMC counters to their current value. (None of the MMC counters are updated due to any transmitted or received frame until this bit is reset to 0. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode.)
2	RW	0x0	ROR When set, the MMC counters will be reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (bits[7:0]) is read.
1	RW	0x0	CSR When set, counter after reaching maximum value will not roll over to zero
0	R/W SC	0x0	CR When set, all counters will be reset. This bit will be cleared automatically after 1 clock cycle

MAC100_MMC_RX_INTR

Address: Operational Base(0xFFB30000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	INT21 The bit is set when the rxfifooverflow counter reaches half the maximum value, and also when it reaches the maximum value.
20:19	RO	0x0	reserved
18	RC	0x0	INT18 The bit is set when the rxlengtherror counter reaches half the maximum value, and also when it reaches the maximum value.
17:6	RO	0x000	reserved
5	RW	0x0	INT5 The bit is set when the rxcrcerror counter reaches half the maximum value, and also when it reaches the maximum value.
4	RC	0x0	INT4 The bit is set when the rxmulticastframes_g counter reaches half the maximum value, and also when it reaches the maximum value.
3	RO	0x0	reserved
2	RC	0x0	INT2 The bit is set when the rxoctetcount_g counter reaches half the maximum value, and also when it reaches the maximum value.
1	RC	0x0	INT1 The bit is set when the rxoctetcount_gb counter reaches half the maximum value, and also when it reaches the maximum value.
0	RC	0x0	INT0 The bit is set when the rxframecount_gb counter reaches half the maximum value, and also when it reaches the maximum value.

MAC100_MMC_TX_INTR

Address: Operational Base(0xFFB30000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RC	0x0	INT21 The bit is set when the txframecount_g counter reaches half the maximum value, and also when it reaches the maximum value.
20	RC	0x0	INT20 The bit is set when the txoctetcount_g counter reaches half the maximum value, and also when it reaches the maximum value.
19	RC	0x0	INT19 The bit is set when the txcarriererror counter reaches half the maximum value, and also when it reaches the maximum value.
18:14	RO	0x00	reserved
13	RC	0x0	INT13 The bit is set when the txunderflowerror counter reaches half the maximum value, and also when it reaches the maximum value.
12:2	RO	0x000	reserved
1	RC	0x0	INT1 The bit is set when the txframecount_gb counter reaches half the maximum value, and also when it reaches the maximum value.
0	RC	0x0	INT0 The bit is set when the txoctetcount_gb counter reaches half the maximum value, and also when it reaches the maximum value.

MAC100_MMC_RX_INT_MSK

Address: Operational Base(0xFFB30000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	INT21 Setting this bit masks the interrupt when the rxfifooverflow counter reaches half the maximum value, and also when it reaches the maximum value.
20:19	RO	0x0	reserved
18	RW	0x0	INT18 Setting this bit masks the interrupt when the rxlengtherror counter reaches half the maximum value, and also when it reaches the maximum value.
17:6	RO	0x000	reserved
5	RW	0x0	INT5 Setting this bit masks the interrupt when the rxcrcerror counter reaches half the maximum value, and also when it reaches the maximum value.
4	RW	0x0	INT4 Setting this bit masks the interrupt when the rxmulticastframes_g counter reaches half the maximum value, and also when it reaches the maximum value.
3	RO	0x0	reserved
2	RW	0x0	INT2 Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half the maximum value, and also when it reaches the maximum value.
1	RW	0x0	INT1 Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half the maximum value, and also when it reaches the maximum value.
0	RW	0x0	INT0 Setting this bit masks the interrupt when the rxframecount_gb counter reaches half the maximum value, and also when it reaches the maximum value.

MAC100_MMC_TX_INT_MSK

Address: Operational Base(0xFFB30000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	INT21 Setting this bit masks the interrupt when the txframecount_g counter reaches half the maximum value, and also when it reaches the maximum value.
20	RW	0x0	INT20 Setting this bit masks the interrupt when the txoctetcount_g counter reaches half the maximum value, and also when it reaches the maximum value.
19	RW	0x0	INT19 Setting this bit masks the interrupt when the txcarriererror counter reaches half the maximum value, and also when it reaches the maximum value.
18:14	RO	0x00	reserved
13	RW	0x0	INT13 Setting this bit masks the interrupt when the txunderflowerror counter reaches half the maximum value, and also when it reaches the maximum value.
12:2	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	INT1 Setting this bit masks the interrupt when the txframecount_gb counter reaches half the maximum value, and also when it reaches the maximum value.
0	RW	0x0	INT0 Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half the maximum value, and also when it reaches the maximum value.

MAC100_MMC_TXOCTETCNT_GB

Address: Operational Base(0xFFB30000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txoctetcount_gb Number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad frames.

MAC100_MMC_TXFRMCNT_GB

Address: Operational Base(0xFFB30000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txframecount_gb Number of good and bad frames transmitted, exclusive of retried frames.

MAC100_MMC_TXUNDFLWERR

Address: Operational Base(0xFFB30000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txunderflowerror Number of frames aborted due to frame underflow error.

MAC100_MMC_TXCARERR

Address: Operational Base(0xFFB30000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txcarriererror Number of frames aborted due to carrier sense error (no carrier or loss of carrier).

MAC100_MMC_TXOCTETCNT_G

Address: Operational Base(0xFFB30000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txoctetcount_g Number of bytes transmitted, exclusive of preamble, in good frames only.

MAC100_MMC_TXFRMCNT_G

Address: Operational Base(0xFFB30000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txframecount_g Number of good frames transmitted.

MAC100_MMC_RXFRMCNT_GB

Address: Operational Base(0xFFB30000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxframecount_gb Number of good and bad frames received.

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MAC100_MMC_RXOCTETCNT_GB

Address: Operational Base(0xFFB30000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxoctetcount_gb Number of bytes received, exclusive of preamble, in good and bad frames.

MAC100_MMC_RXOCTETCNT_G

Address: Operational Base(0xFFB30000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxoctetcount_g Number of bytes received, exclusive of preamble, only in good frames.

MAC100_MMC_RXMCFRMCNT_G

Address: Operational Base(0xFFB30000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxmulticastframes_g Number of good multicast frames received.

MAC100_MMC_RXCRCERR

Address: Operational Base(0xFFB30000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxcrcerror Number of frames received with CRC error.

MAC100_MMC_RXLENERR

Address: Operational Base(0xFFB30000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxlengtherror Number of frames received with length error (Length type field frame size), for all frames with valid length field.

MAC100_MMC_RXFIFOOVRFLW

Address: Operational Base(0xFFB30000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxfifooverflow Number of missed received frames due to FIFO overflow.

MAC100_MMC_IPC_INT_MSK

Address: Operational Base(0xFFB30000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	INT29 Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
28	RO	0x0	reserved
27	RW	0x0	INT27 Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
26	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
25	RW	0x0	INT25 Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
24:23	RO	0x0	reserved
22	RW	0x0	INT22 Setting this bit masks the interrupt when the rxipv6_hdrerr_octets counter reaches half the maximum value, and also when it reaches the maximum value.
21:18	RO	0x0	reserved
17	RW	0x0	INT17 Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half the maximum value, and also when it reaches the maximum value.
16:14	RO	0x0	reserved
13	RW	0x0	INT13 Setting this bit masks the interrupt when the rxicmp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
12	RO	0x0	reserved
11	RW	0x0	INT11 Setting this bit masks the interrupt when the rxtcp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
10	RO	0x0	reserved
9	RW	0x0	INT9 Setting this bit masks the interrupt when the rxudp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
8:7	RO	0x0	reserved
6	RW	0x0	INT6 Setting this bit masks the interrupt when the rxipv6_hdrerr_frms counter reaches half the maximum value, and also when it reaches the maximum value.
5	RW	0x0	INT5 Setting this bit masks the interrupt when the rxipv6_gd_frms counter reaches half the maximum value, and also when it reaches the maximum value.
4:2	RO	0x0	reserved
1	RW	0x0	INT1 Setting this bit masks the interrupt when the rxipv4_hdrerr_frms counter reaches half the maximum value, and also when it reaches the maximum value.
0	RW	0x0	INT0 Setting this bit masks the interrupt when the rxipv4_gd_frms counter reaches half the maximum value, and also when it reaches the maximum value.

MAC100_MMC_IPC_INTR

Address: Operational Base(0xFFB30000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RC	0x0	INT29 The bit is set when the rxicmp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
28	RO	0x0	reserved
27	RC	0x0	INT27 The bit is set when the rxtcp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
26	RO	0x0	reserved
25	RC	0x0	INT25 The bit is set when the rxudp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
24:23	RO	0x0	reserved
22	RC	0x0	INT22 The bit is set when the rxipv6_hdrerr_octets counter reaches half the maximum value, and also when it reaches the maximum value.
21:18	RO	0x0	reserved
17	RC	0x0	INT17 The bit is set when the rxipv4_hdrerr_octets counter reaches half the maximum value, and also when it reaches the maximum value.
16:14	RO	0x0	reserved
13	RC	0x0	INT13 The bit is set when the rxicmp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
12	RO	0x0	reserved
11	RC	0x0	INT11 The bit is set when the rxtcp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
10	RO	0x0	reserved
9	RC	0x0	INT9 The bit is set when the rxudp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
8:7	RO	0x0	reserved
6	RC	0x0	INT6 The bit is set when the rxipv6_hdrerr_frms counter reaches half the maximum value, and also when it reaches the maximum value.
5	RC	0x0	INT5 The bit is set when the rxipv6_gd_frms counter reaches half the maximum value, and also when it reaches the maximum value.
4:2	RO	0x0	reserved
1	RC	0x0	INT1 The bit is set when the rxipv4_hdrerr_frms counter reaches half the maximum value, and also when it reaches the maximum value.
0	RC	0x0	INT0 The bit is set when the rxipv4_gd_frms counter reaches half the maximum value, and also when it reaches the maximum value.

MAC100_MMC_RXIPV4GFRM

Address: Operational Base(0xFFB30000) + offset (0x0210)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv4_gd_frms Number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload

MAC100_MMC_RXIPV4HDERRFRM

Address: Operational Base(0xFFB30000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv4_hdrerr_frms Number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors

MAC100_MMC_RXIPV6GFRM

Address: Operational Base(0xFFB30000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv6_gd_frms Number of good IPv6 datagrams received with TCP, UDP, or ICMP payloads.

MAC100_MMC_RXIPV6HDERRFRM

Address: Operational Base(0xFFB30000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv6_hdrerr_frms Number of IPv6 datagrams received with header errors (length or version mismatch).

MAC100_MMC_RXUDPERRFRM

Address: Operational Base(0xFFB30000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxudp_err_frms Number of good IP datagrams whose UDP payload has a checksum error.

MAC100_MMC_RXTCPERRFRM

Address: Operational Base(0xFFB30000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxtcp_err_frms Number of good IP datagrams whose TCP payload has a checksum error.

MAC100_MMC_RXICMPERRFRM

Address: Operational Base(0xFFB30000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxicmp_err_frms Number of good IP datagrams whose ICMP payload has a checksum error.

MAC100_MMC_RXIPV4HDERROCT

Address: Operational Base(0xFFB30000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv4_hdrerr_octets Number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter.

MAC100_MMC_RXIPV6HDERROCT

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Address: Operational Base(0xFFB30000) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv6_hdrerr_octets Number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the IPv6 header's Length field is used to update this counter.

MAC100_MMC_RXUDPERROCT

Address: Operational Base(0xFFB30000) + offset (0x0274)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxudp_err_octets Number of bytes received in a UDP segment that had checksum errors.

MAC100_MMC_RXTCPERROCT

Address: Operational Base(0xFFB30000) + offset (0x027C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxtcp_err_octets Number of bytes received in a TCP segment with checksum errors.

MAC100_MMC_RXICMPERROCT

Address: Operational Base(0xFFB30000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxicmp_err_octets Number of bytes received in an ICMP segment with checksum errors.

MAC100_BUS_MODE

Address: Operational Base(0xFFB30000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	AAL When this bit is set high and the FB bit equals 1, the AXI interface generates all bursts aligned to the start address LS bits. If the FB bit equals 0, the first burst (accessing the data buffer's start address) is not aligned, but subsequent bursts are aligned to the address.
24	RW	0x0	PBL_Mode When set high, this bit multiplies the PBL value programmed (bits [22:17] and bits [13:8]) eight times. Thus the DMA will transfer data in to a maximum of 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.
23	RW	0x0	USP When set high, it configures the RxDMA to use the value configured in bits [22:17] as PBL while the PBL value in bits [13:8] is applicable to TxDMA operations only. When reset to low, the PBL value in bits [13:8] is applicable for both DMA engines.
22:17	RW	0x01	RPBL These bits indicate the maximum number of beats to be transferred in one RxDMA transaction. This will be the maximum value that is used in a single block Read/Write. The RxDMA will always attempt to burst as specified in RPBL each time it starts a Burst transfer on the host bus. RPBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value will result in undefined behavior. These bits are valid and applicable

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Bit	Attr	Reset Value	Description
			only when USP is set high.
16	RW	0x0	FB This bit controls whether the AXI Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AXI will use SINGLE and INCR burst transfer operations.
15:14	RO	0x0	reserved
13:8	RW	0x01	PBL These bits indicate the maximum number of beats to be transferred in one DMA transaction. This will be the maximum value that is used in a single block Read/Write. The DMA will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value will result in undefined behavior. When USP is set high, this PBL value is applicable for TxDMA transactions only. The PBL values have the following limitations. The maximum number of beats (PBL) possible is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified (as given below). For different data bus widths and FIFO sizes, the valid PBL range (including x8 mode) is provided in the following table. If the PBL is common for both transmit and receive DMA, the minimum Rx FIFO and Tx FIFO depths must be considered. Do not program out-of-range PBL values, because the system may not behave properly. For TxFIFO, valid PBL range in full duplex mode and duplex mode is 128 or less. For RxFIFO, valid PBL range in full duplex mode is all.
7	RO	0x0	reserved
6:2	RW	0x00	DSL This bit specifies the number of dword to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When DSL value equals zero, then the descriptor table is taken as contiguous by the DMA, in Ring mode.
1	RO	0x0	reserved
0	R/W SC	0x1	SWR When this bit is set, the MAC DMA Controller resets all GMAC Subsystem internal registers and logic. It is cleared automatically after the reset operation has completed in all of the core clock domains. Read a 0 value in this bit before re-programming any register of the core. Note: The reset operation is completed only when all the resets in all the active clock domains are de-asserted. Hence it is essential that all the PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion.

MAC100_TX_POLL_DEMAND

Address: Operational Base(0xFFB30000) + offset (0x1004)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TPD When these bits are written with any value, the DMA reads the current descriptor pointed to by Register GMAC_CUR_HOST_TX_DESC. If that descriptor is not available (owned by Host), transmission returns to the Suspend state and DMA Register GMAC_STATUS[2] is asserted. If the descriptor is available, transmission resumes.

MAC100_RX_POLL_DEMAND

Address: Operational Base(0xFFB30000) + offset (0x1008)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RPD When these bits are written with any value, the DMA reads the current descriptor pointed to by Register GMAC_CUR_HOST_RX_DESC. If that descriptor is not available (owned by Host), reception returns to the Suspended state and Register GMAC_STATUS[7] is not asserted. If the descriptor is available, the Receive DMA returns to active state.

MAC100_RX_DESC_LIST_ADDR

Address: Operational Base(0xFFB30000) + offset (0x100C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRL This field contains the base address of the First Descriptor in the Receive Descriptor list. The LSB bits [1/2/3:0] for 32/64/128-bit bus width) will be ignored and taken as all-zero by the DMA internally. Hence these LSB bits are Read Only.

MAC100_TX_DESC_LIST_ADDR

Address: Operational Base(0xFFB30000) + offset (0x1010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	STL This field contains the base address of the First Descriptor in the Transmit Descriptor list. The LSB bits [1/2/3:0] for 32/64/128-bit bus width) will be ignored and taken as all-zero by the DMA internally. Hence these LSB bits are Read Only.

MAC100_STATUS

Address: Operational Base(0xFFB30000) + offset (0x1014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	GPI This bit indicates an interrupt event in the GMAC core's PMT module. The software must read the corresponding registers in the GMAC core to get the exact cause of interrupt and clear its source to reset this bit to 1'b0. The interrupt signal from the GMAC subsystem (sbd_intr_o) is high when this bit is high.
27	RO	0x0	GMI This bit reflects an interrupt event in the MMC module of the GMAC core. The software must read the corresponding registers in the GMAC core to get the exact cause of interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the GMAC subsystem (sbd_intr_o) is high when this bit is high.

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Bit	Attr	Reset Value	Description
26	RO	0x0	GLI This bit reflects an interrupt event in the GMAC Core's PCS or RGMII interface block. The software must read the corresponding registers in the GMAC core to get the exact cause of interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the GMAC subsystem (sbd_intr_o) is high when this bit is high.
25:23	RO	0x0	EB These bits indicate the type of error that caused a Bus Error (e.g., error response on the AXI interface). Valid only with Fatal Bus Error bit (Register GMAC_STATUS[13]) set. This field does not generate an interrupt. Bit 23: 1'b1 Error during data transfer by TxDMA 1'b0 Error during data transfer by RxDMA Bit 24: 1'b1 Error during read transfer 1'b0 Error during write transfer Bit 25: 1'b1 Error during descriptor access 1'b0 Error during data buffer access
22:20	RO	0x0	TS These bits indicate the Transmit DMA FSM state. This field does not generate an interrupt. 3'b000: Stopped; Reset or Stop Transmit Command issued. 3'b001: Running; Fetching Transmit Transfer Descriptor. 3'b010: Running; Waiting for status. 3'b011: Running; Reading Data from host memory buffer and queuing it to transmit buffer (Tx FIFO). 3'b100: TIME_STAMP write state. 3'b101: Reserved for future use. 3'b110: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow. 3'b111: Running; Closing Transmit Descriptor.
19:17	RO	0x0	RS These bits indicate the Receive DMA FSM state. This field does not generate an interrupt. 3'b000: Stopped: Reset or Stop Receive Command issued. 3'b001: Running: Fetching Receive Transfer Descriptor. 3'b010: Reserved for future use. 3'b011: Running: Waiting for receive packet. 3'b100: Suspended: Receive Descriptor Unavailable. 3'b101: Running: Closing Receive Descriptor. 3'b110: TIME_STAMP write state. 3'b111: Running: Transferring the receive packet data from receive buffer to host memory.
16	W1C	0x0	NIS Normal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in Register OP_MODE: Register GMAC_STATUS[0]: Transmit Interrupt Register GMAC_STATUS[2]: Transmit Buffer Unavailable Register GMAC_STATUS[6]: Receive Interrupt Register GMAC_STATUS[14]: Early Receive Interrupt Only unmasked bits affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing a 1 to this bit) each time a corresponding bit that causes NIS to be set is cleared.

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Bit	Attr	Reset Value	Description
15	W1C	0x0	AIS Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in Register OP_MODE: Register GMAC_STATUS[1]: Transmit Process Stopped Register GMAC_STATUS[3]: Transmit Jabber Timeout Register GMAC_STATUS[4]: Receive FIFO Overflow Register GMAC_STATUS[5]: Transmit Underflow Register GMAC_STATUS[7]: Receive Buffer Unavailable Register GMAC_STATUS[8]: Receive Process Stopped Register GMAC_STATUS[9]: Receive Watchdog Timeout Register GMAC_STATUS[10]: Early Transmit Interrupt Register GMAC_STATUS[13]: Fatal Bus Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared.
14	W1C	0x0	ERI This bit indicates that the DMA had filled the first data buffer of the packet. Receive Interrupt Register GMAC_STATUS[6] automatically clears this bit.
13	W1C	0x0	FBI This bit indicates that a bus error occurred, as detailed in [25:23]. When this bit is set, the corresponding DMA engine disables all its bus accesses.
12:11	RO	0x0	reserved
10	W1C	0x0	ETI This bit indicates that the frame to be transmitted was fully transferred to the MTL Transmit FIFO.
9	W1C	0x0	RWT This bit is asserted when a frame with a length greater than 2,048 bytes is received.
8	W1C	0x0	RPS This bit is asserted when the Receive Process enters the Stopped state.
7	W1C	0x0	RU This bit indicates that the Next Descriptor in the Receive List is owned by the host and cannot be acquired by the DMA. Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, Receive Process resumes when the next recognized incoming frame is received. Register GMAC_STATUS[7] is set only when the previous Receive Descriptor was owned by the DMA.
6	W1C	0x0	RI This bit indicates the completion of frame reception. Specific frame status information has been posted in the descriptor. Reception remains in the Running state.
5	W1C	0x0	UNF This bit indicates that the Transmit Buffer had an Underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set.
4	W1C	0x0	OVF This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to application, the overflow status is set in RDES0[11].

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Bit	Attr	Reset Value	Description
3	W1C	0x0	TJT This bit indicates that the Transmit Jabber Timer expired, meaning that the transmitter had been excessively active. The transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert.
2	W1C	0x0	TU This bit indicates that the Next Descriptor in the Transmit List is owned by the host and cannot be acquired by the DMA. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing transmit descriptors, the host should change the ownership of the bit of the descriptor and then issue a Transmit Poll Demand command.
1	W1C	0x0	TPS This bit is set when the transmission is stopped.
0	W1C	0x0	TI This bit indicates that frame transmission is finished and TDES1[31] is set in the First Descriptor.

MAC100_OP_MODE

Address: Operational Base(0xFFB30000) + offset (0x1018)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	DT When this bit is set, the core does not drop frames that only have errors detected by the Receive Checksum Offload engine. Such frames do not have any errors (including FCS error) in the Ethernet frame received by the MAC but have errors in the encapsulated payload only. When this bit is reset, all error frames are dropped if the FEF bit is reset.
25	RW	0x0	RSF When this bit is set, the MTL only reads a frame from the Rx FIFO after the complete frame has been written to it, ignoring RTC bits. When this bit is reset, the Rx FIFO operates in Cut-Through mode, subject to the threshold specified by the RTC bits.
24	RW	0x0	DFF When this bit is set, the RxDMA does not flush any frames due to the unavailability of receive descriptors/buffers as it does normally when this bit is reset.
23:22	RO	0x0	reserved
21	RW	0x0	TSF When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values specified in Register GMAC_OP_MODE[16:14] are ignored. This bit should be changed only when transmission is stopped.
20	W1C	0x0	FTF When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost/flushed. This bit is cleared internally when the flushing operation is completed fully. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter will not be flushed. It will be scheduled for transmission and will result in underflow and runt frame transmission. Note: The flush operation completes only after emptying the TxFIFO of its contents and all the pending Transmit Status of the

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Bit	Attr	Reset Value	Description
			transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock (clk_tx_i) is required to be active.
19:17	RO	0x0	reserved
16:14	RW	0x0	TTC These three bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. These bits are used only when the TSF bit (Bit 21) is reset. 3'b000: 64 3'b001: 128 3'b010: 192 3'b011: 256 3'b100: 40 3'b101: 32 3'b110: 24 3'b111: 16
13	RW	0x0	ST When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is the Transmit List Base Address set by Register GMAC_TX_DESC_LIST_ADDR, or from the position retained when transmission was stopped previously. If the current descriptor is not owned by the DMA, transmission enters the Suspended state and Transmit Buffer Unavailable (Register GMAC_STATUS[2]) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting DMA Register TX_DESC_LIST_ADDR, then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and becomes the current position when transmission is restarted. The stop transmission command is effective only the transmission of the current frame is complete or when the transmission is in the Suspended state.
12:11	RW	0x0	RFD These bits control the threshold (Fill-level of Rx FIFO) at which the flow-control is de-asserted after activation. 2'b00: Full minus 1 KB 2'b01: Full minus 2 KB 2'b10: Full minus 3 KB 2'b11: Full minus 4 KB Note that the de-assertion is effective only after flow control is asserted.
10:9	RW	0x0	RFA These bits control the threshold (Fill level of Rx FIFO) at which flow control is activated. 2'b00: Full minus 1 KB 2'b01: Full minus 2 KB 2'b10: Full minus 3 KB 2'b11: Full minus 4 KB Note that the above only applies to Rx FIFOs of 4 KB or more when the EFC bit is set high.

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Bit	Attr	Reset Value	Description
8	RW	0x0	EFC When this bit is set, the flow control signal operation based on fill-level of Rx FIFO is enabled. When reset, the flow control operation is disabled.
7	RW	0x0	FEF When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, overflow). However, if the frame's start byte (write) pointer is already transferred to the read controller side (in Threshold mode), then the frames are not dropped. When FEF is set, all frames except runt error frames are forwarded to the DMA. But when RxFIFO overflows when a partial frame is written, then such frames are dropped even when FEF is set.
6	RW	0x0	FUF When set, the Rx FIFO will forward Undersized frames (frames with no Error and length less than 64 bytes) including pad-bytes and CRC). When reset, the Rx FIFO will drop all frames of less than 64 bytes, unless it is already transferred due to lower value of Receive Threshold (e.g., RTC = 01).
5	RO	0x0	reserved
4:3	RW	0x0	RTC These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. Note that value of 11 is not applicable if the configured Receive FIFO size is 128 bytes. These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. 2'b00: 64 2'b01: 32 2'b10: 96 2'b11: 128
2	RW	0x0	OSF When this bit is set, this bit instructs the DMA to process a second frame of Transmit data even before status for first frame is obtained.
1	RW	0x0	SR When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes incoming frames. Descriptor acquisition is attempted from the current position in the list, which is the address set by register GMAC_RX_DESC_LIST_ADDR or the position retained when the Receive process was previously stopped. If no descriptor is owned by the DMA, reception is suspended and Receive Buffer Unavailable (Register GMAC_STATUS[7]) is set. The Start Receive command is effective only when reception has stopped. If the command was issued before setting register GMAC_RX_DESC_LIST_ADDR, DMA behavior is unpredictable. When this bit is cleared, RxDMA operation is stopped after the transfer of the current frame. The next descriptor position in the Receive list is saved and becomes the current position after the Receive process is restarted. The Stop Receive command is

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Bit	Attr	Reset Value	Description
			effective only when the Receive process is in either the Running (waiting for receive packet) or in the Suspended state.
0	RO	0x0	reserved

MAC100_INT_ENA

Address: Operational Base(0xFFB30000) + offset (0x101C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	NIE When this bit is set, a normal interrupt is enabled. When this bit is reset, a normal interrupt is disabled. This bit enables the following bits: Register GMAC_STATUS[0]: Transmit Interrupt Register GMAC_STATUS[2]: Transmit Buffer Unavailable Register GMAC_STATUS[6]: Receive Interrupt Register GMAC_STATUS[14]: Early Receive Interrupt
15	RW	0x0	AIE When this bit is set, an Abnormal Interrupt is enabled. When this bit is reset, an Abnormal Interrupt is disabled. This bit enables the following bits Register GMAC_STATUS[1]: Transmit Process Stopped Register GMAC_STATUS[3]: Transmit Jabber Timeout Register GMAC_STATUS[4]: Receive Overflow Register GMAC_STATUS[5]: Transmit Underflow Register GMAC_STATUS[7]: Receive Buffer Unavailable Register GMAC_STATUS[8]: Receive Process Stopped Register GMAC_STATUS[9]: Receive Watchdog Timeout Register GMAC_STATUS[10]: Early Transmit Interrupt Register GMAC_STATUS[13]: Fatal Bus Error
14	RW	0x0	ERE When this bit is set with Normal Interrupt Summary Enable (BIT 16), Early Receive Interrupt is enabled. When this bit is reset, Early Receive Interrupt is disabled.
13	RW	0x0	FBE When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), the Fatal Bus Error Interrupt is enabled. When this bit is reset, Fatal Bus Error Enable Interrupt is disabled.
12:11	RO	0x0	reserved
10	RW	0x0	ETE When this bit is set with an Abnormal Interrupt Summary Enable (BIT 15), Early Transmit Interrupt is enabled. When this bit is reset, Early Transmit Interrupt is disabled.
9	RW	0x0	RWE When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), the Receive Watchdog Timeout Interrupt is enabled. When this bit is reset, Receive Watchdog Timeout Interrupt is disabled.
8	RW	0x0	RSE When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Receive Stopped Interrupt is enabled. When this bit is reset, Receive Stopped Interrupt is disabled.
7	RW	0x0	RUE When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled

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Bit	Attr	Reset Value	Description
6	RW	0x0	RIE When this bit is set with Normal Interrupt Summary Enable (BIT 16), Receive Interrupt is enabled. When this bit is reset, Receive Interrupt is disabled.
5	RW	0x0	UNE When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Transmit Underflow Interrupt is enabled. When this bit is reset, Underflow Interrupt is disabled.
4	RW	0x0	OVE When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Receive Overflow Interrupt is enabled. When this bit is reset, Overflow Interrupt is disabled
3	RW	0x0	TJE When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, Transmit Jabber Timeout Interrupt is disabled.
2	RW	0x0	TUE When this bit is set with Normal Interrupt Summary Enable (BIT 16), Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, Transmit Buffer Unavailable Interrupt is disabled.
1	RW	0x0	TSE When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Transmission Stopped Interrupt is enabled. When this bit is reset, Transmission Stopped Interrupt is disabled.
0	RW	0x0	TIE When this bit is set with Normal Interrupt Summary Enable (BIT 16), Transmit Interrupt is enabled. When this bit is reset, Transmit Interrupt is disabled.

MAC100_OVERFLOW_CNT

Address: Operational Base(0xFFB30000) + offset (0x1020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RC	0x0	FIFO_overflow_bit Overflow bit for FIFO Overflow Counter
27:17	RC	0x000	Frame_miss_number This counter is incremented each time the MTL asserts the sideband signal mtl_rxoverflow_o. The counter is cleared when this register is read with mci_be_i[2] at 1'b1.
16	RC	0x0	Miss_frame_overflow_bit Overflow bit for Missed Frame Counter
15:0	RC	0x0000	Frame_miss_number_2 Indicates the number of frames missed by the controller due to the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.

MAC100_REC_INT_WDT_TIMER

Address: Operational Base(0xFFB30000) + offset (0x1024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	RIWT Indicates the number of system clock cycles multiplied by 256 for which the watchdog timer is set. The watchdog timer gets triggered with the programmed value after the RxDMA completes the transfer of a frame for which the RI status bit is not set due to the setting in the corresponding descriptor RDES1[31]. When the watch-dog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when RI bit is set high due to automatic setting of RI as per RDES1[31] of any received frame.

MAC100_AXI_BUS_MODE

Address: Operational Base(0xFFB30000) + offset (0x1028)

Bit	Attr	Reset Value	Description
31	RW	0x0	EN_LPI When set to 1, enable the LPI (Low Power Interface) supported by the GMAC and accepts the LPI request from the AXI System Clock controller. When set to 0, disables the Low Power Mode and always denies the LPI request from the AXI System Clock controller.
30	RW	0x0	UNLCK_ON_MGK_RWK When set to 1, enables it to request coming out of Low Power mode only when Magic Packet or Remote Wake Up Packet is received. When set to 0, enables it requests to come out of Low Power mode when any frame is received.
29:22	RO	0x00	reserved
21:20	RW	0x1	WR_OSR_LMT This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT+1
19:18	RO	0x0	reserved
17:16	RW	0x1	RD_OSR_LMT This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT+1
15:13	RO	0x0	reserved
12	RO	0x0	AXI_AAL This bit is read-only bit and reflects the AAL bit Register0 (register GMAC_BUS_MODE[25]). When this bit set to 1, it performs address-aligned burst transfers on both read and write channels.
11:4	RO	0x00	reserved
3	RW	0x0	BLEN16 When this bit is set to 1, or when UNDEF is set to 1, it is allowed to select a burst length of 16.
2	RW	0x0	BLEN8 When this bit is set to 1, or when UNDEF is set to 1, it is allowed to select a burst length of 8.
1	RW	0x0	BLEN4 When this bit is set to 1, or when UNDEF is set to 1, it is allowed to select a burst length of 4.

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Bit	Attr	Reset Value	Description
0	RO	0x1	UNDEF This bit is read-only bit and indicates the complement (invert) value of FB bit in register GMAC_BUS_MODE[16]. When this bit is set to 1, it is allowed to perform any burst length equal to or below the maximum allowed burst length as programmed in bits[7:1]; When this bit is set to 0, it is allowed to perform only fixed burst lengths as indicated by BLEN256/128/64/32/16/8/4, or a burst length of 1.

MAC100_AXI_STATUS

Address: Operational Base(0xFFB30000) + offset (0x102C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	RD_CH_STA When high, it indicates that AXI Master's read channel is active and transferring data.
0	RO	0x0	WR_CH_STA When high, it indicates that AXI Master's write channel is active and transferring data.

MAC100_CUR_HOST_TX_DESC

Address: Operational Base(0xFFB30000) + offset (0x1048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HTDAP Cleared on Reset. Pointer updated by DMA during operation.

MAC100_CUR_HOST_RX_DESC

Address: Operational Base(0xFFB30000) + offset (0x104C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HRDAP Cleared on Reset. Pointer updated by DMA during operation.

MAC100_CUR_HOST_TX_BUF_ADDR

Address: Operational Base(0xFFB30000) + offset (0x1050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HTBAP Cleared on Reset. Pointer updated by DMA during operation.

MAC100_CUR_HOST_RX_BUF_ADDR

Address: Operational Base(0xFFB30000) + offset (0x1054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HRBAP Cleared on Reset. Pointer updated by DMA during operation.

9.5 Interface Description

Table 9-1 MAC100 Interface

Module Pin	Dir.	Pad Name	IOMUX Setting
RMII interface			
mac100_mclkinout	I/O	I2S2_SCLK_M0/RGMII_CLK_M1/UART4_RX_M1/SPI2_CSN1_M1/RMII_CLK/GPIO1_D5_d	GPIO1D_IOMUX_SEL_H[6:4]=3'h5
mac100_rxdvcrs	I	I2S2_LRCK_M0/RGMII_RXDV_M1/UART4_TX_M1/SPI2_CSN0_M1/RMII_RXDV_CRS/GPIO1_D6_d	GPIO1D_IOMUX_SEL_H[10:8]=3'h5
mac100_rxer	I	I2S2_SDI_M0/RGMII_RXER_M1/UART4_CTSN_M1/SPI2_MISO_M1/PWM15_M1/RMII_RXER/GPIO2_A0_d	GPIO2A_IOMUX_SEL_L[2:0]=3'h5

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Module Pin	Dir.	Pad Name	IOMUX Setting
mac100_rxd0	I	UART1_CTSN_M0/RGMII_RXD0_M1/I2S0_SDI3_M1/PWM7_M1/RMII_RXD0/GPIO1_D4_d	GPIO1D_IOMUX_SEL_H[2:0]=3'h5
mac100_rxd1	I	I2S2_SDO_M0/RGMII_RXD1_M1/UART4_RTSN_M1/SPI2_MOSI_M1/PWM14_M1/RMII_RXD1/GPIO1_D7_d	GPIO1D_IOMUX_SEL_H[14:12]=3'h5
mac100_txen	O	UART1_RTSN_M0/RGMII_TXEN_M1/I2S0_SDI2_M1/PWM6_M1/RMII_TXEN/GPIO1_D3_d	GPIO1D_IOMUX_SEL_L[14:12]=3'h5
mac100_txd0	O	UART1_RX_M0/RGMII_TXD0_M1/I2S0_SDO1_M1/PWM4_M1/RMII_TXD0/GPIO1_D1_d	GPIO1D_IOMUX_SEL_L[6:4]=3'h5
mac100_txd1	O	UART1_TX_M0/RGMII_TXD1_M1/I2S0_SDO2_M1/PWM5_M1/RMII_TXD1/GPIO1_D2_d	GPIO1D_IOMUX_SEL_L[10:8]=3'h5
Management interface			
mac100_mdc	O	SDMMC1_PWREN/RGMII_MDC_M1/PWM2_M1/I2C5_SCL_M1/RMII_MDC/GPIO1_C7_d	GPIO1C_IOMUX_SEL_H[14:12]=3'h5
mac100_mdio	I/O	SDMMC1_DETN/RGMII_MDIO_M1/PWM3_M1/I2C5_SDA_M1/RMII_MDIO/GPIO1_D0_d	GPIO1D_IOMUX_SEL_L[2:0]=3'h5

9.6 Application Note

9.6.1 Descriptors

The DMA in MAC can communicate with Host driver through descriptor lists and data buffers. The DMA transfers data frames received by the core to the Receive Buffer in the Host memory, and Transmit data frames from the Transmit Buffer in the Host memory. Descriptors that reside in the Host memory act as pointers to these buffers.

There are two descriptor lists; one for reception, and one for transmission. The base address of each list is written into DMA Registers RX_DESC_LIST_ADDR and TX_DESC_LIST_ADDR, respectively. A descriptor list is forward linked (either implicitly or explicitly). The last descriptor may point back to the first entry to create a ring structure. Explicit chaining of descriptors is accomplished by setting the second address chained in both Receive and Transmit descriptors (RDES1[24] and TDES1[24]). The descriptor lists reside in the Host physical memory address space. Each descriptor can point to a maximum of two buffers. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.

A data buffer resides in the Host physical memory space, and consists of an entire frame or part of a frame, but cannot exceed a single frame. Buffers contain only data, buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. However, a single descriptor cannot span multiple frames. The DMA will skip to the next frame buffer when end-of-frame is detected. Data chaining can be enabled or disabled The descriptor ring and chain structure is shown in following figure.

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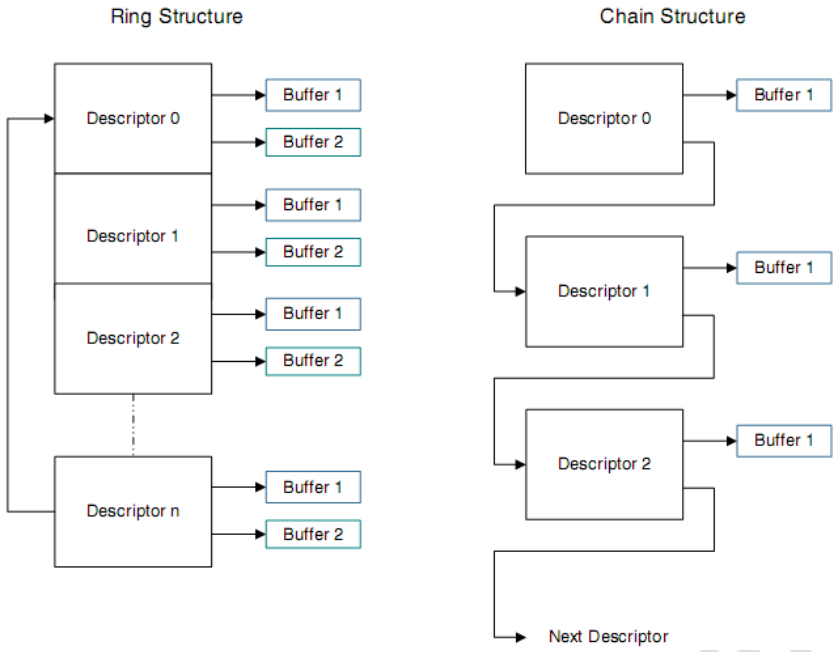

Fig. 9-11Descriptor Ring and Chain Structure

Each descriptor contains two buffers, two byte-count buffers, and two address pointers, which enable the adapter port to be compatible with various types of memory management schemes. The descriptor addresses must be aligned to the bus width used (Word/Dword/Lword for 32/64/128-bit buses).

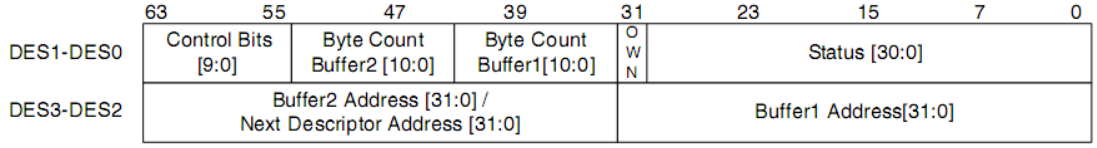

Fig. 9-12Rx/Tx Descriptors definition

9.6.2 Receive Descriptors

The MAC Subsystem requires at least two descriptors when receiving a frame. The Receive state machine of the DMAalways attempts to acquire an extra descriptor in anticipation of an incoming frame. (The size of the incoming frame is unknown). Before the RxDMA closes a descriptor, it will attempt to acquire the next descriptor even if no frames are received. In a single descriptor (receive) system, the subsystem will generate a descriptor error if the receive buffer is unable to accommodate the incoming frame and the next descriptor is not owned by the DMA. Thus, the Host is forced to increase either its descriptor pool or the buffer size. Otherwise, the subsystem starts dropping all incoming frames.

Receive Descriptor 0 (RDES0)

RDES0 contains the received frame status, the frame length, and the descriptor ownership information.

Table 9-2 Receive Descriptor 0

Bit	Description
31	OWN: Own Bit When set, this bit indicates that the descriptor is owned by the DMA of the MAC Subsystem. When this bit is reset, this bit indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	AFM: Destination Address Filter Fail When set, this bit indicates a frame that failed in the DA Filter in the MAC Core.
29:16	FL: Frame Length These bits indicate the byte length of the received frame that was transferred to host memory (including CRC). This field is valid when Last Descriptor (RDES0[8]) is set and either the Descriptor Error (RDES0[14]) or Overflow Error bits are reset. The frame length also includes the two bytes appended to the Ethernet

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Bit	Description
	frame when IP checksum calculation (Type 1) is enabled and the received frame is not a MAC control frame. This field is valid when Last Descriptor (RDES0[8]) is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current frame.
15	ES: Error Summary Indicates the logical OR of the following bits: • RDES0[0]: Payload Checksum Error • RDES0[1]: CRC Error • RDES0[3]: Receive Error • RDES0[4]: Watchdog Timeout • RDES0[6]: Late Collision • RDES0[7]: IPC Checksum • RDES0[11]: Overflow Error • RDES0[14]: Descriptor Error This field is valid only when the Last Descriptor (RDES0[8]) is set.
14	DE: Descriptor Error When set, this bit indicates a frame truncation caused by a frame that does not fit within the current descriptor buffers, and that the DMA does not own the Next Descriptor. The frame is truncated. This field is valid only when the Last Descriptor (RDES0[8]) is set
13	SAF: Source Address Filter Fail When set, this bit indicates that the SA field of frame failed the SA Filter in the MAC Core.
12	LE: Length Error When set, this bit indicates that the actual length of the frame received and that the Length/ Type field does not match. This bit is valid only when the Frame Type (RDES0[5]) bit is reset. Length error status is not valid when CRC error is present.
11	OE: Overflow Error When set, this bit indicates that the received frame was damaged due to buffer overflow.
10	VLAN: VLAN Tag When set, this bit indicates that the frame pointed to by this descriptor is a VLAN frame tagged by the MAC Core.
9	FS: First Descriptor When set, this bit indicates that this descriptor contains the first buffer of the frame. If the size of the first buffer is 0, the second buffer contains the beginning of the frame. If the size of the second buffer is also 0, the next Descriptor contains the beginning of the frame.
8	LS: Last Descriptor When set, this bit indicates that the buffers pointed to by this descriptor are the last buffers of the frame.
7	IPC Checksum Error/Giant Frame When IP Checksum Engine is enabled, this bit, when set, indicates that the 16-bit IPv4 Header checksum calculated by the core did not match the received checksum bytes. The Error Summary bit[15] is NOT set when this bit is set in this mode.
6	LC: Late Collision When set, this bit indicates that a late collision has occurred while receiving the frame in Half-Duplex mode.
5	FT: Frame Type When set, this bit indicates that the Receive Frame is an Ethernet-type frame (the LT field is greater than or equal to 16'h0600). When this bit is reset, it indicates that the received frame is an IEEE802.3 frame. This bit is not valid for

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Bit	Description
	Runt frames less than 14 bytes.
4	RWT: Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer has expired while receiving the current frame and the current frame is truncated after the Watchdog Timeout.
3	RE: Receive Error When set, this bit indicates that the gmii_rxer_i signal is asserted while gmii_rxdv_i is asserted during frame reception. This error also includes carrier extension error in GMII and Half-duplex mode. Error can be of less/no extension, or error (rxd≠ 0f) during extension.
2	DE: Dribble Bit Error When set, this bit indicates that the received frame has a non-integer multiple of bytes (odd nibbles). This bit is valid only in MII Mode.
1	CE: CRC Error When set, this bit indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received frame. This field is valid only when the Last Descriptor (RDES0[8]) is set.
0	Rx MAC Address/Payload Checksum Error When set, this bit indicates that the Rx MAC Address registers value (1 to 15) matched the frame's DA field. When reset, this bit indicates that the Rx MAC Address Register 0 value matched the DA field. If Full Checksum Offload Engine is enabled, this bit, when set, indicates the TCP, UDP, or ICMP checksum the core calculated does not match the received encapsulated TCP, UDP, or ICMP segment's Checksum field. This bit is also set when the received number of payload bytes does not match the value indicated in the Length field of the encapsulated IPv4 or IPv6 datagram in the received Ethernet frame.

Receive Descriptor 1 (RDES1)

RDES1 contains the buffer sizes and other bits that control the descriptor chain/ring.

Table 9-3 Receive Descriptor 1

Bit	Description
31	Disable Interrupt on Completion When set, this bit will prevent the setting of the RI (CSR5[6]) bit of the MAC_STATUS Register for the received frame that ends in the buffer pointed to by this descriptor. This, in turn, will disable the assertion of the interrupt to Host due to RI for that frame.
30:26	Reserved.
25	RER: Receive End of Ring When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a Descriptor Ring.
24	RCH: Second Address Chained When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When RDES1[24] is set, RBS2 (RDES1[21-11]) is a "don't care" value. RDES1[25] takes precedence over RDES1[24].
23:22	Reserved.
21:11	RBS2: Receive Buffer 2 Size These bits indicate the second data buffer size in bytes. The buffer size must be a multiple of 8 depending upon the bus widths (64), even if the value of RDES3 (buffer2 address pointer) is not aligned to bus width. In the case where the buffer size is not a multiple of 8, the resulting behavior is undefined. This field is not valid if RDES1[24] is set.
10:0	RBS1: Receive Buffer 1 Size Indicates the first data buffer size in bytes. The buffer size must be a multiple of

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Bit	Description
	8 depending upon the bus widths (64), even if the value of RDES2 (buffer1 address pointer) is not aligned. In the case where the buffer size is not a multiple of 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or next descriptor depending on the value of RCH (Bit 24).

Receive Descriptor 2 (RDES2)

RDES2 contains the address pointer to the first data buffer in the descriptor.

Table 9-4 Receive Descriptor 2

Bit	Description
31:0	Buffer 1 Address Pointer These bits indicate the physical address of Buffer 1. There are no limitations on the buffer address alignment except for the following condition: The DMA uses the configured value for its address generation when the RDES2 value is used to store the start of frame. Note that the DMA performs a write operation with the RDES2[2:0] bits as 0 during the transfer of the start of frame but the frame data is shifted as per the actual Buffer address pointer. The DMA ignores RDES2[2:0] (corresponding to bus width of 64) if the address pointer is to a buffer where the middle or last part of the frame is stored.

Receive Descriptor 3 (RDES3)

RDES3 contains the address pointer either to the second data buffer in the descriptor or to the next descriptor.

Table 9-5 Receive Descriptor 3

Bit	Description
31:0	Buffer 2 Address Pointer (Next Descriptor Address) These bits indicate the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained (RDES1[24]) bit is set, this address contains the pointer to the physical memory where the Next Descriptor is present. If RDES1[24] is set, the buffer (Next Descriptor) address pointer must be bus width-aligned (RDES3[2:0] = 0, corresponding to a bus width of 64. LSBs are ignored internally.) However, when RDES1[24] is reset, there are no limitations on the RDES3 value, except for the following condition: The DMA uses the configured value for its buffer address generation when the RDES3 value is used to store the start of frame. The DMA ignores RDES3[2:0] (corresponding to a bus width of 64) if the address pointer is to a buffer where the middle or last part of the frame is stored.

9.6.3 Transmit Descriptors

The descriptor addresses must be aligned to the bus width used (64). Each descriptor is provided with two buffers, two byte-count buffers, and two address pointers, which enable the adapter port to be compatible with various types of memory-management schemes.

Transmit Descriptor 0 (TDES0)

TDES0 contains the transmitted frame status and the descriptor ownership information.

Table 9-6 Transmit Descriptor 0

Bit	Description
31	OWN: Own Bit When set, this bit indicates that the descriptor is owned by the DMA. When this bit is reset, this bit indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame transmission or when the buffers allocated in the descriptor are empty. The ownership bit of the First Descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between

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Bit	Description
	fetching a descriptor and the driver setting an ownership bit.
30:17	Reserved.
16	IHE: IP Header Error When set, this bit indicates that the Checksum Offload engine detected an IP header error and consequently did not modify the transmitted frame for any checksum insertion.
15	ES: Error Summary Indicates the logical OR of the following bits: • TDES0[14]: Jabber Timeout • TDES0[13]: Frame Flush • TDES0[11]: Loss of Carrier • TDES0[10]: No Carrier • TDES0[9]: Late Collision • TDES0[8]: Excessive Collision • TDES0[2]: Excessive Deferral • TDES0[1]: Underflow Error
14	JT: Jabber Timeout When set, this bit indicates the MAC transmitter has experienced a jabber time-out.
13	FF: Frame Flushed When set, this bit indicates that the DMA/MTL flushed the frame due to a SW flush command given by the CPU.
12	PCE: Payload Checksum Error This bit, when set, indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either due to insufficient bytes, as indicated by the IP Header's Payload Length field, or the MTL starting to forward the frame to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet frame being transmitted: to avoid deadlock, the MTL starts forwarding the frame when the FIFO is full, even in Store-and-Forward mode.
11	LC: Loss of Carrier When set, this bit indicates that Loss of Carrier occurred during frame transmission. This is valid only for the frames transmitted without collision and when the MAC operates in Half-Duplex Mode.
10	NC: No Carrier When set, this bit indicates that the carrier sense signal form the PHY was not asserted during transmission.
9	LC: Late Collision When set, this bit indicates that frame transmission was aborted due to a collision occurring after the collision window (64 byte times including Preamble in RMII Mode and 512 byte times including Preamble and Carrier Extension in RGMII Mode). Not valid if Underflow Error is set.
8	EC: Excessive Collision When set, this bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame. If the DR (Disable Retry) bit in the MAC Configuration Register is set, this bit is set after the first collision and the transmission of the frame is aborted.
7	VF: VLAN Frame When set, this bit indicates that the transmitted frame was a VLAN-type frame.
6:3	CC: Collision Count This 4-bit counter value indicates the number of collisions occurring before the frame was transmitted. The count is not valid when the Excessive Collisions bit (TDES0[8]) is set.

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Bit	Description
2	ED: Excessive Deferral When set, this bit indicates that the transmission has ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000-Mbps mode) if the Deferral Check (DC) bit is set high in the MAC Control Register.
1	UF: Underflow Error When set, this bit indicates that the MAC aborted the frame because data arrived late from the Host memory. Underflow Error indicates that the DMA encountered an empty Transmit Buffer while transmitting the frame. The transmission process enters the suspended state and sets both Transmit Underflow (Register MAC_STATUS[5]) and Transmit Interrupt (Register MAC_STATUS [0]).
0	DB: Deferred Bit When set, this bit indicates that the MAC defers before transmission because of the presence of carrier. This bit is valid only in Half-Duplex mode.

Transmit Descriptor 1 (TDES1)

TDES1 contains the buffer sizes and other bits which control the descriptor chain/ring and the frame being transferred.

Table 9-7 Transmit Descriptor 1

Bit	Description
31	IC: Interrupt on Completion When set, this bit sets Transmit Interrupt (Register 5[0]) after the present frame has been transmitted.
30	LS: Last Segment When set, this bit indicates that the buffer contains the last segment of the frame.
29	FS: First Segment When set, this bit indicates that the buffer contains the first segment of a frame.
28:27	CIC: Checksum Insertion Control These bits control the insertion of checksums in Ethernet frames that encapsulate TCP, UDP, or ICMP over IPv4 or IPv6 as described below. • 2'b00: Do nothing. Checksum Engine is bypassed • 2'b01: Insert IPv4 header checksum. Use this value to insert IPv4 header checksum when the frame encapsulates an IPv4 datagram. • 2'b10: Insert TCP/UDP/ICMP checksum. The checksum is calculated over the TCP, UDP, or ICMP segment only and the TCP, UDP, or ICMP pseudo-header checksum is assumed to be present in the corresponding input frame's Checksum field. An IPv4 header checksum is also inserted if the encapsulated datagram conforms to IPv4. • 2'b11: Insert a TCP/UDP/ICMP checksum that is fully calculated in this engine. In other words, the TCP, UDP, or ICMP pseudo-header is included in the checksum calculation, and the input frame's corresponding Checksum field has an all-zero value. An IPv4 Header checksum is also inserted if the encapsulated datagram conforms to IPv4. The Checksum engine detects whether the TCP, UDP, or ICMP segment is encapsulated in IPv4 or IPv6 and processes its data accordingly.
26	DC: Disable CRC When set, the MAC does not append the Cyclic Redundancy Check (CRC) to the end of the transmitted frame. This is valid only when the first segment (TDES1[29]).
25	TER: Transmit End of Ring When set, this bit indicates that the descriptor list reached its final descriptor. The returns to the base address of the list, creating a descriptor ring.
24	TCH: Second Address Chained When set, this bit indicates that the second address in the descriptor is the Next

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Bit	Description
	Descriptor address rather than the second buffer address. When TDES1[24] is set, TBS2 (TDES1[21–11]) are "don't care" values. TDES1[25] takes precedence over TDES1[24].
23	DP: Disable Padding When set, the MAC does not automatically add padding to a frame shorter than 64 bytes. When this bit is reset, the DMA automatically adds padding and CRC to a frame shorter than 64 bytes and the CRC field is added despite the state of the DC (TDES1[26]) bit. This is valid only when the first segment (TDES1[29]) is set.
22	Reserved.
21:11	TBS2: Transmit Buffer 2 Size These bits indicate the Second Data Buffer in bytes. This field is not valid if TDES1[24] is set.
10:0	TBS1: Transmit Buffer 1 Size These bits indicate the First Data Buffer byte size. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or next descriptor depending on the value of TCH (Bit 24).

Transmit Descriptor 2 (TDES2)

TDES2 contains the address pointer to the first buffer of the descriptor.

Table 9-8 Transmit Descriptor 2

Bit	Description
31:0	Buffer 1 Address Pointer These bits indicate the physical address of Buffer 1. There is no limitation on the buffer address alignment.

Transmit Descriptor 3 (TDES3)

TDES3 contains the address pointer either to the second buffer of the descriptor or the next descriptor.

Table 9-9 Transmit Descriptor 3

Bit	Description
31:0	Buffer 2 Address Pointer (Next Descriptor Address) Indicates the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained (TDES1[24]) bit is set, this address contains the pointer to the physical memory where the Next Descriptor is present. The buffer address pointer must be aligned to the bus width only when TDES1[24] is set. (LSBs are ignored internally.)

9.6.4 Programming Guide

DMA Initialization – Descriptors

The following operations must be performed to initialize the DMA.

1. Provide a software reset. This will reset all of the MAC internal registers and logic. (MAC_OP_MODE[0]).
2. Wait for the completion of the reset process (poll MAC_OP_MODE[0], which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the Bus Mode Register by setting values in registerMAC_BUS_MODE
   a. Mixed Burst and AAL
   b. Fixed burst or undefined burst
   c. Burst length values and burst mode values.
   d. Descriptor Length (only valid if Ring Mode is used)
   e. Tx and Rx DMA Arbitration scheme
4. Program the AXI Interface options in the register MAC_BUS_MODE
   a. If fixed burst-length is enabled, then select the maximum burst-length possible on the AXI bus (Bits[7:1])

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5. A proper descriptor chain for transmit and receive must be created. It should also ensure that the receive descriptors are owned by DMA (bit 31 of descriptor should be set). When OSF mode is used, at least two descriptors are required.
6. Software should create three or more different transmit or receive descriptors in the chain before reusing any of the descriptors.
7. Initialize receive and transmit descriptor list address with the base address of transmit and receive descriptor (register MAC_RX_DESC_LIST_ADDR andMAC_TX_DESC_LIST_ADDR).
8. Program the following fields to initialize the mode of operation by setting values in registerMAC_OP_MODE
   a. Receive and Transmit Store and Forward
   b. Receive and Transmit Threshold Control (RTC and TTC)
   c. Hardware Flow Control enable
   d. Flow Control Activation and De-activation thresholds for MTL Receive and Transmit FIFO (RFA and RFD)
   e. Error Frame and undersized good frame forwarding enable
   f. OSF Mode
9. Clear the interrupt requests, by writing to those bits of the status register (interrupt bits only) which are set. For example, by writing 1 into bit 16 - normal interrupt summary will clear this bit (registerMAC_STATUS).
10. Enable the interrupts by programming the interrupt enable register MAC_INT_ENA.
11. Start the Receive and Transmit DMA by setting SR (bit 1) and ST (bit 13) of the control register MAC_OP_MODE.

MAC Initialization

The following MAC Initialization operations can be performed after the DMA initialization sequence. If the MAC Initialization is done before the DMA is set-up, then enable the MAC receiver (last step below) only after the DMA is active. Otherwise, received frames will fill the RxFIFO and overflow.
1. Program the register MAC_GMII_ADDR for controlling the management cycles for external PHY, for example, Physical Layer Address PA (bits 15-11). Also set bit 0 (GMII Busy) for writing into PHY and reading from PHY.
2. Read the 16-bit data of (MAC_GMII_DATA) from the PHY for link up, speed of operation, and mode of operation, by specifying the appropriate address value in registerMAC_GMII_ADDR (bits 15-11).
3. Provide the MAC address registers (MAC_MAC_ADDR0_HI and MAC_MAC_ADDR0_LO).
4. If Hash filtering is enabled in your configuration, program the Hash filter register (MAC_HASH_TAB_HI and MAC_HASH_TAB_LO).
5. Program the following fields to set the appropriate filters for the incoming frames in register MAC_MAC_FRM_FILT
   a. Receive All
   b. Promiscuous mode
   c. Hash or Perfect Filter
   d. Unicast, Multicast, broad cast and control frames filter settings etc.
6. Program the following fields for proper flow control in register MAC_FLOW_CTRL.
   a. Pause time and other pause frame control bits
   b. Receive and Transmit Flow control bits
   c. Flow Control Busy/Backpressure Activate
7. Program the Interrupt Mask register bits, as required, and if applicable, for your configuration.
8. Program the appropriate fields in register MAC_MAC_CONF for example, Inter-frame gap while transmission, jabber disable, etc. Based on the Auto-negotiation you can set the Duplex mode (bit 11), port select (bit 15), etc.
9. Set the bits Transmit enable (TE bit-3) and Receive Enable (RE bit-2) in register MAC_MAC_CONF.

Normal Receive and Transmit Operation

For normal operation, the following steps can be followed.

- For normal transmit and receive interrupts, read the interrupt status. Then poll the

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descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).

- On completion of the above step, set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
- If the descriptors were not owned by the DMA (or no descriptor is available), the DMA will go into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and issuing a poll demand by writing 0 into the Tx/Rx poll demand register (MAC_TX_POLL_DEMAND and MAC_RX_POLL_DEMAND).
- The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (MAC_CUR_HOST_TX_DESC andMAC_CUR_HOST_RX_DESC).
- The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (MAC_CUR_HOST_TX_Buf_ADDR andMAC_CUR_HOST_RX_BUF_ADDR).

Stop and Start Operation

When the transmission is required to be paused for some time then the following steps can be followed.

1. Disable the Transmit DMA (if applicable), by clearing ST (bit 13) of the control registerMAC_OP_MODE.
2. Wait for any previous frame transmissions to complete. This can be checked by reading the appropriate bits of MAC Debug register.
3. Disable the MAC transmitter and MAC receiver by clearing the bits Transmit enable (TE bit-3) and Receive Enable (RE bit-2) in register MAC_MAC_CONF.
4. Disable the Receive DMA (if applicable), after making sure the data in the RX FIFO is transferred to the system memory (by reading the registerMAC_DEBUG).
5. Make sure both the TX FIFO and RX FIFO are empty.
6. To re-start the operation, start the DMAs first, before enabling the MAC Transmitter and Receiver.

9.6.5 Clock Architecture

In RMII mode, reference clock and TX/RX clock can be from CRU or external OSC as following figure. GMAC in the picture is MAC100.

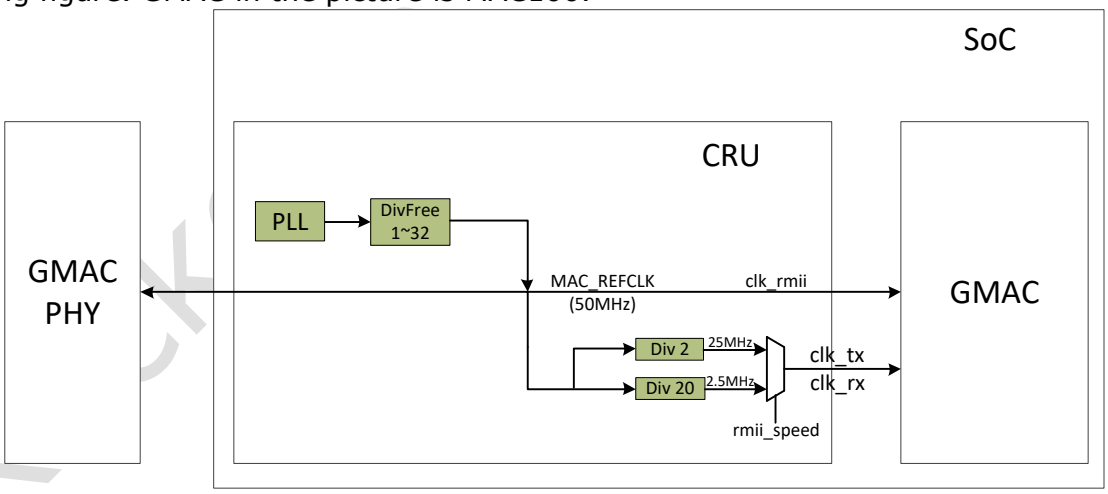

Fig. 9-13 RMII clock architecture when clock source from CRU

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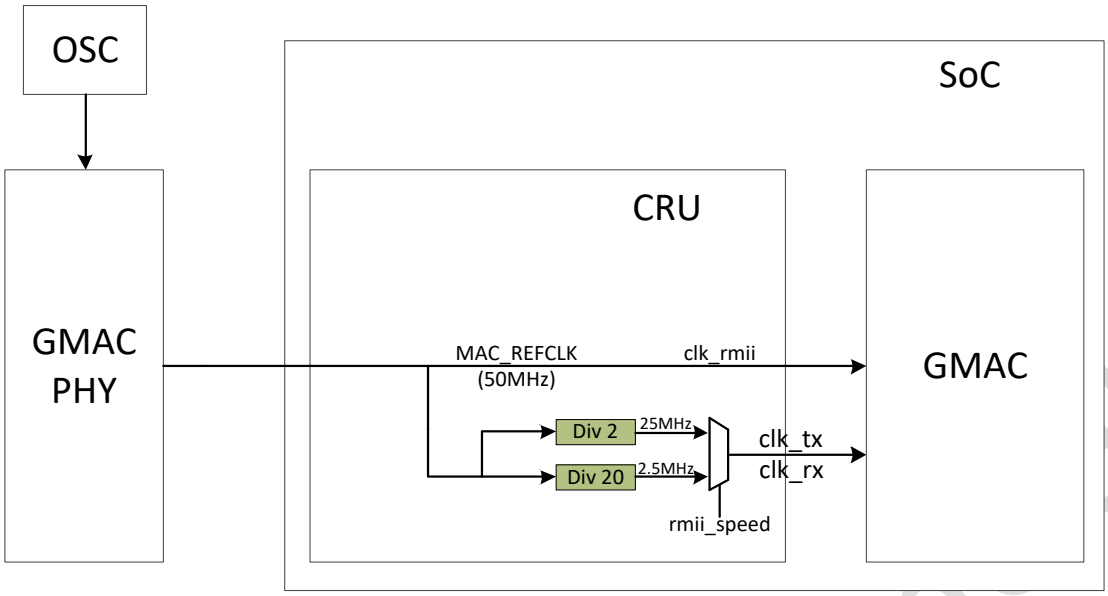

Fig. 9-14 RMII clock architecture when clock source from external OSC

9.6.6 Remote Wake-Up Frame Filter Register

The register wkupfmfilter_reg, address (028H), loads the Wake-up Frame Filter register. To load values in a Wake-up Frame Filter register, the entire register (wkupfmfilter_reg) must be written. The wkupfmfilter_reg register is loaded by sequentially loading the eight register values in address (028) for wkupfmfilter_reg0, wkupfmfilter_reg1, ..., wkupfmfilter_reg7, respectively. Wkupfmfilter_reg is read in the same way.

The internal counter to access the appropriate wkupfmfilter_reg is incremented when lane3 (or lane 0 in big-endian) is accessed by the CPU. This should be kept in mind if you are accessing these registers in byte or half-word mode.

wkupfmfilter_reg0	Filter 0 Byte Mask							
wkupfmfilter_reg1	Filter 1 Byte Mask							
wkupfmfilter_reg2	Filter 2 Byte Mask							
wkupfmfilter_reg3	Filter 3 Byte Mask							
wkupfmfilter_reg4	RSVD	Filter 3 Command	RSVD	Filter 2 Command	RSVD	Filter 1 Command	RSVD	Filter 0 Command
wkupfmfilter_reg5	Filter 3 Offset		Filter 2 Offset		Filter 1 Offset		Filter 0 Offset	
wkupfmfilter_reg6	Filter 1 CRC - 16				Filter 0 CRC - 16			
wkupfmfilter_reg7	Filter 3 CRC - 16				Filter 2 CRC - 16			

Fig. 9-15Wake-Up Frame Filter Register

Filter i Byte Mask

This register defines which bytes of the frame are examined by filter i (0, 1, 2, and 3) in order to determine whether or not the frame is a wake-up frame. The MSB (thirty-first bit) must be zero. Bit j [30:0] is the Byte Mask. If bit j (byte number) of the Byte Mask is set, then Filter i Offset + j of the incoming frame is processed by the CRC block; otherwise Filter i Offset + j is ignored.

Filter i Command

This 4-bit command controls the filter i operation. Bit 3 specifies the address type, defining the pattern's destination address type. When the bit is set, the pattern applies to only multicast frames; when the bit is reset, the pattern applies only to unicast frame. Bit 2 and Bit 1 are reserved. Bit 0 is the enable for filter i; if Bit 0 is not set, filter i is disabled.

Filter i Offset

This register defines the offset (within the frame) from which the frames are examined by filter i. This 8-bit pattern-offset is the offset for the filter i first byte to examined. The minimum allowed is 12, which refers to the 13th byte of the frame (offset value 0 refers to the first byte of the frame).

Filter i CRC-16

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This register contains the CRC_16 value calculated from the pattern, as well as the byte mask programmed to the wake-up filter register block.

9.6.7 System Consideration During Power-Down

MAC neither gates nor stops clocks when Power-Down mode is enabled. Power saving by clock gating must be done outside the core by the CRU. The receive data path must be clocked with clk_rx_i during Power-Down mode, because it is involved in magic packet/wake-on-LAN frame detection. However, the transmit path and the APB path clocks can be gated off during Power-Down mode.

The PMT interrupt is asserted when a valid wake-up frame is received. This interrupt is generated in the clk_rx domain.

The recommended power-down and wake-up sequence is as follows.

1. Disable the Transmit DMA (if applicable) and wait for any previous frame transmissions to complete. These transmissions can be detected when Transmit Interrupt (TI - Register MAC_STATUS[0]) is received.
2. Disable the MAC transmitter and MAC receiver by clearing the appropriate bits in the MAC Configuration register.
3. Wait until the Receive DMA empties all the frames from the Rx FIFO (a software timer may be required).
4. Enable Power-Down mode by appropriately configuring the PMT registers.
5. Enable the MAC Receiver and enter Power-Down mode.
6. Gate the APB and transmit clock inputs to the core (and other relevant clocks in the system) to reduce power and enter Sleep mode.
7. On receiving a valid wake-up frame, the MAC asserts the PMT interrupt signal and exits Power-Down mode.
8. On receiving the interrupt, the system must enable the APB and transmit clock inputs to the core.
9. Read the registerMAC_PMT_CTRL_STA to clear the interrupt, then enable the other modules in the system and resume normal operation.

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Chapter 10 Multiple Protocol PHY

10.1 Overview

The PHY subsystem contains one types of PHY. It is a combo of multiple protocol including the PCIe 2.0 and USB 3.0.

10.1.1 Combo PIPE PHY Overview

The Combo PIPE PHY supports physical layer of multiple protocol including USB3.0 Super Speed (5GT/s), PCIe Gen1/Gen2(2.5GT/s and 5GT/s).
The key features of the Combo PIPE PHY core include:

- Compatible with PCIe 2.0 and USB 3.0 base Specification
- Fully compatible with PIPE 4.2 interface specification
- Data rate configurable to 2.5G/5G for different application
- Support 16-bit or 32-bit parallel interface when encode/decode enabled
- Support 20-bit parallel interface when encode/decode bypassed
- Support flexible reference clock frequency
- Support 100MHz differential reference clock input or output (optional with SSC) in PCIe Mode
- Support Spread-Spectrum clock (SSC) generation and receiving from -5000ppm to 0ppm
- Support programmable transmit amplitude and De-emphasis
- Support TX detect RX function in PCIE and USB3.0 Mode
- Support Beacon signal generation and detection in PCIE Mode
- Support Low Frequency Periodic Signaling (LFPS) generation and detection in USB3.0 Mode
- Support L1 sub-state power management
- Support Loopback BERT and Multiple Pattern BIST Mode

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10.2 Block Diagram

10.2.1 Combo PIPE PHY Function Description

10.2.1.1 Block Diagram and Description

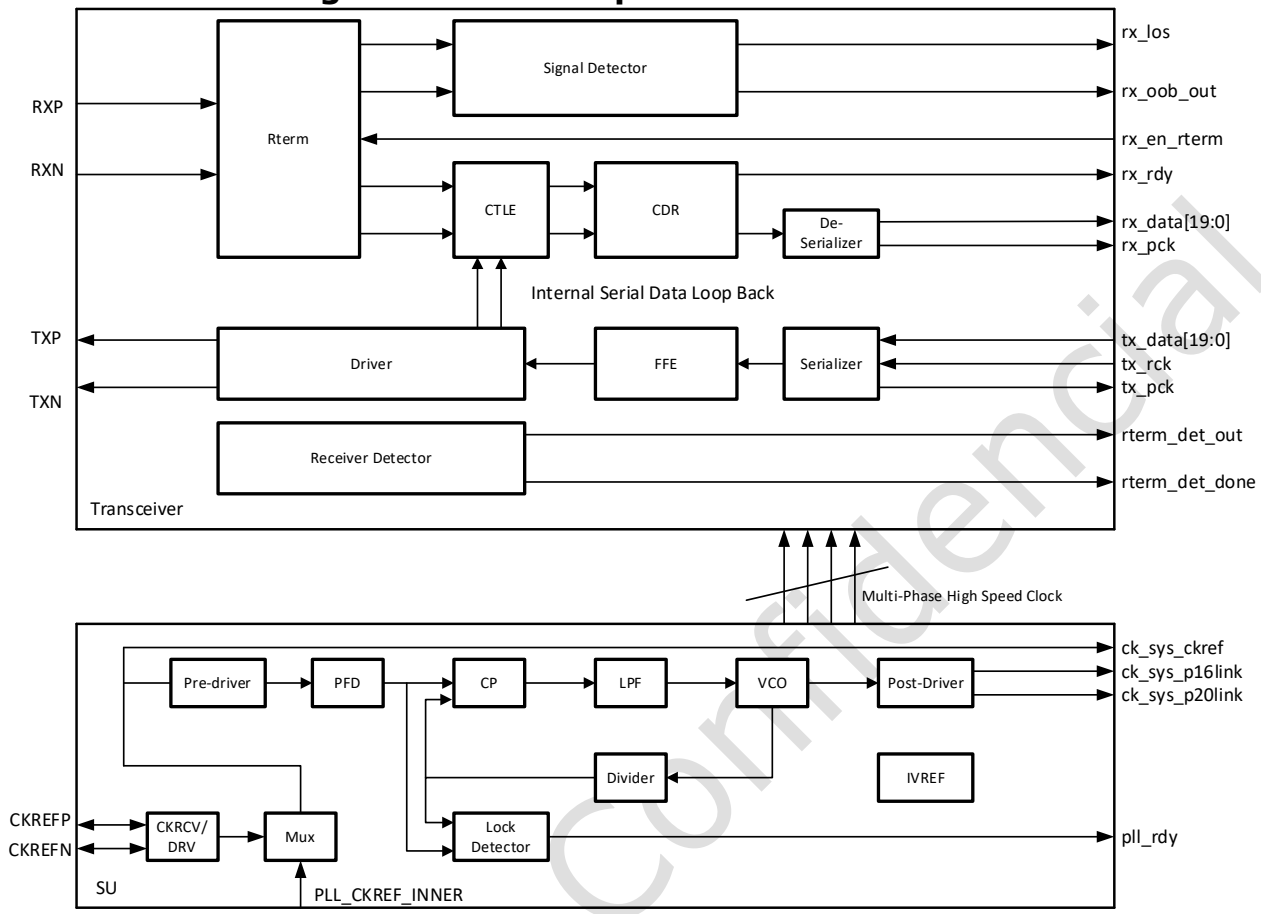

Fig. 10-1 PMA Block Diagram of Multi-PHY

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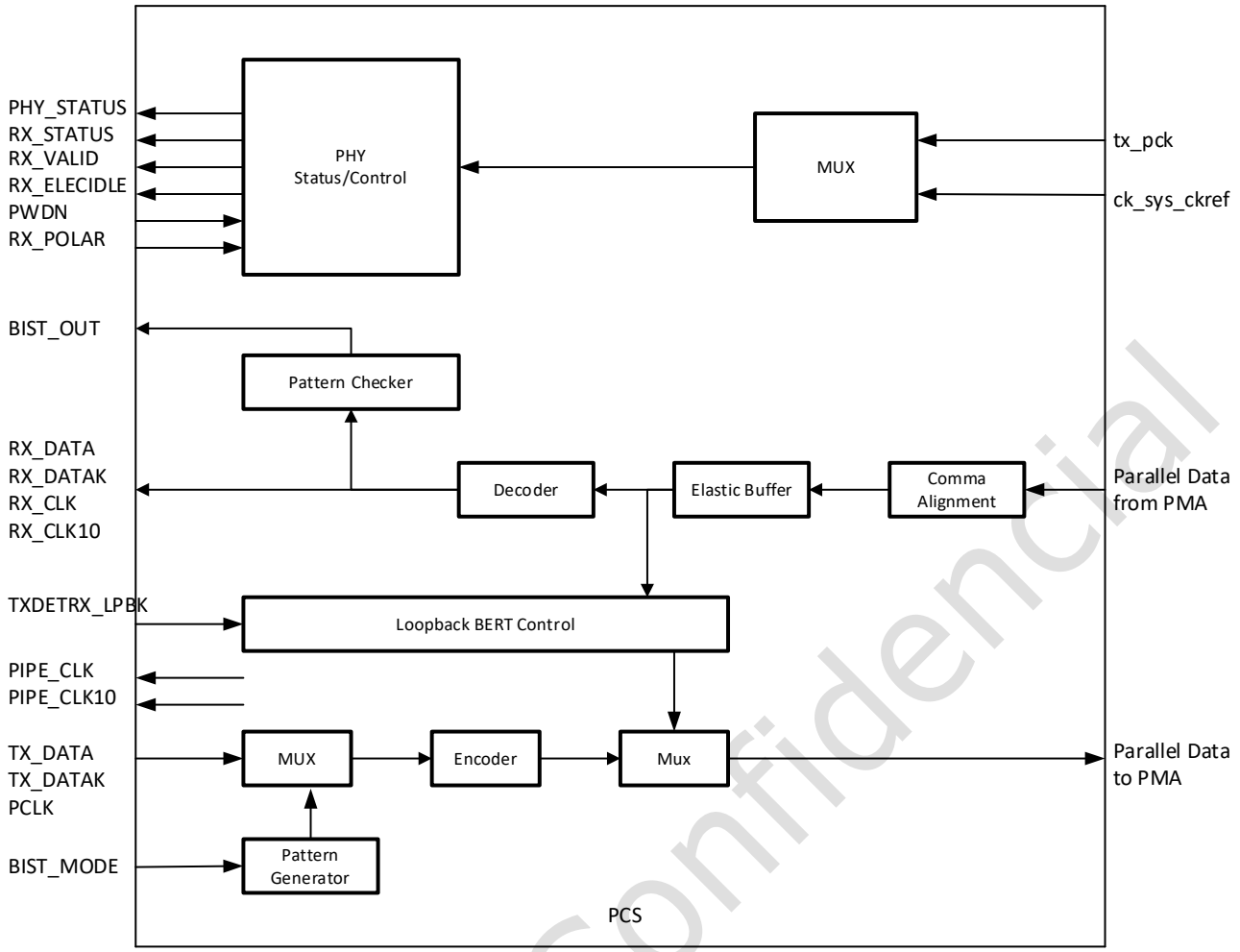

Fig. 10-2 PCS Block Diagram of Multi-PHY

Combo PIPE PHY includes two major blocks, PMA and PCS. PMA is an analog macro to perform serial to parallel and parallel to serial conversion. PMA includes three blocks, Transmitter, Receiver and SU(includes PLL, IVREF, etc.). PCS is a digital synthesis macro to perform PHY coding sub-layer function like 8bit/10bit code and decode, elastic buffer, comma alignment and BERT loopback, it also includes a register interface to access internal control registers with APB interface.

10.2.1.2 SHARED UNIT (SU)

PLL takes reference clock input from CKREFP/N and PLL_CKREF_INNER, to generate a high-speed clock for data transmission and clock data recovery. The high-speed clock generated by PLL could be SSC (spectrum spread clock) modulated if SSC mode is turned on. When SSC is enabled, the PHY is transmitting spread-spectrum serial data with frequency offset in 31.5KHz periodically.

IVREF includes a voltage and current reference generator, which comprises a Bandgap Reference and a Voltage Regulator. Reference voltage and current are generated for internal circuit usage. IVREF block is always on as long as IP power up, it will consume ~170uA static current all the time.

CKDRV is an input/output differential clock buffer, when it is used as input, it can receive a wide range differential reference clock. When used as output, CKDRV can drive a 100MHz differential clock for PCIE host application.

10.2.1.3 TRANSMITTER (TX)

The Serializer block converts parallel data from PHY PCS to high-speed serial data by using high speed clock generated by PLL. A feed forward equalizer (FFE) is implemented to compensate channel ISI.

Driver will convert the serial data to differential signal on TXP/TXM, also the driver will transmit Beacon Signal (PCIE2.0), OOB(SATA) or LFPS(USB3.0) signaling. The differential output amplitude and Deemphasis level can be programmed via setting PIPE3 control pins TX_SWING, TX_DEEMPH[2:0] and TX_MARGIN[2:0].

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The receiver detector will be used to detect the far-end receiver present or not.

10.2.1.4 RECEIVER (RX)

The CTLE (Continuous Time Linear Equalizer) is used to compensate channel loss and cancel ISI of the input signals by boosting high frequency gain. The CTLE can be set to adaptive mode or manual setting mode.
The CDR (Clock and Data Recover) tracks input data stream and generate recovered clock for data de-serializer. De-Serializer converts incoming serial bit stream recovered by CDR into a synchronized parallel data bus and forward it to PHY PCS block.

The Signal Detector detects OOB/LFPS on the RX input pair.

10.2.1.5 PCS

PCS module is a pure digital synthesis module, it works as an interface between PMA and MAC, it accomplishes functions including comma alignment, 8bit/10bit code/decode, elastic buffer, power control and IP testing. This module also includes an APB interface for accessing PHY control registers. PCS is fully compatible with the PIPE3 interface of "PHY interface for PCI express and USB3.0 architecture by intel".

10.3 Function Description

10.4 Register Description

10.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

10.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_000	0x0000	W	0x00000000	Combo PHY Register 0
COMBO_PIPE_PHY_REG_001	0x0004	W	0x00000080	Combo PHY Register 1
COMBO_PIPE_PHY_REG_002	0x0008	W	0x000000FF	Combo PHY Register 2
COMBO_PIPE_PHY_REG_003	0x000C	W	0x00000000	Combo PHY Register 3
COMBO_PIPE_PHY_REG_004	0x0010	W	0x00000000	Combo PHY Register 4
COMBO_PIPE_PHY_REG_005	0x0014	W	0x00000000	Combo PHY Register 5
COMBO_PIPE_PHY_REG_006	0x0018	W	0x00000088	Combo PHY Register 6
COMBO_PIPE_PHY_REG_007	0x001C	W	0x00000008	Combo PHY Register 7
COMBO_PIPE_PHY_REG_008	0x0020	W	0x000000E0	Combo PHY Register 8
COMBO_PIPE_PHY_REG_009	0x0024	W	0x00000029	Combo PHY Register 9
COMBO_PIPE_PHY_REG_010	0x0028	W	0x00000093	Combo PHY Register 10
COMBO_PIPE_PHY_REG_011	0x002C	W	0x00000002	Combo PHY Register 11
COMBO_PIPE_PHY_REG_012	0x0030	W	0x00000008	Combo PHY Register 12
COMBO_PIPE_PHY_REG_013	0x0034	W	0x00000059	Combo PHY Register 13
COMBO_PIPE_PHY_REG_014	0x0038	W	0x00000040	Combo PHY Register 14

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Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_015	0x003C	W	0x00000063	Combo PHY Register 15
COMBO_PIPE_PHY_REG_016	0x0040	W	0x00000000	Combo PHY Register 16
COMBO_PIPE_PHY_REG_017	0x0044	W	0x00000032	Combo PHY Register 17
COMBO_PIPE_PHY_REG_018	0x0048	W	0x0000001B	Combo PHY Register 18
COMBO_PIPE_PHY_REG_019	0x004C	W	0x00000007	Combo PHY Register 19
COMBO_PIPE_PHY_REG_020	0x0050	W	0x0000000B	Combo PHY Register 20
COMBO_PIPE_PHY_REG_021	0x0054	W	0x00000041	Combo PHY Register 21
COMBO_PIPE_PHY_REG_022	0x0058	W	0x0000002C	Combo PHY Register 22
COMBO_PIPE_PHY_REG_023	0x005C	W	0x00000030	Combo PHY Register 23
COMBO_PIPE_PHY_REG_024	0x0060	W	0x00000000	Combo PHY Register 24
COMBO_PIPE_PHY_REG_025	0x0064	W	0x00000000	Combo PHY Register 25
COMBO_PIPE_PHY_REG_026	0x0068	W	0x00000010	Combo PHY Register 26
COMBO_PIPE_PHY_REG_027	0x006C	W	0x00000000	Combo PHY Register 27
COMBO_PIPE_PHY_REG_028	0x0070	W	0x00000005	Combo PHY Register 28
COMBO_PIPE_PHY_REG_029	0x0074	W	0x00000000	Combo PHY Register 29
COMBO_PIPE_PHY_REG_030	0x0078	W	0x00000000	Combo PHY Register 30
COMBO_PIPE_PHY_REG_031	0x007C	W	0x00000010	Combo PHY Register 31
COMBO_PIPE_PHY_REG_032	0x0080	W	0x00000000	Combo PHY Register 32
COMBO_PIPE_PHY_REG_033	0x0084	W	0x00000000	Combo PHY Register 33
COMBO_PIPE_PHY_REG_034	0x0088	W	0x00000000	Combo PHY Register 34
COMBO_PIPE_PHY_REG_035	0x008C	W	0x00000000	Combo PHY Register 35
COMBO_PIPE_PHY_REG_036	0x0090	W	0x00000000	Combo PHY Register 36
COMBO_PIPE_PHY_REG_037	0x0094	W	0x00000000	Combo PHY Register 37
COMBO_PIPE_PHY_REG_038	0x0098	W	0x00000000	Combo PHY Register 38
COMBO_PIPE_PHY_REG_039	0x009C	W	0x00000000	Combo PHY Register 39
COMBO_PIPE_PHY_REG_040	0x00A0	W	0x00000000	Combo PHY Register 40
COMBO_PIPE_PHY_REG_041	0x00A4	W	0x00000000	Combo PHY Register 41

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Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_042	0x00A8	W	0x00000000	Combo PHY Register 42
COMBO_PIPE_PHY_REG_043	0x00AC	W	0x00000000	Combo PHY Register 43
COMBO_PIPE_PHY_REG_044	0x00B0	W	0x00000000	Combo PHY Register 44
COMBO_PIPE_PHY_REG_045	0x00B4	W	0x00000000	Combo PHY Register 45

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.4.3 Detail Registers Description

COMBO_PIPE_PHY_REG_000

Address: Operational Base(0xFF750000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	clk_out_sel Select which internal clock connect to output test_clk 1'b0: TXPLL clock/4 1'b1: RXCDR clock/4
6	RW	0x0	inv_txpll_clk 1'b1: Invert the PLL clock from PHY to PCS in PCS
5	RW	0x0	inv_rxcdr_clk 1'b1: Invert the CDR clock from PHY to PCS in PCS
4:0	RO	0x00	reserved

COMBO_PIPE_PHY_REG_001

Address: Operational Base(0xFF750000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x2	pwdn_ctrl_l [0]: If 1, PHY block power controlled by pwon** signals instead of PIPE signals [1]: Enable IVREF in PMA when pwdn_ctrl[0]=1
5:1	RO	0x00	reserved
0	RW	0x0	custom_specific Bypass elastic_buffer in sata mode

COMBO_PIPE_PHY_REG_002

Address: Operational Base(0xFF750000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0xff	pwdn_ctrl_h [2]: Enable PWON_TX_BUF to power on TX driver in PMA pwdn_ctrl[0]=1 [3]: Enable PWON_TXPLL to power on PLL in PMA pwdn_ctrl[0]=1 [4]: Enable PWON_IDLE_DET to power on PCIE EIDLE detect driver in PMA pwdn_ctrl[0]=1 [5]: Enable PWON_LFPS_DET to power on USB LFPS detect in PMA pwdn_ctr[0]=1 [6]: Enable PWON_RX_BUF to power on RX CTLE in PMA pwdn_ctrl[0]=1 [7]: Enable PWON_CDR to power on RX CDR in PMA pwdn_ctrl[0]=1 [8]: Enable PWON_OOB_DET to power on SATA OOB detect in PMA pwdn_ctr[0]=1 [9]: Enable PWON_HS_DET to power on SATA high speed data detect in PMA pwdn_ctrl[0]=1

COMBO_PIPE_PHY_REG_003

Address: Operational Base(0xFF750000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	rx_rterm_vcom RX vcom voltage select signal 2'b00: GND 2'b01, 2'b10: Floating 2'b11: 320mV
5:0	RO	0x00	reserved

COMBO_PIPE_PHY_REG_004

Address: Operational Base(0xFF750000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	reserved Reserved

COMBO_PIPE_PHY_REG_005

Address: Operational Base(0xFF750000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	pll_ckref_div PLL input clock divider, valid when su_trim[14]=1 2'b00: 1 2'b01: 1/2 2'b10: 1/3 2'b11: 1/4
5:0	RO	0x00	reserved

COMBO_PIPE_PHY_REG_006

Address: Operational Base(0xFF750000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x8	tx_rterm TX output resister adjust signal by step about 1ohm 4'h0: 60 4'h8: 50 4'hf: 44 Others: Reserved
3:0	RW	0x8	rx_rterm RX input resister adjust signal by step about 1ohm 4'h0: 60 4'h8: 50 4'hf: 43.5 Others: Reserved

COMBO_PIPE_PHY_REG_007

Address: Operational Base(0xFF750000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	byps_cdr_en 1'b0: CDR recovered clock will be operation while PLL is locked and CDR is operation, and rx_cdr_trim[7] only can be set to 1'b0 using reference clock for rx_rdy generation. 1'b1: CDR recovered clock will be operation while PLL is locked, and rx_cdr_trim[7] can be set to 1'b1 using recovered clock for rx_rdy generation.
6	RW	0x0	tx_swing Tx_swing control.
5	RW	0x0	near_end_lpk_enable PHY Near end loop back enable in BIST mode.
4	RW	0x0	ssc_en In U3 and SATA mode, this bit= 1, set SSC on. In PCIE mode, this bit=0 set SSC off.
3:0	RW	0x8	tx_swing_com TX boost level adjust signal 3'b000: Minimum 3'b111: Maximum

COMBO_PIPE_PHY_REG_008

Address: Operational Base(0xFF750000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	byps_cdr_fl_en 1'b0: rx_rdy is pulse signal to indicate CDR start to clock and data recovered from input serial data. 1'b1: rx_rdy is not controlled by PMA/PCS interface signal "cdr_fl_en".
6	RW	0x1	byps_cpath_limit 1'b0: CDR CPATH will be reset while CDR CPATH is overflow. 1'b1: CDR CPATH will be locked to MAX frequency offset while CDR CPATH is overflow.
5	RW	0x1	byps_capth_overflow 1'b0: CDR CPATH is controlled by CDR CPATH overflow. 1'b1: CDR CPATH is not controlled by CDR CPATH overflow.

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Bit	Attr	Reset Value	Description
4	RW	0x0	byps_fgain_adpt 1'b0: CDR CPATH gain is X2 while CDR recover frequency while rx_cdr_trim[6]=0. 1'b1: CDR CPATH gain is X1 while CDR recover frequency while rx_cdr_trim[6]=0.
3	RW	0x0	byps_pwon_rx_buf 1'b0: CTLE and LOS detector is controlled by PWDN[1:0]. 1'b1: CTLE and LOS detector is operation while reference clock and RX termination is present.
2	RW	0x0	byps_pown_rx_cdr 1'b0: CDR is controlled by PWDN[1:0]. 1'b1: CDR is operation after PLL is locked while reference clock and RX termination is present.
1	RW	0x0	byps_pwon_tx_buf 1'b0: TX Driver is controlled by PWDN[1:0]. 1'b1: TX Driver is operation after PLL is locked while reference clock is present, and TX detect RX is finished.
0	RW	0x0	byps_resetn 1'b0: PMA is reset by RSTN. 1'b1: PMA is not controlled by RSTN.

COMBO_PIPE_PHY_REG_009

Address: Operational Base(0xFF750000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	byps_rterm_en 1'b0: RX termination is controlled by RTERM_EN. 1'b1: RX termination is present all the way.
6	RW	0x0	byps_rx_cdr_idle 1'b0: CDR is reset if EIDLE is detected by LOS Detect module. 1'b1: CDR is not controlled by LOS Detect module.
5	RW	0x1	byps_rx_rdy_pulse 1'b0: rx_rdy is pulse signal. 1'b1: rx_rdy is step signal while byps_cdr_fl_en=1.
4	RW	0x0	byps_tx_eidle_en 1'b0: TX EIDLE is controlled by PMA/PCS interface signal "tx_eidle_en" (SATA Mode) or "tx_lfps_beacon_en"(PCIE/USB Mode). 1'b1: TX EIDLE is disable.
3:0	RW	0x9	ssc_ppm PLL SCC ppm adjust signal by step 500ppm. 4'h0: 0ppm 4'h1: 500ppm 4'h8: 4000ppm 4'hf: 7500ppm

COMBO_PIPE_PHY_REG_010

Address: Operational Base(0xFF750000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x93	su_trim_bank0 SU adjust signal [2:0]: PLL KVCO adjust, 000: min, 111:max [3]: PLL force lock [6:4]: PLL charge pump current adjust, 000: min, 111:max [10:7]: PLL LPF R1 adjust, 000: max, 111:min [11]: bypass pll power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 0: floating 1: GND [21:20]: CKRCV termination resister adjust 00: 100ohm 01: 200ohm 10: 1000ohm 11: Hi-Z [22]: CKRCV mode select 0: difference receiver mode 1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 00: 480 mV 01: 510 mV 10: 600 mV (default) 11: 660 mV [28:25]: CKDRV output swing adjust, 0000: 100 mV, 1111:860 mV, step: 50 mV [29]: CKDRV input clock select signal, 0: ck100m_pcie from PLL 1: ckref from CKRCV [31:30]: CKDRV output slew rate adjust, 00: fast, 11: slow

COMBO_PIPE_PHY_REG_011

Address: Operational Base(0xFF750000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	su_trim_bank1 SU adjust signal [2:0]: PLL KVCO adjust, 000: min, 111:max [3]: PLL force lock [6:4]: PLL charge pump current adjust, 000: min, 111:max [10:7]: PLL LPF R1 adjust, 000: max, 111:min [11]: bypass pll power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust

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Bit	Attr	Reset Value	Description
			0: floating 1: GND [21:20]: CKRCV termination resister adjust 00: 100ohm 01: 200ohm 10: 1000ohm 11: Hi-Z [22]: CKRCV mode select 0: difference receiver mode 1: signal receiver mode (CKREFP is valid,CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 00: 480 mV 01: 510 mV 10: 600 mV (default) 11: 660 mV [28:25]: CKDRV output swing adjust, 0000: 100 mV, 1111:860 mV, step: 50 mV [29]: CKDRV input clock select signal, 0: ck100m_pcie from PLL 1: ckref from CKRCV [31:30]: CKDRV output slew rate adjust, 00: fast, 11: slow

COMBO_PIPE_PHY_REG_012

Address: Operational Base(0xFF750000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	su_trim_bank2 SU adjust signal [2:0]: PLL KVCO adjust, 000: min, 111:max [3]: PLL force lock [6:4]: PLL charge pump current adjust, 000: min, 111:max [10:7]: PLL LPF R1 adjust, 000: max, 111:min [11]: bypass pll power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 0: floating 1: GND [21:20]: CKRCV termination resister adjust 00: 100ohm 01: 200ohm 10: 1000ohm 11: Hi-Z [22]: CKRCV mode select 0: difference receiver mode 1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 00: 480 mV 01: 510 mV 10: 600 mV (default) 11: 660 mV

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Bit	Attr	Reset Value	Description
			[28:25]: CKDRV output swing adjust, 0000: 100 mV, 1111:860 mV, step: 50 mV [29]: CKDRV input clock select signal, 0: ck100m_pcie from PLL 1: ckref from CKRCV [31:30]: CKDRV output slew rate adjust, 00: fast, 11: slow

COMBO_PIPE_PHY_REG_013

Address: Operational Base(0xFF750000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x59	su_trim_bank3 SU adjust signal [2:0]: PLL KVCO adjust, 000: min, 111:max [3]: PLL force lock [6:4]: PLL charge pump current adjust, 000: min, 111:max [10:7]: PLL LPF R1 adjust, 000: max, 111:min [11]: bypass pll power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 0: floating 1: GND [21:20]: CKRCV termination resister adjust 00: 100ohm 01: 200ohm 10: 1000ohm 11: Hi-Z [22]: CKRCV mode select 0: difference receiver mode 1: signal receiver mode (CKREFP is valid,CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 00: 480 mV 01: 510 mV 10: 600 mV (default) 11: 660 mV [28:25]: CKDRV output swing adjust, 0000: 100 mV, 1111:860 mV, step: 50 mV [29]: CKDRV input clock select signal, 0: ck100m_pcie from PLL 1: ckref from CKRCV [31:30]: CKDRV output slew rate adjust, 00: fast, 11: slow

COMBO_PIPE_PHY_REG_014

Address: Operational Base(0xFF750000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x1	ssc_cnt_l PLL control SSC module period When the pll_ckref_inner is 100MHz/25MHz, this signal should be set to its default value unless the user want to change the 31.5KHz SSC modulation frequency. When the pll_ckref_inner is 24MHz, this signal should be set to its default value unless the user want to change the 32.8KHz SSC modulation frequency.
5:2	RW	0x0	test_sel select the digital test signal. 4'h0: Input Reference Clock 4'h1: PLL Loopback Clock 4'h2: PLL Locked 4'h3: RX PCL enable 4'h4: RX CDR enable 4'h5: RX CTLE enable 4'h6: CDR overflow 4'h7: RX ready 4'h8: RX LFPS idle detect 4'h9: RX PCIE idle detect 4'ha: RX SATA idle detect 4'hb: RX super speed detect 4'hc: Iddq_en 4'hd: Rterm detect Others: Reserved
1	RW	0x0	rx_tseq USB Mode When asserted, it is used to instruct USB3.0 PHY to bypass normal operation and do a receiver equalization training. Please refer to PIPE3 interface and USB3.0 base spec for more detail information.
0	RW	0x0	en_adpt Adaptive Continuous Time Linear Equalizer (CTLE) enable signal 1'b0: Disable adaptive CTLE 1'b1: Enable adaptive CTLE

COMBO_PIPE_PHY_REG_015

Address: Operational Base(0xFF750000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x63	ssc_cnt_h PLL control SSC module period When the pll_ckref_inner is 100MHz/25MHz, This signals should be set to its default value(ssc_cnt[9:0]=0110001101 & 31.5KHz) unless the user want change the 31.5KHz SSC modulation frequency When the pll_ckref_inner is 24MHz, this signal should be set to its default value(ssc_cnt[9:0]=0101111101 & 31.5KHz) unless the user want change the 30.3KHz SSC modulation frequency.

COMBO_PIPE_PHY_REG_016

Address: Operational Base(0xFF750000) + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	pll_div_l PLL loop divider, valid when su_trim[14]=1, [14:10] is the integer number of divider factor, and [9:0] are the decimal fraction.

COMBO_PIPE_PHY_REG_017

Address: Operational Base(0xFF750000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	frez_apt_eq 1'b0: The adaptive equalizer will be always working when the adaptive equalizer function is enabled. 1'b1: The adaptive equalizer will freeze at its final result when equalizer training pattern transmission is done. This signal is used in USB3.1 mode, when equalizer training pattern transmission is done, IP user can stop adaptive equalization and freeze the result.
6:0	RW	0x32	pll_div_h PLL loop divider, valid when su_trim[14]=1, [14:10] is the integer number of divider factor, and [9:0] are the decimal fraction.

COMBO_PIPE_PHY_REG_018

Address: Operational Base(0xFF750000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x3	rx_afe_trim Receiver 2nd stage equalizer res control, used to adjust pole-zero of RX eq.
2:0	RW	0x3	rx_afe_ctrim Receiver 1st stage equalizer cap control, used to adjust pole-zero of RX EQ.

COMBO_PIPE_PHY_REG_019

Address: Operational Base(0xFF750000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	beacon_timeout_sel PCIe beacon timeout select
4	RW	0x0	rx_polar RX output polarity set 1'b0: No invert RX output data polarity 1'b1: Invert RX output data polarity
3:0	RW	0x7	rx_afe_rtrim Receiver 1st stage equalizer res control, used to adjust pole-zero of RX eq.

COMBO_PIPE_PHY_REG_020

Address: Operational Base(0xFF750000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x0b	rx_sqdet_trim_l RX squelch adjust [2:0]: squelch input filler bandwidth adjusts 3'b000: Max bandwidth 3'b111: Min bandwidth [4:3]: squelch delay adjusts 2'b00: Max delay 2'b11: Min delay [6:5]: amp bias adjusts 2'b00: Max ibias 2'b11: Min ibias [8:7]: squelch detect vth adjust 2'b00: Min vth 2'b11: Max vth

COMBO_PIPE_PHY_REG_021

Address: Operational Base(0xFF750000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	rx_adpt_eq_trim [2:0]: adaptive equalizer detection threshold control [3]: adaptive equalizer gain control
3:0	RW	0x1	rx_sqdet_trim_h [9]: bypass rx_superspeed 1'b1: rx_superspeed=1 [10]: rx_superspeed function selects 1'b0: ~los output 1'b1: ~los output | squelch output [11]: rx_pcie_idle function selects 1'b0: ~ squelch output 1'b1: los output

COMBO_PIPE_PHY_REG_022

Address: Operational Base(0xFF750000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	rx_adpt_eq_trim_h [6:4]: adaptive equalizer bandwidth control [8:7]: adaptive output refresh bandwidth control [9]: bypass the adaptive Cj function [10]: test mode selects [11]: Reserved

COMBO_PIPE_PHY_REG_023

Address: Operational Base(0xFF750000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x3	rx_cdr_trim_l [3]: CDR gain adjust 1'b0: 1/4([4]=1), 1/8([4]=0) 1'b1: 1/8 [2:0]: The slew rate control for PI 3'b000: Fast slew rate 3'b111: Slow slew rate

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	rx_los_trim RX los detect adjust [1:0]: Low vth adjust

COMBO_PIPE_PHY_REG_024

Address: Operational Base(0xFF750000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	rx_cdr_trim_h [4]: CDR gain adjust 1'b0: 1/8 1'b1: 1/4 when rx_cdr_trim[3]=1 [5]: CDR phase path gain adjust 1'b0: x1 1'b1: x2 [6]: CDR cpath bandwidth gain adjusts 1'b0: Low bandwidth 1'b1: High bandwidth [7]: rx_rdy counter clock select 1'b0: Ref clock 1'b1: CDR recovery clock [9:8]: rx_rdy delay time select 2'b00: 1.28us 2'b01: 0.64us 2'b10: 2.56us 2'b11: 5.12us [10]: rx_pck10 invert signal, 0: no inverted, 1: inverted [11]: adaptive CTLE control mode select signal, 0: auto control mode, 1, manual control mode, details show as ffollow: rx_cdr_trim[11] PHY_MODE[1:0] RATE[1:0] en_adpt Data Rate 1 XX XX Decided by register 0EH[0] 0 00 00 1 2.5Gbps 0 00 01 1 5.0Gbps 0 01 00 1 5.0Gbps 0 10 00 0 1.5Gbps 0 10 01 1 3.0Gbps 0 10 10 1 6.0Gbps

COMBO_PIPE_PHY_REG_025

Address: Operational Base(0xFF750000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	tx_trim_l TX adjust [3:0]: TX FFE adjust valid when tx_trim[4]=1 [4]: Manual mode enable [5]: Force rterm detect ready 1'b1: Force rtern_det_out=1 [6]: Force eidle 1'b1: txp/txm is eidle [7]: hi-z idle enable [8]: tx_pck invert enable [9]: MSB enable [10]: Bypass low resister eidle mode 1'b0: Eidle has not hi-z mode 1'b1: Eidle has hi-z mode [11]: Bypass 0.6kohm charge resister 1'b0: 0.6kohm resister 1'b1: 1kohm resister [13:12]: Rterm detect vth adjust 2'b00: Max vth 2'b11: Min vth [14]: Bypass signal of gate_tx_pck

COMBO_PIPE_PHY_REG_026

Address: Operational Base(0xFF750000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x10	tx_trim_h TX adjust [3:0]: TX FFE adjust valid when tx_trim[4]=1 [4]: Manual mode enable [5]: Force rterm detect ready 1'b1: Force rtern_det_out=1 [6]: Force eidle 1'b1: txp/txm is eidle [7]: hi-z idle enable [8]: tx_pck invert enable [9]: MSB enable [10]: Bypass low resister eidle mode 1'b0: Eidle has not hi-z mode 1'b1: Eidle has hi-z mode [11]: Bypass 0.6kohm charge resister 1'b0: 0.6kohm resister 1'b1: 1kohm resister [13:12]: Rterm detect vth adjust 2'b00: Max vth 2'b11: Min vth [14]: Bypass signal of gate_tx_pck

COMBO_PIPE_PHY_REG_027

Address: Operational Base(0xFF750000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	rx_trim [0]: rx_pck invert enable [1]: RX MSB enable

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COMBO_PIPE_PHY_REG_028

Address: Operational Base(0xFF750000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	tx_margin Tx margin control
4:0	RW	0x05	rterm_det_trim [1:0]: rterm detect pre-charge time adjust 2'b00: 512us 2'b11: 4096us [3:2]: rterm detect post-charge time adjust 2'b00: 8us 2'b11: 64us [4]: Reserved

COMBO_PIPE_PHY_REG_029

Address: Operational Base(0xFF750000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	tx_deemph Tx_deemph control

COMBO_PIPE_PHY_REG_030

Address: Operational Base(0xFF750000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	testo_sel pcs internal signal to testo io select

COMBO_PIPE_PHY_REG_031

Address: Operational Base(0xFF750000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x10	register_bank0 [0]: bypass the mode of pd_ck100m controlling CKDRV 0: CKDRV is on only in PCIE mode 1: CKDRV is controlled by ckref_src[1:0]; [1]: select signal of pll_lock to TX/RX 0: pll_lock is controlled by rate[1:0] 1: pll_lock is not controlled by rate[1:0] [2]: bypass the mode of rate[1:0] controlling pll_lock_pcs 0: pll_lock_pcs is controlled by rate[1:0] 1: pll_lock_pcs is not controlled by rate[1:0] [3]: 50ohm termination disable signal in CKREP/N TX mode, 0: not disable, 1: disable mode [5:4]: select signal of SSC derection: 00: upward spread spectrum; 01: downward spread spectrum, 10: no spread spectrum, 11: illegal [7:6]: SSC offset compensation. 00: 0ppm; 01: +500ppm; 10/11: -500ppm

COMBO_PIPE_PHY_REG_032

Address: Operational Base(0xFF750000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	register_bank1 [8]: pll_rdy delay control when rate change , 0: delay 3*TX_PCK relative to the falling edge of gate_tx_pck, 1: delay about 20us relative to the falling edge of gate_tx_pck; [9]: select pll_lock to TX/RX, 0: pll_lock_txrx is same to pll_lock_pcs, 1: pll_lock_txrx is not controled by gate_tx_pck [12:10]: PLL KVCO fine tuning signals [15:9]: Reserved

COMBO_PIPE_PHY_REG_033

Address: Operational Base(0xFF750000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	COMMA_DET Comma detect
5	RO	0x0	COMMA_RECEIVED Comma received
4	RO	0x0	CDR_DATA_VALID CDR data valid
3	RO	0x0	RX_SUPERSPEED RX super speed
2	RO	0x0	DET_FINISH_PUSE Detection finish
1	RO	0x0	SKP_REMOVED SKP removed
0	RO	0x0	SKP_INSERTED SKP inserted

COMBO_PIPE_PHY_REG_034

Address: Operational Base(0xFF750000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	EB_OF Ebuffer overflow
6	RO	0x0	EB_UF Ebuffer underflow
5:4	RO	0x0	DISPARITY_ERR Dsiparity error
3:2	RO	0x0	INVALID_CODE Invalid code
1:0	RO	0x0	BRST_SYM BRST_SYM

COMBO_PIPE_PHY_REG_035

Address: Operational Base(0xFF750000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	NO_ERR NO_ERR
6	RO	0x0	BIST_RESULT BIST result

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Bit	Attr	Reset Value	Description
5	RO	0x0	TEST_DONE Test done
4	RO	0x0	RX_ELECIDLE_O RX electrical idle
3	RO	0x0	BIST_DONE BIST done
2	RO	0x0	BIST_TIMEOUT BIST timeout
1	RO	0x0	DET_FINSH Detect finish
0	RO	0x0	DET_RESULT Detect result

COMBO_PIPE_PHY_REG_036

Address: Operational Base(0xFF750000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	ERR_CNT Error count

COMBO_PIPE_PHY_REG_037

Address: Operational Base(0xFF750000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RO	0x00	MAX_JITTER Max jitter
1	RO	0x0	CDR_FL_EN CDR_FL_EN
0	RO	0x0	CDR_FREQ_LK CDR frequency lock

COMBO_PIPE_PHY_REG_038

Address: Operational Base(0xFF750000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	USB3_MODE USB3_MODE
5	RO	0x0	SATA_MODE SATA_MODE
4	RO	0x0	PCIE_MODE PCIE_MODE
3	RO	0x0	BEACON_LFPS BEACON_LFPS
2	RO	0x0	TX_DET_RX_0 TX_DET_RX_0
1	RO	0x0	GAT_PLL_CLK GAT_PLL_CLK
0	RO	0x0	SS_MODULE SS_MODULE

COMBO_PIPE_PHY_REG_039

Address: Operational Base(0xFF750000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RO	0x0	RATE_1_O RATE_1_O
6	RO	0x0	RATE_0_O RATE_0_O
5	RO	0x0	RATE_TX_1 RATE_TX_1
4	RO	0x0	RATE_TX_0 RATE_TX_0
3	RO	0x0	RATE_RX_1 RATE_RX_1
2	RO	0x0	RATE_RX_0 RATE_RX_0
1	RO	0x0	PWON_PLL_O PWON_PLL_O
0	RO	0x0	TXPLL_LOCK TX PLL lock

COMBO_PIPE_PHY_REG_040

Address: Operational Base(0xFF750000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	PWON_IREF PWON_IREF
6	RO	0x0	PWON_LFPS_DET PWON_LFPS_DET
5	RO	0x0	PWON_IDLE_DET PWON_IDLE_DET
4	RO	0x0	PWON_OOB_DET PWON_OOB_DET
3	RO	0x0	PWON_HS_DET PWON_HS_DET
2	RO	0x0	PWON_RX_BUS PWON_TX_BUF
1	RO	0x0	PWON_TX_BUF PWON_TX_BUF
0	RO	0x0	PWON_CDR_O PWON_CDR_O

COMBO_PIPE_PHY_REG_041

Address: Operational Base(0xFF750000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	RX_DETECEED RX_DETECEED
5	RO	0x0	RX_LFPS_I RX_LFPS_I
4	RO	0x0	RX_SUPERSPEED RX_SUPERSPEED
3	RO	0x0	RX_SATA_IDLE RX_SATA_IDLE
2	RO	0x0	RX_PCIE_IDLE RX_PCIE_IDLE
1	RO	0x0	RX_ELECIDLE RX_ELECIDLE

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Bit	Attr	Reset Value	Description
0	RO	0x0	RX_VALID RX_VALID

COMBO_PIPE_PHY_REG_042

Address: Operational Base(0xFF750000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RO	0x0	REFCK_DET_OUT REFCK_DET_OUT
5	RO	0x0	RTERM_DET_OUT RTERM_DET_OUT
4	RO	0x0	RX_ADPE_EQ_FL RX_ADPE_EQ_FL
3:0	RO	0x0	RX_ADPT_EQ_TRIM RX_ADPT_EQ_TRIM

COMBO_PIPE_PHY_REG_043

Address: Operational Base(0xFF750000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RO	0x0	BERC_SYM BERC_SYM
4	RO	0x0	LP_RX_EN LP_RX_EN
3	RO	0x0	LP_SLAVE_EN LP_SLAVE_EN
2:0	RO	0x0	RX_ADPT_EQ_CTRIM RX_ADPT_EQ_CTRIM

COMBO_PIPE_PHY_REG_044

Address: Operational Base(0xFF750000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	RX_DEBUG_R RX_DEBUG_R

COMBO_PIPE_PHY_REG_045

Address: Operational Base(0xFF750000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	UNUSED_DEBUG RX_DEBUG_R

10.5 Interface Description

Table 10-1 Combo PIPE PHY Analog IO Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
AVDH	I/O	MULTI_PHY_AVDD_1V8	N/A
AVDL	I/O	MULTI_PHY_AVDD_0V9	N/A
CKREFN	I/O	PCIE20_REFCLKN	N/A
CKREFP	I/O	PCIE20_REFCLKP	N/A
RXN	I	USB30_OTG0_SSRXN/PCIE20_RXDN	N/A

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Module Pin	Dir	Pin Name	IOMUX Setting
RXP	I	USB30_OTG0_SSRXP/PCIE20_RXDP	N/A
TXN	O	USB30_OTG0_SSTXN/PCIE20_TXDN	N/A
TXP	O	USB30_OTG0_SSTXP/PCIE20_TXDP	N/A

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

10.6 Application Notes

10.6.1 Combo PHY Application Note

10.6.1.1 Operation Mode Support

The following mode are supported for IP operation, IP configuration other than this list are not supported

Table 10-2 PHY operation mode

PHY_MODE	RATE	BUS_WIDTH	PHY Operation Mode
00	00	00	PCIe Gen1, 32bit, PCLK=62.5M
		01	N/A
	01	00	PCIe Gen2, 32bit, PCLK=125M
		01	N/A
01	00	00	USB3.0, 32bit, PCLK=125M
01	00	01	N/A

- PHY_MODE is configured by PIPE_PHY_GRF_PIPE_CON0.pipe_phymode
- RATE is controlled by protocol controller or can be configured PIPE_PHY_GRF_PIPE_CON0.pipe_rate when override is enabled
- BUS_WIDTH is controlled by protocol controller or can be configured PIPE_PHY_GRF_PIPE_CON0.pipe_databuswidth when override is enabled

10.6.1.2 Power Down Mode

Power down control signals to individual analog modules are generated based on PWDN[1:0] setting from PIPE inputs as shown in below table. An override function is provided for debug purpose, see Multi-PHY register list. (√ – active; ×– power down)

Table 10-3 PCIE power down mode

PWDN[3:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
0000	--	√	√	√	√
0001	0(illegal)	√	√	√	√
	1	×	√	√	√
0010	0(illegal)	√	×	×	√
	1	×	×	×	√
0011	0	√	×	×	×
	1	×	×	×	×
1---	0(illegal)	√	×	×	×
	1	×	×	×	×

In PCIe mode, power for IVREF and PCIe idle detector are always on, while power for LFPS, 1.5G SATA idle and 3G/6G SATA idle detectors are always off, and power of Rx buffer is off when RX_STANDBY is high.

Note: If TX_ELECIDLE(pipe_txelecidle) and TX_COMPLIANCE(pipe_txcompliance) is both asserted, all powers are off.

Table 10-4 USB3 power down mode

PWDN[3:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
0000	--	√	√	√	√
0001	0	√	√	×	√
	1	√	√	×	√
0010	0	√	√	×	√
	1	√	√	×	√
0011	0	√	√	×	×

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PWDN[3:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
	1	×	√	×	×

In USB3.0 mode, power for IVREF and LFPS detector are always on, while power for PCIe idle, 1.5G SATA idle and 3G/6G SATA idle detectors are always off, and power of LFPS detector and power of Rx buffer are turned off if termination is not on.

10.6.1.3 Reference Clock

Combo PIPE PHY's reference clock source can be selected from either PLL_CKREF_INNER or PCIE20_REFCLKN/P, according to the status CKREF_SRC[1:0] after the PHY de-asserted reset.

The differential pair PCIE20_REFCLKN/P can be configured as either reference clock input or reference clock output, according to CKREF_SRC[1].

Configure the register signal su_trim[29] to select reference clock(ckref) or 100MHz clock (ck100m_pcie) from PLL to drive to PCIE20_REFCLKN/P.

The CKREF_SRC is controlled by PIPE_PHY_GRF_PIPE_CON3.phy_clk_ref_src, and the PIPE_PHY_GRF_PIPE_CON3.phy_clk_sel is used to set the frequency of the selected reference clock.

The PLL_CKREF_INNER is derived by SoC internal CRU, refers to CRU for detail configurations to generate the appropriate reference clock.

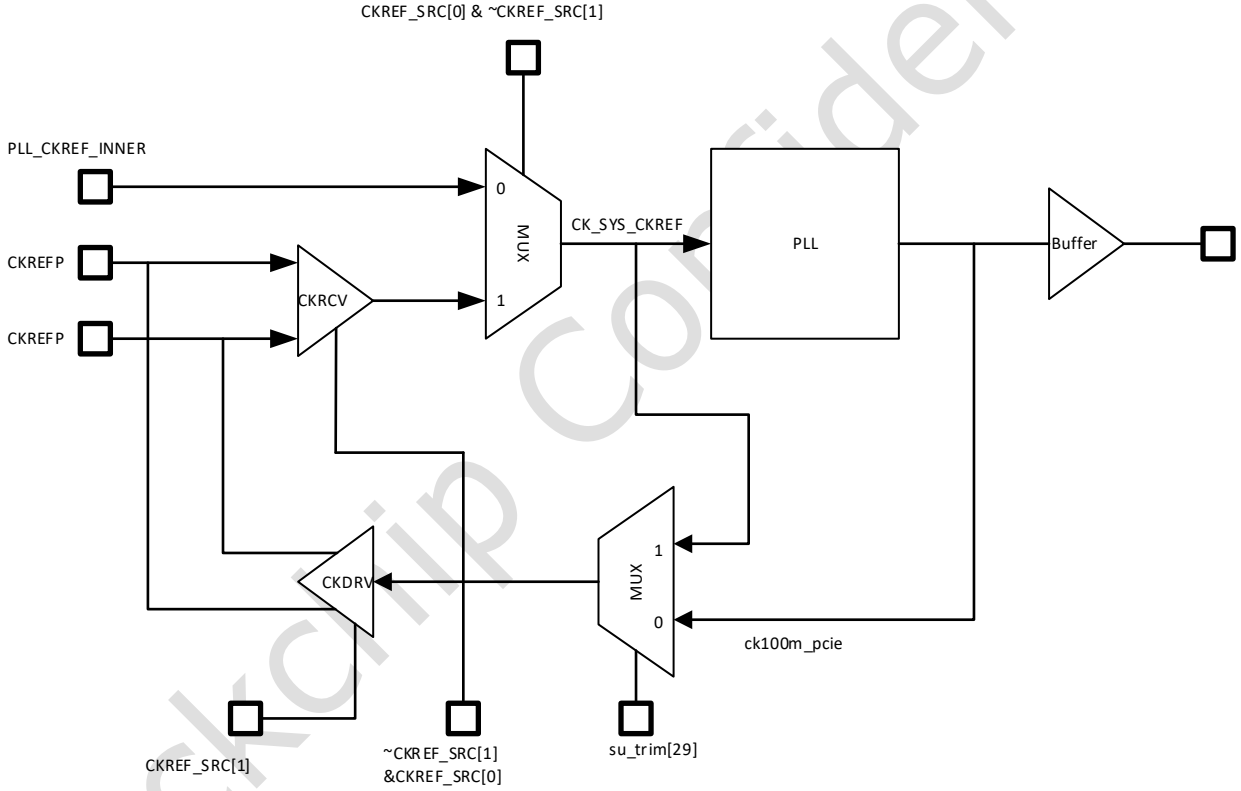

Fig. 10-3 Reference Clock Structure of Combo PIPE PHY

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Chapter 11 Pulse Density Modulation Interface Controller

11.1 Overview

The PDM interface controller and decoder support mono PDM format. It integrates a clock generator driving the PDM microphone and embeds filters which decimate the incoming bit stream to obtain most common audio rates.
PDM supports the following features:

- Support one internal 32-bit wide and 128-location deep FIFOs for receiving audio data
- Support receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of receive FIFO full interrupt
- Support combined interrupt output
- Support AHB bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support PDM master receive mode
- Support 4 paths. Each path is composed of two digital microphone channels. It can be used with four stereo or eight mono microphones. Each path is enabled or disabled independently
- Support 16~24 bit sample resolution
- Support sample rate: 8kHz,16kHz,32kHz,64kHz,128kHz,11.025kHz,22.05kHz,44.1kHz,88.2kHz,176.4kHz,12kHz,24kHz,48kHz,96kHz,192kHz
- Support two 16-bit audio data store together in one 32-bit wide location
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support programmable left and right channel exchange
- Support mono-path output
- Support delete dummy data at the beginning of every channel
- Support CIC output shift right or left 2/4/6/8 bit

11.2 Block Diagram

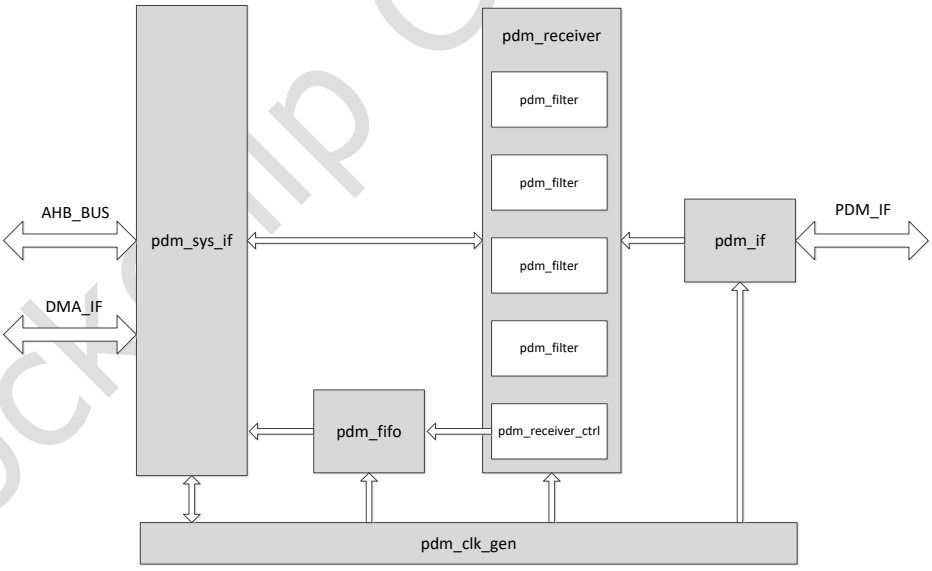

Fig.11-1 PDM Block Diagram

System Interface
The system interface implements the APB slave operation. It contains not only control registers of receiver inside but also interrupt and DMA handshaking interface.
Clock Generator
The Clock Generator implements clock generation function. The input source clock to the module is MCLK, and by the divider of the module, the clock generator generates CLK_PDM to receiver.
Receiver
The receiver can act as a decimation filter of PDM. And export PCM format data.
Receive FIFO

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The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 128.

11.3 Function Description

11.3.1 AHB Interface

There is an AHB slave interface in PDM. It is responsible for accessing registers.

11.3.2 PDM Interface

The PDM interface is a 5-wire interface. The PDM module can support up to four external stereo and eight digital microphones.

Following shows two cases of usage of the PDM, but all configurations are possible with stereo and mono digital microphones.

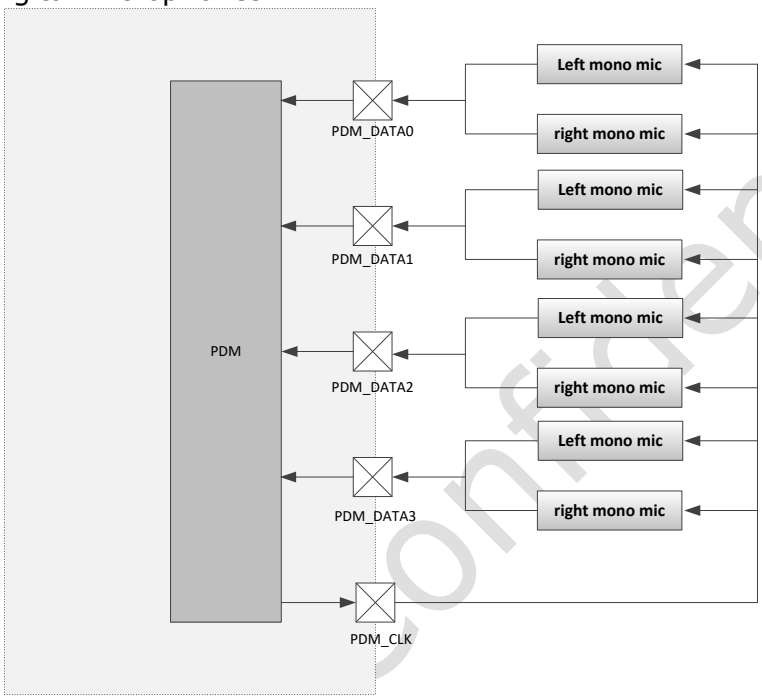

Fig.11-2 PDM with Eight Mono MIC

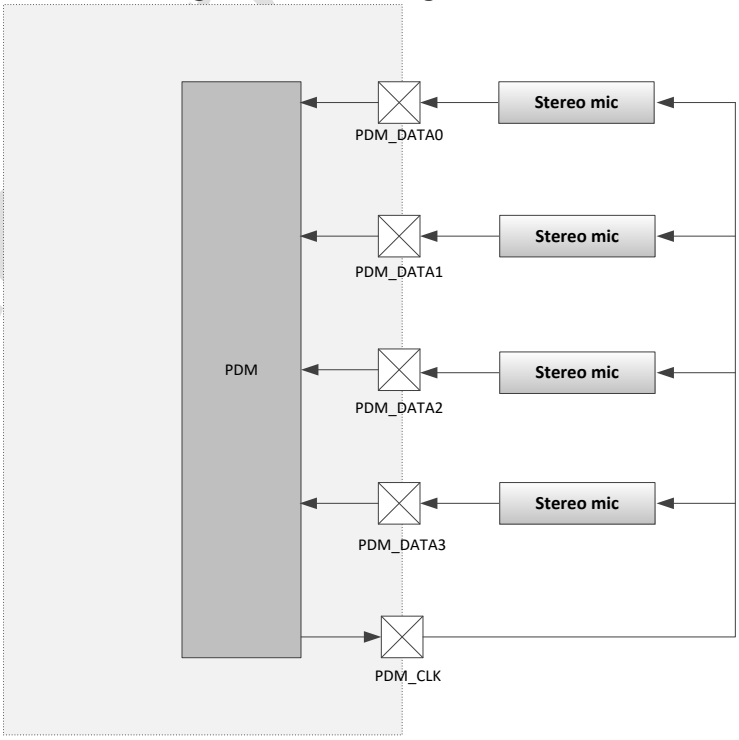

Fig.11-3 PDM with Four Stereo MIC

The PDM interface consists of a serial-data shift clock output (PDM_CLK) and a serial data input (PDM_DATA). The clock is fanned out to both digital MICs, and both digital MICs'

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data(left channel and right channel) outputs share a single signal line. To share a single line, the digital MICs tri-state their output during one phase of the clock(high or low part of cycle, depending on how they are configured via their L/R input).

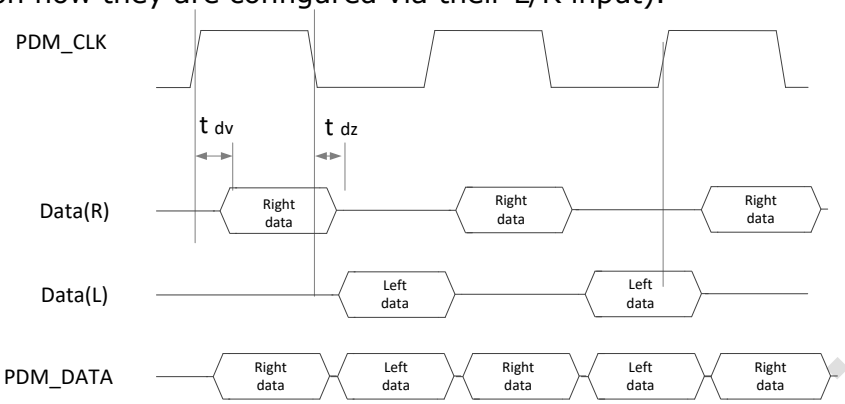

Fig.11-4 PDM interface diagram with external MIC

11.3.3 Digital Filter

The external PDM MIC generates a PDM stream of bits and transfers it in one period or one half-period of the clock provided by the PDM. The aim of the PDM is to process data from the PDM interface, decimate and filter the data, and store the processed data in the FIFO. The four paths are identical. Each path is composed of a left and a right channel. The PDM interface delivers eight parallel data of 1bit. Each bit goes to a filter. The aim of the filter is to limit the noise and export PCM format audio data.

11.3.4 Frequency Configuration

MCLK is the source clock signal. PDM_CLK is the output clocks generated in the PDM and is fed to the external microphones. They are also the internal clock of the external microphones. User must take care about the frequency of PDM_CLK when selecting the source clock (MCLK).

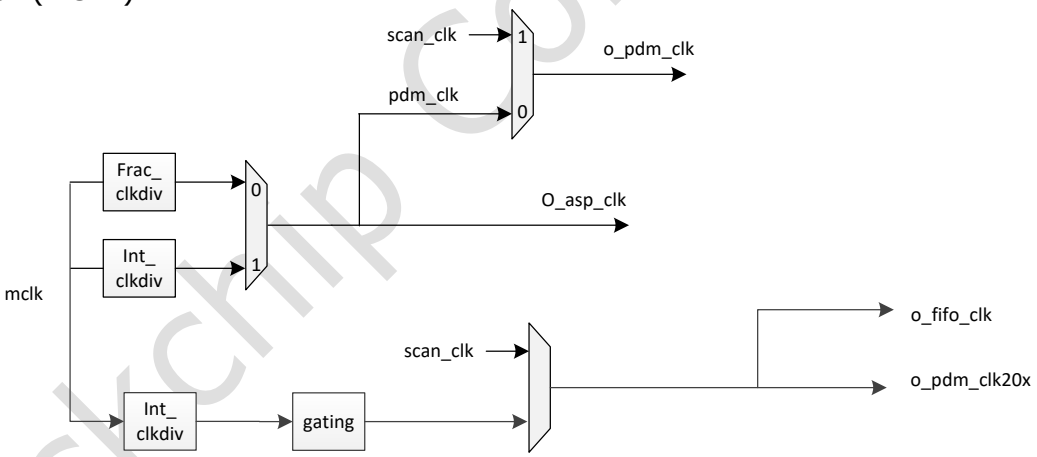

Fig.11-5 PDM Clock Structure

Table 11-1 Relation between PDM_CLK and Sample Rate

PDM_CLK	Sample Rate
3.072MHz	12kHz,24kHz,48kHz,96kHz,192kHz
2.8224MHz	11.025kHz,22.05kHz,44.1kHz,88.2kHz,176.4kHz
2.048MHz	8kHz,16kHz,32kHz,64kHz,128kHz

11.4 Register Description

11.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

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11.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PDM_SYSCONFIG	0x0000	W	0x00000000	PDM System Configure Register
PDM_CTRL0	0x0004	W	0x78000377	PDM Control Register 0
PDM_CTRL1	0x0008	W	0x0BB8EA60	PDM Control Register 1
PDM_CLK_CTRL	0x000C	W	0x0000E401	PDM Clock Control Register
PDM_HPF_CTRL	0x0010	W	0x00000000	PDM High-pass Filter Control Register
PDM_FIFO_CTRL	0x0014	W	0x00000000	PDM FIFO Control Register
PDM_DMA_CTRL	0x0018	W	0x0000001F	PDM DMA Control Register
PDM_INT_EN	0x001C	W	0x00000000	PDM Interrupt Enable Register
PDM_INT_CLR	0x0020	W	0x00000000	PDM Interrupt Clear Register
PDM_INT_ST	0x0024	W	0x00000000	PDM Interrupt Status Register
PDM_RXFIFO_DATA_REG	0x0030	W	0x00000000	PDM Receive FIFO Data Register
PDM_DATA0R_REG	0x0034	W	0x00000000	PDM Path0 Right Channel Data Register
PDM_DATA0L_REG	0x0038	W	0x00000000	PDM Path0 Left Channel Data Register
PDM_DATA1R_REG	0x003C	W	0x00000000	PDM Path1 Right Channel Data Register
PDM_DATA1L_REG	0x0040	W	0x00000000	PDM Path1 Left Channel Data Register
PDM_DATA2R_REG	0x0044	W	0x00000000	PDM Path2 Right Channel Data Register
PDM_DATA2L_REG	0x0048	W	0x00000000	PDM Path2 Left Channel Data Register
PDM_DATA3R_REG	0x004C	W	0x00000000	PDM Path3 Right Channel Data Register
PDM_DATA3L_REG	0x0050	W	0x00000000	PDM Path3 Left Channel Data Register
PDM_DATA_VALID	0x0054	W	0x00000000	PDM Path Data Valid Register
PDM_VERSION	0x0058	W	0x59313031	PDM Version Register
PDM_RDN_DEL_CTRL	0x005C	W	0x00000000	RDN Delete ctrl
PDM_MONO_PATH_CTRL	0x0060	W	0x00000000	Mono path ctrl
PDM_SHIFT_CTRL	0x0064	W	0x00000000	shift ctrl
PDM_INCR_RXDR	0x0400	W	0x00000000	Increment Address Receive FIFO Data Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3 Detail Registers Description

PDM_SYSCONFIG

Address: Operational Base(0xFF830000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	rx_start RX transfer start bit 1'b0: Stop RX transfer 1'b1: Start RX transfer
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	rx_clr PDM RX logic clear This is a self-cleared bit. High active. Write 1'b1: Clear RX logic Write 1'b0: No action Read 1'b1: Clear ongoing Read 1'b0: Clear done

PDM_CTRL0

Address: Operational Base(0xFF830000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	sjm_sel Store justified mode Can be written only when SYSCONFIG[2] is 0. 16bit~31bit DATA stored in 32 bits width FIFO. If VDW select 16bit data, this bit is valid only when HWT select 1. Because if HWT is 0, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 1'b0: Right justified 1'b1: Left justified
30	RW	0x1	path3_en Path 3 enable 1'b1: Enable 1'b0: Disable
29	RW	0x1	path2_en Path 2 enable 1'b1: Enable 1'b0: Disable
28	RW	0x1	path1_en Path 1 enable 1'b1: Enable 1'b0: Disable
27	RW	0x1	path0_en Path 0 enable 1'b1: Enable 1'b0: Disable
26	RW	0x0	hwt_en Halfword word transform Only valid when VDW select 16bit data. 1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid
25	RW	0x0	filter_gate_en Filter gate enable If some filters not work, the filter and its corresponding memory clock will be gated if filter_gate_en is 1'b1, otherwise the clock will be still active.
24	RW	0x0	sig_scale_mode Signal scale mode select 1'b0: CIC outputs the normal latitude. 1'b1: Scale the CIC outputs to half of the normal latitude and scale 2 times after hpf-filter.
23:16	RW	0x00	int_div_20x_con Integer divider for PDM filter operation.

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Bit	Attr	Reset Value	Description
15:8	RW	0x03	int_div_con Integer divider Can be written only when SYSCONFIG[2] is 0.
7:5	RW	0x3	sample_rate_sel Selects which kind of sample rate. 3'b000: 12kHz/11.024kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 32kHz 3'b011: 48kHz/44.1kHz 3'b100: 96kHz/88.2kHz/64kHz 3'b101~3'b111: 192kHz/176.4kHz/128kHz
4:0	RW	0x17	data_vld_width Can be written only when SYSCONFIG[2] is 0. Valid Data width 0~14: Reserved 15: 16bit 16: 17bit 17: 18bit 18: 19bit ..... n: (n+1)bit 23: 24bit

PDM_CTRL1

Address: Operational Base(0xFF830000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0bb8	frac_div_numerator Fraction divider numerator Can be written only when SYSCONFIG[2] is 0.
15:0	RW	0xea60	frac_div_denomonator Fraction divider denominator Can be written only when SYSCONFIG[2] is 0.

PDM_CLK_CTRL

Address: Operational Base(0xFF830000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x3	rx_path_select3 RX Path Select 2'b00: Path3 data from PDM data0 2'b01: Path3 data from PDM data1 2'b10: Path3 data from PDM data2 2'b11: Path3 data from PDM data3
13:12	RW	0x2	rx_path_select2 RX Path Select 2'b00: Path2 data from PDM data0 2'b01: Path2 data from PDM data1 2'b10: Path2 data from PDM data2 2'b11: Path2 data from PDM data3
11:10	RW	0x1	rx_path_select1 RX Path Select 2'b00: Path1 data from PDM data0 2'b01: Path1 data from PDM data1 2'b10: Path1 data from PDM data2 2'b11: Path1 data from PDM data3

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	rx_path_select0 RX Path Select 2'b00: Path0 data from PDM data0 2'b01: Path0 data from PDM data1 2'b10: Path0 data from PDM data2 2'b11: Path0 data from PDM data3
7:6	RO	0x0	reserved
5	RW	0x0	pdm_clk_en PDM clk enable, working at PDM mode. Can be written only when SYSCONFIG[2] is 0. 1'b0: PDM clk disable 1'b1: PDM clk enable
4	RW	0x0	div_type_sel Divider type select signal Can be written only when SYSCONFIG[2] is 0. 1'b0: Fraction divider 1'b1: Integer divider
3	RW	0x0	lr_ch_ex Left and right channel data exchange 1'b0: Not inverted, if mono_path_en, the output path is the Left path. 1'b1: Inverted, if mono_path_en, the output path is the Right path.
2	RW	0x0	fir_com_bps Fir compensate filter bypass 1'b0: Not bypass 1'b1: Bypass
1:0	RW	0x1	cic_ds_ratio CIC filter decimation ratio 2'b00: 16 times decimation 2'b01: 8 times decimation 2'b10: 4 times decimation other: 8 times decimation

PDM_HPF_CTRL

Address: Operational Base(0xFF830000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	hpfle High-pass filter enable for left channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
2	RW	0x0	hpfre High-pass filter enable for right channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
1:0	RW	0x0	hpf_cf High-pass filter configure 2'b00: 3.79Hz 2'b01: 60Hz 2'b10: 243Hz 2'b11: 493Hz

PDM_FIFO_CTRL

Address: Operational Base(0xFF830000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x00	rft Receive FIFO threshold When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO threshold interrupt is triggered.
7:0	RO	0x00	rfl Receive FIFO level Contains the number of valid data entries in the receive FIFO.

PDM_DMA_CTRL

Address: Operational Base(0xFF830000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rde Receive DMA enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
7	RO	0x0	reserved
6:0	RW	0x1f	rdl Receive data level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.

PDM_INT_EN

Address: Operational Base(0xFF830000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxoie RX overflow interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	rxftie RX full threshold interrupt enable 1'b0: Disable 1'b1: Enable

PDM_INT_CLR

Address: Operational Base(0xFF830000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxoic RX overflow interrupt clear (high active, auto clear).
0	RO	0x0	reserved

PDM_INT_ST

Address: Operational Base(0xFF830000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	rxoi RX overflow interrupt 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
0	RO	0x0	rxfi RX full interrupt 1'b0: Inactive 1'b1: Active

PDM_RXFIFO_DATA_REG

Address: Operational Base(0xFF830000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdr Receive FIFO shadow register When the register is read, data in the receive FIFO is accessed.

PDM_DATA0R_REG

Address: Operational Base(0xFF830000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0r Data of the path 0 right channel

PDM_DATA0L_REG

Address: Operational Base(0xFF830000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0l Data of the path 0 left channel

PDM_DATA1R_REG

Address: Operational Base(0xFF830000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1r Data of the path 1 right channel

PDM_DATA1L_REG

Address: Operational Base(0xFF830000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1l Data of the path 1 left channel

PDM_DATA2R_REG

Address: Operational Base(0xFF830000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2r Data of the path 2 right channel

PDM_DATA2L_REG

Address: Operational Base(0xFF830000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2l Data of the path 2 left channel

PDM_DATA3R_REG

Address: Operational Base(0xFF830000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3r Data of the path 3 right channel

PDM_DATA3L_REG

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Address: Operational Base(0xFF830000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3l Data of the path 3 left channel

PDM_DATA_VALID

Address: Operational Base(0xFF830000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RC	0x0	path0_vld 1'b0: DATA0R_REG, DATA0L_REG value is invalid. 1'b1: DATA0R_REG, DATA0L_REG value is valid.
2	RC	0x0	path1_vld 1'b0: DATA1R_REG, DATA1L_REG value is invalid. 1'b1: DAT1R_REG, DATA1L_REG value is valid.
1	RC	0x0	path2_vld 1'b0: DATA2R_REG, DATA2L_REG value is invalid. 1'b1: DATA2R_REG, DATA2L_REG value is valid.
0	RC	0x0	path3_vld 1'b0: DATA3R_REG, DATA3L_REG value is invalid. 1'b1: DATA3R_REG, DATA3L_REG value is valid.

PDM_VERSION

Address: Operational Base(0xFF830000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x59313031	ver PDM version

PDM_RDN_DEL_CTRL

Address: Operational Base(0xFF830000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	del_num delete data num. if sw_cfg_enable=1'b1, del_num is the software config value. if sw_cfg_enalbe=1'b0, del_num is the hardware generate value.
15:2	RO	0x0000	reserved
1	RW	0x0	sw_cfg_enable software config enable bit. only vaild when rdn_del_enable = 1'b1; when sw_cfg_enable=1'b1, delete num due to the software via config del_num; when sw_cfg_enable=1'b0, delete num due to the hardware, and the num read from del_num registers.
0	RW	0x0	rdn_del_enable redundant data delete enable bit.

PDM_MONO_PATH_CTRL

Address: Operational Base(0xFF830000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mono_path_enable mono path enable bit. if mono path enable, path0/path1/path2/path3 only one path enable, and the right or left path depended on the lr_ch_ex reg. if data_vld_width cfg right/left data only 16bit, the data write to memory is combined by two data, L1, L0 or R1, R0.

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PDM_SHIFT_CTRL

Address: Operational Base(0xFF830000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	SHIFT_R_EN CICout data rigth shift enable.
2	RW	0x0	SHIFT_L_EN CICout data left shift enable.
1:0	RW	0x0	SHIFT_BITS CICout shift bits control. 2'b00: 2bit 2'b01: 4bit 2'b10: 6bit 2'b11: 8bit

PDM_INCR_RXDR

Address: Operational Base(0xFF830000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	receive_fifo_data FIFO data can be read from these registers. This register is used when the access address is increment.

11.5 Interface Description

There are two groups of PDM IO interfaces embedded in the chip. Following figure shows the group 0 and group 1 PDM IO interface respectively.

Table 11-2 Group 0 PDM IO Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
o_pdm_clk	O	I2S0_SDO1_M0/I2S0_SDI3_M0/PDM_CLK0_M0/PCIE20_CLKREQN_M1/UART5_TX_M1/GPIO3_A6_d	GPIO3_IOC_GPIO3A_IOMUX_H[11:8]=3
o_pdm_clk	O	I2S0_MCLK_M0/UART2_CTSN_M1/PDM_CLK1_M0/GPIO3_A2_d	GPIO3_IOC_GPIO3A_IOMUX_L[11:8]=3
i_pdm_data0	I	I2S0_SDI0_M0/PDM_SDI0_M0/GPIO3_B1_d	GPIO3_IOC_GPIO3B_IOMUX_L[7:4]=2
i_pdm_data1	I	I2S0_SDO3_M0/I2S0_SDI1_M0/PDM_SDI1_M0/PCIE20_PERSTN_M1/GPIO3_B0_d	GPIO3_IOC_GPIO3B_IOMUX_L[3:0]=3
i_pdm_data2	I	I2S0_SDO2_M0/I2S0_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEN_M1/UART5_RX_M1/GPIO3_A7_d	GPIO3_IOC_GPIO3A_IOMUX_H[15:12]=3
i_pdm_data3	I	I2C3_SCL_M0/UART2_TX_M1/PDM_SDI3_M0/CAN0_TX_M0/UART5_CTSN_M1/GPIO3_A0_d	GPIO3_IOC_GPIO3A_IOMUX_L[3:0]=3

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 11-3 Group 1 PDM IO Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
o_pdm_clk	O	VO_LCDC_CLK/RGMII_CLK_M0/CAM_CLK1_OUT_M1/PDM_CLK0_M1/GPIO4_B7_d	GPIO4_IOC_GPIO4B_IOMUX_H[15:12]=4
o_pdm_clk	O	VO_LCDC_D17/ETH_CLK_25M_OUT_M0/CAM_CLK0_OUT_M1/I2S2_SCLK_M1/PDM_CLK1_M1/GPIO4_B1_d	GPIO4_IOC_GPIO4B_IOMUX_L[7:4]=5
i_pdm_data0	I	VO_LCDC_D9/RGMII_RXDV_M0/UART1_RTSN_M1/PDM_SDI0_M1/UART6_TX_M1/GPIO4_A7_d	GPIO4_IOC_GPIO4A_IOMUX_H[15:12]=4
i_pdm_data1	I	VO_LCDC_D16/RGMII_RXER_M0/UART1_CTSN_M1/PDM_SDI1_M1/UART6_RX_M1/GPIO4_B0_d	GPIO4_IOC_GPIO4B_IOMUX_L[3:0]=4
i_pdm_data2	I	VO_LCDC_D1/RGMII_RXD0_M0/UART1_TX_M1/PDM_SDI2_M1/I2C3_SCL_M1/GPIO4_A5_d	GPIO4_IOC_GPIO4A_IOMUX_H[7:4]=4
i_pdm_data3	I	VO_LCDC_D8/RGMII_RXD1_M0/UART1_RX_M1/PDM_SDI3_M1/I2C3_SDA_M1/GPIO4_A6_d	GPIO4_IOC_GPIO4A_IOMUX_H[11:8]=4

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11.6 Application Notes

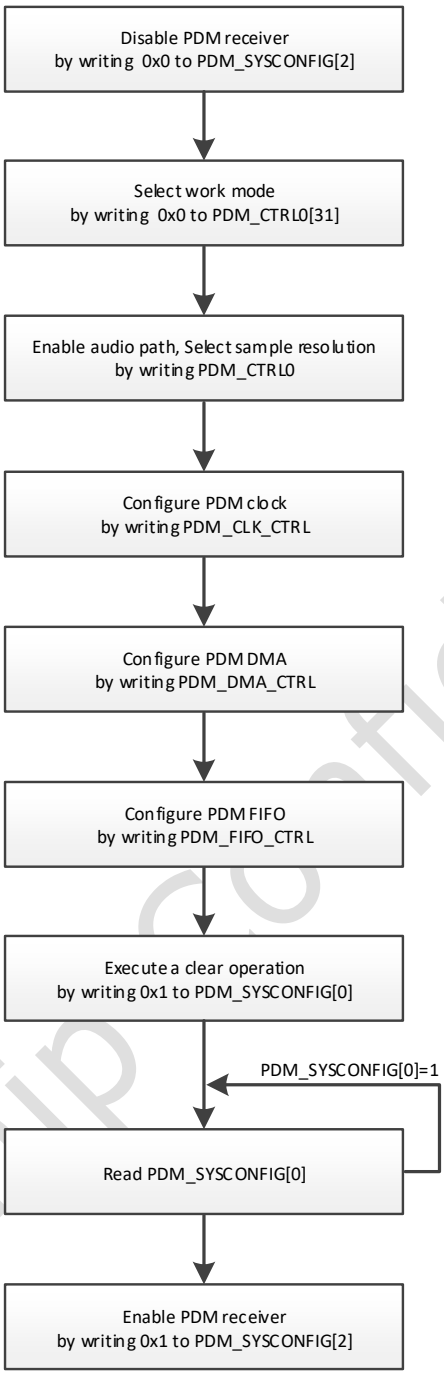

Fig.11-6 PDM Operation Flow

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Chapter 12 Sony/Philips Digital Interface Transmitter (SPDIF TX)

12.1 Overview

The SPDIF transmitter is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to carry stereophonic programmes, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible.
When used for other purposes, the interface is primarily intended to carry audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to carry data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
In all cases, the clock references and auxiliary information are transmitted along with the programme. MCLK is the operation clock of SPDIF transmitter.

Table 12-1 Maximum Frequency of MCLK for the SPDIF Transmitter

SPDIF transmitter	Maximum frequency of MCLK
SPDIF	150MHz

Each SPDIF transmitter supports following features.

- Support one internal 32-bit wide and 32-location deep sample data buffer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support AHB and APB bus interface
- Support biphase format stereo audio data output
- Support DMA handshake interface and configurable DMA water level
- Support sample data buffer empty and block terminate interrupt
- Support combine interrupt output
- Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
- Support 48, 44.1, 32kHz sample rate
- Support MCLK frequencies of 12.288Mhz, 8.192Mhz and 11.2896Mhz
- Support 16, 20, 24 bits audio data transfer
- Support frame transmission frequency, fixed to 128 times of audio data sampling rate

12.2 Block Diagram

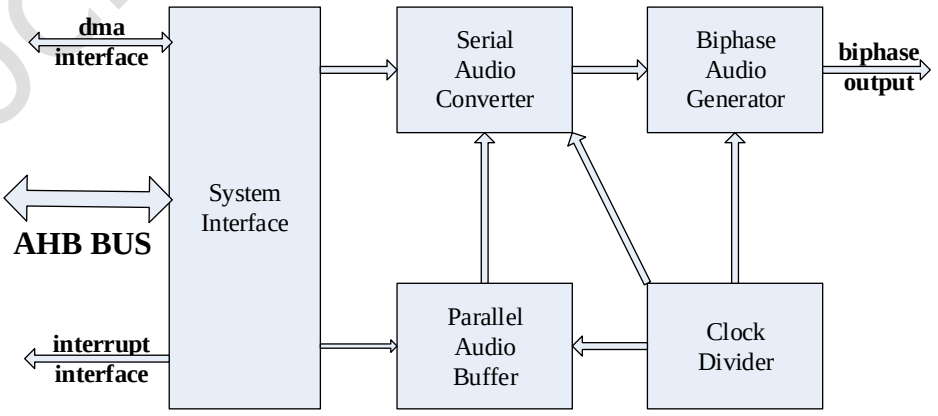

Fig.12-1 SPDIF transmitter Block Diagram

The SPDIF transmitter is composed of following module.

System Interface

The system interface implements the AHB slave operation. It contains not only control

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registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

Clock Divider

The clock divider implements clock generation function. It divides the source clock MCLK to generate the working clock used for the digital audio data transformation and transmission.

Parallel Audio Buffer

The parallel audio buffer stores the audio data to be transmitted. The size of the FIFO is 32bits x 32.

Serial Audio Converter

The serial audio converter converts the parallel audio data from the parallel audio buffer to the serial audio data.

Biphase Audio Generator

The biphase audio generator reads serial audio data from the serial audio converter and generates biphase audio data based on IEC-60958 standard.

12.3 Function Description

12.3.1 Frame Format

A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of transmission of frames corresponds exactly to the source sampling frequency.
In the 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. The first sub-frame(left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information.
The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

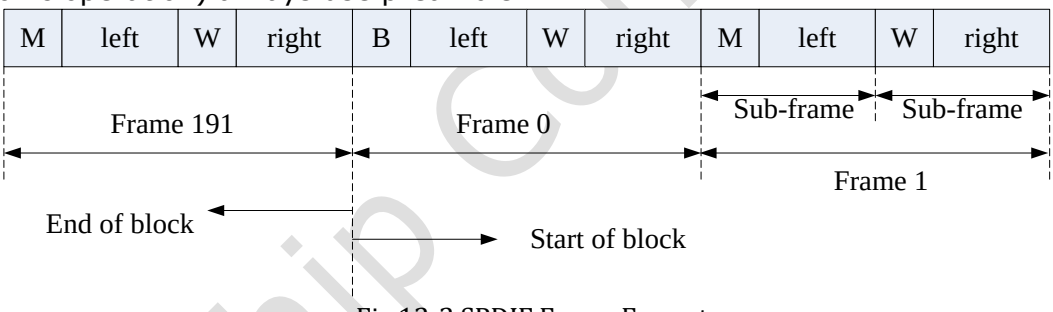

Fig.12-2 SPDIF Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

12.3.2 Sub-frame Format

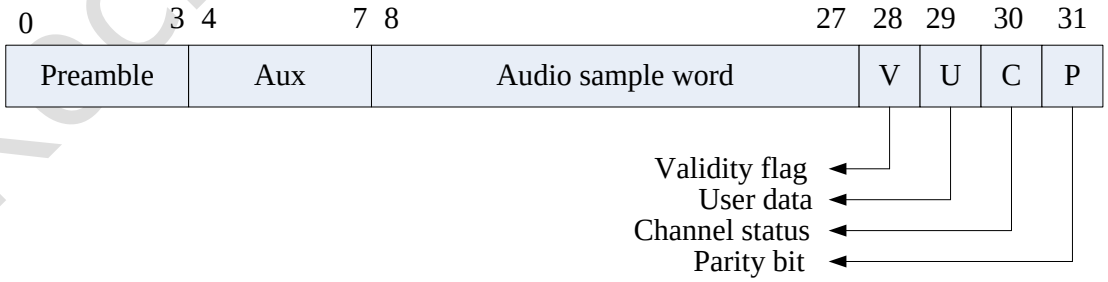

Fig.12-3 SPDIF Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8. Time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to

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7 are designated auxiliary sample bits.
If the source provides fewer bits than the interface allows (either 24 or 20), the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

12.3.3 Channel Coding

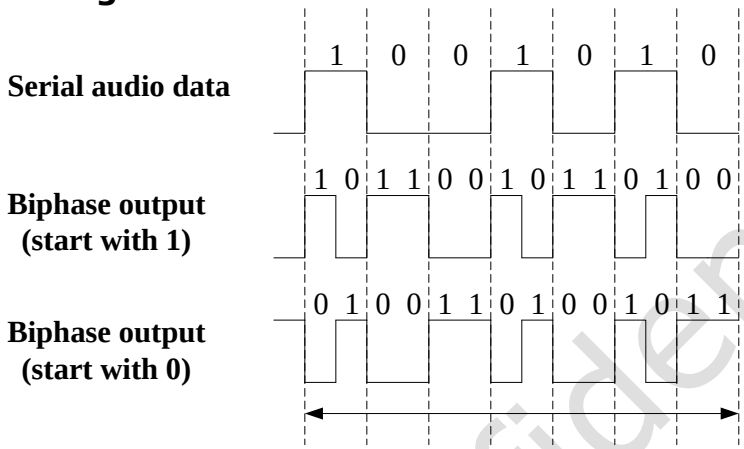

Fig.12-4 SPDIF Channel Coding

To minimize the direct current component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.
Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'. However, it is different from the first if the bit is logical '1'.

12.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.
To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.
A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

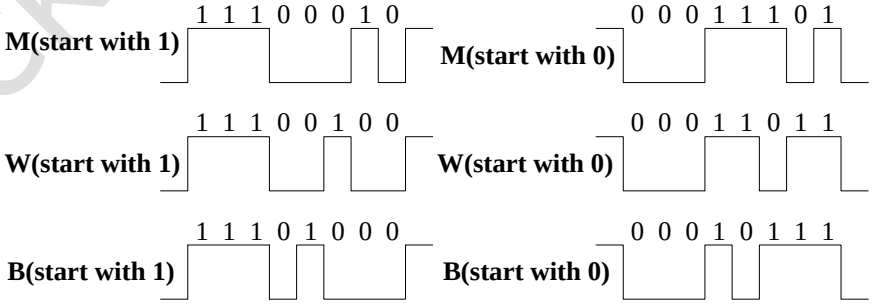

Fig.12-5 SPDIF Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

12.4 Register Description

12.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as

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follows.

12.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPDIF_TX_CFGR	0x0000	W	0x00000000	Transfer Configuration Register
SPDIF_TX_SDBLR	0x0004	W	0x00000000	Sample Date Buffer Level Register
SPDIF_TX_DMACR	0x0008	W	0x00000000	DMA Control Register
SPDIF_TX_INTCR	0x000C	W	0x00000000	Interrupt Control Register
SPDIF_TX_INTSR	0x0010	W	0x00000000	Interrupt Status Register
SPDIF_TX_XFER	0x0018	W	0x00000000	Transfer Start Register
SPDIF_TX_SMPDR	0x0020	W	0x00000000	Sample Data Register
SPDIF_TX_VLDFRn	0x0060	W	0x00000000	Validity Flag Register n
SPDIF_TX_USRDRn	0x0090	W	0x00000000	User Data Register n
SPDIF_TX_CHNSRn	0x00C0	W	0x00000000	Channel Status Register n
SPDIF_TX_BURTSINFO	0x00D0	W	0x00000000	This define the channel burst info when the channel conveys non-linear PCM.
SPDIF_TX_REPETTION	0x0104	W	0x00000000	This register provides the repetition of the bitstream when channel conveys non-linear PCM. In the design, it is defined the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design.
SPDIF_TX_BURTSINFO_SHD	0x0108	W	0x00000000	This define the channel burst info when the channel conveys non-linear PCM.
SPDIF_TX_REPETTION_SHD	0x010C	W	0x00000000	This register provides the repetition of the bitstream when channel conveys non-linear PCM
SPDIF_TX_USRDR_SHDn	0x0190	W	0x00000000	Shadow User Data Register n

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

12.4.3 Detail Registers Description

SPDIF_TX_CFGR

Address: Operational Base(0xFF840000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	MCD Fmclk/Fsdo This parameter can be calculated by Fmclk/(Fs*128). Fs=the sample frequency be wanted
15:9	RO	0x00	reserved
8	RW	0x0	PCMTYPE 0: linear PCM 1: non-linear PCM
7	WO	0x0	CLR Write 1 to clear mclk domain logic. Read return zero.
6	RW	0x0	CSE 0: disable 1: enable The bit should be set to 1 when the channel conveys non-linear PCM

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Bit	Attr	Reset Value	Description
5	RW	0x0	UDE 0: disable 1: enable
4	RW	0x0	VFE 0: disable 1: enable
3	RW	0x0	ADJ 0: Right justified 1: Left justified
2	RW	0x0	HWT 0: disable 1: enable It is valid only when the valid data width is 16bit.
1:0	RW	0x0	VDW 00: 16bit 01: 20bit 10: 24bit 11: reserved The valid data width is 16bit only for non-linear PCM

SPDIF_TX_SDBLR

Address: Operational Base(0xFF840000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	SDBLR Contains the number of valid data entries in the sample data buffer.

SPDIF_TX_DMACR

Address: Operational Base(0xFF840000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	TDE 0: Transmit DMA disabled 1: Transmit DMA enabled
4:0	RW	0x00	TDL This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the Sample Date Buffer is equal to or below this field value

SPDIF_TX_INTCR

Address: Operational Base(0xFF840000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	W1C	0x0	UDTIC Write '1' to clear the user data interrupt.
16	W1C	0x0	BTTIC Write 1 to clear the interrupt.
15:10	RO	0x00	reserved
9:5	RW	0x00	SDBT Sample Date Buffer Threshold for empty interrupt

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Bit	Attr	Reset Value	Description
4	RW	0x0	SDBEIE 0: disable 1: enable
3	RW	0x0	BTTIE When enabled, an interrupt will be asserted when the block transfer is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM. 0: disable 1: enable
2	RW	0x0	UDTIE 0: disable 1: enable If enabled, an interrupt will be asserted when the content of the user data register is fed into the corresponding shadow register
1:0	RO	0x0	reserved

SPDIF_TX_INTSR

Address: Operational Base(0xFF840000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SDBEIS 0: inactive 1: active
3	RW	0x0	BTTIS 0: inactive 1: active
2	RW	0x0	UDTIS 0: inactive 1: active
1:0	RO	0x0	reserved

SPDIF_TX_XFER

Address: Operational Base(0xFF840000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	XFER Transfer Start Register

SPDIF_TX_SMPDR

Address: Operational Base(0xFF840000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SMPDR Sample Data Register

SPDIF_TX_VLDFRn

Address: Operational Base(0xFF840000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VLDFR_SUB_1 Validity Flag Register 0
15:0	RW	0x0000	VLDFR_SUB_0 Validity Flag for Subframe 0

SPDIF_TX_USRDRn

Address: Operational Base(0xFF840000) + offset (0x0090)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	USR_SUB_1 User Data Bit for Subframe 1
15:0	RW	0x0000	USR_SUB_0 User Data Bit for Subframe 0

SPDIF_TX_CHNSRn

Address: Operational Base(0xFF840000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CHNSR_SUB_1 Channel Status Bit for Subframe 1
15:0	RW	0x0000	CHNSR_SUB_0 Channel Status Bit for Subframe 0

SPDIF_TX_BURTSINFO

Address: Operational Base(0xFF840000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PD Preamble Pd for non-linear pcm, indicating the length of burst payload in unit of bytes or bits.
15:13	RW	0x0	BSNUM This field indicates the bitstream number. Usually the bistream number is 0.
12:8	RW	0x00	DATAINFO This field gives the data-type-dependent info
7	RW	0x0	ERRFLAG 0: indicates a valid burst-payload 1: indicates that the burst-payload may contain errors
6:0	RW	0x00	DATATYPE 0000000: null data 0000001: AC-3 data 0000011: Pause data 0000100: MPEG-1 layer 1 data 0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 0000110: MPEG-2 data with extension 0000111: MPEG-2 AAC 0001000: MPEG-2, layer-1 low sampling frequency 0001001: MPEG-2, layer-2 low sampling frequency 0001010: MPEG-2, layer-3 low sampling frequency 0001011: DTS type I 0001100: DTS type II 0001101: DTS type III 0001110: ATRAC 0001111: ATRAC 2/3 0010000: ATRAC-X 0010001: DTS type IV 0010010: WMA professional type I 0110010: WMA professional type II 1010010: WMA professional type III 1110010: WMA professional type IV 0010011: MPEG-2 AAC low sampling frequency 0110011: MPEG-2 AAC low sampling frequency 1010011: MPEG-2 AAC low sampling frequency 1110011: MPEG-2 AAC low sampling frequency 0010100: MPEG-4 AAC 0110100: MPEG-4 AAC 1010100: MPEG-4 AAC

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Bit	Attr	Reset Value	Description
			1110100: MPEG-4 AAC 0010101: Enhanced AC-3 0010110: MAT others: reserved

SPDIF_TX_REPETTION

Address: Operational Base(0xFF840000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	REPETTION This define the repetition period when the channel conveys non-linear PCM

SPDIF_TX_BURTSINFO_SHD

Address: Operational Base(0xFF840000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	PD Preamble Pd for non-linear pcm, indicating the length of burst payload in unit of bytes or bits.
15:13	RO	0x0	BSNUM This field indicates the bitstream number. Usually the birstream number is 0.
12:8	RO	0x00	DATAINFO This field gives the data-type-dependent info
7	RO	0x0	ERRFLAG 0: indicates a valid burst-payload 1: indicates that the burst-payload may contain errors
6:0	RO	0x00	DATATYPE 0000000: null data 0000001: AC-3 data 0000011: Pause data 0000100: MPEG-1 layer 1 data 0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 0000110: MPEG-2 data with extension 0000111: MPEG-2 AAC 0001000: MPEG-2, layer-1 low sampling frequency 0001001: MPEG-2, layer-2 low sampling frequency 0001010: MPEG-2, layer-3 low sampling frequency 0001011: DTS type I 0001100: DTS type II 0001101: DTS type III 0001110: ATRAC 0001111: ATRAC 2/3 0010000: ATRAC-X 0010001: DTS type IV 0010010: WMA professional type I 0110010: WMA professional type II 1010010: WMA professional type III 1110010: WMA professional type IV 0010011: MPEG-2 AAC low sampling frequency 0110011: MPEG-2 AAC low sampling frequency 1010011: MPEG-2 AAC low sampling frequency 1110011: MPEG-2 AAC low sampling frequency 0010100: MPEG-4 AAC 0110100: MPEG-4 AAC 1010100: MPEG-4 AAC

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Bit	Attr	Reset Value	Description
			1110100: MPEG-4 AAC 0010101: Enhanced AC-3 0010110: MAT others: reserved

SPDIF_TX_REPETTION_SHD

Address: Operational Base(0xFF840000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	REPETTION This register provides the repetition of the bitstream when channel conveys non-linear PCM. In the design, it is defined the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design.

SPDIF_TX_USRDR_SHDn

Address: Operational Base(0xFF840000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	USR_SUB_1 User Data Bit for Subframe 1
15:0	RO	0x0000	USR_SUB_0 User Data Bit for Subframe 0

12.5 Interface Description

SPDIF are used to communicate with audio equipment outside this chip. Following table shows the interface of SPDIF.

Table 12-3 SPDIF TX Interface Description

Module Pin	Dir	PIN Name	IOMUX Setting
spdif_sdo	O	I2C3sdam0/UART2rxm1/SPDIFtxm0/CAN0rxm0/UART5rtsnm1/VCCIO1GPIO3a1	GRF_GPIO3A_IOMUX_L[7:4]=3
spdif_sdo	O	SPI0csn1m0/PWM4m0/CPUavs/SPDIFtxm1/PMUIO1GPIO0b7	PMUGRF_GPIO0B_IOMUX_H[15:12]=4
spdif_sdo	O	SDMMC0cmd/SPDIFtxm2/UART5rxm0/CAN1rxm0/VCCIO3GPIO1b7	GRF_GPIO1B_IOMUX_H[15:12]=2

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12.6 Application Notes

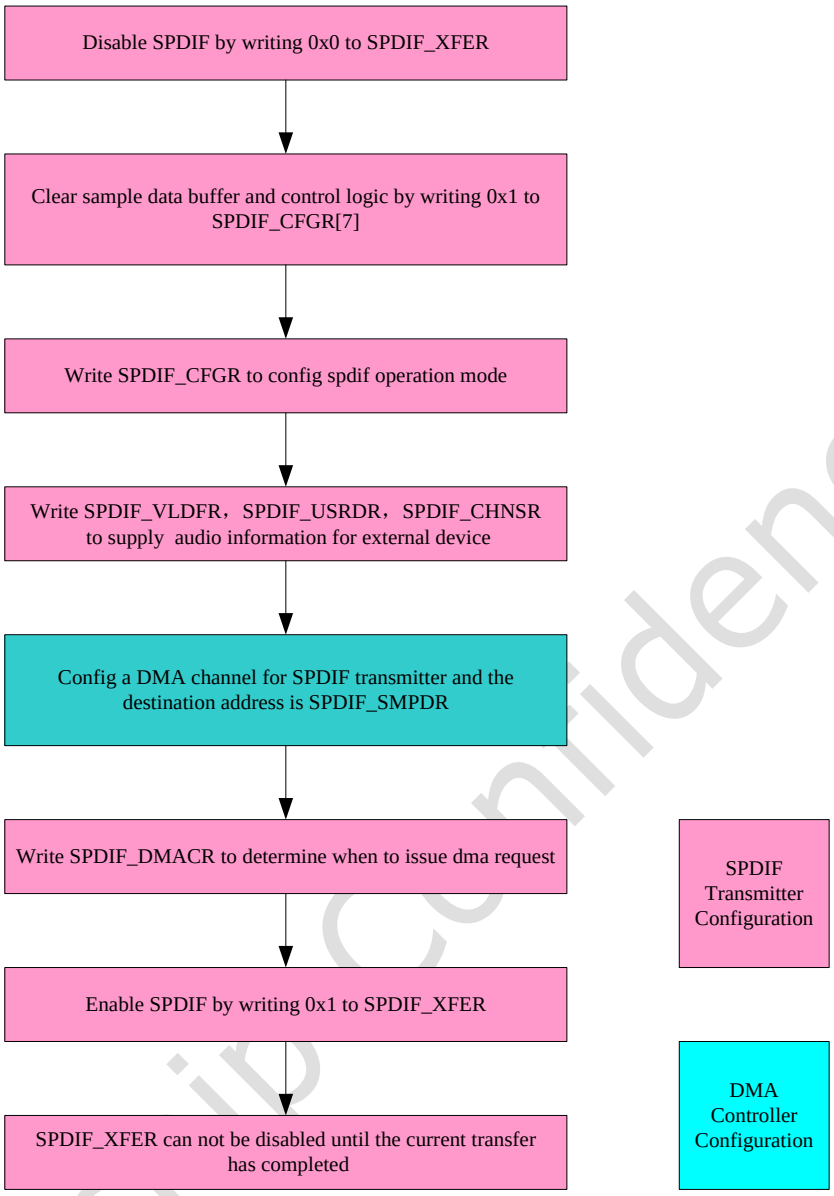

Fig.12-6 SPDIF transmitter operation flow chart

The above figure shows the operation flow of SPDIF operation. Note that the configuration register can be written only when the transfer is stopped.

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Chapter 13 Serial Audio Interface (SAI)

13.1 Overview

The SAI controller is designed for interfacing between the AHB bus and the serial audio interface bus. The SAI is a serial link for digital audio data transfer between devices in the system .The SAI interface (Serial Audio Interface) offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted. I2S standards, PCM, and TDM may be addressed.
SAI is widely used in the devices such as ADC, DAC, DSP, CPU, etc. With the SAI interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.

13.1.1 Features

- Support eight internal 32-bit wide and 32-location deep FIFOs, four for transmitting and
  the other for receiving audio data
- Support AHB bus interface
- Support 8 ~ 32 bits audio data transfer
- Support master and slave mode
- Support DMA handshaking interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combined interrupt output
- Support 8 to 32 bit audio data left or right justified in 32-bit wide FIFO
- Support two 16-bit audio data store together in one 32-bit wide location and support four 8-bit audio data store together in one 32-bit wide location
- Support TX to RX loopback bypass mode
- Support audio protocol: I2S, PCM, TDM
- Support Number of bits by frame can be configurable
- Support First active slot position in the frame is configurable
- Support up to 128 slots available with configurable size
- Support slot length 8 to 32 bits configurable
- Support slot valid data length 8 to 32 bits configurable
- Support Mono audio mode
- Support slot mask configurable
- Support First active bit position in the slot is configurable
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and FS polarity
- Support up to four lanes parallel transceivers
- Support SDI, SDO IOMUX

13.2 Block Diagram

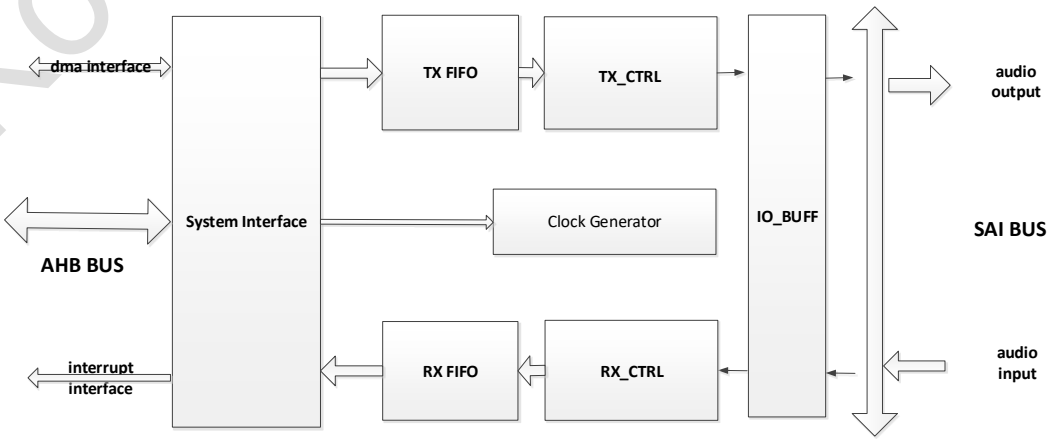

Fig. 13-1 SAI Block Diagram

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System Interface
The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.
Clock Generator
The Clock Generator implements clock generation function. The input source clock to the module is MCLK_SAI, and by the divider of the module, the clock generator generates SCLK and FS to transmitter and receiver.
Transmitters
The Transmitters implement transmission operation. The transmitters can act as either a master or a slave, with I2S, PCM or TDM mode surround serial audio interface.
Receiver
The Receiver implements receive operation. The receiver can act as either a master or a slave, with I2S, PCM or TDM mode stereo serial audio interface.
Transmit FIFO
The Transmit FIFO is the buffer to store transmitted audio data. The size of the FIFO is 32bits x 32.
Receive FIFO
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 32.
IO_BUFF
SDO, SDI, LRCK_IN and LRCK_OUT Register output.

13.3 Function Description

In the SAI controller, there are two types: transmitter-master &receiver-master; transmitter-slave & receiver-slave.
In broadcasting application, the SAI controller is used as a transmitter and external or internal audio CODEC is used as a receiver. In recording application, the SAI controller is used as a receiver and external or internal audio CODEC is used as a transmitter. Either the SAI controller or the audio CODEC can act as a master or a slave, but if one is master, the other must be slave.

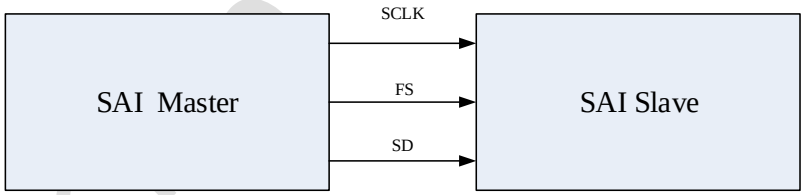

Fig.13-2 SAI transmitter-master & receiver-slave condition

When the transmitter acts as a master, it sends all signals to the receiver (the slave), and CPU controls when to send clock and data to the receiver. When acts as a slave, SD signal still goes from transmitter to receiver, but SCLK and FS signals are from the receiver (the master) to the transmitter. Based on three interface specifications, transmitting data should be ready before transmitter receives SCLK and FS signals. CPU should know when the receiver to initialize a transaction and when the transmitter to send data.
When the receiver acts as a master, it sends SCLK and FS signals to the transmitter (the slave) and receives serial data. So CPU must tell the transmitter when to start a transaction for it to prepare transmitting data then start a transfer and send clock and channel-select signals. When the receiver acts as a slave, CPU should only do initial setting and wait for all signals and then start reading data.
Before transmitting or receiving data, CPU need do initial setting to the SAI register. These includes CPU settings, SAI interface registers settings, and maybe the embedded SoC platform settings. These registers must be set before starting data transfer.
The SAI interface offers a wide set of audio protocols due to its flexibility and wide range of configurations. It can support I2S/PCM/TDM aduio protocol by different configuration.

13.3.1 I2S normal mode

This is the waveform of I2S normal mode. For FS (sai_fs_rx/sai_fs_tx) signal, it goes low to

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indicate left channel and high to right channel. For SD (sai_sdo, sai_sdi) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after FS changes. The range of SD signal width is from 8 to 32bits.

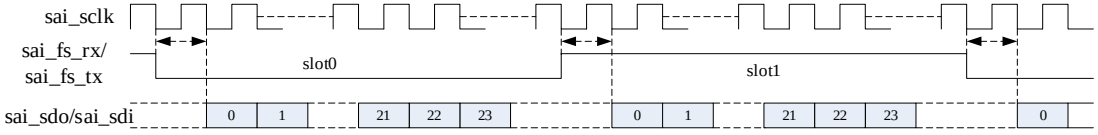

Fig.13-3 I2S Normal Mode Timing Format

13.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sai_sdo, sai_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when FS changes. The range of SD signal width is from 8 to 32bits.

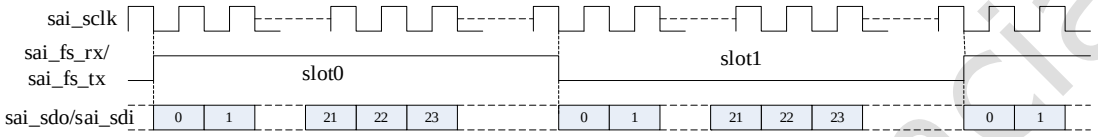

Fig.13-4 I2S Left Justified Mode Timing Format

13.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sai_sdo, sai_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the FS signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 8 to 32bits.

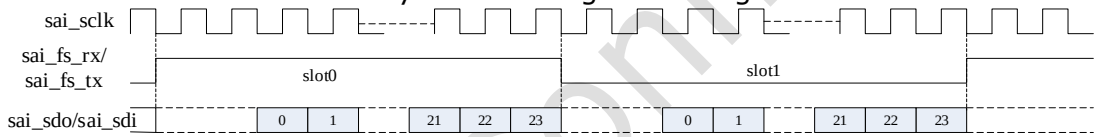

Fig.13-5 I2S Right Justified Mode Timing Format

13.3.4 PCM early mode

This is the waveform of PCM early mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (sai_sdo, sai_sdi) signal, it sends the first bit (MSB or LSB) at the same time when FS goes high. The range of SD signal width is from 8 to 32bits.

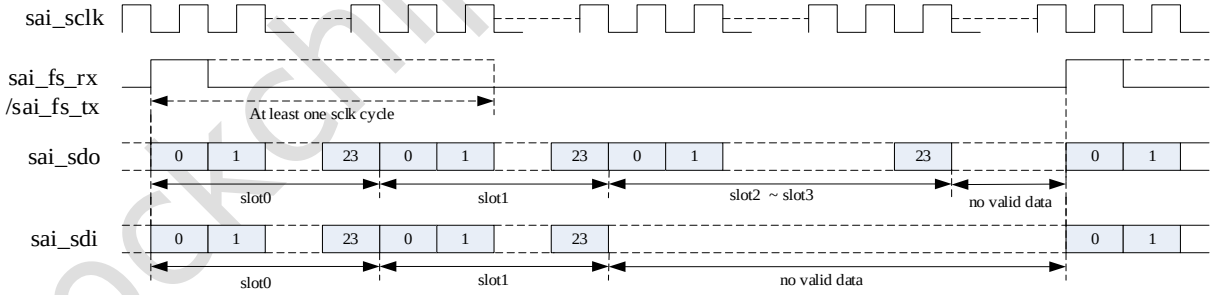

Fig.13-6 PCM Early Mode Timing Format

13.3.5 Flexibility and wide range of configurations

The SAI interface (Serial Audio Interface) offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted. I2S standards, PCM, and TDM may be addressed.

This is the waveform of PCM mode(SBW==VDW,FW >=SBW *SNB). For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate the start of a group of audio data.

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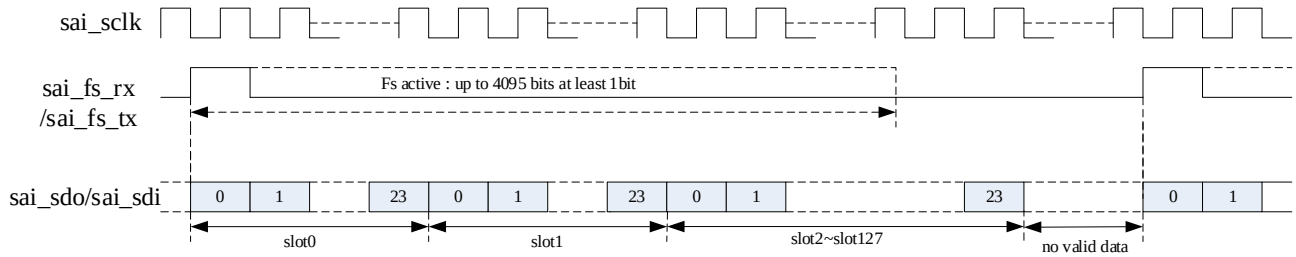

Fig.13-7 SAI PCM mode timing format

This is the waveform of I2S left mode(SBW>=VDW,FW >=SBW *SNB,VDJ==1'b1).

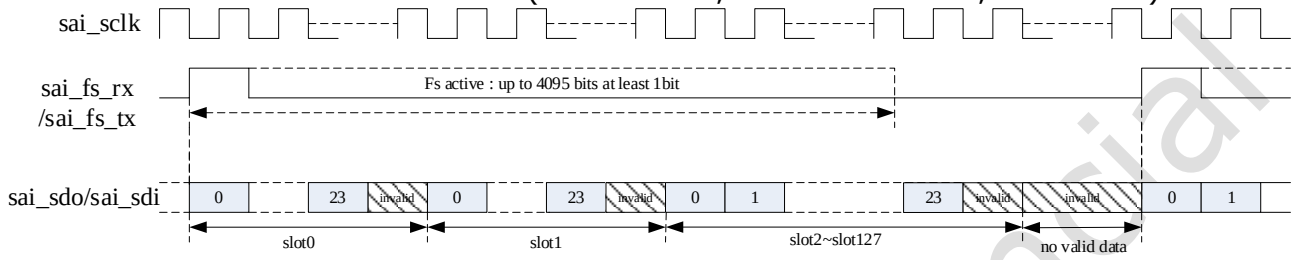

Fig.13-8 SAI I2S left mode timing format

This is the waveform of I2S right mode(SBW>=VDW,FW >=SBW *SNB,VDJ==1'b0).

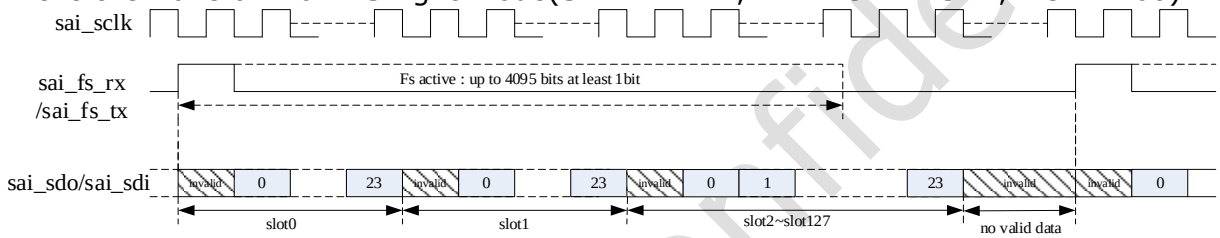

Fig.13-9 SAI I2S right mode timing format

This is the waveform of FS and SD delay time, as the posedge of FS (sai_fs_rx / sai_fs_tx) signal,we can send data at different time ,The time between the FS rise edge and the first valid bit can be configured using the fs_shift register,when fs_shift[0] == 1'b0,data send at posedge of sclk,when fs_shift[0] == 1'b1,data send at negedge of sclk.

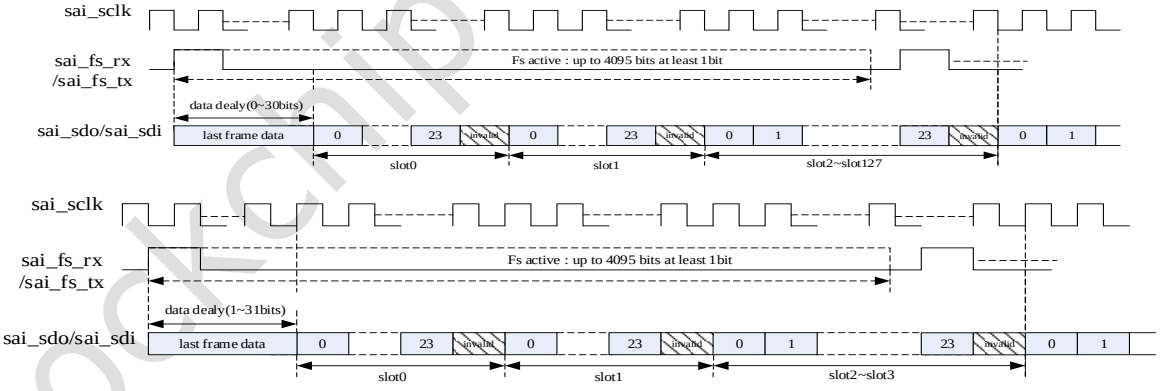

Fig.13-10 fs shift timing format

13.4 Register Description

13.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SAI0	0xFF800000
SAI1	0xFF810000
SAI2	0xFF820000

13.4.2 Registers Summary

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Name	Offset	Size	Reset Value	Description
SAI_TXCR	0x0000	W	0x00000FFF	Transmit Operation Control Register
SAI_FSCR	0x0004	W	0x0001F03F	Transmit Frame Sync Operation Control Register
SAI_RXCR	0x0008	W	0x00000FFF	Receive Operation Control Register
SAI_MONO_CR	0x000C	W	0x00000000	Mono mode control
SAI_XFER	0x0010	W	0x00000000	Transfer Start Register
SAI_CLR	0x0014	W	0x00000000	Sclk Domain Logic Clear Register
SAI_CKR	0x0018	W	0x00000000	Clock Generation Register
SAI_TXFIFOLR	0x001C	W	0x00000000	TX FIFO Level Register
SAI_RXFIFOLR	0x0020	W	0x00000000	RX FIFO Level Register
SAI_DMACR	0x0024	W	0x00000000	DMA Control Register
SAI_INTCR	0x0028	W	0x01F00000	Interrupt Control Register
SAI_INTSR	0x002C	W	0x00000000	Interrupt Status Register
SAI_TXDR	0x0030	W	0x00000000	Transmit FIFO Data Register
SAI_RXDR	0x0034	W	0x00000000	Receive FIFO Data Register
SAI_PATH_SEL	0x0038	W	0x0000E4E4	Path select Register
SAI_TX_SLOT_MASK0	0x003C	W	0x00000000	Transmit Slot 0~31 Mask state
SAI_TX_SLOT_MASK1	0x0040	W	0x00000000	Transmit Slot 32~63 Mask state
SAI_TX_SLOT_MASK2	0x0044	W	0x00000000	Transmit Slot 64~95 Mask state
SAI_TX_SLOT_MASK3	0x0048	W	0x00000000	Transmit Slot 96~127 Mask state
SAI_RX_SLOT_MASK0	0x004C	W	0x00000000	Receive Slot 0~31 Mask state
SAI_RX_SLOT_MASK1	0x0050	W	0x00000000	Receive Slot 32~63 Mask state
SAI_RX_SLOT_MASK2	0x0054	W	0x00000000	Receive Slot 64~95 Mask state
SAI_RX_SLOT_MASK3	0x0058	W	0x00000000	Receive Slot 96~127 Mask state
SAI_TX_DATA_CNT	0x005C	W	0x00000000	Tx data counter register
SAI_RX_DATA_CNT	0x0060	W	0x00000000	Rx data counter register
SAI_SAI_TX_SHIFT	0x0064	W	0x00000000	Tx shift register
SAI_SAI_RX_SHIFT	0x0068	W	0x00000000	Rx shift register
SAI_TIMEOUT	0x006C	W	0x00000000	
SAI_VERSION	0x0070	W	0x20200520	Version Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.3 Detail Registers Description

SAI_TXCR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	tx_delay_en 1'b0: NO DELAY 1'b1: DELAY fsync pos
21:20	RW	0x0	tcsr Transmit channel select register 2'b00: One lane 2'b01: Two lanes 2'b10: Three lanes 2'b11: Four lanes

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Bit	Attr	Reset Value	Description
19	RW	0x0	sjm Store justified mode (Can be written only when XFER[0] bit is 0.) 8bit~31bit DATA stored in 32 bits width FIFO. 1'b0: Right justified 1'b1: Left justified
18	RW	0x0	fbm first bit mode (Can be written only when XFER[0] bit is 0.) 1'b0: MSB 1'b1: LSB
17:11	RW	0x01	snb Transfer slot number (Can be written only when XFER[0] bit is 0.) Number of slots in a frame 7'h00: 1slot 7'h01: 2slot 7'h02: 3slot 7'h03: 4slot ..... 7'h7e: 127slot 7'h7f: 128slot
10	RW	0x1	vdj Valid data justified mode (Can be written only when XFER[0] bit is 0.) 1'b0: Right justified 1'b1: Left justified
9:5	RW	0x1f	sbw Transfer slot bits width (Can be written only when XFER[0] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit
4:0	RW	0x1f	vdw Slot valid data width (Can be written only when XFER[0] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit

SAI_FSCR

Address: **Operational Base** + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	edge_sel 1'h0: pos 1'h1: pos and neg
23:12	RW	0x01f	fpw Transfer frame pulse width (Can be written only when XFER[0] is 0.) 12'h000: 1bit 12'h001: 2bit 12'h002: 3bit ..... 12'hffe:4095bit 12'hfff:res
11:0	RW	0x03f	fw Transfer frame width (Can be written only when XFER[0] is 0.) 12'h000~12'h006: Reserved 12'h007: 8bit 12'h008: 9bit ..... 12'hffe: 4095bit 12'hfff: 4096bit

SAI_RXCR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	rx_delay_en 1'b0: NO DELAY 1'b1: DELAY fsync pos
21:20	RW	0x0	rcsr receive channel select register 2'b00: One lane 2'b01: Two lanes 2'b10: Three lanes 2'b11: Four lanes
19	RW	0x0	sjm Store justified mode (Can be written only when XFER[2] bit is 0.) 8bit~31bit DATA stored in 32 bits width FIFO. 1'b0: Right justified 1'b1: Left justified
18	RW	0x0	fbm first bit mode (Can be written only when XFER[2] bit is 0.) 1'b0: MSB 1'b1: LSB

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Bit	Attr	Reset Value	Description
17:11	RW	0x01	snb receive slot number (Can be written only when XFER[2] bit is 0.) number of slots in a frame 7'h00: 1slot 7'h01: 2slot 7'h02: 3slot 7'h03: 4slot ..... 7'h7e: 127slot 7'h7f: 128slot
10	RW	0x1	vdj Valid data justified mode (Can be written only when XFER[2] bit is 0.) 1'b0: Right justified 1'b1: Left justified
9:5	RW	0x1f	sbw receive slot bits width (Can be written only when XFER[2] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit
4:0	RW	0x1f	vdw Valid fata width (Can be written only when XFER[2] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit

SAI_MONO_CR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:2	RW	0x00	rx_mono_slot_sel Receive mono mode valid slot data select 7'h00: First slot data valid 7'h01: Second slot data valid ..... 7'h7f: Slot128 data valid

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Bit	Attr	Reset Value	Description
1	RW	0x0	rx_mono_en Receive mono audio data enable bit 1'b0: Normal mode 1'b1: Mono mode
0	RW	0x0	tx_mono_en Transmit mono audio data enable bit 1'b0: Normal mode 1'b1: Mono mode

SAI_XFER

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	rx_idle rx idle
7	RO	0x0	tx_idle tx idle
6	RO	0x0	fs_idle fs idle
5	RW	0x0	rx_data_cnt_en 1'b0: Stop cnt 1'b1: Start cnt
4	RW	0x0	tx_data_cnt_en 1'b0: Stop cnt 1'b1: Start cnt
3	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
2	RW	0x0	txs 1'b0: Stop TX transfer 1'b1: Start TX transfer
1	RW	0x0	fss 1'b0: Stop frame sync 1'b1: Start frame sync
0	RW	0x0	clk_gate_en 1'b0: Stop clk 1'b1: Start clk

SAI_CLR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	fsc This is a self-cleared bit. write 1 to clear all receive logic.
1	W1C	0x0	rxc RX logic clear This is a self-cleared bit. write 1 to clear all receive logic.
0	W1C	0x0	txc TX logic clear This is a self-cleared bit. write 1 to clear all transmit logic.

SAI_CKR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:3	RW	0x000	mdiv (Can be written only when XFER[0] bit is 0.) mclk divider = (mclk/sclk)-1. For example, if mclk divider is 5, then the frequency of sclk is mclk/6.
2	RW	0x0	mss Transmit master/slave mode select (Can be written only when XFER[0] bit is 0.) 1'b0: Master mode(sclk output) 1'b1: Slave mode(sclk input)
1	RW	0x0	ckp Transmit sclk polarity (Can be written only when XFER[2] or XFER[0] bit is 0.) 1'b0: Sample data at posedge sclk and drive data at negedge sclk 1'b1: Sample data at negedge sclk and drive data at posedge sclk
0	RW	0x0	fsp Transmit fs polarity (Can be written only when XFER[2] or XFER[0] bit is 0.) 1'b0: Frame sync low active 1'b1: Frame sync high active

SAI_TXFIFOLR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	tfl3 Transmit fifo3 level Contains the number of valid data entries in the transmit fifo3.
17:12	RO	0x00	tfl2 Transmit fifo2 level Contains the number of valid data entries in the transmit fifo2.
11:6	RO	0x00	tfl1 Transmit fifo1 level Contains the number of valid data entries in the transmit fifo1.
5:0	RO	0x00	tfl0 Transmit fifo0 level Contains the number of valid data entries in the transmit fifo0.

SAI_RXFIFOLR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	rfl3 Receive fifo3 level Contains the number of valid data entries in the receive fifo3.
17:12	RO	0x00	rfl2 Receive fifo2 level Contains the number of valid data entries in the receive fifo2.
11:6	RO	0x00	rfl1 Receive fifo1 level Contains the number of valid data entries in the receive fifo1.
5:0	RO	0x00	rfl0 Receive fifo0 level Contains the number of valid data entries in the receive fifo0.

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SAI_DMACR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	rde Receive DMA enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
23:21	RO	0x0	reserved
20:16	RW	0x00	rdl Receive data level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
15:9	RO	0x00	reserved
8	RW	0x0	tde Transmit DMA enable 1'b0: Transmit DMA disabled 1'b1: Transmit DMA enabled
7:5	RO	0x0	reserved
4:0	RW	0x00	tdl Transmit data level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the TX FIFO(TX FIFO0 if CSR=00;TX FIFO1 if CSR=01,TX FIFO2 if CSR=10,TX FIFO3 if CSR=11)is equal to or below this field value.

SAI_INTCR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RW	0x1f	rft Receive fifo threshold When the number of receive fifo entries is more than or equal to this threshold plus 1, the receive fifo full interrupt is triggered.
19	RO	0x0	reserved
18	WO	0x0	rxoic RX overrun interrupt clear Write 1 to clear RX overrun interrupt.
17	RW	0x0	rxoie RX overrun interrupt enable 1'b0: Disable 1'b1: Enable
16	RW	0x0	rxfie RX full interrupt enable 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8:4	RW	0x00	tft Transmit fifo threshold When the number of transmit fifo entries is less than or equal to this threshold, the transmit fifo empty interrupt is triggered.
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	W1C	0x0	txuic TX underrun interrupt clear Write 1 to clear TX underrun interrupt.
1	RW	0x0	txuie TX underrun interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	txeie TX empty interrupt enable 1'b0: Disable 1'b1: Enable

SAI_INTSR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	rxoi RX overrun interrupt 1'b0: Inactive 1'b1: Active
16	RO	0x0	rxfi RX full interrupt 1'b0: Inactive 1'b1: Active
15:2	RO	0x0000	reserved
1	RO	0x0	txui TX underrun interrupt 1'b0: Inactive 1'b1: Active
0	RO	0x0	txei TX empty interrupt 1'b0: Inactive 1'b1: Active

SAI_TXDR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdr Transmit fifo fata register When it is written, data are moved into the transmit fifo.

SAI_RXDR

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxdr Receive fifo data register When the register is read, data in the receive fifo is accessed.

SAI_PATH_SEL

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:22	RW	0x00	sdo_to_sdi_path_sel SDO_TO_SDI_PATH_SEL [23:22]:sdi0 sel sdo0 or sdo1 or sdo2 or sdo3 [25:24]:sdi1 sel sdo0 or sdo1 or sdo2 or sdo3 [27:26]:sdi2 sel sdo0 or sdo1 or sdo2 or sdo3 [29:28]:sdi3 sel sdo0 or sdo1 or sdo2 or sdo3
21:18	RW	0x0	loopback_bypass Loopback by pass enable bit Tx_sdo -> Rx_sdi loopback mode should work at fs_tx_as_common mode and tx=rx=master [18]:Loopback_en0 [19]:Loopback_en1 [20]:Loopback_en2 [21]:Loopback_en3 1'b0: No active 1'b1: Active
17	RW	0x0	sync_out_sel Tx sync out select bit 1'b0: Tx sclk and fs sync out use out signal 1'b1: Tx sclk and fs sync out use in signal
16	RW	0x0	sync_in_sel Tx sync in select bit 1'b0: Tx sclk and fs use pad signal 1'b1: Tx sclk and fs use sync input port
15:14	RW	0x3	rx_path_select3 Rx path select 2'b00: Path3 data from sdi0 2'b01: Path3 data from sdi1 2'b10: Path3 data from sdi2 2'b11: Path3 data from sdi3
13:12	RW	0x2	rx_path_select2 Rx path select 2'b00: Path2 data from sdi0 2'b01: Path2 data from sdi1 2'b10: Path2 data from sdi2 2'b11: Path2 data from sdi3
11:10	RW	0x1	rx_path_select1 Rx path select 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3
9:8	RW	0x0	rx_path_select0 Rx path select 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3
7:6	RW	0x3	tx_path_select3 TX path select 2'b00: Sdo3 output data from path0 2'b01: Sdo3 output data from path1 2'b10: Sdo3 output data from path2 2'b11: Sdo3 output data from path3

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Bit	Attr	Reset Value	Description
5:4	RW	0x2	tx_path_select2 TX path select 2'b00: Sdo2 output data from path0 2'b01: Sdo2 output data from path1 2'b10: Sdo2 output data from path2 2'b11: Sdo2 output data from path3
3:2	RW	0x1	tx_path_select1 TX path select 2'b00: Sdo1 output data from path0 2'b01: Sdo1 output data from path1 2'b10: Sdo1 output data from path2 2'b11: Sdo1 output data from path3
1:0	RW	0x0	tx_path_select0 TX path select 2'b00: Sdo0 output data from path0 2'b01: Sdo0 output data from path1 2'b10: Sdo0 output data from path2 2'b11: Sdo0 output data from path3

SAI_TX_SLOT_MASK0

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask0 Transmit slot 0~31 mask state slot 0~31 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK1

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask1 Transmit slot 32~63 mask state slot 32~63 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK2

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask2 Transmit slot 64~95 mask state slot 64~95 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK3

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask3 Transmit slot 96~127 mask state slot 96~127 mask state 0: Slot active 1: Slot mask,data is invalid

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SAI_RX_SLOT_MASK0

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask0 Receive slot 0~31 mask state Slot 0~31 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK1

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask1 Receive slot 32~63 mask state slot 32~63 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK2

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask2 Receive slot 64~95 mask state slot 64~95 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK3

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask3 Receive Slot 96~127 mask state slot 96~127 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_DATA_CNT

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	tx_data_cnt Tx data counter

SAI_RX_DATA_CNT

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data_cnt Rx data counter

SAI_SAI_TX_SHIFT

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:0	RW	0x000000	fs_shift Transfer frame sync pulse shift control 24'h00: Normal mode 24'h01: Fs 1/2 cycle shift left. 24'h02: Fs 1 cycle shift left. 24'h03: Fs 3/2 cycle shift left. .....

SAI_SAI_RX_SHIFT

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	fs_shift Transfer frame sync pulse shift control 24'h00: Normal mode 24'h01: Fs 1/2 cycle shift left. 24'h02: Fs 1 cycle shift left. 24'h03: Fs 3/2 cycle shift left. .....

SAI_TIMEOUT

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:1	RW	0x0000000	timeout_number set timeout number
0	RW	0x0	timeout_enable 1'b0: Stop timeout 1'b1: Start timeout

SAI_VERSION

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x20200520	sai_vertion SAI version

13.5 Interface Description

The following table shows the SAI0 interface description.

Table 13-1 SAI0 m0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s0_mclk	I/O	I2S0mclkm0/UART2ctsnm1/PDMclk1m0/VCCIO1GPIO3a2	GRF_GPIO3A_IOMUX_L[11:8]=1
i2s0_sclk	I/O	I2S0sclkm0/UART2rtsnm1/VCCIO1GPIO3a3	GRF_GPIO3A_IOMUX_L[15:12]=1
i2s0_lrck	I/O	I2S0lrckm0/PWM8m0/VCCIO1GPIO3a4	GRF_GPIO3A_IOMUX_H[3:0]=1
i2s0_sdo0	O	I2S0sdo0m0/PWM9m0/VCCIO1GPIO3a5	GRF_GPIO3A_IOMUX_H[7:4]=1
i2s0_sdo1/i2s0_sdi3	I/O	I2S0sdo1m0/I2S0sdi3m0/PDMclk0m0/PCIE20clkreqnm1/UART5txm1/VCCIO1GPIO3a6	GRF_GPIO3A_IOMUX_H[11:8]=1 GRF_GPIO3A_IOMUX_H[3:0]=2

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Module Pin	Direction	Pad Name	IOMUX Setting
i2s0_sdo2/i2s0_sdi2	I/O	I2S0sdo2m0/I2S0sdi2m0/PDMsdi2m0/PCIE20wakenm1/UART5rxm1/VCCIO1GPIO3a7	GRF_GPIO3A_IOMUX_H[15:12]=1 GRF_GPIO3A_IOMUX_H[15:12]=2
i2s0_sdo3/i2s0_sdi1	I/O	I2S0sdo3m0/I2S0sdi1m0/PDMsdi1m0/PCIE20perstnm1/VCCIO1GPIO3b0	GRF_GPIO3B_IOMUX_L[3:0]=1 GRF_GPIO3B_IOMUX_L[3:0]=2
i2s0_sdi0	I	I2S0sdi0m0/PDMsdi0m0/VCCIO1GPIO3b1	GRF_GPIO3B_IOMUX_L[7:4]=1

Table 13-2 SAI0 m1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s0_mclk	I/O	SDMMC1clk/RGMIIrxclkm1/I2S0mclkm1/PWM1m1/VCCIO4GPIO1c6	GRF_GPIO1C_IOMUX_H[11:8]=3
i2s0_sclk	I/O	SDMMC1cmd/RGMIIrxd3m1/I2S0sclkm1/PWM0m1/VCCIO4GPIO1c5	GRF_GPIO1C_IOMUX_H[7:4]=3
i2s0_lrck	I/O	SDMMC1d3/RGMIIrxd2m1/I2S0lrckm1/PWM11m1/VCCIO4GPIO1c4	GRF_GPIO1C_IOMUX_H[3:0]=3
i2s0_sdo0	O	SDMMC1d2/RGMIItxclkm1/I2S0sdo0m1/PWM10m1/VCCIO4GPIO1c3	GRF_GPIO1C_IOMUX_L[15:12]=3
i2s0_sdo1	O	UART1rxm0/RGMIItxd0m1/I2S0sdo1m1/PWM4m1/RMIItxd0/VCCIO4GPIO1d1	GRF_GPIO1D_IOMUX_L[7:4]=3
i2s0_sdo2	O	UART1txm0/RGMIItxd1m1/I2S0sdo2m1/PWM5m1/RMIItxd1/VCCIO4GPIO1d2	GRF_GPIO1D_IOMUX_L[11:8]=3
i2s0_sdo3	O	I2S2mclkm0/ETHclk25moutm1/CLK132kout/SPI2clkm1/I2S0sdo3m1/VCCIO4GPIO2a1	GRF_GPIO2A_IOMUX_L[7:4]=5
i2s0_sdi0	I	SDMMC1d0/RGMIItxd2m1/I2S0sdi0m1/PWM8m1/VCCIO4GPIO1c1	GRF_GPIO1C_IOMUX_L[7:4]=3
i2s0_sdi1	I	ISDMMC1d1/RGMIItxd3m1/I2S0sdi1m1/PWM9m1/VCCIO4GPIO1c2	GRF_GPIO1C_IOMUX_L[11:8]=3
i2s0_sdi2	I	UART1rtsnm0/RGMIItxenm1/I2S0sdi2m1/PWM6m1/RMIItxen/VCCIO4GPIO1d3	GRF_GPIO1D_IOMUX_L[15:12]=3
i2s0_sdi3	I	UART1ctsnm0/RGMIIrxd0m1/I2S0sdi3m1/PWM7m1/RMIIrxd0/VCCIO4GPIO1d4	GRF_GPIO1D_IOMUX_H[3:0]=3

Table 13-3 SAI1 m0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s1_mclk	I/O	VOlcdcd3/I2S1mclkm0/UART7txm0/VCCIO6GPIO3c4	GRF_GPIO3C_IOMUX_H[3:0]=2
i2s1_sclk	I/O	VOlcdcd4/I2S1sclkm0/UART4ctsnm0/PWM14m0/VCCIO6GPIO3c5	GRF_GPIO3C_IOMUX_H[7:4]=2
i2s1_lrck	I/O	VOlcdcd5/I2S1lrckm0/UART4rtsnm0/PWM15m0/VCCIO6GPIO3c6	GRF_GPIO3C_IOMUX_H[11:8]=2
i2s1_sdo0	O	VOlcdcd6/I2S1sdo0m0/UART7rxm0/VCCIO6GPIO3c7	GRF_GPIO3C_IOMUX_H[15:12]=2
i2s1_sdo1	O	VOlcdchsync/I2S1sdo1m0/UART9ctsnm0/SPI2csn1m0/I2C1sclm1/UART3txm0/VCCIO6GPIO4b4	GRF_GPIO4B_IOMUX_H[3:0]=2

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Module Pin	Direction	Pad Name	IOMUX Setting
i2s1_sdo2	O	VOlcdcvsync/I2S1sdo2m0/UART9rtsnm0/SPI2csn0m0/I2C1sdam1/UART3rxm0/VCCIO6GPIO4b5	GRF_GPIO4B_IOMUX_H[7:4]=2
i2s1_sdo3	O	VOlcdcden/I2S1sdo3m0/UART3ctsnm0/SPI2clkm0/VCCIO6GPIO4b6	GRF_GPIO4B_IOMUX_H[11:8]=2
i2s1_sdi0	I	VOlcdcd7/I2S1sdi0m0/UART4txm0/VCCIO6GPIO3d0	GRF_GPIO3D_IOMUX_L[3:0]=2
i2s1_sdi1	I	VOlcdcd10/I2S1sdi1m0/UART4rxm0/UART3rtsnm0/VCCIO6GPIO3d1	GRF_GPIO3D_IOMUX_L[7:4]=2
i2s1_sdi2	I	VOlcdcd11/I2S1sdi2m0/UART7ctsnm0/SPI2misom0/I2C2sclm1/VCCIO6GPIO3d2	GRF_GPIO3D_IOMUX_L[11:8]=2
i2s1_sdi3	I	VOlcdcd12/I2S1sdi3m0/UART7rtsnm0/SPI2mosim0/I2C2sdam1/VCCIO6GPIO3d3	GRF_GPIO3D_IOMUX_L[15:12]=2

Table 13-4 SAI1 m1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s1_mclk	I/O	I2S1mclkm1/CAMclk0outm0/UART8txm0/VCCIO5GPIO3b2	GRF_GPIO3B_IOMUX_L[11:8]=1
i2s1_sclk	I/O	I2S1sclkm1/CAMclk1outm0/UART8rxm0/VCCIO5GPIO3b3	GRF_GPIO3B_IOMUX_L[15:12]=1
i2s1_lrck	I/O	I2S1lrckm1/CAMclk2out/UART8ctsnm0/SPI0mosim1/PWM12m1/VCCIO5GPIO3b4	GRF_GPIO3B_IOMUX_H[3:0]=1
i2s1_sdo0	O	I2S1sdo0m1/CAMclk3out/UART8rtsnm0/SPI0clkm1/PWM13m1/VCCIO5GPIO3b5	GRF_GPIO3B_IOMUX_H[7:4]=1
i2s1_sdo1/i2s1_sdi3	I/O	I2S1sdo1m1/I2S1sdi3m1/UART3ctsnm1/SPI0csn1m1/I2C4sclm0/CAN0txm1/VCCIO5GPIO3b6	GRF_GPIO3B_IOMUX_H[11:8]=1 GRF_GPIO3B_IOMUX_H[11:8]=2
i2s1_sdo2/i2s1_sdi2	I/O	I2S1sdo2m1/I2S1sdi2m1/UART3txm1/SPI0csn0m1/I2C4sdam0/CAN0rxm1/VCCIO5GPIO3b7	GRF_GPIO3B_IOMUX_H[15:12]=1 GRF_GPIO3B_IOMUX_H[15:12]=2
i2s1_sdo3/i2s1_sdi1	I/O	I2S1sdo3m1/I2S1sdi1m1/UART3rxm1/SPI0misom1/VCCIO5GPIO3c0	GRF_GPIO3C_IOMUX_L[3:0]=1 GRF_GPIO3C_IOMUX_L[3:0]=2
i2s1_sdi0	I	I2S1sdi0m1/ISPflashtrigin/UART3rtsnm1/VCCIO5GPIO3c1	GRF_GPIO3C_IOMUX_L[7:4]=1

Table 13-5 SAI2 m0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s2_mclk	I/O	I2S2mclkm0/ETHclk25moutm1/CLK132kout/SPI2clkm1/I2S0sdo3m1/VCCIO4GPIO2a1	GRF_GPIO2A_IOMUX_L[7:4]=1
i2s2_sclk	I/O	I2S2sclkm0/RGMIIclkm1/UART4rxm1/SPI2csn1m1/RMIIclk/VCCIO4GPIO1d5	GRF_GPIO1D_IOMUX_H[7:4]=1
i2s2_lrck	I/O	I2S2lrckm0/RGMIIrxdvm1/UART4txm1/SPI2csn0m1/RMIIrxdvcrs/VCCIO4GPIO1d6	GRF_GPIO1D_IOMUX_H[11:8]=1
i2s2_sdo0	O	I2S2sdom0/RGMIIrxd1m1/UART4rtsnm1/SPI2mosim1/PWM14m1/RMIIrxd1/VCCIO4GPIO1d7	GRF_GPIO1D_IOMUX_H[15:12]=1

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Module Pin	Direction	Pad Name	IOMUX Setting
i2s2_sdi0	I	I2S2sdim0/RGMIIrxerm1/UART4ctsnm1/SPI2misom1/PWM15m1/RMIIrxer/VCCIO4GPIO2a0	GRF_GPIO2A_IOMUX_L[3:0]=1

Table 13-6 SAI2 m1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s2_mclk	I/O	VOlcdcd15/RGMIItxclkm0/I2S2mclkm1/SPI1clkm0/VCCIO6GPIO3d6	GRF_GPIO3D_IOMUX_H[11:8]=3
i2s2_sclk	I/O	VOlcdcd17/ETHclk25moutm0/CAMclk0outm1/I2S2sclkm1/PDMclk1m1/VCCIO6GPIO4b1	GRF_GPIO4B_IOMUX_L[7:4]=4
i2s2_lrck	I/O	VOlcdcd21/RGMIIrxclkm0/I2S2lrckm1/PWM12m0/VCCIO6GPIO4a1	GRF_GPIO4A_IOMUX_L[7:4]=3
i2s2_sdo0	O	VOlcdcd14/RGMIItxd3m0/UART8rxm1/I2S2sdom1/VCCIO6GPIO3d5	GRF_GPIO3D_IOMUX_H[7:4]=4
i2s2_sdi0	I	VOlcdcd13/RGMIItxd2m0/UART8txm1/I2S2sdim1/VCCIO6GPIO3d4	GRF_GPIO3D_IOMUX_H[3:0]=4

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13.6 Application Notes

13.6.1 Software Application Notes

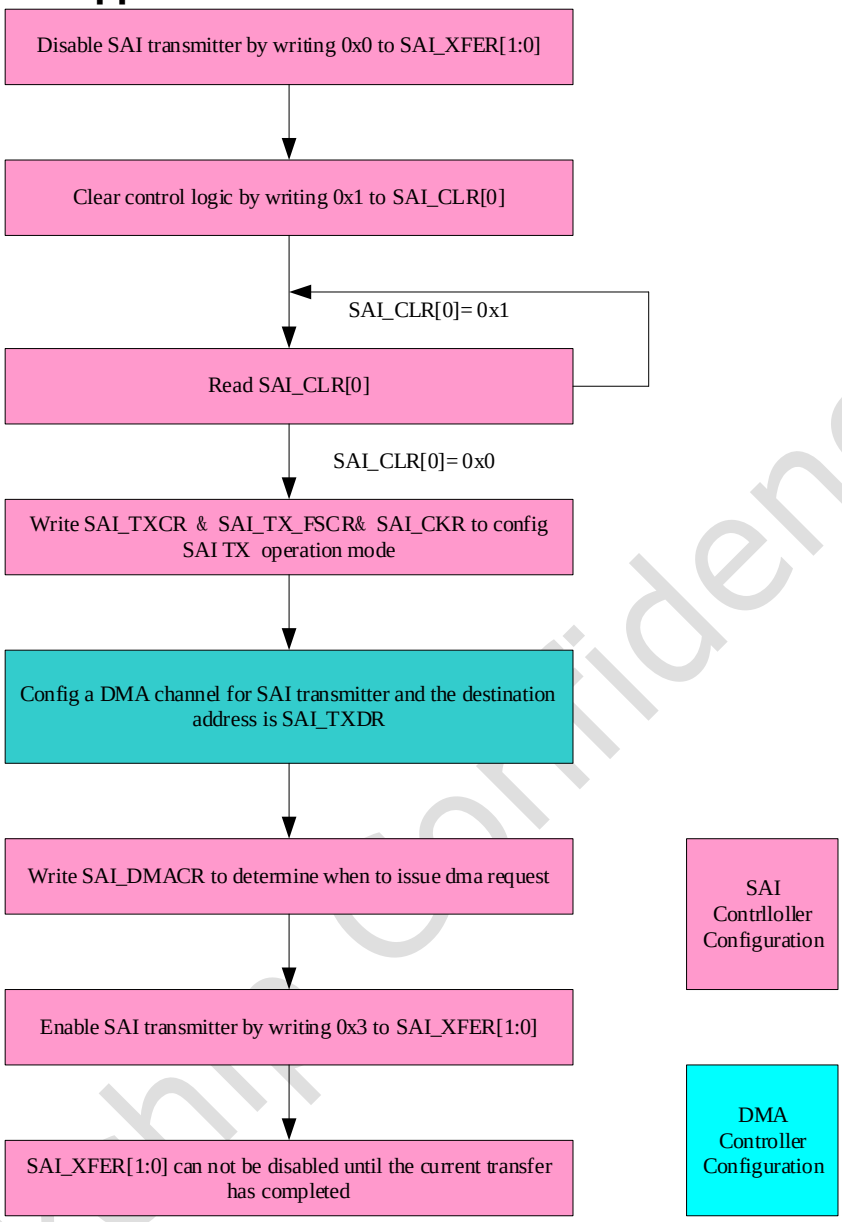

Fig.13-5 SAI controller transmit operation flow chart

Note: User should clear TX/RX logical by CLR[0]/CLR[1] and wait clear operation done before configure the other registers.

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Chapter 14 RK DSM

14.1 Overview

RK DSM is a 16-bit digital audio encoder which supports multiple sample rates. It is mainly composed of digital DAC. The aim of digital DAC is to process the data received from I2S/PCM interface through filters, volume control and modulation.
The RK DSM supports the following features.

- Support 8-bit APB and AHB bus slave interface
- Support 2-channel digital DAC
- Support I2S/PCM interface
- Support I2S/PCM master and slave mode
- Support 2-channel audio receiving in I2S mode
- Support 2-channel audio receiving in PCM mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and LRCK polarity
- Support 16 bit sample resolution
- Support programmable left and right channel exchangeable in I2S mode and PCM mode
- Support three modes of mixing for every digital DAC channel
- Support volume control
- Support programmable negative and positive volume gain

14.2 Block Diagram

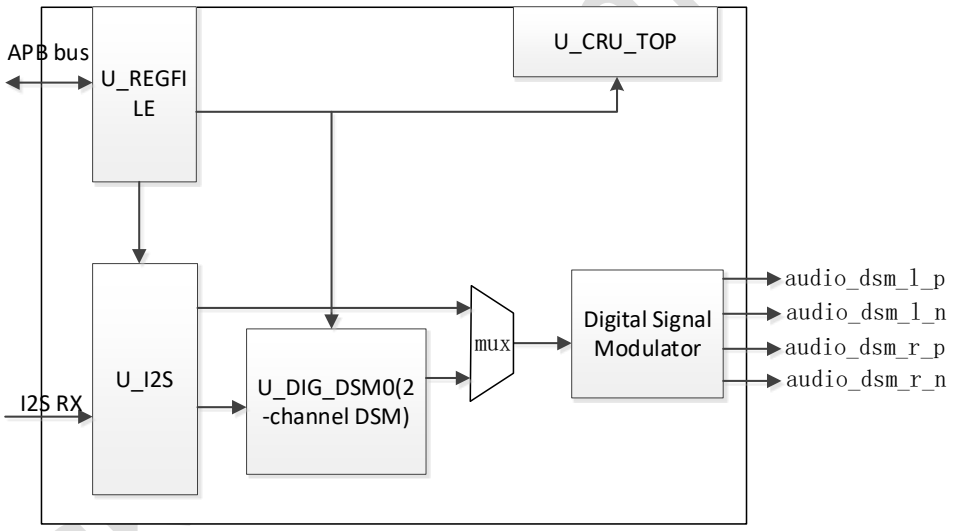

Fig.14-1 RK DSM Block Diagram

RK DSM_RF
The RK DSM_RF implements the 8-bit APB/AHB slave operation through APB/AHB bus. It is responsible for configuring the operation registers of other modules.
RK DSM_CRU
The RK DSM_CRU implements clock and reset generation function. It is responsible for generating sample clock, digital DAC operation clock and I2S operation clock.
RK DSM
There are 2 digital DAC channels. The digital DAC receives audio data from ACDC_I2S module. It includes one CIC filter, one high-pass filter, several low-pass decimation filters and other audio signal processing related modules. The output of digital DAC is sent to DSM modular before transmitting outside.
RK DSM_I2S
The I2S/PCM audio interface can be configured to master mode or slave mode. In Master Mode, SCLK and LRCK are configured as output. In slave mode, SCLK and LRCK are

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configured as input. The RK DSM_I2S module can only operate in RX mode. When in RX mode, it receives audio data from I2S RX interface and sends it to digital DAC.

DSM Modulator

It is a modulator that converts 16 bits audio sample data to 1 bit audio data.

14.3 Function description

The I2S/PCM interface of Digital Audio Codec is connected to the I2S1 controller. Please refer to the I2S chapter for detailed information about I2S and PCM format that Digital Audio Codec supports.

14.3.1 Filters of Digital DAC

I2S module receives two-channel audio data from I2S RX interface and drives it to the digital DAC which supports mixing function or directly to the DSM modulator. How to pour 2-channel audio data into 2-channel digital DAC can be achieved by programming mixing mode.

The 2-channel digital DAC includes a high-pass filter and a maximum of 5 half-band filters. The high-pass filter is used to filter DC components in audio data stream. Result of high-pass filter is sent to the digital DAC volume control module. The input of 5 half-band filters comes from output of volume control module with each perform 2-times interpolation. But not all of them are working all the time. How many of them are needed to work depends on the sample rate of digital DAC. The result of half-band filters is sent to a modulator.

14.3.2 Volume Control

For digital DAC, output of high-pass filters is fed into volume control module. The volume control module inside digital DAC contains several sub-modules such as peak detect, frequency cross zero detect, LIMITER and digital gain control. It can be digitally attenuated over a range of -96dB~0dB in 0.375dB/step for negative gain and amplified over a range of 0dB~96dB in 0.375dB/step for positive gain. Whether is attenuated or amplified can be software programmed.

14.4 Register Description

14.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

14.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKDSM_DSMVUCTL	0x0000	W	0x00000001	DAC Volume Control Register
RKDSM_DSMVUCTIME	0x0004	W	0x00000000	DAC Volume Control Time Limit Register
RKDSM_DSMDIGEN	0x0008	W	0x00000000	DAC Digital Enable Register
RKDSM_DSMCLKCTRL	0x000C	W	0x00000000	DAC Clock Control Register
RKDSM_DSMINTMOD_DIV	0x0014	W	0x00000007	DAC Integer Clock Divider Register
RKDSM_DSMINTSCLK_DIV	0x0020	W	0x0000001F	I2S SCLK RX Integer Divider Register
RKDSM_DSM_DIV	0x0024	W	0x00000003	PWM Mode Integer Divider Register
RKDSM_DSM_CTRL	0x0028	W	0x00000000	PWM Mode Control Register
RKDSM_DSMCFG1	0x0044	W	0x00000004	DAC Configure Register 1
RKDSM_DSMMUTE	0x0048	W	0x00000000	DAC Mute Control Register
RKDSM_DSMMUTEST	0x004C	W	0x00000000	DAC Mute Status Register
RKDSM_DSMVOLL0	0x0050	W	0x00000000	Volume of DAC Left Channel 0 Register
RKDSM_DSMVOLL1	0x0054	W	0x00000000	
RKDSM_DSMVOLL2	0x0058	W	0x00000000	
RKDSM_DSMVOLL3	0x005C	W	0x00000000	

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Name	Offset	Size	Reset Value	Description
RKDSM_DSMVOLR0	0x0060	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOLR1	0x0064	W	0x00000000	
RKDSM_DSMVOLR2	0x0068	W	0x00000000	
RKDSM_DSMVOLR3	0x006C	W	0x00000000	
RKDSM_DSMVOGP	0x0070	W	0x00000000	DAC Volume Gain Polarity Register
RKDSM_DSMRVOLL0	0x0074	W	0x000000FF	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLL1	0x0078	W	0x00000000	
RKDSM_DSMRVOLL2	0x007C	W	0x00000000	
RKDSM_DSMRVOLL3	0x0080	W	0x00000000	
RKDSM_DSMRVOLR0	0x0084	W	0x000000FF	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMRVOLR1	0x0088	W	0x00000000	
RKDSM_DSMRVOLR2	0x008C	W	0x00000000	
RKDSM_DSMRVOLR3	0x0090	W	0x00000000	
RKDSM_DSMLMT0	0x0094	W	0x00000000	DAC Limiter Register 0
RKDSM_DSMLMT1	0x0098	W	0x00000000	DAC Limiter Register 1
RKDSM_DSMLMT2	0x009C	W	0x00000000	DAC Limiter Register 2
RKDSM_DSMMIXCTRLL	0x00A0	W	0x00000000	DAC Mixing Control Register Of Left Channels
RKDSM_DSMMIXCTRLR	0x00A4	W	0x00000000	DAC Mixing Control Register Of right Channels
RKDSM_DSMHPF	0x00A8	W	0x00000000	DAC High-pass Filter Control Register
RKDSM_DSM_I2S_RXCR0	0x010C	W	0x0000000F	Receive Operation Control Register 0
RKDSM_DSM_I2S_RXCR1	0x0110	W	0x00000000	Receive Operation Control Register 1
RKDSM_DSM_I2S_CKR0	0x0114	W	0x00000000	Clock Generation Register 0
RKDSM_DSM_I2S_CKR1	0x0118	W	0x00000000	Clock Generation Register 1
RKDSM_DSM_I2S_XFER	0x011C	W	0x00000000	Transfer Start Register
RKDSM_DSM_I2S_CLR	0x0120	W	0x00000000	SCLK Domain Logic Clear Register
RKDSM_DSM_VERSION	0x0140	W	0x00000010	Version Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3 Detail Registers Description

RKDSM_DSMVUCTL

Address: Operational Base(0xFF850000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	dac_byps Digital DAC volume control bypass. 1'b0: Digital DAC volume control enable 1'b1: Digital DAC volume control bypass
1	RW	0x0	dacfade Digital DAC volume adjust mode. 1'b0: Update to new volume immediately. 1'b1: Update volume as daczdt field describes.

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Bit	Attr	Reset Value	Description
0	RW	0x1	daczdt Digital DAC volume cross zero detect enable. It works when dac_byps is 1'b0 and dacfade is 1'b1. 1'b0: Volume adjusts every sample. 1'b1: Volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets.

RKDSM_DSMVUCTIME

Address: Operational Base(0xFF850000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacvuct Volume control time limit, valid only in fade cross zero mode. Time limit = dacvuct*(1/sample rate) Unit: Sample rate

RKDSM_DSMDIGEN

Address: Operational Base(0xFF850000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	dacglben Global enable of all Digital DAC channels. Only when dacglben and the enable signal corresponding to each Digital DAC channel is valid before starting work. 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	dacen_l0r1 Digital DAC left channel 0 and right channel 1 enable. 1'b0: Disable 1'b1: Enable

RKDSM_DSMCLKCTRL

Address: Operational Base(0xFF850000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	dac_cke Digital DAC operation clock enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	i2srx_cke Clock enable of internal I2S RX channel. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cke_bclkrx Clock enable of sclk_out_rx. 1'b0: Disable 1'b1: Enable
2	RW	0x0	dac_sync_ena Enable of the synchronization signal used internally generated by Digital DAC. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RO	0x0	dac_sync_status There is a counter to generate synchronization signal of Digital DAC. In order to ensure the integrity of synchronization signal, it is necessary to read back dac_sync_status to judge whether the counter stops working when dac_sync_ena is set from 1'b1 to 1'b0. If the signal is read back to 1'b0, it means that the counter stops working and the synchronization signal of Digital DAC is complete.
0	RW	0x0	dac_mod_attenu_en When enabled, the input of the Digital DAC modulator is attenuated by 6dB, and the output of the Digital DAC modulator is increased by 6dB. 1'b0: Disable 1'b1: Enable

RKDSM_DSMINTMOD_DIV

Address: Operational Base(0xFF850000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x07	int_div_con Integer clock divider to provide 6.144/5.644/4.096MHz sample clock for internal filters. Make sure that int_div_con is an odd number between 7(8 times division) and 15(16 times division).

RKDSM_DSMINTSCLK_DIV

Address: Operational Base(0xFF850000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	sckrxdiv Integer clock divider to generate sclk_out_rx when I2S RX works in master mode. It is ignored when in slave mode. Sckrxdiv=((frequency of input operation clock)/(frequency of sclk_out_rx))-1. Sckrxdiv can be any value from 0 to 255.

RKDSM_DSM_DIV

Address: Operational Base(0xFF850000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	audio_pwm_div PWM mode division of Digital DAC's operation clock. The operation clock frequency of DSM module is equal to the input operation clock frequency of Digital DAC's divided by audio_pwm_div+1. It's recommended that audio_pwm_div is set 8'h3.

RKDSM_DSM_CTRL

Address: Operational Base(0xFF850000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	pwm_mode_cke Clock enable of 1-bit PWM modulator 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	pwm_mode Audio PWM mode selection 2'b01: Audio PWM mode 0. The input of 1-bit PWM modulator is from the last filter of Audio DAC. 2'b10: Audio PWM mode 1. The input of 1-bit PWM modulator is directly from output of I2S RX inside the ACDCDIG. Others: Reserved
3	RW	0x0	pwm_en 1-bit PWM modulator enable 1'b0: Disable 1'b1: Enable
2:0	RW	0x0	dith_sel Dith mode selection of 1-bit PWM modulator.

RKDSM_DSMCFG1

Address: Operational Base(0xFF850000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x1	dacsrt Sample rates of Digital DAC when in audio PWM mode 0. This field is ignored when in audio PWM mode 1. 3'b000: 12kHz/11.024kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 32kHz/48kHz/44.1kHz 3'b011: 96kHz/88.2kHz/64kHz 3'b100: 192kHz/176.4kHz/128kHz 3'b101~3'b111: Reserved
1:0	RO	0x0	reserved

RKDSM_DSMMUTE

Address: Operational Base(0xFF850000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dacunmt 1'b0: DAC normal mode 1'b1: DAC unmute mode. In this mode, DAC volume control block will adjust volume to match the value in DACVOLL* and DACVOLR*.
0	RW	0x0	dacmt 1'b0: DAC normal mode 1'b1: DAC mute mode

RKDSM_DSMMUTEST

Address: Operational Base(0xFF850000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	unmutest_l0r1 Unmute status for Digital DAC left channel 0 and right channel 1. When unmute is done, it indicates that internal volume is equal to the value programmed in DACVOLL* and DACVOLR*. 1'b0: Unmute not done 1'b1: Unmute done
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	mutest_l0r1 Mute status for Digital DAC left channel 0 and right channel 1. 1'b0: Not mute 1'b1: Mute

RKDSM_DSMVOLL0

Address: Operational Base(0xFF850000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv0 Volume of Digital DAC left channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL1

Address: Operational Base(0xFF850000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv1 Volume of Digital DAC left channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL2

Address: Operational Base(0xFF850000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	daclv2 Volume of Digital DAC left channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL3

Address: Operational Base(0xFF850000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	daclv3 Volume of Digital DAC left channel 3. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR0

Address: Operational Base(0xFF850000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacrv0 Volume of Digital DAC right channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR1

Address: Operational Base(0xFF850000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv1 Volume of Digital DAC right channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR2

Address: Operational Base(0xFF850000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv2 Volume of Digital DAC right channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR3

Address: Operational Base(0xFF850000) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv3 Volume of Digital DAC right channel 3. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOGP

Address: Operational Base(0xFF850000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	volgpr1 Gain polarity for the volume of Digital DAC right channel 1. 1'b0: Negative gain 1'b1: Positive gain
0	RW	0x0	volgpl0 Gain polarity for the volume of Digital DAC left channel 0. 1'b0: Negative gain 1'b1: Positive gain

RKDSM_DSMRVOLL0

Address: Operational Base(0xFF850000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvoll0 Internal real-time volume of Digital DAC left channel 0.

RKDSM_DSMRVOLL1

Address: Operational Base(0xFF850000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll1 Internal real-time volume of Digital DAC left channel 1.

RKDSM_DSMRVOLL2

Address: Operational Base(0xFF850000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll2 Internal real-time volume of Digital DAC left channel 2.

RKDSM_DSMRVOLL3

Address: Operational Base(0xFF850000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll3 Internal real-time volume of Digital DAC left channel 3.

RKDSM_DSMRVOLR0

Address: Operational Base(0xFF850000) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvolr0 Internal real-time volume of Digital DAC right channel 0.

RKDSM_DSMRVOLR1

Address: Operational Base(0xFF850000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr1 Internal real-time volume of Digital DAC right channel 1.

RKDSM_DSMRVOLR2

Address: Operational Base(0xFF850000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr2 Internal real-time volume of Digital DAC right channel 2.

RKDSM_DSMRVOLR3

Address: Operational Base(0xFF850000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr3 Internal real-time volume of Digital DAC right channel 3.

RKDSM_DSMLMT0

Address: Operational Base(0xFF850000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	limen LIMITER enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	limdct Limiter detect mode. 1'b0: (Left channel + right channel)/2 1'b0: Left channel or right channel independently

RKDSM_DSMLMT1

Address: Operational Base(0xFF850000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	atk_rate LIMITER attack rate=(power(2, atk_rate)*(8*clk)), clk is such as 4.096Mhz, 5.6448Mhz, 6.144Mhz.
3:0	RW	0x0	rls_rate LIMITER release rate=(power(2, rls_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz.

RKDSM_DSMLMT2

Address: Operational Base(0xFF850000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	max_lilmt The highest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step
3	RO	0x0	reserved
2:0	RW	0x0	min_lilmt The lowest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step

RKDSM_DSMMIXCTRLL

Address: Operational Base(0xFF850000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_l0 Digital DAC left channel 0 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

RKDSM_DSMMIXCTRLR

Address: Operational Base(0xFF850000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_r0 Digital DAC right channel 1 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

RKDSM_DSMHPF

Address: Operational Base(0xFF850000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	hpfcf High-pass filter control. 2'b00: 80Hz 2'b01: 100Hz 2'b10: 120Hz 2'b11: 140Hz
3:1	RO	0x0	reserved
0	RW	0x0	hpfen_l0r1 High-pass filter enable for left channel 0 and right channel 1. 1'b0: High-pass filter is disabled. 1'b1: High-pass filter is enabled.

RKDSM_DSM_I2S_RXCR0

Address: Operational Base(0xFF850000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	pbm PCM bus mode 2'b00: PCM no delay mode 2'b01: PCM delay 1 mode 2'b10: PCM delay 2 mode 2'b11: PCM delay 3 mode
5	RW	0x0	tfs Transfer format select 1'b0: I2S format 1'b1: PCM format
4:0	RW	0x0f	vdw Valid data width 5'b00000~5'b01110: Reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit ..... 5'b11100: 29bit 5'b11101: 30bit 5'b11110: 31bit 5'b11111: 32bit

RKDSM_DSM_I2S_RXCR1

Address: Operational Base(0xFF850000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	rcsr Channel select 2'b00: Two channel Others: Reserved
5	RO	0x0	reserved
4	RW	0x0	cex Exchange left channel and right channel in the every receive line. 1'b0: Not exchange 1'b1: Exchange
3	RO	0x0	reserved
2	RW	0x0	fbm First bit mode 1'b0: MSB 1'b1: LSB
1:0	RW	0x0	ibm I2S bus mode 2'b00: I2S normal 2'b01: I2S Left justified 2'b10: I2S Right justified 2'b11: Reserved

RKDSM_DSM_I2S_CKR0

Address: Operational Base(0xFF850000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	rsd I2S rx sclk divider for rx_lrck generator. 2'b00: 64 2'b01: 128 2'b10~2'b11: 256
1:0	RO	0x0	reserved

RKDSM_DSM_I2S_CKR1

Address: Operational Base(0xFF850000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	mss Master/slave mode select 1'b0: Master mode(sclk output) 1'b1: Slave mode(sclk input)
2	RW	0x0	ckp Sclk polarity 1'b0: Sample data at posedge sclk and drive data at negedge sclk. 1'b1: Sample data at negedge sclk and drive data at posedge sclk.
1	RW	0x0	rlp 1'b0: Normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal: high valid) 1'b1: Opposite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal: low valid)
0	RO	0x0	reserved

RKDSM_DSM_I2S_XFER

Address: Operational Base(0xFF850000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
0	RO	0x0	reserved

RKDSM_DSM_I2S_CLR

Address: Operational Base(0xFF850000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxc This is a self-cleared bit. Write 1'b1 to clear all receive logic. This bit can be set only when rxs is 1'b0. After writing rxc to 1'b1, wait until rxc become 1'b0 by polling rxc.
0	RO	0x0	reserved

RKDSM_DSM_VERSION

Address: Operational Base(0xFF850000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x10	ver Version of DSM.

14.5 Interface Description

The I2S RX interface of Digital Audio Codec is connected to the TX interface of I2S1 when GRF_AUDIO_CON[14] is set to 1'b1.
When operating in audio PWM mode 0 or 1, Digital Audio Codec outputs two pairs of differential signals encoded in PWM format. The following table shows the RK DSM interface description for audio PWM mode.

Table 14-1 Digital Audio Codec Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
AUDIO_DSM_L_P	O	SDMMC0d0/UART0rxm1/UART7rxm1/SPI1mosim1/DSMaudlp/VCCIO3GPIO1b3	GRF_GPIO1B_IOMUX_L[15:12]=5
AUDIO_DSM_L_N	O	SDMMC0d1/UART0txm1/UART7txm1/SPI1misom1/DSMaudln/VCCIO3GPIO1b4	GRF_GPIO1B_IOMUX_H[3:0]=5
AUDIO_DSM_R_P	O	SDMMC0d2/JTAGcpumcutckm1/UART5ctsnm0/SPI1csn1m1/PWM10m0/DSMaudrp/VCCIO3GPIO1b5	GRF_GPIO1B_IOMUX_H[7:4]=6
AUDIO_DSM_R_N	O	SDMMC0d3/JTAGcpumcutmsm1/UART5rtsnm0/SPI1csn0m1/PWM11m0/DSMaudrn/VCCIO3GPIO1b6	GRF_GPIO1B_IOMUX_H[11:8]=6

14.6 Application Notes

14.6.1 Software Application Notes

Steps to configure Digital DAC to work in audio PWM mode 0 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program DSMINTMOD_DIV to 0x07.
3. Program DSMCLKCTRL to 0x3d.
4. Program DSMINTSCLK_DIV if Digital DAC I2S RX acts as master.
5. Program DSMPWM_CTRL to 0x58.
6. Program DSM_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S RX related registers.
7. Program DSM_I2S_CLR to clear RX logic.
8. Program DSM_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
9. Program GRF_AUDIO_CON[14] to 1'b1 and program registers of I2S1 that is connected to Digital Audio Codec. Don't start transfer at this time.
10. Program DAC related registers such as DSMHPF, DSMVUCTL and DSMCFG1 to achieve basic configuration.
11. Program ACDCDIG_I2S_XFER to start I2S RX.
12. Program registers of I2S1 outside Digital Audio Codec to start TX.
13. Program DSMDIGEN to enable digital DAC channels. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio PWM mode 0 transfer are as follows.
1. Program registers of I2S1 to stop TX and ACDCDIG_I2S_XFER to stop RX.
2. Program DSMPWM_CTRL to 0x0.
3. Program DSMDIGEN to disable digital DAC channels.
4. Program DSMCLKCTRL to 0x0. Wait DSMCLKCTRL.dac_sync_status until read back to be 1'b0.

Steps to configure Digital DAC to work in audio PWM mode 1 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program DSMCLKCTRL to 0x3d.
3. Program DSMSCLKRXINT_DIV if Digital DAC I2S RX acts as master.

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4. Program DSMPWM_CTRL to 0x68.
5. Program DSM_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S RX related registers.
6. Program DSM_I2S_CLR to clear RX logic.
7. Program DSM_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
8. Program GRF_AUDIO_CON[14] to 1'b1 and program registers of I2S1 to start TX.
9. Program DSM_I2S_XFER to start I2S RX. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio PWM mode 1 transfer are as follows.

1. Program registers of I2S1 to stop TX and DSM_I2S_XFER to stop RX.
2. Program DSMPWM_CTRL to 0x0.
3. Program DSMCLKCTRL to 0x0. Wait DSMCLKCTRL.dac_sync_status until read back to be 1'b0.

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Chapter 15 Flexible Serial Peripheral Interface（FSPI）

15.1 Overview

The FSPI is a flexible serial peripheral interface host controller to interface with external device.

The FSPI supports the following features:

- Support various vendor devices with flexible command sequencer engine
  - Serial NOR Flash
  - Serial NAND Flash
  - Serial pSRAM
  - Serial SRAM
- Support SDR mode
- Support Single/Dual/Quad IO mode
- Support a 32-bit AHB slave to read and write controller register bank and initiate command sequence, including transfer data from/to external device indirectly
- Support a 32-bit AHB master with embedded DMA engine to transfer data from/to external device indirectly
- Support independent clock for system bus HCLK and controller core SCLK
- Support maskable interrupts generation
- Support sampling clock with optionally configurable delay line
- Support 2 CS# operation

15.2 Block Diagram

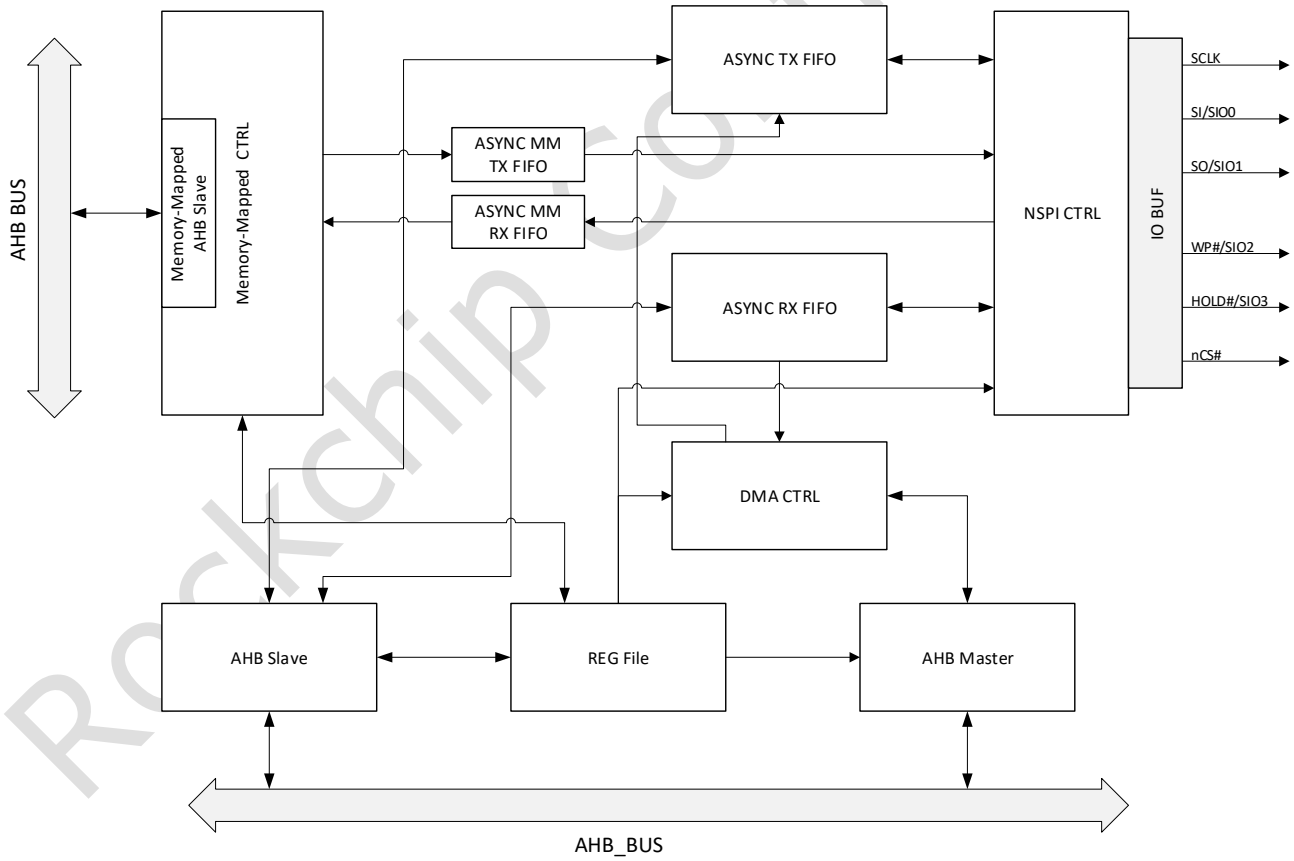

Fig. 15-1FSPI Architecture

Memory-Mapped AHB slave is available when XIP feature is present. In current chip, this feature is not provided.

15.3 Function Description

15.3.1 AHB Slave

The AHB slave block is used to configure the register of controller to generate flexible

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command sequence, process the interrupt exception, target various device feature and AC timing specification. It is also used to write CMD/ADDR/DATA to TX FIFO and read DATA from RX FIFO which buffer the DATA from external device.

15.3.2 AHB Master

When the embedded DMA CTRL is used to transfer DATA, the AHB master is used to transfer data to other system region, such as internal SRAM, peripheral, external DRAM.

15.3.3 REG File

The REG File is configurable register bank to control the store the static configuration and dynamic status of controller.

15.3.4 DMA CTRL

A block takes responsible for splitting a long length transfer trans into AHB bus transaction and interfacing with ASYNC TX or RX FIFO.

15.3.5 FIFO

There are four FIFO in the FSPI controller. ASYNC TX FIFO and ASYNC RX FIFO is for normal transaction that initiated by command sequence driver. The ASYNC MM (Memory-Mapped) TX FIFO and ASYNC MM (Memory-Mapped) RX FIFO is only used to buffer DATA from or to external device initiated by system bus master directly.

15.3.6 NSPI CTRL

Sequence decode engine which generates specialized timing sequence for various device. The NSPI decode the transaction from TX FIFO and Memory-Mapped Controller and convert it to relative CMD/ADDR/DATA frame based on the configuration.

15.4 Register Description

15.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

15.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
FSPI_CTRL0	0x0000	W	0x00000000	Control Register for CS0 Device
FSPI_IMR	0x0004	W	0x000001FF	Interrupt Mask Register
FSPI_ICLR	0x0008	W	0x00000000	Interrupt Clear Register
FSPI_FTLR	0x000C	W	0x00001010	FIFO Threshold Level Register
FSPI_RCVR	0x0010	W	0x00000000	FSPI Recover Register
FSPI_AX0	0x0014	W	0x00000000	FSPI Auxiliary Data Value for CS0 Device
FSPI_ABIT0	0x0018	W	0x00000000	Extend Address Bits for CS0 Device
FSPI_ISR	0x001C	W	0x00000000	Interrupt Status
FSPI_FSR	0x0020	W	0x00000001	FIFO Status Register
FSPI_SR	0x0024	W	0x00000000	FSPI Status Register
FSPI_RISR	0x0028	W	0x00000000	Raw Interrupt Status Register
FSPI_VER	0x002C	W	0x00000008	Version Register
FSPI_QOP	0x0030	W	0x00000000	Quad Line Operation IO Level Pre-set Register
FSPI_EXT_CTRL	0x0034	W	0x00004023	Extend Control Register
FSPI_DLL_CTRL0	0x003C	W	0x00000001	Delay Line Control Register for CS0 Device
FSPI_EXT_AX	0x0044	W	0x0000F0FF	Extend Auxiliary Data Control Register
FSPI_SCLK_INATM_CNT	0x0048	W	0xFFFFFFFF	SCLK Inactive Timeout Counter
FSPI_XMMC_WCMD0	0x0050	W	0x00000000	Memory Mapped Control Write Command Register for CS0 Device
FSPI_XMMC_RCMD0	0x0054	W	0x00000000	Memory Mapped Control Read Command Register for CS0 Device

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Name	Offset	Size	Reset Value	Description
FSPI_XMMC_CTRL	0x0058	W	0x000072E0	Memory Mapped Control Register
FSPI_MODE	0x005C	W	0x00000000	Controller Working Mode Register
FSPI_DEVRGN	0x0060	W	0x00000017	Device Region Size Register
FSPI_DEVSIZE0	0x0064	W	0x00000012	Device Size Register for CS0 Device
FSPI_TME0	0x0068	W	0x00000000	Timeout Enable Control Register for CS0 Device
FSPI_XMMC_RX_WTMRK	0x0070	W	0x00000002	Memory Mapped Mode Receiver FIFO Water Mark Register
FSPI_DMATR	0x0080	W	0x00000000	DMA Trigger Register
FSPI_DMAADDR	0x0084	W	0x00000000	DMA Address Register
FSPI_LEN_CTRL	0x0088	W	0x00000000	Length Control Register
FSPI_LEN_EXT	0x008C	W	0x00000000	Length Extended Register
FSPI_XMMCSR	0x0094	W	0x00000000	Memory Mapped Status Register
FSPI_CMD	0x0100	W	0x00000000	Indirect Command Register
FSPI_ADDR	0x0104	W	0x00000000	Address Register
FSPI_DATA	0x0108	W	0x00000000	Data Register
FSPI_CTRL1	0x0200	W	0x00000000	Control Register for CS1 Device
FSPI_AX1	0x0214	W	0x00000000	FSPI Auxiliary Data Value for CS1 Device
FSPI_ABIT1	0x0218	W	0x00000000	Extend Address Bits for CS1 Device
FSPI_DLL_CTRL1	0x023C	W	0x00000001	Delay Line Control Register for CS1 Device
FSPI_XMMC_WCMD1	0x0250	W	0x00000000	Memory Mapped Control Write Command Register for CS1 Device
FSPI_XMMC_RCMD1	0x0254	W	0x00000000	Memory-Mapped Command Control Register for CS1 Device
FSPI_DEVSIZE1	0x0264	W	0x00000012	Device Size Register for CS1 Device
FSPI_TME1	0x0268	W	0x00000000	Timeout Enable Control Register for CS1 Device

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

15.4.3 Detail Registers Description

FSPI_CTRL0

Address: Operational Base(0xFF860000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this ADRB to match the CMD sequence before doing indirect

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Bit	Attr	Reset Value	Description
			access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3:2	RO	0x0	reserved
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_IMR

Address: Operational Base(0xFF860000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	DMAM DMA Finish Interrupt Mask 1'b0: DMA finish interrupt is not masked 1'b1: DMA finish interrupt is masked Only valid in indirect access mode.
6	RW	0x1	NSPIM NSPI Interrupt Mask 1'b0: NSPI interrupt is not masked 1'b1: NSPI interrupt is masked Valid in indirect access mode and memory mapped mode.
5	RW	0x1	AHBM AMBA AHB Error Interrupt Mask 1'b0: AMBA AHB Error interrupt is not masked 1'b1: AMBA AHB Error interrupt is masked Only valid in indirect access mode.

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Bit	Attr	Reset Value	Description
4	RW	0x1	TRANSM Transfer Finish Interrupt Mask 1'b0: Transfer finish interrupt is not masked 1'b1: Transfer finish interrupt is masked Only valid in indirect access mode.
3	RW	0x1	TXEM Transmit FIFO Empty Interrupt Mask 1'b0: Transmit FIFO empty interrupt is not masked 1'b1: Transmit FIFO empty interrupt is masked Only valid in indirect access mode.
2	RW	0x1	TXOM Transmit FIFO Overflow Interrupt Mask 1'b0: Transmit FIFO overflow interrupt is not masked 1'b1: Transmit FIFO overflow interrupt is masked Only valid in indirect access mode.
1	RW	0x1	RXUM Receive FIFO Underflow Interrupt Mask 1'b0: Receive FIFO underflow interrupt is not masked 1'b1: Receive FIFO underflow interrupt is masked Only valid in indirect access mode.
0	RW	0x1	RXFM Receive FIFO Full Interrupt Mask 1'b0: Receive FIFO full interrupt is not masked 1'b1: Receive FIFO full interrupt is masked Only valid in indirect access mode.

FSPI_ICLR

Address: Operational Base(0xFF860000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	DMAC DMA Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the DMAS
6	W1C	0x0	NSPIC NSPI Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the NSPIS.
5	W1C	0x0	AHBC AMBA AHB Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the AHBS.
4	W1C	0x0	TRANSC Transfer Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TRANSS.
3	W1C	0x0	TXEC Transmit FIFO Empty Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXES.

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Bit	Attr	Reset Value	Description
2	W1C	0x0	TXOC Transmit FIFO Overflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXOS.
1	W1C	0x0	RXUC Receive FIFO Underflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXUS.
0	W1C	0x0	RXFC Receive FIFO Full Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXFS.

FSPI_FTLR

Address: Operational Base(0xFF860000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x10	RXFTLR Receive FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of receive FIFO entries is bigger than or equal to this value, the receive FIFO full interrupt is triggered.
7:0	RW	0x10	TXFTLR Transmit FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

FSPI_RCVR

Address: Operational Base(0xFF860000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	R/WSC	0x0	RCVR FSPI Recover Write any values to trigger the recovery of SMC NSPI state machine, FIFO state and other logic state.

FSPI_AX0

Address: Operational Base(0xFF860000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT0

Address: Operational Base(0xFF860000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	ABIT Address Bits Extend 5'h0: 1 bit 5'h1: 2 bits ... 5'h1f: 32 bits Only valid when ADDRB is set to 2'b11.

FSPI_ISR

Address: Operational Base(0xFF860000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
6	RO	0x0	NSPIS NSPI Transaction Decode Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
0	RW	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

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Address: Operational Base(0xFF860000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	RXWLVL RX FIFO Water Level 5'h0: FIFO is empty 5'h1: 1 entry is taken ... 5'h10: 16 entry is taken, FIFO is full
15:13	RO	0x0	reserved
12:8	RO	0x00	TXWLVL TX FIFO Water Level 5'h0: FIFO is full 5'h1: 1 entry is left ... 5'h10: 16 entry is left, FIFO is empty
7:4	RO	0x0	reserved
3	RO	0x0	RXFS Receive FIFO Full Status 1'b0: RX FIFO is not full 1'b1: RX FIFO is full
2	RO	0x0	RXES Receive FIFO Empty Status 1'b0: RX FIFO is not empty 1'b1: RX FIFO is empty
1	RO	0x0	TXES Transmit FIFO Empty Status 1'b0: TX FIFO is not empty 1'b1: TX FIFO is empty
0	RO	0x1	TXFS Transmit FIFO Full Status 1'b0: TX FIFO is not full 1'b1: TX FIFO is full

FSPI_SR

Address: Operational Base(0xFF860000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	SR Status Register 1'b0: NSPI Controller is idle 1'b1: NSPI Controller is busy When controller is busy, don't change the setting of control register. When NSPI is idle, the software can initiate new transaction to external device.

FSPI_RISR

Address: Operational Base(0xFF860000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

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Bit	Attr	Reset Value	Description
6	RO	0x0	NSPIS NSPI Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
0	RO	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

FSPI_VER

Address: Operational Base(0xFF860000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0008	VER The Version ID of FSPI

FSPI_QOP

Address: Operational Base(0xFF860000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	SO123BP SO123 Bypass Mode 1'b0: Disable bypass 1'b1: Enable bypass Default is enabled.
0	RW	0x0	SO123 D1/D2/D3 Data Value During Inactive When CS is Active 1'b0: Set to "0" 1'b1: Set to "1" The value of SO1, SO2 and SO3 during command and address bits input.

FSPI_EXT_CTRL

Address: Operational Base(0xFF860000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	SR_GEN_MODE Status Register Generation Mode 1'b0: Compatible mode with old controller 1'b1: Robust generation to indicates the status of controller If set to "1", the controller will only clear the SR bit after operation sequence done and CS is high.
13	RW	0x0	TRANS_INT_MODE Transmit Done Interrupt Generation Mode 1'b0: Trigger NSPI end in data done 1'b1: Trigger NSPI end in CS inactive Default Generation is compatible with old controller.
12	RO	0x0	reserved
11:8	RW	0x0	SWITCH_IO_O2I_CNT Switch IO Attribute Cycles in O2I Idle Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in O2I idle phase.
7:4	RW	0x2	SWITCH_IO_DUMM_CNT Switch IO Attribute Cycles in Dummy Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in Dummy data phase.
3:0	RW	0x3	CS_DESEL_CTRL CS Inactive Control 4'h0: Not support 4'h1: 2 cycles 4'h2: 3 cycles 4'h3: 4 cycles ... 4'hf: 16 cycles

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Bit	Attr	Reset Value	Description
			The target cycles to hold CS inactive after de-assert the CS. Default value are 4 SCLK cycles that is enough for normal device.

FSPI_DLL_CTRL0

Address: Operational Base(0xFF860000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	SCLK_SMP_SEL SCLK Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_EXT_AX

Address: Operational Base(0xFF860000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xf0	AX_SETUP_PAT Auxiliary Setup Data Pattern The AX data pattern that setup the continuous/enhance/XIP read mode
7:0	RW	0xff	AX_CANCEL_PAT Auxiliary Cancel Data Pattern The AX data pattern that cancel the continuous/enhance/XIP read mode.

FSPI_SCLK_INATM_CNT

Address: Operational Base(0xFF860000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	SCLK_INATM_CNT SCLK Inactive Timeout Counter When CS is active and SCLK is hold in high or low due to TX FIFO is empty or RX FIFO is full, if SCLK_INATM_EN is enabled, and timeout occurs, the controller will go back to idle and RX FIFO is flushed.

FSPI_XMMC_WCMD0

Address: Operational Base(0xFF860000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits

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Bit	Attr	Reset Value	Description
			2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD0

Address: Operational Base(0xFF860000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_CTRL

Address: Operational Base(0xFF860000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x1	PFT_EN Prefetch Enable 1'b0: Disable 1'b1: Enable Should disable prefetch if controller communicate with pSRAM which need refresh.
5	RW	0x1	DEV_HWEN Device AMBA AHB HWRITE Enable 1'b0: Disable 1'b1: Enable
4:0	RO	0x00	reserved

FSPI_MODE

Address: Operational Base(0xFF860000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	XMMC_MODE_EN Memory Mapped Mode Enable 1'b0: Disable, indirect access mode 1'b1: Enable, Memory-Mapped mode Before switching from indirect access mode to Memory-Mapped mode, the application should make sure the controller is in idle state and no pending transaction. If switch from Memory-Mapped to indirect access mode, software should initiate a dummy read by CPU before that.

FSPI_DEVRGN

Address: Operational Base(0xFF860000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DEC_CTRL Decode Control 2'b00: 1 CS# 2'b01: 2 CS# 2'b10: 4 CS# 2'b11: Reserved Only valid in XMMC mode.
7:5	RO	0x0	reserved
4:0	RW	0x17	RSIZE Region Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes In Memory-Mapped mode, the CS is controlled by AHB address bus, region size is used to generate CS.

FSPI_DEVSIZE0

Address: Operational Base(0xFF860000) + offset (0x0064)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G byte Device size is used to generate slop over status.

FSPI_TME0

Address: Operational Base(0xFF860000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

FSPI_XMMC_RX_WTMRK

Address: Operational Base(0xFF860000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	RX_FULL_WTMRK Memory Mapped Mode Receiver FIFO Water Mark. Default is enough.

FSPI_DMATR

Address: Operational Base(0xFF860000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	DMATR DMA Trigger Write "1" to start the DMA transfer.

FSPI_DMAADDR

Address: Operational Base(0xFF860000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAADDR DMA Address The destination or source data address in current system.

FSPI_LEN_CTRL

Address: Operational Base(0xFF860000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	TRB_SEL Total Transfer Bytes Selection 1'b0: TRB controlled by CMD[TRB] 1'b1: TRB controlled by LEN_EXT

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FSPI_LEN_EXT

Address: Operational Base(0xFF860000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRB_EXT Total Transfer Bytes Extended 32'd0: No data 32'd1: 1 Byte 32'd2: 2 Bytes ... Total data bytes number that will write to /read from the device.

FSPI_XMMCSR

Address: Operational Base(0xFF860000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/WSC	0x0	SLOPOVER1 Slop Over Register for CS1 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.
0	R/WSC	0x0	SLOPOVER0 Slop Over Register for CS0 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.

FSPI_CMD

Address: Operational Base(0xFF860000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	WO	0x0	CS Device Chip Select. 2'b00: Chip select 0 2'b01: Chip select 1 2'b10: Reserved 2'b11: Reserved
29:16	WO	0x0000	TRB Total Transfer Bytes 14'd0: No data 14'd1: 1 Byte 14'd2: 2 Bytes ... Total data bytes number that will write to or read from the device.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in indirect access mode. If there is not address command to send, set to zero.

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Bit	Attr	Reset Value	Description
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	WO	0x0	WR Write or Read 1'b0: Read 1'b1: Write
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in indirect access mode.
7:0	WO	0x00	CMD Command Command data in indirect access mode.

FSPI_ADDR

Address: Operational Base(0xFF860000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ADDR Address Register Indirect access start address data for current command sequence.

FSPI_DATA

Address: Operational Base(0xFF860000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DATA Data Register Device data read or write from/to device.

FSPI_CTRL1

Address: Operational Base(0xFF860000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this ADRB to match the CMD sequence before doing indirect

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Bit	Attr	Reset Value	Description
			access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3:2	RO	0x0	reserved
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_AX1

Address: Operational Base(0xFF860000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT1

Address: Operational Base(0xFF860000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	ABIT Address Bits Extend 5'h0: 1 bit 5'h1: 2 bits ... 5'h1f: 32 bits Only valid when ADDRB is set to 2'b11.

FSPI_DLL_CTRL1

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Address: Operational Base(0xFF860000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	SCLK_SMP_SEL SCLK sampling selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_XMMC_WCMD1

Address: Operational Base(0xFF860000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD1

Address: Operational Base(0xFF860000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_DEVSIZE1

Address: Operational Base(0xFF860000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes Device size is used to generate slop over status.

FSPI_TME1

Address: Operational Base(0xFF860000) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

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15.5 Interface Description

Table 15-1FSPI Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sfc_sclk	O	EMMC_CLK/FSPI_CLK/GPIO1_B1_d	GPIO1_IOC_GPIO1B_IOMUX_SEL_L[7:4]=4'h2
sfc_cs0n	O	EMMC_CMD/FSPI_CSN0/GPIO1_B0_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_L[3:0]=4'h2
sfc_cs1n	O	EMMC_STRB/FSPI_CSN1/GPIO1_B2_d	GPIO1_IOC_GPIO1B_IOMUX_SEL_L[11:8]=4'h2
sfc_sio0	I/O	EMMC_D0/FSPI_D0/GPIO1_A0_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_L[3:0]=4'h2
sfc_sio1	I/O	EMMC_D1/FSPI_D1/GPIO1_A1_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_L[7:4]=4'h2
sfc_sio2	I/O	EMMC_D2/FSPI_D2/GPIO1_A2_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4'h2
sfc_sio3	I/O	EMMC_D3/FSPI_D3/GPIO1_A3_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

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15.6 Application Notes

15.6.1 Typical Program Flow Without DMA

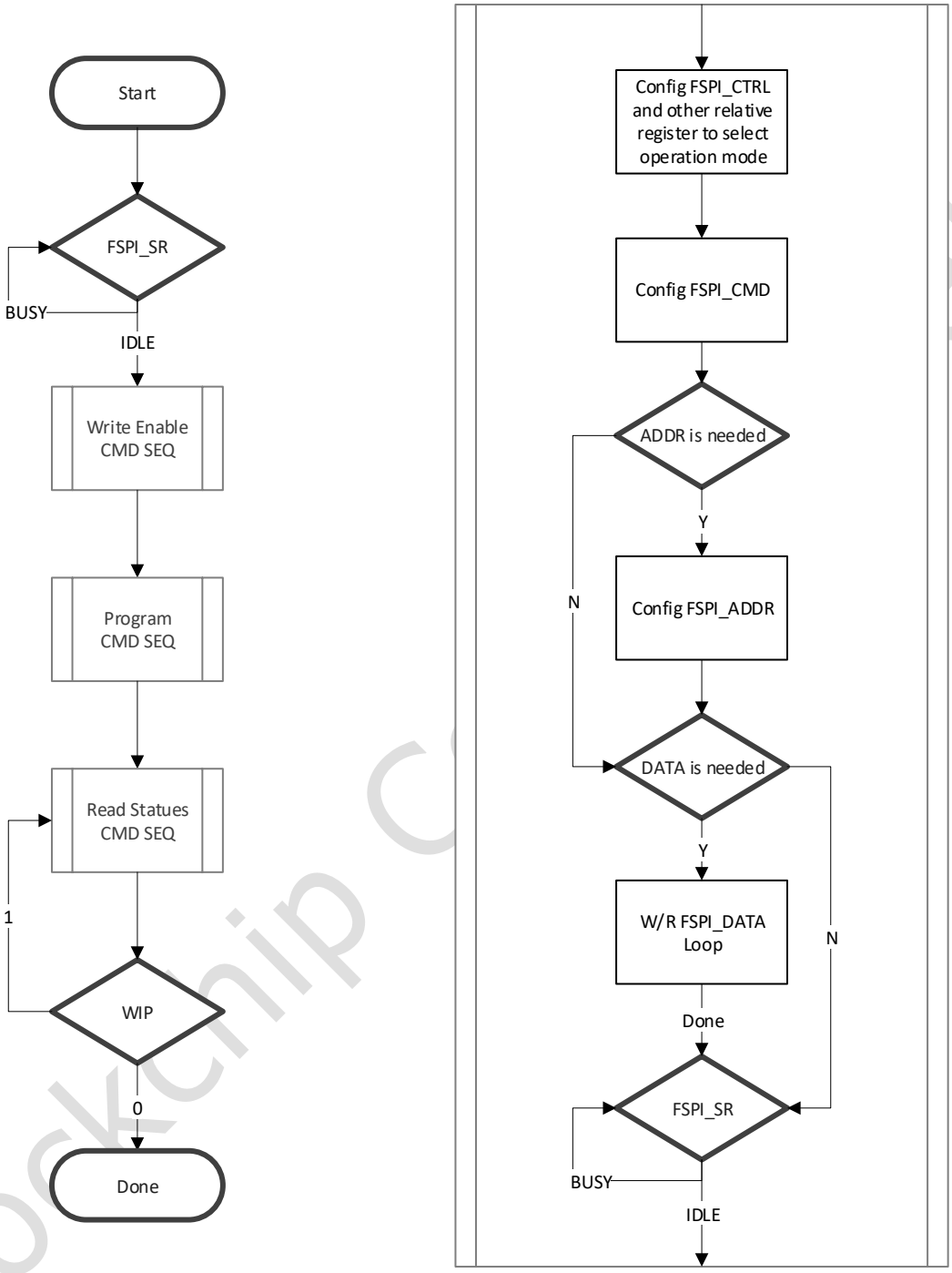

Fig. 15-2 Program Flow

All the AHB bus write data to FSPI_CMD, FSPI_ADDR and FSPI_DATA will be marked with different header and then pushed into transmit FIFO by writing order.

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15.6.2 Typical READ Flow Without DMA

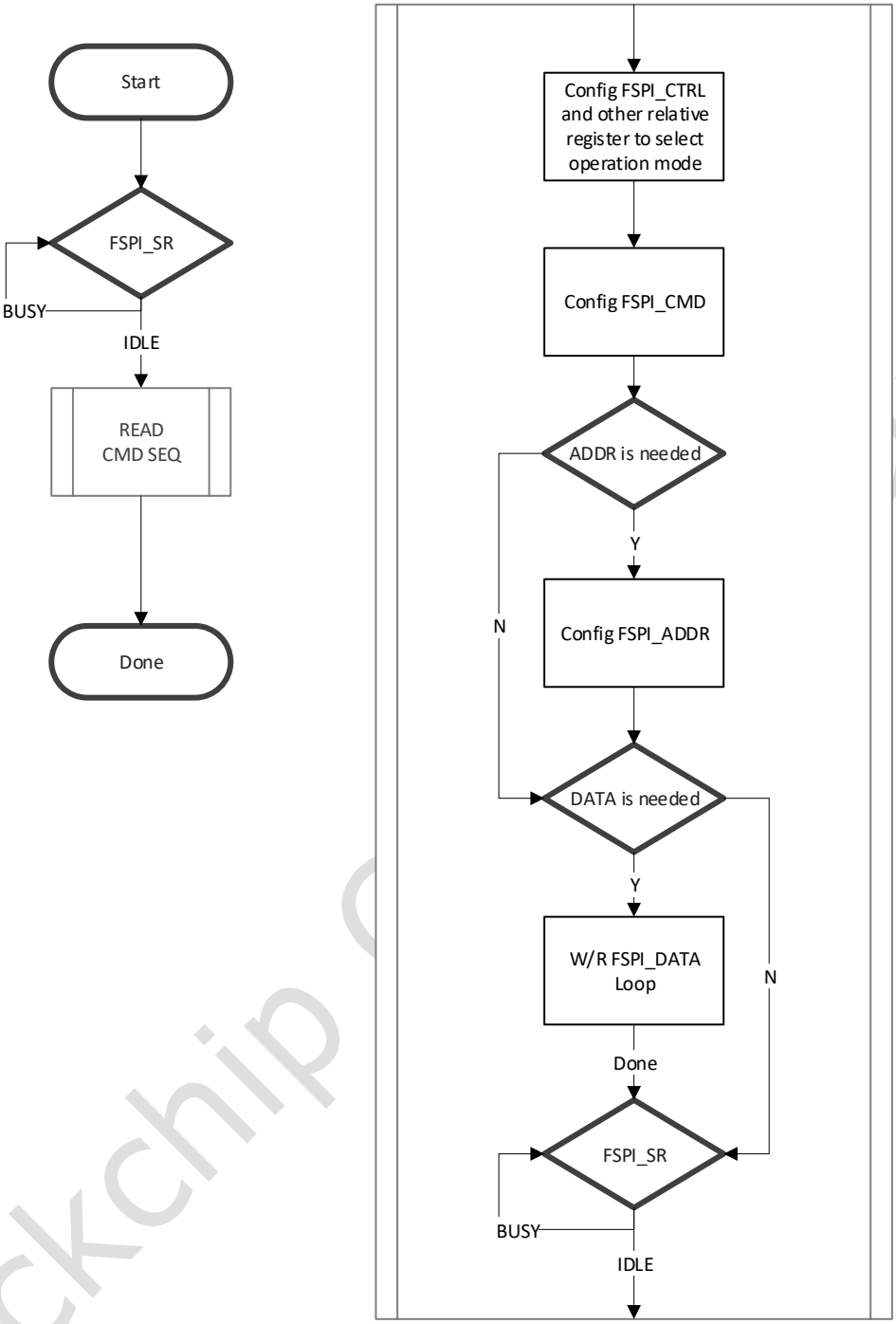

Fig. 15-3 Read Flow

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15.6.3 Command Flow with DMA

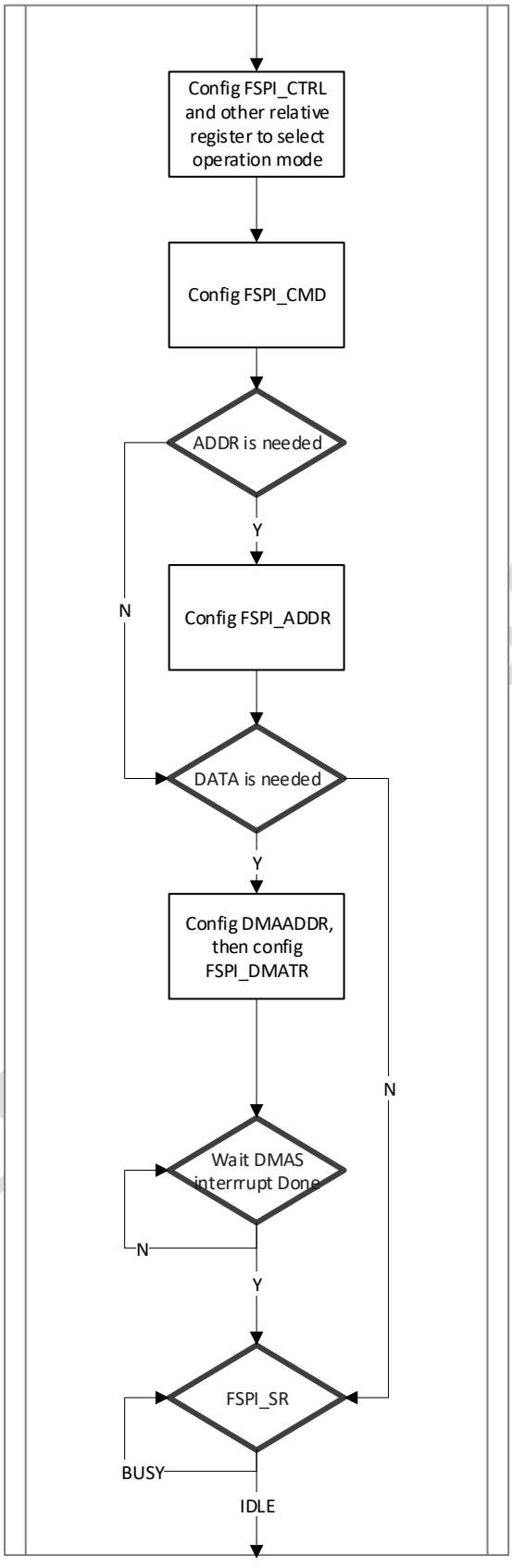

Fig. 15-4Command with DMA Flow

The total transfer bytes is decided by TRB register in FSPI_CMD and must be aligned to 2 bytes.

15.6.4 SPI Mode and Sampling Phase Control

The register SPIM in FSPI_CTRL will decide the default value of SCLK when CS# is inactive. When SPIM=0, the default value is 0, means Mode 0. When SPIM=1, the default value is 1,

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means SPI Mode 3.
The register SHIFTPAHSE in FSPI_CTRL will decide when to sample the SIO data. If SHIFTPAHSE=0, it will sample the data at the posedge of SCLK sampling clock. If SHIFTPHASE=1, it will sample the data at the negedge of SCLK sampling. The phase delay of sampling clock SCLK is configurable by SMP_DLL_CFG. It is strongly recommended that the SMP_DLL_CFG is set to 1 when SCLK_SMP_SEL is in bypass mode.
Individual FSPI_DLL_CTRL[n] allows flexibly control the DLL for each CSn channel, and the DLL is switched dynamically when the CSn is in operation.

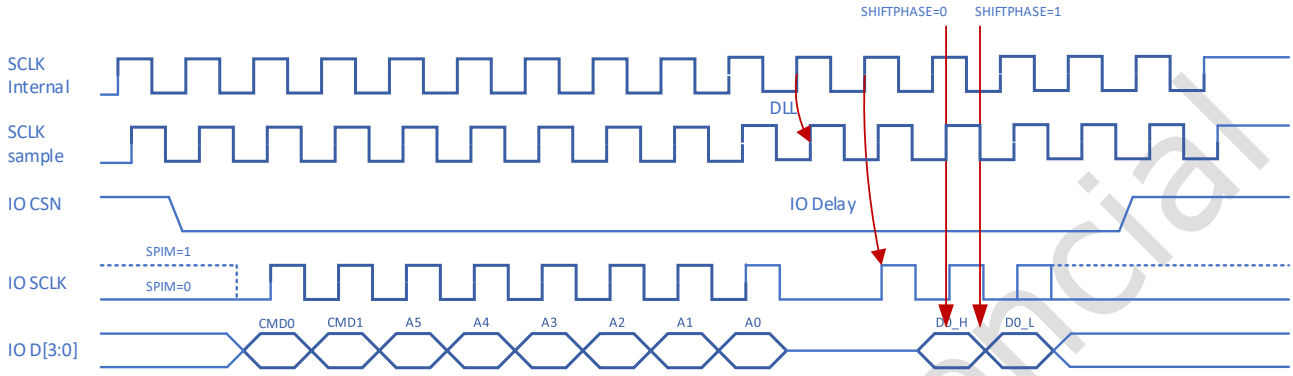

Fig. 15-5SPI mode

15.6.5 Idle Cycles

The FSPI_CTRL register is a global control register, when the controller is in busy state (FSPI_SR), FSPI_CTRL cannot be set. The field IDLE_CYCLE (FSPI_CTRL[7:4]) of this register are used to configure the idle level cycles of FSPI core clock (SCLK) before reading the first bit of the read command.
Like the following picture shows, the highlighted line of the SCLK is the idle cycles, during these cycles, the chip pad is switched to output. When IDLE_CYCLE =0, it means there will be no idle level cycles.

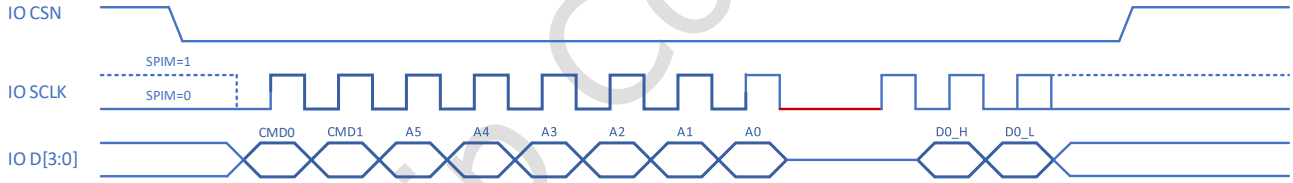

Fig. 15-6Idle cycles

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Chapter 16 Serial Peripheral Interface (SPI)

16.1 Overview

The serial peripheral interface is an APB slave device. A four wire full duplex serial protocol from Motorola. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of slave select signals or the first edge of the serial clock. The slave select line is held high when the SPI is idle or disabled. This SPI controller can work as either master or slave mode.

SPI Controller supports the following features:

- Support Motorola SPI, TI Synchronous Serial Protocol and National Semiconductor Micro wire interface
- Support 32-bit APB bus, the maximum address space of the configuration register is 0x54
- Support two internal 16-bit wide and 64-location deep FIFOs, one for transmitting and the other for receiving serial data
- Support two chip select signals in master mode
- Support the IOMUX multiplexing function. Two sets of IOMUX multiplexing for each of the three SPIs
- Support 4,8,16 bit serial data transfer
- Support configurable interrupt polarity
- Support asynchronous APB bus and SPI clock
- Support master and slave mode
- Support DMA handshake interface and configurable DMA water level
- Support RKDMA working method is the same as DMA
- Support RKDMA rx single req function. When the timeout signal is high, one single burst data is transmitted from receive FIFO
- Support transmit FIFO empty, underflow, receive FIFO full, overflow, interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combine interrupt output
- Support up to half of SPI clock frequency transfer in master mode and one sixth of SPI clock frequency transfer in slave mode
- Support full and half duplex mode transfer
- Stop transmitting SCLK if transmit FIFO is empty or receive FIFO is full in master mode
- Support configurable delay from chip select active to SCLK active in master mode
- Support configurable period of chip select inactive between two parallel data in master mode
- Support big and little endian, MSB and LSB first transfer
- Support two 8-bit audio data store together in one 16-bit wide location
- Support sample RXD 0~3 SPI clock cycles later
- Support configurable SCLK polarity and phase
- Support fix and incremental address access to transmit and receive FIFO
- Support timeout mechanism in slave mode

Support BYPASS slave mode, in which RX and TX logic is drive by SCLK_IN directly instead of spi_clk

16.2 Block Diagram

The SPI Controller is comprised of:

- AMBA APB interface and DMA Controller Interface
- Transmit and receive FIFO controllers and an FSM controller
- Register block
- Shift control and interrupt

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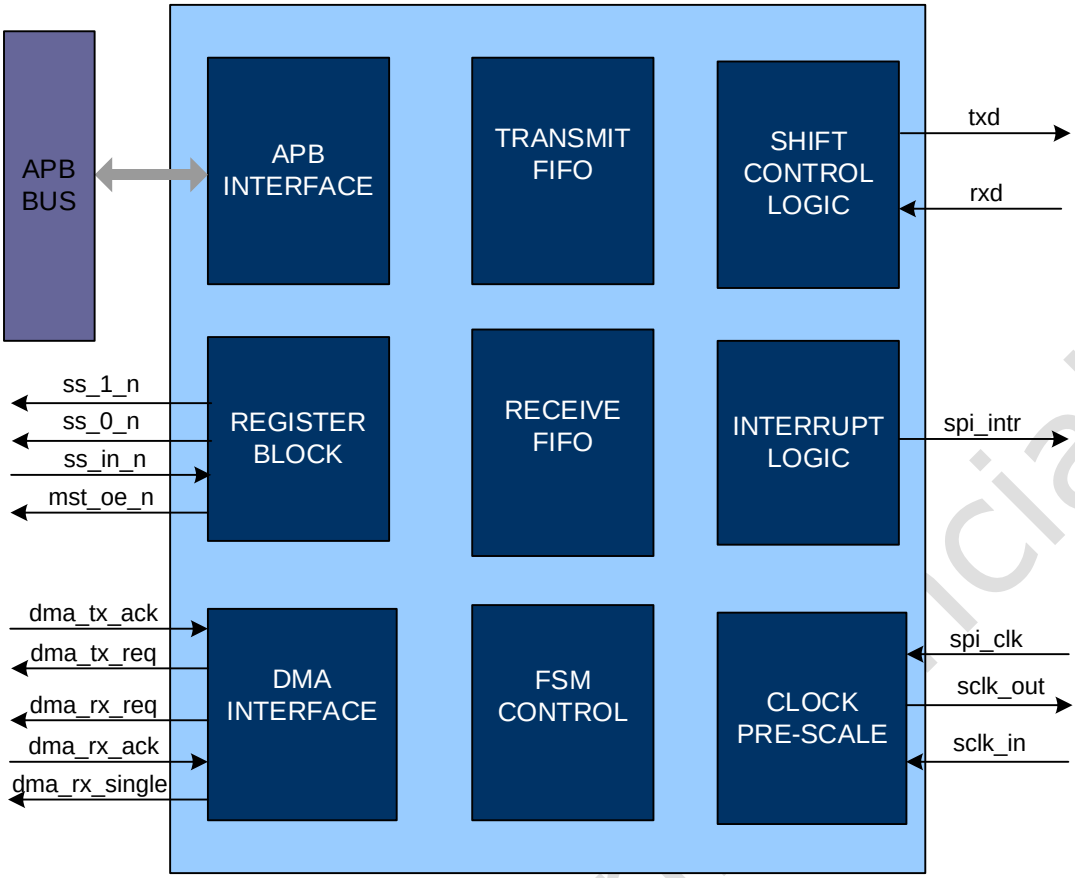

Fig. 16-1 SPI Controller Block Diagram

APB INTERFACE

The host processor accesses data, control, and status information on the SPI through the APB interface. The SPI supports APB data bus widths of 32 bits and 8 or 16 bits when reading or writing internal FIFO if data frame size(SPI_CTRL0[1:0]) is set to 8 bits.

DMA INTERFACE

This block has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA Controller.

FIFO LOGIC

For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the transmit FIFO. Data received from the external serial device into the SPI is pushed into the receive FIFO. Both fifos are 64x16bits.

FSM CONTROL

Control the state's transformation of the design.

REGISTER BLOCK

All registers in the SPI are addressed at 32-bit boundaries to remain consistent with the APB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

SHIFT CONTROL

Shift control logic shift the data from the transmit fifo or to the receive fifo. This logic automatically right-justifies receive data in the receive FIFO buffer.

INTERRUPT CONTROL

The SPI supports combined and individual interrupt requests, each of which can be masked. The combined interrupt request is the ORed result of all other SPI interrupts after masking.

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16.3 Function Description

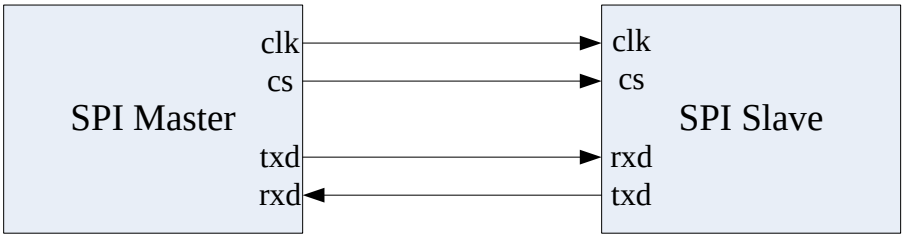

Fig. 16-2 SPI Master and Slave Interconnection

The SPI controller support dynamic switching between master and slave in a system. The diagram show how the SPI controller connects with other SPI devices.

16.3.1 Operation Modes

The SPI can be configured in the following two fundamental modes of operation: Master Mode when SPI_CTRLR0 [20] is 1'b0, Slave Mode when SPI_CTRLR0 [20] is 1'b1

16.3.2 Transfer Modes

The SPI operates in the following three modes when transferring data on the serial bus.

1). Transmit and Receive

When SPI_CTRLR0 [19:18] == 2'b00, both transmit and receive logic are valid.

2). Transmit Only

When SPI_CTRLR0 [19:18] == 2'b01, the receive data are invalid and should not be stored in the receive FIFO.

3). Receive Only

When SPI_CTRLR0 [19:18] == 2'b10, the transmit data are invalid

16.3.3 RKDMA RX single Mode

SPI supports rx single transmission when using RKDMA. Enable DMA and set receive FIFO threshold level, then set timeout time and enable timeout by SPI_TIMEOUT. If there is data in RXFIFO but it does not reach the threshold level of receive FIFO, when RKDMA has a read operation, multiple burst of single read requests will be generated after timeout time, so that RKDMA can read the data.

16.3.4 Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as,

When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})

When SPI Controller works as slave, the F_{spi_clk}>= 6 × (maximum F_{sclk_in})

With the SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical serial clock phase (SCPH) and clock polarity (SCPOL) values. The data frame can be 4/8/16 bits in length.

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the txd and rxd lines prior to the first serial clock edge. The following two figures show a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for configuration parameters SCPOL = 0 and SCPOL = 1.

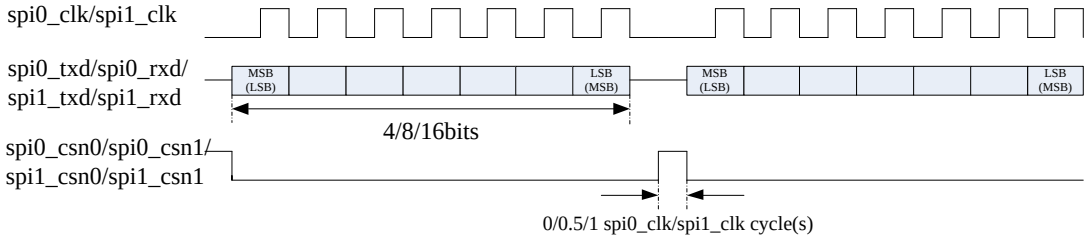

Fig. 16-3 SPI Format (SCPH=0 SCPOL=0)

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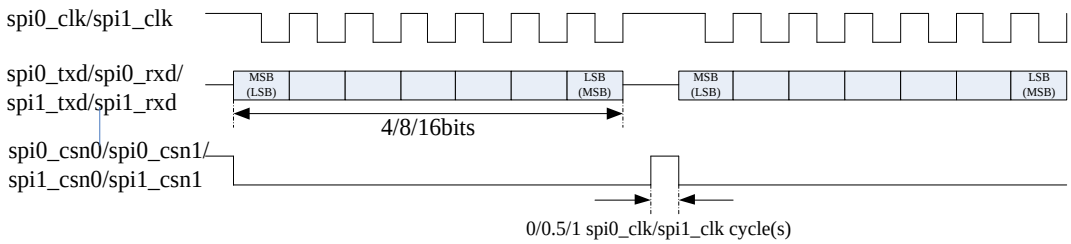

Fig. 16-4 SPI Format (SCPH=0 SCPOL=1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the SPI format when the configuration parameter SCPH = 1.

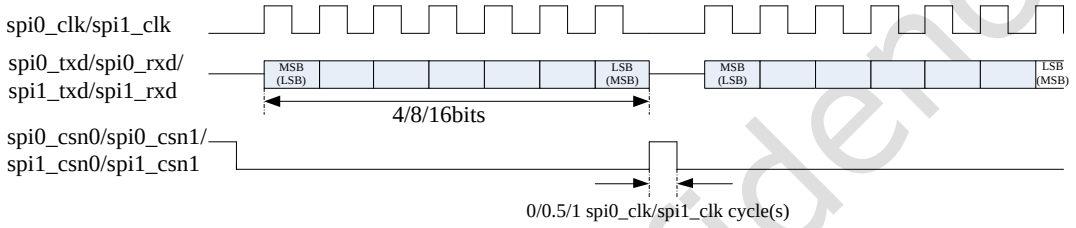

Fig. 16-5 SPI Format (SCPH=1 SCPOL=0)

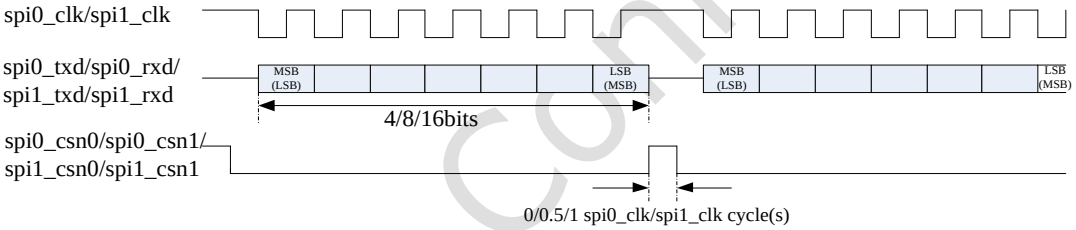

Fig. 16-6 SPI Format (SCPH=1 SCPOL=1)

16.4 Register Description

16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SPI0	0xFF220000
SPI1	0xFF640000
SPI2	0xFF650000

16.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI_CTRLR0	0x0000	W	0x00000002	Control Register 0
SPI_CTRLR1	0x0004	W	0x00000000	Control Register 1
SPI_ENR	0x0008	W	0x00000000	SPI Enable Register
SPI_SER	0x000C	W	0x00000000	Slave Enable Register
SPI_BAUDR	0x0010	W	0x00000000	Baud Rate Select
SPI_TXFTLR	0x0014	W	0x00000000	Transmit FIFO Threshold Level
SPI_RXFTLR	0x0018	W	0x00000000	Receive FIFO Threshold Level
SPI_TXFLR	0x001C	W	0x00000000	Transmit FIFO Level
SPI_RXFLR	0x0020	W	0x00000000	Receive FIFO Level

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Name	Offset	Size	Reset Value	Description
SPI_SR	0x0024	W	0x0000004C	SPI Status
SPI_IPR	0x0028	W	0x00000000	Interrupt Polarity
SPI_IMR	0x002C	W	0x00000000	Interrupt Mask
SPI_ISR	0x0030	W	0x00000000	Interrupt Status
SPI_RISR	0x0034	W	0x00000001	Raw Interrupt Status
SPI_ICR	0x0038	W	0x00000000	Interrupt Clear
SPI_DMACR	0x003C	W	0x00000000	DMA Control
SPI_DMATDLR	0x0040	W	0x00000000	DMA Transmit Data Level
SPI_DMARDLR	0x0044	W	0x00000000	DMA Receive Data Level
SPI_VERSION	0x0048	W	0x00110002	IP version
SPI_TIMEOUT	0x004C	W	0x00000000	Timeout control register
SPI_BYPASS	0x0050	W	0x00000000	BYPASS control register
SPI_TXDR	0x0400	W	0x00000000	Transmit FIFO Data
SPI_RXDR	0x0800	W	0x00000000	Receive FIFO Data

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

16.4.3 Detail Register Description

SPI_CTRLR0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	lbk Loop back mode select. 1'b0: Normal mode. 1'b1: Loop back mode, rxd is connected to txd.
24:23	RW	0x0	soi SS_N output inverted. [23]: 1'b0: Corresponding bit of ss_n[0] is not inverted. 1'b1: Corresponding bit of ss_n[0] is inverted. [24]: 1'b0: Corresponding bit of ss_n[1] is not inverted. 1'b1: Corresponding bit of ss_n[1] is inverted.
22	RW	0x0	sm SCLK_IN is masked by SS_N or not. 1'b0: SCLK_IN is masked 1'b1: SCLK_IN is not masked
21	RW	0x0	mtm Valid when frame format is set to National Semiconductors Microwire. 1'b0: Non-sequential transfer 1'b1: Sequential transfer
20	RW	0x0	opm Master and slave mode select. 1'b0: Master Mode 1'b1: Slave Mode
19:18	RW	0x0	xfm Transmit and receive mode select. 2'b00: Transmit & Receive 2'b01: Transmit Only 2'b10: Receive Only 2'b11: Reserved
17:16	RW	0x0	frf 2'b00: Motorola SPI 2'b01: Texas Instruments SSP 2'b10: National Semiconductors Microwire 2'b11: Reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	rsd When SPI is configured as a master, if the rxd data cannot be sampled by the sclk_out edge at the right time, this register should be configured to define the number of the spi_clk cycles after the active sclk_out edge to sample rxd data later when SPI works at high frequency. 2'b00: Do not delay 2'b01: 1 cycle delay 2'b10: 2 cycles delay 2'b11: 3 cycles delay
13	RW	0x0	bht Valid when data frame size is 8bit. 1'b0: APB 16bit write/read, spi 8bit write/read. 1'b1: APB 8bit write/read, spi 8bit write/read.
12	RW	0x0	fbm 1'b0: First bit is MSB. 1'b1: First bit is LSB.
11	RW	0x0	em Serial endian mode can be configured by this bit. APB endian mode is always little endian. 1'b0: Little endian 1'b1: Big endian
10	RW	0x0	ssd Valid when the frame format is set to Motorola SPI and SPI used as a master. 1'b0: The period between ss_n active and sclk_out active is half sclk_out cycles. 1'b1: The period between ss_n active and sclk_out active is one sclk_out cycle.
9:8	RW	0x0	csm Valid when the frame format is set to Motorola SPI and SPI used as a master. 2'b00: ss_n keep low after every frame data is transferred. 2'b01: ss_n be high for half sclk_out cycles after every frame data is transferred. 2'b10: ss_n be high for one sclk_out cycle after every frame data is transferred. 2'b11: Reserved
7	RW	0x0	scpol Valid when the frame format is set to Motorola SPI. 1'b0: Inactive state of serial clock is low. 1'b1: Inactive state of serial clock is high.
6	RW	0x0	scph Valid when the frame format is set to Motorola SPI. 1'b0: Serial clock toggles in middle of first data bit. 1'b1: Serial clock toggles at start of first data bit.
5:2	RW	0x0	cfs Selects the length of the control word for the Microwire frame format. 4'b0000~0010: Reserved 4'b0011: 4-bit serial data transfer 4'b0100: 5-bit serial data transfer 4'b0101: 6-bit serial data transfer 4'b0110: 7-bit serial data transfer 4'b0111: 8-bit serial data transfer 4'b1000: 9-bit serial data transfer

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Bit	Attr	Reset Value	Description
			4'b1001: 10-bit serial data transfer 4'b1010: 11-bit serial data transfer 4'b1011: 12-bit serial data transfer 4'b1100: 13-bit serial data transfer 4'b1101: 14-bit serial data transfer 4'b1110: 15-bit serial data transfer 4'b1111: 16-bit serial data transfer
1:0	RW	0x2	dfs Selects the data frame length. 2'b00: 4bit data 2'b01: 8bit data 2'b10: 16bit data 2'b11: Reserved

SPI_CTRLR1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ndm When Transfer Mode is receive only, this register field sets the number of data frames to be continuously received by the SPI. The SPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 4GB of data in a continuous transfer.

SPI_ENR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	enr Enables and disables all SPI operations. Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_SER

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	ser Slave enable register.The register enable the individual slave select output lines, 2 slave-select output pins are available.This register is valid only when SPI is configured as a master device.

SPI_BAUDR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	baudr SPI Clock Divider. This register is valid only when the SPI is configured as a master device. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fspi_clk/ SCKDV Where SCKDV is any even value between 2 and 65534. For example:

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Bit	Attr	Reset Value	Description
			for Fspi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2= 1.8432MHz

SPI_TXFTLR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	xftlr When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

SPI_RXFTLR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rxftlr When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

SPI_TXFLR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	txflr Contains the number of valid data entries in the transmit FIFO.

SPI_RXFLR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	rxflr Contains the number of valid data entries in the receive FIFO.

SPI_SR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x1	ssi 1'b0: ss_in_n is low. 1'b1: ss_in_n is high.
5	RO	0x0	stb 1'b0: Slave tx not busy. 1'b1: Slave tx busy.
4	RO	0x0	rff 1'b0: Receive FIFO is not full. 1'b1: Receive FIFO is full.
3	RO	0x1	rfe 1'b0: Receive FIFO is not empty. 1'b1: Receive FIFO is empty.
2	RO	0x1	tfe 1'b0: Transmit FIFO is not empty. 1'b1: Transmit FIFO is empty.
1	RO	0x0	tff 1'b0: Transmit FIFO is not full. 1'b1: Transmit FIFO is full.

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Bit	Attr	Reset Value	Description
0	RO	0x0	bsf When set, indicates that a serial transfer is in progress; when cleared, indicates that the SPI is idle or disabled. 1'b0: SPI is idle or disabled. 1'b1: SPI is actively transferring data.

SPI_IPR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ipr Interrupt Polarity Register. 1'b0: Active Interrupt Polarity Level is HIGH. 1'b1: Active Interrupt Polarity Level is LOW.

SPI_IMR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfim 1'b0: TX finish interrupt is masked. 1'b1: TX finish interrupt is not masked.
6	RW	0x0	sspim 1'b0: ss_in_n posedge interrupt is masked. 1'b1: ss_in_n posedge interrupt is not masked.
5	RW	0x0	toim 1'b0: spi timeout interrupt is masked. 1'b1: spi timeout interrupt is not masked.
4	RW	0x0	rffim 1'b0: spi_rxf_intr interrupt is masked. 1'b1: spi_rxf_intr interrupt is not masked.
3	RW	0x0	rfoim 1'b0: spi_rxo_intr interrupt is masked. 1'b1: spi_rxo_intr interrupt is not masked.
2	RW	0x0	rfuim 1'b0: spi_rxu_intr interrupt is masked. 1'b1: spi_rxu_intr interrupt is not masked.
1	RW	0x0	tfoim 1'b0: spi_txo_intr interrupt is masked. 1'b1: spi_txo_intr interrupt is not masked.
0	RW	0x0	tfeim 1'b0: spi_txe_intr interrupt is masked. 1'b1: spi_txe_intr interrupt is not masked.

SPI_ISR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfis 1'b0: TX finish interrupt is not active after masking. 1'b1: TX finish interrupt is active after masking.
6	RW	0x0	sspis 1'b0: ss_in_n posedge interrupt is not active after masking. 1'b1: ss_in_n posedge interrupt is active after masking.

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Bit	Attr	Reset Value	Description
5	RW	0x0	tois 1'b0: spi timeout interrupt is not active after masking. 1'b1: spi timeout interrupt is active after masking.
4	RO	0x0	rffis 1'b0: spi_rxf_intr interrupt is not active after masking. 1'b1: spi_rxf_intr interrupt is full after masking.
3	RO	0x0	rfois 1'b0: spi_rxo_intr interrupt is not active after masking. 1'b1: spi_rxo_intr interrupt is active after masking.
2	RO	0x0	rfuis 1'b0: spi_rxu_intr interrupt is not active after masking. 1'b1: spi_rxu_intr interrupt is active after masking.
1	RO	0x0	tfois 1'b0: spi_txo_intr interrupt is not active after masking. 1'b1: spi_txo_intr interrupt is active after masking.
0	RO	0x0	tfeis 1'b0: spi_txe_intr interrupt is not active after masking. 1'b1: spi_txe_intr interrupt is active after masking.

SPI_RISR

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	txfris 1'b0: TX finish interrupt is not active prior to masking. 1'b1: TX finish interrupt is active prior to masking.
6	RO	0x0	sspris 1'b0: ss_in_n posedge interrupt is not active prior to masking. 1'b1: ss_in_n posedge interrupt is active prior to masking.
5	RO	0x0	toris 1'b0: spi_timeout interrupt is not active prior to masking. 1'b1: spi_timeout interrupt is active prior to masking.
4	RO	0x0	rffris 1'b0: spi_rxf_intr interrupt is not active prior to masking. 1'b1: spi_rxf_intr interrupt is full prior to masking.
3	RO	0x0	rforis 1'b0: spi_rxo_intr interrupt is not active prior to masking. 1'b1: spi_rxo_intr interrupt is active prior to masking.
2	RO	0x0	rfuris 1'b0: spi_rxu_intr interrupt is not active prior to masking. 1'b1: spi_rxu_intr interrupt is active prior to masking.
1	RO	0x0	tforis 1'b0: spi_txo_intr interrupt is not active prior to masking. 1'b1: spi_txo_intr interrupt is active prior to masking.
0	RO	0x1	tferis 1'b0: spi_txe_intr interrupt is not active prior to masking. 1'b1: spi_txe_intr interrupt is active prior to masking.

SPI_ICR

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	WO	0x0	ctxfi Write 1 to Clear tx finish Interrupt.

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Bit	Attr	Reset Value	Description
5	WO	0x0	csspi Write 1 to Clear ss_in_n posedge Interrupt.
4	WO	0x0	ctoi Write 1 to Clear Timeout Interrupt.
3	WO	0x0	ctfoi Write 1 to Clear Transmit FIFO Overflow Interrupt.
2	WO	0x0	crfoi Write 1 to Clear Receive FIFO Overflow Interrupt.
1	WO	0x0	crfui Write 1 to Clear Receive FIFO Underflow Interrupt.
0	WO	0x0	cci Write 1 to Clear Combined Interrupt.

SPI_DMACR

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	tde 1'b0: Transmit DMA disabled. 1'b1: Transmit DMA enabled.
0	RW	0x0	rde 1'b0: Receive DMA disabled. 1'b1: Receive DMA enabled.

SPI_DMATDLR

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	tdl This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and transmit DMA is enabled (DMACR[1] = 1).

SPI_DMARDLR

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rdl This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and receive DMA is enabled(DMACR[0]=1).

SPI_VERSION

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00110002	version IP version

SPI_TIMEOUT

Address: **Operational Base** + offset (0x004C)

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Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	dtsr DMA Timeout single request enable. 1'b0: DMA Timeout single request disable. 1'b1: DMA Timeout single request enable.
17	RW	0x0	tsb Timeout sclkcnt_bypass 1'b0: Timeout counter will be active after the first rising edge of sclk_in. 1'b1: Timeout counter will be active after the first rising edge of pclk.
16	RW	0x0	toe Timeout enable. 1'b0: Timeout counter is inactive. 1'b1: Timeout counter will be active after the first rising edge of sclk_in.
15:0	RW	0x0000	tov Timeout threshold value. If sclk_in keep inactive for a threshold time , timeout interrupt will be triggered .The timeout threshold time is TOV*pclk_perid*16.

SPI_BYPASS

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	txcp TX clock polarity.This bit is only valid in bypass mode. 1'b0: TX logic use raw SCLK. 1'b1: TX logic use inverted SCLK.
3	RW	0x0	rxcp RX clock polarity.This bit is only valid in bypass mode. 1'b0: RX logic use raw SCLK. 1'b1: RX logic use inverted SCLK.
2	RW	0x0	end Endian mode.This bit is only valid in bypass mode. 1'b0: Work in little endian mode. 1'b1: Work in big endian mode.
1	RW	0x0	fbm First bit mode.This bit is only valid in bypass mode. 1'b0: First bit is LSB. 1'b1: First bit is MSB.
0	RW	0x0	byen Bypass enable. 1'b0: Normal mode. 1'b1: Bypass mode, SPI serial/parallel convert logic is drive by SCLK.

SPI_TXDR

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	WO	0x0000	txdr When it is written to, data are moved into the transmit FIFO.

SPI_RXDR

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Address: **Operational Base** + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rxdr When the register is read, data in the receive FIFO is accessed.

16.5 Interface Description

Table 16-1 SPI interface description

Module Pin	Direction	Pad Name	IOMUX Setting
SPI0mux0 Interface			
spi0_sclk	I/O	UART2_RTSN_M0/PWM0_M0/SPI0_CLK_M0/GPIO0_C3_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L[15:12]=4'h3
spi0_rxd	I	UART6_RTSN_M0/PWM2_M0/SPI0_MISO_M0/GPIO0_C5_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_H[7:4]=4'h3
spi0_txd	O	UART6_CTSN_M0/PWM1_M0/SPI0_MOSI_M0/GPIO0_C4_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_H[3:0]=4'h3
spi0_csn0	I/O	UART2_CTSN_M0/PWM5_M0/SPI0_CSN0_M0/GPIO0_C2_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L[11:8]=4'h3
spi0_csn1	O	SPI0_CSN1_M0/PWM4_M0/CPU_AVS/SPDIF_TX_M1/GPIO0_B7_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_H[15:12]=4'h1
SPI0mux1 Interface			
spi0_sclk	I/O	I2S1_SDO0_M1/CAM_CLK3_OUT/UART8_RTSN_M0/SPI0_CLK_M1/PWM13_M1/GPIO3_B5_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'h4
spi0_rxd	I	I2S1_SDO3_M1/I2S1_SDI1_M1/UART3_RX_M1/SPI0_MISO_M1/GPIO3_C0_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_L[3:0]=4'h4
spi0_txd	O	I2S1_LRCK_M1/CAM_CLK2_OUT/UART8_CTSN_M0/SPI0_MOSI_M1/PWM12_M1/GPIO3_B4_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H[3:0]=4'h4
spi0_csn0	I/O	I2S1_SDO2_M1/I2S1_SDI2_M1/UART3_TX_M1/SPI0_CSN0_M1/I2C4_SDA_M0/CAN0_RX_M1/GPIO3_B7_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H[15:12]=4'h4
spi0_csn1	O	I2S1_SDO1_M1/I2S1_SDI3_M1/UART3_CTSN_M1/SPI0_CSN1_M1/I2C4_SCL_M0/CAN0_TX_M1/GPIO3_B6_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'h4
SPI1mux0 Interface			
spi1_sclk	I/O	VO_LCDC_D15/RGMII_TXCLK_M0/I2S2_MCLK_M1/SPI1_CLK_M0/GPIO3_D6_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[11:8]=4'h4
spi1_rxd	I	VO_LCDC_D23/RGMII_TXD1_M0/UART6_RTSN_M1/SPI1_MISO_M0/GPIO4_A3_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[15:12]=4'h4
spi1_txd	O	VO_LCDC_D22/RGMII_TXD0_M0/UART6_CTSN_M1/SPI1_MOSI_M0/GPIO4_A2_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[11:8]=4'h4
spi1_csn0	I/O	VO_LCDC_D19/RGMII_RXD2_M0/UART8_CTSN_M1/SPI1_CSN0_M0/GPIO3_D7_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[15:12]=4'h4
spi1_csn1	O	VO_LCDC_D20/RGMII_RXD3_M0/UART8_RTSN_M1/SPI1_CSN1_M0/GPIO4_A0_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4'h4
SPI1mux1 Interface			
spi1_sclk	I/O	SDMMC0_CLK/TEST_CLK_OUT/UART5_TX_M0/SPI1_CLK_M1/CAN1_TX_M0/GPIO1_C0_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L[3:0]=4'h4
spi1_rxd	I	SDMMC0_D1/UART0_TX_M1/UART7_TX_M1/SPI1_MISO_M1/DSM_AUD_LN/GPIO1_B4_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4'h4
spi1_txd	O	SDMMC0_D0/UART0_RX_M1/UART7_RX_M1/SPI1_MOSI_M1/DSM_AUD_LP/GPIO1_B3_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h4
spi1_csn0	I/O	SDMMC0_D3/JTAG_CPU_MCU_TMS_M1	GPIO1_IOC_GPIO1B_IOMUX_SE

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Module Pin	Direction	Pad Name	IOMUX Setting
		/UART5_RTSN_M0/SPI1_CSN0_M1/PWM11_M0/DSM_AUD_RN/GPIO1_B6_u	L_H[11:8]=4'h4
spi1_csn1	O	SDMMC0_D2/JTAG_CPU_MCU_TCK_M1/UART5_CTSN_M0/SPI1_CSN1_M1/PWM10_M0/DSM_AUD_RP/GPIO1_B5_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[7:4]=4'h4
SPI2mux0 Interface			
spi2_sclk	I/O	VO_LCDC_DEN/I2S1_SDO3_M0/UART3_CTSN_M0/SPI2_CLK_M0/GPIO4_B6_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[11:8]=4'h4
spi2_rxd	I	VO_LCDC_D11/I2S1_SDI2_M0/UART7_CTSN_M0/SPI2_MISO_M0/I2C2_SCL_M1/GPIO3_D2_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[11:8]=4'h4
spi2_txd	O	VO_LCDC_D12/I2S1_SDI3_M0/UART7_RTSN_M0/SPI2_MOSI_M0/I2C2_SDA_M1/GPIO3_D3_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[15:12]=4'h4
spi2_csn0	I/O	VO_LCDC_VSYNC/I2S1_SDO2_M0/UART9_RTSN_M0/SPI2_CSN0_M0/I2C1_SDA_M1/UART3_RX_M0/GPIO4_B5_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4'h4
spi2_csn1	O	VO_LCDC_HSYNC/I2S1_SDO1_M0/UART9_CTSN_M0/SPI2_CSN1_M0/I2C1_SCL_M1/UART3_TX_M0/GPIO4_B4_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'h4
SPI2mux1 Interface			
spi2_sclk	I/O	I2S2_MCLK_M0/ETH_CLK_25M_OUT_M1/CLK1_32K_OUT/SPI2_CLK_M1/I2S0_SDO3_M1/GPIO2_A1_d	GPIO2_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'h4
spi2_rxd	I	I2S2_SDI_M0/RGMII_RXER_M1/UART4_CTSN_M1/SPI2_MISO_M1/PWM15_M1/RMII_RXER/GPIO2_A0_d	GPIO2_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'h4
spi2_txd	O	I2S2_SDO_M0/RGMII_RXD1_M1/UART4_RTSN_M1/SPI2_MOSI_M1/PWM14_M1/RMII_RXD1/GPIO1_D7_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H[15:12]=4'h4
spi2_csn0	I/O	I2S2_LRCK_M0/RGMII_RXDV_M1/UART4_TX_M1/SPI2_CSN0_M1/RMII_RXDV_CRS/GPIO1_D6_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H[11:8]=4'h4
spi2_csn1	O	I2S2_SCLK_M0/RGMII_CLK_M1/UART4_RX_M1/SPI2_CSN1_M1/RMII_CLK/GPIO1_D5_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional. spi_csn1 can only be used in master mode

16.6 Application Notes

16.6.1 Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as,
When SPI Controller works as master, the Fspi_clk>= 2 × (maximum Fsclk_out)
When SPI Controller works as slave, the Fspi_clk>= 6 × (maximum Fsclk_in)

16.6.2 Master Transfer Flow

When configured as a serial-master device, the SPI initiates and controls all serial transfers. The serial bit-rate clock, generated and controlled by the SPI, is driven out on the sclk_out line. When the SPI is disabled (SPI_ENR = 0), no serial transfers can occur and sclk_out is held in "inactive" state, as defined by the serial protocol under which it operates.

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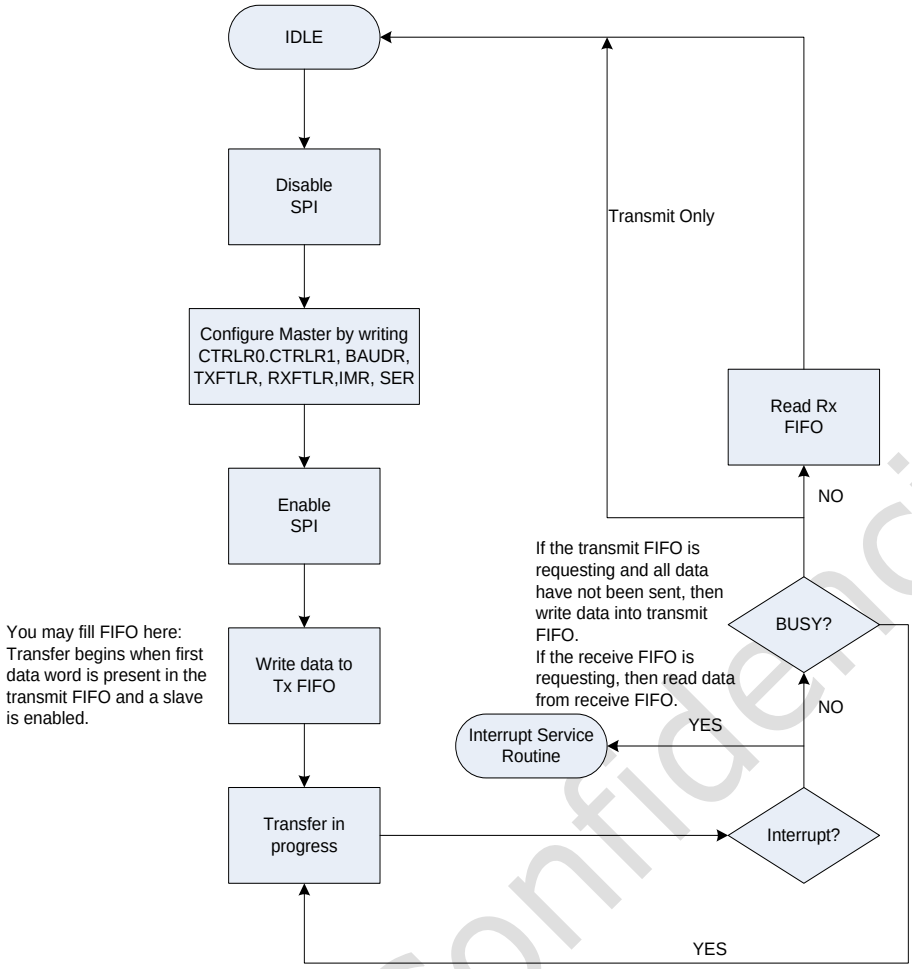

Fig. 16-7 SPI Master transfer flow diagram

16.6.3 Slave Transfer Flow

When the SPI is configured as a slave device, all serial transfers are initiated and controlled by the serial bus master.

When the SPI serial slave is selected during configuration, it enables its txd data onto the serial bus. All data transfers to and from the serial slave are regulated on the serial clock line (sclk_in), driven from the serial-master device. Data are propagated from the serial slave on one edge of the serial clock line and sampled on the opposite edge.

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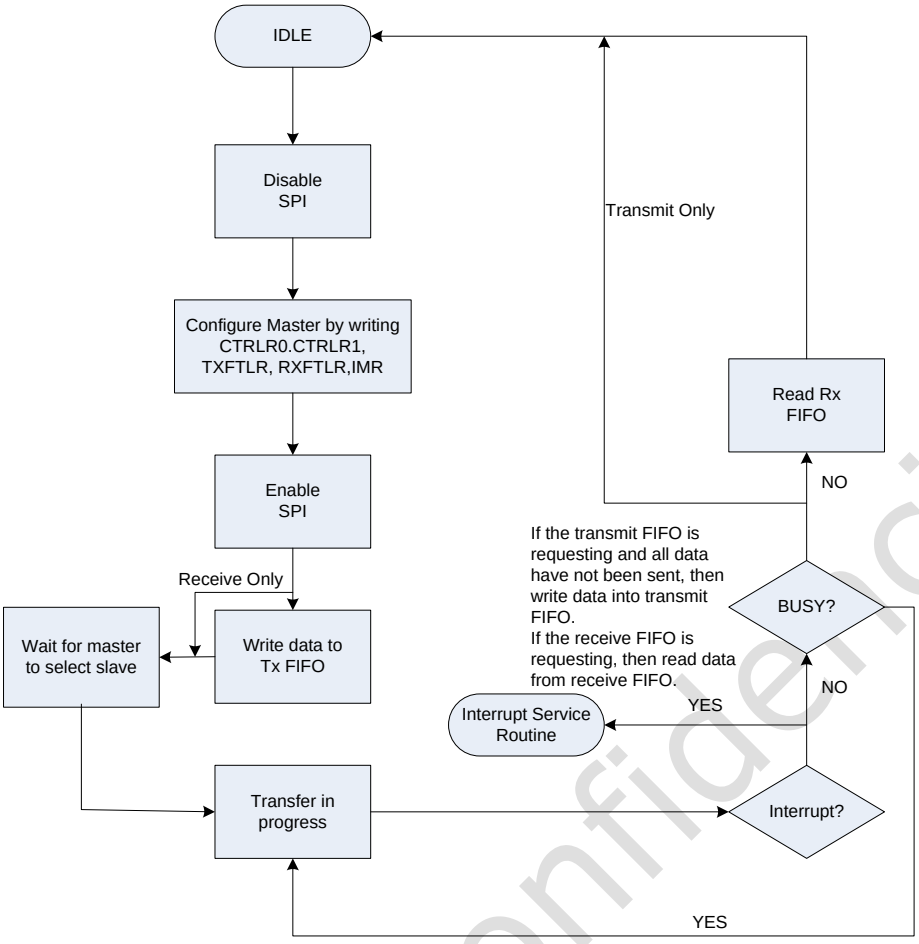

Fig. 16-8 SPI Slave transfer flow diagram

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Chapter 17 Universal Asynchronous Receiver/Transmitter (UART)

17.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

UART Controller supports the following features:

- Support 10 independent UART controller: UART0-UART9
- Support 32-bit APB bus
- Support the IOMUX multiplexing function. Two sets of IOMUX multiplexing for each of the all ten UARTs
- Support none FIFO data transmission mode
- Support FIFO data transmission mode
- All contain two 64Bytes FIFOs for data receive and transmit
- Support maskable combined interrupt output (5 types)
- UART1/2/3/4/5/6/8-m0/m1 and UART7/9-m0 support auto flow-control (AFC) , other not support auto flow-control
- Support bit rates 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps
- Support programmable baud rates, even with non-integer clock divider
- Standard asynchronous communication bits (start, stop and parity)
- Support interrupt-based or DMA-based mode
- Support RKDMA working method is the same as DMA
- Support 5-8 bits width transfer
- Support RKDMA rx single req function. When the timeout signal is high, one single burst data is transmitted from receive FIFO
- Support UART0 and jtag reuse GPIO

17.2 Block Diagram

This section provides a description about the functions and behavior under various conditions. The UART Controller is comprised of:

- AMBA APB interface
- FIFO controllers
- Register block
- Modem synchronization block and baud clock generation block
- Serial receiver and serial transmitter

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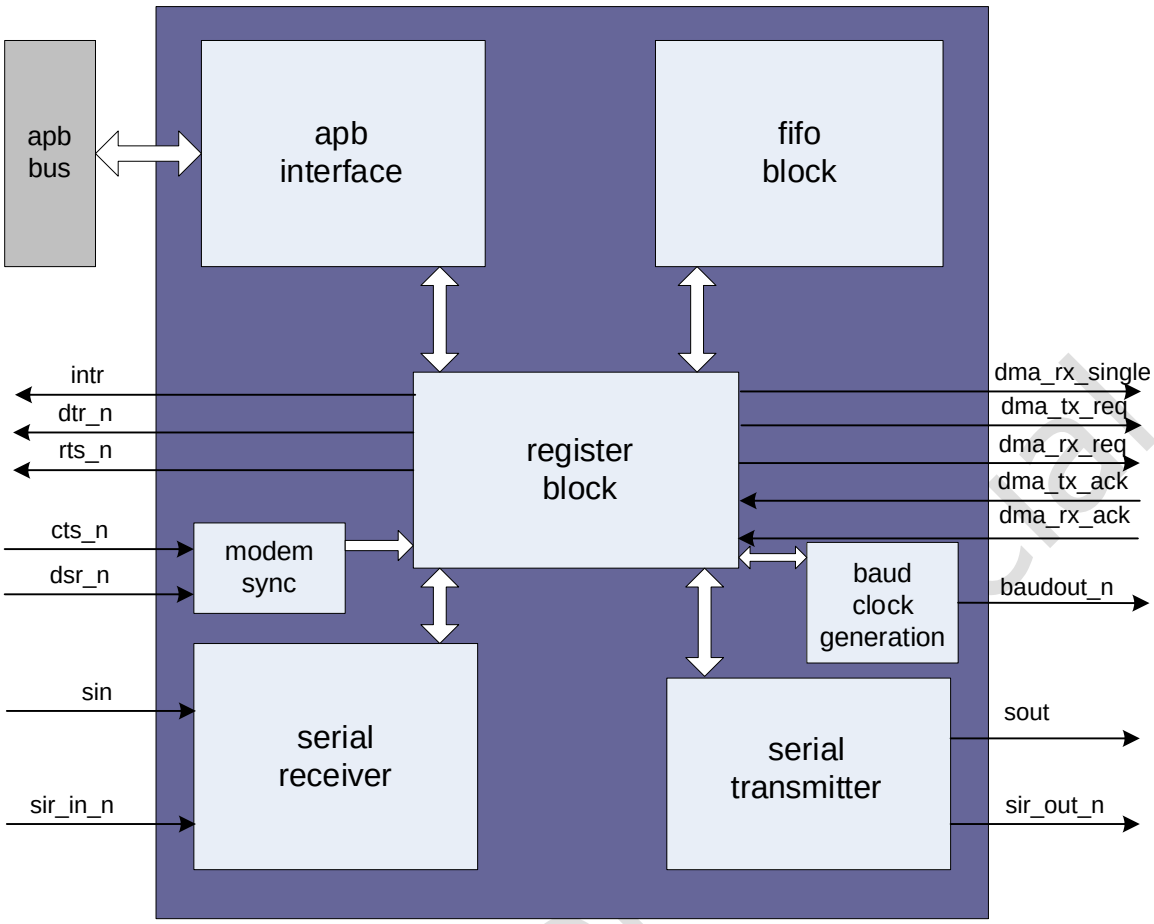

Fig. 17-1 UART Architecture

APB INTERFACE

The host processor accesses data, control, and status information on the UART through the APB interface. The UART supports APB data bus widths of 8, 16, and 32 bits.

Register block

Be responsible for the main UART functionality including control, status and interrupt generation.

Modem Synchronization block

Synchronizes the modem input signal.

FIFO block

Be responsible for FIFO control and storage (when using internal RAM) or signaling to control external RAM (when used).

Baud Clock Generator

Generates the transmitter and receiver baud clock along with the output reference clock signal (baudout_n).

Serial Transmitter

Converts the parallel data, written to the UART, into serial form and adds all additional bits, as specified by the control register, for transmission. This makeup of serial data, referred to as a character can exit the block in two forms, either serial UART format or IrDA 1.0 SIR format.

Serial Receiver

Converts the serial data character (as specified by the control register) received in either the UART or IrDA 1.0 SIR format to parallel form. Parity error detection, framing error detection and line break detection is carried out in this block.

17.3 Function Description

17.3.1 UART (RS232) Serial Protocol

Because the serial communication is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. An additional parity bit may be added to the serial character. This bit appears after the last data bit and before the stop bit(s) in the

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character structure to perform simple error checking on the received data, as shown in Figure.

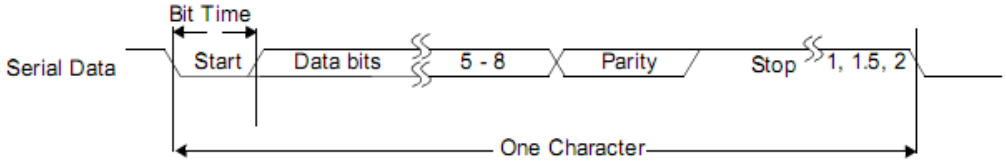

Fig. 17-2 UART Serial protocol

17.3.2 IrDA 1.0 SIR Protocol

The Infrared Data Association (IrDA) 1.0 Serial Infrared (SIR) mode supports bi-directional data communications with remote devices using infrared radiation as the transmission medium. IrDA 1.0 SIR mode specifies a maximum baud rate of 115.2 Kbaud.

Transmitting a single infrared pulse signals a logic zero, while a logic one is represented by not sending a pulse. The width of each pulse is 3/16ths of a normal serial bit time. Data transfers can only occur in half-duplex fashion when IrDA SIR mode is enabled.

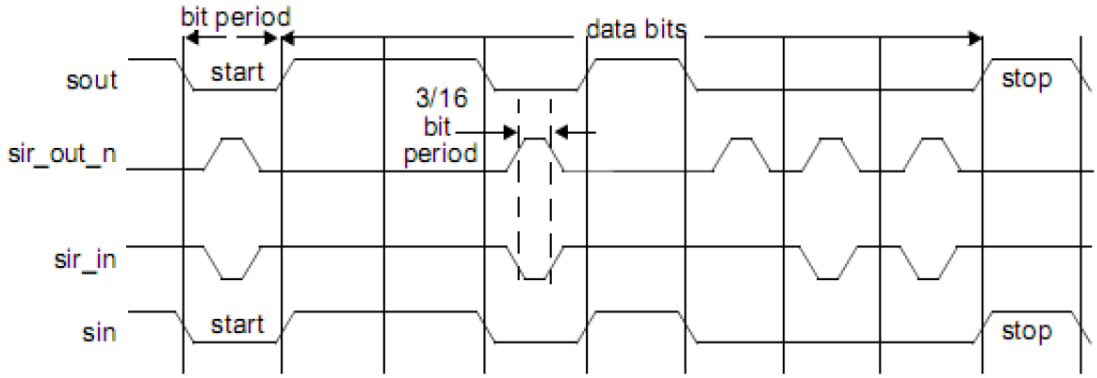

Fig. 17-3 IrDA 1.0

17.3.3 Baud Clock

The baud rate is controlled by the serial clock (sclk or pclk in a single clock implementation) and the Divisor Latch Register (DLH and DLL). As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit.

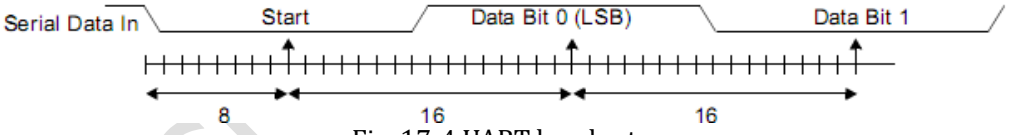

Fig. 17-4 UART baud rate

17.3.4 FIFO Support

17.3.4.1 None FIFO Mode

If FIFO support is not selected, then no FIFOs are implemented and only a single receive data byte and transmit data byte can be stored at a time in the RBR and THR.

17.3.4.2 FIFO Mode

The FIFO depth of UART is 64bytes. The FIFO mode of all the UART is enabled by register FCR[0].

17.3.5 Interrupts

The following interrupt types can be enabled with the IER register.

- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)
- Transmitter Holding Register Empty at/below threshold (in Programmable THRE Interrupt mode)
- Modem Status

17.3.6 DMA Support

The UART supports DMA signaling with the use of two output signals (dma_tx_req_n and dma_rx_req_n) to indicate when data is ready to be read or when the transmit FIFO is empty.

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The dma_tx_req_n signal is asserted under the following conditions:

- When the Transmitter Holding Register is empty in non-FIFO mode.
- When the transmitter FIFO is empty in FIFO mode with Programmable THRE interrupt mode disabled.
- When the transmitter FIFO is at, or below the programmed threshold with Programmable THRE interrupt mode enabled.

The dma_rx_req_n signal is asserted under the following conditions:

- When there is a single character available in the Receive Buffer Register in non-FIFO mode.

When the Receiver FIFO is at or above the programmed trigger level in FIFO mode.

17.3.7 RKDMA RX single Mode

UART supports rx single transmission when use RKDMA. First disable uart_rx_single_ bypass signal, then set the threshold Level of the FIFO and enable FIFO, start the transmission, and start the RKDMA read operation. When the data in the RX FIFO of the UART is less than the threshold Level and lasts for a period of time, the UART will send an rx single request to the RKDMA for multiple burst to single transmission, thus completing the RKDMA read task.

17.3.8 Auto Flow Control

The UART can be configured to have a 16750-compatible Auto RTS and Auto CTS serial data flow control mode available. If FIFOs are not implemented, then this mode cannot be selected. When Auto Flow Control mode has been selected, it can be enabled with the Modem Control Register (MCR[5]). Following figure shows a block diagram of the Auto Flow Control functionality.

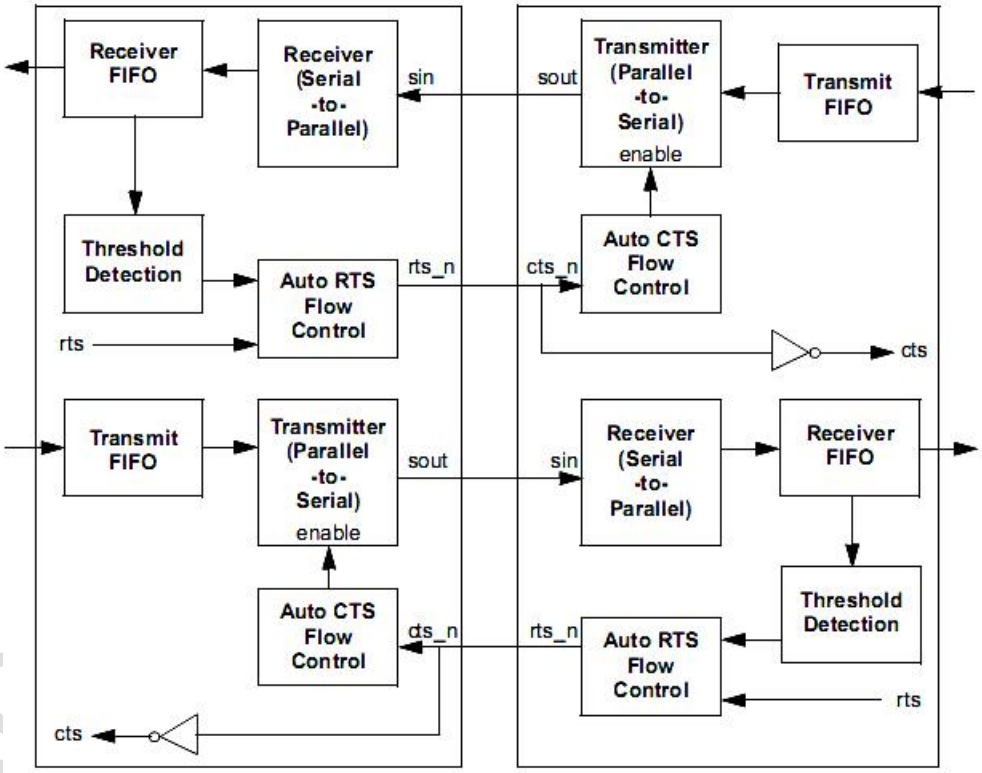

Fig. 17-5 UART Auto flow control block diagram

Auto RTS – Becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- RTS (MCR[1] bit and MCR[5]bit are both set)
- FIFOs are enabled (FCR[0]) bit is set)
- SIR mode is disabled (MCR[6] bit is not set)

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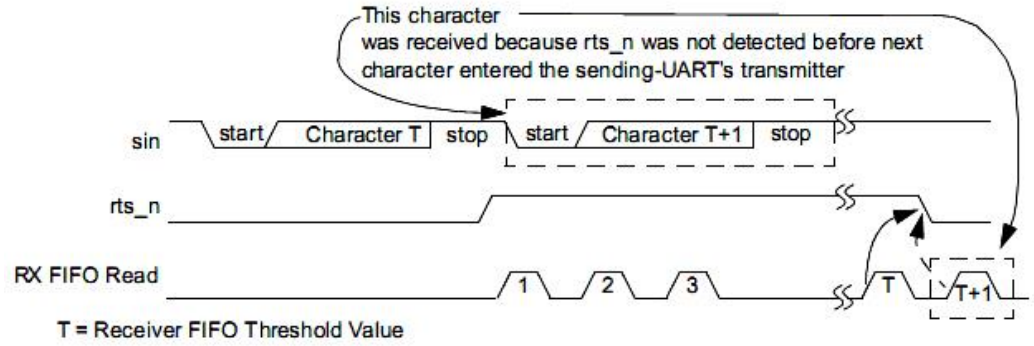

Fig. 17-6 UART AUTO RTS TIMING

Auto CTS – becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- AFCE (MCR[5] bit is set)
- FIFOs are enabled through FIFO Control Register FCR[0] bit
- SIR mode is disabled (MCR[6] bit is not set)

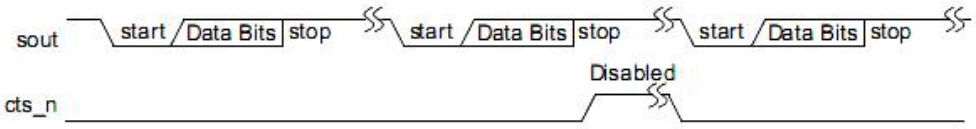

Fig. 17-7 UART AUTO CTS TIMING

17.4 Register Description

17.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
UART0	0xFF210000
UART1	0xFF670000
UART2	0xFF680000
UART3	0xFF690000
UART4	0xFF6A0000
UART5	0xFF6B0000
UART6	0xFF6C0000
UART7	0xFF6D0000
UART8	0xFF6E0000
UART9	0xFF6F0000

17.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
UART_RBR	0x0000	W	0x00000000	Receive Buffer Register
UART_DLL	0x0000	W	0x00000000	Divisor Latch Low
UART_THR	0x0000	W	0x00000000	Transmit Buffer Register
UART_DLH	0x0004	W	0x00000000	Divisor Latch High
UART_IER	0x0004	W	0x00000000	Interrupt Enable Register
UART_FCR	0x0008	W	0x00000000	FIFO Enable
UART_IIR	0x0008	W	0x00000001	Interrupt Identity Register
UART_LCR	0x000C	W	0x00000000	Line Control Register
UART_MCR	0x0010	W	0x00000000	Modem Control Register
UART_LSR	0x0014	W	0x00000060	Line Status Register
UART_MSR	0x0018	W	0x00000000	Modem Status Register

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Name	Offset	Size	Reset Value	Description
UART_SCR	0x001C	W	0x00000000	Scratchpad Register
UART_SRBR	0x0030	W	0x00000000	Shadow Receive Buffer Register
UART_STHR	0x0050	W	0x00000000	Shadow Transmit Holding Register
UART_FAR	0x0070	W	0x00000000	FIFO Access Register
UART_TFR	0x0074	W	0x00000000	Transmit FIFO Read
UART_RFW	0x0078	W	0x00000000	Receive FIFO write
UART_USR	0x007C	W	0x00000006	UART Status Register
UART_TFL	0x0080	W	0x00000000	Transmit FIFO level
UART_RFL	0x0084	W	0x00000000	Receive FIFO level
UART_SRR	0x0088	W	0x00000000	Software Reset Register
UART_SRTS	0x008C	W	0x00000000	Shadow Request to Send
UART_SBCR	0x0090	W	0x00000000	Shadow Break Control Register
UART_SDMAM	0x0094	W	0x00000000	Shadow DMA Mode
UART_SFE	0x0098	W	0x00000000	Shadow FIFO enable
UART_SRT	0x009C	W	0x00000000	Shadow RCVR Trigger
UART_STET	0x00A0	W	0x00000000	Shadow TX Empty Trigger
UART_HTX	0x00A4	W	0x00000000	Halt TX
UART_DMASA	0x00A8	W	0x00000000	DMA Software Acknowledge
UART_CPR	0x00F4	W	0x00043FF2	Component Parameter Register
UART_UCV	0x00F8	W	0x3430322A	UART Component Version
UART_CTR	0x00FC	W	0x44570110	Component Type Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

17.4.3 Detail Register Description

UART_RBR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	data_input Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

UART_DLL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	baud_rate_divisor_l Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.

UART_THR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	data_output Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full.. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_DLH

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	baud_rate_divisor_h Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.

UART_IER

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	prog_thre_int_en Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. 1'b0: Disabled 1'b1: Enabled
6:4	RO	0x0	reserved
3	RW	0x0	modem_status_int_en Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	receive_line_status_int_en Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
1	RW	0x0	trans_hold_empty_int_en Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	receive_data_available_int_en Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1'b0: Disabled 1'b1: Enabled

UART_FCR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	WO	0x0	rcvr_trigger at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to "DMA Suppor". The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full

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Bit	Attr	Reset Value	Description
5:4	WO	0x0	tx_empty_trigger TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to " DMA Support". The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full
3	WO	0x0	dma_mode DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support. 1'b0: Mode 0 1'b1: Mode 1
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	fifo_en FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

UART_IIR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RO	0x0	fifos_en FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 2'b00: Disabled 2'b11: Enabled
5:4	RO	0x0	reserved
3:0	RO	0x1	int_id Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 4'b0000: Modem status 4'b0001: No interrupt pending 4'b0010: THR empty 4'b0100: Received data available 4'b0110: Receiver line status 4'b0111: Busy detect 4'b1100: Character timeout

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Bit	Attr	Reset Value	Description
			The interrupt priorities are split into four levels that are detailed in Table X. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

UART_LCR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	div_lat_access Divisor Latch Access Bit.Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	RW	0x0	break_ctrl Break Control Bit.This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	RW	0x0	stick_parity If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	RW	0x0	even_parity_sel Even Parity Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	RW	0x0	parity_en Parity Enable. Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 1'b0: Parity disabled 1'b1: Parity enabled
2	RW	0x0	stop_bits_num Number of stop bits. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number

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Bit	Attr	Reset Value	Description
			of stop bits selected, the receiver checks only the first stop bit. 1'b0: 1 stop bit 1'b1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit.
1:0	RW	0x0	data_length_sel Data Length Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 2'b00: 5 bits 2'b01: 6 bits 2'b10: 7 bits 2'b11: 8 bits

UART_MCR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sir_mode_en SIR Mode Enable. Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in "IrDA 1.0 SIR Protocol". 1'b0: IrDA SIR Mode disabled 1'b1: IrDA SIR Mode enabled
5	RW	0x0	auto_flow_ctrl_en Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in "Auto Flow Control". 1'b0: Auto Flow Control Mode disabled 1'b1: Auto Flow Control Mode enabled
4	RW	0x0	loopback LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	RW	0x0	out2 OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 1'b0: Out2_n de-asserted (logic 1) 1'b1: Out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.

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Bit	Attr	Reset Value	Description
2	RW	0x0	out1 OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 1'b0: Out1_n de-asserted (logic 1) 1'b1: Out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	RW	0x0	req_to_send Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	RW	0x0	data_terminal_ready Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 1'b0: dtr_n de-asserted (logic 1) 1'b1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive

UART_LSR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	receiver_fifo_error Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 1'b0: No error in RX FIFO 1'b1: Error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	RO	0x1	trans_empty Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.

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Bit	Attr	Reset Value	Description
5	RO	0x1	trans_hold_reg_empty Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	RO	0x0	break_int Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RO	0x0	framing_error Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No framing error 1'b1: Framing error Reading the LSR clears the FE bit.
2	RO	0x0	parity_error Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No parity error 1'b1: Parity error Reading the LSR clears the PE bit.

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Bit	Attr	Reset Value	Description
1	RO	0x0	overrun_error Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 1'b0: No overrun error 1'b1: Overrun error Reading the LSR clears the OE bit.
0	RO	0x0	data_ready Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 1'b0: No data ready 1'b1: Data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

UART_MSR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	data_carrior_detect Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 1'b0: dcd_n input is de-asserted (logic 1) 1'b1: dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	RO	0x0	ring_indicator Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 1'b0: ri_n input is de-asserted (logic 1) 1'b1: ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	RO	0x0	data_set_ready Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. 1'b0: dsr_n input is de-asserted (logic 1) 1'b1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).

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Bit	Attr	Reset Value	Description
4	RO	0x0	clear_to_send Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. 1'b0: cts_n input is de-asserted (logic 1) 1'b1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RO	0x0	delta_data_carrier_detect Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 1'b0: No change on dcd_n since last read of MSR 1'b1: Change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	RO	0x0	trailing_edge_ring_indicator Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 1'b0: No change on ri_n since last read of MSR 1'b1: Change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	RO	0x0	delta_data_set_ready Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 1'b0: No change on dsr_n since last read of MSR 1'b1: Change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RO	0x0	delta_clear_to_send Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 1'b0: No change on ctsdsr_n since last read of MSR 1'b1: Change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

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UART_SCR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	temp_store_space Scratchpad register.This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

UART_SRBR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	shadow_rbr This is a shadow register for the RBR and has been allocated sixteen 32-bit locations (0x30-0x6c) so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs.

UART_STHR

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	shadow_thr This is a shadow register for the THR and has been allocated sixteen 32-bit locations(0x30-0x6c) so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_FAR

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	fifo_access_test_en Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 1'b0: FIFO access mode disabled 1'b1: FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty.

UART_TFR

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	trans_fifo_read Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR.

UART_RFW

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	WO	0x0	receive_fifo_framing_error Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	WO	0x0	receive_fifo_parity_error Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	WO	0x00	receive_fifo_write Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

UART_USR

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Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	receive_fifo_full Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. 1'b0: Receive FIFO not full 1'b1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	RO	0x0	receive_fifo_not_empty Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. 1'b0: Receive FIFO is empty 1'b1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	RO	0x1	trasn_fifo_empty Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	RO	0x1	trans_fifo_not_full Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. 1'b0: Transmit FIFO is full 1'b1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	RO	0x0	uart_busy UART Busy. This is indicates that a serial transfer is in progress, when cleared indicates that the DW_apb_uart is idle or inactive. 1'b0: DW_apb_uart is idle or inactive 1'b1: DW_apb_uart is busy (actively transferring data) Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock.

UART_TFL

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	trans_fifo_level Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.

UART_RFL

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	receive_fifo_level Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.

UART_SRR

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	uart_reset UART Reset. This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.

UART_SRTS

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_req_to_send Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.

UART_SBCR

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Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_break_ctrl Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver.

UART_SDMAM

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_dma_mode Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). 1'b0: Mode 0 1'b1: Mode 1

UART_SFE

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_fifo_en Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.

UART_SRT

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	shadow_rcvr_trigger Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store thepreviously written value to the FCR in memory and having to mask thisvalue so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which theReceived Data Available Interrupt is generated. It also determines when thedma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger

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Bit	Attr	Reset Value	Description
			levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full

UART_STET

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	shadow_tx_empty_trigger Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full

UART_HTX

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	halt_tx_en This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 1'b0: Halt TX disabled 1'b1: Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation.

UART_DMASA

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	dma_software_ack This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

UART_CPR

Address: **Operational Base** + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x04	fifo_mode 8'h4 means FIFO mode is 64.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RO	0x1	dma_extra 1'b1 means DMA_EXTRA enabled.
12	RO	0x1	uart_add_encoded_params 1'b1 means UART_ADD_ENCODED_PARAMS enabled.
11	RO	0x1	shadow 1'b1 means SHADOW mode enabled.
10	RO	0x1	fifo_stat 1'b1 means FIFO_STAT enabled.
9	RO	0x1	fifo_access 1'b1 means FIFO ACCESS enabled.
8	RO	0x1	new_feat 1'b1 means Additional features enabled.
7	RO	0x1	sir_lp_mode 1'b1 means SIR_LP mode enabled.
6	RO	0x1	sir_mode 1'b1 means SIR mode enabled.
5	RO	0x1	thre_mode 1'b1 means THRE mode enabled.
4	RO	0x1	afce_mode 1'b1 means AFCE mode enabled.
3:2	RO	0x0	reserved
1:0	RO	0x2	apb_data_width 2'b10 means APB data width is 32bit.

UART_UCV

Address: **Operational Base** + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3430322a	ver ASCII value for each number in the version.

UART_CTR

Address: **Operational Base** + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x44570110	peripheral_id This register contains the peripherals identification code.

17.5 Interface Description

Table 17-1 UART interface description

Module Pin	Direction	Pad Name	IOMUX Setting
UART0mux0 Interface			
uart0_sin	I	UART0_RX_M0/JTAG_CPU_MCU_TMS_M0/GPIO0_D0_u	GPIO0_IOC_GPIO0D_IOMUX_SEL_L[3:0]=4'h1
uart0_sout	O	UART0_TX_M0/JTAG_CPU_MCU_TCK_M0/GPIO0_D1_u	GPIO0_IOC_GPIO0D_IOMUX_SEL_L[7:4]=4'h1
uart0_cts_n	I	Not support	
uart0_rts_n	O	Not support	
UART0mux1 Interface			
uart0_sin	I	SDMMC0_D0/UART0_RX_M1/UART7_RX_M1/SPI1_MOSI_M1/DSM_AUD_LP/GPIO1_B3_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h2
uart0_sout	O	SDMMC0_D1/UART0_TX_M1/UART7_TX_M1/SPI1_MISO_M1/DSM_AUD_LN/GPIO1_B4_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4'h2
uart0_cts_n	I	Not support	
uart0_rts_n	O	Not support	
UART1mux0 Interface			

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Module Pin	Direction	Pad Name	IOMUX Setting
uart1_sin	I	UART1_RX_M0/RGMII_TXD0_M1/I2S0_SDO1_M1/PWM4_M1/RMII_TXD0/GPIO1_D1_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_L[7:4]=4'h1
uart1_sout	O	UART1_TX_M0/RGMII_TXD1_M1/I2S0_SDO2_M1/PWM5_M1/RMII_TXD1/GPIO1_D2_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_L[11:8]=4'h1
uart1_cts_n	I	UART1_CTSN_M0/RGMII_RXD0_M1/I2S0_SDI3_M1/PWM7_M1/RMII_RXD0/GPIO1_D4_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H[3:0]=4'h1
uart1_rts_n	O	UART1_RTSN_M0/RGMII_TXEN_M1/I2S0_SDI2_M1/PWM6_M1/RMII_TXEN/GPIO1_D3_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_L[15:12]=4'h1
UART1mux1 Interface			
uart1_sin	I	VO_LCDC_D8/RGMII_RXD1_M0/UART1_RX_M1/PDM_SDI3_M1/I2C3_SDA_M1/GPIO4_A6_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H[11:8]=4'h3
uart1_sout	O	VO_LCDC_D1/RGMII_RXD0_M0/UART1_TX_M1/PDM_SDI2_M1/I2C3_SCL_M1/GPIO4_A5_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H[7:4]=4'h3
uart1_cts_n	I	VO_LCDC_D16/RGMII_RXER_M0/UART1_CTSN_M1/PDM_SDI1_M1/UART6_RX_M1/GPIO4_B0_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'h3
uart1_rts_n	O	VO_LCDC_D9/RGMII_RXDV_M0/UART1_RTSN_M1/PDM_SDI0_M1/UART6_TX_M1/GPIO4_A7_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H[15:12]=4'h3
UART2mux0 Interface			
uart2_sin	I	UART2_RX_M0/PWM6_M0/NPU_AVS/CAN1_RX_M1/GPIO0_C1_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L[7:4]=4'h1
uart2_sout	O	UART2_TX_M0/PWM7_M0/GPU_AVS/CAN1_TX_M1/GPIO0_C0_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L[3:0]=4'h1
uart2_cts_n	I	UART2_CTSN_M0/PWM5_M0/SPI0_CSN0_M0/GPIO0_C2_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L[11:8]=4'h1
uart2_rts_n	O	UART2_RTSN_M0/PWM0_M0/SPI0_CLK_M0/GPIO0_C3_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L[15:12]=4'h1
UART2mux1 Interface			
uart2_sin	I	I2C3_SDA_M0/UART2_RX_M1/SPDIF_TX_M0/CAN0_RX_M0/UART5_RTSN_M1/GPIO3_A1_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'h2
uart2_sout	O	I2C3_SCL_M0/UART2_TX_M1/PDM_SDI3_M0/CAN0_TX_M0/UART5_CTSN_M1/GPIO3_A0_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'h2
uart2_cts_n	I	I2S0_MCLK_M0/UART2_CTSN_M1/PDM_CLK1_M0/GPIO3_A2_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'h2
uart2_rts_n	O	I2S0_SCLK_M0/UART2_RTSN_M1/GPIO3_A3_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4'h2
UART3mux0 Interface			
uart3_sin	I	VO_LCDC_VSYNC/I2S1_SDO2_M0/UART9_RTSN_M0/SPI2_CSN0_M0/I2C1_SDA_M1/UART3_RX_M0/GPIO4_B5_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4'h6
uart3_sout	O	VO_LCDC_HSYNC/I2S1_SDO1_M0/UART9_CTSN_M0/SPI2_CSN1_M0/I2C1_SCL_M1/UART3_TX_M0/GPIO4_B4_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'h6
uart3_cts_n	I	VO_LCDC_DEN/I2S1_SDO3_M0/UART3_CTSN_M0/SPI2_CLK_M0/GPIO4_B6_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[11:8]=4'h3
uart3_rts_n	O	VO_LCDC_D10/I2S1_SDI1_M0/UART4_RX_M0/UART3_RTSN_M0/GPIO3_D1_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[7:4]=4'h4
UART3mux1 Interface			
uart3_sin	I	I2S1_SDO3_M1/I2S1_SDI1_M1/UART3_RX_M1/SPI0_MISO_M1/GPIO3_C0_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_L[3:0]=4'h3
uart3_sout	O	I2S1_SDO2_M1/I2S1_SDI2_M1/UART3_TX_M1/SPI0_CSN0_M1/I2C4_SDA_M0/CAN0_RX_M1/GPIO3_B7_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H[15:12]=4'h3

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Module Pin	Direction	Pad Name	IOMUX Setting
uart3_cts_n	I	I2S1_SDO1_M1/I2S1_SDI3_M1/UART3_CTSN_M1/SPI0_CSN1_M1/I2C4_SCL_M0/CAN0_TX_M1/GPIO3_B6_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'h3
uart3_rts_n	O	I2S1_SDI0_M1/ISP_FLASH_TRIGIN/UART3_RTSN_M1/GPIO3_C1_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_L[7:4]=4'h3
UART4mux0 Interface			
uart4_sin	I	VO_LCDC_D10/I2S1_SDI1_M0/UART4_RX_M0/UART3_RTSN_M0/GPIO3_D1_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[7:4]=4'h3
uart4_sout	O	VO_LCDC_D7/I2S1_SDI0_M0/UART4_TX_M0/GPIO3_D0_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4'h3
uart4_cts_n	I	VO_LCDC_D4/I2S1_SCLK_M0/UART4_CTSN_M0/PWM14_M0/GPIO3_C5_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4'h3
uart4_rts_n	O	VO_LCDC_D5/I2S1_LRCK_M0/UART4_RTSN_M0/PWM15_M0/GPIO3_C6_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H[11:8]=4'h3
UART4mux1 Interface			
uart4_sin	I	I2S2_SCLK_M0/RGMII_CLK_M1/UART4_RX_M1/SPI2_CSN1_M1/RMII_CLK/GPIO1_D5_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'h3
uart4_sout	O	I2S2_LRCK_M0/RGMII_RXDV_M1/UART4_TX_M1/SPI2_CSN0_M1/RMII_RXDV_CRS/GPIO1_D6_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H[11:8]=4'h3
uart4_cts_n	I	I2S2_SDI_M0/RGMII_RXER_M1/UART4_CTSN_M1/SPI2_MISO_M1/PWM15_M1/RMII_RXER/GPIO2_A0_d	GPIO2_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'h3
uart4_rts_n	O	I2S2_SDO_M0/RGMII_RXD1_M1/UART4_RTSN_M1/SPI2_MOSI_M1/PWM14_M1/RMII_RXD1/GPIO1_D7_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H[15:12]=4'h3
UART5mux0 Interface			
uart5_sin	I	SDMMC0_CMD/SPDIF_TX_M2/UART5_RX_M0/CAN1_RX_M0/GPIO1_B7_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4'h3
uart5_sout	O	SDMMC0_CLK/TEST_CLK_OUT/UART5_TX_M0/SPI1_CLK_M1/CAN1_TX_M0/GPIO1_C0_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L[3:0]=4'h3
uart5_cts_n	I	SDMMC0_D2/JTAG_CPU_MCU_TCK_M1/UART5_CTSN_M0/SPI1_CSN1_M1/PWM10_M0/DSM_AUD_RP/GPIO1_B5_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[7:4]=4'h3
uart5_rts_n	O	SDMMC0_D3/JTAG_CPU_MCU_TMS_M1/UART5_RTSN_M0/SPI1_CSN0_M1/PWM11_M0/DSM_AUD_RN/GPIO1_B6_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4'h3
UART5mux1 Interface			
uart5_sin	I	I2S0_SDO2_M0/I2S0_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEN_M1/UART5_RX_M1/GPIO3_A7_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_H[15:12]=4'h5
uart5_sout	O	I2S0_SDO1_M0/I2S0_SDI3_M0/PDM_CLK0_M0/PCIE20_CLKREQN_M1/UART5_TX_M1/GPIO3_A6_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_H[11:8]=4'h5
uart5_cts_n	I	I2C3_SCL_M0/UART2_TX_M1/PDM_SDI3_M0/CAN0_TX_M0/UART5_CTSN_M1/GPIO3_A0_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'h5
uart5_rts_n	O	I2C3_SDA_M0/UART2_RX_M1/SPDIF_TX_M0/CAN0_RX_M0/UART5_RTSN_M1/GPIO3_A1_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'h5
UART6mux0 Interface			
uart6_sin	I	UART6_RX_M0/CAN0_RX_M2/GPIO0_C7_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_H[15:12]=4'h1
uart6_sout	O	UART6_TX_M0/CAN0_TX_M2/GPIO0_C6_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_H[11:8]=4'h1
uart6_cts_n	I	UART6_CTSN_M0/PWM1_M0/SPI0_MOSI_M0/GPIO0_C4_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_H[3:0]=4'h1
uart6_rts_n	O	UART6_RTSN_M0/PWM2_M0/SPI0_MISO_M0/GPIO0_C5_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_H[7:4]=4'h1
UART6mux1 Interface			
uart6_sin	I	VO_LCDC_D16/RGMII_RXER_M0/UART1_CTSN_M1/PDM_SDI1_M1/UART6_RX_M1/GPIO4_B0_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'h5

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Module Pin	Direction	Pad Name	IOMUX Setting
uart6_sout	O	VO_LCDC_D9/RGMII_RXDV_M0/UART1_RTSN_M1/PDM_SDI0_M1/UART6_TX_M1/GPIO4_A7_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H[15:12]=4'h5
uart6_cts_n	I	VO_LCDC_D22/RGMII_TXD0_M0/UART6_CTSN_M1/SPI1_MOSI_M0/GPIO4_A2_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[11:8]=4'h3
uart6_rts_n	O	VO_LCDC_D23/RGMII_TXD1_M0/UART6_RTSN_M1/SPI1_MISO_M0/GPIO4_A3_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[15:12]=4'h3
UART7mux0 Interface			
uart7_sin	I	VO_LCDC_D6/I2S1_SDO0_M0/UART7_RX_M0/GPIO3_C7_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H[15:12]=4'h3
uart7_sout	O	VO_LCDC_D3/I2S1_MCLK_M0/UART7_TX_M0/GPIO3_C4_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4'h3
uart7_cts_n	I	VO_LCDC_D11/I2S1_SDI2_M0/UART7_CTSN_M0/SPI2_MISO_M0/I2C2_SCL_M1/GPIO3_D2_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[11:8]=4'h3
uart7_rts_n	O	VO_LCDC_D12/I2S1_SDI3_M0/UART7_RTSN_M0/SPI2_MOSI_M0/I2C2_SDA_M1/GPIO3_D3_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L[15:12]=4'h3
UART7mux1 Interface			
uart7_sin	I	SDMMC0_D0/UART0_RX_M1/UART7_RX_M1/SPI1_MOSI_M1/DSM_AUD_LP/GPIO1_B3_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h3
uart7_sout	O	SDMMC0_D1/UART0_TX_M1/UART7_TX_M1/SPI1_MISO_M1/DSM_AUD_LN/GPIO1_B4_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4'h3
uart7_cts_n	I	Not support	
uart7_rts_n	O	Not support	
UART8mux0 Interface			
uart8_sin	I	I2S1_SCLK_M1/CAM_CLK1_OUT_M0/UART8_RX_M0/GPIO3_B3_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_L[15:12]=4'h3
uart8_sout	O	I2S1_MCLK_M1/CAM_CLK0_OUT_M0/UART8_TX_M0/GPIO3_B2_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_L[11:8]=4'h3
uart8_cts_n	I	I2S1_LRCK_M1/CAM_CLK2_OUT/UART8_CTSN_M0/SPI0_MOSI_M1/PWM12_M1/GPIO3_B4_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H[3:0]=4'h3
uart8_rts_n	O	I2S1_SDO0_M1/CAM_CLK3_OUT/UART8_RTSN_M0/SPI0_CLK_M1/PWM13_M1/GPIO3_B5_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'h3
UART8mux1 Interface			
uart8_sin	I	VO_LCDC_D14/RGMII_TXD3_M0/UART8_RX_M1/I2S2_SDO_M1/GPIO3_D5_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[7:4]=4'h3
uart8_sout	O	VO_LCDC_D13/RGMII_TXD2_M0/UART8_TX_M1/I2S2_SDI_M1/GPIO3_D4_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[3:0]=4'h3
uart8_cts_n	I	VO_LCDC_D19/RGMII_RXD2_M0/UART8_CTSN_M1/SPI1_CSN0_M0/GPIO3_D7_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_H[15:12]=4'h3
uart8_rts_n	O	VO_LCDC_D20/RGMII_RXD3_M0/UART8_RTSN_M1/SPI1_CSN1_M0/GPIO4_A0_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4'h3
UART9mux0 Interface			
uart9_sin	I	VO_LCDC_D18/RGMII_MDIO_M0/UART9_RX_M0/GPIO4_B3_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'h3
uart9_sout	O	VO_LCDC_D2/RGMII_MDC_M0/UART9_TX_M0/GPIO4_B2_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_L[11:8]=4'h3
uart9_cts_n	I	VO_LCDC_HSYNC/I2S1_SDO1_M0/UART9_CTSN_M0/SPI2_CSN1_M0/I2C1_SCL_M1/UART3_TX_M0/GPIO4_B4_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'h3
uart9_rts_n	O	VO_LCDC_VSYNC/I2S1_SDO2_M0/UART9_RTSN_M0/SPI2_CSN0_M0/I2C1_SDA_M1/UART3_RX_M0/GPIO4_B5_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4'h3
UART9mux1 Interface			
uart9_sin	I	I2C5_SDA_M0/ISP_FLASH_TRIGOUT/UART9_RX_M1/GPIO3_C3_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_L[15:12]=4'h3

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Module Pin	Direction	Pad Name	IOMUX Setting
uart9_sout	O	I2C5_SCL_M0/ISP_PRELIGHT_TRIGOUT/UART9_TX_M1/GPIO3_C2_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_L[11:8]=4'h3
uart9_cts_n	I	Not support	
uart9_rts_n	O	Not support	

Notes: I=input, O=output, I/O=input/output, bidirectional. spi_csn1 can only be used in master mode

17.6 Application Notes

17.6.1 None FIFO Mode Transfer Flow

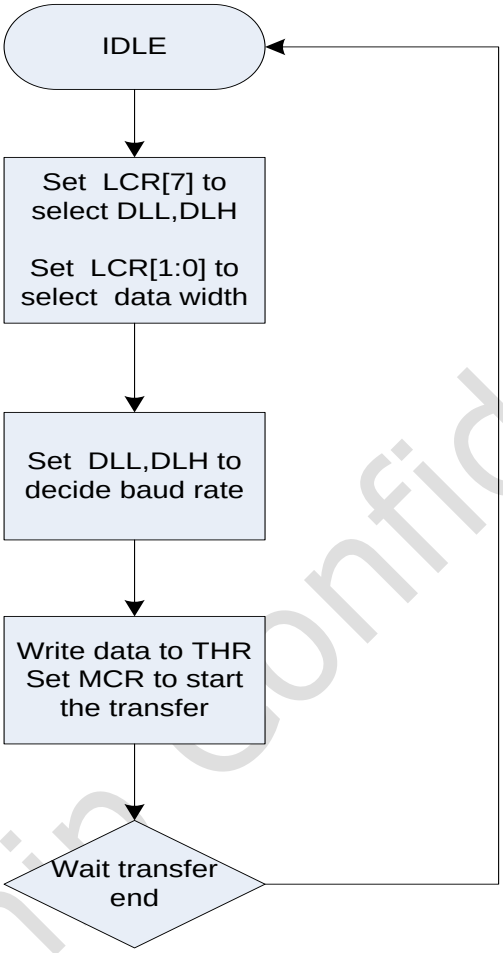

Fig. 17-8 UART none fifo mode

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17.6.2 FIFO Mode Transfer Flow

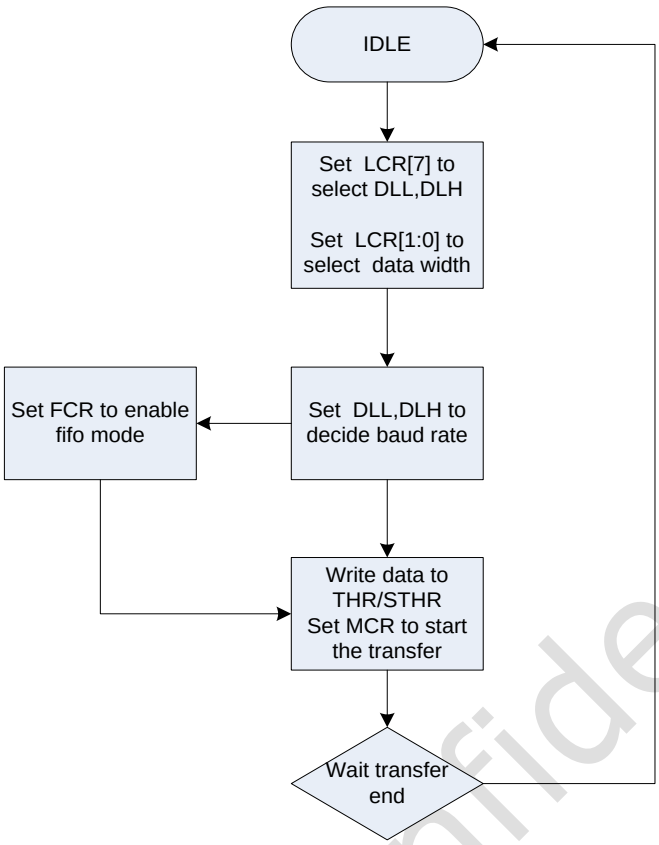

Fig. 17-9 UART fifo mode

The UART is an APB slave performing:
Serial-to-parallel conversion on data received from a peripheral device.
Parallel-to-serial conversion on data transmitted to the peripheral device.
The CPU reads and writes data and control/status information through the APB interface.
The transmitting and receiving paths are buffered with internal FIFO memories enabling up to 64-bytes to be stored independently in both transmit and receive modes. A baud rate generator can generate a common transmit and receive internal clock input. The baud rates will depend on the internal clock frequency. The UART will also provide transmit, receive and exception interrupts to system. A DMA interface is implemented for improving the system performance.

17.6.3 Baud Rate Calculation

The following table provides some reference configuration for different UART baud rates.

Table 17-2 UART baud rate configuration

Baud Rate	Reference Configuration
115.2 Kbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 32/20625 to get 115.2KHz clock;
460.8 Kbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 128/20625 to get 460.8KHz clock;
921.6 Kbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 256/20625 to get 921.6KHz clock;
1.5 Mbps	Choose default 24M clock; Divide 24M clock by 16 to get 1.5MHz clock;
3 Mbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 4/99 to get 3MHz clock;
4 Mbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 16/297 to get 4MHz clock;

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Chapter 18 Inter-Integrated Circuit (I2C)

18.1 Overview

The Inter-Integrated Circuit (I2C) is a two wired (SCL and SDA), bi-directional serial bus that provides an efficient and simple method of information exchange between devices. This I2C bus controller supports master mode acting as a bridge between AMBA protocol and generic I2C bus system.

I2C Controller supports the following features:

- Support 8 independent I2C: I2C0~7, with 13 pairs IOs.
- Item Compatible with I2C-bus
- AMBA APB slave interface
- Supports master mode of I2C bus
- Software programmable clock frequency and transfer rate up to 400Kbit/sec
- Supports 7 bits and 10 bits addressing modes
- Interrupt or polling driven multiple bytes data transfer
- Clock stretching and wait state generation
- Filter out glitch on SCL and SDA

18.2 Block Diagram

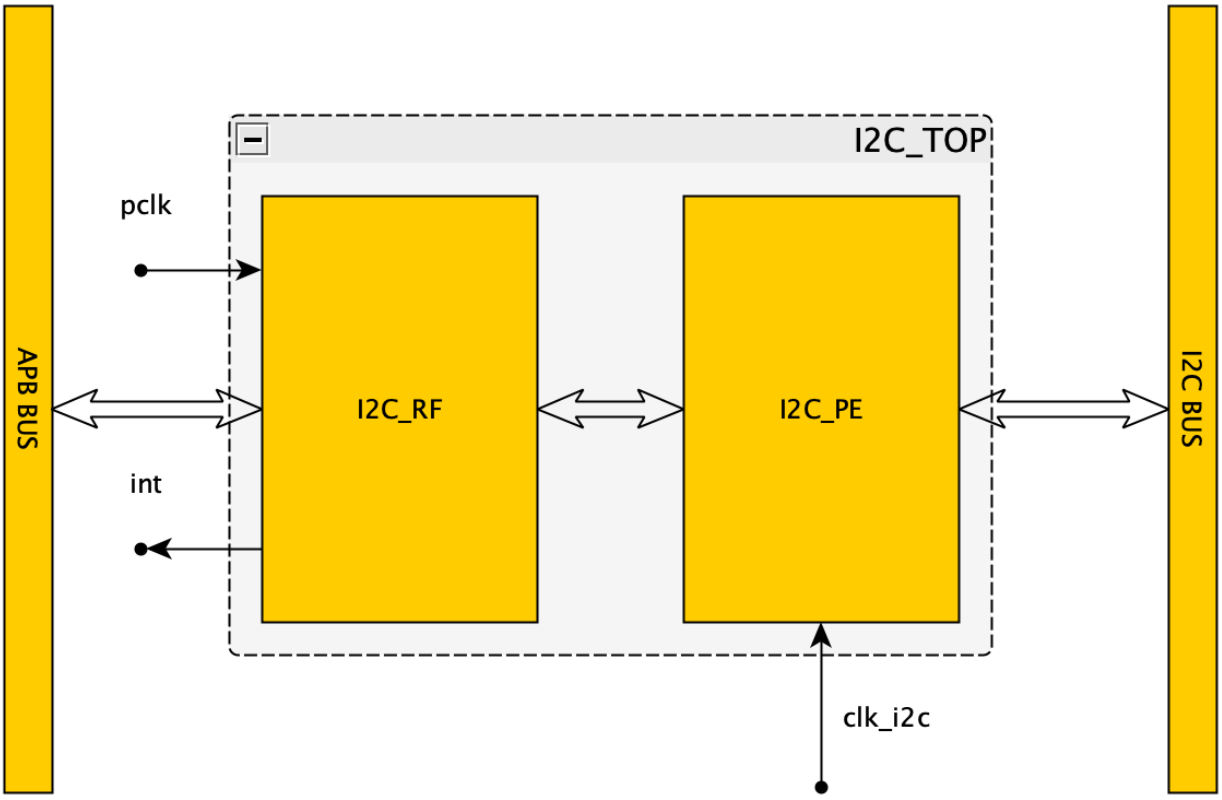

Fig.18-1 I2C architecture

18.2.1 I2C_RF

I2C_RF module is used to control the I2C controller operation by the host with APB interface. It implements the register set and the interrupt functionality. The I2C_RF component operates synchronously with the pclk.

18.2.2 I2C_PE

I2C_PE module implements the I2C master operation for transmit data to and receive data from other I2C devices. The I2C master controller operates synchronously with the clk_i2c.

18.2.3 I2C_TOP

I2C_TOP module is the top module of the I2C controller.

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18.3 Function Description

This chapter provides a description about the functions and behavior under various conditions.
The I2C controller supports only Masterfunction. Itsupports the 7-bits/10-bits addressing mode and support general call address. The maximum clock frequency and transfer rate can be up to 400Kbit/sec.
The operations of I2C controller is divided to 2 parts and described separately: initialization and master mode programming.

18.3.1 Initialization

The I2C controller is based on AMBA APB bus architecture and usually is part of a SOC. So before I2C operates, some system setting and configuration must be conformed, which includes:

- I2C interrupt connection type: CPU interrupt scheme should be considered. If the I2C interrupt is connected to extra Interrupt Controller module, we need decide the INTC vector.
- I2C Clock Rate: The I2C controller uses the APB clock to configure controller and uses clk_i2c as the working clock. The correct register setting is subject to the system requirement.

18.3.2 Master Mode Programming

- SCL Clock
  When the I2C controller is programmed in Master mode, the SCL frequency is determined by I2C_CLKDIV register. The SCL frequency is calculated by the following formula:
  SCL Divisor = 8*(CLKDIVL + 1 + CLKDIVH + 1); clk_i2c = 100MHz~200MHz.
  SCL = clk_i2c/ SCLK Divisor.
- Data Receiver Register Access
  When the I2C controller received MRXCNT bytes data, CPU can get the data through register RXDATA0 ~ RXDATA7. The controller can receive up to 32 bytes' data in one transaction.
  When MRXCNT register is written, the I2C controller will start to drive SCL to receive data.
- Transmit Transmitter Register
  Data to transmit are written to TXDATA0~7 by CPU. The controller can transmit up to 32 bytes' data in one transaction. The lower byte will be transmitted first.
  When MTXCNT register is written, the I2C controller will start to transmit data.
- Start Command
  Write 1 to I2C_CON[3], the controller will send I2C start command.
- Stop Command
  Write 1 to I2C_CON[4], the controller will send I2C stop command.
- I2C Operation mode
  There are four i2c operation modes.
  - When I2C_CON[2:1] is 2'b00, the controller transmit all valid data in TXDATA0~TXDATA7 byte by byte. The controller will transmit lower byte first.
  - When I2C_CON[2:1] is 2'b01, the controller will transmit device address in MRXADDR first (Write/Read bit = 0) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enter receive mode.
  - When I2C_CON[2:1] is 2'b10, the controller is in receive mode, it will trigger clock to read MRXCNT byte data.
  - When I2C_CON[2:1] is 2'b11, the controller will transmit device address in MRXADDR first (Write/Read bit = 1) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enter receive mode.

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- Read/Write Command
  - When I2C_OPMODE(I2C_CON[2:1]) is 2'b01 or 2'b11, the Read/Write command bit is decided by controller itself.
  - In RX only mode (I2C_CON[2:1] is 2'b10), the Read/Write command bit is decided by MRXADDR[0].
  - In TX only mode (I2C_CON[[2:1] is 2'b00), the Read/Write command bit is decided by TXDATA[0].
- Master Interrupt Condition

  There are 7 interrupt bits in I2C_ISR register related to master mode.
  - Byte transmitted finish interrupt (Bit 0): The bit is asserted when Master completed transmitting a byte.
  - Byte received finish interrupt (Bit 1): The bit is asserted when Master completed receiving a byte.
  - MTXCNT bytes data transmitted finish interrupt (Bit 2): The bit is asserted when Master completed transmitting MTXCNT bytes.
  - MRXCNT bytes data received finish interrupt (Bit 3): The bit is asserted when Master completed receiving MRXCNT bytes.
  - Start interrupt (Bit 4): The bit is asserted when Master finished asserting start command to I2C bus.
  - Stop interrupt (Bit 5): The bit is asserted when Master finished asserting stop command to I2C bus.
  - NAK received interrupt (Bit 6): The bit is asserted when Master received a NAK handshake.
- Last byte acknowledge control
  - If I2C_CON[5] is 1, the I2C controller will transmit NAK handshake to slave when the last byte received in RX only mode.
  - If I2C_CON[5] is 0, the I2C controller will transmit ACK handshake to slave when the last byte received in RX only mode.
- How to handle NAK handshake received
  - If I2C_CON[6] is 1, the I2C controller will stop all transactions when NAK handshake received. And the software should take responsibility to handle the problem.
  - If I2C_CON[6] is 0, the I2C controller will ignore all NAK handshake received.
- I2C controller data transfer waveform
  - Bit transferring
    - Data Validity

      The SDA line must be stable during the high period of SCL, and the data on SDA line can only be changed when SCL is in low state.

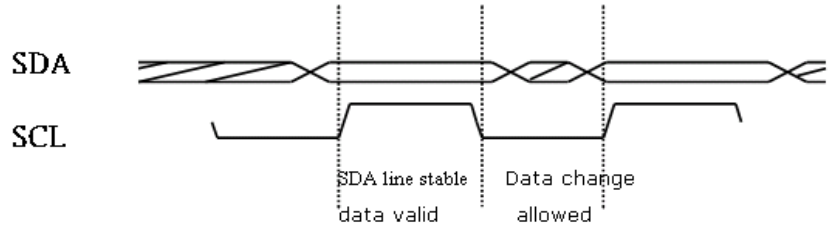

Fig.18-2 I2C DATA Validity

    - START and STOP conditions

      START condition occurs when SDA goes low while SCL is in high period. STOP condition is generated when SDA line goes high while SCL is in high state.

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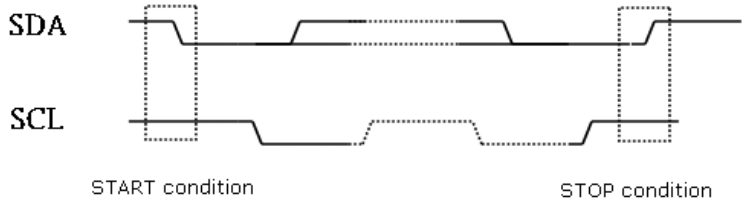

Fig.18-3 I2C Start and stop conditions

- Data transfer
  - Acknowledge

    After a byte of data transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK signal on SDA line, if the receiver pulls SDA line to low, it means "ACK", on the contrary, it's "NOT ACK".

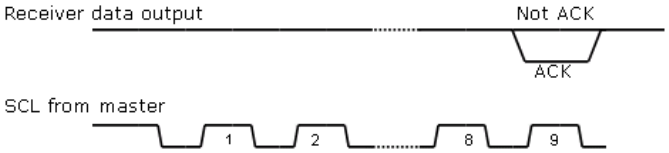

Fig.18-4 I2C Acknowledge

  - Byte transfer

    The master own I2C bus might initiate multi byte to transfer to a slave. The transfer starts from a "START" command and ends in a "STOP" command. After every byte transfer, the receiver must reply an ACK to transmitter.

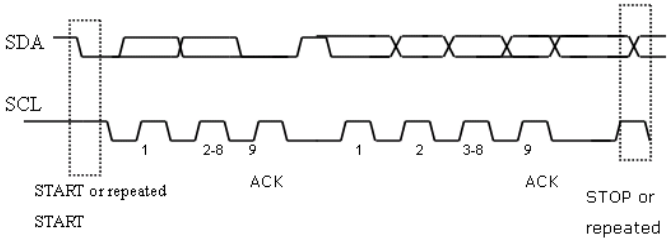

Fig.18-5 I2C byte transfer

18.4 Register Description

18.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
I2C0	0xFF200000
I2C1	0xFFA00000
I2C2	0xFFA10000
I2C3	0xFFA20000
I2C4	0xFFA30000
I2C5	0xFFA40000

18.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKI2C_CON	0x0000	W	0x00050000	Control register
RKI2C_CLKDIV	0x0004	W	0x00000001	Clock divider register I2C CLK = PCLK / (16*CLKDIV)
RKI2C_MRXADDR	0x0008	W	0x00000000	The slave address accessed for master rx mode

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Name	Offset	Size	Reset Value	Description
RKI2C_MRXRADDR	0x000C	W	0x00000000	The slave register address accessed for master rx mode
RKI2C_MTXCNT	0x0010	W	0x00000000	Master transmit count, specify the total bytes to be transmit (0~32)
RKI2C_MRXCNT	0x0014	W	0x00000000	Master rx count, specify the total bytes to be recieved(0~32)
RKI2C_IEN	0x0018	W	0x00000000	Interrupt enable register
RKI2C_IPD	0x001C	W	0x00000000	Interrupt pending register
RKI2C_FCNT	0x0020	W	0x00000000	Finished count: the count of data which has been transmitted or received for debug purpose
RKI2C_SCL_OE_DB	0x0024	W	0x00000020	Slave hold debounce configure register
RKI2C_TXDATA0	0x0100	W	0x00000000	I2C tx data register 0
RKI2C_TXDATA1	0x0104	W	0x00000000	I2C tx data register 1
RKI2C_TXDATA2	0x0108	W	0x00000000	I2C tx data register 2
RKI2C_TXDATA3	0x010C	W	0x00000000	I2C tx data register 3
RKI2C_TXDATA4	0x0110	W	0x00000000	I2C tx data register 4
RKI2C_TXDATA5	0x0114	W	0x00000000	I2C tx data register 5
RKI2C_TXDATA6	0x0118	W	0x00000000	I2C tx data register 6
RKI2C_TXDATA7	0x011C	W	0x00000000	I2C tx data register 7
RKI2C_RXDATA0	0x0200	W	0x00000000	I2C rx data register 0
RKI2C_RXDATA1	0x0204	W	0x00000000	I2C rx data register 1
RKI2C_RXDATA2	0x0208	W	0x00000000	I2C rx data register 2
RKI2C_RXDATA3	0x020C	W	0x00000000	I2C rx data register 3
RKI2C_RXDATA4	0x0210	W	0x00000000	I2C rx data register 4
RKI2C_RXDATA5	0x0214	W	0x00000000	I2C rx data register 5
RKI2C_RXDATA6	0x0218	W	0x00000000	I2C rx data register 6
RKI2C_RXDATA7	0x021C	W	0x00000000	I2C rx data register 7
RKI2C_ST	0x0220	W	0x00000000	Status debug register
RKI2C_DBGCTRL	0x0224	W	0x00000000	Debug config register
RKI2C_CON1	0x0228	W	0x00000000	Control register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.4.3 Detail Registers Description

RKI2C_CON

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0005	version Rki2c version information.
15:14	RW	0x0	stop_setup Stop setup config. TSU;sto = (stop_setup + 1) * T(SCL_HIGH) + Tclk_i2c.
13:12	RW	0x0	start_setup Start setup config. TSU;sta = (start_setup + 1) * T(SCL_HIGH) + Tclk_i2c. THD;sta = (start_setup + 2) * T(SCL_HIGH) - Tclk_i2c.
11:8	RW	0x0	data_upd_st SDA update point config. Used to config sda change state when scl is low, used to adjust setup/hold time. 4'bn: Thold = (n + 1) * Tclk_i2c. Note: 0 <= n <= 5
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	act2nak Operation when NAK handshake is received. 1'b0: Ignored. 1'b1: Stop transaction.
5	RW	0x0	ack Last byte acknowledge control in master receive mode. 1'b0: ACK 1'b1: NAK
4	RW	0x0	stop Stop enable, when this bit is written to 1, I2C will generate stop signal.
3	RW	0x0	start Start enable, when this bit is written to 1, I2C will generate start signal.
2:1	RW	0x0	i2c_mode I2c mode select. 2'b00: Transmit only. 2'b01: Transmit address (device + register address) --> Restart --> Transmit address -> Receive only. 2'b10: Receive only. 2'b11: Transmit address (device + register address, write/read bit is 1) --> Restart --> Transmit address (device address) --> Receive data.
0	RW	0x0	i2c_en I2c module enable. 1'b0: Disable 1'b1: Enable

RKI2C_CLKDIV

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CLKDIVH SCL high level clock count. T(SCL_HIGH) = Tclk_i2c * (CLKDIVH + 1) * 8.
15:0	RW	0x0001	CLKDIVL SCL low level clock count. T(SCL_LOW) = Tclk_i2c * (CLKDIVL + 1) * 8.

RKI2C_MRXADDR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	addhvld Address high byte valid. 1'b0: Invalid 1'b1: Valid
25	RW	0x0	addmvld Address middle byte valid. 1'b0: Invalid 1'b1: Valid
24	RW	0x0	addlvld Address low byte valid. 1'b0: Invalid 1'b1: Valid

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Bit	Attr	Reset Value	Description
23:0	RW	0x000000	saddr Master address register. The lowest bit indicate write or read. 24 bits address register.

RKI2C_MRXRADDR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	sraddhvld Address high byte valid. 1'b0: Invalid 1'b1: Valid
25	RW	0x0	sraddmvld Address middle byte valid. 1'b0: Invalid 1'b1: Valid
24	RW	0x0	sraddlvld Address low byte valid. 1'b0: Invalid 1'b1: Valid
23:0	RW	0x000000	sraddr Slave register address accessed. 24 bits register address

RKI2C_MTXCNT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	mtxcnt Master transmit count. 6 bits counter

RKI2C_MRXCNT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	mrxcnt Master rx count. 6 bits counter

RKI2C_IEN

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	slavehdsclen Slave hold scl interrupt enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	nakrcvien NAK handshake received interrupt enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	stopien Stop operation finished interrupt enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	startien Start operation finished interrupt enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	mbrfien MRXCNT data received finished interrupt enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	mbtfien MTXCNT data transfer finished interrupt enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	brfien Byte rx finished interrupt enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	btfien Byte tx finished interrupt enable. 1'b0: Disable 1'b1: Enable

RKI2C_IPD

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	slavehdsclipd Slave hold scl interrupt pending bit. 1'b0: No interrupt available. 1'b1: Slave hold scl interrupt appear, write 1 to clear.
6	W1C	0x0	nakrcvipd NAK handshake received interrupt pending bit. 1'b0: No interrupt available. 1'b1: NAK handshake received interrupt appear, write 1 to clear.
5	W1C	0x0	stopipd Stop operation finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Stop operation finished interrupt appear, write 1 to clear.
4	W1C	0x0	startipd Start operation finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Start operation finished interrupt appear, write 1 to clear.
3	W1C	0x0	mbrfipd MRXCNT data received finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: MRXCNT data received finished interrupt appear, write 1 to clear.
2	W1C	0x0	mbtfipd MTXCNT data transfer finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: MTXCNT data transfer finished interrupt appear, write 1 to clear.

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Bit	Attr	Reset Value	Description
1	W1C	0x0	brfipd Byte rx finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Byte rx finished interrupt appear, write 1 to clear.
0	W1C	0x0	btfipd Byte tx finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Byte tx finished interrupt appear, write 1 to clear.

RKI2C_FCNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	fcnt The count of data which has been transmitted or received for debug purpose.

RKI2C_SCL_OE_DB

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x20	scl_oe_db Slave hold scl debounce. Cycles for debounce (unit: Tclk_i2c).

RKI2C_TXDATA0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata0 Data0 to be transmitted. 32 bits data

RKI2C_TXDATA1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata1 Data1 to be transmitted. 32 bits data

RKI2C_TXDATA2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata2 Data2 to be transmitted. 32 bits data

RKI2C_TXDATA3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata3 Data3 to be transmitted. 32 bits data

RKI2C_TXDATA4

Address: Operational Base + offset (0x0110)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata4 Data4 to be transmitted. 32 bits data

RKI2C_TXDATA5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata5 Data5 to be transmitted. 32 bits data

RKI2C_TXDATA6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata6 Data6 to be transmitted. 32 bits data

RKI2C_TXDATA7

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata7 Data7 to be transmitted. 32 bits data

RKI2C_RXDATA0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata0 Data0 received. 32 bits data

RKI2C_RXDATA1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata1 Data1 received. 32 bits data

RKI2C_RXDATA2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata2 Data2 received. 32 bits data

RKI2C_RXDATA3

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata3 Data3 received. 32 bits data

RKI2C_RXDATA4

Address: Operational Base + offset (0x0210)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata4 Data4 received. 32 bits data

RKI2C_RXDATA5

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata5 Data5 received. 32 bits data

RKI2C_RXDATA6

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata6 Data6 received. 32 bits data

RKI2C_RXDATA7

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata7 Data7 received. 32 bits data

RKI2C_ST

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	scl_st SCL status. 1'b0: SCL status low. 1'b0: SCL status high.
0	RO	0x0	sda_st SDA status. 1'b0: SDA status low. 1'b0: SDA status high.

RKI2C_DBGCTRL

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	h0_check_scl 1'b0: Check if scl been pull down by slave at the whole SCL_HIGH. 1'b1: Check if scl been pull down by slave only at the h0 of SCL_HIGH(SCL_HIGH including h0~h7).
13	RW	0x0	nak_release_scl 1'b0: Hold scl as low when recieved nack. 1'b1: Release scl as high when recieved nack.
12	RW	0x0	flt_en SCL edage glitch filter enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	slv_hold_scl_th Slave hold scl threshold = slv_hold_scl_db * Tclk_i2c.
7:4	RW	0x0	flt_r Filter scl rising edge glitches of width less than flt_r * Tclk_i2c.
3:0	RW	0x0	flt_f Filter scl falling edge glitches of width less than flt_f * Tclk_i2c.

RKI2C_CON1

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	auto_stop_nak Auto stop when i2c master recieved nak from slave. Work when CON1[0]=1'b1. 1'b0: Do not auto stop when recieved nak. 1'b1: Auto stop when recieved nak.
1	RW	0x0	auto_stop_tx_end Auto stop when i2c master tx end. Work when CON1[0]=1'b1. 1'b0: Do not auto stop when tx end. 1'b1: Auto stop when tx end.
0	RW	0x0	auto_stop Auto stop when i2c master recieved nak from slave or tx end. 1'b0: Do not auto stop when recieved nak or tx end. 1'b1: Auto stop when recieved nak or tx end.

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18.5 Interface Description

Table 18-1 I2C Interface Description

Module pin	Direction	Pin name	IOMUX
I2C0_SCL_M0	I/O	I2C0_SCL/GPIO0_B1_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_L [7:4] = 4'h1
I2C0_SDA_M0	I/O	I2C0_SDA/GPIO0_B2_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_L [11:8] = 4'h1
I2C1_SCL_M0	I/O	I2C1_SCL_M0/GPIO0_B3_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_L [15:12] = 4'h1
I2C1_SDA_M0	I/O	I2C1_SDA_M0/GPIO0_B4_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_H [3:0] = 4'h1
I2C1_SCL_M1	I/O	VO_LCDC_HSYNC/I2S1_SDO1_M0/UART9_CTSN_M0/SPI2_CSN1_M0/I2C1_SCL_M1/UART3_TX_M0/GPIO4_B4_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H[3:0] = 4'h5
I2C1_SDA_M1	I/O	VO_LCDC_VSYNC/I2S1_SDO2_M0/UART9_RTSN_M0/SPI2_CSN0_M0/I2C1_SDA_M1/UART3_RX_M0/GPIO4_B5_d	GPIO4_IOC_GPIO4B_IOMUX_SEL_H [7:4] = 4'h5
I2C2_SCL_M0	I/O	I2C2_SCL_M0/PCIE20_PERSTN_M0/GPIO0_B5_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_H [7:4] = 4'h1
I2C2_SDA_M0	I/O	I2C2_SDA_M0/PCIE20_WAKEN_M0/GPIO0_B6_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_H [11:8] = 4'h1
I2C2_SCL_M1	I/O	VO_LCDC_D11/I2S1_SDI2_M0/UART7_CTSN_M0/SPI2_MISO_M0/I2C2_SCL_M1/GPIO3_D2_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L [11:8] = 4'h5
I2C2_SDA_M1	I/O	VO_LCDC_D12/I2S1_SDI3_M0/UART7_RTSN_M0/SPI2_MOSI_M0/I2C2_SDA_M1/GPIO3_D3_d	GPIO3_IOC_GPIO3D_IOMUX_SEL_L [15:12] = 4'h5
I2C3_SCL_M0	I/O	I2C3_SCL_M0/UART2_TX_M1/PDM_SDI3_M0/CAN0_TX_M0/UART5_CTSN_M1/GPIO3_A0_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_L [3:0] = 3'h1
I2C3_SDA_M0	I/O	I2C3_SDA_M0/UART2_RX_M1/SPDIF_TX_M0/CAN0_RX_M0/UART5_RTSN_M1/GPIO3_A1_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_L [7:4] = 3'h1
I2C3_SCL_M1	I/O	VO_LCDC_D1/RGMII_RXD0_M0/UART1_TX_M1/PDM_SDI2_M1/I2C3_SCL_M1/GPIO4_A5_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H [7:4] = 4'h5
I2C3_SDA_M1	I/O	VO_LCDC_D8/RGMII_RXD1_M0/UART1_RX_M1/PDM_SDI3_M1/I2C3_SDA_M1/GPIO4_A6_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H [11:8] = 4'h5
I2C4_SCL_M0	I/O	I2S1_SDO1_M1/I2S1_SDI3_M1/UART3_CTSN_M1/SPI0_CSN1_M1/I2C4_SCL_M0/CAN0_TX_M1/GPIO3_B6_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H [11:8] = 4'h5
I2C4_SDA_M0	I/O	I2S1_SDO2_M1/I2S1_SDI2_M1/UART3_TX_M1/SPI0_CSN0_M1/I2C4_SDA_M0/CAN0_RX_M1/GPIO3_B7_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H [15:12] = 3'h5
I2C4_SCL_M1	I/O	SDMMC0_PWREN/I2C4_SCL_M1/PMU_DEBUG/GPIO0_A5_d	GPIO0_IOC_GPIO0A_IOMUX_SEL_H [3:0] = 4'h2
I2C4_SDA_M1	I/O	SDMMC0_DETN/I2C4_SDA_M1/GPIO0_A4_u	GPIO0_IOC_GPIO0A_IOMUX_SEL_H [7:4] = 4'h2
I2C5_SCL_M0	I/O	I2C5_SCL_M0/ISP_PRELIGHT_TRIGOUT/UART9_TX_M1/GPIO3_C2_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_L [11:8] = 3'h1
I2C5_SDA_M0	I/O	I2C5_SDA_M0/ISP_FLASH_TRIGOUT/UART9_RX_M1/GPIO3_C3_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_L [15:12] = 3'h1
I2C5_SCL_M1	I/O	SDMMC1_PWREN/RGMII_MDC_M1/PWM2_M1/I2C5_SCL_M1/RMII_MDC/GPIO1_C7_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_H [15:12] = 4'h4
I2C5_SDA_M1	I/O	SDMMC1_DETN/RGMII_MDIO_M1/PWM3_M1/I2C5_SDA_M1/RMII_MDIO/GPIO1_D0_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H [3:0] = 4'h4

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18.6 Application Notes

The I2C controller core operation flow chart below is to describe how the software configures and performs an I2C transaction through this I2C controller core. Descriptions are divided into 3 sections, transmit only mode, receive only mode, and mix mode. Users are strongly advised to follow:

- Transmit only mode (I2C_CON[1:0]=2'b00)

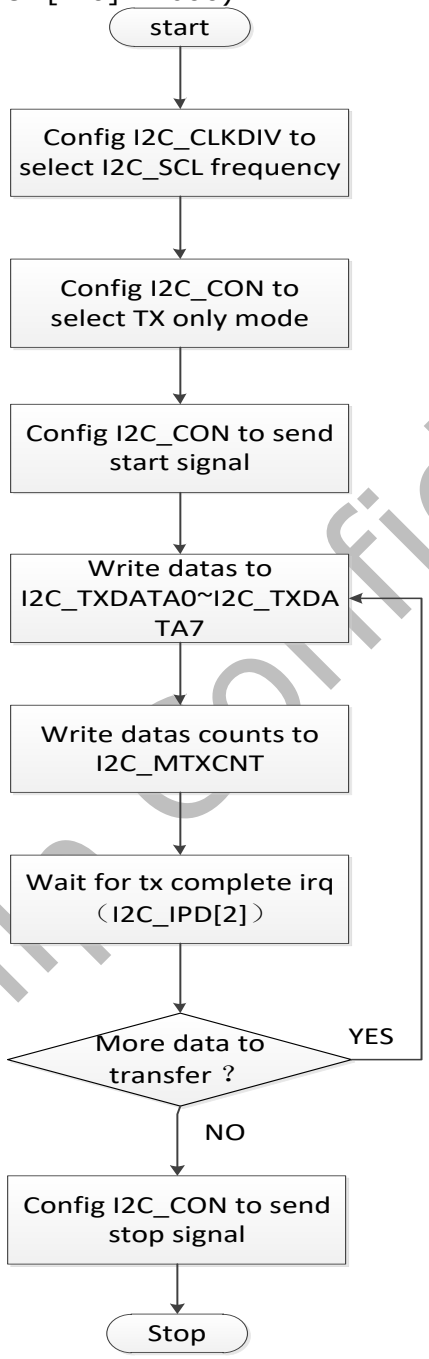

Fig.18-6 I2C Flow chat for transmit only mode

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- Receive only mode (I2C_CON[1:0]=2'b10)

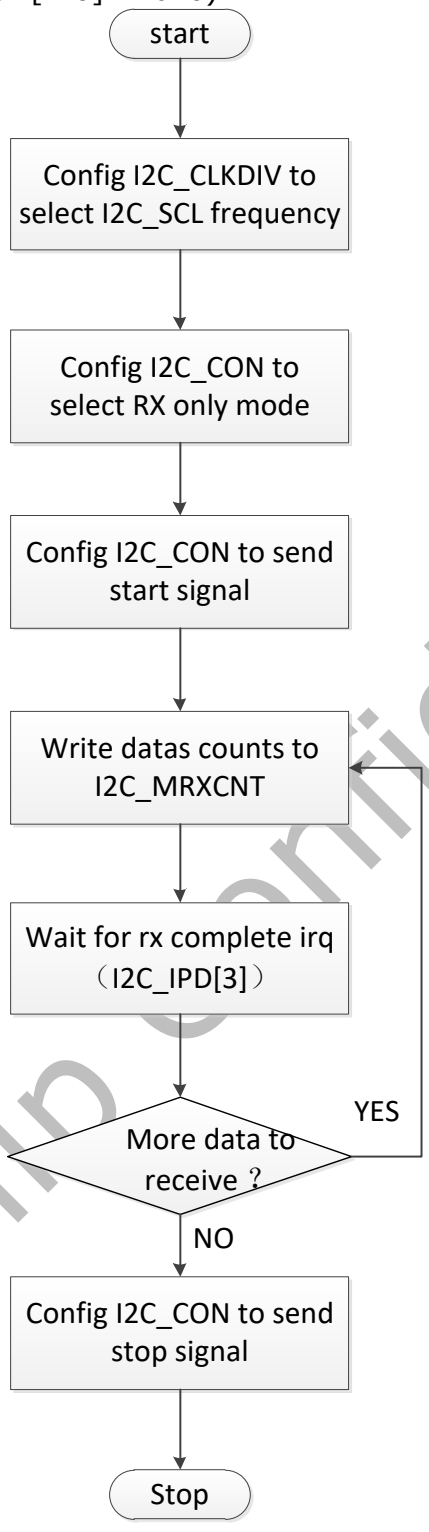

Fig.18-7 I2C Flow chat for receive only mode

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- Mix mode (I2C_CON[1:0]=2'b01 or I2C_CON[1:0]=2'b11)

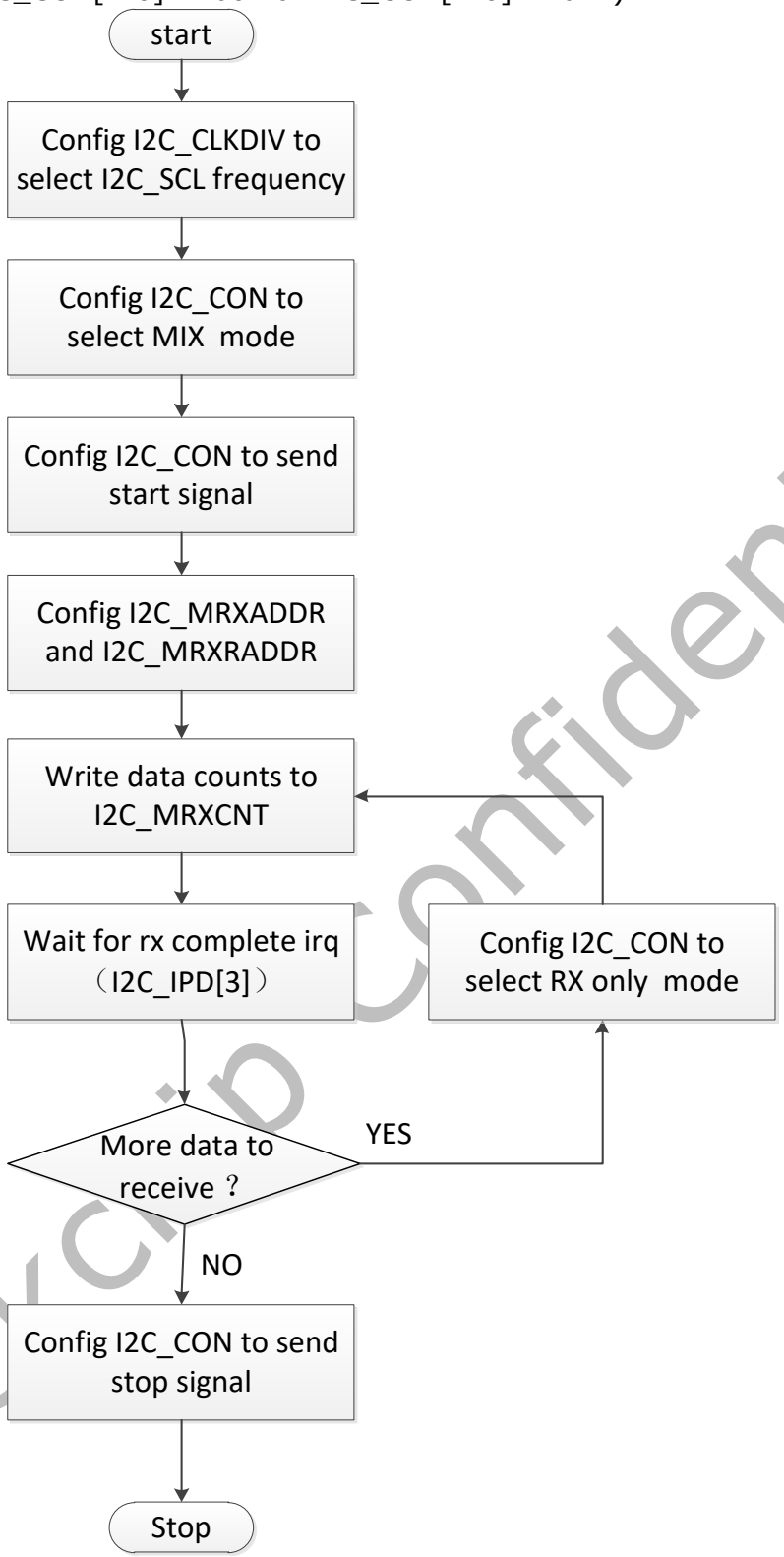

Fig.18-8 I2C Flow chat for mix mode

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Chapter 19 GPIO

19.1 Overview

GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. GPIO controls the output data and direction of external I/O pads. It can also read back the data on external pads using memory-mapped registers.
GPIO supports the following features:

- 32 bits APB data bus width
- Up to 32 independently configurable signals
- Software control registers with write mask for each bit of each signal
- Configurable debounce logic with a slow clock to debounce interrupts
- Configurable interrupt mode
- Two virtual OS with independent control registers can be supported
- In two virtual OS models, each OS has an independent interrupt
- Not in two virtual OS models, two interrupts with priority can be set

19.2 Block Diagram

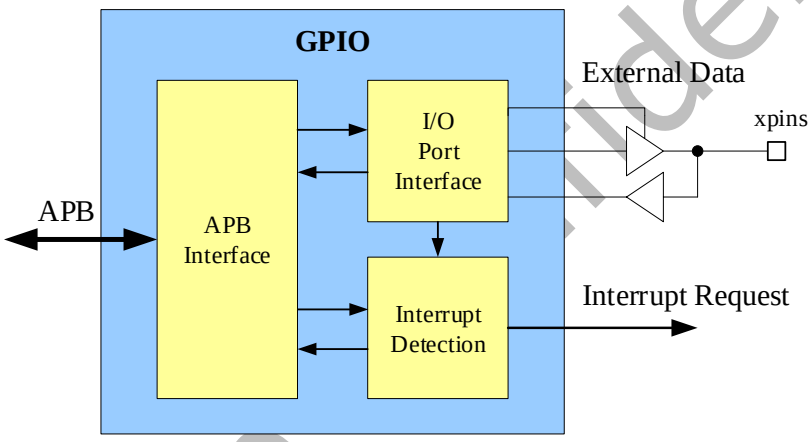

Fig. 19-1 GPIO Block Diagram

GPIO is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Interrupt Detection

Interrupt interface to or from interrupt controller.

19.3 Function Description

19.3.1 Data Control

Under software control, the data and direction control for the signal are sourced from the port data registers (GPIO_SWPORT_DR_L/GPIO_SWPORT_DR_H) and direction control registers (GPIO_SWPORT_DDR_L/GPIO_SWPORT_DRR_H).
The direction of the external I/O pad is controlled by the value of the port data direction registers. The data written to these memory-mapped registers gets mapped onto an output signal (gpio_port_ddr) of the GPIO peripheral. This output signal controls the direction of an external I/O pad. The default data direction is Input.
The data written to the port data registers drives the output buffer (gpio_port_dr) of the I/O pad.
External data are input into the external data signal (gpio_ext_port). Reading the external signal register (GPIO_EXT_PORT) shows the value of this signal, regardless of the direction. This register is read-only, meaning that it cannot be written from the APB software

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interface.

19.3.2 Interrupts

I/O port can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge
- Both the rising edge and the falling edge

The interrupts can be masked by programming the GPIO_INT_MASK_L/GPIO_INT_MASK_H registers. The interrupt status can be read before masking (GPIO_INT_RAWSTATUS) and after masking (GPIO_INT_STATUS).

For edge-sensitive interrupts, the Interrupt Service Routine (ISR) can clear the interrupt by writing a 1 to the corresponding bit of the GPIO_PORT_EOI_L/GPIO_PORT_EOI_H registers. This write operation also clears the interrupt status and raw status registers. Writing to the interrupt clear registers has no effect on level-sensitive interrupts. If level-sensitive interrupts cause the processor to interrupt, then the ISR can poll the interrupt raw status register until the interrupt source disappears, or it can write to the interrupt mask register to mask the interrupt before exiting the ISR. If the ISR exits without masking or disabling the interrupt prior to exiting, then the level-sensitive interrupt repeatedly requests an interrupt until the interrupt is cleared at the source.

The interrupts are combined into an active-high interrupt output signal. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its mask bit.

Whenever the I/O port is configured for interrupts, the data direction must be set to Input. If the data direction is reprogrammed to Output, then any pending edge-sensitive interrupts are not lost. However, no new interrupts are generated, and level-sensitive interrupts are lost.

Interrupt signals are internally synchronized to a system clock pclk_intr, which is connected to the APB bus clock pclk. Therefore, the pclk needs to be running for interrupt detection.

19.3.3 Debounce Operation

The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock.

When an input interrupt signal is debounced using a slow debounce clock (external input clock dbclk or internally divided clock dbclk_div), the signal must be active for a minimum of two cycles of the debounce clock to guarantee that it is registered. Any input pulse widths less than a debounce clock period are bounced. A pulse width between one and two debounce clock widths may or may not propagate, depending on its phase relationship to the debounce clock. If the input pulse spans two rising edges of the debounce clock, it is registered. If it spans only one rising edge, it is not registered.

The debounce function can be controlled by programming the debounce enable registers (GPIO_DEBOUNCE_L/GPIO_DEBOUNCE_H), debounce clock divide enable registers (GPIO_DBCLK_DIV_EN_L/GPIO_DBCLK_DIV_EN_H) and debounce clock divide control register (GPIO_DBCLK_DIV_CON).

19.3.4 Two OS Operations and Two Interrupt

To select this model, a virtual enable register should be set(GPIO_VIRTUAL_EN). Then all the configure can be allotted to two OS（for example OS_A and OS_B). OS_A will use the original address offset, and OS_B will use the offset + 0x1000. The 32-bit I/O port should also be allotted to the OS by setting reg group registers(GPIO_REG_GROUP_L and GPIO_REG_GROUP_H). Once the reg group is set, the I/O operation can only be used by the setting address offset. Each OS has own interrupt for the I/O port, and this is depended on the reg group.

If the virtual enable register is disabled, the reg group can also be used to allot I/O interrupt. These two independent interrupts may be used for priority interrupt settings.

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19.4 Register Description

19.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
GPIO0	0xFF260000
GPIO1	0xFF620000
GPIO2	0xFF630000
GPIO3	0xFFAC0000
GPIO4	0xFFAD0000

19.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO_SWPORT_DR_L	0x0000	W	0x00000000	Port Data Register (Low)
GPIO_SWPORT_DR_H	0x0004	W	0x00000000	Port Data Register (High)
GPIO_SWPORT_DDR_L	0x0008	W	0x00000000	Port Data Direction Register (Low)
GPIO_SWPORT_DDR_H	0x000C	W	0x00000000	Port Data Direction Register (High)
GPIO_INT_EN_L	0x0010	W	0x00000000	Interrupt Enable Register (Low)
GPIO_INT_EN_H	0x0014	W	0x00000000	Interrupt Enable Register (High)
GPIO_INT_MASK_L	0x0018	W	0x00000000	Interrupt Mask Register (Low)
GPIO_INT_MASK_H	0x001C	W	0x00000000	Interrupt Mask Register (High)
GPIO_INT_TYPE_L	0x0020	W	0x00000000	Interrupt Level Register (Low)
GPIO_INT_TYPE_H	0x0024	W	0x00000000	Interrupt Level Register (High)
GPIO_INT_POLARITY_L	0x0028	W	0x00000000	Interrupt Polarity Register (Low)
GPIO_INT_POLARITY_H	0x002C	W	0x00000000	Interrupt Polarity Register (High)
GPIO_INT_BOTHEDGE_L	0x0030	W	0x00000000	Interrupt Both Edge Type Register (Low)
GPIO_INT_BOTHEDGE_H	0x0034	W	0x00000000	Interrupt Both Edge Type Register (High)
GPIO_DEBOUNCE_L	0x0038	W	0x00000000	Debounce Enable Register (Low)
GPIO_DEBOUNCE_H	0x003C	W	0x00000000	Debounce Enable Register (High)
GPIO_DBCLK_DIV_EN_L	0x0040	W	0x00000000	DBCLK Divide Enable Register (Low)
GPIO_DBCLK_DIV_EN_H	0x0044	W	0x00000000	DBCLK Divide Enable Register (High)
GPIO_DBCLK_DIV_CON	0x0048	W	0x00000001	DBCLK Divide Control Register
GPIO_INT_STATUS	0x0050	W	0x00000000	Interrupt Status Register
GPIO_INT_RAWSTATUS	0x0058	W	0x00000000	Interrupt Raw Status Register
GPIO_PORT_EOI_L	0x0060	W	0x00000000	Interrupt Clear Register (Low)
GPIO_PORT_EOI_H	0x0064	W	0x00000000	Interrupt Clear Register (High)
GPIO_EXT_PORT	0x0070	W	0x00000000	External Port Data Register
GPIO_VER_ID	0x0078	W	0x0101157C	Version ID Register
GPIO_GPIO_REG_GROUP_L	0x0100	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP_H	0x0104	W	0x0000FFFF	GPIO Group Control
GPIO_GPIO_VIRTUAL_EN	0x0108	W	0x00000000	GPIO Virtual Enable

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

19.4.3 Detail Registers Description

GPIO_SWPORT_DR_L

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Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_low Output data for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the lower 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DR_H

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_high Output data for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the upper 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DDR_L

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_low Data direction for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the lower 16 bits of I/O Port.

GPIO_SWPORT_DDR_H

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	swport_ddr_high Data direction for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the upper 16 bits of I/O Port.

GPIO_INT_EN_L

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_en_low Allows each bit of the lower 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_EN_H

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_en_high Allows each bit of the upper 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_MASK_L

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_mask_low Controls whether an interrupt on the lower 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_MASK_H

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_mask_high Controls whether an interrupt on the upper 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_TYPE_L

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_type_low Controls the type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_TYPE_H

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_type_high Controls the type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

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GPIO_INT_POLARITY_L

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_polarity_low Controls the polarity of edge or level sensitivity that can occur on the lower 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_POLARITY_H

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_polarity_high Controls the polarity of edge or level sensitivity that can occur on the upper 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_BOTHEDGE_L

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_bothedge_low Controls the edge type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_low and int_polarity_low for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_low and int_polarity_low registers.

GPIO_INT_BOTHEDGE_H

Address: **Operational Base** + offset (0x0034)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_bothedge_high Controls the edge type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_high and int_polarity_high for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_high and int_polarity_high registers.

GPIO_DEBOUNCE_L

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_low Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DEBOUNCE_H

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_high Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DBCLK_DIV_EN_L

Address: **Operational Base** + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_low Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the lower 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_low is set to 0.

GPIO_DBCLK_DIV_EN_H

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_high Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the upper 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_high is set to 0.

GPIO_DBCLK_DIV_CON

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000001	dbclk_div_con dbclk_div = dbclk / (dbclk_div_con + 1)

GPIO_INT_STATUS

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_status Interrupt status of I/O Port.

GPIO_INT_RAWSTATUS

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_rawstatus Interrupt raw status of I/O Port (premasking bits).

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GPIO_PORT_EOI_L

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/WSC	0x0000	port_eoi_low Controls the clearing of edge type interrupts from the lower 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_PORT_EOI_H

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/WSC	0x0000	port_eoi_high Controls the clearing of edge type interrupts from the upper 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_EXT_PORT

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ext_port This register always reflects the value of the signals on the external I/O Port.

GPIO_VER_ID

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x0101157c	ver_id Version ID.

GPIO_GPIO_REG_GROUP_L

Address: **Operational Base** + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by OS_A with offset 0x0000 1'b0: GPIO control by OS_B with offset 0x1000 When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag 1'b0: GPIO interrupt connect to gpio_int_flag_exp

GPIO_GPIO_REG_GROUP_H

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xffff	gpio_reg_group_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by OS_A with offset 0x0000 1'b0: GPIO control by OS_B with offset 0x1000 When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag 1'b0: GPIO interrupt connect to gpio_int_flag_exp

GPIO_GPIO_VIRTUAL_EN

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	gpio_virtual_en 1'b1: Enable virtual, two OS supported 1'b0: Disable virtual.

19.5 Interface Description

Table 19-1 GPIO Interface Description

Module Pin	Pad Name	IOMUX Setting
GPIO0 Interface		
gpio0_port[0]	REF_CLK_OUT/GPIO0_A0_d	GPIO0A_IOMUX_SEL_L[2:0]=0
gpio0_port[1]	TSADC_SHUT_M0/TSADC_SHUT_ORG/GPIO0_A1_z	GPIO0A_IOMUX_SEL_L[6:4]=0
gpio0_port[2]	PWR_CTRL0/TSADC_SHUT_M1/GPIO0_A2_d	GPIO0A_IOMUX_SEL_L[10:8]=0
gpio0_port[3]	PWR_CTRL1/GPIO0_A3_u	GPIO0A_IOMUX_SEL_L[14:12]=0
gpio0_port[4]	SDMMC0_DETN/I2C4_SDA_M1/GPIO0_A4_u	GPIO0A_IOMUX_SEL_H[2:0]=0
gpio0_port[5]	SDMMC0_PWREN/I2C4_SCL_M1/PMU_DEBUG/GPIO0_A5_d	GPIO0A_IOMUX_SEL_H[6:4]=0

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Module Pin	Pad Name	IOMUX Setting
gpio0_port[6]	PCIE20_CLKREQN_M0/GPIO0_A6_d	GPIO0A_IOMUX_SEL_H[10:8]=0
gpio0_port[7]	PWM3_M0/GPIO0_A7_d	GPIO0A_IOMUX_SEL_H[14:12]=0
gpio0_port[8]	CLK_32K_IN/CLK0_32K_OUT/PCIE20_BUTTONRSTN/GPIO0_B0_d	GPIO0B_IOMUX_SEL_L[2:0]=0
gpio0_port[9]	I2C0_SCL/GPIO0_B1_d	GPIO0B_IOMUX_SEL_L[6:4]=0
gpio0_port[10]	I2C0_SDA/GPIO0_B2_d	GPIO0B_IOMUX_SEL_L[10:8]=0
gpio0_port[11]	I2C1_SCL_M0/GPIO0_B3_d	GPIO0B_IOMUX_SEL_L[14:12]=0
gpio0_port[12]	I2C1_SDA_M0/GPIO0_B4_d	GPIO0B_IOMUX_SEL_H[2:0]=0
gpio0_port[13]	I2C2_SCL_M0/PCIE20_PERSTN_M0/GPIO0_B5_d	GPIO0B_IOMUX_SEL_H[6:4]=0
gpio0_port[14]	I2C2_SDA_M0/PCIE20_WAKEN_M0/GPIO0_B6_d	GPIO0B_IOMUX_SEL_H[10:8]=0
gpio0_port[15]	SPI0_CSN1_M0/PWM4_M0/CPU_AVS/SPDIF_TX_M1/GPIO0_B7_d	GPIO0B_IOMUX_SEL_H[14:12]=0
gpio0_port[16]	UART2_TX_M0/PWM7_M0/GPU_AVS/CAN1_TX_M1/GPIO0_C0_d	GPIO0C_IOMUX_SEL_L[2:0]=0
gpio0_port[17]	UART2_RX_M0/PWM6_M0/NPU_AVS/CAN1_RX_M1/GPIO0_C1_d	GPIO0C_IOMUX_SEL_L[6:4]=0
gpio0_port[18]	UART2_CTSN_M0/PWM5_M0/SPI0_CSN0_M0/GPIO0_C2_d	GPIO0C_IOMUX_SEL_L[10:8]=0
gpio0_port[19]	UART2_RTSN_M0/PWM0_M0/SPI0_CLK_M0/GPIO0_C3_d	GPIO0C_IOMUX_SEL_L[14:12]=0
gpio0_port[20]	UART6_CTSN_M0/PWM1_M0/SPI0_MOSI_M0/GPIO0_C4_d	GPIO0C_IOMUX_SEL_H[2:0]=0
gpio0_port[21]	UART6_RTSN_M0/PWM2_M0/SPI0_MISO_M0/GPIO0_C5_d	GPIO0C_IOMUX_SEL_H[6:4]=0
gpio0_port[22]	UART6_TX_M0/CAN0_TX_M2/GPIO0_C6_d	GPIO0C_IOMUX_SEL_H[10:8]=0
gpio0_port[23]	UART6_RX_M0/CAN0_RX_M2/GPIO0_C7_d	GPIO0C_IOMUX_SEL_H[14:12]=0
gpio0_port[24]	UART0_RX_M0/JTAG_CPU_MCU_TMS_M0/GPIO0_D0_u	GPIO0D_IOMUX_SEL_L[2:0]=0
gpio0_port[25]	UART0_TX_M0/JTAG_CPU_MCU_TCK_M0/GPIO0_D1_u	GPIO0D_IOMUX_SEL_L[6:4]=0
gpio1_port[0]	EMMC_D0/FSPI_D0/GPIO1_A0_u	GPIO1A_IOMUX_SEL_L[2:0]=0
gpio1_port[1]	EMMC_D1/FSPI_D1/GPIO1_A1_u	GPIO1A_IOMUX_SEL_L[6:4]=0
gpio1_port[2]	EMMC_D2/FSPI_D2/GPIO1_A2_u	GPIO1A_IOMUX_SEL_L[10:8]=0
gpio1_port[3]	EMMC_D3/FSPI_D3/GPIO1_A3_u	GPIO1A_IOMUX_SEL_L[14:12]=0
gpio1_port[4]	EMMC_D4/GPIO1_A4_u	GPIO1A_IOMUX_SEL_H[2:0]=0
gpio1_port[5]	EMMC_D5/GPIO1_A5_u	GPIO1A_IOMUX_SEL_H[6:4]=0
gpio1_port[6]	EMMC_D6/GPIO1_A6_u	GPIO1A_IOMUX_SEL_H[10:8]=0
gpio1_port[7]	EMMC_D7/GPIO1_A7_u	GPIO1A_IOMUX_SEL_H[14:12]=0
gpio1_port[8]	EMMC_CMD/FSPI_CSN0/GPIO1_B0_u	GPIO1B_IOMUX_SEL_L[2:0]=0
gpio1_port[9]	EMMC_CLK/FSPI_CLK/GPIO1_B1_d	GPIO1B_IOMUX_SEL_L[6:4]=0
gpio1_port[10]	EMMC_STRB/FSPI_CSN1/GPIO1_B2_d	GPIO1B_IOMUX_SEL_L[10:8]=0
gpio1_port[11]	SDMMC0_D0/UART0_RX_M1/UART7_RX_M1/SPI1_MOSI_M1/DSM_AUD_LP/GPIO1_B3_u	GPIO1B_IOMUX_SEL_L[14:12]=0
gpio1_port[12]	SDMMC0_D1/UART0_TX_M1/UART7_TX_M1/SPI1_MISO_M1/DSM_AUD_LN/GPIO1_B4_u	GPIO1B_IOMUX_SEL_H[2:0]=0
gpio1_port[13]	SDMMC0_D2/JTAG_CPU_MCU_TCK_M1/UART5_CTSN_M0/SPI1_CSN1_M1/PWM10_M0/DSM_AUD_RP/GPIO1_B5_u	GPIO1B_IOMUX_SEL_H[6:4]=0
gpio1_port[14]	SDMMC0_D3/JTAG_CPU_MCU_TMS_M1/UART5_RTSN_M0/SPI1_CSN0_M1/PWM11_M0/DSM_AUD_RN/GPIO1_B6_u	GPIO1B_IOMUX_SEL_H[10:8]=0
gpio1_port[15]	SDMMC0_CMD/SPDIF_TX_M2/UART5_RX_M0/CAN1_RX_M0/GPIO1_B7_u	GPIO1B_IOMUX_SEL_H[14:12]=0
gpio1_port[16]	SDMMC0_CLK/TEST_CLK_OUT/UART5_TX_M0/SPI1_CLK_M1/CAN1_TX_M0/GPIO1_C0_d	GPIO1C_IOMUX_SEL_L[2:0]=0
gpio1_port[17]	SDMMC1_D0/RGMII_TXD2_M1/I2S0_SDI0_M1/PWM8_M1/GPIO1_C1_d	GPIO1C_IOMUX_SEL_L[6:4]=0
gpio1_port[18]	SDMMC1_D1/RGMII_TXD3_M1/I2S0_SDI1_M1/PWM9_M1/GPIO1_C2_d	GPIO1C_IOMUX_SEL_L[10:8]=0
gpio1_port[19]	SDMMC1_D2/RGMII_TXCLK_M1/I2S0_SDO0_M1/PWM10_M1/GPIO1_C3_d	GPIO1C_IOMUX_SEL_L[14:12]=0
gpio1_port[20]	SDMMC1_D3/RGMII_RXD2_M1/I2S0_LRCK_M1/PWM11_M1/GPIO1_C4_d	GPIO1C_IOMUX_SEL_H[2:0]=0
gpio1_port[21]	SDMMC1_CMD/RGMII_RXD3_M1/I2S0_SCLK_M1/PWM0_M1/GPIO1_C5_d	GPIO1C_IOMUX_SEL_H[6:4]=0

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Module Pin	Pad Name	IOMUX Setting
gpio1_port[22]	SDMMC1_CLK/RGMII_RXCLK_M1/I2S0_MCLK_M1/PWM1_M1/GPIO1_C6_d	GPIO1C_IOMUX_SEL_H[10:8]=0
gpio1_port[23]	SDMMC1_PWREN/RGMII_MDC_M1/PWM2_M1/I2C5_SCL_M1/RMII_MDC/GPIO1_C7_d	GPIO1C_IOMUX_SEL_H[14:12]=0
gpio1_port[24]	SDMMC1_DETN/RGMII_MDIO_M1/PWM3_M1/I2C5_SDA_M1/RMII_MDIO/GPIO1_D0_d	GPIO1D_IOMUX_SEL_L[2:0]=0
gpio1_port[25]	UART1_RX_M0/RGMII_TXD0_M1/I2S0_SDO1_M1/PWM4_M1/RMII_TXD0/GPIO1_D1_d	GPIO1D_IOMUX_SEL_L[6:4]=0
gpio1_port[26]	UART1_TX_M0/RGMII_TXD1_M1/I2S0_SDO2_M1/PWM5_M1/RMII_TXD1/GPIO1_D2_d	GPIO1D_IOMUX_SEL_L[10:8]=0
gpio1_port[27]	UART1_RTSN_M0/RGMII_TXEN_M1/I2S0_SDI2_M1/PWM6_M1/RMII_TXEN/GPIO1_D3_d	GPIO1D_IOMUX_SEL_L[14:12]=0
gpio1_port[28]	UART1_CTSN_M0/RGMII_RXD0_M1/I2S0_SDI3_M1/PWM7_M1/RMII_RXD0/GPIO1_D4_d	GPIO1D_IOMUX_SEL_H[2:0]=0
gpio1_port[29]	I2S2_SCLK_M0/RGMII_CLK_M1/UART4_RX_M1/SPI2_CSN1_M1/RMII_CLK/GPIO1_D5_d	GPIO1D_IOMUX_SEL_H[6:4]=0
gpio1_port[30]	I2S2_LRCK_M0/RGMII_RXDV_M1/UART4_TX_M1/SPI2_CSN0_M1/RMII_RXDV_CRS/GPIO1_D6_d	GPIO1D_IOMUX_SEL_H[10:8]=0
gpio1_port[31]	I2S2_SDO_M0/RGMII_RXD1_M1/UART4_RTSN_M1/SPI2_MOSI_M1/PWM14_M1/RMII_RXD1/GPIO1_D7_d	GPIO1D_IOMUX_SEL_H[14:12]=0
gpio2_port[0]	I2S2_SDI_M0/RGMII_RXER_M1/UART4_CTSN_M1/SPI2_MISO_M1/PWM15_M1/RMII_RXER/GPIO2_A0_d	GPIO2A_IOMUX_SEL_L[2:0]=0
gpio2_port[1]	I2S2_MCLK_M0/ETH_CLK_25M_OUT_M1/CLK1_32K_OUT/SPI2_CLK_M1/I2S0_SDO3_M1/GPIO2_A1_d	GPIO2A_IOMUX_SEL_L[6:4]=0
gpio3_port[0]	I2C3_SCL_M0/UART2_TX_M1/PDM_SDI3_M0/CAN0_TX_M0/UART5_CTSN_M1/GPIO3_A0_d	GPIO3A_IOMUX_SEL_L[2:0]=0
gpio3_port[1]	I2C3_SDA_M0/UART2_RX_M1/SPDIF_TX_M0/CAN0_RX_M0/UART5_RTSN_M1/GPIO3_A1_d	GPIO3A_IOMUX_SEL_L[6:4]=0
gpio3_port[2]	I2S0_MCLK_M0/UART2_CTSN_M1/PDM_CLK1_M0/GPIO3_A2_d	GPIO3A_IOMUX_SEL_L[10:8]=0
gpio3_port[3]	I2S0_SCLK_M0/UART2_RTSN_M1/GPIO3_A3_d	GPIO3A_IOMUX_SEL_L[14:12]=0
gpio3_port[4]	I2S0_LRCK_M0/PWM8_M0/GPIO3_A4_d	GPIO3A_IOMUX_SEL_H[2:0]=0
gpio3_port[5]	I2S0_SDO0_M0/PWM9_M0/GPIO3_A5_d	GPIO3A_IOMUX_SEL_H[6:4]=0
gpio3_port[6]	I2S0_SDO1_M0/I2S0_SDI3_M0/PDM_CLK0_M0/PCIE20_CLKREQN_M1/UART5_TX_M1/GPIO3_A6_d	GPIO3A_IOMUX_SEL_H[10:8]=0
gpio3_port[7]	I2S0_SDO2_M0/I2S0_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEN_M1/UART5_RX_M1/GPIO3_A7_d	GPIO3A_IOMUX_SEL_H[14:12]=0
gpio3_port[8]	I2S0_SDO3_M0/I2S0_SDI1_M0/PDM_SDI1_M0/PCIE20_PERSTN_M1/GPIO3_B0_d	GPIO3B_IOMUX_SEL_L[2:0]=0
gpio3_port[9]	I2S0_SDI0_M0/PDM_SDI0_M0/GPIO3_B1_d	GPIO3B_IOMUX_SEL_L[6:4]=0
gpio3_port[10]	I2S1_MCLK_M1/CAM_CLK0_OUT_M0/UART8_TX_M0/GPIO3_B2_d	GPIO3B_IOMUX_SEL_L[10:8]=0
gpio3_port[11]	I2S1_SCLK_M1/CAM_CLK1_OUT_M0/UART8_RX_M0/GPIO3_B3_d	GPIO3B_IOMUX_SEL_L[14:12]=0
gpio3_port[12]	I2S1_LRCK_M1/CAM_CLK2_OUT/UART8_CTSN_M0/SPI0_MOSI_M1/PWM12_M1/GPIO3_B4_d	GPIO3B_IOMUX_SEL_H[2:0]=0
gpio3_port[13]	I2S1_SDO0_M1/CAM_CLK3_OUT/UART8_RTSN_M0/SPI0_CLK_M1/PWM13_M1/GPIO3_B5_d	GPIO3B_IOMUX_SEL_H[6:4]=0
gpio3_port[14]	I2S1_SDO1_M1/I2S1_SDI3_M1/UART3_CTSN_M1/SPI0_CSN1_M1/I2C4_SCL_M0/CAN0_TX_M1/GPIO3_B6_d	GPIO3B_IOMUX_SEL_H[10:8]=0
gpio3_port[15]	I2S1_SDO2_M1/I2S1_SDI2_M1/UART3_TX_M1/SPI0_CSN0_M1/I2C4_SDA_M0/CAN0_RX_M1/GPIO3_B7_d	GPIO3B_IOMUX_SEL_H[14:12]=0
gpio3_port[16]	I2S1_SDO3_M1/I2S1_SDI1_M1/UART3_RX_M1/SPI0_MISO_M1/GPIO3_C0_d	GPIO3C_IOMUX_SEL_L[2:0]=0
gpio3_port[17]	I2S1_SDI0_M1/ISP_FLASH_TRIGIN/UART3_RTSN_M1/GPIO3_C1_d	GPIO3C_IOMUX_SEL_L[6:4]=0
gpio3_port[18]	I2C5_SCL_M0/ISP_PRELIGHT_TRIGOUT/UART9_TX_M1/GPIO3_C2_d	GPIO3C_IOMUX_SEL_L[10:8]=0
gpio3_port[19]	I2C5_SDA_M0/ISP_FLASH_TRIGOUT/UART9_RX_M1/GPIO3_C3_d	GPIO3C_IOMUX_SEL_L[14:12]=0

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Module Pin	Pad Name	IOMUX Setting
gpio3_port[20]	VO_LCDC_D3/I2S1_MCLK_M0/UART7_TX_M0/GPIO3_C4_d	GPIO3C_IOMUX_SEL_H[2:0]=0
gpio3_port[21]	VO_LCDC_D4/I2S1_SCLK_M0/UART4_CTSN_M0/PWM14_M0/GPIO3_C5_d	GPIO3C_IOMUX_SEL_H[6:4]=0
gpio3_port[22]	VO_LCDC_D5/I2S1_LRCK_M0/UART4_RTSN_M0/PWM15_M0/GPIO3_C6_d	GPIO3C_IOMUX_SEL_H[10:8]=0
gpio3_port[23]	VO_LCDC_D6/I2S1_SDO0_M0/UART7_RX_M0/GPIO3_C7_d	GPIO3C_IOMUX_SEL_H[14:12]=0
gpio3_port[24]	VO_LCDC_D7/I2S1_SDI0_M0/UART4_TX_M0/GPIO3_D0_d	GPIO3D_IOMUX_SEL_L[2:0]=0
gpio3_port[25]	VO_LCDC_D10/I2S1_SDI1_M0/UART4_RX_M0/UART3_RTSN_M0/GPIO3_D1_d	GPIO3D_IOMUX_SEL_L[6:4]=0
gpio3_port[26]	VO_LCDC_D11/I2S1_SDI2_M0/UART7_CTSN_M0/SPI2_MISO_M0/I2C2_SCL_M1/GPIO3_D2_d	GPIO3D_IOMUX_SEL_L[10:8]=0
gpio3_port[27]	VO_LCDC_D12/I2S1_SDI3_M0/UART7_RTSN_M0/SPI2_MOSI_M0/I2C2_SDA_M1/GPIO3_D3_d	GPIO3D_IOMUX_SEL_L[14:12]=0
gpio3_port[28]	VO_LCDC_D13/RGMII_TXD2_M0/UART8_TX_M1/I2S2_SDI_M1/GPIO3_D4_d	GPIO3D_IOMUX_SEL_H[2:0]=0
gpio3_port[29]	VO_LCDC_D14/RGMII_TXD3_M0/UART8_RX_M1/I2S2_SDO_M1/GPIO3_D5_d	GPIO3D_IOMUX_SEL_H[6:4]=0
gpio3_port[30]	VO_LCDC_D15/RGMII_TXCLK_M0/I2S2_MCLK_M1/SPI1_CLK_M0/GPIO3_D6_d	GPIO3D_IOMUX_SEL_H[10:8]=0
gpio3_port[31]	VO_LCDC_D19/RGMII_RXD2_M0/UART8_CTSN_M1/SPI1_CSN0_M0/GPIO3_D7_d	GPIO3D_IOMUX_SEL_H[14:12]=0
gpio3_port[0]	VO_LCDC_D20/RGMII_RXD3_M0/UART8_RTSN_M1/SPI1_CSN1_M0/GPIO4_A0_d	GPIO4A_IOMUX_SEL_L[2:0]=0
gpio3_port[1]	VO_LCDC_D21/RGMII_RXCLK_M0/I2S2_LRCK_M1/PWM12_M0/GPIO4_A1_d	GPIO4A_IOMUX_SEL_L[6:4]=0
gpio3_port[2]	VO_LCDC_D22/RGMII_TXD0_M0/UART6_CTSN_M1/SPI1_MOSI_M0/GPIO4_A2_d	GPIO4A_IOMUX_SEL_L[10:8]=0
gpio3_port[3]	VO_LCDC_D23/RGMII_TXD1_M0/UART6_RTSN_M1/SPI1_MISO_M0/GPIO4_A3_d	GPIO4A_IOMUX_SEL_L[14:12]=0
gpio3_port[4]	VO_LCDC_D0/RGMII_TXEN_M0/PWM13_M0/GPIO4_A4_d	GPIO4A_IOMUX_SEL_H[2:0]=0
gpio3_port[5]	VO_LCDC_D1/RGMII_RXD0_M0/UART1_TX_M1/PDM_SDI2_M1/I2C3_SCL_M1/GPIO4_A5_d	GPIO4A_IOMUX_SEL_H[6:4]=0
gpio3_port[6]	VO_LCDC_D8/RGMII_RXD1_M0/UART1_RX_M1/PDM_SDI3_M1/I2C3_SDA_M1/GPIO4_A6_d	GPIO4A_IOMUX_SEL_H[10:8]=0
gpio3_port[7]	VO_LCDC_D9/RGMII_RXDV_M0/UART1_RTSN_M1/PDM_SDI0_M1/UART6_TX_M1/GPIO4_A7_d	GPIO4A_IOMUX_SEL_H[14:12]=0
gpio3_port[8]	VO_LCDC_D16/RGMII_RXER_M0/UART1_CTSN_M1/PDM_SDI1_M1/UART6_RX_M1/GPIO4_B0_d	GPIO4B_IOMUX_SEL_L[2:0]=0
gpio3_port[9]	VO_LCDC_D17/ETH_CLK_25M_OUT_M0/CAM_CLK0_OUT_M1/I2S2_SCLK_M1/PDM_CLK1_M1/GPIO4_B1_d	GPIO4B_IOMUX_SEL_L[6:4]=0
gpio3_port[10]	VO_LCDC_D2/RGMII_MDC_M0/UART9_TX_M0/GPIO4_B2_d	GPIO4B_IOMUX_SEL_L[10:8]=0
gpio3_port[11]	VO_LCDC_D18/RGMII_MDIO_M0/UART9_RX_M0/GPIO4_B3_d	GPIO4B_IOMUX_SEL_L[14:12]=0

Notes: Unused Module Pin is tied to zero!

19.6 Application Notes

- Reading from an unused location or unused bits in a particular register always returns zeros. There is no error mechanism in the APB.
- Programming the GPIO registers for interrupt detection should be completed prior to enabling the interrupts to prevent spurious glitches on the interrupt output signal to the interrupt controller.

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Chapter 20 TIMER

20.1 Overview

TIMER is a programmable timer peripheral. This component is an APB slave device. There are three types of TIMER according to the count type, which are normal decrement count TIMER, normal increment count TIMER and special function increment count TIMER. The normal decrement count TIMER is called NDCTIMER. The normal increment count TIMER is called NICTIMER. The special function increment count TIMER is called HPTIMER (High Precision TIMER).

- 6-channel TIMER consists of 5 normal decrement count TIMERs and 1 normal increment count TIMER. In 6-channel TIMER, TIMER5 is the normal increment count TIMER, and the other channel TIMER is the normal decrement count TIMER.
- 2-channel TIMER consists of 2 normal increment count TIMERs.
- HPTIMER has calibration function and provides count value for CPU.

Timer supports the following features:

- Common feature
  - Support 32-bit APB slave in all three kinds of counter
  - Support configuration of loading count value in all three kinds of counter
  - Support two counting mode: free-running and user-defined mode in all three kinds of counter
  - Support mask interrupt in all three kinds of counter
- HPTIMER
  - Support three timer mode: Normal, Hardware adjust, Software adjust
  - Support calibrate back to exact count value without software calculation in Hardware adjust mode
  - Support calibrate back to exact count value with software-aided calculation in Software adjust mode
  - Support common multiple configuration of slow and fast clock period

20.2 Block Diagram

20.2.1 Normal Count TIMER

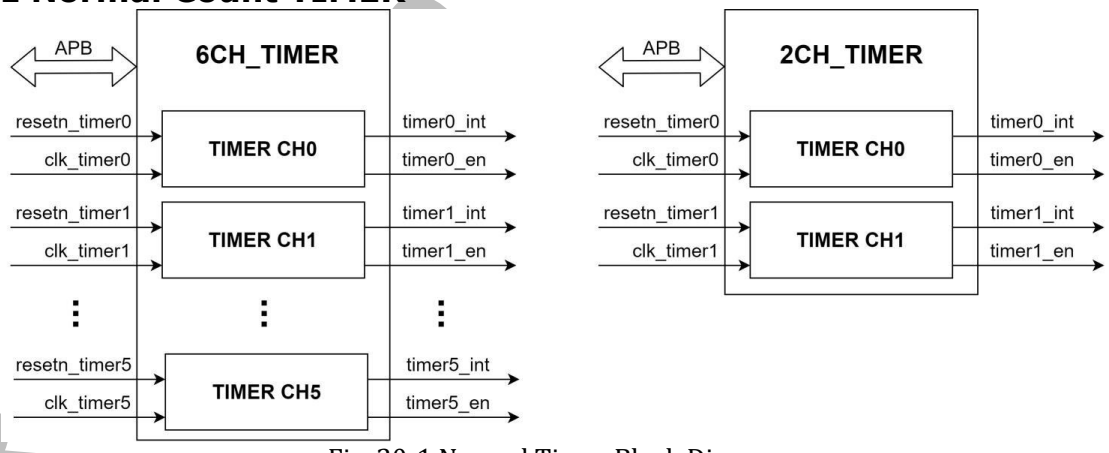

Fig. 20-1 Normal Timer Block Diagram

This figure show 6-channel TIMER and 2-channel TIMER. At 6CH_TIMER, the TIMER ch0~ch4 are the normal decrement count TIMER and ch5 is the normal increment count TIMER. At 2CH_TIMER, ch0 and ch1 are common normal increment count TIMER. APB is the read and write interface of timer register. reset_timern and clk_timern are reset and count clock for each channel timer. Timern_int and timern_en are interrupt and clock enable for each channel timer respectively. (timern is the signal corresponding to TIMER CHn)

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20.2.2 HPTIMER

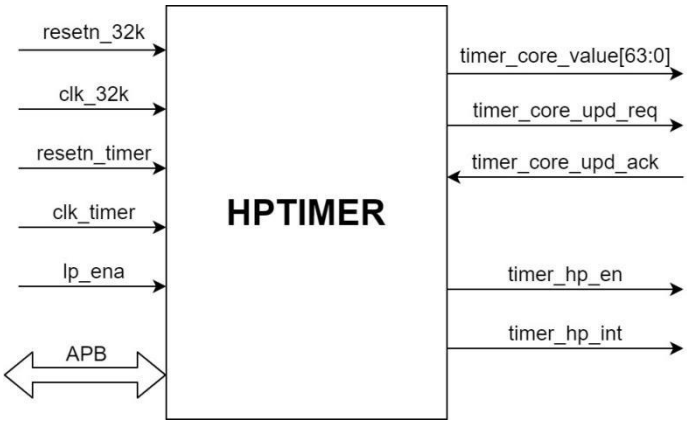

Fig. 20-2 HPTIMER Block Diagram

This figure shows the block diagram of HPTIMER.
HPTIMER has a set of APB interfaces for reading and writing registers.
lp_ena is the low power enable signal sent by PMU to HPTIMER, and it is also the indication signal of clk_timer frequency switching.
timer_core_value[63:0], timer_core_upd_req, timer_core_upd_ack is the interaction signal with core. timer_core_value[63:0] is the count update value, timer_core_upd_req is the update count request signal, timer_core_upd_ack is the update count response signal.
timer_hp_en is the enabling signal of clk_32k and clk_timer clocks. timer_hp_int is the interrupt output of HPTIMER.

20.3 Function Description

20.3.1 TIMER Clock

The clock frequency of the counting clock source of NICTIMER and NDCTIMER is 24MHz.
The clock source clock of clk_32k of HPTIMER is 32KHz, and the clock frequency of clk_timer clock source is switched between 24MHz and 32KHz.

20.3.2 Programming Flow

20.3.2.1 NDCTIMER and NICTIMER

1. Initialize the TIMER by the TIMER_TIMERn_CONTROLREG (0≤n≤5) register:
   (1) Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
   (2) Program the timer mode—free-running or user-defined—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
   (3) Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).
2. Load the timer count value into the TIMER_TIMERn_LOAD_COUNT1 (0≤n≤5) and TIMER_TIMERn_LOAD_COUNT0 (0≤n≤5) register.
3. Enable the TIMER by writing a "1" to bit 0 of TIMER_TIMERn_CONTROLREG (0≤n≤5).

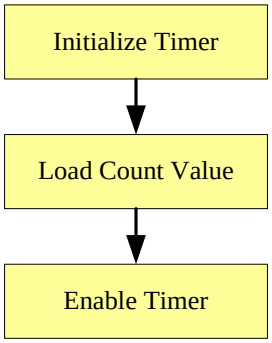

Fig. 20-3 Timer Usage Flow

20.3.2.2 HPTIMER

- **Normal mode**

1. Initialize the HPTIMER by the TIMER_HP_CTRL register:

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(1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
(2) Program the timer mode, normal mode by writing a 0x0 to the timer mode bits (bit 1 to bit 2).
(3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).

2. Load the HPTIMER count value into the TIMER_HP_LOAD_COUNT1 and TIMER_HP_LOAD_ COUNT0 register.
3. Enable the HPTIMER by writing a '1' to bit 0 of TIMER_HP_CTRL.

If you want to do another count, repeat steps 1 to 3.

- **Hardware adjust mode**

1. Initialize the HPTIMER by the TIMER_HP_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x1 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Initialize the HPTIMER by the TIMER_HP_INTR_STATUS register. Write 0x7 to TIMER_HP_ INTR_STATUS register to clear TIMER_HP_INTR_STATUS register.
3. Load the HPTIMER count value into the TIMER_HP_LOAD_COUNT1 and TIMER_HP_LOAD_ COUNT0 register.
4. Configure the HPTIMER GCD register.
   (1) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_timer clock cycle and configure it in TIMER_HP_T24_GCD register.
   (2) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_32k clock cycle and configure it in TIMER_HP_T32_GCD register.
5. Enable the HPTIMER by writing a '1' to bit 0 of TIMER_HP_CTRL.
6. Read out the INTR_STATUS register until the ini_adj_done bit segment (bit 1) is '1', which means that the HPTIMER 32K count is initially adjusted. The low power mode can only be entered after the initial adjustment is completed.
7. The chip enters and exits the low power consumption mode at any time in between.
8. Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the HPTIMER count is adjusted.
9. Write 0x7 to TIMER_HP_ INTR_STATUS register to clear TIMER_HP_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 7 to 9.

- **Software adjust mode**

1. Initialize the HPTIMER by the TIMER_HP_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x2 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Initialize the HPTIMER by the TIMER_HP_INTR_STATUS and BEGIN_END_VALID register. Write 0x7 to TIMER_HP_ INTR_STATUS register to clear TIMER_HP_INTR_STATUS register. write 0x3 to BEGIN_END_VALID register to clear BEGIN_END_VALID register.
3. Load the HPTIMER count value into the TIMER_HP_LOAD_COUNT1 and TIMER_HP_LOAD_ COUNT0 register.
4. Enable the HPTIMER by writing a '1' to bit 0 of TIMER_HP_CTRL.
5. The chip enters and exits the low power consumption mode at any time in between.
6. Read out BEGIN_END_VALID register until the value of it is 0x3, which indicates that the chip has entered and exited the low power consumption mode, then you can adjust the timer count value. Then write 0x3 to BEGIN_END_VALID register to clear the register.

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7. The count value of HPTIMER compensation.
   (1) Read out TIMER_HP_T24_32BEGIN1, TIMER_ HP_T24_32BEGIN0, TIMER_HP_T32_24END1 and TIMER_HP_T32_24END0 register.
   (2) configure TIMER_HP_T24_DELAT_COUNT1 and TIMER_HP_T24_DELAT_COUNT0 registers to compensate for the count values according to the values of these registers read out above.
   (3) Write 0x1 to TIMER_HP_SYNC_REQ register to start compensation counting.
   (4) Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the compensation count is completed.
8. Write 0x7 to TIMER_HP_ INTR_STATUS register to clear TIMER_HP_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 5 to 8.

20.3.3 Loading a Timer Count Value

For the descending TIMER (that is, the value from which it counts down). The initial value for each TIMER is loaded into the TIMER using the load count register (TIMER_TIMERn_LOAD_ COUNT1 and TIMER_TIMERn_ LOAD_COUNT0). Two events can cause a TIMER to load the initial value from its load count register:

- TIMER is enabled after reset or disabled.
- TIMER counts down to 0, when TIMER is configured into free-running mode.

For the incremental TIMER(that is, the value from which it counts up). The initial value for each timer is zero. The count register will count up to the value loaded in the register TIMER_ TIMERn_LOAD_COUNT1 and TIMER_TIMERn_ LOAD_COUNT0. Two events can cause a TIMER to load zero:

- TIMER is enabled after reset or disabled.
- TIMER counts up to the value stored in TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_COUNT0, when timer is configured into free-running mode.

20.3.4 Timer Mode Selection

- **User-defined Count Mode**

TIMER loads TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_ COUNT0 registers (for descending TIMER) or zero (for incremental TIMER) as initial value. When the TIMER counts down to 0 (for descending TIMER) or counts up to the value in TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_ LOAD_ COUNT0 (for incremental TIMER), it will not automatically reload the count value register. User need to disable timer firstly and follow the programming sequence to make timer work again.

- **Free-running Count Mode**

TIMER loads the TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_COUNT0 (for descending TIMER) or zero (for incremental TIMER) register as initial value. TIMER will automatically reload the count value register, when timer counts down to 0 (for descending TIMER) or counts up to the value in TIMER_TIMERn_LOAD_ COUNT1 and TIMER_TIMERn_LOAD_COUNT0 (for incremental TIMER).

20.4 TIMER_6CH Register Description

20.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
TIMER0	0xFFA50000
TIMER1	0xFFA50020
TIMER2	0xFFA50040
TIMER3	0xFFA50060
TIMER4	0xFFA50080
TIMER5	0xFFA500A0

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20.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TIMER_6CH_TIMERn_LOAD_COUNT0	0x0000	W	0x00000000	Low 32 bits value to be loaded into Timer0
TIMER_6CH_TIMERn_LOAD_COUNT1	0x0004	W	0x00000000	High 32 bits value to be loaded into Timer0.
TIMER_6CH_TIMERn_CURR_VALUE0	0x0008	W	0x00000000	Low 32 bits of current value of Timer0.
TIMER_6CH_TIMERn_CURR_VALUE1	0x000C	W	0x00000000	High 32 bits of current value of Timer0.
TIMER_6CH_TIMERn_CONTROL	0x0010	W	0x00000000	Timer Control Register
TIMER_6CH_TIMERn_INTSTATUS	0x0018	W	0x00000000	Timer Interrupt Status Register
TIMER_6CH_REVISION	0x00F0	W	0x11972006	Timer Version Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

20.4.3 Detail Register Description

TIMER_6CH_TIMERn_LOAD_COUNT0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count0 Load count low bits

TIMER_6CH_TIMERn_LOAD_COUNT1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count1 Load count high bits

TIMER_6CH_TIMERn_CURR_VALUE0

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	current_value0 Current_cnt_low bits

TIMER_6CH_TIMERn_CURR_VALUE1

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	current_value1 Current_cnt_high bits

TIMER_6CH_TIMERn_CONTROL

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	int_en Timer interrupt enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	timer_mode Timer mode 1'b0: Free-running mode 1'b1: User-defined count mode

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Bit	Attr	Reset Value	Description
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

TIMER_6CH_TIMERn_INTSTATUS

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	int_pd This register contains the interrupt status for Timer. Write 1 to this register will clear the interrupt.

TIMER_6CH_REVISION

Address: **Operational Base** + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x1197	svn_revision SVN revision: 16'd4503.
15:14	RO	0x0	reserved
13	RW	0x1	ch5_type Channel 5 is a count up counter.
12	RW	0x0	ch4_type Channel 4 is a count down counter.
11	RW	0x0	ch3_type Channel 3 is a count down counter.
10	RW	0x0	ch2_type Channel 2 is a count down counter.
9	RW	0x0	ch1_type Channel 1 is a count down counter.
8	RW	0x0	ch0_type Channel 0 is a count down counter.
7:0	RW	0x06	ip_function IP function: 16'd6.

20.5 STIMER_2CH Register Description

20.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
STIMER0	0xFFA90000
STIMER1	0xFFA90020

20.5.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TIMER_2CH_TIMERn_LOAD_COUNT0	0x0000	W	0x00000000	Low 32 bits value to be loaded into Timer0
TIMER_2CH_TIMERn_LOAD_COUNT1	0x0004	W	0x00000000	High 32 bits value to be loaded into Timer0.
TIMER_2CH_TIMERn_CURR_VALUE0	0x0008	W	0x00000000	Low 32 bits of current value of Timer0.

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Name	Offset	Size	Reset Value	Description
TIMER_2CH_TIMERn_CURR_VALUE1	0x000C	W	0x00000000	High 32 bits of current value of Timer0.
TIMER_2CH_TIMERn_CONTROL	0x0010	W	0x00000000	Timer Control Register
TIMER_2CH_TIMERn_INTSTATUS	0x0018	W	0x00000000	Timer Interrupt Status Register
TIMER_2CH_REVISION	0x00F0	W	0x15650302	Timer Version Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

20.5.3 Detail Register Description

TIMER_2CH_TIMERn_LOAD_COUNT0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count0 Load count low bits

TIMER_2CH_TIMERn_LOAD_COUNT1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count1 Load count high bits

TIMER_2CH_TIMERn_CURR_VALUE0

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value0 Current_cnt_low bits

TIMER_2CH_TIMERn_CURR_VALUE1

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value1 Current_cnt_high bits

TIMER_2CH_TIMERn_CONTROL

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	int_en Timer interrupt mask 1'b0: Mask 1'b1: Not mask
1	RW	0x0	timer_mode Timer mode 1'b0: Free-running mode 1'b1: User-defined count mode
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

TIMER_2CH_TIMERn_INTSTATUS

Address: **Operational Base** + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	int_pd This register contains the interrupt status for Timer. Write 1 to this register will clear the interrupt.

TIMER_2CH_REVISION

Address: **Operational Base** + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	RO	0x1565	svn_revision SVN revision: 16'd5477.
15:10	RO	0x00	reserved
9	RW	0x1	ch1_type Channel 1 is a count up counter.
8	RW	0x1	ch0_type Channel 0 is a count up counter.
7:0	RO	0x02	ip_function IP function: 16'd2.

20.6 HPTIMER Register Description

20.6.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

20.6.2 Registers Summary

Name	Offset	Size	Reset Value	Description
HPTIMER_REVISION	0x0000	W	0x19E10201	HPTIMER Version Register
HPTIMER_CTRL	0x0004	W	0x00000000	HPTIMER Control Register
HPTIMER_INTR_EN	0x0008	W	0x00000000	Interrupt Mask Register
HPTIMER_T24_GCD	0x000C	W	0x00000000	Common Multiple div 24M
HPTIMER_T32_GCD	0x0010	W	0x00000000	Common Multiple div 32K
HPTIMER_LOAD_COUNT0	0x0014	W	0x00000000	Low 32bits of load count value
HPTIMER_LOAD_COUNT1	0x0018	W	0x00000000	High 32bits of load count value
HPTIMER_T24_DELAT_COUNT0	0x001C	W	0x00000000	Low 32bits of 24M clock delay time count value
HPTIMER_T24_DELAT_COUNT1	0x0020	W	0x00000000	High 32bits of 24M clock delay time count value
HPTIMER_CURR_32K_VALUE0	0x0024	W	0x00000000	Low 32bits of current cnt_32k value
HPTIMER_CURR_32K_VALUE1	0x0028	W	0x00000000	High 32bits of current cnt_32k value
HPTIMER_CURR_TIMER_VALUE0	0x002C	W	0x00000000	Low 32bits of current timer_cnt value
HPTIMER_CURR_TIMER_VALUE1	0x0030	W	0x00000000	High 32bits of current timer_cnt value
HPTIMER_T24_32BEGIN0	0x0034	W	0x00000000	Low 32 bits of low power begin
HPTIMER_T24_32BEGIN1	0x0038	W	0x00000000	High 32 bits of low power begin
HPTIMER_T32_24END0	0x003C	W	0x00000000	Low 32 bits of low power end
HPTIMER_T32_24END1	0x0040	W	0x00000000	High 32 bits of low power end
HPTIMER_BEGIN_END_VALID	0x0044	W	0x00000000	Low power count value valid
HPTIMER_SYNC_REQ	0x0048	W	0x00000000	Synchronize request
HPTIMER_INTR_STATUS	0x004C	W	0x00000000	Interrupt Status Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

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Double WORD (64 bits) access

20.6.3 Detail Register Description

HPTIMER_REVISION

Address: Operational Base(0xFF270000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x19e1	svn_revision Svn revision 16'd6625
15:10	RO	0x00	reserved
9:8	RW	0x2	ch_type Channel 0 is a low power recovery self-correction count up counter.
7:0	RO	0x01	ip_function IP function. 16'd1

HPTIMER_CTRL

Address: Operational Base(0xFF270000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	count_mode Timer count mode 1'b0: Free-running mode 1'b1: User-defined count mode
2:1	RW	0x0	timer_mode Select timer as which timer 2'b00: Normal timer 2'b01: Adjust timer with hardware adjust 2'b10: Adjust timer with software adjust
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

HPTIMER_INTR_EN

Address: Operational Base(0xFF270000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	sync_done_intr_en Synchronization done interrupt enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	ini_adj_done_intr_en Initial adjust done interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	count_reach_intr_en Timer count reach load_count interrupt enable 1'b0: Disable 1'b1: Enable

HPTIMER_T24_GCD

Address: Operational Base(0xFF270000) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_gcd The least common multiple of 24M and 32K clock cycles divided by 24M clock cycles.

HPTIMER_T32_GCD

Address: Operational Base(0xFF270000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t32_gcd The least common multiple of 24M and 32K clock cycles divided by 32K clock cycles.

HPTIMER_LOAD_COUNT0

Address: Operational Base(0xFF270000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count0 Low 32bits of load count value.

HPTIMER_LOAD_COUNT1

Address: Operational Base(0xFF270000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count1 High 32bits of load count value.

HPTIMER_T24_DELAT_COUNT0

Address: Operational Base(0xFF270000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_delay_time_count0 Low 32bits of 24M clock delay time count value.

HPTIMER_T24_DELAT_COUNT1

Address: Operational Base(0xFF270000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_delay_time_count1 High 32bits of 24M clock delay time count value.

HPTIMER_CURR_32K_VALUE0

Address: Operational Base(0xFF270000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_32k_value0 Low 32bits of current cnt_32k value.

HPTIMER_CURR_32K_VALUE1

Address: Operational Base(0xFF270000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_32k_value1 High 32bits of current cnt_32k value.

HPTIMER_CURR_TIMER_VALUE0

Address: Operational Base(0xFF270000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value0 Low 32bits of current timer_cnt value.

HPTIMER_CURR_TIMER_VALUE1

Address: Operational Base(0xFF270000) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value1 High 32bits of current timer_cnt value.

HPTIMER_T24_32BEGIN0

Address: Operational Base(0xFF270000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t24_32begin0 24M switches to 32K clock, with a low 32 bits of timer_cnt value.

HPTIMER_T24_32BEGIN1

Address: Operational Base(0xFF270000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t24_32begin1 24M switches to 32K clock, with a high 32 bits of timer_cnt value.

HPTIMER_T32_24END0

Address: Operational Base(0xFF270000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t32_24end0 32K switches to 24M clock, with a low 32 bits of timer_cnt value.

HPTIMER_T32_24END1

Address: Operational Base(0xFF270000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t32_24end1 32K switches to 24M clock, with a high 32 bits of timer_cnt value.

HPTIMER_BEGIN_END_VALID

Address: Operational Base(0xFF270000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	W1C	0x0	t32_24end_valid T32_24END value valid 1'b0: Invalid 1'b1: Valid
0	W1C	0x0	t24_32begin_valid T24_32BEGIN value valid 1'b0: Invalid 1'b1: Valid

HPTIMER_SYNC_REQ

Address: Operational Base(0xFF270000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	R/WSC	0x0	sync_request Timer_cnt synchronize request

HPTIMER_INTR_STATUS

Address: Operational Base(0xFF270000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	sync_done Timer_cnt synchronization done

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Bit	Attr	Reset Value	Description
1	W1C	0x0	ini_adj_done Cnt_32k initial adjust done
0	W1C	0x0	count_reach Normal counter: Timer_cnt reach load_count value

20.7 Application Notes

20.7.1 Clock and Enable

In the chip, the timer_clk is from 24MHz XIN_OSC, asynchronous to the pclk. When user disables the timer enables bit (bit 0 of TIMERn_CONTROLREG (0≤n≤5)), the timer en output signal is de-asserted, and timer_clk will stop. When user enables the timer, the timer_en signal is asserted and timer_clk will start running.

The application is only allowed to re-config registers when timer_en is low.

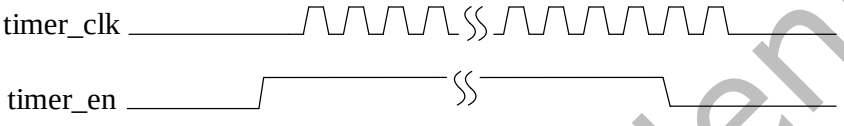

Fig. 20-4 Timing between timer_en and timer_clk

Please refer to function description section for the timer usage flow.

20.7.2 HPTIMER Application Notes

- Initial adjustment, synchronous counting adjustment time is about 2ms.
- The timer_en of the CTRL register will output as a reference signal for timer clock gating. When timer_en is '0', it will gate the 24M and 32K clocks of the input timer. The application is only allowed to re-config registers when timer_en is low.

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Chapter 21 Pulse Width Modulation (PWM)

21.1 Overview

The pulse-width modulator (PWM) feature is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components.
The PWM Module supports the following features:

- 4-built-in PWM channels
- Support capture mode
  - Measures the high/low polarity effective cycles of this input waveform
  - Generates a single interrupt at the transition of input waveform polarity
  - 32-bit high polarity capture register
  - 32-bit low polarity capture register
  - 32-bit current value register
  - The capture result can be stored in a FIFO, and the depth of FIFO is 8. The data of FIFO can be read by CPU or DMA
  - Channel 3 support 32-bits power key capture mode
  - Support switchIO between channel 3 and channel0/1/2
  - Support input pulse counter
  - Support an input filter to remove glitch
- Support continuous mode or one-shot mode
  - 32-bit period counter
  - 32-bit duty register
  - 32-bit current value register
  - PWM output polarity in inactive state and duty cycle polarity can be configured
  - Period and duty cycle are shadow buffered. Change takes effect when the end of the effective period is reached or when the channel is disabled
  - Programmable center or left aligned outputs, and change takes effect when the end of the effective period is reached or when the channel is disabled
  - 8-bit repeat counter for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value, and generates a single interrupt at the end of operation
  - Continuous mode generates the waveform continuously, and does not generates any interrupts
  - Support global lock register to control shadow register effective time
  - Support IR transmission in NEC with full repeat, NEC with simple repeat, TC9012 or SONY mode
- Pre-scaled operation to clk_pwm and then further scaled
- Available low-power mode to reduce power consumption when the channel is inactive.

21.2 Block Diagram

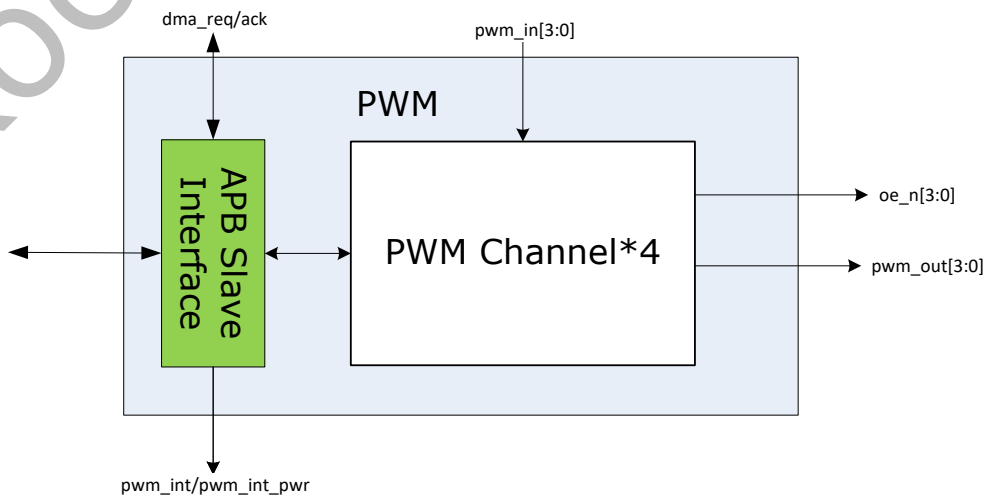

Fig. 21-1PWM Block Diagram

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The host processor gets access to PWM Register Block through the APB slave interface with 32-bit bus width, and asserts the active-high level interrupt. PWM only supports one interrupt output, please refer to interrupt register to know the raw interrupt status when an interrupt is asserted.
PWM Channel is the control logic of PWM module, it controls the operation of PWM module according to the configured working mode.

21.3 Function Description

The PWM supports three operation modes: capture mode, one-shot mode and continuous mode. For the one-shot mode and the continuous mode, the PWM output can be configured as the left-aligned mode or the center-aligned mode.

21.3.1 Capture mode

The capture mode is used to measure the PWM channel input waveform high/low effective cycles with the PWM channel clock, and asserts an interrupt when the polarity of the input waveform changes. The number of the high effective cycles is recorded in the WMx_PERIOD_HPC register, while the number of the low effective cycles is recorded in the PWMx_DUTY_LPC register.
Notes: the PWM input waveform is doubled buffered when the PWM channel isworking in order to filter unexpected shot-time polarity transition, and therefore the interrupt is asserted several cycles after the input waveform polarity changes, and so does the change of the values of PWMx_PERIOD_HPC and PWMx_DUTY_LPC.

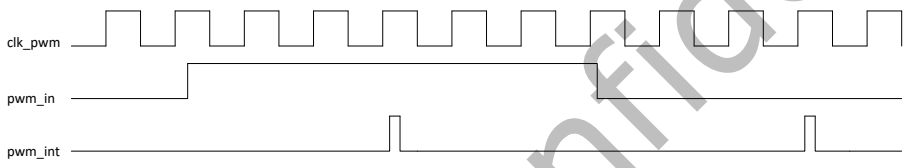

Fig. 21-2PWMCapture Mode

The capture result also can be stored in a FIFO. The FIFO has an almost full indicator. The indicator can be chosed to use as an interrupt or DMA request. When it is used as an interrupt, the data in FIFO can be read by CPU. When it is used as a DMA request, the data in FIFO can be read through DMA. It also supports timeout interrupt when the data in FIFO has not been read in a time threshold.
Only one channel can support 32-bits power key capture mode. The default channel is channel 3. User can also use other channels by switchingIO between channel 3 and channel0/1/2.User can configure 10 power keys to match, the interrupt will be asserted when the capture value matching anyone.
The capture mode is also used to get the pulse counter of input waveform. Tt can use to calculate the frequency by working with system timer.

21.3.2 Continuous mode

The PWM channel generates a series of the pulses continuously as expected once the channel is enabled with continuous mode.
In the continuous mode, the PWM output waveforms can be in one form of the two mode: left-aligned mode or center-aligned mode.
For the left-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWMx_CTRL.duty_pol). Once duty cycle number (PWMx_DUTY_LPC) is reached, the output is switched to the opposite polarity. After the period number (PWMx_PERIOD_HPC) is reached, the output is again switched to the opposite polarity to start another period of desired pulse.

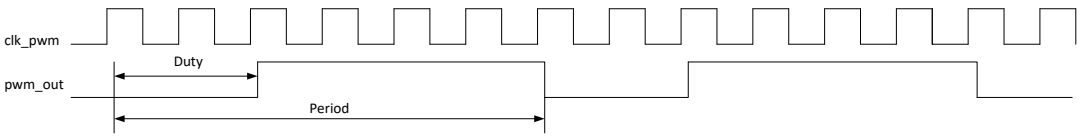

Fig. 21-3PWM Continuous Left-aligned Output Mode

For the center-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWMx_CTRL.duty_pol). Once one half of duty cycle number (PWMx_DUTY_LPC) is reached, the output is switched to the opposite polarity. Then if there is one half of duty cycle left for the whole period, the output is again switched to the

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opposite polarity. Finally after the period number (PWMx_PERIOD_HPC) is reached, the output starts another period of desired pulse.

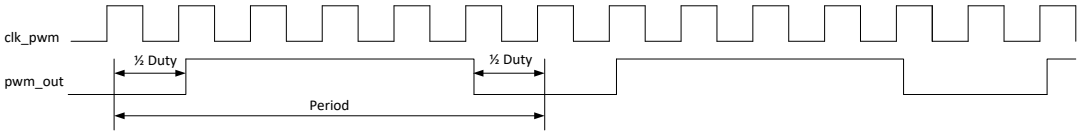

Fig. 21-4PWM Continuous Center-aligned Output Mode

Once disable the PWM channel, the channel stops generating the output waveforms and output polarity is fixed as the configured inactive polarity (PWMx_CTRL.inactive_pol).

21.3.3 One-shot mode

Unlike the continuous mode, the PWM channel generates the output waveforms within the configured periods (PWM_CTRL.rpt + 1), and then stops. At the same times, an interrupt is asserted to inform that the operation has been finished.

There are also two output modes for the one-shot mode: the left-aligned mode and the center-aligned mode.

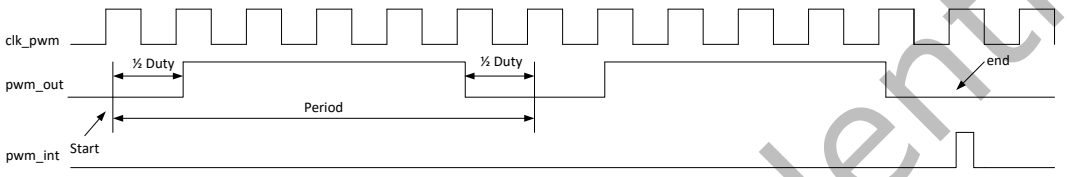

Fig. 21-5PWM One-shot Center-aligned Output Mode

21.4 Register Description

21.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
PWM_PMU(PWM0)	0xFF230000
PWM1	0xFF700000
PWM2	0xFF710000
PWM3	0xFF720000

21.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PWM_PWM0_CNT	0x0000	W	0x00000000	PWM Channel 0 Counter Register
PWM_PWM0_PERIOD_HPR	0x0004	W	0x00000000	PWM Channel 0 Period Register/High Polarity Capture Register
PWM_PWM0_DUTY_LPR	0x0008	W	0x00000000	PWM Channel 0 Duty Register/Low Polarity Capture Register
PWM_PWM0_CTRL	0x000C	W	0x00000000	PWM Channel 0 Control Register
PWM_PWM1_CNT	0x0010	W	0x00000000	PWM Channel 1 Counter Register
PWM_PWM1_PERIOD_HPR	0x0014	W	0x00000000	PWM Channel 1 Period Register/High Polarity Capture Register
PWM_PWM1_DUTY_LPR	0x0018	W	0x00000000	PWM Channel 1 Duty Register/Low Polarity Capture Register
PWM_PWM1_CTRL	0x001C	W	0x00000000	PWM Channel 1 Control Register
PWM_PWM2_CNT	0x0020	W	0x00000000	PWM Channel 2 Counter Register
PWM_PWM2_PERIOD_HPR	0x0024	W	0x00000000	PWM Channel 2 Period Register/High Polarity Capture Register

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Name	Offset	Size	Reset Value	Description
PWM_PWM2_DUTY_LPR	0x0028	W	0x00000000	PWM Channel 2 Duty Register/Low Polarity Capture Register
PWM_PWM2_CTRL	0x002C	W	0x00000000	PWM Channel 2 Control Register
PWM_PWM3_CNT	0x0030	W	0x00000000	PWM Channel 3 Counter Register
PWM_PWM3_PERIOD_HPR	0x0034	W	0x00000000	PWM Channel 3 Period Register/High Polarity Capture Register
PWM_PWM3_DUTY_LPR	0x0038	W	0x00000000	PWM Channel 3 Duty Register/Low Polarity Capture Register
PWM_PWM3_CTRL	0x003C	W	0x00000000	PWM Channel 3 Control Register
PWM_INTSTS	0x0040	W	0x00000000	Interrupt Status Register
PWM_INT_EN	0x0044	W	0x00000000	Interrupt Enable Register
PWM_FIFO_CTRL	0x0050	W	0x00000000	PWM Channel 3 FIFO Mode Control Register
PWM_FIFO_INTSTS	0x0054	W	0x00000010	FIFO Interrupts Status Register
PWM_FIFO_TOUTTHR	0x0058	W	0x00000000	FIFO Timeout Threshold Register
PWM_VERSION_ID	0x005C	W	0x03120B34	PWM Version ID Register
PWM_FIFO	0x0060	W	0x00000000	FIFO Register
PWM_PWRMATCH_CTRL	0x0080	W	0x00000000	Power Key Match Control Register
PWM_PWRMATCH_LPRE	0x0084	W	0x238C22C4	Power Key Match Of Low Preload Register
PWM_PWRMATCH_HPRE	0x0088	W	0x11F81130	Power Key Match Of High Preload Register
PWM_PWRMATCH_LD	0x008C	W	0x029401CC	Power Key Match Of Low Data Register
PWM_PWRMATCH_HD_ZERO	0x0090	W	0x029401CC	Power Key Match Of High Data For Zero Register
PWM_PWRMATCH_HD_ONE	0x0094	W	0x06FE0636	Power Key Match Of High Data For One Register
PWM_PWRMATCH_VALUE0	0x0098	W	0x00000000	Power Key Match Value 0 Register
PWM_PWRMATCH_VALUE1	0x009C	W	0x00000000	Power Key Match Value 1 Register
PWM_PWRMATCH_VALUE2	0x00A0	W	0x00000000	Power Key Match Value 2 Register
PWM_PWRMATCH_VALUE3	0x00A4	W	0x00000000	Power Key Match Value 3 Register
PWM_PWRMATCH_VALUE4	0x00A8	W	0x00000000	Power Key Match Value 4 Register
PWM_PWRMATCH_VALUE5	0x00AC	W	0x00000000	Power Key Match Value 5 Register
PWM_PWRMATCH_VALUE6	0x00B0	W	0x00000000	Power Key Match Value 6 Register
PWM_PWRMATCH_VALUE7	0x00B4	W	0x00000000	Power Key Match Value 7 Register
PWM_PWRMATCH_VALUE8	0x00B8	W	0x00000000	Power Key Match Value 8 Register
PWM_PWRMATCH_VALUE9	0x00BC	W	0x00000000	Power Key Match Value 9 Register
PWM_PWM3_PWRCAPTURE_VALUE	0x00CC	W	0x00000000	Channel 3 Power Key Capture Value Register
PWM_FILTER_CTRL	0x00D0	W	0x00000000	Filter Control Register

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Name	Offset	Size	Reset Value	Description
PWM_PWM0_OFFSET	0x00E0	W	0x00000000	Channel0 Output Offset
PWM_PWM1_OFFSET	0x00E4	W	0x00000000	Channel1 Output Offset
PWM_PWM2_OFFSET	0x00E8	W	0x00000000	Channel2 Output Offset
PWM_PWM3_OFFSET	0x00EC	W	0x00000000	Channel3 Output Offset
PWM_IR_TRANS_CTRL	0x0100	W	0x00001F02	IR Transmission control register
PWM_IR_TRANS_PRE	0x0104	W	0x11942328	IR transmission preload period
PWM_IR_TRANS_SPRE	0x0108	W	0x000008CA	IR transmission simple preload low period
PWM_IR_TRANS_LD	0x010C	W	0x00000230	IR Trans Out Data Low Period
PWM_IR_TRANS_HD	0x0110	W	0x069A0230	IR Trans Out High Period
PWM_IR_TRANS_BURST_FRAME	0x0114	W	0x2261A5E0	IR transmission frame and burst period
PWM_IR_TRANS_DATA_VALUE	0x0118	W	0x00000000	IR Trans Output Data Value
PWM_PWM0_CAPTURE_CNT_EN	0x0120	W	0x00000000	PWM Channel 0 Capture Counter Enable Register
PWM_PWM1_CAPTURE_CNT_EN	0x0124	W	0x00000000	PWM Channel 1 Capture Counter Enable Register
PWM_PWM2_CAPTURE_CNT_EN	0x0128	W	0x00000000	PWM Channel 2 Capture Counter Enable Register
PWM_PWM3_CAPTURE_CNT_EN	0x012C	W	0x00000000	PWM Channel 3 Capture Counter Enable Register
PWM_PWM0_POS_CNT	0x0130	W	0x00000000	PWM Channel 0 Posedge Counter Register
PWM_PWM1_POS_CNT	0x0134	W	0x00000000	PWM Channel 1 Posedge Counter Register
PWM_PWM2_POS_CNT	0x0138	W	0x00000000	PWM Channel 2 Posedge Counter Register
PWM_PWM3_POS_CNT	0x013C	W	0x00000000	PWM Channel 3 Posedge Counter Register
PWM_PWM0_NEG_CNT	0x0140	W	0x00000000	PWM Channel 0 Negedge Counter Register
PWM_PWM1_NEG_CNT	0x0144	W	0x00000000	PWM Channel 1 Negedge Counter Register
PWM_PWM2_NEG_CNT	0x0148	W	0x00000000	PWM Channel 2 Negedge Counter Register
PWM_PWM3_NEG_CNT	0x014C	W	0x00000000	PWM Channel 3 Negedge Counter Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

21.4.3 Detail Registers Description

PWM_PWM0_CNT

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM0_PERIOD_HPR

Address: **Operational Base**+ offset (0x0004)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD_HPR If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM0_DUTY_LPR

Address: **Operational Base**+ offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY_LPR If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM0_CTRL

Address: **Operational Base**+ offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11	RW	0x0	aligned_vld_n 0: Aligned Mode Valid 1: Aligned Mode Invalid
10	RW	0x0	clk_src_sel 1'b0: Select clk_pwm as root clock source, Clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_capture as root clock source, Clock is from crystal oscillator and the frequency is fixed.
9	RW	0x0	clk_sel 1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source. 1'b1: Scaled clock is selected as PWM clock source.

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Bit	Attr	Reset Value	Description
8	RW	0x0	force_clk_en 1'b0: Disabled, when PWM channel is inactive state, the clk_pwm to PWM Clock prescale module is blocked to reduce power consumption. 1'b1: Enabled, the clk_pwm to PWM Clock prescale module is always enabled.
7	RW	0x0	ch_cnt_en 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	conlock pwm period and duty lock to previous configuration 1'b0: Disable lock 1'b1: Enable lock
5	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode, PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt . 2'b01: Continuous mode, PWM produces the waveform continuously. 2'b10: Capture mode, PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved
0	RW	0x0	pwm_en 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWM1_CNT

Address: **Operational Base**+ offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT The 32-bit indicates current value of PWM Channel 1 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM1_PERIOD_HPR

Address: **Operational Base**+ offset (0x0014)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD_HPR If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM1_DUTY_LPR

Address: **Operational Base**+ offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY_LPR If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM1_CTRL

Address: **Operational Base**+ offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11	RW	0x0	aligned_vld_n 0: Aligned Mode Valid 1: Aligned Mode Invalid
10	RW	0x0	clk_src_sel 1'b0: Select clk_pwm as root clock source, Clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_capture as root clock source, Clock is from crystal oscillator and the frequency is fixed.
9	RW	0x0	clk_sel 1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source. 1'b1: Scaled clock is selected as PWM clock source.

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Bit	Attr	Reset Value	Description
8	RW	0x0	force_clk_en 1'b0: Disabled, when PWM channel is inactive state, the clk_pwm to PWM Clock prescale module is blocked to reduce power consumption. 1'b1: Enabled, the clk_pwm to PWM Clock prescale module is always enabled.
7	RW	0x0	ch_cnt_en 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	conlock pwm period and duty lock to previous configuration 1'b0: Disable lock 1'b1: Enable lock
5	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode, PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt. 2'b01: Continuous mode, PWM produces the waveform continuously. 2'b10: Capture mode, PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved
0	RW	0x0	pwm_en 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWM2_CNT

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT The 32-bit indicates current value of PWM Channel 2 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM2_PERIOD_HPR

Address: **Operational Base** + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD_HPR If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM2_DUTY_LPR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY_LPR If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM2_CTRL

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale This fields defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11	RW	0x0	aligned_vld_n 0: Aligned Mode Valid 1: Aligned Mode Invalid
10	RW	0x0	clk_src_sel 1'b0: Select clk_pwm as root clock source, Clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_capture as root clock source, Clock is from crystal oscillator and the frequency is fixed.
9	RW	0x0	clk_sel 1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source. 1'b1: Scaled clock is selected as PWM clock source.

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Bit	Attr	Reset Value	Description
8	RW	0x0	force_clk_en 1'b0: Disabled, when PWM channel is inactive state, the clk_pwm to PWM Clock prescale module is blocked to reduce power consumption. 1'b1: Enabled, the clk_pwm to PWM Clock prescale module is always enabled.
7	RW	0x0	ch_cnt_en 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	conlock pwm period and duty lock to previous configuration 1'b0: Disable lock 1'b1: Enable lock
5	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode, PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt. 2'b01: Continuous mode, PWM produces the waveform continuously. 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved
0	RW	0x0	pwm_en 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWM3_CNT

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT The 32-bit indicates current value of PWM Channel 3 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM3_PERIOD_HPR

Address: **Operational Base** + offset (0x0034)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD_HPR If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM3_DUTY_LPR

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY_LPR If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM3_CTRL

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11	RW	0x0	aligned_vld_n 0: Aligned Mode Valid 1: Aligned Mode Invalid
10	RW	0x0	clk_src_sel 1'b0: Select clk_pwm as root clock source, Clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_capture as root clock source, Clock is from crystal oscillator and the frequency is fixed.
9	RW	0x0	clk_sel 1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source. 1'b1: Scaled clock is selected as PWM clock source.

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Bit	Attr	Reset Value	Description
8	RW	0x0	force_clk_en 1'b0: Disabled, when PWM channel is inactive state, the clk_pwm to PWM Clock prescale module is blocked to reduce power consumption. 1'b1: Enabled, the clk_pwm to PWM Clock prescale module is always enabled.
7	RW	0x0	ch_cnt_en 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	conlock pwm period and duty lock to previous configuration 1'b0: Disable lock 1'b1: Enable lock
5	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode, PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt 2'b01: Continuous mode, PWM produces the waveform continuously. 2'b10: Capture mode, PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved
0	RW	0x0	pwm_en 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_INTSTS

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RO	0x0	CH3_Pol This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM3_PERIOD_HPR to know the effective high cycle of Channel 3 input waveform. Otherwise, please refer to PWM3_PERIOD_LPR to know the effective low cycle of Channel 3 input waveform. Write 1 to CH3_IntSts will clear this bit.

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Bit	Attr	Reset Value	Description
10	RO	0x0	CH2_Pol This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM2_PERIOD_HPR to know the effective high cycle of Channel 2 input waveform. Otherwise, please refer to PWM2_PERIOD_LPR to know the effective low cycle of Channel 2 input waveform. Write 1 to CH2_IntSts will clear this bit.
9	RO	0x0	CH1_Pol This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM1_PERIOD_HPR to know the effective high cycle of Channel 1 input waveform. Otherwise, please refer to PWM1_PERIOD_LPR to know the effective low cycle of Channel 1 input waveform. Write 1 to CH1_IntSts will clear this bit.
8	RO	0x0	CH0_Pol This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM0_PERIOD_HPR to know the effective high cycle of Channel 0 input waveform. Otherwise, please refer to PWM0_PERIOD_LPR to know the effective low cycle of Channel 0 input waveform. Write 1 to CH0_IntSts will clear this bit.
7	W1C	0x0	CH3_pwr_IntSts 1'b0: Channel 3 power key Interrupt not generated 1'b1: Channel 3 power key Interrupt generated
6	W1C	0x0	CH2_pwr_IntSts 1'b0: Channel 2 power key Interrupt not generated 1'b1: Channel 2 power key Interrupt generated
5	W1C	0x0	CH1_pwr_IntSts 1'b0: Channel 1 power keyInterrupt not generated 1'b1: Channel 1 power key Interrupt generated
4	W1C	0x0	CH0_pwr_IntSts 1'b0: Channel 0 power key Interrupt not generated 1'b1: Channel 0 power key Interrupt generated
3	W1C	0x0	CH3_IntSts 1'b0: Channel 3 Interrupt not generated 1'b1: Channel 3 Interrupt generated
2	W1C	0x0	CH2_IntSts 1'b0: Channel 2 Interrupt not generated 1'b1: Channel 2 Interrupt generated
1	W1C	0x0	CH1_IntSts 1'b0: Channel 1 Interrupt not generated 1'b1: Channel 1 Interrupt generated
0	W1C	0x0	CH0_IntSts 1'b0: Channel 0 Interrupt not generated 1'b1: Channel 0 Interrupt generated

PWM_INT_EN

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	CH3_pwr_Int_en 1'b0: Channel 3 power key Interrupt disabled 1'b1: Channel 3 power key Interrupt enabled

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Bit	Attr	Reset Value	Description
6	RW	0x0	CH2_pwr_Int_en 1'b0: Channel 2 power key Interrupt disabled 1'b1: Channel 2 power key Interrupt enabled
5	RW	0x0	CH1_pwr_Int_en 1'b0: Channel 1 power key Interrupt disabled 1'b1: Channel 1 power key Interrupt enabled
4	RW	0x0	CH0_pwr_Int_en 1'b0: Channel 0 power key Interrupt disabled 1'b1: Channel 0 power key Interrupt enabled
3	RW	0x0	CH3_Int_en 1'b0: Channel 3 Interrupt disabled 1'b1: Channel 3 Interrupt enabled
2	RW	0x0	CH2_Int_en 1'b0: Channel 2 Interrupt disabled 1'b1: Channel 2 Interrupt enabled
1	RW	0x0	CH1_Int_en 1'b0: Channel 1 Interrupt disabled 1'b1: Channel 1 Interrupt enabled
0	RW	0x0	CH0_Int_en 1'b0: Channel 0 Interrupt disabled 1'b1: Channel 0 Interrupt enabled

PWM_FIFO_CTRL

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	dma_ch_sel 2'b00: Select PWM0 2'b01: Select PWM1 2'b10: Select PWM2 2'b11: Select PWM3
11	RO	0x0	reserved
10	RW	0x0	dma_ch_sel_en 1'b1: Enable, use dma_ch_sel to select the channel to FIFO mode and DMA mode. 1'b0: Disable, select the channel PWM3 to FIFO mode and DMA mode.
9	RW	0x0	timeout_en FIFO timeout enable
8	RW	0x0	dma_mode_en 1'b1: Enable 1'b0: Disable
7	RO	0x0	reserved
6:4	RW	0x0	almost_full_watermark Almost full Watermark level
3	RW	0x0	watermark_int_en Watermark full interrupt
2	RW	0x0	overflow_int_en When high, an interrupt asserts when the fifo overflow.
1	RW	0x0	full_int_en When high, an interrupt asserts when the FIFO is full.
0	RW	0x0	fifo_mode_sel When high, PWM FIFO mode is activated.

PWM_FIFO_INTSTS

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Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x1	fifo_empty_status This bit indicates the FIFO is empty.
3	W1C	0x0	timieout_intsts Timeout interrupt
2	W1C	0x0	fifo_watermark_full_intsts This bit indicates the FIFO is Watermark Full.
1	W1C	0x0	fifo_overflow_intsts This bit indicates the FIFO is overflow.
0	W1C	0x0	fifo_full_intsts This bit indicates the FIFO is full.

PWM_FIFO_TOUTTHR

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	timeout_threshold FIFO Timeout value(unit pwm clock)

PWM_VERSION_ID

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x03	main_version Main version 8'h0: Base version 8'h1: Support DMA mode 8'h2: Support DMA mode and Power key mode 8'h3: Support DMA mode and Power key mode and IR transmission
23:16	RO	0x12	minor_version Minor version
15:0	RO	0x0b34	svn_version SVN version

PWM_FIFO

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31	RO	0x0	pol This bit indicates the polarity of the lower 31-bit counter. 1'b0: Low 1'b1: High
30:0	RO	0x00000000	cycle_cnt This 31-bit counter indicates the effective cycles of high/low waveform.

PWM_PWRMATCH_CTRL

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	CH3_pwrkey_int_ctrl 1'b0: Assert interrupt after key capture with power key match 1'b1: Assert interrupt after key capture without power key match
14:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	CH3_pwrkey_capture_ctrl 1'b0: Capture the value after interrupt 1'b1: Capture the value directly
10:8	RO	0x0	reserved
7	RW	0x0	CH3_pwrkey_polarity 1'b0: PWM in polarity is positive 1'b1: PWM in polarity is negative
6:4	RO	0x0	reserved
3	RW	0x0	CH3_pwrkey_enable 1'b0: Disabled 1'b1: Enabled
2:0	RO	0x0	reserved

PWM_PWRMATCH_LPRE

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x238c	cnt_max The maximum counter value
15:0	RW	0x22c4	cnt_min The minimum counter value

PWM_PWRMATCH_HPRE

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x11f8	cnt_max The maximum counter value
15:0	RW	0x1130	cnt_min The minimum counter value

PWM_PWRMATCH_LD

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value
15:0	RW	0x01cc	cnt_min The minimum counter value

PWM_PWRMATCH_HD_ZERO

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value
15:0	RW	0x01cc	cnt_min The minimum counter value

PWM_PWRMATCH_HD_ONE

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x06fe	cnt_max The maximum counter value
15:0	RW	0x0636	cnt_min The minimum counter value

PWM_PWRMATCH_VALUE0

Address: **Operational Base** + offset (0x0098)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value0 Power key match value 0

PWM_PWRMATCH_VALUE1

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value1 Power key match value 1

PWM_PWRMATCH_VALUE2

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value2 Power key match value 2

PWM_PWRMATCH_VALUE3

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value3 Power key match value 3

PWM_PWRMATCH_VALUE4

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value4 Power key match value 4

PWM_PWRMATCH_VALUE5

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value5 Power key match value 5

PWM_PWRMATCH_VALUE6

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value6 Power key match value 6

PWM_PWRMATCH_VALUE7

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value7 Power key match value 7

PWM_PWRMATCH_VALUE8

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value8 Power key match value 8

PWM_PWRMATCH_VALUE9

Address: **Operational Base** + offset (0x00BC)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value9 Power key match value 9

PWM_PWM3_PWRCAPTURE_VALUE

Address: **Operational Base** + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pwrkey_capture_value Power key capture value

PWM_FILTER_CTRL

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	pwm3_global_lock PWM3 disable/enable lock to previous configuration 0: PWM3 disable lock to previous configuration 1: PWM3 enable lock to previous configuration
22	RW	0x0	pwm2_global_lock PWM2 disable/enable lock to previous configuration 0: PWM2 disable lock to previous configuration 1: PWM2 enable lock to previous configuration
21	RW	0x0	pwm1_global_lock PWM1 disable/enable lock to previous configuration 0: PWM1 disable lock to previous configuration 1: PWM1 enable lock to previous configuration
20	RW	0x0	pwm0_global_lock PWM0 disable/enable lock to previous configuration 0: PWM0 disable lock to previous configuration 1: PWM0 enable lock to previous configuration
19	RO	0x0	reserved
18	RW	0x0	CH2_and_CH3_switch_en 1'b0: Disabled 1'b1: Enabled
17	RW	0x0	CH1_and_CH3_switch_en 1'b0: Disabled 1'b1: Enabled
16	RW	0x0	CH0_and_CH3_switch_en 1'b0: Disabled 1'b1: Enabled
15:13	RO	0x0	reserved
12:4	RW	0x000	filter_number Filter window number
3	RW	0x0	CH3_input_filter_enable 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	CH2_input_filter_enable 1'b0: Disabled 1'b1: Enabled
1	RW	0x0	CH1_input_filter_enable 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	CH0_input_filter_enable 1'b0: Disabled 1'b1: Enabled

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PWM_PWM0_OFFSET

Address: **Operational Base** + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	channel_output_offset If PWM is operated at the continuous mode or one-shot mode, this value defines the offset of the output waveform. This value is based on the PWM clock. The value ranges from 0 to (period-duty). This register takes effective when output aligned mode is invalid.

PWM_PWM1_OFFSET

Address: **Operational Base** + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	channel_output_offset If PWM is operated at the continuous mode or one-shot mode, this value defines the offset of the output waveform. This value is based on the PWM clock. The value ranges from 0 to (period-duty). This register takes effective when output aligned mode is invalid.

PWM_PWM2_OFFSET

Address: **Operational Base** + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	channel_output_offset If PWM is operated at the continuous mode or one-shot mode, this value defines the offset of the output waveform. This value is based on the PWM clock. The value ranges from 0 to (period-duty). This register takes effective when output aligned mode is invalid.

PWM_PWM3_OFFSET

Address: **Operational Base** + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	channel_output_offset If PWM is operated at the continuous mode or one-shot mode, this value defines the offset of the output waveform. This value is based on the PWM clock. The value ranges from 0 to (period-duty). This register takes effective when output aligned mode is invalid.

PWM_IR_TRANS_CTRL

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x1f	ir_trans_length_within_one_frame 0x00~0x1F represet data lenth 1~32
7:4	RW	0x0	ir_trans_format PWM IR Trans format 4'h0: NEC with simple repeat code 4'h1: NEC with full repeat code 4'h2: TC9012 4'h3: SONY Others: reserved
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x1	ir_state_idle 1'b0: PWM IR Trans Busy 1'b1: PWM IR Trans Idle
0	RW	0x0	ir_trans_out_enable 1'b0: disable PWM IR Trans Out Function 1'b1: enable PWM IR Trans Out Function

PWM_IR_TRANS_PRE

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x1194	ir_trans_out_high_preload IR Trans Out High Preload Register
15:0	RW	0x2328	ir_trans_out_low_preload IR Trans Out Low Preload Register

PWM_IR_TRANS_SPRE

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x08ca	ir_trans_out_low_simple_preload PWM IR Trans Out Low Simple Preload Register

PWM_IR_TRANS_LD

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0230	ir_trans_out_data_low_period IR Trans Out Data Low Period Register

PWM_IR_TRANS_HD

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x069a	ir_trans_out_high_period_for_one IR Trans Out High Period For One Register
15:0	RW	0x0230	ir_trans_out_high_period_for_zero IR Trans Out High Period For Zero Register

PWM_IR_TRANS_BURST_FRAME

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x226	ir_trans_out_burst_period PWM IR Trans Out Burst Period Register
19:18	RO	0x0	reserved
17:0	RW	0x1a5e0	ir_trans_out_frame_period PWM IR Trans Out Frame Period

PWM_IR_TRANS_DATA_VALUE

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ir_trans_out_value PWM IR Trans Out Value Register

PWM_PWM0_CAPTURE_CNT_EN

Address: **Operational Base** + offset (0x0120)

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Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	neg_capture_en Negedge capture counter enable 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	pos_capture_en Posedge capture counter enable 1'b0: Disabled 1'b1: Enabled

PWM_PWM1_CAPTURE_CNT_EN

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	neg_capture_en Negedge capture counter enable 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	pos_capture_en Posedge capture counter enable 1'b0: Disabled 1'b1: Enabled

PWM_PWM2_CAPTURE_CNT_EN

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	neg_capture_en Negedge capture counter enable 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	pos_capture_en Posedge capture counter enable 1'b0: Disabled 1'b1: Enabled

PWM_PWM3_CAPTURE_CNT_EN

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	neg_capture_en Negedge capture counter enable 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	pos_capture_en Posedge capture counter enable 1'b0: Disabled 1'b1: Enabled

PWM_PWM0_POS_CNT

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pos_cnt The 32-bit indicates the number of posedge of PWM Channel 0 input waveform, The value ranges from 0 to (2^32-1).

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PWM_PWM1_POS_CNT

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pos_cnt The 32-bit indicates the number of posedge of PWM Channel 1 input waveform, The value ranges from 0 to (2^32-1).

PWM_PWM2_POS_CNT

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pos_cnt The 32-bit indicates the number of posedge of PWM Channel 2 input waveform, The value ranges from 0 to (2^32-1).

PWM_PWM3_POS_CNT

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pos_cnt The 32-bit indicates the number of posedge of PWM Channel 3 input waveform, The value ranges from 0 to (2^32-1).

PWM_PWM0_NEG_CNT

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	neg_cnt The 32-bit indicates the number of negedge of PWM Channel 0 input waveform, The value ranges from 0 to (2^32-1).

PWM_PWM1_NEG_CNT

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	neg_cnt The 32-bit indicates the number of negedge of PWM Channel 1 input waveform, The value ranges from 0 to (2^32-1).

PWM_PWM2_NEG_CNT

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	neg_cnt The 32-bit indicates the number of negedge of PWM Channel 2 input waveform, The value ranges from 0 to (2^32-1).

PWM_PWM3_NEG_CNT

Address: **Operational Base** + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	neg_cnt The 32-bit indicates the number of negedge of PWM Channel 3 input waveform, The value ranges from 0 to (2^32-1).

21.5 Interface Description

Table 21-1PWM Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
PWM0m0	I/O	UART2_RTSN_M0/PWM0_M0/SPI0_CLK_M0/GPIO0_C3_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L [15:12] = 4'h2
PWM0m1	I/O	SDMMC1_CMD/RGMII_RXD3_M1/I2	GPIO1_IOC_GPIO1C_IOMUX_SE

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Module Pin	Direction	Pad Name	IOMUX Setting
		S0_SCLK_M1/PWM0_M1/GPIO1_C5_d	L_H [7:4] = 4'h4
PWM1m0	I/O	UART6_CTSN_M0/PWM1_M0/SPI0_MOSI_M0/GPIO0_C4_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_H [3:0] = 4'h2
PWM1m1	I/O	SDMMC1_CLK/RGMII_RXCLK_M1/I2S0_MCLK_M1/PWM1_M1/GPIO1_C6_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_H [11:8] = 4'H4
PWM2m0	I/O	UART6_RTSN_M0/PWM2_M0/SPI0_MISO_M0/GPIO0_C5_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_H [7:4] = 4'h2
PWM2m1	I/O	SDMMC1_PWREN/RGMII_MDC_M1/PWM2_M1/I2C5_SCL_M1/RMII_MDC/GPIO1_C7_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_H [15:12] = 4'h3
PWM3m0	I/O	PWM3_M0/GPIO0_A7_d	GPIO0_IOC_GPIO0A_IOMUX_SEL_H [15:12] = 4'h1
PWM3m1	I/O	SDMMC1_DETN/RGMII_MDIO_M1/PWM3_M1/I2C5_SDA_M1/RMII_MDIO/GPIO1_D0_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H [3:0] = 4'h3
PWM4m0	I/O	SPI0_CSN1_M0/PWM4_M0/CPU_AVS/SPDIF_TX_M1/GPIO0_B7_d	GPIO0_IOC_GPIO0B_IOMUX_SEL_H [15:12] = 4'h2
PWM4m1	I/O	UART1_RX_M0/RGMII_TXD0_M1/I2S0_SDO1_M1/PWM4_M1/RMII_TXD0/GPIO1_D1_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_L [7:4] = 4'h4
PWM5m0	I/O	UART2_CTSN_M0/PWM5_M0/SPI0_CSN0_M0/GPIO0_C2_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L [11:8] = 4'h2
PWM5m1	I/O	UART1_TX_M0/RGMII_TXD1_M1/I2S0_SDO2_M1/PWM5_M1/RMII_TXD1/GPIO1_D2_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_L [11:8] = 4'h4
PWM6m0	I/O	UART2_RX_M0/PWM6_M0/NPU_AVS/CAN1_RX_M1/GPIO0_C1_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L [7:4] = 4'h2
PWM6m1	I/O	UART1_RTSN_M0/RGMII_TXEN_M1/I2S0_SDI2_M1/PWM6_M1/RMII_TXEN/GPIO1_D3_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_L [15:12] = 4'h4
PWM7m0	I/O	UART2_TX_M0/PWM7_M0/GPU_AVS/CAN1_TX_M1/GPIO0_C0_d	GPIO0_IOC_GPIO0C_IOMUX_SEL_L [3:0] = 4'h2
PWM7m1	I/O	UART1_CTSN_M0/RGMII_RXD0_M1/I2S0_SDI3_M1/PWM7_M1/RMII_RXD0/GPIO1_D4_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H [3:0] = 4'h4
PWM8m0	I/O	I2S0_LRCK_M0/PWM8_M0/GPIO3_A4_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_H [3:0] = 4'h2
PWM8m1	I/O	SDMMC1_D0/RGMII_TXD2_M1/I2S0_SDI0_M1/PWM8_M1/GPIO1_C1_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L [7:4] = 4'h4
PWM9m0	I/O	I2S0_SDO0_M0/PWM9_M0/GPIO3_A5_d	GPIO3_IOC_GPIO3A_IOMUX_SEL_H [7:4] = 4'h2
PWM9m1	I/O	SDMMC1_D1/RGMII_TXD3_M1/I2S0_SDI1_M1/PWM9_M1/GPIO1_C2_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L [11:8] = 4'h4
PWM10m0	I/O	SDMMC0_D2/JTAG_CPU_MCU_TCK_M1/UART5_CTSN_M0/SPI1_CSN1_M1/PWM10_M0/DSM_AUD_RP/GPIO1_B5_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H [7:4] = 4'h5
PWM10m1	I/O	SDMMC1_D2/RGMII_TXCLK_M1/I2S0_SDO0_M1/PWM10_M1/GPIO1_C3_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L [15:12] = 4'h4
PWM11m0	I/O	SDMMC0_D3/JTAG_CPU_MCU_TMS_M1/UART5_RTSN_M0/SPI1_CSN0_M1/PWM11_M0/DSM_AUD_RN/GPIO1_B6_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H [11:8] = 4'h5
PWM11m1	I/O	SDMMC1_D3/RGMII_RXD2_M1/I2S0_LRCK_M1/PWM11_M1/GPIO1_C4_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_H [3:0] = 4'h4
PWM12m0	I/O	VO_LCDC_D21/RGMII_RXCLK_M0/I2S2_LRCK_M1/PWM12_M0/GPIO4_A1_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H [7:4] = 4'h4
PWM12m1	I/O	I2S1_LRCK_M1/CAM_CLK2_OUT/UART8_CTSN_M0/SPI0_MOSI_M1/PWM12_M1/GPIO3_B4_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H [3:0] = 4'h5

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Module Pin	Direction	Pad Name	IOMUX Setting
PWM13m0	I/O	VO_LCDC_D0/RGMII_TXEN_M0/PWM13_M0/GPIO4_A4_d	GPIO4_IOC_GPIO4A_IOMUX_SEL_H [3:0] = 4'h3
PWM13m1	I/O	I2S1_SDO0_M1/CAM_CLK3_OUT/UART8_RTSN_M0/SPI0_CLK_M1/PWM13_M1/GPIO3_B5_d	GPIO3_IOC_GPIO3B_IOMUX_SEL_H [7:4] = 4'h5
PWM14m0	I/O	VO_LCDC_D4/I2S1_SCLK_M0/UART4_CTSN_M0/PWM14_M0/GPIO3_C5_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H [7:4] = 4'h4
PWM14m1	I/O	I2S2_SDO_M0/RGMII_RXD1_M1/UART4_RTSN_M1/SPI2_MOSI_M1/PWM14_M1/RMII_RXD1/GPIO1_D7_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_H [15:12] = 4'h5
PWM15m0	I/O	VO_LCDC_D5/I2S1_LRCK_M0/UART4_RTSN_M0/PWM15_M0/GPIO3_C6_d	GPIO3_IOC_GPIO3C_IOMUX_SEL_H [11:8] = 4'h4
PWM15m1	I/O	I2S2_SDI_M0/RGMII_RXER_M1/UART4_CTSN_M1/SPI2_MISO_M1/PWM15_M1/RMII_RXER/GPIO2_A0_d	GPIO2_IOC_GPIO2A_IOMUX_SEL_L [3:0] = 4'h5

Notes: I=input, O=output, I/O=input/output, bidirectional

21.6 Application Notes

21.6.1 PWM Capture Mode Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel.
3. Configure the channel to work in the capture mode.
4. Enable the PWM_INT_EN.chx_int_en to enable the interrupt generation.
5. Set PWM_FILTER_CTRL.filter_number, then Enable the PWM_FILTER_CTRL.CHx_input_filter_enable(Optional).
6. Enable the channel by writing '1' to PWM_PWMx_CTRL.pwm_en bit to start the channel.
7. When an interrupt is asserted, refer to INTSTS register to know the raw interrupt status. If the corresponding polarity flag is set, turn to PWM_PWMx_PERIOD_HPC register to know the effective high cycles of input waveforms, otherwise turn to PWM_PWMx_DUTY_LPC register to know the effective low cycles.
8. Write '0' to PWM_PWMx_CTRL.pwm_en to disable the channel.

21.6.2 PWM Capture Modefor Input Pulse Counter Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel.
3. Configure the channel to work in the capture mode.
4. Configure PWM_PWMx_CAPTURE_CNT_EN.pos_capture_en to '1'
5. ConfigurePWM_PWMx_POS_CNT.pos_cnt to '0'
6. Enable the channel by writing '1' to PWM_PWMx_CTRL.pwm_en bit to start the channel.
7. Configure the system timer to work.
8. Read timer couter and save as time_cnt0, and then read PWM_PWMx_POS_CNT.pos_cnt and save as pwm_cnt0.
9. Wait 1 second
10. Read timer couter and save as time_cnt1, and then read PWM_PWMx_POS_CNT.pos_cnt and save as pwm_cnt1.
11. Write '0' to PWM_PWMx_CTRL.pwm_en to disable the channel
12. Calculate the input waveform frequency as following formula: timer_frequency*(pwm_cnt1-pwm_cn0)/(timer_cnt1-timer_cnt0)

21.6.3 PWM Capture DMA Mode Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel.

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3. Configure the channel 3 to work in the capture mode.
4. Configure the PWM_FIFO_CTRL.dma_mode_enand PWM_FIFO_CTRL.fifo_mode_sel to enable the DMA mode. Configure PWM_FIFO_CTRL.almost_full_watermark at appropriate value.
5. Configure DMAC_BUS to transfer data from PWM to DDR.
6. Set PWM_FILTER_CTRL.filter_number, then Enable the PWM_FILTER_CTRL.CHx_input_filter_enable(Optional).
7. Enable the channel by writing '1' to PWM_PWMx_CTRL.pwm_en bit to start the channel.
8. When a dma_req is asserted, DMAC_BUS transfer the data of effective high cycles and low cycles of input waveforms to DDR.
9. Write '0' to PWM_PWMx_CTRL.pwm_en to disable the channel.

21.6.4 PWM Power key Capture Mode Standard Usage Flow

1. Set PWM_PWM3_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWM3_CTRL.prescale and PWM_PWM3_CTRL.scale, and select the clock needed by setting PWM_PWM3_CTRL.clk_sel. The clock should be 1 Mhz after division.
3. Configure the channel to work in the capture mode.
4. Enable the PWM_INT_EN.CH3_int_pwr to enable the interrupt generation.
5. Set the PWM_PWRMATCH_VALUE0~9 registers for the 10 power key match value.
6. Set max_cnt and min_cnt of follow register: PWM_PWRMATCH_LPRE, PWM_PWRMATCH_HPRE, PWM_PWRMATCH_LD, PWM_PWRMATCH_HD_ZERO, PWM_PWRMATCH_HD_ONE. It doesn't need to set these registers when the default value can meet the requirement.
7. Set PWM_PWRMATCH_CTRL.CH3_pwrkey_polarity for the polarity of power key signal, the default value is 0. Enable the PWM_PWRMATCH_CTRL.CH3_pwrkey_enable.
8. Set PWM_FILTER_CTRL.filter_number, then Enable the PWM_FILTER_CTRL.CH3_input_filter_enable(Optional).
9. Enable the channel by writing '1' to PWM_PWM3_CTRL.pwm_en bit to start the channel.
10. When an interrupt is asserted, refer to INTSTS register to know the raw interrupt status, and refer to PWM_PWM3_PWRCAPTURE_VALUE to know the power key capture value.
11. Write '0' to PWM_PWM3_CTRL.pwm_en to disable the channel.

21.6.5 PWM One-shot Mode/ContinuousStandard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for pclk by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel.
3. Choose the output mode by setting PWM_PWMx_CTRL.output_mode, and set the duty polarity and inactive polarity by programming PWM_PWMx_CTRL.duty_pol and PWM_PWMx_CTRL.inactive_pol.
4. Set the PWM_PWMx_CTRL.rpt if the channel is desired to work in the one-shot mode.
5. Configure the channel to work in the one-shot mode or the continuous mode.
6. Enable the PWM_INT_EN.chx_int_en to enable the interrupt generation if if the channel is desired to work in the one-shot mode.
7. If the channel is working in the one-shot mode, an interrupt is asserted after the end of operation, and the PWM_PWMx_CTRL.pwm_en is automatically cleared. Whatever mode the channel is working in, write '0' to PWM_PWMx_CTRL.pwm_en bit to disable the PWM channel.

21.6.6 Low-power UsageFlow

The default value of PWM_PWMx_CTRL.force_clk_enis '0' which make the channel enter the low-power mode. In low-power mode, When the PWM channel is inactive, the clk_pwm to the clock prescale module is gated in order to reduce the power consumption. User can set PWM_PWMx_CTRL.force_clk_en to '1' which will make the channel quit the low-power mode. After the setting, the clk_pwm to the clock prescale module is always enable.

21.6.7 Multi-channel synchronous start UsageFlow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.

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2. Set PWM_FILTER_CTRL.PWMx_global_lock '1' to lock previous configuration.
3. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel.
4. Choose the output mode by setting PWM_PWMx_CTRL.output_mode, and set the duty polarity and inactive polarity by programming PWM_PWMx_CTRL.duty_pol and PWM_PWMx_CTRL.inactive_pol.
5. Set the PWM_PWMx_CTRL.rpt if the channel is desired to work in the one-shot mode.
6. Configure the channel to work in the one-shot mode or the continuous mode.
7. Enable the PWM_INT_EN.chx_int_en to enable the interrupt generation if the channel is desired to work in the one-shot mode.
8. Set PWM_PWMx_CTRL.pwm_en to '1' to start pwm.
9. Set PWM_FILTER_CTRL.PWMx_global_lock '0' to unlock previous configuration and the latest configuration will be take effective immediately.
10. If the channel is working in the one-shot mode, an interrupt is asserted after the end of operation, and the PWM_PWMx_CTRL.pwm_en is automatically cleared.

21.6.8 Multi-channel synchronous stop or frequency change UsageFlow

1. Set PWM_FILTER_CTRL.PWMx_global_lock '1' to lock previous configuration.
2. Set PWM_PWMx_CTRL.pwm_en to '0' to stop pwm or set PWM_PWMx_PERIOD_HPC and PWM_PWMx_DUTY_LPC to change frequency.
3. Set PWM_FILTER_CTRL.PWMx_global_lock '0' to unlock previous configuration and the latest configuration will be take effective immediately.

21.6.9 IR transmission UsageFlow

1. Set PWM_PWM2_CTRL.pwm_en to '0' to disable the PWM channel.
2. Set PWM_IR_TRANS_CTRL.transout_en to '1' enable PWM IR Trans Out Function.
3. Set PWM_IR_TRANS_CTRL.format, PWM_IR_TRANS_CTRL.length, PWM_IR_TRANS_PRE, PWM_IR_TRANS_DATA_VALUE .et.
4. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWM2_CTRL.prescale and PWM_PWM2_CTRL.scale, and select the clock needed by setting PWM_PWM2_CTRL.clk_sel. The clock should be 1 MHz after division.
5. Choose the output mode by setting PWM_PWM2_CTRL.output_mode, and set the duty polarity and inactive polarity by programming PWM_PWM2_CTRL.duty_pol and PWM_PWM2_CTRL.inactive_pol.
6. Set the PWM_PWM2_CTRL.rpt if the channel is desired to work in the one-shot mode.
7. Enable the channel by writing '1' to PWM_PWM3_CTRL.pwm_en bit to start the channel.
8. If you want to disable the output waveform, write '0' PWM_PWM2_CTRL.pwm_en, and the channel will be disable at the end of one frame. Please refer to PWM_IR_TRANS_CTRL.idle to see if the channel is true stop.

21.6.10 Other notes

When the channel is active to produce waveforms, it is free to program the PWM_PWMx_PERIOD_HPC and PWM_PWMx_DUTY_LPC register. User can use PWM_PWMx_CTRL.conlock to take period and duty effect at the same time. The usage flow is as follow:

1. Set PWM_PWMx_CTRL.conlock to '1'.
2. Set PWM_PWMx_PERIOD_HPC and PWM_PWMx_DUTY_LPC.
3. Set PWM_PWMx_CTRL.conlock to '0', others bits in PWM_PWMx_CTRL should be appropriate.

After above configuration, the change will not take effect immediately until the current period ends.

An active channel can be changed to another operation mode without disable the PWM channel. However, during the transition of the operation mode there may be some irregular output waveforms. So does changing the clock division factor when the channel is active.

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Chapter 22 Watchdog Timer (WDT)

22.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that caused by conflicting parts or programs in a SOC. The WDT would generate interrupt or reset signal when its counter reaches zero, then a reset controller would reset the system.

WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock can be chosen from 24MHz or 32KHz clock
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined ranges of main timeout period
- There are 3 WDTs: WDT, WDTS, WDT_PMU
- All the five WDTs can drive CRU to generate global software reset

22.2 Block Diagram

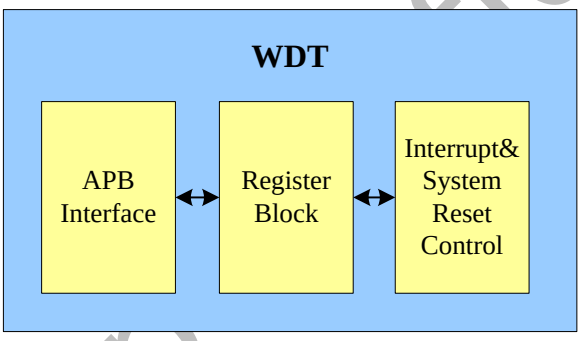

Fig. 22-1 WDT Block Diagram

WDT is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & System Reset Control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

22.3 Function Description

22.3.1 Operation

22.3.1.1 Counter

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR).

22.3.1.2 Interrupts

The WDT can be programmed to generate an interrupt (and then a system reset) when a timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the

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Watchdog Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

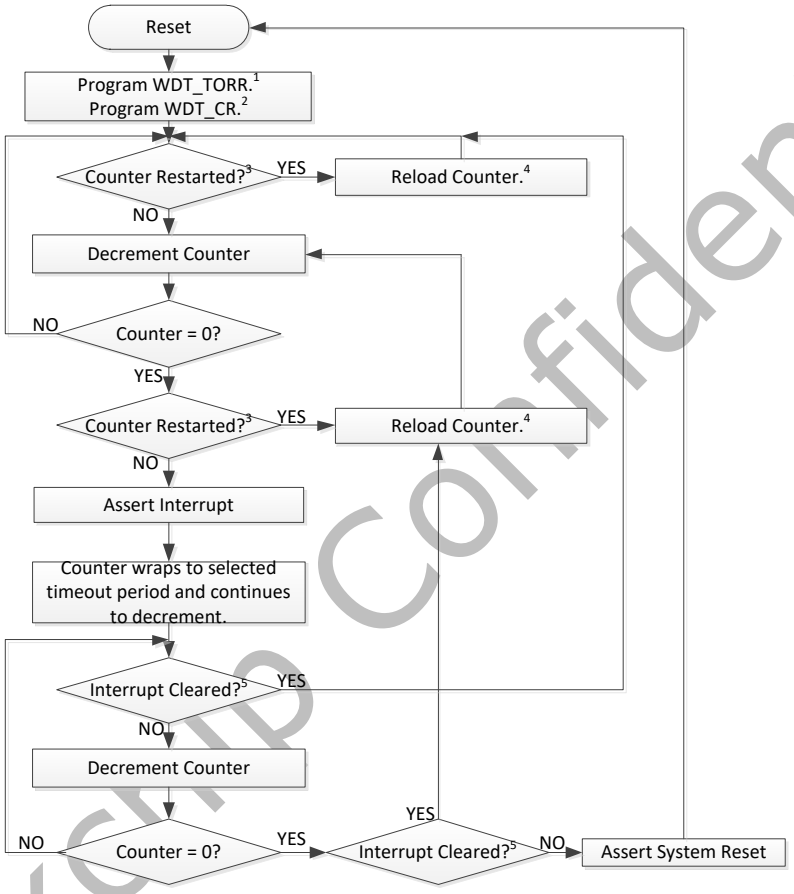
22.3.1.3 System Resets

When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

22.3.1.4 Reset Pulse Length

The reset pulse length is the number of pclk cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

22.3.2 Programming Sequence



1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 22-2 WDT Operation Flow (RMOD=1)

22.4 Register Description

22.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
WDTNS	0xFFA60000
WDTS	0xFF900000
WDTPMU	0xFF2A0000

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22.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
WDT_CR	0x0000	W	0x00000008	Control Register
WDT_TORR	0x0004	W	0x00000000	Timeout Range Register
WDT_CCVR	0x0008	W	0x0000FFFF	Current Counter Value Register
WDT_CRR	0x000C	W	0x00000000	Counter Restart Register
WDT_STAT	0x0010	W	0x00000000	Interrupt Status Register
WDT_EOI	0x0014	W	0x00000000	Interrupt Clear Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

22.4.3 Detail Register Description

WDT_CR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x2	rst_pluse_length This is used to select the number of pclk cycles for which the system reset stays asserted. 3'b000: 2 pclk cycles 3'b001: 4 pclk cycles 3'b010: 8 pclk cycles 3'b011: 16 pclk cycles 3'b100: 32 pclk cycles 3'b101: 64 pclk cycles 3'b110: 128 pclk cycles 3'b111: 256 pclk cycles
1	RW	0x0	resp_mode Selects the output response generated to a timeout. 1'b0: Generate a system reset. 1'b1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset.
0	RW	0x0	en This bit is used to enable and disable the WDT.When disabled, the counter dose not decrement .Thus, no interrupt or system reset are generated. Once this bit has been enabled, it can be cleared only by a system reset. 1'b0: WDT disabled. 1'b1: WDT enabled.

WDT_TORR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	timeout_period This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values available for a 32-bit watchdog counter are: 4'b0000: 0x0000ffff 4'b0001: 0x0001ffff 4'b0010: 0x0003ffff 4'b0011: 0x0007ffff 4'b0100: 0x000fffff 4'b0101: 0x001fffff 4'b0110: 0x003fffff

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Bit	Attr	Reset Value	Description
			4'b0111: 0x007fffff 4'b1000: 0x00ffffff 4'b1001: 0x01ffffff 4'b1010: 0x03ffffff 4'b1011: 0x07ffffff 4'b1100: 0x0fffffff 4'b1101: 0x1fffffff 4'b1110: 0x3fffffff 4'b1111: 0x7fffffff

WDT_CCVR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000ffff	cur_cnt This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read.

WDT_CRR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	cnt_restart This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

WDT_STAT

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	status This register shows the interrupt status of the WDT. 1'b1: Interrupt is active regardless of polarity. 1'b0: Interrupt is inactive.

WDT_EOI

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	int_clr This can be used to clear the interrupt without restarting the watchdog counter.

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Chapter 23 SARADC

23.1 Overview

The ADC is an 8-channel single-ended 10-bit Successive Approximation Register (SAR) A/D Converter. It uses the supply and ground as its reference which avoids the use of any external reference. The input range is typically 0V to 1.8V.
SARADC controller supports the following features:

- Support single mode and series conversion mode.
- In single mode, the conversion operates once each software is accessed.
- In series conversion, the controller samples each channel then loops until the software stops conversion.
- High/low threshold can be set, higher/lower/between high-low-threshold interrupt can be enabled

23.2 Block Diagram

SARADC block shows in the following figure. This includes:

- APB Interface
- Control FSM
- SARADC PHY

The software can configure the SARADC controller by APB interface, then the inter FSM will communicate with SARADC PHY for limited timing requests.

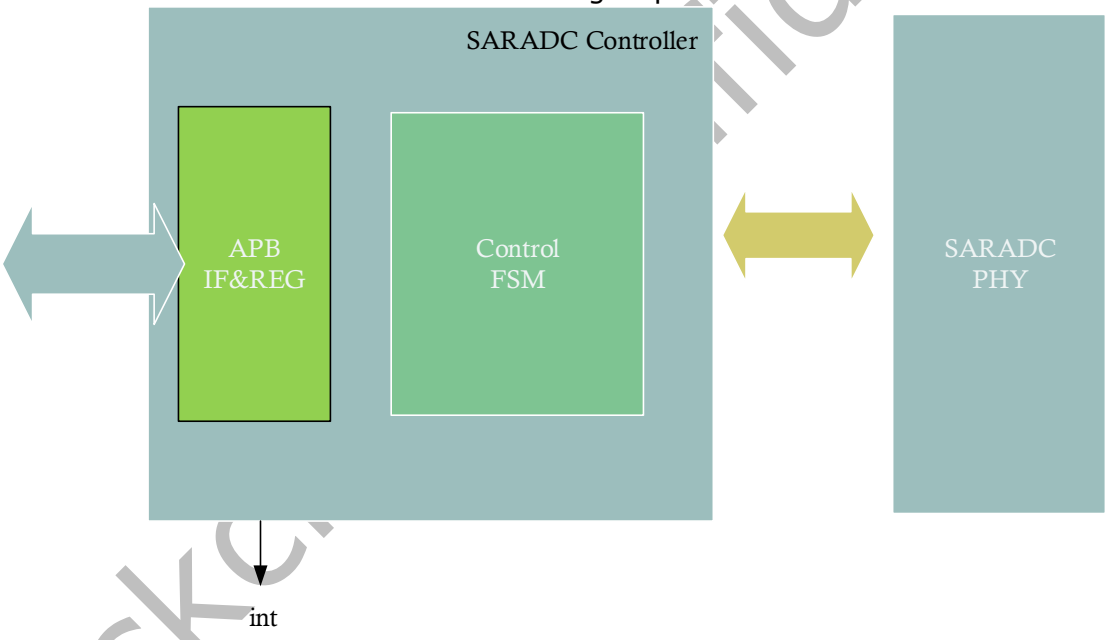

Fig. 23-1 SARADC Block Diagram

23.3 Function Description

SARADC block includes controller and PHY, user cannot directly access SARADC PHY. Software access the SARADC through SARADC controller by APB interface. SARADC controller will sample the conversion result from SARADC PHY.

23.4 Register Description

23.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SARADC0	0xFF730000
SARADC1	0xFFAA0000

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23.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SARADC_CONV_CON	0x0000	W	0x00000000	Conversion control
SARADC_T_PD_SOC	0x0004	W	0x00026000	Timing control for PD to SOC
SARADC_T_AS_SOC	0x0008	W	0x00000000	Timing control for assert SOC
SARADC_T_DAS_SOC	0x000C	W	0x00000007	Timing control from dis-assert SOC to change channel
SARADC_T_SEL_SOC	0x0010	W	0x00000002	Timimg control from change channel sel to assert SOC
SARADC_HIGH_COMP0	0x0014	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP1	0x0018	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP2	0x001C	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP3	0x0020	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP4	0x0024	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP5	0x0028	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP7	0x0030	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP8	0x0034	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP9	0x0038	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP10	0x003C	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP11	0x0040	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP12	0x0044	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP13	0x0048	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP14	0x004C	W	0x00000000	High threshold for adc output data
SARADC_HIGH_COMP15	0x0050	W	0x00000000	High threshold for adc output data
SARADC_LOW_COMP0	0x0054	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP1	0x0058	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP2	0x005C	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP3	0x0060	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP4	0x0064	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP5	0x0068	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP6	0x006C	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP7	0x0070	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP8	0x0074	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP9	0x0078	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP10	0x007C	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP11	0x0080	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP12	0x0084	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP13	0x0088	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP14	0x008C	W	0x00000000	Low threshold for adc output data
SARADC_LOW_COMP15	0x0090	W	0x00000000	Low threshold for adc output data
SARADC_DEBOUNCE	0x0094	W	0x00000003	Threshold debounce
SARADC_HT_INT_EN	0x0098	W	0x00000000	High threshold int enable
SARADC_LT_INT_EN	0x009C	W	0x00000000	Low threshold int enable
SARADC_MT_INT_EN	0x0100	W	0x00000000	Middle threshold int enable
SARADC_END_INT_EN	0x0104	W	0x00000000	End conversion int enable
SARADC_ST_CON	0x0108	W	0x0000001C	Adc static control
SARADC_STATUS	0x010C	W	0x00000002	Adc status
SARADC_END_INT_ST	0x0110	W	0x00000000	End conversion int state
SARADC_HT_INT_ST	0x0114	W	0x00000000	High threshold int state
SARADC_LT_INT_ST	0x0118	W	0x00000000	Low threshold int state
SARADC_MT_INT_ST	0x011C	W	0x00000000	Middle threshold int state
SARADC_DATA0	0x0120	W	0x00000000	ADC output data
SARADC_DATA1	0x0124	W	0x00000000	ADC output data

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Name	Offset	Size	Reset Value	Description
SARADC_DATA2	0x0128	W	0x00000000	ADC output data
SARADC_DATA3	0x012C	W	0x00000000	ADC output data
SARADC_DATA4	0x0130	W	0x00000000	ADC output data
SARADC_DATA5	0x0134	W	0x00000000	ADC output data
SARADC_DATA6	0x0138	W	0x00000000	ADC output data
SARADC_DATA7	0x013C	W	0x00000000	ADC output data
SARADC_DATA8	0x0140	W	0x00000000	ADC output data
SARADC_DATA9	0x0144	W	0x00000000	ADC output data
SARADC_DATA10	0x0148	W	0x00000000	ADC output data
SARADC_DATA11	0x014C	W	0x00000000	ADC output data
SARADC_DATA12	0x0150	W	0x00000000	ADC output data
SARADC_DATA13	0x0154	W	0x00000000	ADC output data
SARADC_DATA14	0x0158	W	0x00000000	ADC output data
SARADC_DATA15	0x015C	W	0x00000000	ADC output data
SARADC_AUTO_CH_EN	0x0160	W	0x00000000	Channel enable in auto channel mode

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.4.3 Detail Registers Description

SARADC_CONV_CON

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	int_lock This is used to lock the sample data when interrupt happened. 1'b1: Enable lock. 1'b0: Disable lock.
8	RW	0x0	as_pd_mode If this bit is set to 1'b1, each time conversion ends, PD will be asserts. Then next time conversion starts, PD will be set to low auto automaticly. This is not used in signal mode.
7	W1C	0x0	end_conv End conversion, this is not used when CONV_CON[5] is set to 1'b1. If this bit set to 1'b1, PD will set to 1'b1 after the last conversion and this bit will be cleared to 1'b0.
6	RW	0x0	auto_channel_mode Auto channel mode. If this is enable, channel will be round auto according which is set in AUTO_CH_EN.
5	RW	0x0	single_pd_mode Single conversion mode. If this bit is set to 1, conversion only operate once, then PD single will be set to 1.
4	W1C	0x0	start_adc Enable adc, if this bit set to one, conversion will start. Then this bit will be clear to 0.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	channel_sel Channel for SARADC, 16 channel is supported. This fileld is not used when CONV_CON[6] is set to 1. 4'd0: sel channel 0. 4'd1: sel channel 1. 4'd2: sel channel 2. 4'd3: sel channel 3. 4'd4: sel channel 4. 4'd5: sel channel 5. 4'd6: sel channel 6. 4'd7: sel channel 7.

SARADC_T_PD_SOC

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:13	RW	0x13	t_pd_soc Timing control between power up to start-of-conversion.
12:0	RO	0x0000	reserved

SARADC_T_AS_SOC

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t_as_soc Timing control for assert SOC signal.

SARADC_T_DAS_SOC

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000007	t_das_soc Timing form dis-assret SOC to channel sel change.

SARADC_T_SEL_SOC

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0002	t_sel_soc Timing form channel load to SOC assert.

SARADC_HIGH_COMP0

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp0 High threshold for adc output data for channel 0.

SARADC_HIGH_COMP1

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp1 High threshold for adc output data for channel 1.

SARADC_HIGH_COMP2

Address: **Operational Base** + offset (0x001C)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp2 High threshold for adc output data for channel 2.

SARADC_HIGH_COMP3

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp3 High threshold for adc output data for channel 3.

SARADC_HIGH_COMP4

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp4 High threshold for adc output data for channel 4.

SARADC_HIGH_COMP5

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp5 High threshold for adc output data for channel 5.

SARADC_HIGH_COMP7

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp7 High threshold for adc output data for channel 7.

SARADC_HIGH_COMP8

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp8 Not used in this application.

SARADC_HIGH_COMP9

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp9 Not used in this application.

SARADC_HIGH_COMP10

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp10 Not used in this application.

SARADC_HIGH_COMP11

Address: **Operational Base** + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp11 Not used in this application.

SARADC_HIGH_COMP12

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp12 Not used in this application.

SARADC_HIGH_COMP13

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp13 Not used in this application.

SARADC_HIGH_COMP14

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp14 Not used in this application.

SARADC_HIGH_COMP15

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp15 Not used in this application.

SARADC_LOW_COMP0

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp0 Low threshold for adc output data for channel 0.

SARADC_LOW_COMP1

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp1 Low threshold for adc output data for channel 1.

SARADC_LOW_COMP2

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp2 Low threshold for adc output data for channel 2.

SARADC_LOW_COMP3

Address: **Operational Base** + offset (0x0060)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp3 Low threshold for adc output data for channel 3.

SARADC_LOW_COMP4

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp4 Low threshold for adc output data for channel 4.

SARADC_LOW_COMP5

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp5 Low threshold for adc output data for channel 5.

SARADC_LOW_COMP6

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp6 Low threshold for adc output data for channel 6.

SARADC_LOW_COMP7

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp7 Low threshold for adc output data for channel 7.

SARADC_LOW_COMP8

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp8 Not used in this application.

SARADC_LOW_COMP9

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp9 Not used in this application.

SARADC_LOW_COMP10

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	low_comp10 Not used in this application.

SARADC_LOW_COMP11

Address: **Operational Base** + offset (0x0080)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp11 Not used in this application.

SARADC_LOW_COMP12

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp12 Not used in this application.

SARADC_LOW_COMP13

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	low_comp13 Not used in this application.

SARADC_LOW_COMP14

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp14 Not used in this application.

SARADC_LOW_COMP15

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp15 Not used in this application.

SARADC_DEBOUNCE

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce ADC controller will only generate interrupt data is higher/lower/between setting threshold for "debounce" times.

SARADC_HT_INT_EN

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	ht_int_en15 Not used in this application.
14	RW	0x0	ht_int_en14 Not used in this application.
13	RW	0x0	ht_int_en13 Not used in this application.
12	RW	0x0	ht_int_en12 Not used in this application.

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Bit	Attr	Reset Value	Description
11	RW	0x0	ht_int_en11 Not used in this application.
10	RW	0x0	ht_int_en10 Not used in this application.
9	RW	0x0	ht_int_en9 Not used in this application.
8	RW	0x0	ht_int_en8 Not used in this application.
7	RW	0x0	ht_int_en7 High threshold interrupt for channel7. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
6	RW	0x0	ht_int_en6 High threshold interrupt for channel6. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
5	RW	0x0	ht_int_en5 High threshold interrupt for channel5. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
4	RW	0x0	ht_int_en4 High threshold interrupt for channel4. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
3	RW	0x0	ht_int_en3 High threshold interrupt for channel3. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
2	RW	0x0	ht_int_en2 High threshold interrupt for channel2. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
1	RW	0x0	ht_int_en1 High threshold interrupt for channel1. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
0	RW	0x0	ht_int_en0 High threshold interrupt for channel0. 1'b1: Enable ht intr. 1'b0: Disable ht intr.

SARADC_LT_INT_EN

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	lt_int_en15 Not used in this application.
14	RW	0x0	lt_int_en14 Not used in this application.
13	RW	0x0	lt_int_en13 Not used in this application.

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Bit	Attr	Reset Value	Description
12	RW	0x0	lt_int_en12 Not used in this application.
11	RW	0x0	lt_int_en11 Not used in this application.
10	RW	0x0	lt_int_en10 Not used in this application.
9	RW	0x0	lt_int_en9 Not used in this application.
8	RW	0x0	lt_int_en8 Not used in this application.
7	RW	0x0	lt_int_en7 Low threshold interrupt for channel7. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
6	RW	0x0	lt_int_en6 Low threshold interrupt for channel6. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
5	RW	0x0	lt_int_en5 Low threshold interrupt for channel5. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
4	RW	0x0	lt_int_en4 Low threshold interrupt for channel4. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
3	RW	0x0	lt_int_en3 Low threshold interrupt for channel3. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
2	RW	0x0	lt_int_en2 Low threshold interrupt for channel2. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
1	RW	0x0	lt_int_en1 Low threshold interrupt for channel1. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
0	RW	0x0	lt_int_en0 Low threshold interrupt for channel0. 1'b1: Enable ht intr. 1'b0: Disable ht intr.

SARADC_MT_INT_EN

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mt_int_en15 Not used in this application.
14	RW	0x0	mt_int_en14 Not used in this application.

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Bit	Attr	Reset Value	Description
13	RW	0x0	mt_int_en13 Not used in this application.
12	RW	0x0	mt_int_en12 Not used in this application.
11	RW	0x0	mt_int_en11 Not used in this application.
10	RW	0x0	mt_int_en10 Not used in this application.
9	RW	0x0	mt_int_en9 Not used in this application.
8	RW	0x0	mt_int_en8 Not used in this application.
7	RW	0x0	mt_int_en7 Middle threshold interrupt for channel7. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
6	RW	0x0	mt_int_en6 Middle threshold interrupt for channel6. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
5	RW	0x0	mt_int_en5 Middle threshold interrupt for channel5. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
4	RW	0x0	mt_int_en4 Middle threshold interrupt for channel4. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
3	RW	0x0	mt_int_en3 Middle threshold interrupt for channel3. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
2	RW	0x0	mt_int_en2 Middle threshold interrupt for channel2. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
1	RW	0x0	mt_int_en1 Middle threshold interrupt for channel1. 1'b1: Enable ht intr. 1'b0: Disable ht intr.
0	RW	0x0	mt_int_en0 Middle threshold interrupt for channel0. 1'b1: Enable ht intr. 1'b0: Disable ht intr.

SARADC_END_INT_EN

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	end_int_en 1'b1: Enable end conversion intr. 1'b0: Disable end conversion intr.

SARADC_ST_CON

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x3	ictrl Control the bias current of the preamplifier in the SAR-ADC
2:0	RW	0x4	cctrl Control the capacitance of the capacitor DAC array, which is related to the linearity of the SAR-ADC.

SARADC_STATUS

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:2	RO	0x0	sel Adc channel sel.
1	RO	0x1	pd 1'b1: ADC is power down. 1'b0: ADC is power up and in conversion.
0	RO	0x0	conv_st Conversion status 1'b1: ADC controller fsm is busy. 1'b0: ADC controller fsm is idle.

SARADC_END_INT_ST

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	end_int_st ADC end conversion interrupt status. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.

SARADC_HT_INT_ST

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	ht_int_st15 Not used in this application.
14	W1C	0x0	ht_int_st14 Not used in this application.
13	W1C	0x0	ht_int_st13 Not used in this application.
12	W1C	0x0	ht_int_st12 Not used in this application.
11	W1C	0x0	ht_int_st11 Not used in this application.
10	W1C	0x0	ht_int_st10 Not used in this application.
9	W1C	0x0	ht_int_st9 Not used in this application.

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Bit	Attr	Reset Value	Description
8	W1C	0x0	ht_int_st8 Not used in this application.
7	W1C	0x0	ht_int_st7 High threshold interrupt state for channel7. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
6	W1C	0x0	ht_int_st6 High threshold interrupt state for channel6. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
5	W1C	0x0	ht_int_st5 High threshold interrupt state for channel5. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
4	W1C	0x0	ht_int_st4 High threshold interrupt state for channel4. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
3	W1C	0x0	ht_int_st3 High threshold interrupt state for channel3. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
2	W1C	0x0	ht_int_st2 High threshold interrupt state for channel2. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
1	W1C	0x0	ht_int_st1 High threshold interrupt state for channel1. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
0	W1C	0x0	ht_int_st0 High threshold interrupt state for channel0. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.

SARADC_LT_INT_ST

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	lt_int_st15 Not used in this application.
14	W1C	0x0	lt_int_st14 Not used in this application.
13	W1C	0x0	lt_int_st13 Not used in this application.
12	W1C	0x0	lt_int_st12 Not used in this application.
11	W1C	0x0	lt_int_st11 Not used in this application.
10	W1C	0x0	lt_int_st10 Not used in this application.
9	W1C	0x0	lt_int_st9 Not used in this application.
8	W1C	0x0	lt_int_st8 Not used in this application.

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Bit	Attr	Reset Value	Description
7	W1C	0x0	lt_int_st7 Low threshold interrupt state for channel7. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
6	W1C	0x0	lt_int_st6 Low threshold interrupt state for channel6. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
5	W1C	0x0	lt_int_st5 Low threshold interrupt state for channel5. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
4	W1C	0x0	lt_int_st4 Low threshold interrupt state for channel4. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
3	W1C	0x0	lt_int_st3 Low threshold interrupt state for channel3. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
2	W1C	0x0	lt_int_st2 Low threshold interrupt state for channel2. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
1	W1C	0x0	lt_int_st1 Low threshold interrupt state for channel1. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
0	W1C	0x0	lt_int_st0 Low threshold interrupt state for channel0. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.

SARADC_MT_INT_ST

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	mt_int_st15 Not used in this application.
14	W1C	0x0	mt_int_st14 Not used in this application.
13	W1C	0x0	mt_int_st13 Not used in this application.
12	W1C	0x0	mt_int_st12 Not used in this application.
11	W1C	0x0	mt_int_st11 Not used in this application.
10	W1C	0x0	mt_int_st10 Not used in this application.
9	W1C	0x0	mt_int_st9 Not used in this application.
8	W1C	0x0	mt_int_st8 Not used in this application.

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Bit	Attr	Reset Value	Description
7	W1C	0x0	mt_int_st7 Between high and low threshold interrupt state for channel7. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
6	W1C	0x0	mt_int_st6 Between high and low threshold interrupt state for channel6. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
5	W1C	0x0	mt_int_st5 Between high and low threshold interrupt state for channel5. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
4	W1C	0x0	mt_int_st4 Between high and low threshold interrupt state for channel4. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
3	W1C	0x0	mt_int_st3 Between high and low threshold interrupt state for channel3. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
2	W1C	0x0	mt_int_st2 Between high and low threshold interrupt state for channel2. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
1	W1C	0x0	mt_int_st1 Between high and low threshold interrupt state for channel1. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.
0	W1C	0x0	mt_int_st0 Between high and low threshold interrupt state for channel0. 1'b1: Interrupt happened. 1'b0: Interrupt not happened.

SARADC_DATA0

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data0 ADC channel 0 data.

SARADC_DATA1

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data1 ADC channel 1 data.

SARADC_DATA2

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data2 ADC channel 2 data.

SARADC_DATA3

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Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data3 ADC channel 3 data.

SARADC_DATA4

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data4 ADC channel 4 data.

SARADC_DATA5

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data5 ADC channel 5 data.

SARADC_DATA6

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data6 ADC channel 6 data.

SARADC_DATA7

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data7 ADC channel 7 data.

SARADC_DATA8

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data8 Not used in this application.

SARADC_DATA9

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data9 Not used in this application.

SARADC_DATA10

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data10 Not used in this application.

SARADC_DATA11

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Address: **Operational Base** + offset (0x014C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data11 Not used in this application.

SARADC_DATA12

Address: **Operational Base** + offset (0x0150)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data12 Not used in this application.

SARADC_DATA13

Address: **Operational Base** + offset (0x0154)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data13 Not used in this application.

SARADC_DATA14

Address: **Operational Base** + offset (0x0158)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data14 Not used in this application.

SARADC_DATA15

Address: **Operational Base** + offset (0x015C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data15 Not used in this application.

SARADC_AUTO_CH_EN

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	auto_ch15_en Not used in this application.
14	RW	0x0	auto_ch14_en Not used in this application.
13	RW	0x0	auto_ch13_en Not used in this application.
12	RW	0x0	auto_ch12_en Not used in this application.
11	RW	0x0	auto_ch11_en Not used in this application.
10	RW	0x0	auto_ch10_en Not used in this application.
9	RW	0x0	auto_ch9_en Not used in this application.

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Bit	Attr	Reset Value	Description
8	RW	0x0	auto_ch8_en Not used in this application.
7	RW	0x0	auto_ch7_en Enable channel 7 in auto channel mode.
6	RW	0x0	auto_ch6_en Enable channel 6 in auto channel mode.
5	RW	0x0	auto_ch5_en Enable channel 5 in auto channel mode.
4	RW	0x0	auto_ch4_en Enable channel 4 in auto channel mode.
3	RW	0x0	auto_ch3_en Enable channel 3 in auto channel mode.
2	RW	0x0	auto_ch2_en Enable channel 2 in auto channel mode.
1	RW	0x0	auto_ch1_en Enable channel 1 in auto channel mode.
0	RW	0x0	auto_ch0_en Enable channel 0 in auto channel mode.

23.5 Application Notes

Steps of ADC conversion in series conversion mode:

- Decide which channel should be used and whether auto_channel mode should be set. In auto_channel mode, the channel will be changed from 0-1 then to 0. Please refer to the SARADC_CONV_CON register.
- Set SARADC_CONV_CON[4] to 1'b1, then the conversion will start.
- If conversion wants to be ended, set SARADC_CONV_CON[7] to 1'b1.
- Conversion could be read from SARADC_DATAn (n is from 0-1).
- If threshold compare interrupt wants to be used, high/low threshold could be set, and interrupt should be set as an application.
- If auto_channel mode is not set, you could set the channel as an application.

Steps of ADC conversion in single mode:

- Decide which channel should be used and set SARADC_CONV_CON[3:0].
- Set SARADC_CONV_CON[5] to 1'b1.
- Set SARADC_CONV_CON[4] to 1'b1, then the conversion will start.
- The conversion only operates once then ends. PD will be asserted and PD status could be got by reading SARADC_STATUS.
- Conversion could be read from SARADC_DATAn (n is from 0-1).

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Chapter 24 Temperature-Sensor ADC (TS-ADC)

24.1 Overview

TS-ADC Controller is used to control and get the temperature information. TS-ADC will convert for each enabled channel in loop after the initial setting and can be stopped by software. If you find that the temperature is High in a period of time, an interrupt is generated to the processor down-measures taken; if the temperature over a period of time High, the resulting TSHUT gave CRU module, let it reset the entire chip, or via GPIO give PMIC. Also, if you find that the temperature Low in a period of time, an interrupt can be generated.

TS-ADC Controller supports the following features:

- The temperature for High and Low interrupt can be configurable
- The temperature of system reset can be configurable
- The time interval of temperature detection can be configurable
- When detecting a high temperature, the time interval of temperature detection can be configurable
- High temperature debounce can be configurable
- An interrupt can be generated after TS-ADC converts all setting channel
- 5°C temperature resolution

24.2 Block Diagram

TS-ADC controller is comprised of:

- APB Interface
- TS-ADC control logic

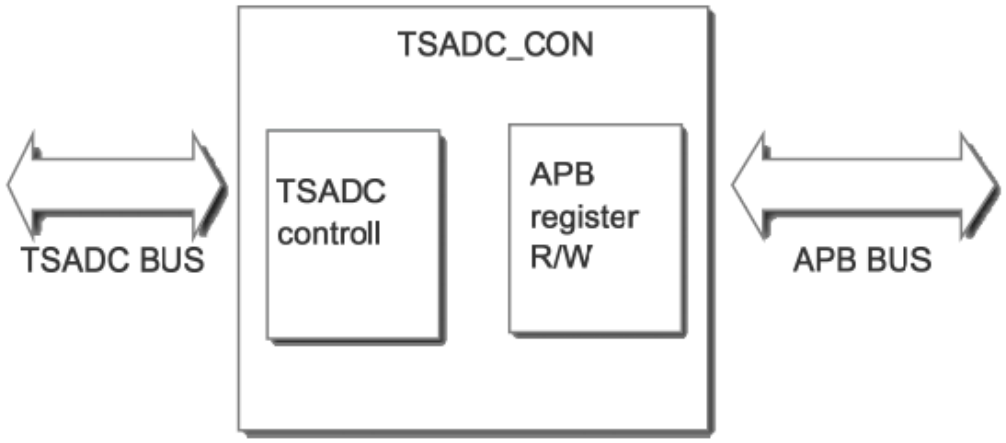

Fig. 24-1 TS-ADC Controller Block Diagram

24.3 Function Description

24.3.1 APB Interface

There is an APB Slave interface in TS-ADC Controller, which is used to configure the TS-ADC Controller registers and look up the temperature from the temperature sensor.

24.3.2 TS-ADC Controller

This block is used to control the TS-ADC PHY to meet the conversion timing and receive the temperature information from TS-ADC PHY.

24.4 Register Description

24.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

24.4.2 Registers Summary

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Name	Offset	Size	Reset Value	Description
TSADC_USER_CON	0x0000	W	0x00000000	User control
TSADC_AUTO_CON	0x0004	W	0x00000000	Auto control
TSADC_AUTO_STATUS	0x0008	W	0x00000000	Status used in auto mode
TSADC_AUTO_SRC	0x000C	W	0x00000000	Channel sel for tsadc in auto mode
TSADC_LT_EN	0x0010	W	0x00000000	Low temperature check logic enable
TSADC_HT_INT_EN	0x0014	W	0x00000000	High temperature interrupt enable
TSADC_GPIO_EN	0x0018	W	0x00000000	Temperature violation to gpio enable
TSADC_CRU_EN	0x001C	W	0x00000000	Temperature violation to cru enable
TSADC_LT_INT_EN	0x0020	W	0x00000000	Low temperature interrupt enable
TSADC_HLT_INT_PD	0x0024	W	0x00000000	High and low temperature interrupt status
TSADC_EOC_HSHUT_PD	0x0028	W	0x00000000	High temperature shut and round int status
TSADC_DATA0	0x002C	W	0x00000000	Channel0 data
TSADC_COMP0_INT	0x006C	W	0x00000000	High temperature interrupt threshold for channel0
TSADC_COMP0_SHUT	0x010C	W	0x00000000	High temperature shut threshold for channel0
TSADC_HIGH_INT_DEBOUNCE	0x014C	W	0x00000003	High interrupt debounce
TSADC_HIGH_TSHUT_DEBOUNCE	0x0150	W	0x00000003	High shut debounce
TSADC_AUTO_PERIOD	0x0154	W	0x00010000	Auto conversion period
TSADC_AUTO_PERIOD_HT	0x0158	W	0x00010000	Auto conversion period for high tempture
TSADC_COMP0_LOW_INT	0x015C	W	0x00000000	Low temperature threshold for channel0
TSADC_T_SETUP	0x019C	W	0x0000005F	Timing for setup
TSADC_T_PW_EN	0x0200	W	0x00000000	Timing for pw_en
TSADC_T_EN_CLK	0x0204	W	0x00000001	Timing for en_clk
TSADC_T_NON_OV	0x0208	W	0x00000002	Timong for non_ov
TSADC_T_HOLD	0x020C	W	0x00000013	Timing for hold
TSADC_Q_MAX	0x0210	W	0x00000000	Max data used for data inversion
TSADC_STATIC_CON	0x0214	W	0x0280001B	Static control signal
TSADC_CLK_CH_PERIOD	0x021C	W	0x0000012B	CLK_CH_TS period control
TSADC_T_PW_CLK	0x0220	W	0x00000030	Timing for pw_clk

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

24.4.3 Detail Registers Description

TSADC_USER_CON

Address: Operational Base(0xFFA70000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RO	0x0	adc_status 1'b0: ADC stop 1'b1: Conversion in progress
7	R/WSC	0x0	start When software write 1 to this bit, start-of-conversion will be assert. This bit will be cleared after TSADC access finishing. Only when TSADC_USER_CON[5] = 1'b1, this bit takes effect.
6	RW	0x0	eoc_inten Enable eoc interrupt for each conversion. 1'b1: Enable 1'b0: Disable
5	RW	0x0	start_mode Start mode. 1'b0: TSADC controller will assert start_of_conversion after power up. 1'b1: The start_of_conversion will be controlled by TSADC_USER_CON[7].
4	RW	0x0	power_control ADC power control 1'b0: power down 1'b1: power up This bit is not enable when TSADC_AUTO_CON[0] is set to 1.
3:0	RW	0x0	input_src_sel ADC input src sel in user mode. Can be changed from 0 - 6.

TSADC_AUTO_CON

Address: Operational Base(0xFFA70000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:9	RO	0x00	reserved
8	RW	0x0	tshut_polarity This bit is used to control the output signal polarity to gpio when the temperature is higher than threshold. 1'b0: Low active 1'b1: High active
7:3	RO	0x00	reserved
2	RW	0x0	round_int_en Int enable for round model. Used for auto model all channel set is sampled. 1'b1: Enable 1'b0: Disable
1	RW	0x0	q_sel 1'b0: Use tsadc_q as output (positive temperature coefficient) 1'b1: Use (q_max - tsadc_q) as output (negative temperature coefficient)
0	RW	0x0	auto_en Auto conversion enable 1'b0: TSADC controller works at user-define mode 1'b1: TSADC controller works at auto mode

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TSADC_AUTO_STATUS

Address: Operational Base(0xFFA70000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ht_wram High temperature status 1'b0: TSADC data is not higher than ht shut temperature 1'b1: TSADC data is higher than ht shut temperature
2	RW	0x0	auto_status TSADC auto mode status 1'b0: Auto mode stop 1'b1: Auto mode in progress
1	W0C	0x0	last_tshut_cru Status for cru reset latest tshut, write 1 to clear.
0	W1C	0x0	last_tshut_gpio Status for gpio latest tshut, write 1 to clear.

TSADC_AUTO_SRC

Address: Operational Base(0xFFA70000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	auto_src Enable channel for TSADC in auto mode. Each bit can enable for one channel form 0 - 6. *Only bit0 is valid, the other bits are reserved since only one temperature sensor is used in RK3562*

TSADC_LT_EN

Address: Operational Base(0xFFA70000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	low_temperature_vio_en Low temperature violation logic enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable *Only bit0 is valid, the other bits are reserved since only one temperature sensor is used in RK3562*

TSADC_HT_INT_EN

Address: Operational Base(0xFFA70000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	high_temperature_int_en Low temperature interrupt enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable *Only bit0 is valid, the other bits are reserved since only one temperature sensor is used in RK3562*

TSADC_GPIO_EN

Address: Operational Base(0xFFA70000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	gpio_en Temperature violation to gpio enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable *Only bit0 is valid, the other bits are reserved since only one temperature sensor is used in RK3562*

TSADC_CRU_EN

Address: Operational Base(0xFFA70000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	cru_en Temperature violation to cru reset enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable *Only bit0 is valid, the other bits are reserved since only one temperature sensor is used in RK3562*

TSADC_LT_INT_EN

Address: Operational Base(0xFFA70000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	low_tempeture_int_en Low temperature interrupt enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable *Only bit0 is valid, the other bits are reserved since only one temperature sensor is used in RK3562*

TSADC_HLT_INT_PD

Address: Operational Base(0xFFA70000) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:16	W1C	0x0000	lt_int_status Low temperature interrupt status for each channel. *Only bit16 is valid, the other bits are reserved since only one temperature sensor is used in RK3562*
15:0	W1C	0x0000	ht_int_status High temperature interrupt status for each channel. *Only bit0 is valid, the other bits are reserved since only one temperature sensor is used in RK3562*

TSADC_EOC_HSHUT_PD

Address: Operational Base(0xFFA70000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	W1C	0x0	round_int_pd Auto model interrupt for each round of all set channel.
16	W1C	0x0	usr_eoc_irq_pd User model end interrupt status.
15:0	W1C	0x0000	ht_shut_pd High temperature shut down status for each channel.

TSADC_DATA0

Address: Operational Base(0xFFA70000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	adc_data A/D value of the channel 0 last conversion.

TSADC_COMP0_INT

Address: Operational Base(0xFFA70000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP0_SHUT

Address: Operational Base(0xFFA70000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_HIGH_INT_DEBOUNCE

Address: Operational Base(0xFFA70000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_INT for "debounce" times.

TSADC_HIGH_TSHUT_DEBOUNCE

Address: Operational Base(0xFFA70000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_SHUT for "debounce" times.

TSADC_AUTO_PERIOD

Address: Operational Base(0xFFA70000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period When auto mode is enabled, this register controls the interleave between every conversion for all channel enabled of TSADC.

TSADC_AUTO_PERIOD_HT

Address: Operational Base(0xFFA70000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period This register controls the interleave between every conversion for all channel enabled of TSADC after the temperature is higher than COMP_SHUT or COMP_INT.

TSADC_COMP0_LOW_INT

Address: Operational Base(0xFFA70000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	tsadc_comp_src0 TSADC low temperature level. TSADC output is lower than tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_T_SETUP

Address: Operational Base(0xFFA70000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x005f	t_setup The timing between TSADC power up and start conversion.

TSADC_T_PW_EN

Address: Operational Base(0xFFA70000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	t_pw_en The timing assert start conversion signal(EN_TEMP_SEN_TS).

TSADC_T_EN_CLK

Address: Operational Base(0xFFA70000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x01	t_en_clk The timing between dis-assert start conversion signal (EN_TEMP_SEN_TS) and assert CLK_SEN_TS[8].

TSADC_T_NON_OV

Address: Operational Base(0xFFA70000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	t_non_ov The timing between each bit assertion of CLK_SENSE_TS.

TSADC_T_HOLD

Address: Operational Base(0xFFA70000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0013	t_hold The timing between dis-assert CLK_SENSE_TS and TSADC data valid.

TSADC_Q_MAX

Address: Operational Base(0xFFA70000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	q_max This register used for TSADC_AUTO_CON[1] for inverison output data.

TSADC_STATIC_CON

Address: Operational Base(0xFFA70000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	buf_vref_sel Offset control for tempetature output code.
26:23	RW	0x5	buf_slope_sel Slope control for temperature output code.
22:21	RW	0x0	comp_i_trim Comparator current timing ports.
20:17	RW	0x0	vbe_i_trm Current timing ports for VBE in PTAT generator.
16:13	RW	0x0	verf_trim Reference voltage trimming ports for reference gengrator.
12:9	RW	0x0	bgr_r_trim BGR control ports in reference generator.
8:5	RW	0x0	bgr_i_trim BJT emitter current control ports in reference generator.
4:2	RW	0x6	avg_mode Average mode control ports for digital filter.
1	RW	0x1	en_dem Dynamic element matching enable port.
0	RW	0x1	en_ch Digital offset cancellation enable port.

TSADC_CLK_CH_PERIOD

Address: Operational Base(0xFFA70000) + offset (0x021C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x0000012b	clk_ch_period Control the period of CLK_CH_TS.

TSADC_T_PW_CLK

Address: Operational Base(0xFFA70000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0030	t_pw_clk The timing for assertion of each bit of CLK_SENSE_TS.

24.5 Application Notes

24.5.1 Coversion Flow

The system works as follows

1) Temperature violation and other configurations may be set.
2) Assert tsadc_tsen_en and tsadc_ana_reg0, which could be found in VOGRF.
3) Set the bit[0] in register TSADC_AUTO_CON, then TS-ADC will work.
4) Then temperature information can be read from the APB interface.
5) If TS-ADC needs to be closed, set bit[0] in register TSADC_AUTO_CON to 1'b0.

24.5.2 Timing Diagram

When TS-ADC start to work, the timing is shown in the following figure.
The timing requirement is also listed as follows.

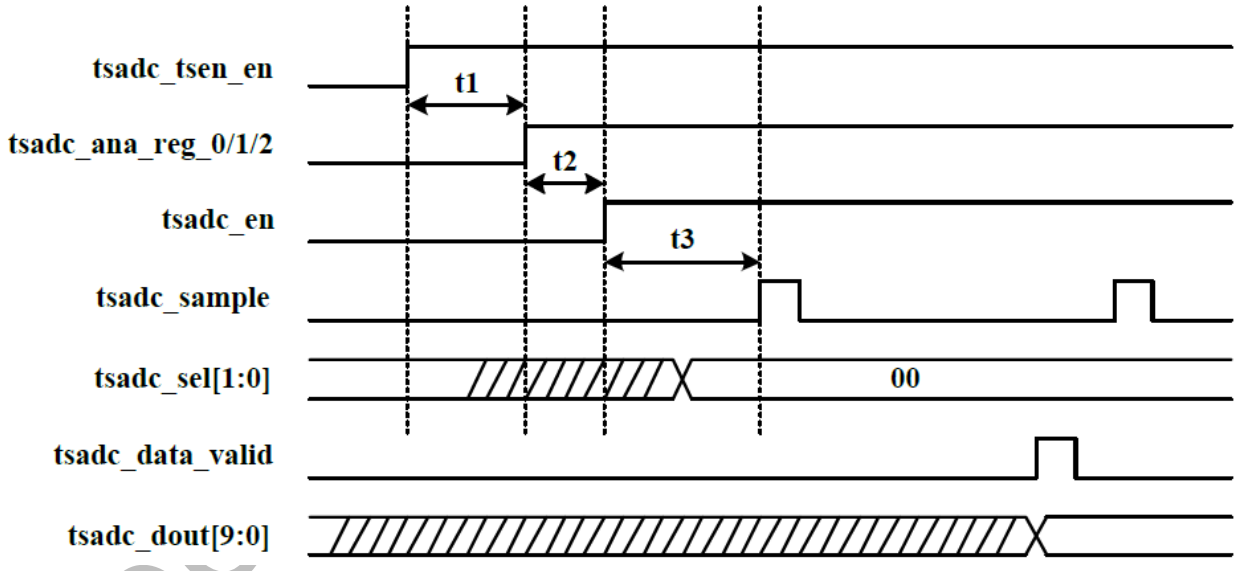

Fig. 24-2 Timing diagram for TS-ADC

Table 24-1 TS-ADC Start Timing

parameter	min
t1	10us
t2	0us
t3	90us

24.5.3 Temperature-to-Code Mapping

Table 24-2 TS-ADC Look up Table

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Temperature (℃)	Temperature Sensor Output		
	Min	Typ	Max
-40	-	2512	-
-35	-	2476	-
-30	-	2444	-
-25	-	2408	-
-20	-	2376	-
-15	-	2340	-
-10	-	2308	-
-5	-	2272	-
0	-	2240	-
5	-	2204	-
10	-	2172	-
15	-	2140	-
20	-	2104	-
25	-	2072	-
30	-	2036	-
35	-	2004	-
40	-	1968	-
45	-	1936	-
50	-	1900	-
55	-	1868	-
60	-	1832	-
65	-	1796	-
70	-	1764	-
75	-	1728	-
80	-	1696	-
85	-	1660	-
90	-	1628	-
95	-	1596	-
100	-	1560	-
105	-	1524	-
110	-	1492	-
115	-	1460	-

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Temperature (℃)	Temperature Sensor Output		
	Min	Typ	Max
120	-	1424	-
125	-	1392	-

Note: Code to Temperature mapping of the Temperature sensor is a linear curve. Any temperature, code falling between to 2 given temperatures can be linearly interpolated.
Code to Temperature mapping should be updated based on silicon results.

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Chapter 25 MIPI CSI HOST

25.1 Overview

The CSI-2 Host Controller is designed to receive data from a CSI-2 compliant camera sensor. A D-PHY configured as a Slave acts as the physical layer.
The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Specification for CSI-2, Version 1.01.00-9 November 2010
- Interface with MIPI D-PHY v1.2
- Up to four D-PHY RX data lanes.
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Several Frame formats
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data Type (Packet or Frame Level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- All primary and secondary data formats
  - RGB, YUV, and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
- Error detection and correction
  - PHY level
  - Packet level
  - Line level
  - Frame level
- Support DSI video mode/command mode
- Support reading back header.

25.2 Block Diagram

The following diagram shows the MIPI CSI-2 Host Controller architecture.

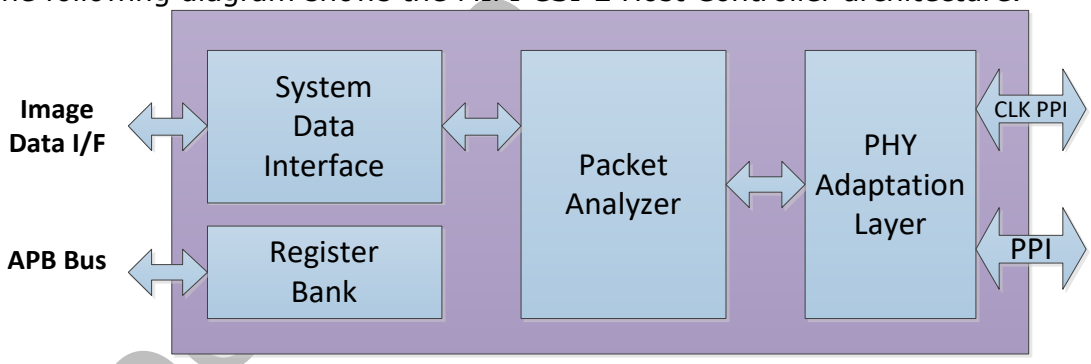

Fig. 25-1 MIPI CSI-2 Host Controller Architecture

- **PHY Adaptation Layer:** Manages the D-PHY PPI interface
- **Packet Analyzer:** Merges the data from the different lanes
- **Image Data Interface:** Reorders pixels into 32-bit data for memory storage and generates timing accurate video synchronization signals
- **AMBA-APB Register Bank:** Provides access to configuration and control registers

25.3 Function Description

25.3.1 Supported Resolutions and Frame Rates

The CSI-2 specification does not define the supported standard resolutions or frame rates. Camera sensor resolution, blanking periods, synchronization events, frame rates, and pixel color depth play a fundamental role in the required bandwidth. All these variables make it difficult to define a standard procedure to estimate the minimum lane rate and the minimum number of lanes that support a specific CSI-2 device.

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Following table presents some predefined and supported camera settings, assuming the following:

- Clock lane frequency is 500 MHz or 750 MHz that results in a bandwidth of 1 Gbps or 1.5 Gbps respectively, for each data lane.
- No significant control/reserved traffic is present on the link when pixel data is being transmitted.

The last column of following table presents the minimum number of lanes required for each configuration.

Table 25-1 Supported Camera Settings

Mega Pixels	Mega Pixels with Overhead	Refresh Rate (Hz)	Color Depth (bpp)	CSI2 BW (Mbits)	D-PHY at 1 Gbps Number of Lanes	D-PHY at 1.5Gbps Number of Lanes
2MP	2560000	15	24	922	1	1
2MP	2560000	30	24	1843	2	2
3MP	3840000	15	16	922	1	1
3MP	3840000	30	16	1843	2	2
3MP	3840000	30	24	2765	3	2
5MP	6400000	15	16	1536	2	2
5MP	6400000	15	24	2304	3	2
5MP	6400000	30	16	3072	4	3
8MP	10240000	15	16	2458	3	2
8MP	10240000	15	24	3686	4	3
8MP	10240000	30	12	3686	4	3
12MP	15360000	15	12	2765	3	2
12MP	15360000	15	16	3686	4	3
14MP	17920000	15	12	3226	4	3
16MP	20480000	15	12	3686	4	3
Video Formats						
1280x720 pixels(720p)	921600	30	24	664	1	1
1280x720 pixels(720p)	921600	60	24	1327	2	1
1920x1080 pixels(1080p)	2073600	60	24	2986	3	2

25.3.2 Error Detection

The CSI-2 Host Controller analyzes the received packets and determines if there are protocol errors. It is possible to monitor the following errors:

- Frame errors such as incorrect Frame sequence, reception of a CRC error in the most recent frame, and the mismatch between Frame Start and Frame End
- Line errors such as incorrect line sequence and mismatch between Line Start and Line End
- Packet errors such as ECC or CRC mismatch
- D-PHY errors such as synchronization pattern mismatch

Following table shows all the errors that CSI-2 Host Controller can identify.

Table 25-2 Errors Identified by the CSI-2 Host Controller

Error	Description	Level	Action
phy_errsotsynchs_*	Start of transmission error on data lane* with no synchronization achieved	PHY	Packets with this error are not delivered in IDI interface
phy_erresc_*	Escape entry error (ULPM) on data lane*	PHY	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

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Error	Description	Level	Action
phy_errsoths_*	Start of transmission error on data lane* but synchronization can still be achieved	PHY	Informative only since PHY can recover from this error. Error is acknowledged in register and the interrupt pin is raised.
phy_errcontrol_*	An incorrect line state sequence is detected on data lane*	PHY	Informative only. Error is acknowledged in the register and the interrupt pin is raised.
vc*_err_crc	Checksum error detected on virtual channel*	Packet	Informative only. Error is acknowledged in the register and Interrupt pin is raised.
vc*_err_crc	Header ECC contains one error detected on virtual channel*	Packet	Informative only since controller can recover the correct header. Error is acknowledged in the register and the interrupt pin is raised.
err_ecc_double	Header ECC contains two errors. Unrecoverable.	Packet	Packets with this error are not delivered in IDI.s
err_id_vc*	Unrecognized or unimplemented data type detected in virtual channel*	Packet	Informative only. Error is acknowledged in the register and the interrupt pin is raised
err_f_bndry_match_vc*	Error matching Frame Start with Frame End for virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_f_seq_vc*	Incorrect Frame Sequence detected in virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_frame_data_vc*	Last received frame, in virtual channel*, had at least one CRC error	Frame	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

25.4 Register Description

25.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
CSI2HOST0	0xFF380000
CSI2HOST1	0xFF390000
CSI2HOST2	0xFF3A0000
CSI2HOST3	0xFF3B0000

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25.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CSI2HOST_VERSION	0x0000	W	0x00000000	Controller version identification
CSI2HOST_N_LANES	0x0004	W	0x00000000	Number of active data lanes
CSI2HOST_CSI2_RESETN	0x0010	W	0x00000000	CSI2 controller reset
CSI2HOST_PHY_STATE	0x0014	W	0x00000000	General settings for all blocks
CSI2HOST_ERR1	0x0020	W	0x00000000	Error state register 1
CSI2HOST_ERR2	0x0024	W	0x00000000	Error state register 2
CSI2HOST_MSK1	0x0028	W	0x00000000	Masks for errors 1
CSI2HOST_MSK2	0x002C	W	0x00000000	Masks for errors 2
CSI2HOST_CONTROL	0x0040	W	0x0C204000	Control
CSI2HOST_HEADER_0	0x0050	W	0x00000000	Header 0
CSI2HOST_HEADER_1	0x0054	W	0x00000000	Header 1
CSI2HOST_HEADER_2	0x0058	W	0x00000000	Header 2
CSI2HOST_HEADER_3	0x005C	W	0x00000000	Header 3

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

25.4.3 Detail Registers Description

CSI2HOST_VERSION

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	version Version of the csi2host.

CSI2HOST_N_LANES

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	n_lanes Number of active data lanes. 2'b00: 1 data lane(lane 0) 2'b01: 2 data lanes(lane0 and 1) 2'b10: 3 data lanes(lane0,1,and 2) 2'b11: 4 data lanes(ALL) Can only be updated when the D-PHY lane is in the Stop state.

CSI2HOST_CSI2_RESETN

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	csi2_resetn CSI2 controller reset output. Active low.

CSI2HOST_PHY_STATE

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	bypass_2ecc_tst Payload Bypass test mode for double ECC errors.
30:15	RO	0x0000	reserved
14	RO	0x0	phy_rxactivehs_3 Lane3 high-speed receive active. Active high.

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Bit	Attr	Reset Value	Description
13	RO	0x0	phy_rxactivehs_2 Lane2 high-speed receive active. Active high.
12	RO	0x0	phy_rxactivehs_1 Lane1 high-speed receive active. Active high.
11	RO	0x0	phy_rxactivehs_0 Lane0 high-speed receive active. Active high.
10	RO	0x0	phy_stopstateclk Clock lane in Stop state.
9	RO	0x0	phy_rxulpsclknot This signal indicates that the clock lane module has entered the Ultra Low Power state. Active low.
8	RO	0x0	phy_rxclkactivehs Indicates that the clock lane is actively receiving a DDR clock.
7	RO	0x0	phy_stopstatedata_3 Data lane 3 in Stop state.
6	RO	0x0	phy_stopstatedata_2 Data lane 2 in Stop state.
5	RO	0x0	phy_stopstatedata_1 Data lane 1 in Stop state.
4	RO	0x0	phy_stopstatedata_0 Data lane 0 in Stop state.
3	RO	0x0	phy_rxulpsesc_3 Lane module0 has entered the Ultra Low Power mode.
2	RO	0x0	phy_rxulpsesc_2 Lane module2 has entered the Ultra Low Power mode.
1	RO	0x0	phy_rxulpsesc_1 Lane module1 has entered the Ultra Low Power mode.
0	RO	0x0	phy_rxulpsesc_0 Lane module0 has entered the Ultra Low Power mode.

CSI2HOST_ERR1

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	err_ph_crc_lane2 Packet crc error of lane2 when sw_cphy_en=1.
30	RW	0x0	err_ph_crc_lane1 Packet crc error of lane1 when sw_cphy_en=1.
29	RW	0x0	err_ph_crc_lane0 Packet crc error of lane0 when sw_cphy_en=1.
28	RO	0x0	err_ecc_double Header ECC contains 2 errors, unrecoverable.
27	RO	0x0	vc3_err_crc Checksum error detected on virtual channel 3.
26	RO	0x0	vc2_err_crc Checksum error detected on virtual channel 2.
25	RO	0x0	vc1_err_crc Checksum error detected on virtual channel 1.
24	RO	0x0	vc0_err_crc Checksum error detected on virtual channel 0.
23:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15	RO	0x0	err_frame_data_vc3 Last received frame, in virtual channel 3, had at least one CRC error.
14	RO	0x0	err_frame_data_vc2 Last received frame, in virtual channel 2, had at least one CRC error.
13	RO	0x0	err_frame_data_vc1 Last received frame, in virtual channel 1, had at least one CRC error.
12	RO	0x0	err_frame_data_vc0 Last received frame, in virtual channel 0, had at least one CRC error.
11	RO	0x0	err_f_seq_vc3 Incorrect frame sequence detected in virtual channel 3.
10	RO	0x0	err_f_seq_vc2 Incorrect frame sequence detected in virtual channel 2.
9	RO	0x0	err_f_seq_vc1 Incorrect frame sequence detected in virtual channel 1.
8	RO	0x0	err_f_seq_vc0 Incorrect frame sequence detected in virtual channel 0.
7	RO	0x0	err_f_bndry_match_vc3 Error matching frame start with frame end for virtual channel 3.
6	RO	0x0	err_f_bndry_match_vc2 Error matching frame start with frame end for virtual channel 2.
5	RO	0x0	err_f_bndry_match_vc1 Error matching frame start with frame end for virtual channel 1.
4	RO	0x0	err_f_bndry_match_vc0 Error matching frame start with frame end for virtual channel 0.
3	RO	0x0	phy_errsotsynchs_3 Start of transmission error on data lane 3.
2	RO	0x0	phy_errsotsynchs_2 Start of transmission error on data lane 2.
1	RO	0x0	phy_errsotsynchs_1 Start of transmission error on data lane 1.
0	RO	0x0	phy_errsotsynchs_0 Start of transmission error on data lane 0(no synchronization achieved).

CSI2HOST_ERR2

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	fifo_overflow FIFO overflow in adapter.
27	RW	0x0	cphy_errcodehs_3 Lane 3 receive invalid code whensw_cphy_en=1.
26	RW	0x0	cphy_errcodehs_2 Lane 2 receive invalid code whensw_cphy_en=1.
25	RW	0x0	cphy_errcodehs_1 Lane 1 receive invalid code whensw_cphy_en=1.
24	RW	0x0	cphy_errcodehs_0 Lane 0 receive invalid code whensw_cphy_en=1.
23:20	RO	0x0	reserved
19	RW	0x0	phy_errcontrol_3 Control error on data lane 3.

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Bit	Attr	Reset Value	Description
18	RW	0x0	phy_errcontrol_2 Control error on data lane 2.
17	RW	0x0	phy_errcontrol_1 Control error on data lane 1.
16	RW	0x0	phy_errcontrol_0 Control error on data lane 0.
15	RW	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3.
14	RW	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2.
13	RW	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1.
12	RW	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0.
11	RW	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3.
10	RW	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2.
9	RW	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1.
8	RW	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0.
7	RW	0x0	phy_errsoths_3 Start of transmission error on data lane 3(synchronization can still be achieved).
6	RW	0x0	phy_errsoths_2 Start of transmission error on data lane 2(synchronization can still be achieved).
5	RW	0x0	phy_errsoths_1 Start of transmission error on data lane 1(synchronization can still be achieved).
4	RW	0x0	phy_errsoths_0 Start of transmission error on data lane 0(synchronization can still be achieved).
3	RW	0x0	phy_erresc_3 Escape entry error(ULPM) on data lane 3.
2	RW	0x0	phy_erresc_2 Escape entry error(ULPM) on data lane 2.
1	RW	0x0	phy_erresc_1 Escape entry error(ULPM) on data lane 1.
0	RW	0x0	phy_erresc_0 Escape entry error(ULPM) on data lane 0.

CSI2HOST_MSK1

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31	RW	0x0	mask_err_ph_crc_lane2 Mask for err_ph_crc_lane2.
30	RW	0x0	mask_err_ph_crc_lane1 Mask for err_ph_crc_lane1.

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Bit	Attr	Reset Value	Description
29	RW	0x0	mask_err_ph_crc_lane0 Mask for err_ph_crc_lane0.
28	RW	0x0	mask_err_ecc_double Mask for err_ecc_double.
27	RW	0x0	mask_vc3_err_crc Mask for vc3_err_crc.
26	RW	0x0	mask_vc2_err_crc Mask for vc2_err_crc.
25	RW	0x0	mask_vc1_err_crc Mask for vc1_err_crc.
24	RW	0x0	mask_vc0_err_crc Mask for vc0_err_crc.
23:16	RO	0x00	reserved
15	RW	0x0	mask_err_frame_data_vc3 Mask for err_frame_data_vc3.
14	RW	0x0	mask_err_frame_data_vc2 Mask for err_frame_data_vc2.
13	RW	0x0	mask_err_frame_data_vc1 Mask for err_frame_data_vc1.
12	RW	0x0	mask_err_frame_data_vc0 Mask for err_frame_data_vc0.
11	RW	0x0	mask_err_f_seq_vc3 Mask for err_f_seq_vc3.
10	RW	0x0	mask_err_f_seq_vc2 Mask for err_f_seq_vc2.
9	RW	0x0	mask_err_f_seq_vc1 Mask for err_f_seq_vc1.
8	RW	0x0	mask_err_f_seq_vc0 Mask for err_f_seq_vc0.
7	RW	0x0	mask_err_f_bndry_match_vc3 Mask for err_f_bndry_match_vc3.
6	RW	0x0	mask_err_f_bndry_match_vc2 Mask for err_f_bndry_match_vc2.
5	RW	0x0	mask_err_f_bndry_match_vc1 Mask for err_f_bndry_match_vc1.
4	RW	0x0	mask_err_f_bndry_match_vc0 Mask for err_f_bndry_match_vc0.
3	RW	0x0	mask_phy_errsotsynchs_3 Mask for phy_errsotsynchs_3.
2	RW	0x0	mask_phy_errsotsynchs_2 Mask for phy_errsotsynchs_2.
1	RW	0x0	mask_phy_errsotsynchs_1 Mask for phy_errsotsynchs_1.
0	RW	0x0	mask_phy_errsotsynchs_0 Mask for phy_errsotsynchs_0.

CSI2HOST_MSK2

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	mask_fifo_overflow Mask for fifo overflow.
27	RW	0x0	mask_phy_errcodehs_3 Mask for phy_errcodehs_3.

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Bit	Attr	Reset Value	Description
26	RW	0x0	mask_phy_errcodehs_2 Mask for phy_errcodehs_2.
25	RW	0x0	mask_phy_errcodehs_1 Mask for phy_errcodehs_1.
24	RW	0x0	mask_phy_errcodehs_0 Mask for phy_errcodehs_0.
23:20	RO	0x0	reserved
19	RW	0x0	mask_phy_errcontrol_3 Mask for phy_errcontrol_3.
18	RW	0x0	mask_phy_errcontrol_2 Mask for phy_errcontrol_2.
17	RW	0x0	mask_phy_errcontrol_1 Mask for phy_errcontrol_1.
16	RW	0x0	mask_phy_errcontrol_0 Mask for phy_errcontrol_0.
15	RW	0x0	mask_err_id_vc3 Mask for err_id_vc3.
14	RW	0x0	mask_err_id_vc2 Mask for err_id_vc2.
13	RW	0x0	mask_err_id_vc1 Mask for err_id_vc1.
12	RW	0x0	mask_err_id_vc0 Mask for err_id_vc0.
11	RW	0x0	mask_vc3_err_ecc_corrected Mask for vc3_err_ecc_corrected.
10	RW	0x0	mask_vc2_err_ecc_corrected Mask for vc2_err_ecc_corrected.
9	RW	0x0	mask_vc1_err_ecc_corrected Mask for vc1_err_ecc_corrected.
8	RW	0x0	mask_vc0_err_ecc_corrected Mask for vc0_err_ecc_corrected.
7	RW	0x0	mask_phy_errsoths_3 Mask for phy_errsoths_3.
6	RW	0x0	mask_phy_errsoths_2 Mask for phy_errsoths_2.
5	RW	0x0	mask_phy_errsoths_1 Mask for phy_errsoths_1
4	RW	0x0	mask_phy_errsoths_0 Mask for phy_errsoths_0.
3	RW	0x0	mask_phy_erresc_3 Mask for phy_erresc_3.
2	RW	0x0	mask_phy_erresc_2 Mask for phy_erresc_2.
1	RW	0x0	mask_phy_erresc_1 Mask for phy_erresc_1.
0	RW	0x0	mask_phy_erresc_0 Mask for phy_erresc_0.

CSI2HOST_CONTROL

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RW	0x03	sw_datatype_le The datatype of line end.
25:20	RW	0x02	sw_datatype_ls The datatype of line start.

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Bit	Attr	Reset Value	Description
19:14	RW	0x01	sw_datatype_fe The datatype of frame end.
13:8	RW	0x00	sw_datatype_fs The datatype of frame start.
7:6	RO	0x0	reserved
5	RW	0x0	sw_adapter_mux 1'b0: New rtl code for dphy adapter 1'b1: Old rtl code for dphy adapter
4	RW	0x0	sw_dsi_en 1'b0: For csi2 1'b1: For dsi
3:1	RO	0x0	reserved
0	RW	0x0	sw_cphy_en 1'b0: For dphy 1'b1: For cphy

CSI2HOST_HEADER_0

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_header_0 32bit header {2'd0,ecc,word_count,vc,data_type} ro_header_0 is latest and ro_header_3 is earliest.

CSI2HOST_HEADER_1

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_header_1 32bit header {2'd0,ecc,word_count,vc,data_type}

CSI2HOST_HEADER_2

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_header_2 32bit header {2'd0,ecc,word_count,vc,data_type}

CSI2HOST_HEADER_3

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_header_3 32bit header {2'd0,ecc,word_count,vc,data_type}

25.5 Application Notes

- The most important step is configuring the right CSI2HOST_N_LANES before pulling up csi_resetn. If the host is used to receive DSI data, the sw_dsi_en must be enabled, and the sw_datatype_fs, sw_datatype_fe, sw_datatype_ls, sw_datatype_le must be configured correctly. When the sw_dsi_en is enabled, those debug or error detection registers are useless.
- There are four MIPI CSI HOST in RK3562 SOC, CSI HOST0/1 are connectted to MIPI DPHY0. When the MIPI DPHY0 works in 4 lanes mode, only CSI HOST0 works. And when the MIPI DPHY0 works in 2x2lanes mode, CSI HOST0 is connected to 0/1 lane, CSI HOST1 is connected to 2/3 lane. CSI HOST2/3 are connected to MIPI DPHY1, When the MIPI DPHY1 works in 4 lanes mode, only CSI HOST2 works. And when the MIPI DPHY1 works in 2x2lanes mode, CSI HOST2 is connected to 0/1 lane, CSI HOST3 is connected to 2/3 lane.

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Chapter 26 MIPI CSI DPHY

26.1 Overview

The features of MIPI CSI DPHY are as follow:

- Analog mixed-signal hard-macro LP/HS Receiver solution
- Designed to MIPI v1.2 Specifications
- Integrated PHY Protocol Interface(PPI) interfaces to DSI/CSI and UniPro MIPI protocols
- 2.5 Gbps maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 10 Gbps transfer rate
- HS-RX, LP-RX, LP-TX and Calibration supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- LOW-Power dissipation: less than 1.5mA/Lane in D-PHY HS RX mode
- Buffers with tunable On-Die-Termination
- Includes embedded ESD, boundary scan and BIST
- Dual clock lanes mode supported

26.2 Block Diagram

MIPI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Figure below shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all Lane types. The requirements for the 'Control and Interface Logic'(CIL) function depend on the Lane type and Lane side.

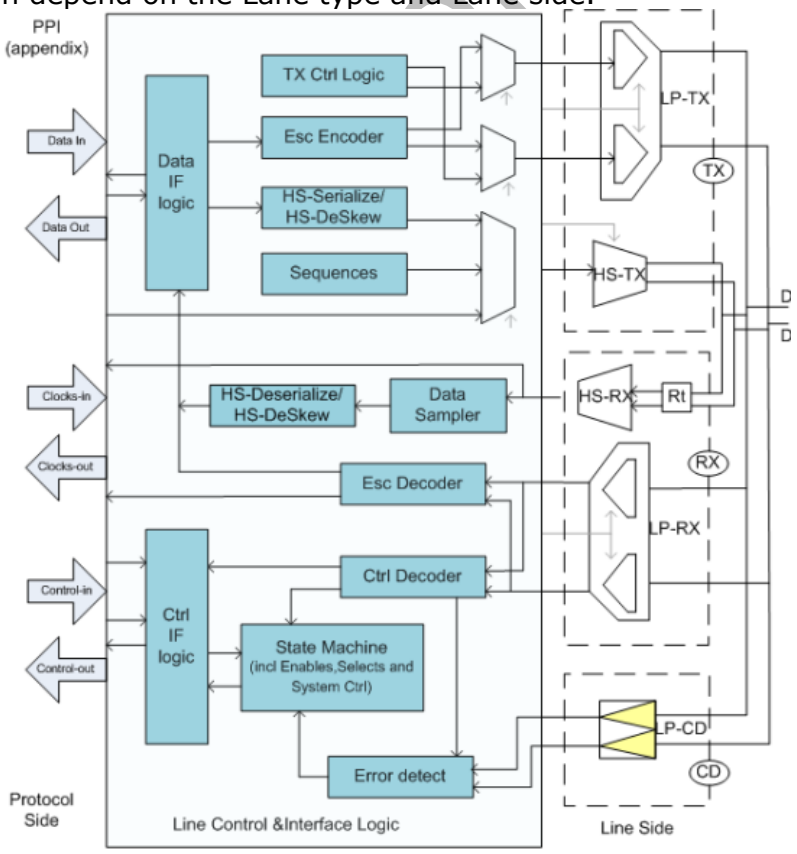

Fig. 26-1 MIPI CSI DPHY Block Diagram

26.3 Register Description

26.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as

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follows.

Operational Base

Name	Base Address
CSI_DPHY0	0xFF3C0000
CSI_DPHY1	0xFF3D0000

26.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CSI_DPHY_LANE_EN	0x0000	W	0x00000000	Clk/data lane enable
CSI_DPHY_DIGITAL_CLK_PHASE	0x0034	W	0x00000000	Digital clock phase
CSI_DPHY_LANE_CLK_3_PHASE	0x0038	W	0x00000000	Lane clock/3 phase
CSI_DPHY_LANE_2_1_0_PHASE	0x003C	W	0x00000000	Data lane 2/1/0 phase
CSI_DPHY_DIGITAL_CLK_REVERSE	0x0048	W	0x00000000	Digital clock reverse
CSI_DPHY_DUAL_CLK_ENABLE	0x0080	W	0x00000001	MIPI/LVDS enable
CSI_DPHY_LANE_CK_MODE	0x0128	W	0x00000000	Clock lane mode
CSI_DPHY_LANE_CK_MSB	0x0138	W	0x00000000	MSB enable
CSI_DPHY_LANE_CK_TTAGO	0x0140	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_CK_TTASURE	0x0144	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_CK_TTAWAIT	0x0148	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_CK_THSSETTLE	0x0160	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_CK_CAL_EN	0x0168	W	0x00000000	Calibration reception enable
CSI_DPHY_LANE_0_MSB	0x01B8	W	0x00000000	MSB enable
CSI_DPHY_LANE_0_TTAGO	0x01C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_0_TTASURE	0x01C4	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_0_TTAWAIT	0x01C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_0_THSSETTLE	0x01E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_0_CAL_EN	0x01E8	W	0x00000000	Calibration reception enable
CSI_DPHY_LANE_1_MSB	0x0238	W	0x00000000	MSB enable
CSI_DPHY_LANE_1_TTAGO	0x0240	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_1_TTASURE	0x0244	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_1_TTAWAIT	0x0248	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_1_THSSETTLE	0x0260	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_1_CAL_EN	0x0268	W	0x00000000	Calibration reception enable
CSI_DPHY_LANE_2_MSB	0x02B8	W	0x00000000	MSB enable

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Name	Offset	Size	Reset Value	Description
CSI_DPHY_LANE_2_TTAGO	0x02C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_2_TTASURE	0x02C4	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_2_TTAWAIT	0x02C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_2_THSSETTLE	0x02E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_2_CAL_EN	0x02E8	W	0x00000000	Calibration reception enable
CSI_DPHY_LANE_3_MSB	0x0338	W	0x00000000	MSB enable
CSI_DPHY_LANE_3_TTAGO	0x0340	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_3_TTASURE	0x0344	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_3_TTAWAIT	0x0348	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_3_THSSETTLE	0x0360	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_3_CAL_EN	0x0368	W	0x00000000	Calibration reception enable
CSI_DPHY_LANE_CK1_MODE	0x03A8	W	0x00000000	Clock lane1 mode
CSI_DPHY_LANE_CK1_MSB	0x03B8	W	0x00000000	MSB enable
CSI_DPHY_LANE_CK1_TTAGO	0x03C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_CK1_TTASURE	0x03C4	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_CK1_TTAWAIT	0x03C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_CK1_THSSETTLE	0x03E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_CK1_CAL_EN	0x03E8	W	0x00000000	Calibration reception enable

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.3.3 Detail Registers Description

CSI_DPHY_LANE_EN

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_en_ck Enable D-PHY clock lane:active high.
5	RW	0x0	lane_en_3 Enable D-PHY lane3:active high.
4	RW	0x0	lane_en_2 Enable D-PHY lane2:active high.
3	RW	0x0	lane_en_1 Enable D-PHY lane1:active high.
2	RW	0x0	lane_en_0 Enable D-PHY lane0:active high.
1:0	RO	0x0	reserved

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CSI_DPHY_DIGITAL_CLK_PHASE

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	digital_clk_phase 3'b000: Phase 0(default value) 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

CSI_DPHY_LANE_CLK_3_PHASE

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	lane_clk_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
3:1	RW	0x0	lane_3_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
0	RW	0x0	lane_2_phase_msb See lane_2_phase for the details of the register.

CSI_DPHY_LANE_2_1_0_PHASE

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	lane_2_phase {lane_2_phase_msb,lane_2_phase} 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
5:3	RW	0x0	lane_1_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
2:0	RW	0x0	lane_0_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

CSI_DPHY_DIGITAL_CLK_REVERSE

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	digital_clk_reverse 1'b0: Make the digital sample clock positive(default value) 1'b1: Reverse the digital sample clock
6:0	RO	0x00	reserved

CSI_DPHY_DUAL_CLK_ENABLE

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	dual_clk_mode_en 1'b0: Enable single clock lane mode 1'b1: Enable dual clock lanes mode
5:1	RO	0x00	reserved
0	RW	0x1	reg_dig_rstn 1'b0: Reset 1'b1: Normal

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CSI_DPHY_LANE_CK_MODE

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode
3:0	RO	0x0	reserved

CSI_DPHY_LANE_CK_MSB

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_ck_msb MSB enable for pin_rxdatahs_* 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

CSI_DPHY_LANE_CK_TTAGO

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_CK_TTASURE

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_CK_TTAWAIT

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_CK_THSSETTLE

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_ck_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110Mbps 02 110-150Mbps 03 150-200Mbps 06 200-250Mbps 06 250-300Mbps 06 300-400Mbps 08 400-500Mbps 0b 500-600Mbps 0e 600-700Mbps 10 700-800Mbps 12 800-1000Mbps 16 1000-1200Mbps 1e 1200-1400Mbps 23 1400-1600Mbps 2d 1600-1800Mbps 32 1800-2000Mbps 37 2000-2200Mbps 3c 2200-2400Mbps 41 2400-2500Mbps 46

CSI_DPHY_LANE_CK_CAL_EN

Address: **Operational Base** + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

CSI_DPHY_LANE_0_MSB

Address: **Operational Base** + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_0_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

CSI_DPHY_LANE_0_TTAGO

Address: **Operational Base** + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_0_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_0_TTASURE

Address: **Operational Base** + offset (0x01C4)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_0_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_0_TTAWAIT

Address: **Operational Base** + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_0_THSSETTLE

Address: **Operational Base** + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_0_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110Mbps 02 110-150Mbps 03 150-200Mbps 06 200-250Mbps 06 250-300Mbps 06 300-400Mbps 08 400-500Mbps 0b 500-600Mbps 0e 600-700Mbps 10 700-800Mbps 12 800-1000Mbps 16 1000-1200Mbps 1e 1200-1400Mbps 23 1400-1600Mbps 2d 1600-1800Mbps 32 1800-2000Mbps 37 2000-2200Mbps 3c 2200-2400Mbps 41 2400-2500Mbps 46

CSI_DPHY_LANE_0_CAL_EN

Address: **Operational Base** + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_0_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

CSI_DPHY_LANE_1_MSB

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Address: **Operational Base** + offset (0x0238)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_1_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

CSI_DPHY_LANE_1_TTAGO

Address: **Operational Base** + offset (0x0240)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_1_TTASURE

Address: **Operational Base** + offset (0x0244)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_1_TTAWAIT

Address: **Operational Base** + offset (0x0248)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_1_THSSETTLE

Address: **Operational Base** + offset (0x0260)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110Mbps 02 110-150Mbps 03 150-200Mbps 06 200-250Mbps 06 250-300Mbps 06 300-400Mbps 08 400-500Mbps 0b 500-600Mbps 0e 600-700Mbps 10 700-800Mbps 12 800-1000Mbps 16 1000-1200Mbps 1e 1200-1400Mbps 23 1400-1600Mbps 2d 1600-1800Mbps 32 1800-2000Mbps 37 2000-2200Mbps 3c 2200-2400Mbps 41 2400-2500Mbps 46

CSI_DPHY_LANE_1_CAL_EN

Address: **Operational Base** + offset (0x0268)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

CSI_DPHY_LANE_2_MSB

Address: **Operational Base** + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_2_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

CSI_DPHY_LANE_2_TTAGO

Address: **Operational Base** + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_2_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_2_TTASURE

Address: **Operational Base** + offset (0x02C4)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_2_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_2_TTAWAIT

Address: **Operational Base** + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_2_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_2_THSSETTLE

Address: **Operational Base** + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_2_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110Mbps 02 110-150Mbps 03 150-200Mbps 06 200-250Mbps 06 250-300Mbps 06 300-400Mbps 08 400-500Mbps 0b 500-600Mbps 0e 600-700Mbps 10 700-800Mbps 12 800-1000Mbps 16 1000-1200Mbps 1e 1200-1400Mbps 23 1400-1600Mbps 2d 1600-1800Mbps 32 1800-2000Mbps 37 2000-2200Mbps 3c 2200-2400Mbps 41 2400-2500Mbps 46

CSI_DPHY_LANE_2_CAL_EN

Address: **Operational Base** + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_2_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

CSI_DPHY_LANE_3_MSB

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Address: **Operational Base** + offset (0x0338)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_3_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

CSI_DPHY_LANE_3_TTAGO

Address: **Operational Base** + offset (0x0340)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_3_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_3_TTASURE

Address: **Operational Base** + offset (0x0344)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_3_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_3_TTAWAIT

Address: **Operational Base** + offset (0x0348)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_3_THSSETTLE

Address: **Operational Base** + offset (0x0360)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_3_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110Mbps 02 110-150Mbps 03 150-200Mbps 06 200-250Mbps 06 250-300Mbps 06 300-400Mbps 08 400-500Mbps 0b 500-600Mbps 0e 600-700Mbps 10 700-800Mbps 12 800-1000Mbps 16 1000-1200Mbps 1e

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Bit	Attr	Reset Value	Description
			1200-1400Mbps 23 1400-1600Mbps 2d 1600-1800Mbps 32 1800-2000Mbps 37 2000-2200Mbps 3c 2200-2400Mbps 41 2400-2500Mbps 46

CSI_DPHY_LANE_3_CAL_EN

Address: **Operational Base** + offset (0x0368)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_3_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

CSI_DPHY_LANE_CK1_MODE

Address: **Operational Base** + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck1_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode
3:0	RO	0x0	reserved

CSI_DPHY_LANE_CK1_MSB

Address: **Operational Base** + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_ck1_msb MSB enable for pin_rxdatahs_* 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

CSI_DPHY_LANE_CK1_TTAGO

Address: **Operational Base** + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_CK1_TTASURE

Address: **Operational Base** + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_CK1_TTAWAIT

Address: **Operational Base** + offset (0x03C8)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_CK1_THSSETTLE

Address: **Operational Base** + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_ck1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110Mbps 02 110-150Mbps 03 150-200Mbps 06 200-250Mbps 06 250-300Mbps 06 300-400Mbps 08 400-500Mbps 0b 500-600Mbps 0e 600-700Mbps 10 700-800Mbps 12 800-1000Mbps 16 1000-1200Mbps 1e 1200-1400Mbps 23 1400-1600Mbps 2d 1600-1800Mbps 32 1800-2000Mbps 37 2000-2200Mbps 3c 2200-2400Mbps 41 2400-2500Mbps 46

CSI_DPHY_LANE_CK1_CAL_EN

Address: **Operational Base** + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

26.4 Application Notes

26.4.1 MIPI DPHY0 SINGLE CLOCK LANE Mode Application

step1: send 0x7d to register LANE_EN. Enable the D-PHY.
step2: send 0x01f001f0 to register GRF_VI_CON0. Enable the clock lane and 4 data lanes.
step3: According to data rate, write corresponding value to Ths-settle registers for lanes.

26.4.2 MIPI DPHY0 DUAL CLOCK LANES MODE Application

step1: send 0x7d to register LANE_EN. Enable the D-PHY.
step2: send 0x5f to register DUAL_CLK_ENABLE.Enable dual clock lanes mode.
step3: send 0x15f015f0 to register GRF_VI_CON0. Enable 2 clock lanes/4 data lanes and

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2x2lane mode.
step4: According to data rate, write corresponding value to Ths-settle registers for lanes.

26.4.3 MIPI DPHY1 SINGLE CLOCK LANE Mode Application

step1: send 0x7d to register LANE_EN. Enable the D-PHY.
step2: send 0x01f001f0 to register GRF_VI_CON1. Enable the clock lane and 4 data lanes.
step3: According to data rate, write corresponding value to Ths-settle registers for lanes.

26.4.4 MIPI DPHY1 DUAL CLOCK LANES MODE Application

step1: send 0x7d to register LANE_EN. Enable the D-PHY.
step2: send 0x5f to register DUAL_CLK_ENABLE.Enable dual clock lanes mode.
step3: send 0x05f005f0 to register GRF_VI_CON1. Enable 2 clock lanes/4 data lanes. send 0x20002000 to register GRF_VI_CON0. Enable 2x2lane mode.
step4: According to data rate, write corresponding value to Ths-settle registers for lanes.

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Chapter 27 MIPI DSI HOST Controller

27.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI HOST Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI HOST Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI DSI HOST Controller supports one to four lanes for data transmission with MIPI D-PHY.

The MIPI DSI HOST Controller supports the following features:

- The MIPI DSI HOST Controller conforms to the following standards
  - MIPI Alliance Specification for DSI v1.1
  - MIPI Alliance Specification for DCS v1.1
  - MIPI Alliance Standard for DPI-2
  - MIPI Alliance Specification for SDF v1.0
  - MIPI Alliance Specification for DPHY v1.2
  - AMBA 2.0 Specification(APB) from ARM
- Support the DPI interface color coding mappings into 24-bit Interface
  - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Maximum resolution is 1920x1080@60Hz
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands
- ECC and Checksum capabilities
- End of Transmission Packet(EOTp)
- Ultra Low-Power mode
- Fault recovery schemes

27.2 Block Diagram

The following diagram shows the MIPI DSI HOST Controller architecture.

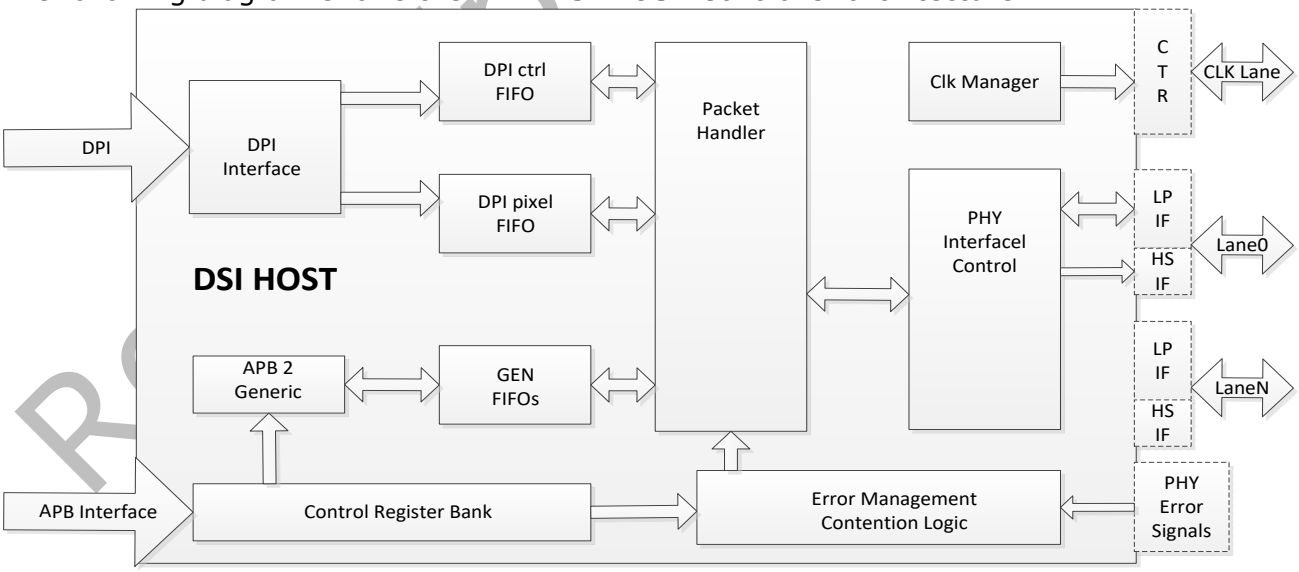

Fig. 27-1 MIPI DSI HOST Controller architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video control signals and another one for pixel data. This data is then used to build Video packets, hen in Video mode.

The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI DSI HOST Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.

The PHY Interface Control is responsible for managing the D-PHY PPI interface. It

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acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.
The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.
The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFO: Command FIFO, Write payload FIFO, Read payload FIFO.
The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

27.3 Function Description

27.3.1 DPI interface function

The DPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands, which are triggered directly by writing to the register of VO_CON[9:8] in the GRF Module. To transfer additional commands(for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.
The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpipixdata bus. The following table shows the Interface pixel color coding.

Table 27-1 Color table

Signal Line	24bit
Config	Config1
Dpidata23	R7
Dpidata22	R6
Dpidata21	R5
Dpidata20	R4
Dpidata19	R3
Dpidata18	R2
Dpidata17	R1
Dpidata16	R0
Dpidata15	G7
Dpidata14	G6
Dpidata13	G5
Dpidata12	G4
Dpidata11	G3
Dpidata10	G2
Dpidata9	G1
Dpidata8	G0
Dpidata7	B7
Dpidata6	B6
Dpidata5	B5
Dpidata4	B4
Dpidata3	B3

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Signal Line	24bit
Config	Config1
Dpidata2	B2
Dpidata1	B1
Dpidata0	B0

The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows: Polarity control: All the control signals are programmable to change the polarity depending on system requirements.
After the MIPI DSI HOST Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame.
If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the configuration are always inferred as zero. The specification states that in this mode, the pixel line size should be a multiple of four.

27.3.2 APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.
The MIPI DSI HOST Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN_PLD_DATA register has two distinct functions based on the operation. Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN_HDR register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN_PLD_DATA register.
The valid packets available to be transmitted through the Generic interface are as follows:

- Generic Write Short Packet 0 Parameters
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Generic Write Short Packet 0 Parameter
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Maximum Read Packet Configuration
- Generic Long Write Packet
- DCS Write Short Packet 0 Parameter
- DCS Write Short Packet 1 Parameter
- DCS Write Short Packet 0 Parameter
- DCS Write Long Packet

A set of bits in the CMD_PKT_STATUS register report the status of the FIFOs associated with APB interface support.
Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these mode is selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.
The transfer of packets through the APB bus is based on the following conditions:
The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.
The data input bus has a maximum width of 32 bits. This allows for a relation to be defined between the input APB clock frequency and maximum bi rate achievable by the APB

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interface.
The DSI link bit rate when using solely APB is equal to (APB clock frequency) *16 Mbps. The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.
To drive the APB interface to achieve high bandwidth Command mode traffic transported by the DSI link, the MIPI DSI HOST Controller should operate in the Command mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does not share it with any another input interface source.
The memory write commands require maximum throughout from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN_PLD_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least significant byte position of the APB data bus. After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figure show how the pixel data should be organized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams. In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

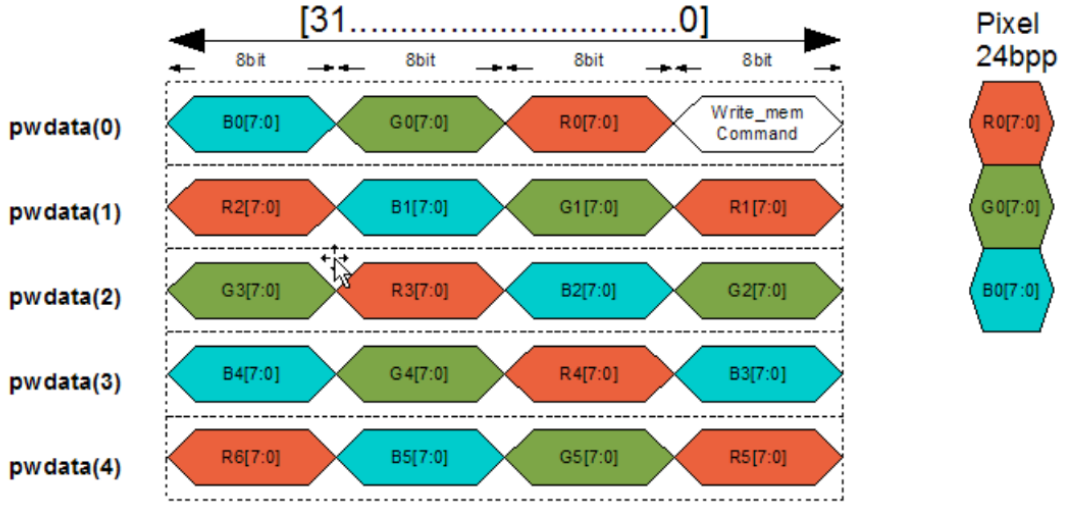

Fig 27-2 24 bpp APB Pixel to Byte Organization

27.3.3 Transmission of Commands in Video Mode

The MIPI DSI HOST Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

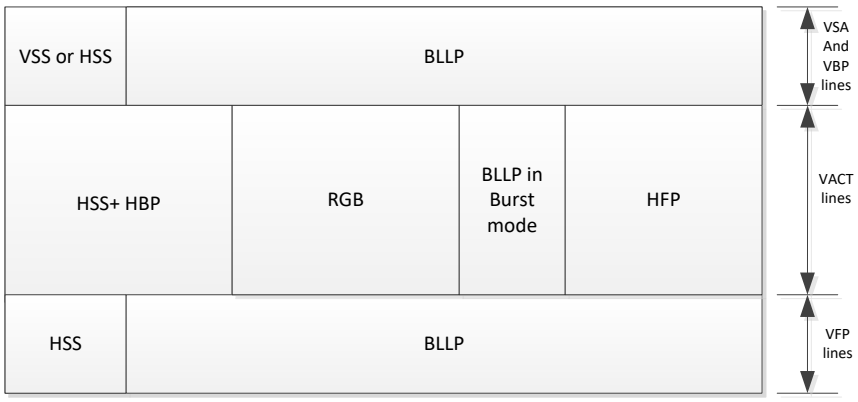

Fig. 27-3 Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packet/states:

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- Bertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.
The MIPI DSI HOST Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (tL) could be half a cycle longer than the tL on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being (1/2 cycle) * (number of lines -1) shorter than tL.
The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the lpcmden bit of the VID_MODE_CFG register is 1, these commands are sent in LP mode. In LP mode, the ouvact_lpcmd_time field of the LP_CMD_TIM register is used to determine if these commands can be transmitted. It is assumed that outvact_lpcmd_time is greater than or equal to 4 bytes (number of bytes in a short packet), because the DSI HOST does not transmit these commands on the last line.
If the frame_BTA_ack field is set in the VID_MODE_CFG register, a BTA is generated by DSI HOST after the last line of a frame. This may coincide with a write command or a read command. In either case, the edpihalt signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).
If the lpcmden bit of the VID_MODE_CFG register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch(VFP) regions.
The outvact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP
Outvact_lpcmd_time=(tL-(Time to transmit HSS and HSE frames +tHSA+Time to enter and leave LP mode+Time to send the D-PHY LPDT command)) / escape clock period / 8 / 2
Where, tL=Line time, and tHSA=Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses).
In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles.
The outvact_lpcmd_time filed can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size of a command that can be transmitted in LP mode is limited to 255 bytes by this field. This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.
Consider an example with 12.6 µs per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed:

- Sync pulses are not being transmitted
- Two lane byte clock ticks are required to transmit a short packet

$$phy_lp2hs_time = 16$$
$$phy_lp2p_time = 20$$

In this example, a 11-byte command can be transmitted as follows:

$$outvact_lpcmd_time = 11bytes$$

The invact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmite a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:
Invact_lpcmd_time=((tHFP-Time to enter and leave low-power mode + Blanking period before the HFP when in Burst mode- Time to send the D-PHY LPDT command) / escape

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clock period) / 8. Where,

$$tHFP = line_time - tHSA - tHBP - tHACT$$

tHACT=vid_pkt_size*bits_per_pixel*lane_byte_clock_period / num_lanes
The invact_lpcmd_time field can be compared directly with the size of the command to be transmitted to determined if there is time to transmit the command.
Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The tL in this case is 12.6µs. With a lane byte clock of 100 MHz, 1260 clock ticks are available to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks (4.6µs) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that 2.3µs is available for HFP and the escape clock is 15MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to enter and leave LP mode. Therefore, only 1 byte could be transmitted in this period.
A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore, in this exampled, commands are not sent in the VACT region. If Burst mode is enabled, more time is available to transmit commands in the VACT region. The following are assumed:
The controller is not in Burst mode:

$$phy_lp2hs_time = 16$$

In this example invact_lpcmd_time is calculated as follows:
Invact_lpcmd_time = (2.3µs –(16*10 ns)-(20*10 ns)-(8*66 ns)) /66 ns / 8 = 2 bytes
The outvact_lpcmd_time and invact_lpcmd_time fields allow a simple comparison to determine if a command can be transmitted in any of the BLLP periods.
Following figure illustrates the meaning of invact_lpcmd_time and outvact_lpcmd_time, matching them with the shaded areas and the VACT region.

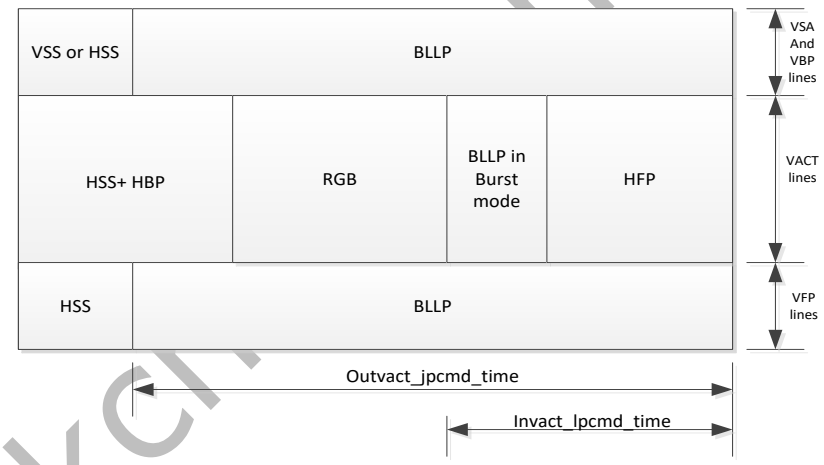

Fig. 27-4 Location in the Image Area

If the lpcmden bit of the VID_MODE_CFG register is 0, the commands are sent in high_speed in Video Mode. In this case, the DSI HOST automatically determines the area where each command can be sent and no programming or calculation is required.
On read command Transmission, the max_rd_time field of the PHY_TMR_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.
The maximum time required to perform a read command in Lane byte clock cycles (max_rd_time) =Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.
The time to return the read data packet from the peripheral depends on the number of bytes read and the escape clock frequency of the peripheral; not the escape clock of the host. The max_rd_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.
In high-speed mode (lpcmden=0), max_rd_time is calculated as follows:
max_rd_time = phy_hs2lp_time + Time to return the read data packet from the peripheral device + phy_hs2hs_time
In low-power mode (lpcmden = 1), max_rd_time is calculated as follows:

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max_rd_time = phy_hs2lp_time +LPDT command time + Read command time in LP mode + Time to return the data read from the peripheral device + phy_lp2hs_time
Where,
LPDT command time = (8*Host escape clock period) / Lane byte clock period
Read command time in LP mode = (32 * host escape clock period) / lane byte clock period
It is recommended to keep the maximum number of bytes read from the peripheral to a minimum to have sufficient time available to issue the read commands on a line. Ensure that max_rd_time* Lane byte clock period is less than outvact_lpcmd_time *8*Escape clock period of the host.
Otherwise, the read commands are serviced on the last line of a frame and the edpihalt signal may be asserted. If it is necessary to read a large number of parameters (>16), increase the max_rd_time while the read command is being executed. When the read has completed, decrease the max_rd_time to a lower value.

27.4 Register Description

27.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

27.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VERSION	0x0000	W	0x3133302a	Version
MIPI_DSI_HOST_PWR_UP	0x0004	W	0x00000000	Power up
MIPI_DSI_HOST_CLKMGR_CFG	0x0008	W	0x00000000	Configure the factor of the internal dividers to divide lanebyteclk
MIPI_DSI_HOST_DPI_VCID	0x000c	W	0x00000000	DPI virtual channel id
MIPI_DSI_HOST_DPI_COLOR_CODING	0x0010	W	0x00000000	DPI color coding
MIPI_DSI_HOST_DPI_CFG_POL	0x0014	W	0x00000000	Polarity of the DPI signals
MIPI_DSI_HOST_DPI_LP_CMD_TIM	0x0018	W	0x00000000	The timing for the low-power command while in video mode
MIPI_DSI_HOST_PCKHDL_CFG	0x002c	W	0x00000000	Configures how EoTp,BTA,CRC and ECC are to be used , to meet the peripheral’s characteristics
MIPI_DSI_HOST_GEN_VCID	0x0030	W	0x00000000	The virtual channel id of the read responses to store and return to the Generic interface
MIPI_DSI_HOST_MODE_CFG	0x0034	W	0x00000001	This register configures the mode of operation - Video mode or Command mode(Commands can be sent even in video mode too)
MIPI_DSI_HOST_VID_MODE_CFG	0x0038	W	0x00000000	Configure several aspects of the Video mode operation
MIPI_DSI_HOST_VID_PKT_SIZE	0x003c	W	0x00000000	The video packet size

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VID_NUM_CHUNKS	0x0040	W	0x00000000	The number of chunks to use
MIPI_DSI_HOST_VID_NULL_SIZE	0x0044	W	0x00000000	The size of null packets
MIPI_DSI_HOST_VID_HSA_TIME	0x0048	W	0x00000000	HSA time
MIPI_DSI_HOST_VID_HBP_TIME	0x004c	W	0x00000000	HBP time
MIPI_DSI_HOST_VID_HLINE_TIME	0x0050	W	0x00000000	The overall time for video line
MIPI_DSI_HOST_VID_VSA_LINES	0x0054	W	0x00000000	VSA period
MIPI_DSI_HOST_VID_VBP_LINES	0x0058	W	0x00000000	VBP period
MIPI_DSI_HOST_VID_VFP_LINES	0x005c	W	0x00000000	VFP period
MIPI_DSI_HOST_VID_VACTIVE_LINES	0x0060	W	0x00000000	The vertical resolution of the video
MIPI_DSI_HOST_EDPI_CMD_SIZE	0x0064	W	0x00000000	The size of eDPI packet
MIPI_DSI_HOST_CMD_MODE_CFG	0x0068	W	0x00000000	Configure several aspects of the command mode operation
MIPI_DSI_HOST_GEN_HDR	0x006c	W	0x00000000	Set the header for new packets sent using the Generic interface
MIPI_DSI_HOST_GEN_PLD_DATA	0x0070	W	0x00000000	The payload for the packet sent using the Generic interface
MIPI_DSI_HOST_CMD_PKT_STATUS	0x0074	W	0x00000000	The status of FIFOs related to the Generic interface
MIPI_DSI_HOST_TO_CNT_CFG	0x0078	W	0x00000000	The counters that trigger the timeout error
MIPI_DSI_HOST_HS_RD_TO_CNT	0x007c	W	0x00000000	The Peripheral Response timeout after high-speed read operation
MIPI_DSI_HOST_LP_RD_TO_CNT	0x0080	W	0x00000000	The Peripheral Response timeout after low-power read operation
MIPI_DSI_HOST_HS_WR_TO_CNT	0x0084	W	0x00000000	The Peripheral Response timeout after high-speed write operation
MIPI_DSI_HOST_LP_WR_TO_CNT	0x0088	W	0x00000000	The Peripheral Response timeout after low-power write operation
MIPI_DSI_HOST_BTA_TO_CNT	0x008c	W	0x00000000	The Peripheral Response timeout after the Bus Turnaround completion
MIPI_DSI_HOST_SDF_3D	0x0090	W	0x00000000	The 3D control information for VSS Packets in video mode

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_LPCLK_CTRL	0x0094	W	0x00000000	Using non-continuous clock in the clock lane
MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG	0x0098	W	0x00000000	Set the time that the HOST assumes in calculations for the clock lane to switch between high-speed and low-power
MIPI_DSI_HOST_PHY_TMR_CFG	0x009c	W	0x00000000	Set the time that the HOST assumes in calculations for the data lanes to switch between high-speed and low-power
MIPI_DSI_HOST_PHY_RSTZ	0x00a0	W	0x00000000	The reset of the PLL and DPHY
MIPI_DSI_HOST_PHY_IF_CFG	0x00a4	W	0x00000003	The minimum time to remain in Stop state
MIPI_DSI_HOST_PHY_STATUS	0x00b0	W	0x00000000	The DPHY status
MIPI_DSI_HOST_INT_ST0	0x00bc	W	0x00000000	The status of the interrupt sources
MIPI_DSI_HOST_INT_ST1	0x00c0	W	0x00000000	The status of the interrupt sources
MIPI_DSI_HOST_INT_MSK0	0x00c4	W	0x00000000	The masks of interrupt sources
MIPI_DSI_HOST_INT_MSK1	0x00c8	W	0x00000000	The masks of interrupt sources
MIPI_DSI_HOST_INT_FORCE0	0x00d8	W	0x00000000	Force interrupts
MIPI_DSI_HOST_INT_FORCE1	0x00dc	W	0x00000000	Force interrupts
MIPI_DSI_HOST_VID_SHADOW_CTRL	0x0100	W	0x00000000	Control the DPI shadow register
MIPI_DSI_HOST_DPI_VCID_ACT	0x010c	W	0x00000000	The virtual channel id for the DPI traffic
MIPI_DSI_HOST_DPI_COLOR_CODING_ACT	0x0110	W	0x00000000	DPI color coding
MIPI_DSI_HOST_DPI_LP_CMD_TIM_ACT	0x0118	W	0x00000000	The timing for low-power commands sent while in Video mode
MIPI_DSI_HOST_VID_MODE_CFG_ACT	0x0138	W	0x00000000	Configure several aspects of Video mode operation
MIPI_DSI_HOST_VID_PKT_SIZE_ACT	0x013c	W	0x00000000	Configure the video packet size
MIPI_DSI_HOST_VID_NUM_CHUNKS_ACT	0x0140	W	0x00000000	Configure the number of chunks to use

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VID_NULL_SIZE_ACT	0x0144	W	0x00000000	The size of null packets
MIPI_DSI_HOST_VID_HSA_TIME_ACT	0x0148	W	0x00000000	HSA time
MIPI_DSI_HOST_VID_HBP_TIME_ACT	0x014c	W	0x00000000	HBP time
MIPI_DSI_HOST_VID_HLINE_TIME_ACT	0x0150	W	0x00000000	The overall time for each video line
MIPI_DSI_HOST_VID_VSA_LINES_ACT	0x0154	W	0x00000000	VSA period
MIPI_DSI_HOST_VID_VBP_LINES_ACT	0x0158	W	0x00000000	VBP period
MIPI_DSI_HOST_VID_VFP_LINES_ACT	0x015c	W	0x00000000	VFP period
MIPI_DSI_HOST_VID_VACTIVE_LINES_ACT	0x0160	W	0x00000000	The vertical resolution of video
MIPI_DSI_HOST_SDF_3D_ACT	0x0190	W	0x00000000	Store 3D control information for VSS in video mode

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

27.4.3 Detail Register Description

MIPI_DSI_HOST_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x3133302a	version

MIPI_DSI_HOST_PWR_UP

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	shutdownz This bit configures the core either to power up or to reset. Its default value is 0. After the core configuration, to enable the DSI Host Controller, set this register to 1. 1'b0: Reset 1'b1: Power-up

MIPI_DSI_HOST_CLKMGR_CFG

Address: Operational Base + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:8	RW	0x00	to_clk_division This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error
7:0	RW	0x00	tx_esc_clk_division This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation

MIPI_DSI_HOST_DPI_VCID

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets

MIPI_DSI_HOST_DPI_COLOR_CODING

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	Reserved
8	RW	0x0	loosely18_en When set to 1, this bit activates loosely packed variant to 18-bit configurations
7:4	RO	0x0	Reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 4'b0000: 16-bit configuration 1 4'b0001: 16-bit configuration 2 4'b0010: 16-bit configuration 3 4'b0011: 18-bit configuration 1 4'b0100: 18-bit configuration 2 4'b0101: 24-bit 4'b0110: 20-bit YCbCr 4:2:2 loosely packed 4'b0111: 24-bit YCbCr 4:2:2 4'b1000: 16-bit YCbCr 4:2:2 4'b1001: 30-bit 4'b1010: 36-bit 4'b1011-4'b1111: 12-bit YCbCr 4:2:0

MIPI_DSI_HOST_DPI_CFG_POL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	colorm_active_low When set to 1, this bit configures the color mode pin (dpicolorm) as active low
3	RW	0x0	shutd_active_low When set to 1, this bit configures the shutdown pin (dpishutdn) as active low
2	RW	0x0	hsync_active_low When set to 1, this bit configures the horizontal synchronism pin (dpihsync) as active low
1	RW	0x0	vsync_active_low When set to 1, this bit configures the vertical synchronism pin (dpivsync) as active low
0	RW	0x0	dataen_active_low When set to 1, this bit configures the data enable pin (dpidataen) as active low

MIPI_DSI_HOST_DPI_LP_CMD_TIM

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved
23:16	RW	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions
15:8	RO	0x0	Reserved
7:0	RW	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region

MIPI_DSI_HOST_PCKHDL_CFG

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	Reserved
4	RW	0x0	crc_rx_en When set to 1, this bit enables the CRC reception and error reporting
3	RW	0x0	ecc_rx_en When set to 1, this bit enables the ECC reception, error correction, and reporting
2	RW	0x0	bta_en When set to 1, this bit enables the Bus Turn-Around (BTA) request
1	RW	0x0	eotp_rx_en When set to 1, this bit enables the EoTp reception

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Bit	Attr	Reset Value	Description
0	RW	0x0	eotp_tx_en When set to 1, this bit enables the EoTp transmission

MIPI_DSI_HOST_GEN_VCID

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	gen_vcid_rx This field indicates the Generic interface read-back virtual channel identification

MIPI_DSI_HOST_MODE_CFG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x1	cmd_video_mode This bit configures the operation mode: 1'b0: Video mode 1'b1: Command mode

MIPI_DSI_HOST_VID_MODE_CFG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 1'b0: Vertical mode 1'b1: Horizontal mode
23:21	RO	0x0	Reserved
20	RW	0x0	vpg_mode This field is to select the pattern: 1'b0: Color bar (horizontal or vertical) 1'b1: BER pattern (vertical only)
19:17	RO	0x0	Reserved
16	RW	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator
15	RW	0x0	lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode
14	RW	0x0	frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RW	0x0	lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows

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Bit	Attr	Reset Value	Description
12	RW	0x0	lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows
11	RW	0x0	lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows
10	RW	0x0	lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows
9	RW	0x0	lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows
8	RW	0x0	lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows
7:2	RO	0x0	Reserved
1:0	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 2'b11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RW	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification

MIPI_DSI_HOST_VID_NUM_CHUNKS

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RW	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line

MIPI_DSI_HOST_VID_NULL_SIZE

Address: Operational Base + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets

MIPI_DSI_HOST_VID_HSA_TIME

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HBP_TIME

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HLINE_TIME

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14:0	RW	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles

MIPI_DSI_HOST_VID_VSA_LINES

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VBP_LINES

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VFP_LINES

Address: Operational Base + offset (0x005c)

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VACTIVE_LINES

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RW	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines

MIPI_DSI_HOST_EDPI_CMD_SIZE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	edpi_allowed_cmd_size This field configures the maximum allowed size for an eDPI write memory command, measured in pixels. Automatic partitioning of data obtained from eDPI is permanently enabled

MIPI_DSI_HOST_CMD_MODE_CFG

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	max_rd_pkt_size This bit configures the maximum read packet size command transmission type: 1'b0: High-speed 1'b1: Low-power
23:20	RO	0x0	Reserved
19	RW	0x0	dcs_lw_tx This bit configures the DCS long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
18	RW	0x0	dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power

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Bit	Attr	Reset Value	Description
17	RW	0x0	dcs_sw_1p_tx This bit configures the DCS short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
16	RW	0x0	dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
15	RO	0x0	Reserved
14	RW	0x0	gen_lw_tx This bit configures the Generic long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
13	RW	0x0	gen_sr_2p_tx This bit configures the Generic short read packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power
12	RW	0x0	gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
11	RW	0x0	gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
10	RW	0x0	gen_sw_2p_tx This bit configures the Generic short write packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power

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Bit	Attr	Reset Value	Description
9	RW	0x0	gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
8	RW	0x0	gen_sw_0p_tx This bit configures the Generic short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
7:2	RO	0x0	Reserved
1	RW	0x0	ack_rqst_en When set to 1, this bit enables the acknowledge request after each packet transmission
0	RW	0x0	tear_fx_en When set to 1, this bit enables the tearing effect acknowledge request

MIPI_DSI_HOST_GEN_HDR

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved
23:16	RW	0x00	gen_wc_msbyte
15:8	RW	0x00	gen_wc_lsbyte This field configures the least significant byte of the header packet's word count for long packets or data 0 for short packets
7:6	RW	0x0	gen_vc This field configures the virtual channel id of the header packet
5:0	RW	0x00	gen_dt This field configures the packet data type of the header packet

MIPI_DSI_HOST_GEN_PLD_DATA

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gen_pld_b4 This field indicates byte 4 of the packet payload
23:16	RW	0x00	gen_pld_b3 This field indicates byte 3 of the packet payload
15:8	RW	0x00	gen_pld_b2 This field indicates byte 2 of the packet payload
7:0	RW	0x00	gen_pld_b1 This field indicates byte 1 of the packet payload

MIPI_DSI_HOST_CMD_PKT_STATUS

Address: Operational Base + offset (0x0074)

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Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14	RW	0x0	dbi_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO
13	RO	0x0	dbi_pld_r_full This bit indicates the full status of the DBI read payload FIFO
12	RO	0x0	dbi_pld_r_empty This bit indicates the empty status of the DBI read payload FIFO
11	RO	0x0	dbi_pld_w_full This bit indicates the full status of the DBI write payload FIFO
10	RO	0x0	dbi_pld_w_empty This bit indicates the empty status of the DBI write payload FIFO
9	RO	0x0	dbi_cmd_full This bit indicates the full status of the DBI command FIFO
8	RO	0x0	dbi_cmd_empy This bit indicates the empty status of the DBI command FIFO
7	RO	0x0	Reserved
6	RO	0x0	gen_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO
5	RO	0x0	gen_pld_r_full This bit indicates the full status of the generic read payload FIFO
4	RO	0x0	gen_pld_r_empty This bit indicates the empty status of the generic read payload FIFO
3	RO	0x0	gen_pld_w_full This bit indicates the full status of the generic write payload FIFO
2	RO	0x0	gen_pld_w_empty This bit indicates the empty status of the generic write payload FIFO
1	RO	0x0	gen_cmd_full This bit indicates the full status of the generic command FIFO
0	RO	0x0	gen_cmd_empty This bit indicates the empty status of the generic command FIFO

MIPI_DSI_HOST_TO_CNT_CFG

Address: Operational Base + offset (0x0078)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hstx_to_cnt This field configures the timeout counter that triggers a high-speed transmission timeout contention detection (measured in TO_CLK_DIVISION cycles). If using the non-burst mode and there is no sufficient time to switch from HS to LP and back in the period which is from one line data finishing to the next line sync start, the DSI link returns the LP state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one FRAME data transmission * (1 + 10%) In burst mode, RGB pixel packets are time-compressed, leaving more time during a can line. Therefore, if in burst mode and there is sufficient time to switch from HS to LP and back in the period of time from one line data finishing to the next line sync start, the DSI link can return LP mode and back in this time interval to save power. For this, configure the TO_CLK_DIVISION and hstx_to_cnt to be in ccordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one LINE data transmission * (1 + 10%)
15:0	RW	0x0000	lprx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in TO_CLK_DIVISION cycles)

MIPI_DSI_HOST_HS_RD_TO_CNT

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	hs_rd_to_cnt This field sets a period for which the DSI Host Controller keeps the link still, after sending a high-speed read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_LP_RD_TO_CNT

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	lp_rd_to_cnt This field sets a period for which the DSI Host Controller keeps the link still, after sending a low-power read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_HS_WR_TO_CNT

Address: Operational Base + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	presp_to_mode When set to 1, this bit ensures that the peripheral response timeout caused by hs_wr_to_cnt is used only once per eDPI frame, when both the following conditions are met: dpivsync_edpiwms has risen and fallen. Packets originated from eDPI have been transmitted and its FIFO is empty again. In this scenario no non-eDPI requests are sent to the D-PHY, even if there is traffic from generic or DBI ready to be sent, making it return to stop state. When it does so, PRESP_TO counter is ctivated and only when it finishes does the controller send any other traffic that is ready
23:16	RO	0x0	Reserved
15:0	RW	0x0000	hs_wr_to_cnt This field sets a period for which the DSI Host Controller keeps the link inactive after sending a high-speed write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_LP_WR_TO_CNT

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	lp_wr_to_cnt This field sets a period for which the DSI Host Controller keeps the link still, after sending a low-power write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_BTA_TO_CNT

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	bta_to_cnt This field sets a period for which the DSI Host Controller keeps the link still, after completing a Bus Turn-Around. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_SDF_3D

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved
16	RW	0x0	send_3d_cfg When set, causes the next VSS packet to include 3D control payload in every VSS packet

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Bit	Attr	Reset Value	Description
15:6	RO	0x0	Reserved
5	RW	0x0	right_first This bit defines the left or right order: 1'b0: Left eye data is sent first, and then the right eye data is sent 1'b1: Right eye data is sent first, and then the left eye data is sent
4	RW	0x0	second_vsync This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 1'b0: No sync pulses between left and right data 1'b1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data
3:2	RW	0x0	format_3d This field defines the 3D image format: 2'b00: Line (alternating lines of left and right data) 2'b01: Frame (alternating frames of left and right data) 2'b10: Pixel (alternating pixels of left and right data) 2'b11: Reserved
1:0	RW	0x0	mode_3d This field defines the 3D mode on/off and display orientation: 2'b00: 3D mode off (2D mode on) 2'b01: 3D mode on, portrait orientation 2'b10: 3D mode on, landscape orientation 2'b11: Reserved

MIPI_DSI_HOST_LPCLK_CTRL

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1	RW	0x0	auto_clklane_ctrl This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows
0	RW	0x0	phy_txrequestclkhs This bit controls the D-PHY PPI txrequestclkhs signal

MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG

Address: Operational Base + offset (0x0098)

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Bit	Attr	Reset Value	Description
31:26	RO	0x0	Reserved
25:16	RW	0x000	phy_clkhs2lp_time This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles
15:10	RO	0x0	Reserved
9:0	RW	0x000	phy_clklp2hs_time This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles

MIPI_DSI_HOST_PHY_TMR_CFG

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	phy_hs2lp_time This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles
23:16	RW	0x00	phy_lp2hs_time This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles
15	RO	0x0	Reserved
14:0	RW	0x0000	max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress

MIPI_DSI_HOST_PHY_RSTZ

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	Reserved
3	RW	0x0	phy_forcepll When the D-PHY is in ULPS, this bit enables the D-PHY PLL. Dependency: DSI_HOST_FPGA = 0. Otherwise, this bit is Reserved
2	RW	0x0	phy_enableclk When set to1, this bit enables the D-PHY Clock Lane module
1	RW	0x0	phy_rstz When set to 0, this bit places the digital section of the D-PHY in the reset state
0	RW	0x0	phy_shutdownz When set to 0, this bit places the D-PHY macro in power-down state

MIPI_DSI_HOST_PHY_IF_CFG

Address: Operational Base + offset (0x00a4)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:8	RW	0x00	phy_stop_wait_time This field configures the minimum wait period to request a high-speed transmission after the Stop state
7:2	RO	0x0	Reserved
1:0	RW	0x3	n_lanes This field configures the number of active data lanes: 2'b00: One data lane (lane 0) 2'b01: Two data lanes (lanes 0 and 1) 2'b10: Three data lanes (lanes 0, 1, and 2) 2'b11: Four data lanes (lanes 0, 1, 2, and 3)

MIPI_DSI_HOST_PHY_STATUS

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12	RO	0x0	phy_ulpsactivenot3lane This bit indicates the status of ulpsactivenot3lane D-PHY signal
11	RO	0x0	phy_stopstate3lane This bit indicates the status of phystopstate3lane D-PHY signal
10	RO	0x0	phy_ulpsactivenot2lane This bit indicates the status of ulpsactivenot2lane D-PHY signal
9	RO	0x0	phy_stopstate2lane This bit indicates the status of phystopstate2lane D-PHY signal
8	RO	0x0	phy_ulpsactivenot1lane This bit indicates the status of ulpsactivenot1lane D-PHY signal
7	RO	0x0	phy_stopstate1lane This bit indicates the status of phystopstate1lane D-PHY signal
6	RO	0x0	phy_rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal
5	RO	0x0	phy_ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal
4	RO	0x0	phy_stopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal
3	RO	0x0	phy_ulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal
2	RO	0x0	phy_stopstateclklane This bit indicates the status of phystopstateclklane D-PHY signal
1	RO	0x0	phy_direction This bit indicates the status of phydirection D-PHY signal
0	RO	0x0	phy_lock This bit indicates the status of phylock D-PHY signal

MIPI_DSI_HOST_INT_ST0

Address: Operational Base + offset (0x00bc)

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Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved
20	RO	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RO	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RO	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
13	RO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RO	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RO	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RO	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RO	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report

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Bit	Attr	Reset Value	Description
5	RO	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RO	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_ST1

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RO	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RO	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RO	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RO	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RO	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted

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Bit	Attr	Reset Value	Description
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RO	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_INT_MSK0

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0

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Bit	Attr	Reset Value	Description
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RW	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report

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Bit	Attr	Reset Value	Description
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_MSK1

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RW	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RW	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted

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Bit	Attr	Reset Value	Description
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_INT_FORCE0

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0

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Bit	Attr	Reset Value	Description
18	RW	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RW	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report

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Bit	Attr	Reset Value	Description
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_FORCE1

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RW	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RW	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent

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Bit	Attr	Reset Value	Description
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_VID_SHADOW_CTRL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved
16	RW	0x0	vid_shadow_pin_req When set to 1, the video request is done by external pin. In this mode, vid_shadow_req is ignored
15:9	RO	0x0	Reserved
8	RW	0x0	vid_shadow_req When set to 1, the DPI registers are copied to the auxiliary registers. After copying, this bit is auto cleared
7:1	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	vid_shadow_en When set to 1, DPI receives the active configuration from the auxiliary registers. When this bit is set along with the id_shadow_req bit, the auxiliary registers are automatically updated

MIPI_DSI_HOST_DPI_VCID_ACT

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the video mode packets

MIPI_DSI_HOST_DPI_COLOR_CODING_ACT

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	Reserved
8	RW	0x0	loosely18_en When set to 1, this bit activates loosely packed variant to 18-bit configurations
7:4	RO	0x0	Reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 4'b0000: 16-bit configuration 1 4'b0001: 16-bit configuration 2 4'b0010: 16-bit configuration 3 4'b0011: 18-bit configuration 1 4'b0100: 18-bit configuration 2 4'b0101: 24-bit 4'b0110: 20-bit YCbCr 4:2:2 loosely packed 4'b0111: 24-bit YCbCr 4:2:2 4'b1000: 16-bit YCbCr 4:2:2 4'b1001: 30-bit 4'b1010: 36-bit 4'b1011-4'b1111: 12-bit YCbCr 4:2:0

MIPI_DSI_HOST_DPI_LP_CMD_TIM_ACT

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved
23:16	RO	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions
15:8	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region

MIPI_DSI_HOST_VID_MODE_CFG_ACT

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 1'b0: Vertical mode 1'b1: Horizontal mode
23:21	RO	0x0	Reserved
20	RO	0x0	vpg_mode This field is to select the pattern: 1'b0: Color bar (horizontal or vertical) 1'b1: BER pattern (vertical only)
19:17	RO	0x0	Reserved
16	RO	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator
15	RO	0x0	lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode
14	RO	0x0	frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RO	0x0	lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows
12	RO	0x0	lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows
11	RO	0x0	lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows
10	RO	0x0	lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows
9	RO	0x0	lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows
8	RO	0x0	lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows
7:2	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
1:0	RO	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 2'b11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE_ACT

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RO	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification

MIPI_DSI_HOST_VID_NUM_CHUNKS_ACT

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RO	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line

MIPI_DSI_HOST_VID_NULL_SIZE_ACT

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets

MIPI_DSI_HOST_VID_HSA_TIME_ACT

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RO	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HBP_TIME_ACT

Address: Operational Base + offset (0x014c)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HLINE_TIME_ACT

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14:0	RO	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles

MIPI_DSI_HOST_VID_VSA_LINES_ACT

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RO	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VBP_LINES_ACT

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VFP_LINES_ACT

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RO	0x0	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VACTIVE_LINES_ACT

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RO	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines

MIPI_DSI_HOST_SDF_3D_ACT

Address: Operational Base + offset (0x0190)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved
16	RW	0x0	send_3d_cfg When set, causes the next VSS packet to include 3D control payload in every VSS packet
15:6	RO	0x0	Reserved
5	RO	0x0	right_first This bit defines the left or right order: 1'b0: Left eye data is sent first, and then the right eye data is sent. 1'b1: Right eye data is sent first, and then the left eye data is sent
4	RO	0x0	second_vsync This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 1'b0: No sync pulses between left and right data 1'b1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data
3:2	RO	0x0	format_3d This field defines the 3D image format: 2'b00: Line (alternating lines of left and right data) 2'b01: Frame (alternating frames of left and right data) 2'b10: Pixel (alternating pixels of left and right data) 2'b11: Reserved
1:0	RO	0x0	mode_3d This field defines the 3D mode on/off and display orientation: 2'b00: 3D mode off (2D mode on) 2'b01: 3D mode on, portrait orientation 2'b10: 3D mode on, landscape orientation 2'b11: Reserved

27.5 Application Notes

Perform the following steps to configure the DPI packet transmission:

- Step1: Global configuration:
  - Configure n_lanes (PHY_IF_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.
- Step2: Configure the DPI Interface to define how the DPI interface interacts with the controller.
  - Configure dpi_vid (DPI_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.
  - Configure dpi_color_coding (DPI_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable_18_loosely_packed is not active, the number or pixels per line should be a multiple of four.
  - Configure dataen_active_low (DPI_CFG-[5]): This bit configures the polarity of the dpidataen signal and enables if it is active low.
  - Configure vsync_active_low (DPI_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
  - Configure vsync_active_low (DPI_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

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- Configure vsync_active_low (DPI_CFG-[8]): This bit configures the polarity of the dpishutdn signal and enables if it is active low.
- Configure vsync_active_low (DPI_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.
- Configure en18_loosely (DPI_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when dpi_color_coding is 18 bpp. This bit enables loosely packing.

- Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.
  - Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video line to be transported through the DSI link.
  - Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.
  - Configure frame_BTA_ack (VID_MODE_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.
  - Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packed with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the DSI Host Controller to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.
    - Configure the register fiedl vid_mode_type (VID_MODE_CFG-[10]), num_chunks (VID_PKT_CFG-[20:11]), and null_pkt_size (VID_PKT_CFG-[30:21]) are automatically ignored by the DSI Host Controller.
  - Non-Burst mode: In this mode, the processor uses the partitioning properties of the DSI Host Controller to divide the video line transmission into several DSI packets. This is done to match th pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration does not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.
    - Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’ b0x.
    - Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’ b00x to enable the transmission of sync pulses.
    - Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’ b01to enable the transmission of sync events.
    - Configure the vid_mode_type field (VID_MODE_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.
    - Configure the en_multi_pkt field (VID_MODE_CFG-[9]) to enable the division of the active video transmission into more than one packet.
    - Configure the num_chunks field (VID_MODE_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.
    - Configure the en_null_pkt field (VID_MODE_CFG-[10]) to enable the insertion of null packets between video packets.
    - The field is effective only when en_multi_pkt field is activated, otherwise the controller ignores it and does not sent the null packets.
    - Configure the null_pkt_size field (VID_MODE_CFG-[30:21]) with the actual size of the inserted null packet.
- Step4: Define the DPI Horizontal timing configuration as follows:
  - Configure the hline_time field (TMR_LINE_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the hline_time is a result of a round of a number. If the DSI Host Controller is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines, the DSI Host Controller can have a number of errors that can cause a malfunction of the video transmission.
  - Configure the hsa_time field (TMR_LINE_CFG-[8:0]) with the time taken by a DPI

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Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).
  - Configure the hbp_time field (TMR_LINE_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns). Special attention should be given to the calculation of this parameter.
- Step5: Define the Vertical line configuration:
  - Configure the vsa_lines field (VTIMING_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.
  - Configure the vbp_lines field (VTIMING_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.
  - Configure the vfp_lines field (VTIMING_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.
  - Configure the v_active_lines field (VTIMING_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.

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Chapter 28 MIPI_TX_DPHY

28.1 Overview

The MIPI TX DPHY supports up to 1.5Gbps high speed data transmitter, plus a MIPI low-power low speed transceiver that supports data transfer in the bi-directional mode.

Features

- MIPI
  - One clock lane channel and four data channels
  - Designed to MIPI 1.2 specification
  - Data Channel 0: Bi-directional with Low-Power RX(LP-RX) and Low-Power CD(LP-CD)
  - Channel1~4: High-Speed TX(HS-TX) and a low-Power TX(LP-TX)
  - Maximum HS data rate: 2.5Gbps per lane
  - LP operation rate: 10Mbps per lane
  - Skew-Calibration supported
  - Automatic termination control for HS and LP modes
  - Low-Power dissipation: less than 16mW/lane in MIPI HS TX mode
- LVDS
  - Maximum Support data rate: 1.2Gbps per lane

28.2 Function Description

MIPI TX DPHY configuration contains one clock lane module and four data lane modules. Each of these PHY lane modules communicates via two lines to a complementary part at the other side of the lane interconnect. Figure below shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function.

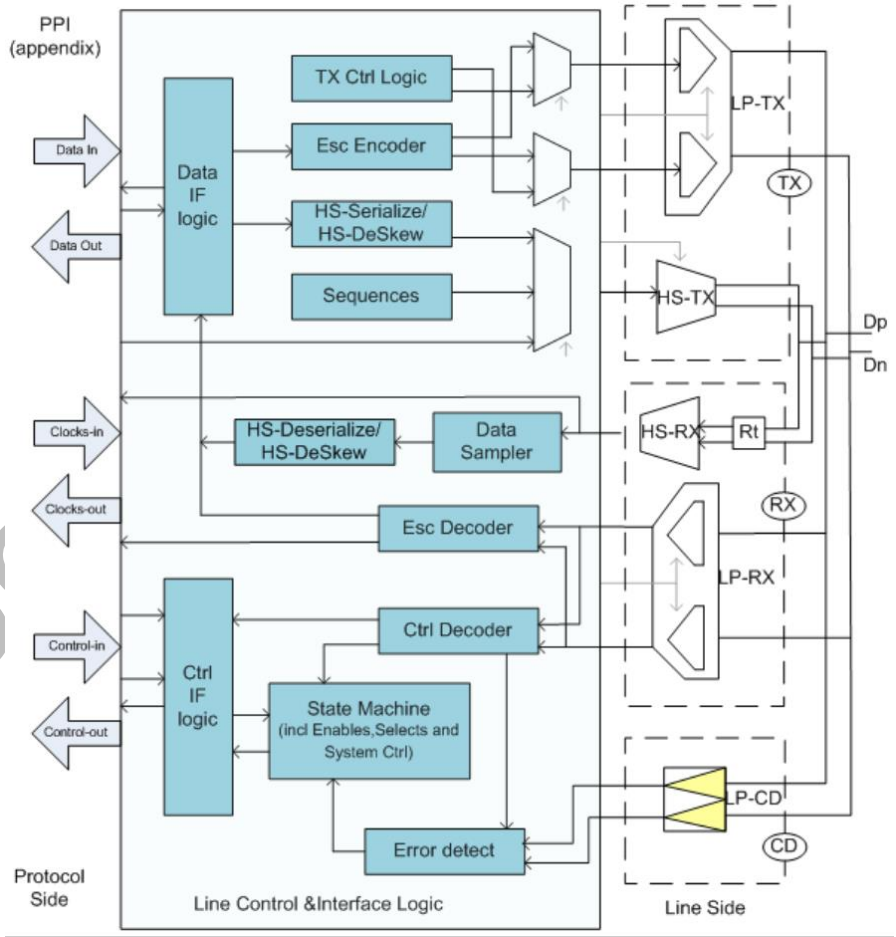

Fig. 28-1 MIPI TX DPHY Architecture

28.2.1 MIPI Mode High Speed Data Transmission

Once the initialization sequence is completed, the TX DPHY remains in control mode. From the transmitter side, high-speed mode is entered when the corresponding txrequesths input is set high through DSI Host Controller. A burst contains the low-power initialization

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sequenc, the high-speed data payload,and the end of transmission sequence.

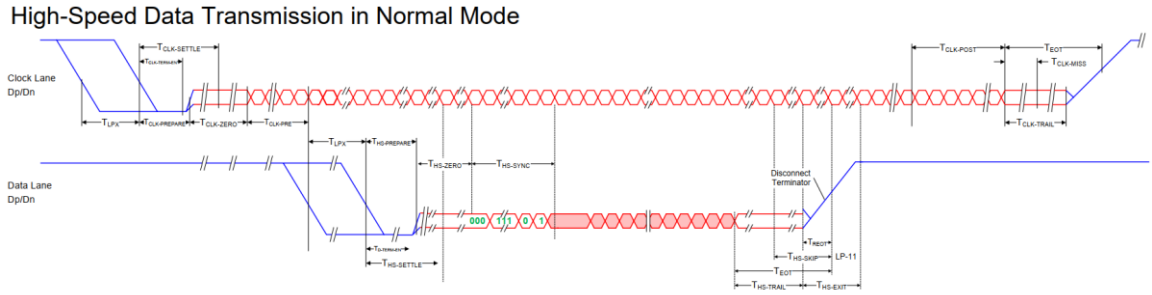

Fig. 28-2 MIPI High Speed Data Transmission in Bursts

28.2.2 LVDS Mode Data Transmission

Figure below shows the LVDS output timing. CLKP is the output clock, whose frequency is the same as the pixel clock. D0P/D0N is a pair differential serial data output. The output serial data is transmitted as MSB first. The rising edge of the output clock is at the transition of bit2 and bit1 of the pin_pdata_*[6:0].

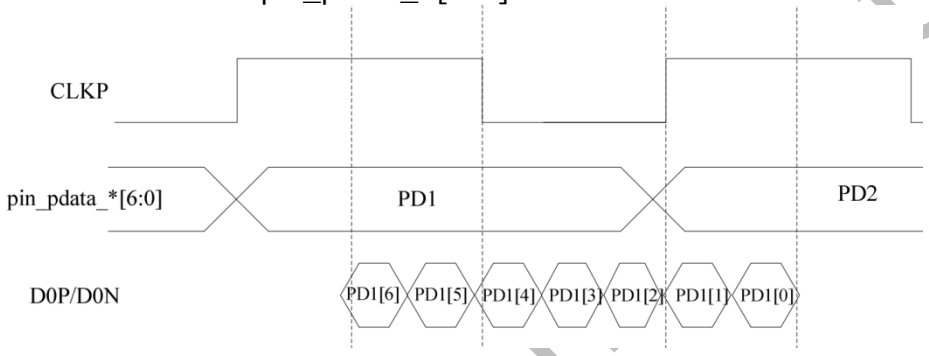

Fig. 28-3 LVDS Data Transmission

28.3 Register Description

28.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

28.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MIPI_TX_PHY_ANALOG_REG00	0x0000	B	0x00000001	Power control and lane enable
MIPI_TX_PHY_ANALOG_REG01	0x0001	B	0x000000E3	PLL power control
MIPI_TX_PHY_ANALOG_REG03	0x0003	B	0x00000083	PLL_PREDIV
MIPI_TX_PHY_ANALOG_REG04	0x0004	B	0x000000FA	PLL_FBDIV
MIPI_TX_PHY_ANALOG_REG08	0x0008	B	0x0000004E	PLL post divider
MIPI_TX_PHY_DIGITAL_REG00	0x0020	B	0x0000001F	Digital Reset
MIPI_TX_PHY_DIGITAL_REG01	0x0021	B	0x00000000	Revert clock
MIPI_TX_PHY_LVDS_REG00	0x00E0	B	0x00000045	LVDS MSB mode
MIPI_TX_PHY_LVDS_REG01	0x00E1	B	0x00000012	LVDS digital enable
MIPI_TX_PHY_LVDS_REG03	0x00E3	B	0x00000001	PHY Mode

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Name	Offset	Size	Reset Value	Description
MIPI_TX_PHY_LVDS_REG0B	0x00EB	B	0x00000004	LVDS power ctrl and lane enable

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

28.3.3 Detail Registers Description

MIPI_TX_PHY_ANALOG_REG00

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
7	RW	0x0	bandgap_power bandgap power down enable 1'b1: Power down 1'b0: Power on
6	RW	0x0	lane_en_ck Clock lane enable 1'b1: Enable 1'b0: Disable
5	RW	0x0	lane_en_3 Lane3 enable 1'b1: Enable 1'b0: Disable
4	RW	0x0	lane_en_2 Lane2 enable 1'b1: Enable 1'b0: Disable
3	RW	0x0	lane_en_1 Lane1 enable 1'b1: Enable 1'b0: Disable
2	RW	0x0	lane_en_0 Lane0 enable 1'b1: Enable 1'b0: Disable
1:0	RW	0x1	power 3'b00/3'b01: Power work enable 3'b10: Power work disable 3'b11: Reserved

MIPI_TX_PHY_ANALOG_REG01

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
7:3	RW	0x1c	Reserved Reserved
2	RW	0x0	syncrst 1'b1: Reset 1'b0: Normal
1	RW	0x1	ldopd 1'b1: Power down 1'b0: Power on
0	RW	0x1	pllpd 1'b1: Power down 1'b0: Power on

MIPI_TX_PHY_ANALOG_REG03

Address: Operational Base + offset (0x0003)

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Bit	Attr	Reset Value	Description
7:6	RW	0x2	Reserved Reserved
5	RW	0x0	fbdiv_msb Interger value programmed into feedback fbdiv[8]
4:0	RW	0x03	pll_prediv PLL input reference clock divider

MIPI_TX_PHY_ANALOG_REG04

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
7:0	RW	0xfa	pll_fbdiv PLL feedback divider[7:0]

MIPI_TX_PHY_ANALOG_REG08

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
7	RW	0x0	Pre_emphasis Pre-emphasis enable 1'b1: Enable 1'b0: Disable(default)
6	RW	0x1	Reserved Reserved
5	RW	0x0	pll_postdiv 1'b1: Enable 1'b0: Disable
4	RO	0x0	reserved
3:0	RW	0xe	data_lane_vod Data lanes Vod range set 4'h0: Min-range 4'h1: Mid-range 4'h3: Bigger-range(default value) 4'hf: Max-range

MIPI_TX_PHY_DIGITAL_REG00

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
7:1	RW	0x0f	Reserved Reserved
0	RW	0x1	dig_rstn PHY digital logic reset 1'b1: Normal 1'b0: Reset

MIPI_TX_PHY_DIGITAL_REG01

Address: Operational Base + offset (0x0021)

Bit	Attr	Reset Value	Description
7:2	RO	0x0	reserved
1	RW	0x0	txclkesc_revert Inverting pin_txclkesc enable 1'b1: Enable 1'b0: Disable
0	RW	0x0	txbyteclk_revert Inverting pin_txbyteclkhs enable 1'b1: Enable 1'b0: Disable

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MIPI_TX_PHY_LVDS_REG00

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
7:3	RW	0x08	Reserved Reserved
2	RW	0x1	lvds_digital_reset Digital internal reset 1'b1: Normal(default) 1'b0: Reset
1	RO	0x0	reserved
0	RW	0x1	msb_mode Selection for MSB and LSB 1'b1: MSB 1'b0: LSB

MIPI_TX_PHY_LVDS_REG01

Address: Operational Base + offset (0x00E1)

Bit	Attr	Reset Value	Description
7	RW	0x0	lvds_dig_internal_enable lvds_dig_internal_enable 1'b1: Active 1'b0: Off
6:0	RW	0x12	Reserved Reserved

MIPI_TX_PHY_LVDS_REG03

Address: Operational Base + offset (0x00E3)

Bit	Attr	Reset Value	Description
7:3	RW	0x00	Reserved Reserved
2	RW	0x0	ttl_mode_enable TTL mode enable 1'b1: Enable TTL Mode 1'b0: Disable
1	RW	0x0	lvds_mode_enable LVDS mode enable 1'b1: Enable LVDS Mode 1'b0: Disable
0	RW	0x1	mipi_mode_enable MIPI mode enable 1'b1: Enable MIPI Mode 1'b0: Disable

MIPI_TX_PHY_LVDS_REG0B

Address: Operational Base + offset (0x00EB)

Bit	Attr	Reset Value	Description
7	RW	0x0	lane_en_0 Lane0 enable LVDS mode 1'b1: Enable 1'b0: Disable
6	RW	0x0	lane_en_1 Lane1 enable LVDS mode 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
5	RW	0x0	lane_en_2 Lane2 enable LVDS mode 1'b1: Enable 1'b0: Disable
4	RW	0x0	lane_en_3 Lane3 enable for LVDS mode 1'b1: Enable 1'b0: Disable
3	RW	0x0	lane_en_ck Clock lane enable for LVDS mode 1'b1: Enable 1'b0: Disable
2	RW	0x1	power PLL power for LVDS mode 1'b1: Power off 1'b0: Power on
1:0	RO	0x0	reserved

28.4 Application Notes

28.4.1 MIPI Mode Initialization

Setup Steps:

1. After power on and reset done, set the pin_enable_ck/0/1/2/3 of lanes to be used to high level and the others to low.
2. Send 8'h02 to register 8'h03. Configure PLL PREDIV.
3. Send 8'h53 to register 8'h04. Configure PLL FBDIV.
4. If disable post-divider, send 8'h4e to register 8'h08. Configure PLL POSTDIV.
5. Send 8'he4 to register 8'h01. Enable PLL and LDO.
6. Send 8'h7d to register 8'h00. Enable all lanes on analog part, enable power work, bandgap power on.
7. Send 8'he0 to register 8'h01.Reset analog.
8. Wait a period after analog has been reset.
9. Send 8'h1e to register 8'h20.Reset digital.
10. Send 8'h1f to register 8'h20.Reset digital.
11. Wait some interbal until PLL locked.

28.4.2 LVDS Mode Initialization

1. Set forcerxmode = 1 through *GRF VO_CON2*(for TX DPHY0) register.
2. Configure PLL.Write 8'h01 to the register 8'h03.Write 8'h0e to the register 8'h04.
3. Select LSB mode, default MSB mode. Write 8'h44 to the register 8'he0.(Optional)
4. Enable LVDS digital logic. Write 8'h92 to the register 8'he1.
5. Enable LVDS analog driver. Write 8'hf8 to the register 8'heb.
6. Select LVDS mode. Write 8'h02 to the register 8'he3.
7. Wait a period until PLL locked.

28.4.3 Programmable PLL

The TX DPHY PLL output frequency can be calculated using a sample formula:

$$PLL_OUTPUT_FREQUENCY = \frac{((\frac{FREF}{PREDIV}) \times FBDIV)}{POSTDIV}$$

Where PLL_OUTPUT_FREQUENCY equals to the (DDR-Clock-Frequence * 2)

FREF: PLL input reference frequency, 24Mhz.

PREDIV: PLL input reference clock divider which can be configured by the register of reg_prediv.

FBDIV: Integer value programmed into feedback divider which can configured by the

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register of reg_fbdiv.
POSTDIV: PLL post-divider 2 can be configured by the registers of reg_postdiv.If reg_postdiv is set to 1 , the POSTDIV value is 2. Otherwise, the value is 1.

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Chapter 29 KEYLAD

29.1 Overview

KEYLAD is used to securely protect the transmission and operation of the KEY and ensure that other masters cannot access the KEY.
The KEYLAD supports following features:

- Support Link List Item (LLI) DMA transfer
- Support AES-128, AES-192, AES-256 cipher
- Support DES & TDES cipher
- Support symmetric block cipher ECB mode
- Support for caching specific data of OTP or RKRNG or TRNG and deriving it
- Support write out the data of KEY TABLE to some specific modules
- Support to use data in KEY TABLE as encryption or decryption key
- Support to use data in KEY TABLE as input of symmetric encryption
- Support clear the data in KEY TABLE

29.2 Block Diagram

KEYLAD contains several modules: AHB Slave, DMA, CIPHER, GRANT, KEY TABLE, APB Master.

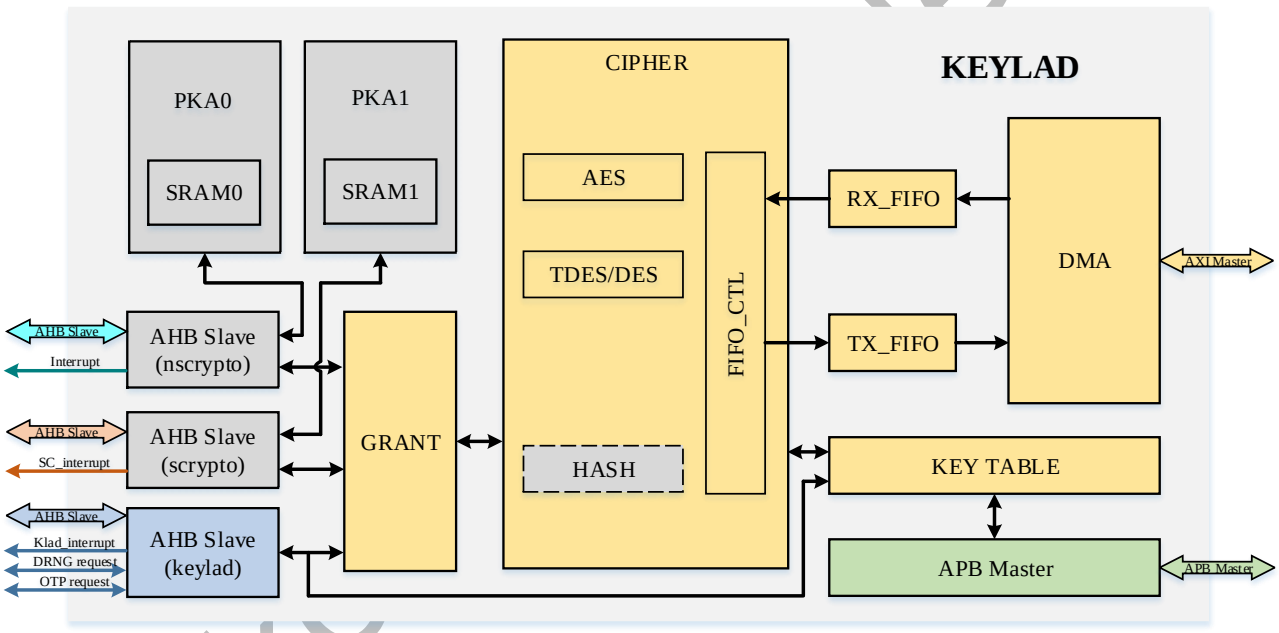

Fig. 29-1 KEYLAD Architecture

29.3 Function Description

29.3.1 AHB Interface

There are three AHB slave interfaces in CRYPTO, AHB Slave(nscrypto) is used to configure registers in non-secure world, AHB Slave(scrypto) and AHB Slave(keylad) are used to configure registers in secure world. These modules are in hclk domain.

29.3.2 DMA

DMA is used to transfer data from external memory to RX_FIFO, or from TX_FIFO to external memory. DMA uses AXI3 protocol with 33-bits address width, 64-bits data width and max burst length to 16. LLI transfer is also supported for performance and convenience consideration. This module is in aclk domain.

29.3.3 CIPHER

CIPHER contains AES, DES/TDES engines. And it also supports various mode operations. The source data is either from RX_FIFO, or from other engine output. The result data is sending either to TX_FIFO, or KEY TABLE. This module is in clk_core domain.

29.3.4 KEY TABLE

The KEY TABLE is used to store OTP KEY, RKRNG data and CIPHER calculate result. The size

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of KEY TABLE is 16 words. The content in KEY TABLE is un-accessible for CPU. This module is in aclk domain.

29.3.5 APB Master

APB Master is used to write data to specific module that require secret configuration data. This APB Master is write-only master. This module is in pclk domain.

29.4 Register Description

29.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

29.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
KEYLAD_CLK_CTL	0x0000	W	0x00000001	Clock Control Register
KEYLAD_RST_CTL	0x0004	W	0x00000000	Reset Control Register
KEYLAD_DMA_INT_EN	0x0008	W	0x00000000	DMA Interrupt Enable Register
KEYLAD_DMA_INT_ST	0x000C	W	0x00000000	DMA Interrupt Status Register
KEYLAD_DMA_CTL	0x0010	W	0x00000000	DMA Control Register
KEYLAD_DMA_LLI_ADDR	0x0014	W	0x00000000	DMA LIST Start Address Register
KEYLAD_DMA_ST	0x0018	W	0x00000000	DMA Status Register
KEYLAD_DMA_STATE	0x001C	W	0x00000000	DMA State Register
KEYLAD_DMA_LLI_RADDR	0x0020	W	0x00000000	DMA LLI Read Address Register
KEYLAD_DMA_SRC_RADDR	0x0024	W	0x00000000	DMA Source Data Read Address Register
KEYLAD_DMA_DST_WADDR	0x0028	W	0x00000000	DMA Destination Data Read Address Register
KEYLAD_DMA_ITEM_ID	0x002C	W	0x00000000	DMA Descriptor ID Register
KEYLAD_FIFO_CTL	0x0040	W	0x00000001	FIFO Control Register
KEYLAD_BC_CTL	0x0044	W	0x00000000	Block Cipher Control Register
KEYLAD_CIPHER_ST	0x004C	W	0x00000000	Cipher Status Register
KEYLAD_CIPHER_STATE	0x0050	W	0x00000400	Cipher Current State Register
KEYLAD_CH0_IV_0	0x0100	W	0x00000000	Channel 0 Iv 0
KEYLAD_CH0_IV_1	0x0104	W	0x00000000	Channel 0 Iv 1
KEYLAD_CH0_IV_2	0x0108	W	0x00000000	Channel 0 Iv 2
KEYLAD_CH0_IV_3	0x010C	W	0x00000000	Channel 0 Iv 3
KEYLAD_APB_CMD	0x0450	W	0x00000000	APB master Command Enable Register
KEYLAD_APB_PADDR	0x0454	W	0x00000000	APB Paddr Register
KEYLAD_APB_PWDATA	0x0458	W	0x00000000	APB Pwdata Register
KEYLAD_DATA_CTL	0x0460	W	0x00000000	Usage of Keytable Data
KEYLAD_KD_VID	0x0464	W	0x00000000	Vendor ID Register
KEYLAD_KD_MODE	0x0468	W	0x00000000	The Cipher and Enc/dec Type in Root Key Derivation
KEYLAD_INTER_COPY	0x0608	W	0x00000000	Inter Copy Control Register
KEYLAD_KEY_SEL	0x0610	W	0x00000000	Key Select Register
KEYLAD_LOCKSTEP	0x0618	W	0x00000000	Lock Step Status Register
KEYLAD_LOCKSTEP_EN	0x061C	W	0x00000000	Lock Step Enable Register
KEYLAD_OTP_KEY_REQ	0x0640	W	0x00000000	OTP Key Request Register
KEYLAD_KEY_CLEAR	0x0644	W	0x00000000	Clear Keytable's Data
KEYLAD_OTP_KEY_LEN	0x0648	W	0x00000000	OTP Key Length Register
KEYLAD_HW_DRNG_REQ	0x064C	W	0x00000000	Random Number Request Register
KEYLAD_AES_VERSION	0x0680	W	0x00071003	AES_VERSION
KEYLAD_DES_VERSION	0x0684	W	0x00070003	DES_VERSION
KEYLAD_SM4_VERSION	0x0688	W	0x00000000	SM4_VERSION

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Name	Offset	Size	Reset Value	Description
KEYLAD_HASH_VERSION	0x068C	W	0x00000000	HASH_VERSION
KEYLAD_HMAC_VERSION	0x0690	W	0x00000000	HMAC_VERSION
KEYLAD_PKA_VERSION	0x0698	W	0x00000000	PKA_VERSION
KEYLAD_EXTRA_FEATURE	0x069C	W	0x00000002	Extra Feature Register
KEYLAD_CRYPTO_VERSION	0x06F0	W	0x04000003	CRYPTO_VERSION

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

29.4.3 Detail Registers Description

KEYLAD_CLK_CTL

Address: Operational Base(0xFF8B0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	auto_clkgate_en CRYPTO will gate unused Block Cipher and HASH module automatically 1'b0: Disable 1'b1: Enable

KEYLAD_RST_CTL

Address: Operational Base(0xFF8B0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	R/WSC	0x0	sw_cc_reset Software set this bit to start a reset to Symmetric Cipher and HASH module. After the reset is done, CRYPTO will clear this bit.

KEYLAD_DMA_INT_EN

Address: Operational Base(0xFF8B0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	unequal_len_int_en 1'b0: Disable 1'b1: Enable
8:7	RO	0x0	reserved
6	RW	0x0	zero_len_int_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	list_err_int_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	src_err_int_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	dst_err_int_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	src_item_done_int_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	dst_item_done_int_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	list_done_int_en 1'b0: Disable 1'b1: Enable

KEYLAD_DMA_INT_ST

Address: Operational Base(0xFF8B0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	unequal_len 1'b0: Nothing 1'b1: indicate that DMA has met an unequal transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use
8:7	RO	0x0	reserved
6	RW	0x0	zero_len 1'b0: Nothing 1'b1: Indicate that DMA has met an 0 byte source transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use
5	RW	0x0	list_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer list descriptors. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
4	W1C	0x0	src_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer source data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
3	W1C	0x0	dst_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer destination data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
2	W1C	0x0	src_item_done 1'b0: Nothing 1'b1: Indicate that DMA has completed a read transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use

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Bit	Attr	Reset Value	Description
1	W1C	0x0	dst_item_done 1'b0: Nothing 1'b1: Indicate that DMA has completed a write transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use
0	W1C	0x0	list_done 1'b0: Nothing 1'b1: Indicate that DMA has completed all the transfers which the list descriptors pointed to. After the bit is read, the application should write 1 to clear this bit for next time use

KEYLAD_DMA_CTL

Address: Operational Base(0xFF8B0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	R/WSC	0x0	dma_start DMA asserts the bit to start DMA transfer, then Crypto will clear the bit automatically.

KEYLAD_DMA_LLI_ADDR

Address: Operational Base(0xFF8B0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_lli_addr When DMA_CTL start asserted, Crypto will read the address to get the 1'st descriptor. It should be 8-bytes align. We suggest dma_lli_addr 64-byte align for best performance consideration.

KEYLAD_DMA_ST

Address: Operational Base(0xFF8B0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	dma_busy 1'b1: DMA busy 1'b0: DMA idle

KEYLAD_DMA_STATE

Address: Operational Base(0xFF8B0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RO	0x0	dma_lli_state For debug use only 2'b00: IDLE STATE 2'b01: FETCH STATE 2'b10: WORK STATE Others: Reserved

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Bit	Attr	Reset Value	Description
3:2	RO	0x0	dma_src_state For debug use only 2'b00: IDLE STATE 2'b01: LOAD STATE 2'b10: WORK STATE Others: Reserved
1:0	RO	0x0	dma_dst_state For debug use only 2'b00: IDLE STATE 2'b01: LOAD STATE 2'b10: WORK STATE Others: Reserved

KEYLAD_DMA_LLI_RADDR

Address: Operational Base(0xFF8B0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_lli_raddr For debug use only It indicates the current DMA lli read address

KEYLAD_DMA_SRC_RADDR

Address: Operational Base(0xFF8B0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_src_raddr For debug use only. It represents the value of the current DMA source read address shifted EXTRA_FEATURE.axi_expand_bit bits to the right

KEYLAD_DMA_DST_WADDR

Address: Operational Base(0xFF8B0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_dst_waddr For debug use only. It represents the value of the current DMA destination write address shifted EXTRA_FEATURE.axi_expand_bit bits to the right

KEYLAD_DMA_ITEM_ID

Address: Operational Base(0xFF8B0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	dma_item_id For debug use only It indicates the current descriptor ID

KEYLAD_FIFO_CTL

Address: Operational Base(0xFF8B0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	write_enable Write enable for lower 2bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
17:2	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	dout_byteswap 1'b0: Little endian 1'b1: Big endian
0	RW	0x1	din_byteswap 1'b0: Little endian 1'b1: Big endian

KEYLAD_BC_CTL

Address: Operational Base(0xFF8B0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	WO	0x000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	bc_cipher_sel 2'b00: AES 2'b01: SM4 2'b10: DES 2'b11: TDES Others: Reserved Note: The algorithm mode actually supported is subject to XXX_VERSION(XXX can be AES, DES, SM4)
7:4	RW	0x0	mode For AES 4'h0: ECB 4'h1: CBC 4'h2: CTS 4'h3: CTR 4'h4: CFB 4'h5: OFB 4'h6: XTS 4'h7: CCM 4'h8: GCM 4'h9: CMAC 4'hA: CBC-MAC Others: Reserved For TDES/DES 4'h0: ECB 4'h1: CBC 4'h4: CFB 4'h5: OFB Others: Reserved 4'hf: through Note: The algorithm mode actually supported is subject to XXX_VERSION(XXX can be AES, DES, SM4)
3:2	RW	0x0	key_size For AES 2'b00: 128 bit 2'b01: 192 bit 2'b10: 256 bit 2'b11: Reserved For TDES/DES, it is reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	decrypt 1'b0: Encrypt 1'b1: Decrypt
0	RW	0x0	bc_enable 1'b0: Disable 1'b1: Enable

KEYLAD_CIPHER_ST

Address: Operational Base(0xFF8B0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	hash_busy 1'b0: IDLE 1'b1: BUSY
0	RO	0x0	block_cipher_busy 1'b0: IDLE 1'b1: BUSY

KEYLAD_CIPHER_STATE

Address: Operational Base(0xFF8B0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:10	RO	0x01	hash_state For debug use only 5'h01: IDLE State 5'h02: IPAD State 5'h04: TEXT State 5'h08: OPAD State 5'h10: OPAD EXT State
9:8	RO	0x0	gcm_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: NA State 2'b11: PC State
7:6	RO	0x0	ccm_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: NA State 2'b11: PC State
5:4	RO	0x0	parallel_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State Others: Reserved
3:2	RO	0x0	mac_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State Others: Reserved

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Bit	Attr	Reset Value	Description
1:0	RO	0x0	serial_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State 2'b11: Reserved

KEYLAD_CH0_IV_0

Address: Operational Base(0xFF8B0000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_iv_0 Channel 0 IV[127:96].

KEYLAD_CH0_IV_1

Address: Operational Base(0xFF8B0000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_iv_1 Channel 0 IV[95:64].

KEYLAD_CH0_IV_2

Address: Operational Base(0xFF8B0000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_iv_2 Channel 0 IV[63:32].

KEYLAD_CH0_IV_3

Address: Operational Base(0xFF8B0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_iv_3 Channel 0 IV[31:0].

KEYLAD_APB_CMD

Address: Operational Base(0xFF8B0000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	apb_cmd_en Apb master command enable: 1'b0: Disable 1'b1: Enable After write is completed, the hardware automatically clears.

KEYLAD_APB_PADDR

Address: Operational Base(0xFF8B0000) + offset (0x0454)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	apb_paddr Where to write out. The address unit is Byte.

KEYLAD_APB_PWDATA

Address: Operational Base(0xFF8B0000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	apb_pwdata Choose which 32 bits data in key table will be write out. 5'h0: Choose key_tab[31:0]; 5'h1: Choose key_tab[63:32]; 5'hn: Choose key_tab[(n*32+31):(n*32)]. The address unit is Word.

KEYLAD_DATA_CTL

Address: Operational Base(0xFF8B0000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	klad_data_en Whether to enable KEY register inside IP as the cipher operation data 1'b0: Disable 1'b1: Enable when enable, IP choose data source according to the value of KLAD_KEY_SEL, When KLAD_KEY_SEL=2, select klad_k2 as data When KLAD_KEY_SEL=1, select klad_k1 as data When KLAD_KEY_SEL=0 or 0x5a5a5a5a, select keytable as data
14:0	RO	0x0000	reserved

KEYLAD_KD_VID

Address: Operational Base(0xFF8B0000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	vendor_id Set vendor ID, length 16bit

KEYLAD_KD_MODE

Address: Operational Base(0xFF8B0000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	frkd_dec 1'b0: Encrypt 1'b1: Decrypt
13:12	RW	0x0	frkd_alg Bc_cipher_sel 2'b00: AES 2'b01: SM4 2'b10: DES 2'b11: TDES
11	RO	0x0	reserved
10	RW	0x0	vsf_dec 1'b0: Encrypt 1'b1: Decrypt
9:8	RW	0x0	vsf_alg Bc_cipher_sel 2'b00: AES 2'b01: SM4 2'b10: DES 2'b11: TDES
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	psck_dec 1'b0: Encrypt 1'b1: Decrypt
5:4	RW	0x0	psck_alg Bc_cipher_sel 2'b00: AES 2'b01: SM4 2'b10: DES 2'b11: TDES
3	RO	0x0	reserved
2	RW	0x0	esck_re_dec 1'b0: Encrypt 1'b1: Decrypt
1:0	RW	0x0	esck_re_alg Bc_cipher_sel 2'b00: AES 2'b01: SM4 2'b10: DES 2'b11: TDES

KEYLAD_INTER_COPY

Address: Operational Base(0xFF8B0000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31	RW	0x0	inter_copy_en Internal key copy enable: 1'b0: Disable 1'b1: Enable After copy is completed, the hardware automatically clears. The operation address unit is Word.
30:21	RO	0x000	reserved
20:16	RW	0x00	inter_copy_des_addr OTP key copy des address. After copy is completed, the hardware automatically clears. The operation address unit is Word.
15:5	RO	0x000	reserved
4:0	RW	0x00	inter_copy_src_addr OTP key copy src address. After copy is completed, the hardware automatically clears. The operation address unit is Word.

KEYLAD_KEY_SEL

Address: Operational Base(0xFF8B0000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31	RW	0x0	klad_kl_high_sel 1'b0: Big endian 1'b1: Little endian
30:3	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	klad_kl_key_sel Select the key source to use, and determined the destination 3'h3: Source reg: klad_k3 ----destination reg: klad_k2; 3'h2: Source reg: klad_k2 ----destination reg: when KLAD_DATA_CTL.bit15=0: klad_k1 when KLAD_DATA_CTL.bit15=1: klad_a; 3'h1: Source reg: klad_k1 ----destination reg: when KLAD_DATA_CTL.bit15=0: key_table(The address is specified by lli) when KLAD_DATA_CTL.bit15=1: klad_a; 3'h4: Source reg: klad_a ----destination: MEM(The address is specified by lli); Others: Invalid When [30:0] is set to 0x5a5a5a5a or 0x0, this register all as 0x0, key source and key destination are all key table0.

KEYLAD_LOCKSTEP

Address: Operational Base(0xFF8B0000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	lock_step_flag Lock step status: 1'b0: No mistake 1'b1: Mistake happened

KEYLAD_LOCKSTEP_EN

Address: Operational Base(0xFF8B0000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	lockstep_en 1'b0: Disable 1'b1: Enable Note: Whether the lockstep_en takes effect depends on whether this IP has the function of lockstep described in register XXX_VERSION(XXX can be AES, DES, SM4, HASH, HMAC)

KEYLAD_OTP_KEY_REQ

Address: Operational Base(0xFF8B0000) + offset (0x0640)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	otp_key_addr OTP key offset address. The address unit is 2B. After read is completed, the hardware automatically clears.
15:9	RO	0x00	reserved
8	RW	0x0	otp_key_req OTP key read requst. After read is completed, the hardware automatically clears.
7:6	RO	0x0	reserved
5	RW	0x0	word_endian 1'b0: Stays the same 1'b1: In reverse order Reverse 8 Word order, not related to OTP_KEY_LEN. After read is completed, the hardware automatically clears.

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Bit	Attr	Reset Value	Description
4	RW	0x0	byte_endian 1'b0: Stays the same 1'b1: In reverse order Reverse 4B order in each Word. After read is completed, the hardware automatically clears.
3:1	RO	0x0	reserved
0	RW	0x0	otp_key_dst_addr OTP key copy des address. The address unit is 8 Word. After read is completed, the hardware automatically clears.

KEYLAD_KEY_CLEAR

Address: Operational Base(0xFF8B0000) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	klad_key_clear_req Write 0x1 to begin clearing. After the key table data is cleared, the hardware clears the register automatically

KEYLAD_OTP_KEY_LEN

Address: Operational Base(0xFF8B0000) + offset (0x0648)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	otp_key_len The unit is Byte, when it is greater than 32, the hardware assigns it to 32.

KEYLAD_HW_DRNG_REQ

Address: Operational Base(0xFF8B0000) + offset (0x064C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	hw_drng_req Hardware DRNG requst. After read is completed, the hardware automatically clears.
7:1	RO	0x00	reserved
0	RW	0x0	hw_drng_dst_addr Hardware DRNG copy destination address. The address unit is 8 Word. After read is completed, the hardware automatically clears.

KEYLAD_AES_VERSION

Address: Operational Base(0xFF8B0000) + offset (0x0680)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	multichannel_flag Whether the AES supports multichannel 1'b0: No support 1'b1: Support
21	RW	0x0	secure_flag Whether the AES supports anti-side channel attack 1'b0: No support 1'b1: Support

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Bit	Attr	Reset Value	Description
20	RW	0x0	lockstep_flag Whether the AES supports lockstep 1'b0: No support 1'b1: Support
19	RO	0x0	reserved
18	RO	0x1	aes256_flag Whether the AES supports AES256 1'b0: No support 1'b1: Support
17	RO	0x1	aes192_flag Whether the AES supports AES192 1'b0: No support 1'b1: Support
16	RO	0x1	aes128_flag Whether the AES supports AES128 1'b0: No support 1'b1: Support
15:13	RO	0x0	reserved
12	RO	0x1	bypass Whether IP supports data bypass 1'b0: No support 1'b1: Support
11	RO	0x0	reserved
10	RO	0x0	cbc-mac_flag Whether the AES supports CBC-MAC 1'b0: No support 1'b1: Support
9	RO	0x0	cmac_flag Whether the AES supports CMAC 1'b0: No support 1'b1: Support
8	RO	0x0	gcm_flag Whether the AES supports GCM 1'b0: No support 1'b1: Support
7	RO	0x0	ccm_flag Whether the AES supports CCM 1'b0: No support 1'b1: Support
6	RO	0x0	xts_flag Whether the AES supports XTS 1'b0: No support 1'b1: Support
5	RO	0x0	ofb_flag Whether the AES supports OFB 1'b0: No support 1'b1: Support
4	RO	0x0	cfb_flag Whether the AES supports CFB 1'b0: No support 1'b1: Support
3	RO	0x0	ctr_flag Whether the AES supports CTR 1'b0: No support 1'b1: Support

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Bit	Attr	Reset Value	Description
2	RO	0x0	cts_flag Whether the AES supports CTS 1'b0: No support 1'b1: Support
1	RO	0x1	cbc_flag Whether the AES supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the AES supports ECB 1'b0: No support 1'b1: Support

KEYLAD_DES_VERSION

Address: Operational Base(0xFF8B0000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	multichannel_flag Whether the DES supports multichannel 1'b0: No support 1'b1: Support
21	RW	0x0	secure_flag Whether the DES supports anti-side channel attack 1'b0: No support 1'b1: Support
20	RW	0x0	lockstep_flag Whether the DES supports lockstep 1'b0: No support 1'b1: Support
19	RO	0x0	reserved
18	RW	0x1	ede_flag Whether the DES supports EDE mode 1'b0: No support 1'b1: Support
17	RO	0x1	eee_flag Whether the DES supports EEE mode 1'b0: No support 1'b1: Support
16	RO	0x1	tdes_flag Whether the DES supports TDES 1'b0: No support 1'b1: Support
15:6	RO	0x000	reserved
5	RO	0x0	ofb_flag Whether the DES supports OFB 1'b0: No support 1'b1: Support
4	RO	0x0	cfb_flag Whether the DES supports CFB 1'b0: No support 1'b1: Support
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x1	cbc_flag Whether the DES supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the DES supports ECB 1'b0: No support 1'b1: Support

KEYLAD_SM4_VERSION

Address: Operational Base(0xFF8B0000) + offset (0x0688)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	multichannel_flag Whether the SM4 supports multichannel 1'b0: No support 1'b1: Support
21	RW	0x0	secure_flag Whether the SM4 supports anti-side channel attack 1'b0: No support 1'b1: Support
20	RW	0x0	lockstep_flag Whether the SM4 supports lockstep 1'b0: No support 1'b1: Support
19:11	RO	0x000	reserved
10	RO	0x0	cbc-mac_flag Whether the SM4 supports CBC-MAC 1'b0: No support 1'b1: Support
9	RO	0x0	cmac_flag Whether the SM4 supports CMAC 1'b0: No support 1'b1: Support
8	RO	0x0	gcm_flag Whether the SM4 supports GCM 1'b0: No support 1'b1: Support
7	RO	0x0	ccm_flag Whether the SM4 supports CCM 1'b0: No support 1'b1: Support
6	RO	0x0	xts_flag Whether the SM4 supports XTS 1'b0: No support 1'b1: Support
5	RO	0x0	ofb_flag Whether the SM4 supports OFB 1'b0: No support 1'b1: Support
4	RO	0x0	cfb_flag Whether the SM4 supports CFB 1'b0: No support 1'b1: Support

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Bit	Attr	Reset Value	Description
3	RO	0x0	ctr_flag Whether the SM4 supports CTR 1'b0: No support 1'b1: Support
2	RO	0x0	cts_flag Whether the SM4 supports CTS 1'b0: No support 1'b1: Support
1	RO	0x0	cbc_flag Whether the SM4 supports CBC 1'b0: No support 1'b1: Support
0	RO	0x0	ecb_flag Whether the SM4 supports ECB 1'b0: No support 1'b1: Support

KEYLAD_HASH_VERSION

Address: Operational Base(0xFF8B0000) + offset (0x068C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	lockstep_flag Whether the HASH supports lockstep 1'b0: No support 1'b1: Support
19:9	RO	0x000	reserved
8	RO	0x0	sm3_flag Whether the HASH supports SM3 1'b0: No support 1'b1: Support
7	RO	0x0	md5_flag Whether the HASH supports MD5 1'b0: No support 1'b1: Support
6	RO	0x0	sha512-256_flag Whether the HASH supports SHA-512/256 1'b0: No support 1'b1: Support
5	RO	0x0	sha512-224_flag Whether the HASH supports SHA-512/224 1'b0: No support 1'b1: Support
4	RO	0x0	sha512_flag Whether the HASH supports SHA-512 1'b0: No support 1'b1: Support
3	RO	0x0	sha384_flag Whether the HASH supports SHA-384 1'b0: No support 1'b1: Support
2	RO	0x0	sha256_flag Whether the HASH supports SHA-256 1'b0: No support 1'b1: Support

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Bit	Attr	Reset Value	Description
1	RO	0x0	sha224_flag Whether the HASH supports SHA-224 1'b0: No support 1'b1: Support
0	RO	0x0	sha1_flag Whether the HASH supports SHA-1 1'b0: No support 1'b1: Support

KEYLAD_HMAC_VERSION

Address: Operational Base(0xFF8B0000) + offset (0x0690)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	multichannel Whether the HMAC supports multichannel 1'b0: No support 1'b1: Support
21	RO	0x0	reserved
20	RW	0x0	lockstep_flag Whether the HMAC supports lockstep 1'b0: No support 1'b1: Support
19:5	RO	0x0000	reserved
4	RO	0x0	sm3_flag Whether the HMAC supports SM3 1'b0: No support 1'b1: Support
3	RO	0x0	md5_flag Whether the HMAC supports MD5 1'b0: No support 1'b1: Support
2	RO	0x0	sha512_flag Whether the HMAC supports SHA-512 1'b0: No support 1'b1: Support
1	RO	0x0	sha256_flag Whether the HMAC supports SHA-256 1'b0: No support 1'b1: Support
0	RO	0x0	sha1_flag Whether the HMAC supports SHA-1 1'b0: No support 1'b1: Support

KEYLAD_PKA_VERSION

Address: Operational Base(0xFF8B0000) + offset (0x0698)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pka_version_code PKA version_code is 0x0000_0000.

KEYLAD_EXTRA_FEATURE

Address: Operational Base(0xFF8B0000) + offset (0x069C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:0	RO	0x2	axi_expand_bit AXI Address extension width.

KEYLAD_CRYPTO_VERSION

Address: Operational Base(0xFF8B0000) + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x04000003	crypto_version_code CRYPTO version_code is 0x0400_0003.

29.5 Application Notes

29.5.1 Usage of KEY TABLE

- Read key from OTP to KEY TABLE (OTP -> KEY TABLE)
  - Configure OTP_KEY_LEN to set the key length of the OTP request
  - Configure OTP_KEY_REQ to set the source address, destination address of the OTP request
  - Wait for OTP_KEY_REQ auto clear, which means key reading is completed
- Read random number from RKRNG to KEY TABLE(RKRNG -> KEY TABLE)
  - Configure HW_DRNG_REQ to set the destination of the DRNG request
  - Wait for HW_DRNG_REQ auto clear, which means random number reading is completed
- Write CIPHER result to KEY TABLE (CIPHER -> KEY TABLE)
  - When KEYLAD calling cipher core to do symmetric encryption, the calculation result will write to KEY TABLE
  - The write address in KEY TABLE is determine by the destination address in LLI mod 0x40
- Copy data within KEY TABLE (KEY TABLE -> KEY TABLE)
  - Configure INTER_COPY to set the source address, destination address and the enable of inter copy, the address unit is word
  - Wait for INTER_COPY auto clear, which means data copy is completed
- Write data in KEY TABLE to specific module (KEY TABLE -> specific module)
  - Configure APB_PWDATA to set the source address in KEY TABLE
  - Configure APB_PADDR to set the destination address, when address base set to 0xfe420000, the destination module is SCRYPTO's KEY TBALE
  - Configure APB_CMD to enable the transfer
  - Wait for APB_CMD auto clear, which means the transfer is completed

29.5.2 Root Key Derivation

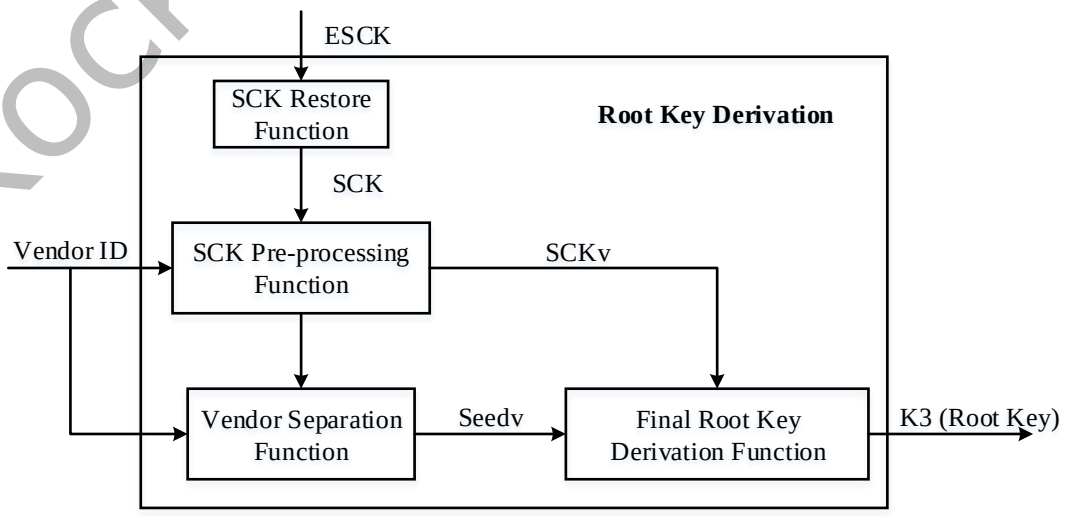

Fig. 29-2 Root Key Derivation Flow

When the source address of OTP request is set to a specific value, which means the key

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read back must be calculate with restore function and root key derivation function to get the final key. The specific value is 0xff00 in RK3562. So set OTP_KEY_REQ to 0xff000100, and KEYLAD will auto perform root key derivation.

- Configure BC_CTL as 0xffff0000
- Configure KD_VID to set the Vendor ID
- Configure KD_MODE to set the algorithm and encryption mode
- Configure OTP_KEY_LEN to set key length
- Configure OTP_KEY_REQ as 0xff000100 to enable root key derivation
- Wait for OTP_KEY_REQ auto clear, which means root key derivation is completed, and the K3 is stored at special register KD_K3

29.5.3 Key Ladder Calculation

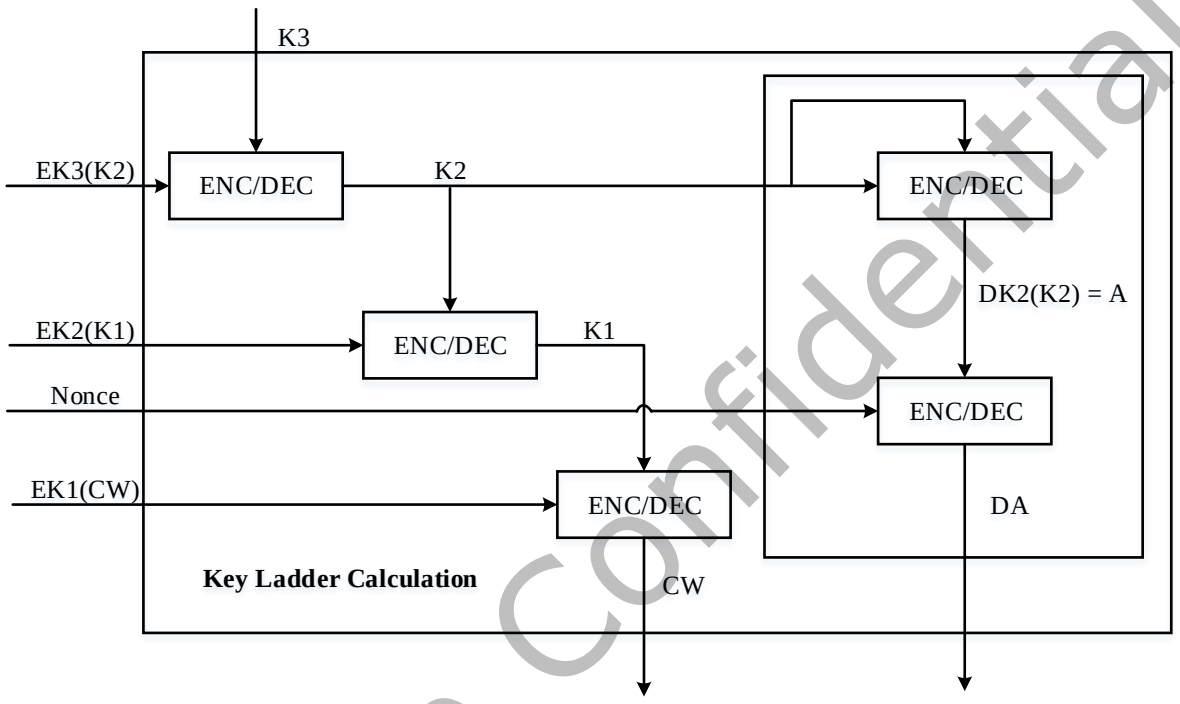

Fig. 29-3 Key Ladder Calculation Flow

Use key read from OTP as K3 directly.

- Generating K2
  - Configure OTP_KEY_LEN and OTP_KEY_REQ to request OTP key, store key to KEY TABLE as K3
  - Configure KEY_SEL as 0x5a5a5a5a to select K3 in KEY TABLE as cipher key
  - Configure BC_CTL to choose algorithm and encryption mode
  - Configure DMA_LLI_ADDR to set the LLI address
  - Configure DMA_INT_EN to set interrupt enable
  - Configure DMA_CTL to start DMA transfer and begin to calculate K2
  - Wait for Klad_interrupt set, which means K2 calculation is completed, and K2 is written to KEY TABLE
- Generating K1
  - Configure KEY_SEL as 0x5a5a5a5a to select K2 in KEY TABLE as cipher key
  - Configure BC_CTL to choose algorithm and encryption mode
  - Configure DMA_LLI_ADDR to set the LLI address
  - Configure DMA_INT_EN to set interrupt enable
  - Configure DMA_CTL to start DMA transfer and begin to calculate K1
  - Wait for Klad_interrupt set, which means K1 calculation is completed, and K1 is written to KEY TABLE
- Generating CW
  - Configure KEY_SEL as 0x5a5a5a5a to select K1 in KEY TABLE as cipher key
  - Configure BC_CTL to choose algorithm and encryption mode
  - Configure DMA_LLI_ADDR to set the LLI address
  - Configure DMA_INT_EN to set interrupt enable

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    - Configure DMA_CTL to start DMA transfer and begin to calculate CW
    - Wait for Klad_interrupt set, which means CW calculation is completed, and CW is written to KEY TABLE
- Generating A
    - Configure KEY_SEL as 0x5a5a5a5a to select K2 in KEY TABLE as cipher key
    - Configure DATA_CTL to set 0x00008000 to select K2 in KEY TABLE as cipher data
    - Configure BC_CTL to choose algorithm and encryption mode
    - Configure DMA_LLI_ADDR to set the LLI address
    - Configure DMA_INT_EN to set interrupt enable
    - Configure DMA_CTL to start DMA transfer and begin to calculate A
    - Wait for Klad_interrupt set, which means A calculation is completed, and A is written to KEY TABLE
- Generating DA
    - DA should be calculated by SCRYPTO, so before calculating DA, it's necessary to copy A from KEYLAD's KEY TABLE to SCRYPTO's KEY TABLE
    - Configure APB_PWDATA, APB_PADDR, APB_CMD to copy A to SCRYPTO's KEY TABLE
    - Configure KEY_SEL as 0x5a5a5a5a to select A in KEY TABLE as cipher key
    - Configure BC_CTL to choose algorithm and encryption mode
    - Configure DMA_LLI_ADDR to set the LLI address
    - Configure DMA_INT_EN to set interrupt enable
    - Configure DMA_CTL to start DMA transfer and begin to calculate DA
    - Wait for SC_interrupt set, which means DA calculation is completed, and DA is written out by AXI master

In this case, K2, K1, CW, A are calculated by KEYLAD, so the address base of registers is KEYALD base. DA is calculated by SCRYPTO, so the address base of registers is SCRYPTO base, except for registers related to APB_*.

Use key after root key derivation as K3

- Generating K3
    - Configure OTP_KEY_LEN and OTP_KEY_REQ to request OTP key, and perform root key derivation to generate K3
    - K3 is store at special register KD_K3
- Generating K2
    - Configure KEY_SEL as 0x3 to select K3 in KD_K3 as cipher key
    - Configure BC_CTL to choose algorithm and encryption mode
    - Configure DMA_LLI_ADDR to set the LLI address
    - Configure DMA_INT_EN to set interrupt enable
    - Configure DMA_CTL to start DMA transfer and begin to calculate K2
    - Wait for Klad_interrupt set, which means K2 calculation is completed, and K2 is written to special register KD_K2
- Generating K1
    - Configure KEY_SEL as 0x2 to select K2 in KD_K2 as cipher key
    - Configure BC_CTL to choose algorithm and encryption mode
    - Configure DMA_LLI_ADDR to set the LLI address
    - Configure DMA_INT_EN to set interrupt enable
    - Configure DMA_CTL to start DMA transfer and begin to calculate K1
    - Wait for Klad_interrupt set, which means K1 calculation is completed, and K1 is written to special register KD_K1
- Generating CW
    - Configure KEY_SEL as 0x1 to select K1 in KD_K1 as cipher key
    - Configure BC_CTL to choose algorithm and encryption mode
    - Configure DMA_LLI_ADDR to set the LLI address
    - Configure DMA_INT_EN to set interrupt enable
    - Configure DMA_CTL to start DMA transfer and begin to calculate CW
    - Wait for Klad_interrupt set, which means CW calculation is completed, and CW is written to KEY TABLE
- Generating A

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  - Configure KEY_SEL as 0x2 to select K2 in KD_K2 as cipher key
  - Configure DATA_CTL to set 0x00008000 to select K2 in KD_K2 as cipher data
  - Configure BC_CTL to choose algorithm and encryption mode
  - Configure DMA_LLI_ADDR to set the LLI address
  - Configure DMA_INT_EN to set interrupt enable
  - Configure DMA_CTL to start DMA transfer and begin to calculate A
  - Wait for Klad_interrupt set, which means A calculation is completed, and A is written to special register KD_A
- Generating DA
  - Configure KEY_SEL as 0x4 to select A in KD_A as cipher key
  - Configure FIFO_CTL(offset is 0x40) as 0x000c0003 to set the output of AXI in big endian
  - Configure BC_CTL to choose algorithm and encryption mode
  - Configure DMA_LLI_ADDR to set the LLI address
  - Configure DMA_INT_EN to set interrupt enable
  - Configure DMA_CTL to start DMA transfer and begin to calculate DA
  - Wait for Klad_interrupt set, which means DA calculation is completed, and DA is written out by AXI master

In this case, K3, K2, K1, CW, A, DA are all calculated by KEYLAD, so the address base is KEYLAD base. Note that when calculate DA, it necessary to configure FIFO_CTL to change the endian of AXI output. If not, application must change the endian of DA by yourself.

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Chapter 30 True Random Number Generator(TRNG)

30.1 Overview

TRNG is a true random number generator to generate random number:

- A 32 bits AHB slave
- The generated random number length can be configured as 64bits 128bits, 192bits and 256 bits
- OSC is available in four lengths
- The sampling period for random number per bit is available

30.2 Block Diagram

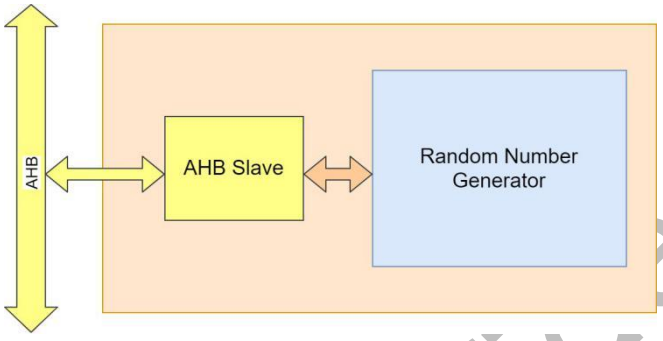

Fig. 30-1 TRNG Block Diagram

TRNG is comprised of:

- AHB Slave

The AHB slave implements the AHB slave operation. Its data bus width is 32 bits.

- Random Number Generator

The Random Number Generator generate true random number according to register configuration.

30.3 Function Description

30.3.1 Operation

- **True random number generate**

User first configures the RNG_SAMPLE_CNT and RNG_CTL register, excluding the rng_start field of the RNG_CTL register. The rng_start field of the RNG_CTL register is then finally configured to start the random number generation. Wait until the rng_start field of the RST_CTL register reads out a value of 0, which indicates that the random number is generated.

- **Reset operation**

User write 0x00020002 to RST_CTL register. Then, wait until the RST_CTL register reads out a value of 0. After these operations, TRNG clear RNG_DOUT and the internal state.

30.4 Register Description

30.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
TRNG_NS	0xFF8F0000
RKRNG_S	0xFF8D0000

30.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TRNG_CTRL	0x0000	W	0x00000000	Command control.
TRNG_MODE	0x0008	W	0x00000008	Random number length.
TRNG_IE	0x0010	W	0x00000000	Interrupt enable.

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Name	Offset	Size	Reset Value	Description
TRNG_ISTAT	0x0014	W	0x00000000	Interrupt state.
TRNG_RAND0	0x0020	W	0x00000000	Random number 0.
TRNG_RAND1	0x0024	W	0x00000000	Random number 1.
TRNG_RAND2	0x0028	W	0x00000000	Random number 2.
TRNG_RAND3	0x002C	W	0x00000000	Random number 3.
TRNG_RAND4	0x0030	W	0x00000000	Random number 4.
TRNG_RAND5	0x0034	W	0x00000000	Random number 5.
TRNG_RAND6	0x0038	W	0x00000000	Random number 6.
TRNG_RAND7	0x003C	W	0x00000000	Random number 7.
TRNG_VERSION	0x00F0	W	0x00000000	TRNG VERSION.

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

30.4.3 Detail Registers Description

TRNG_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	CMD Execute a command 3'b000: Execute a NOP 3'b001: Generate a random number 3'b010: Execute a random reseed

TRNG_MODE

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x1	R256 Current length for PRNG RANDx registers 1'b0: PRNG set up for 128-bit maximum 1'b1: PRNG set up for 256-bit maximum
2:0	RO	0x0	reserved

TRNG_IE

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	GLBL_EN Global interrupt enable 1'b0: Globally disable interrupts 1'b1: Globally enable interrupts
30:2	RO	0x00000000	reserved
1	RW	0x0	SEED_DONE_EN Include or exclude SEED_DONE interrupt contribution 1'b0: Disable SEED_DONE interrupt contribution 1'b1: Enable SEED_DONE interrupt contribution
0	RW	0x0	RAND_RDY_EN Include or exclude RAND_RDY interrupt contribution 1'b0: Disable RAND_RDY interrupt contribution 1'b1: Enable RAND_RDY interrupt contribution

TRNG_ISTAT

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	W1C	0x0	SEED_DONE Status and acknowledgment (clearing) of SEED_DONE indicator 1'b0(SEED_DONE_R0): No unacknowledged SEED_DONE indicator 1'b1(SEED_DONE_R1): Unacknowledged SEED_DONE indicator 1'b0(SEED_DONE_W0): NOP 1'b1(SEED_DONE_W1): Acknowledge SEED_DONE indicator
0	W1C	0x0	RAND_RDY Status and acknowledgment (clearing) of RAND_RDY indicator 1'b0(RAND_RDY_R0): No unacknowledged RAND_RDY indicator 1'b1(RAND_RDY_R1): Unacknowledged RAND_RDY indicator 1'b0(RAND_RDY_W0): NOP 1'b1(RAND_RDY_W1): Acknowledge RAND_RDY indicator

TRNG_RAND0

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RAND Random data word 0.

TRNG_RAND1

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RAND Random data word 1.

TRNG_RAND2

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RAND Random data word 2.

TRNG_RAND3

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RAND Random data word 3.

TRNG_RAND4

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RAND Random data word 4.

TRNG_RAND5

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RAND Random data word 5.

TRNG_RAND6

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RAND Random data word 6.

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TRNG_RAND7

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RAND Random data word 7.

TRNG_VERSION

Address: **Operational Base** + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	version_code Version code is 0x46bc.

30.5 Application Notes

- When random numbers do not meet randomness requirements, user can resolve the problem by adjusting the RNG_SAMPLE_CNT register and ring_sel field of RNG_CTL register.

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Chapter 31 Random Number Generator(RKRNG)

31.1 Overview

Random Number Generator is used to generate random number for IP which need random number. It consists of True Random Number Generator (TRNG) and Deterministic Random Number Generator (DRNG). The entropy source generated by TRNG can be used as random number directly, and can also be used as the input entropy of DRNG.
RKRNG supports the following features:

- Two AHB slave interfaces
  - AHB_S is used for configure RNG IP and request the data of TRNG and DRNG
  - AHB_NS is only used for request the data of TRNG and DRNG
- TRNG
  - Support configure the length of oscillating ring
  - Support monitor the status of work clock, and switch on/off internal work clock
  - Support 32 switchable and length configurable CRO oscillating rings
  - Support 2 switchable and initial value configurable STR oscillating rings
  - Support entropy enhancement to original entropy source by XOR or von Neumann processing
  - Support frequency checking, can check original entropy and enhanced entropy both
  - Support itinerary checking, can check original entropy and enhanced entropy both
  - Support longest itinerary checking within a block, can check original entropy and enhanced entropy both
  - Support variance checking, can check original entropy only
- DRNG
  - Support generate pseudo random number by AES-CTR algorithm without derived function
  - Support AES-128/AES-192/AES-256
  - Support auto healthy detect after hardware/software reset
  - Support auto generate random number after healthy detect success, and output warning signal after healthy detect fail
  - Support request instantiation operation by software
  - Support request healthy detect by software, and support operate healthy detect by hardware regularly
  - Support request reseed operation by software, and support operate reseed by hardware regularly
  - Support request random number by software/hardware, and the random number is different between software and hardware request
  - Support anti-prediction function

31.2 Block Diagram

RKRNG is comprised of:

- NSIF: Non-secure AHB Slave Interface
- SIF: Secure AHB Slave Interface
- TRNG: True Random Number Generator
- DRNG: Deterministic Random Number Generator
- HDL: Healthy Detect Logic

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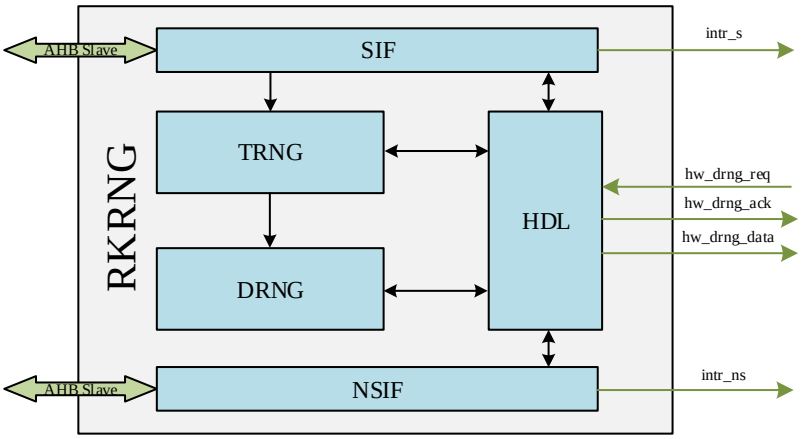

Fig. 31-1 RKRNG Block Diagram

31.3 Function Description

31.3.1 AHB Interface

There are two AHB slave interface in RKRNG, NSIF is used for non-secure world, and SIF is used for secure world. RNG is only configurable by SIF in secure world. The data of TRNG or DRNG are both accessible by SIF in secure world and NSIF in non-secure world. And hardware will ensure the difference of data in two worlds.

31.3.2 TRNG

TRNG has two entropy sources, one is CRO oscillating ring, the other one is STR oscillating ring. The CRO oscillating ring is switchable and length configurable, The STR oscillating ring is switchable and initial value configurable. The output of the oscillating ring which means original entropy can be performed entropy enhance by XOR or von Neumann processing. Several check functions, such as frequency check, itinerary check, block itinerary check and variance check, are support to ensure the quality of entropy.

31.3.3 DRNG

DRNG is a deterministic random number generator, which generate pseudo random number by AES-CTR algorithm without derived function. It supports three type of algorithms: AES-128/AES-192/AES-256.

31.3.4 HDL

HDL is healthy detect logic. It is not an individual module in hardware, but is implemented in TRNG and DRNG.

31.4 Register Description

31.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
RKRNG_NS	0xFF8E0000
RKRNG_S	0xFF8C0000

The register address ranges that can be used by RKRNG_NS is :0x10~x18, 0x50~0x8c.

31.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKRNG_CFG	0x0000	W	0x00000000	RNG Configuration Register
RKRNG_INV_NUM	0x0004	W	0x00000000	The number of inverters in each oscillating ring
RKRNG_NONCE_LEN	0x0008	W	0x00000000	NONCE Length Register
RKRNG_ADDITION_LEN	0x000C	W	0x00000000	ADDITION Length Register
RKRNG_CTRL	0x0010	W	0x00000000	RNG Control Register
RKRNG_STATE	0x0014	W	0x00000000	RNG Status Register

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Name	Offset	Size	Reset Value	Description
RKRNG_INT_EN	0x0018	W	0x00000000	Interrupt Enable Register
RKRNG_TEST_CNT	0x001C	W	0x00000200	Interval of auto test
RKRNG_RESEED_CNT	0x0020	W	0x00000400	Interval of auto reseed
RKRNG_UPDATE_CNT	0x0024	W	0x00000200	Interval of auto update
RKRNG_ALLAN_ACC_NUM	0x0028	W	0x00000000	The number of samples needed to calculate the variance
RKRNG_ALLAN_LIMIT_LOW	0x002C	W	0x00000000	Lower bound of variance
RKRNG_ALLAN_LIMIT_HIGH	0x0030	W	0x00000000	Lower bound of variance
RKRNG_ALLAN_AVAR_RESULT	0x0034	W	0x00000000	Variance result
RKRNG_AUTO_CLK_GATE	0x0038	W	0x00000001	Auto Gate Enable Register
RKRNG_DBG_SEL	0x0040	W	0x00000000	Divide enable of debug clock
RKRNG_TRNG_DATA_0	0x0050	W	0x00000000	TRNG data 0
RKRNG_TRNG_DATA_1	0x0054	W	0x00000000	TRNG data 1
RKRNG_TRNG_DATA_2	0x0058	W	0x00000000	TRNG data 2
RKRNG_TRNG_DATA_3	0x005C	W	0x00000000	TRNG data 3
RKRNG_TRNG_DATA_4	0x0060	W	0x00000000	TRNG data 4
RKRNG_TRNG_DATA_5	0x0064	W	0x00000000	TRNG data 5
RKRNG_TRNG_DATA_6	0x0068	W	0x00000000	TRNG data 6
RKRNG_TRNG_DATA_7	0x006C	W	0x00000000	TRNG data 7
RKRNG_DRNG_DATA_0	0x0070	W	0x00000000	DRNG data 0
RKRNG_DRNG_DATA_1	0x0074	W	0x00000000	DRNG data 1
RKRNG_DRNG_DATA_2	0x0078	W	0x00000000	DRNG data 2
RKRNG_DRNG_DATA_3	0x007C	W	0x00000000	DRNG data 3
RKRNG_DRNG_DATA_4	0x0080	W	0x00000000	DRNG data 4
RKRNG_DRNG_DATA_5	0x0084	W	0x00000000	DRNG data 5
RKRNG_DRNG_DATA_6	0x0088	W	0x00000000	DRNG data 6
RKRNG_DRNG_DATA_7	0x008C	W	0x00000000	DRNG data 7
RKRNG_WORK_CLK_EN	0x0090	W	0x00000001	TRNG Work Clock Enable Register
RKRNG_WORK_CLK_FLAG	0x0094	W	0x00000000	TRNG Work Clock Flag Register
RKRNG_WORK_CLK_NUM_LIMIT	0x0098	W	0x00000000	TRNG work clock no flip limit
RKRNG_SOFT_RING_EN0	0x009C	W	0x0000FFFF	Entropy Source Ring Enable Register 0
RKRNG_SOFT_RING_EN2	0x00A4	W	0x00000001	Entropy Source Ring Enable Register 2
RKRNG_STR1_0_INIT	0x00AC	W	0x00000000	STR1 Initial Value Register 0
RKRNG_ENTROPY_EN_CTL	0x00B8	W	0x000A6401	Entropy Source Enable Control Register
RKRNG_ENTROPY_MASK_CTL	0x00BC	W	0x00000011	Entropy Source Mask Control Register
RKRNG_ENTROPY_POST_CTL	0x00C0	W	0x00000000	Entropy Source Enhanced Post-processing Control Register
RKRNG_ENTROPY_CK_CTL	0x00C4	W	0x00000000	Entropy Source Check Control Register
RKRNG_ENTROPY_FB_LIMIT0	0x00C8	W	0x00000000	Entropy source frequency of bit limit 0
RKRNG_ENTROPY_FB_LIMIT1	0x00CC	W	0x00000000	Entropy source frequency of bit limit 1
RKRNG_ENTROPY_FI_BIT_NUM	0x00D0	W	0x00000000	Entropy source frequency of itinerary check bit length number

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Name	Offset	Size	Reset Value	Description
RKRNG_ENTROPY_FI_LIMIT	0x00D4	W	0x00000000	Entropy source frequency of itinerary check limit
RKRNG_ENTROPY_BI_CTL	0x00D8	W	0x00000000	Entropy source block statistical of itinerary check control
RKRNG_ENTROPY_BI_LIMIT_LOW0	0x00DC	W	0x00000000	Entropy source block statistical of itinerary check lower limit 0
RKRNG_ENTROPY_BI_LIMIT_LOW1	0x00E0	W	0x00000000	Entropy source block statistical of itinerary check lower limit 1
RKRNG_ENTROPY_BI_LIMITHIGH0	0x00E4	W	0x00000000	Entropy source block statistical of itinerary check higher limit 0
RKRNG_ENTROPY_BI_LIMIT_HIGH1	0x00E8	W	0x00000000	Entropy source block statistical of itinerary check higher limit 1
RKRNG_TRAND_CK_CTL	0x00EC	W	0x00000000	True Random Number Check Control Register
RKRNG_TRAND_FB_LIMIT0	0x00F0	W	0x00000000	True random number frequency of bit limit 0
RKRNG_TRAND_FB_LIMIT1	0x00F4	W	0x00000000	True random number frequency of bit limit 1
RKRNG_TRAND_FI_BIT_NUM	0x00F8	W	0x00000000	True random number frequency of itinerary check bit length number
RKRNG_TRAND_FI_LIMIT	0x00FC	W	0x00000000	True random number frequency of itinerary check limit
RKRNG_TRAND_BI_CTL	0x0100	W	0x00000000	True random number block statistical of itinerary check control
RKRNG_TRAND_BI_LIMIT_LOW0	0x0104	W	0x00000000	True random number block statistical of itinerary check lower limit 0
RKRNG_TRAND_BI_LIMIT_LOW1	0x0108	W	0x00000000	True random number block statistical of itinerary check lower limit 1
RKRNG_TRAND_BI_LIMIT_HIGH0	0x010C	W	0x00000000	True random number block statistical of itinerary check higher limit 0
RKRNG_TRAND_BI_LIMIT_HIGH1	0x0110	W	0x00000000	True random number block statistical of itinerary check higher limit 1
RKRNG_BI_PASS_AUTO	0x0114	W	0x00000001	Block statistical of itinerary check automatic pass through hardware check
RKRNG_SOFT_BI_RESULT_VLD	0x0118	W	0x00000000	Software block statistical of itinerary check result valid
RKRNG_SOFT_BI_RESULT_PASS	0x011C	W	0x00000000	Software block statistical of itinerary check result
RKRNG_ENTROPY_CK_RESULT_VLD	0x0120	W	0x00000000	Entropy source check result valid
RKRNG_ENTROPY_FB_CK_RESULT	0x0124	W	0x00000000	Entropy source frequency of bit check result
RKRNG_ENTROPY_FI_CK_RESULT	0x0128	W	0x00000000	Entropy source frequency of itinerary check result
RKRNG_ENTROPY_BI_CK_RESULT0	0x012C	W	0x00000000	Entropy source block statistical of itinerary check result 0
RKRNG_ENTROPY_BI_CK_RESULT1	0x0130	W	0x00000000	Entropy source block statistical of itinerary check result 1

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Name	Offset	Size	Reset Value	Description
RKRNG_TRAND_CK_RESULT_VLD	0x0134	W	0x00000000	Entropy source check result valid
RKRNG_TRAND_FB_CK_RESULT	0x0138	W	0x00000000	True random number frequency of bit check result
RKRNG_TRAND_FI_CK_RESULT	0x013C	W	0x00000000	True random number frequency of itinerary check result
RKRNG_TRAND_BI_CK_RESULT0	0x0140	W	0x00000000	True random number block statistical of itinerary check result 0
RKRNG_TRAND_BI_CK_RESULT1	0x0144	W	0x00000000	True random number block statistical of itinerary check result 1
RKRNG_NONCE_0	0x0200	W	0x00000000	NONCE 0
RKRNG_NONCE_1	0x0204	W	0x00000000	NONCE 1
RKRNG_NONCE_2	0x0208	W	0x00000000	NONCE 2
RKRNG_NONCE_3	0x020C	W	0x00000000	NONCE 3
RKRNG_NONCE_4	0x0210	W	0x00000000	NONCE 4
RKRNG_NONCE_5	0x0214	W	0x00000000	NONCE 5
RKRNG_NONCE_6	0x0218	W	0x00000000	NONCE 6
RKRNG_NONCE_7	0x021C	W	0x00000000	NONCE 7
RKRNG_NONCE_8	0x0220	W	0x00000000	NONCE 8
RKRNG_NONCE_9	0x0224	W	0x00000000	NONCE 9
RKRNG_NONCE_10	0x0228	W	0x00000000	NONCE 10
RKRNG_NONCE_11	0x022C	W	0x00000000	NONCE 11
RKRNG_ADDITION_0	0x0300	W	0x00000000	ADDITION 0
RKRNG_ADDITION_1	0x0304	W	0x00000000	ADDITION 1
RKRNG_ADDITION_2	0x0308	W	0x00000000	ADDITION 2
RKRNG_ADDITION_3	0x030C	W	0x00000000	ADDITION 3
RKRNG_ADDITION_4	0x0310	W	0x00000000	ADDITION 4
RKRNG_ADDITION_5	0x0314	W	0x00000000	ADDITION 5
RKRNG_ADDITION_6	0x0318	W	0x00000000	ADDITION 6
RKRNG_ADDITION_7	0x031C	W	0x00000000	ADDITION 7
RKRNG_ADDITION_8	0x0320	W	0x00000000	ADDITION 8
RKRNG_ADDITION_9	0x0324	W	0x00000000	ADDITION 9
RKRNG_ADDITION_10	0x0328	W	0x00000000	ADDITION 10
RKRNG_ADDITION_11	0x032C	W	0x00000000	ADDITION 11

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

31.4.3 Detail Registers Description

RKRNG_CFG

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	hash_df 0: No derived function 1: Has derived function
2	RW	0x0	pr_flag 0: Disable PredictionResistance 1: Enable PredictionResistance
1:0	RW	0x0	aes_key_size 2'b00: Aes128 2'b01: Aes192 2'b10: Aes256

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RKRNG_INV_NUM

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	inv_num 3'b000: Inverters num is 32 3'b001: Inverters num is 2 3'b010: Inverters num is 4 3'b011: Inverters num is 6 3'b100: Inverters num is 8 3'b101: Inverters num is 16 3'b110: Inverters num is 20 3'b111: Inverters num is 24

RKRNG_NONCE_LEN

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nonce_len Length of the nonce in bytes

RKRNG_ADDITION_LEN

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addition_len Length of the addition in bytes

RKRNG_CTRL

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	WO	0x00	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	WO	0x0	sw_trng_req Software set this bit to request trng data, After data is valid, RK_RNG will clear this bit.
3	WO	0x0	sw_drng_req Software set this bit to request drng data, After data is valid, RK_RNG will clear this bit.
2	WO	0x0	test_req Software set this bit to request testn DRNG, After responding to the request, RK_RNG will clear this bit.
1	WO	0x0	reseed_req Software set this bit to request reseed DRNG, After responding to the request, RK_RNG will clear this bit.
0	WO	0x0	inst_req Software set this bit to request instantiation DRNG, After responding to the request, RK_RNG will clear this bit.

RKRNG_STATE

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RC/W1C	0x0	work_clk_abnormal 1'b0: Work clk normal 1'b1: Work clk abnormal
6	RC/W1C	0x0	allan_avar_overflow 1'b0: Allan avar is not overflow 1'b1: Allan avar is overflow
5	RC/W1C	0x0	drng_test_fail 1'b0: DRNG test successful 1'b1: DRNG test failed
4	RC/W1C	0x0	sw_trng_ack 1'b0: TRNG data is not valid 1'b1: TRNG data is valid
3	RC/W1C	0x0	sw_drng_ack 1'b0: DRNG data is not valid 1'b1: DRNG data is valid
2	RC/W1C	0x0	test_ack 1'b0: No respond to the request 1'b1: Respond to the request
1	RC/W1C	0x0	reseed_ack 1'b0: No respond to the request 1'b1: Respond to the request
0	RC/W1C	0x0	inst_ack 1'b0: No respond to the request 1'b1: Respond to the request

RKRNG_INT_EN

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	work_clk_abnormal_int_en 1'b0: Disable 1'b1: Enable
6	RW	0x0	allan_int_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	drng_test_fail_int_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_trng_int_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	sw_drng_int_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	test_int_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	reseed_int_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	inst_int_en 1'b0: Disable 1'b1: Enable

RKRNG_TEST_CNT

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Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	test_interval Count The Times of reseed and Auto Reseed, and perform auto-test when the value reaches the set value of the register

RKRNG_RESEED_CNT

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000400	reseed_interval The update operation is counted and reseed is executed when the count reaches the set value in the register.

RKRNG_UPDATE_CNT

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	update_interval Count the number of random data, and perform self-check when the value reaches the set value of the register.

RKRNG_ALLAN_ACC_NUM

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	allan_acc_num The number of samples needed to calculate the variance.

RKRNG_ALLAN_LIMIT_LOW

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	allan_linit_low Lower bound of variance

RKRNG_ALLAN_LIMIT_HIGH

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	allan_linit_high Upper bound of variance

RKRNG_ALLAN_AVAR_RESULT

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	allan_avar_result Variance result

RKRNG_AUTO_CLK_GATE

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved
0	RW	0x1	auto_clkgate_en 1'b0: No auto gate 1'b1: Auto gate

RKRNG_DBG_SEL

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	cro_str_dout_div Whether the output signal of cro_str_dout is divided frequency. 1'b0: No division of cro_str_dout 1'b1: 16 division of cro_str_dout
0	RW	0x0	work_clk_div Whether the output signal of work clk is divided frequency. 1'b0: No division of work clk 1'b1: 16 division of work clk

RKRNG_TRNG_DATA_0

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trng_data_0 TRNG data 0

RKRNG_TRNG_DATA_1

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trng_data_1 TRNG data 1

RKRNG_TRNG_DATA_2

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trng_data_2 TRNG data 2

RKRNG_TRNG_DATA_3

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trng_data_3 TRNG data 3

RKRNG_TRNG_DATA_4

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trng_data_4 TRNG data 4

RKRNG_TRNG_DATA_5

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trng_data_5 TRNG data 5

RKRNG_TRNG_DATA_6

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Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trng_data_6 TRNG data 6

RKRNG_TRNG_DATA_7

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trng_data_7 TRNG data 7

RKRNG_DRNG_DATA_0

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	drng_data_0 DRNG DATA 0

RKRNG_DRNG_DATA_1

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	drng_data_1 DRNG DATA 1

RKRNG_DRNG_DATA_2

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	drng_data_2 DRNG DATA 2

RKRNG_DRNG_DATA_3

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	drng_data_3 DRNG DATA 3

RKRNG_DRNG_DATA_4

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	drng_data_4 DRNG DATA 4

RKRNG_DRNG_DATA_5

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	drng_data_5 DRNG DATA 5

RKRNG_DRNG_DATA_6

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	drng_data_6 DRNG DATA 6

RKRNG_DRNG_DATA_7

Address: **Operational Base** + offset (0x008C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	drng_data_7 DRNG DATA 7

RKRNG_WORK_CLK_EN

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	work_clk_en TRNG work clock enable 1'b0: Disable work clock, and reset TRNG 1'b1: Enable work clock, and release the reset of TRNG

RKRNG_WORK_CLK_FLAG

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	work_clk_flag TRNG work clock flag. Indicates whether TRNG work clock oscillates normally 1'b0: Normally 1'b1: Abnormally

RKRNG_WORK_CLK_NUM_LIMIT

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	work_clk_num_limit TRNG work clock not flip limit. Indicates the maximum acceptable non flipped clock cycle of TRNG work clock

RKRNG_SOFT_RING_EN0

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	soft_ring_en0 Entropy source ring enable register 0

RKRNG_SOFT_RING_EN2

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	soft_ring_en2 Entropy source ring enable register 2

RKRNG_STR1_0_INIT

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00000000	str1_0_init STR1 initial value register 0

RKRNG_ENTROPY_EN_CTL

Address: **Operational Base** + offset (0x00B8)

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Bit	Attr	Reset Value	Description
31:16	RW	0x000a	entropy_cnt_num Indicates how many TRNG work clock cycles a bit entropy source is collected
15:8	RW	0x64	entropy_dly_num Indicates how many TRNG work clock cycles have passed before TRNG starts working after entropy source is enabled
7:1	RO	0x00	reserved
0	RW	0x1	entropy_en Entropy source enable 1'b0: Disable 1'b1: Enable

RKRNG_ENTROPY_MASK_CTL

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x1	entropy_xor_mask Entropy source XOR mask. When entropy_post_en[0] of ENTROPY_POST_CTL register is equal to 0, entropy_xor_mask has at most one valid bit, and the lower bit has higher priority
3:2	RO	0x0	reserved
1:0	RW	0x1	entropy_ck_mask Entropy source check mask

RKRNG_ENTROPY_POST_CTL

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:2	RW	0x00	bypass_num_jvn John von Neumann entropy source enhancement timeout limit 0xFF: Must pass others: Reach this register num, ignore (When the number of John von Neumann entropy enhancement errors reaches the value of this register, it is mandatory to pass. When the register value is 0xFF, it must be enhanced by John von Neumann entropy)
1	RW	0x0	entropy_post_jvn_en Entropy source John von Neumann enhanced post-processing enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	entropy_post_xor_en Entropy source XOR enhanced post-processing enable 1'b0: Disable 1'b1: Enable

RKRNG_ENTROPY_CK_CTL

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	entropy_always_check Entropy source always check enable.

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Bit	Attr	Reset Value	Description
3	RW	0x0	entropy_check_must_pass Entropy source check must pass enable. When this register is enabled, the entropy source check corresponding to the enable must pass 1'b0: Disable 1'b1: Enable
2	RW	0x0	entropy_bi_check_en Entropy source block statistical of itinerary check enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	entropy_fi_check_en Entropy source frequency of itinerary check enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	entropy_fb_check_en Entropy source frequency of bit check enable 1'b0: Disable 1'b1: Enable

RKRNG_ENTROPY_FB_LIMIT0

Address: **Operational Base** + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	entropy_fb_bit64_limit Frequency limit of entropy source per 64 bits. When equal to 0, disable this type check
23:21	RO	0x0	reserved
20:16	RW	0x00	entropy_fb_bit32_limit Frequency limit of entropy source per 32 bits. When equal to 0, disable this type check
15:12	RO	0x0	reserved
11:8	RW	0x0	entropy_fb_bit16_limit Frequency limit of entropy source per 16 bits. When equal to 0, disable this type check
7:3	RO	0x00	reserved
2:0	RW	0x0	entropy_fb_bit8_limit Frequency limit of entropy source per 8 bits. When equal to 0, disable this type check

RKRNG_ENTROPY_FB_LIMIT1

Address: **Operational Base** + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	entropy_fb_bit_full_limit Frequency limit of complete random number length of entropy source. When equal to 0, disable this type check
15:7	RO	0x000	reserved
6:0	RW	0x00	entropy_fb_bit128_limit Frequency limit of entropy source per 128 bits. When equal to 0, disable this type check

RKRNG_ENTROPY_FI_BIT_NUM

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	entropy_fi_bit_num Entropy source frequency of itinerary check bit length number

RKRNG_ENTROPY_FI_LIMIT

Address: **Operational Base** + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	entropy_fi_limit_high Entropy source frequency of itinerary higher limit
15:0	RW	0x0000	entropy_fi_limit_low Entropy source frequency of itinerary lower limit

RKRNG_ENTROPY_BI_CTL

Address: **Operational Base** + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:2	RW	0x00000	entropy_bi_bit_num Total check bit length of entropy source block statistical of itinerary check
1:0	RW	0x0	entropy_bi_count_sel Entropy source block statistical of itinerary block counting selection 2'b00: 8 bits per block 2'b01: 128 bits per block 2'b10: 10000 bits per block 2'b11: Reserved

RKRNG_ENTROPY_BI_LIMIT_LOW0

Address: **Operational Base** + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	entropy_bi_v3_low Entropy source block statistical of itinerary check v3 lower limit
23:16	RW	0x00	entropy_bi_v2_low Entropy source block statistical of itinerary check v2 lower limit
15:8	RW	0x00	entropy_bi_v1_low Entropy source block statistical of itinerary check v1 lower limit
7:0	RW	0x00	entropy_bi_v0_low Entropy source block statistical of itinerary check v0 lower limit

RKRNG_ENTROPY_BI_LIMIT_LOW1

Address: **Operational Base** + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	entropy_bi_v6_low Entropy source block statistical of itinerary check v6 lower limit
15:8	RW	0x00	entropy_bi_v5_low Entropy source block statistical of itinerary check v5 lower limit
7:0	RW	0x00	entropy_bi_v4_low Entropy source block statistical of itinerary check v4 lower limit

RKRNG_ENTROPY_BI_LIMITHIGH0

Address: **Operational Base** + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	entropy_bi_v3_high Entropy source block statistical of itinerary check v3 higher limit

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	entropy_bi_v2_high Entropy source block statistical of itinerary check v2 higher limit
15:8	RW	0x00	entropy_bi_v1_high Entropy source block statistical of itinerary check v1 higher limit
7:0	RW	0x00	entropy_bi_v0_high Entropy source block statistical of itinerary check v0 higher limit

RKRNG_ENTROPY_BI_LIMIT_HIGH1

Address: **Operational Base** + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	entropy_bi_v6_high Entropy source block statistical of itinerary check v6 higher limit
15:8	RW	0x00	entropy_bi_v5_high Entropy source block statistical of itinerary check v5 higher limit
7:0	RW	0x00	entropy_bi_v4_high Entropy source block statistical of itinerary check v4 higher limit

RKRNG_TRAND_CK_CTL

Address: **Operational Base** + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	trand_check_must_pass True random number check must pass enable. When this register is enabled, the true random number check corresponding to the enable must pass 1'b0: Disable 1'b1: Enable
2	RW	0x0	trand_bi_check_en True random number block statistical of itinerary check enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	trand_fi_check_en True random number frequency of itinerary check enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	trand_fb_check_en True random number frequency of block check enable 1'b0: Disable 1'b1: Enable

RKRNG_TRAND_FB_LIMIT0

Address: **Operational Base** + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	trand_fb_bit64_limit Frequency limit of true random number per 64 bits. When equal to 0, disable this type check
23:21	RO	0x0	reserved
20:16	RW	0x00	trand_fb_bit32_limit Frequency limit of true random number per 32 bits. When equal to 0, disable this type check
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	trand_fb_bit16_limit Frequency limit of true random number per 16 bits. When equal to 0, disable this type check
7:3	RO	0x00	reserved
2:0	RW	0x0	trand_fb_bit8_limit Frequency limit of true random number per 8 bits. When equal to 0, disable this type check

RKRNG_TRAND_FB_LIMIT1

Address: **Operational Base** + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	trand_fb_bit_full_limit Frequency limit of complete random number length of true random number. When equal to 0, disable this type check
15:7	RO	0x000	reserved
6:0	RW	0x00	trand_fb_bit128_limit Frequency limit of true random number per 128 bits. When equal to 0, disable this type check

RKRNG_TRAND_FI_BIT_NUM

Address: **Operational Base** + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trand_fi_bit_num True random number frequency of itinerary check bit length number

RKRNG_TRAND_FI_LIMIT

Address: **Operational Base** + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	trand_fi_limit_high True random number frequency of itinerary higher limit
15:0	RW	0x0000	trand_fi_limit_low True random number frequency of itinerary lower limit

RKRNG_TRAND_BI_CTL

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:2	RW	0x00000	trand_bi_bit_num Total check bit length of true random number block statistical of itinerary check
1:0	RW	0x0	trand_bi_count_sel True random number block statistical of itinerary block counting selection 2'b00: 8 bits per block 2'b01: 128 bits per block 2'b10: 10000 bits per block 2'b11: Reserved

RKRNG_TRAND_BI_LIMIT_LOW0

Address: **Operational Base** + offset (0x0104)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	trand_bi_v3_low True random number block statistical of itinerary check v3 lower limit
23:16	RW	0x00	trand_bi_v2_low True random number block statistical of itinerary check v2 lower limit
15:8	RW	0x00	trand_bi_v1_low True random number block statistical of itinerary check v1 lower limit
7:0	RW	0x00	trand_bi_v0_low True random number block statistical of itinerary check v0 lower limit

RKRNG_TRAND_BI_LIMIT_LOW1

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	trand_bi_v6_low True random number block statistical of itinerary check v6 lower limit
15:8	RW	0x00	trand_bi_v5_low True random number block statistical of itinerary check v5 lower limit
7:0	RW	0x00	trand_bi_v4_low True random number block statistical of itinerary check v4 lower limit

RKRNG_TRAND_BI_LIMIT_HIGH0

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	trand_bi_v3_high True random number block statistical of itinerary check v3 higher limit
23:16	RW	0x00	trand_bi_v2_high True random number block statistical of itinerary check v2 higher limit
15:8	RW	0x00	trand_bi_v1_high True random number block statistical of itinerary check v1 higher limit
7:0	RW	0x00	trand_bi_v0_high True random number block statistical of itinerary check v0 higher limit

RKRNG_TRAND_BI_LIMIT_HIGH1

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	trand_bi_v6_high True random number block statistical of itinerary check v6 higher limit
15:8	RW	0x00	trand_bi_v5_high True random number block statistical of itinerary check v5 higher limit

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	trand_bi_v4_high True random number block statistical of itinerary check v4 higher limit

RKRNG_BI_PASS_AUTO

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	bi_pass_auto Enable block statistical of itinerary check automatic pass through hardware check 1'b0: Disable 1'b1: Enable

RKRNG_SOFT_BI_RESULT_VLD

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	soft_bi_result_vld Software block statistical of itinerary check result valid 1'b0: Invalid 1'b1: Valid

RKRNG_SOFT_BI_RESULT_PASS

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	soft_bi_result_pass Software block statistical of itinerary check result 1'b0: Fail 1'b1: Pass

RKRNG_ENTROPY_CK_RESULT_VLD

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	entropy_avar_vld Entropy source Allan Variance AVAR check result valid 1'b0: Invalid 1'b1: Valid
2	RW	0x0	entropy_bi_ck_vld Entropy source block statistical of itinerary check result valid 1'b0: Invalid 1'b1: Valid
1	RW	0x0	entropy_fi_ck_vld Entropy source frequency of itinerary check result valid 1'b0: Invalid 1'b1: Valid
0	RW	0x0	entropy_fb_ck_vld Entropy source frequency of bit check result valid 1'b0: Invalid 1'b1: Valid

RKRNG_ENTROPY_FB_CK_RESULT

Address: **Operational Base** + offset (0x0124)

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Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	entropy_fb_bit_global_result Entropy source frequency of global check result 1'b0: All PASS 1'b1: At least one check FAIL in bit8/bit16/bit32/bit64/bit128/bit_full
5	RW	0x0	entropy_fb_bit_full_result Entropy source frequency of full entropy number check result 1'b0: PASS 1'b1: FAIL
4	RW	0x0	entropy_fb_bit128_result Entropy source frequency of bit128 check result 1'b0: PASS 1'b1: FAIL
3	RW	0x0	entropy_fb_bit64_result Entropy source frequency of bit64 check result 1'b0: PASS 1'b1: FAIL
2	RW	0x0	entropy_fb_bit32_result Entropy source frequency of bit32 check result 1'b0: PASS 1'b1: FAIL
1	RW	0x0	entropy_fb_bit16_result Entropy source frequency of bit16 check result 1'b0: PASS 1'b1: FAIL
0	RW	0x0	entropy_fb_bit8_result Entropy source frequency of bit8 check result 1'b0: PASS 1'b1: FAIL

RKRNG_ENTROPY_FI_CK_RESULT

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	entropy_fi_check_result Entropy source frequency of itinerary check result 1'b0: PASS 1'b1: FAIL

RKRNG_ENTROPY_BI_CK_RESULT0

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	entropy_bi_v3_result Entropy source block statistical of itinerary check result v3
23:16	RW	0x00	entropy_bi_v2_result Entropy source block statistical of itinerary check result v2
15:8	RW	0x00	entropy_bi_v1_result Entropy source block statistical of itinerary check result v1
7:0	RW	0x00	entropy_bi_v0_result Entropy source block statistical of itinerary check result v0

RKRNG_ENTROPY_BI_CK_RESULT1

Address: **Operational Base** + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	entropy_bi_v6_result Entropy source block statistical of itinerary check result v6
15:8	RW	0x00	entropy_bi_v5_result Entropy source block statistical of itinerary check result v5
7:0	RW	0x00	entropy_bi_v4_result Entropy source block statistical of itinerary check result v4

RKRNG_TRAND_CK_RESULT_VLD

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	trand_avar_vld True random number Allan Variance AVAR check result valid 1'b0: Invalid 1'b1: Valid
2	RW	0x0	trand_bi_ck_vld True random number block statistical of itinerary check result valid 1'b0: Invalid 1'b1: Valid
1	RW	0x0	trand_fi_ck_vld True random number frequency of itinerary check result valid 1'b0: Invalid 1'b1: Valid
0	RW	0x0	trand_fb_ck_vld True random number frequency of bit check result valid 1'b0: Invalid 1'b1: Valid

RKRNG_TRAND_FB_CK_RESULT

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	trand_fb_bit_global_result True random number frequency of global check result 1'b0: All PASS 1'b1: At least one check FAIL in bit8/bit16/bit32/bit64/bit128/bit_full
5	RW	0x0	trand_fb_bit_full_result True random number frequency of full entropy number check result 1'b0: PASS 1'b1: FAIL
4	RW	0x0	trand_fb_bit128_result True random number frequency of bit128 check result 1'b0: PASS 1'b1: FAIL
3	RW	0x0	trand_fb_bit64_result True random number frequency of bit64 check result 1'b0: PASS 1'b1: FAIL

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Bit	Attr	Reset Value	Description
2	RW	0x0	trand_fb_bit32_result True random number frequency of bit32 check result 1'b0: PASS 1'b1: FAIL
1	RW	0x0	trand_fb_bit16_result True random number frequency of bit16 check result 1'b0: PASS 1'b1: FAIL
0	RW	0x0	trand_fb_bit8_result True random number frequency of bit8 check result 1'b0: PASS 1'b1: FAIL

RKRNG_TRAND_FI_CK_RESULT

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	trand_fi_check_result True random number frequency of itinerary check result 1'b0: PASS 1'b1: FAIL

RKRNG_TRAND_BI_CK_RESULT0

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	trand_bi_v3_result True random number block statistical of itinerary check result v3
23:16	RW	0x00	trand_bi_v2_result True random number block statistical of itinerary check result v2
15:8	RW	0x00	trand_bi_v1_result True random number block statistical of itinerary check result v1
7:0	RW	0x00	trand_bi_v0_result True random number block statistical of itinerary check result v0

RKRNG_TRAND_BI_CK_RESULT1

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	trand_bi_v6_result True random number block statistical of itinerary check result v6
15:8	RW	0x00	trand_bi_v5_result True random number block statistical of itinerary check result v5
7:0	RW	0x00	trand_bi_v4_result True random number block statistical of itinerary check result v4

RKRNG_NONCE_0

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_0 NONCE 0

RKRNG_NONCE_1

Address: **Operational Base** + offset (0x0204)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_1 NONCE 1

RKRNG_NONCE_2

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_2 NONCE 2

RKRNG_NONCE_3

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_3 NONCE 3

RKRNG_NONCE_4

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_4 NONCE 4

RKRNG_NONCE_5

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_5 NONCE 5

RKRNG_NONCE_6

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_6 NONCE 6

RKRNG_NONCE_7

Address: **Operational Base** + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nonce_7 NONCE 7

RKRNG_NONCE_8

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_8 NONCE 8

RKRNG_NONCE_9

Address: **Operational Base** + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_9 NONCE 9

RKRNG_NONCE_10

Address: **Operational Base** + offset (0x0228)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_10 NONCE 10

RKRNG_NONCE_11

Address: **Operational Base** + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	nonce_11 NONCE 11

RKRNG_ADDITION_0

Address: **Operational Base** + offset (0x0300)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_0 ADDITION 0

RKRNG_ADDITION_1

Address: **Operational Base** + offset (0x0304)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_1 ADDITION 1

RKRNG_ADDITION_2

Address: **Operational Base** + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_2 ADDITION 2

RKRNG_ADDITION_3

Address: **Operational Base** + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_3 ADDITION 3

RKRNG_ADDITION_4

Address: **Operational Base** + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_4 ADDITION 4

RKRNG_ADDITION_5

Address: **Operational Base** + offset (0x0314)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_5 ADDITION 5

RKRNG_ADDITION_6

Address: **Operational Base** + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_6 ADDITION 6

RKRNG_ADDITION_7

Address: **Operational Base** + offset (0x031C)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_7 ADDITION 7

RKRNG_ADDITION_8

Address: **Operational Base** + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_8 ADDITION 8

RKRNG_ADDITION_9

Address: **Operational Base** + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_9 ADDITION 9

RKRNG_ADDITION_10

Address: **Operational Base** + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_10 ADDITION 10

RKRNG_ADDITION_11

Address: **Operational Base** + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	addition_11 ADDITION 11

31.5 Application Notes

31.5.1 Clock and Reset

Table 31-1 Clock Description of RKRNG

Clock Name	Description	Frequency
s_hclk	Clock of secure AHB slave	200M（follow SOC design）
ns_hclk	Clock of non-secure AHB slave	200M（follow SOC design）
work_clk	Output of inverter oscillating ring	50M-500M

Clock domains of RKRNG are as follow:

- SIF and DRNG are in s_hclk domain
- NSIF is in ns_hclk domain
- TRNG is in work_clk domain

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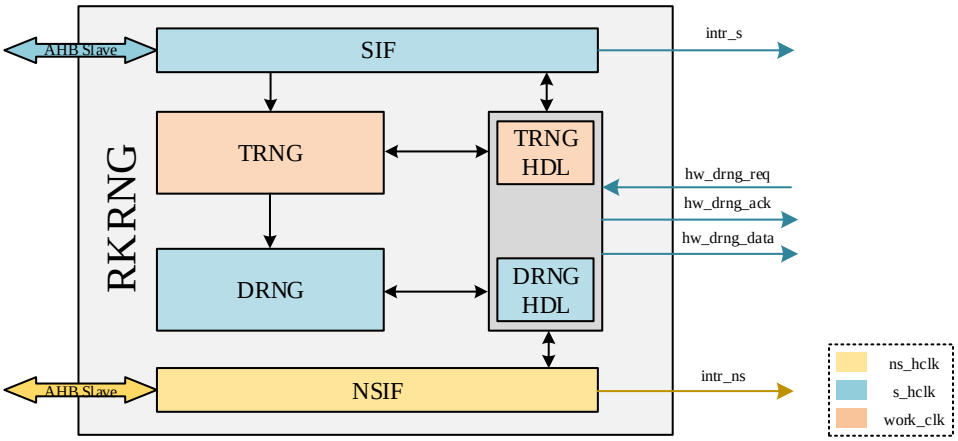

Fig. 31-2 Clock Domain of RKRNG

Note: hw_drng_ack/hw_drng_data are in s_hclk domain, if there is hardware drng request, must set s_hclk valid.

31.5.2 TRNG Implementation Principle

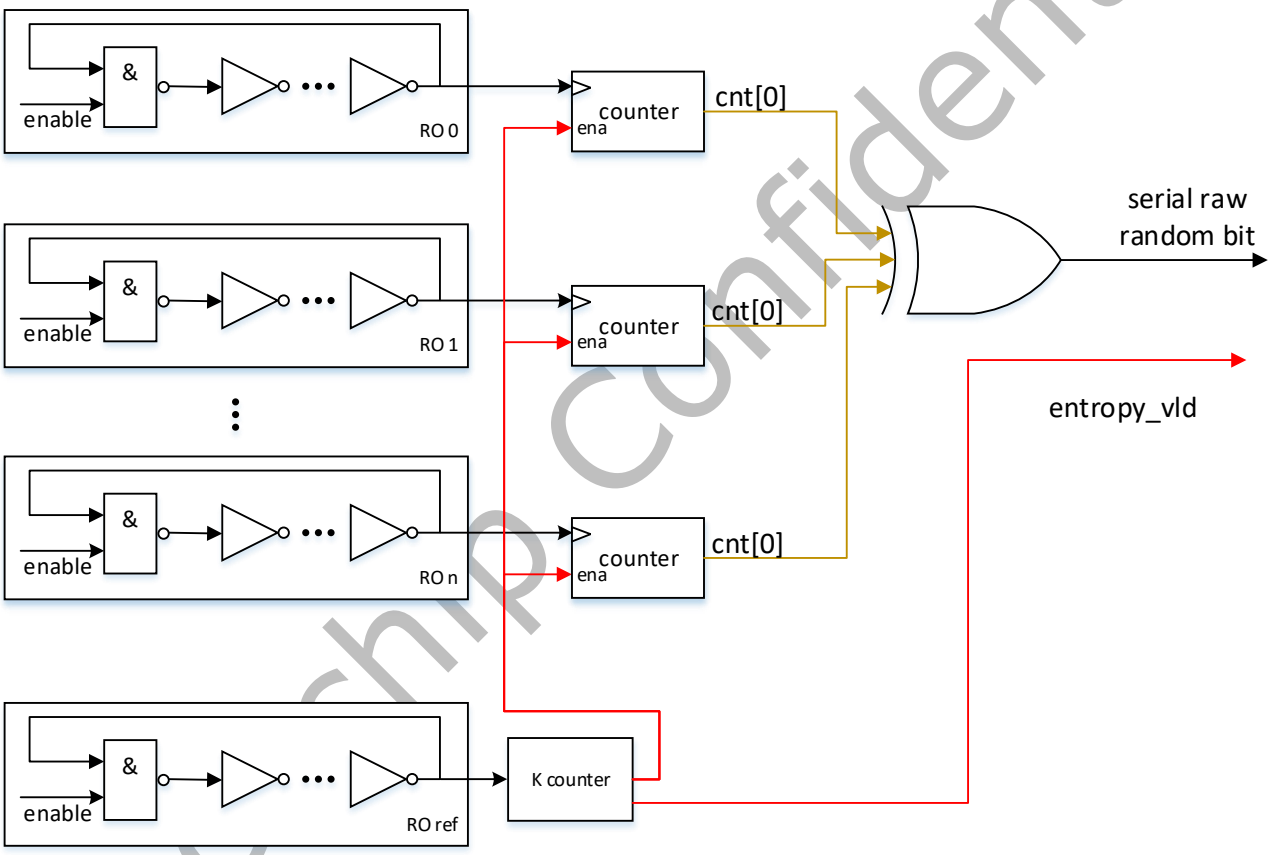

Fig. 31-3 CRO-TRNG Schematic Diagram

- Related registers
  - RK_RNG_INV_NUM: control the inverter number of all CRO oscillating ring, used to adjust the frequency of CRO
  - RK_RNG_WORK_CLK_EN: control the RO ref enable, when set to 0, will reset the TRNG
  - RK_RNG_WORK_CLK_NUM_LIMIT: check whether work clk works normally, when hardware detected that un-reverse time of work clk is more than the number of WORK_CLK_NUM_LIMIT period on hclk, hardware will set RK_RNG_WORK_CLK_FLAG and RK_RNG_STATE[7]
  - RK_RNG_SOFT_RING_EN0: every bit is related an enable of the inverter in oscillating ring
  - RK_RNG_ENTROPY_EN_CTL:
    - entropy_en: enable of TRNG, generally no used

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- entroy_dly_num: when set this bit, hardware will count for the work clk. After the counter value is greater or equal to the setting value, TRNG begin to sample the entropy of the oscillating ring.
- entropy_cnt_num: indicate how many work clk cycles used to output an entropy bit, bigger the value means greater the quality of random number, and slower the time to generate a random number

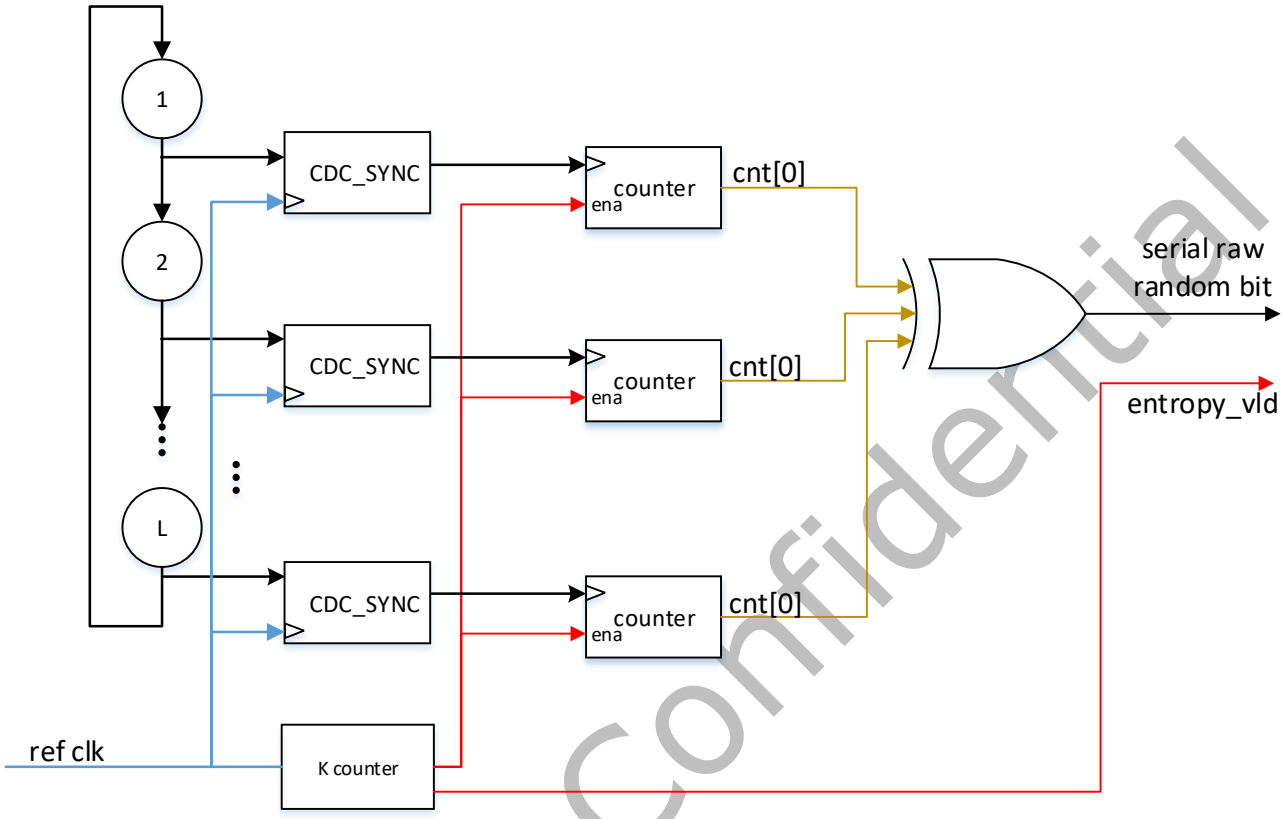

Fig. 31-4 STR-TRNG Schematic Diagram

- Related registers
  - RK_RNG_SOFT_RING_EN2: enable of STR oscillating ring, when set to 0, the RK_RNG_STR1_0_INIT can be initialed to STR
  - RK_RNG_STR1_0_INIT: the initial value of STR
  - RK_RNG_ENTROPY_MASK_CTL:
    - entropy_ck_mask: default value is 1, which means select CRO as entropy source only; when set to 2, means select STR as entropy source only; when set to 3, means select the logic OR of CRO and STR as entropy source
    - entropy_xor_mask: default value is 1, which means select CRO as the input of post processing only; when set to 2, means select STR as the input of post processing only; when set to 3, means select the XOR of CRO and STR as the input of post processing
  - RK_RNG_ENTROPY_POST_CTL:
    - entropy_post_xor_en: default value is 0, which means select highest priority entropy source as the input of post processing according to the value of entropy_xor_mask. Lower bit means higher priority. When set to 1, means enable the XOR post processing according to value of entropy_xor_mask.
    - Entropy_post_jvn_en: default value is 0, which means entropy without post processing; when set to 1, means entropy with post processing
    - Bypass_num_jvn: post processing time out limitation, configure to 0xff

31.5.3 Register Related to Online Checking

Online checking includes frequency checking(fb), itinerary checking(fi) and block itinerary checking(bi). Frequency checking and itinerary checking must pass before checking block itinerary. Original entropy and the entropy after post processing are both support to perform checking. Checking or not is depending on the register configuration.

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31.5.3.1 Online Checking on Original Entropy

- RK_RNG_ALLAN_ACC_NUM: used to count sample number of variance
- RK_RNG_ALLAN_LIMIT_LOW、RK_RNG_ALLAN_LIMIT_HIGH:
  - When the variance is in the closed interval, then pass
  - Otherwise, set RK_RNG_STATE.allan_avar_overflow
- RK_RNG_ALLAN_AVAR_RESULT:
  - When RK_RNG_ENTROPY_CK_RESULT_VLD.entropy_avar_vld is set, means the value of RK_RNG_ALLAN_AVAR_RESULT is valid
- RK_RNG_ENTROPY_CK_CTL:
  - entropy_always_check: when set this bit, means need to checking the original entropy after every random bit generation
  - entropy_check_must_pass: when set this bit, means all enable online checking must pass, can the random number output
  - entropy_fi_check_en: enable of itinearary checking
  - entropy_fb_check_en: enable of frequency checking
  - entropy_bi_check_en: block itinerary checking, when set this bit, entropy_fi_check_en and entropy_fb_check_en must also be set
- RK_RNG_ENTROPY_FB_LIMIT0:
  - entropy_fb_bit8_limit: the threshold of 8bit block, entropy_fb_bit8_limit =< x =< (8-entropy_fb_bit8_limit)
  - entropy_fb_bit_full_limit: the block size is equal to the value of seed_len and related to RK_RNG_CFG.aes_key_size. The seed_len of aes-128 is 256bit, the seed_len of aes-192 is 320bit, and the seed_len of aes-256 is 384bit.
- RK_RNG_ENTROPY_FI_BIT_BUM: used to count for the bit number of itinerary sequence
- RK_RNG_ENTROPY_FI_LIMIT: the limitation of itinerary, when itinerary x meet the condition of lower limitation =< x =< higher limitation, then checking pass
- RK_RNG_ENTROPY_BI_CTL:
  - entropy_bi_bit_num: the total length of checking sequence
  - entropy_bit_count_sel: the length of block
- RK_RNG_ENTROPY_BI_LIMIT_LOW0, RK_RNG_ENTROPY_BI_LIMIT_LOW1, RK_RNG_ENTROPY_BI_LIMIT_HIGH0, RK_RNG_ENTROPY_BI_LIMIT_HIGH1
  - The threshold of each itinerary, hardware counting number is in the setting scope means pass

31.5.3.2 Online checking on post processing entropy

The related registers are as follow, and the meaning of registers are same to the register of online checking on original entropy.

- RK_RNG_TRAND_CK_CTL
- RK_RNG_TRAND_FB_LIMIT0
- RK_RNG_TRAND_FB_LIMIT1
- RK_RNG_TRAND_FI_BIT_NUM
- RK_RNG_TRAND_FI_LIMIT
- RK_RNG_TRAND_BI_CTL
- RK_RNG_TRAND_BI_LIMIT_LOW0
- RK_RNG_TRAND_BI_LIMIT_LOW1
- RK_RNG_TRAND_BI_LIMIT_HIGH0
- RK_RNG_TRAND_BI_LIMIT_HIGH1

31.5.4 Status Register

- RK_RNG_ENTROPY_CK_RESULT_VLD, RK_RNG_TRAND_CK_RESULT_VLD
  - Indicate whether the onling checking is completed
- RK_RNG_ENTROPY_FB_CK_RESULT, RK_RNG_TRAND_FB_CK_RESULT
  - Indicate whether the frequency checking is pass
- RK_RNG_ENTROPY_FI_CK_RESULT, RK_RNG_TRAND_FI_CK_RESULT
  - Indicate whether the itinerary checking is pass
- RK_RNG_ENTROPY_BI_CK_RESULT0, RK_RNG_ENTROPY_BI_CK_RESULT1, RK_RNG_TRAND_BI_CK_RESULT0, RK_RNG_TRAND_BI_CK_RESULT1
  - The result of block itinerary checking

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- RK_RNG_BI_PASS_AUTO
  - Default value is 1, means hardware auto check the result of block itinerary
  - When set to 0, means software will check the result of block itinerary
- RK_RNG_SOFT_BI_RESULT_VLD, RK_RNG_SOFT_BI_RESULT_PASS
  - when RK_RNG_BI_PASS_AUTO is set to 1, there is no need to configure these registers
  - when RK_RNG_BI_PASS_AUTO is set to 0, software need to configure RK_RNG_SOFT_BI_RESULT_PASS firstly, then write 1 to RK_RNG_SOFT_BI_RESULT_VLD, and wait hardware auto clear this bit.

31.5.5 Example of Configuration

- Select CRO as entropy source without post processing and online checking
  - Reset TRNG by setting WORK_CLK_EN to 0x0
  - Set ENTROPY_POST_CTL to 0x0 for no post processing (default value, no need to configure)
  - Set ENTROPY_MASK_CTL to 0x0101 (default value, no need to configure)
  - Set ENTROPY_EN_CTL to (0x1 | 0x20<<8 | 0x100<<16), changing value of (0x100<<16) can adjust the sampling interval, the value is bigger, and the rate of random number generation is slower
  - Set SOFT_RING_EN0 to 0xffff (default value, no need to configure)
  - Set SOFT_RING_EN2 to 0x0
  - Release reset of TRNG by setting WORK_CLK_EN to 0x1, entropy source begins to generate random number at this time
  - Request random number of TRNG or DRNG
- Select STR as entropy source without post processing and online checking
  - Reset TRNG by setting WORK_CLK_EN to 0x0
  - Set ENTROPY_POST_CTL to 0x0 for no post processing (default value, no need to configure)
  - Set ENTROPY_MASK_CTL to 0x0202
  - Set ENTROPY_EN_CTL to (0x1 | 0x20<<8 | 0x100<<16), changing value of (0x100<<16) can adjust the sampling interval, the value is bigger, and the rate of random number generation is slower
  - Set SOFT_RING_EN2 to 0x0
  - Set STR1_0_INIT = 0x68ab4130
  - Set SOFT_RING_EN0 to 0x0
  - Set SOFT_RING_EN2 to 0x1
  - Release reset of TRNG by setting WORK_CLK_EN to 0x1, entropy source begins to generate random number at this time
  - Request random number of TRNG or DRNG
- Select XOR of CRO and STR as entropy source without post processing and online checking
  - Reset TRNG by setting WORK_CLK_EN to 0x0
  - Set ENTROPY_POST_CTL to (0x1 | 0xff<<2)
  - Set ENTROPY_MASK_CTL to 0x0303
  - Set ENTROPY_EN_CTL to (0x1 | 0x20<<8 | 0x100<<16), changing value of (0x100<<16) can adjust the sampling interval, the value is bigger, and the rate of random number generation is slower
  - Set SOFT_RING_EN2 to 0x0
  - Set STR1_0_INIT = 0x68ab4130
  - Set SOFT_RING_EN0 to 0xffff
  - Set SOFT_RING_EN2 to 0x1
  - Release reset of TRNG by setting WORK_CLK_EN to 0x1, entropy source begins to generate random number at this time
  - Request random number of TRNG or DRNG

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