Rockchip
RK3506
Technical Reference Manual
(Part 1)

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Revision History

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2025-03-11	1.2	Update the TSADC and GPIO chapters
2024-11-22	1.1	Update the CRU, PMU, GRF, Mailbox, Audio Subsystem, ASRC, and SDMMC Chapters.
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Chapter 1 System Overview

1.1 Address Mapping

RK3506 address mapping is provided in below two table.

Table 1-1 RK3506 Address Mapping

Module	Start Address	Size	Module	Start Address	Size
DDR	0x00000000	3072MB	SAI4	0xFF4A8000	32KB
DSMC_MEM	0xC0000000	1008MB	Audio DSM	0xFF4B0000	32KB
DMAC0	0xFF000000	32KB	SPI2	0xFF4C0000	32KB
DMAC1	0xFF008000	32KB	MAC0	0xFF4C8000	32KB
I2C0	0xFF040000	64KB	MAC1	0xFF4D0000	32KB
I2C1	0xFF050000	64KB	GPIO2/3/4_IOC	0xFF4D8000	32KB
I2C2	0xFF060000	64KB	UART5	0xFF4E0000	32KB
UART0	0xFF0A0000	64KB	SARADC	0xFF4E8000	32KB
UART1	0xFF0B0000	64KB	NS OPTC	0xFF4F0000	32KB
UART2	0xFF0C0000	64KB	Audio ADC	0xFF4F8000	32KB
UART3	0xFF0D0000	64KB	Secure OTPC	0xFF520000	32KB
UART4	0xFF0E0000	64KB	OTP MASK	0xFF528000	32KB
SPI0	0xFF120000	64KB	KEY READER	0xFF530000	32KB
SPI1	0xFF130000	64KB	GIC400	0xFF580000	32KB
PWM1	0xFF170000	32KB	VOP	0xFF600000	64KB
GPIO2	0xFF1C0000	16KB	RGA	0xFF610000	64KB
GPIO3	0xFF1D0000	16KB	DSI HOST	0xFF640000	64KB
GPIO4	0xFF1E0000	16KB	TSADC	0xFF650000	64KB
Secure DMAC0	0xFF200000	32KB	GPIO1_IOC	0xFF660000	64KB
Secure DMAC1	0xFF208000	32KB	DPHY	0xFF670000	64KB
SGRF	0xFF210000	32KB	NS CRYPTO	0xFF700000	64KB
SPINLOCK	0xFF240000	16KB	NS RNG	0xFF710000	64KB
TIMER0	0xFF250000	32KB	USB2.0 OTG0	0xFF740000	256KB
TIMER1	0xFF258000	32KB	USB2.0 OTG1	0xFF780000	256KB
WDT0	0xFF260000	32KB	DDRPHY	0xFF7C0000	64KB
WDT1	0xFF268000	32KB	A7_DEBUG	0xFF800000	256KB
DDRCTL	0xFF270000	32KB	GRF_CORE	0xFF840000	16KB
DDRMON	0xFF278000	32KB	GPIO1	0xFF870000	16KB
DDR_LPC	0xFF280000	32KB	FLEXBUS/Slave DSMC	0xFF880000	64KB
GRF	0xFF288000	16KB	DSMC	0xFF8B0000	64KB
MAILBOX	0xFF290000	16KB	PMU	0xFF900000	64KB
INTMUX	0xFF2A0000	32KB	GRF_PMU/RMIO	0xFF910000	16KB
DMA2DDR	0xFF2A8000	32KB	PWM0	0xFF930000	16KB
USBPHY	0xFF2B0000	32KB	GPIO0	0xFF940000	16KB
SAI0	0xFF300000	64KB	GPIO0_SHADOW	0xFF948000	16KB
SAI1	0xFF310000	64KB	GPIO0_IOC	0xFF950000	64KB
CAN0	0xFF320000	64KB	SGRF_PMU	0xFF960000	64KB
CAN1	0xFF330000	64KB	HPTIMER	0xFF980000	64KB
PDM	0xFF380000	64KB	TOUCH KEY	0xFF990000	64KB

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Module	Start Address	Size	Module	Start Address	Size
SPDIF_TX	0xFF3A0000	64KB	CRU	0xFF9A0000	64KB
SPDIF_RX	0xFF3B0000	64KB	CRU_PMU	0xFF9B0000	64KB
ASRC0	0xFF3C0000	64KB	System SRAM	0xFFF80000	48KB
ASRC1	0xFF3D0000	64KB	Secure Crypto	0xFFFC0000	32KB
SDMMC	0xFF480000	32KB	Secure KEYLAD	0xFFFD0000	64KB
FSPI	0xFF488000	32KB	Secure RNG	0xFFFE0000	64KB
SAI2	0xFF498000	32KB	BOOTROM	0xFFFF0000	24KB
SAI3	0xFF4A0000	32KB			

The following table shows the BootROM /System SRAM address before and after remapping. Before remapping, 0xFFF80000 and 0xFFFF0000 is the base address for System SRAM and BootROM separately. After remapping, BootROM could not be accessed, both 0xFFFF80000 and 0xFFFF0000 are the base address for System SRAM and only 64KB System SRAM space could be accessed from 0xFFFF0000 base address.

Table 1-2 RK3506 BootROM /System SRAM Remap Function

Before remap		After remap	
0xFFF80000	System SRAM(48K)	0xFFF80000/0xFFFF0000	System SRAM(48K)
0xFFFF0000	BootROM(24K)	Not Access	BootROM(24K)

The following table shows the DDR /DSMC_MEM address before and after remapping. Before remapping, 0x00000000 and 0xC00000000 is the base address for DDR and DSMC_MEM separately. After remapping, DDR could not be accessed, 0x00000000 is the base address for DSMC_MEM.

Table 1-3 RK3506 DDR /DSMC_MEM Remap Function

Before remap		After remap	
0xC0000000	DSMC_MEM(1008M)	0x00000000	DSMC_MEM(1008M
0x00000000	DDR(3072M)	Not Access	DDR(3072M)

1.2 System Boot

RK3506 provides system boot from off-chip devices such as eMMC memory, Serial NAND or NOR Flash, SDMMC card. When boot code is not ready in these devices, the boot code can be programmed through USB2.0 OTG interface or SPI2 interface by running ROM code in BootROM. All of the ROM code is hard code in internal BootROM. Below figure shows the procedure of ROM code execution.

The following features are supported by ROM code.

- Support system boot from the following device:
  - eMMC Interface, 4bits data width
  - Serial NOR Flash, 1/4bits data width
  - SDMMC Card, 4bits data width
- Support system code download by USB2.0 OTG0
- Support system code download by SPI2

Following figure shows typical RK3506 boot procedure flow. Boot sequence can be adjusted by changing SARADC_IN0 voltage level.

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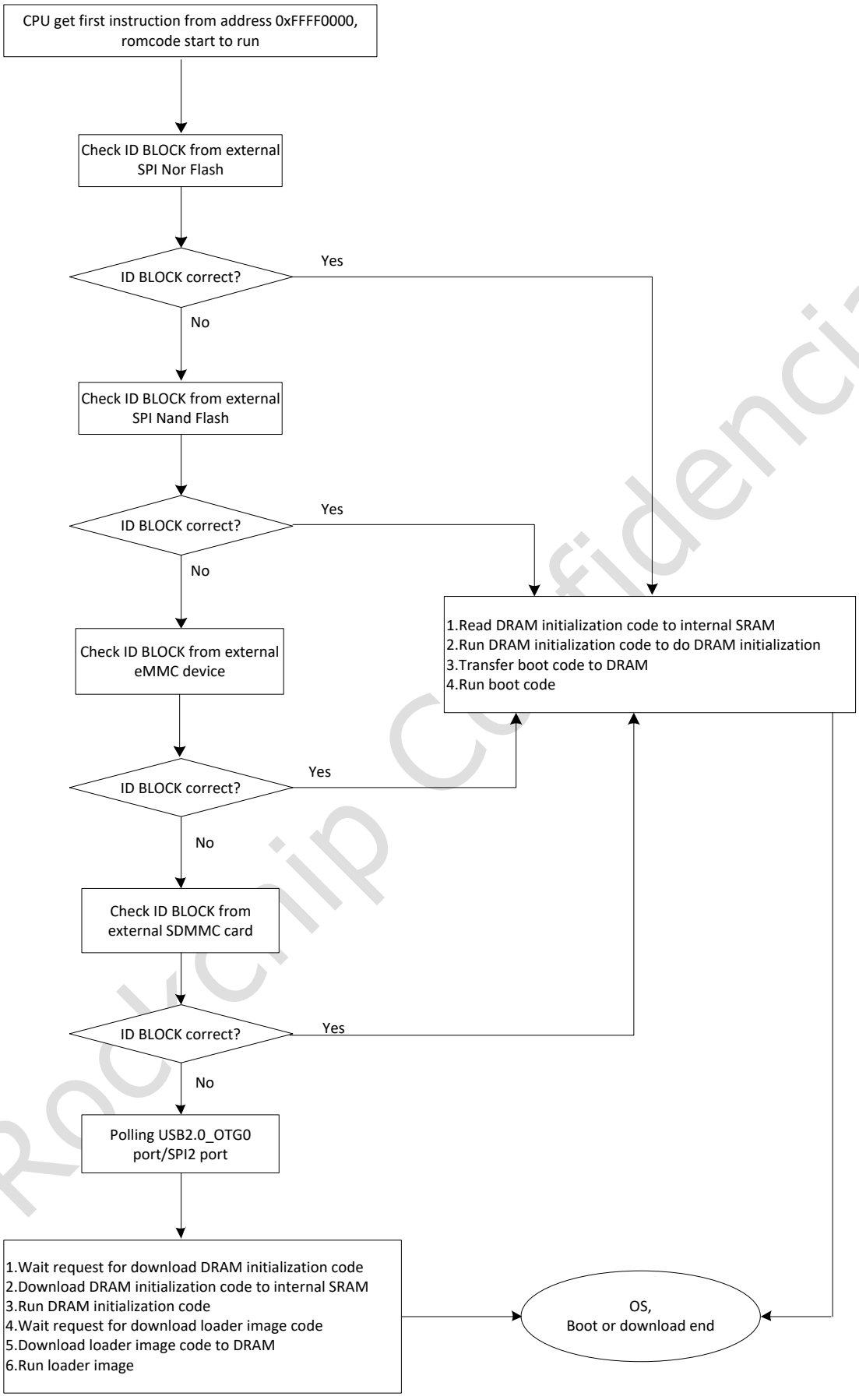

Fig. 1-1 RK3506 Boot Procedure Flow

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1.3 System Interrupt Connection

RK3506 provides a general interrupt controller (GIC) for CPU, which has 154 SPI (shared peripheral interrupts) interrupt sources and 6 PPI (Private peripheral interrupt) interrupt sources. The triggered type for each SPI interrupt is high level sensitive, and for each PPI interrupt is low level sensitive, both are not programmable. The detailed interrupt sources connection is in the following table.

Table 1-4 RK3506 Interrupt Connection List

Interrupt Type	Interrupt ID	Source	Polarity
PPI	N/A	16	Low level
	N/A	17	Low level
	N/A	18	Low level
	N/A	19	Low level
	N/A	20	Low level
	N/A	21	Low level
	N/A	22	Low level
	N/A	23	Low level
	N/A	24	Low level
	N/A	25	Low level
	CNTHPIRQ	26	Low level
	CNTVIRQ	27	Low level
	LEGACYFIQ	28	Low level
	CNTPSIRQ	29	Low level
	CNTPNSIRQ	30	Low level
	LEGACYIRQ	31	Low level
SPI	GPIO0_0	32	High level
	GPIO0_1	33	High level
	GPIO0_2	34	High level
	GPIO0_3	35	High level
	GPIO1_0	36	High level
	GPIO1_1	37	High level
	GPIO1_2	38	High level
	GPIO1_3	39	High level
	GPIO2_0	40	High level
	GPIO2_1	41	High level
	GPIO2_2	42	High level
	GPIO2_3	43	High level
	GPIO3_0	44	High level
	GPIO3_1	45	High level
	GPIO3_2	46	High level
	GPIO3_3	47	High level
	GPIO4_0	48	High level
	GPIO4_1	49	High level
	GPIO4_2	50	High level
	GPIO4_3	51	High level
	TOUCH_KEY_POS	52	High level
	TOUCH_KEY_NEG	53	High level
	PWM0_CH0	54	High level
	PWM0_CH1	55	High level
	PWM0_CH2	56	High level
	PWM0_CH3	57	High level
	PWM1_CH0	58	High level
	PWM1_CH1	59	High level

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	PWM1_CH2	60	High level
	PWM1_CH3	61	High level
	PWM1_CH4	62	High level
	PWM1_CH5	63	High level
	PWM1_CH6	64	High level
	PWM1_CH7	65	High level
	UART0	66	High level
	UART1	67	High level
	UART2	68	High level
	UART3	69	High level
	UART4	70	High level
	UART5	71	High level
	I2C0	72	High level
	I2C1	73	High level
	I2C2	74	High level
	SPI0	75	High level
	SPI1	76	High level
	CAN0	77	High level
	CAN1	78	High level
	SPDIF_TX	79	High level
	SPDIF_RX	80	High level
	PDM	81	High level
	SAI0	82	High level
	SAI1	83	High level
	SAI2	84	High level
	SAI3	85	High level
	SAI4	86	High level
	ASRC0	87	High level
	ASRC1	88	High level
	SARADC	89	High level
	TSADC	90	High level
	VOP	91	High level
	MIPI_DSIHOST	92	High level
	RGA	93	High level
	OTPC_NS	94	High level
	OTPC_S	95	High level
	KEY_READER	96	High level
	OTPC_MASK	97	High level
	MAC0_SBD	98	High level
	MAC0_SBD_TX	99	High level
	MAC0_SBD_RX	100	High level
	MAC0_PMT	101	High level
	MAC1_SBD	102	High level
	MAC1_SBD_TX	103	High level
	MAC1_SBD_RX	104	High level
	MAC1_PMT	105	High level
	USB2.0_OTG0	106	High level
	USB2.0_OTG0_BVALID	107	High level
	USB2.0_OTG0_ID	108	High level
	USB2.0_OTG0_LINESTATE	109	High level
	USB2.0_OTG0_DISCONNECT	110	High level
	USB2.0_OTG1	111	High level

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	USB2.0_OTG1_BVALID	112	High level
	USB2.0_OTG1_ID	113	High level
	USB2.0_OTG1_LINESTATE	114	High level
	USB2.0_OTG1_DISCONNECT	115	High level
	SPI2	116	High level
	FSPI	117	High level
	SDMMC	118	High level
	DDRC_AWPOISON[0]	119	High level
	DDRC_AWPOISON[1]	120	High level
	DDRC_ARPOISON[0]	121	High level
	DDRC_ARPOISON[1]	122	High level
	DDRC_DFI_ALERT_ERR	123	High level
	DDRMON	124	High level
	DDRPHY	125	High level
	TIMER0_0	126	High level
	TIMER0_1	127	High level
	TIMER0_2	128	High level
	TIMER0_3	129	High level
	TIMER0_4	130	High level
	TIMER0_5	131	High level
	TIMER1_0	132	High level
	TIMER1_1	133	High level
	TIMER1_2	134	High level
	TIMER1_3	135	High level
	TIMER1_4	136	High level
	TIMER1_5	137	High level
	HPTIMER	138	High level
	WDT0	139	High level
	WDT1	140	High level
	Reserved	141	High level
	Reserved	142	High level
	CRYPTO	143	High level
	CRYPTO_KEYLAD	144	High level
	CRYPTO_SC	145	High level
	NS_RNG	146	High level
	S_RNG	147	High level
	DMAC0	148	High level
	DMAC0_ABORT	149	High level
	DMAC1	150	High level
	DMAC1_ABORT	151	High level
	SLAVE_DSMC	152	High level
	A7_PMUIRQ_0	153	High level
	A7_PMUIRQ_1	154	High level
	A7_PMUIRQ_2	155	High level
	A7_PMUIRQ_3	156	High level
	A7_AXIERRIRQ	157	High level
	DSMC	158	High level
	FLEXBUS	159	High level
	PMU	160	High level
	NPOR_POWERGOOD	161	High level
	GPIO1_SHADOW_0	162	High level
	GPIO1_SHADOW_1	163	High level

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	GPIO1_SHADOW_2	164	High level
	GPIO1_SHADOW_3	165	High level
	USB2.0_OTG0_VBUSVALID	166	High level
	USB2.0_OTG1_VBUSVALID	167	High level
	VOP_LB_INTR	168	High level
	DMA2DDR	169	High level
	MAILBOX_AP[0]	170	High level
	MAILBOX_AP[1]	171	High level
	MAILBOX_AP[2]	172	High level
	MAILBOX_AP[3]	173	High level
	MAILBOX_BB[0]	174	High level
	MAILBOX_BB[1]	175	High level
	MAILBOX_BB[2]	176	High level
	MAILBOX_BB[3]	177	High level
	MAC0_MCGR_REQ	178	High level
	MAC1_MCGR_REQ	179	High level
	DMAC0_MASK_IRQ0	180	High level
	DMAC0_MASK_IRQ1	181	High level
	DMAC0_MASK_IRQ2	182	High level
	DMAC1_MASK_IRQ0	183	High level
	DMAC1_MASK_IRQ1	184	High level
	DMAC1_MASK_IRQ2	185	High level

There is a Nested Vectored Interrupt Controller (NVIC) embedded in MCU, which has general interrupt sources for internal blocks or external devices. Each interrupt's triggered type is high level, not programmable. The detailed interrupt sources connection is in the following table.

Table 1-5 RK3506 MCU Interrupt Connection List

Interrupt Type	Interrupt ID	Source	Polarity
SPI	GPIO0_1	0	High level
	GPIO0_2	1	High level
	GPIO0_3	2	High level
	GPIO1_1/GPIO1_SHADOW_1	3	High level
	GPIO1_2/GPIO1_SHADOW_2	4	High level
	GPIO1_3/GPIO1_SHADOW_3	5	High level
	GPIO2_3	6	High level
	GPIO3_3	7	High level
	TOUCH_KEY_POS	8	High level
	TOUCH_KEY_NEG	9	High level
	PWM1_CH6	10	High level
	PWM1_CH7	11	High level
	UART3	12	High level
	UART4	13	High level
	I2C2	14	High level
	SPI1	15	High level
	SARADC	16	High level
	SDMMC	17	High level
	TIMER0_4	18	High level
	TIMER0_5	19	High level
	TIMER1_4	20	High level
	TIMER1_5/DSMC	21	High level
	MAILBOX_8MUX1	22	High level

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	DMAC0	23	High level
	DMAC0_ABORT	24	High level
	DMAC1	25	High level
	DMAC1_ABORT	26	High level
	FLEXBUS	27	High level
	INTMUX0	28	High level
	INTMUX1	29	High level
	INTMUX2	30	High level
	INTMUX3	31	High level

The interrupt INTMUX0~3 in above table is from INTMUX which is a 128 to 4 interrupt arbitration controller. INTMUX source is connected to general interrupt sources for internal blocks or external devices. Each interrupts triggered type is high level, not programmable. The detailed interrupt sources connection is in the following table.

Table 1-6 INTMUX Interrupt Connection List

Interrupt ID	INTMUX Source	INTMUX Output	Polarity
0	GPIO0_0	INTMUX0	High level
1	GPIO1_0		High level
2	GPIO2_0		High level
3	GPIO2_1		High level
4	GPIO2_2		High level
5	GPIO3_0		High level
6	GPIO3_1		High level
7	GPIO3_2		High level
8	GPIO4_0		High level
9	GPIO4_1		High level
10	GPIO4_2		High level
11	GPIO4_3		High level
12	PWM0_CH0		High level
13	PWM0_CH1		High level
14	PWM0_CH2		High level
15	PWM0_CH3		High level
16	PWM1_CH0		High level
17	PWM1_CH1		High level
18	PWM1_CH2		High level
19	PWM1_CH3		High level
20	PWM1_CH4		High level
21	PWM1_CH5		High level
22	UART0		High level
23	UART1		High level
24	UART2		High level
25	UART5		High level
26	I2C0		High level
27	I2C1		High level
28	SPI0		High level
29	CAN0		High level
30	CAN1		High level
31	SPDIF_TX		High level
32	SPDIF_RX	INTMUX1	High level
33	PDM		High level
34	SAI0		High level
35	SAI1		High level
36	SAI2		High level
37	SAI3		High level
38	SAI4		High level

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39	ASRC0		High level
40	ASRC1		High level
41	TSADC		High level
42	VOP		High level
43	MIPI_DSIHOST		High level
44	RGA		High level
45	OTPC_NS		High level
46	OTPC_S		High level
47	KEY_READER		High level
48	OTPC_MASK		High level
49	MAC0_SBD		High level
50	MAC0_SBD_TX		High level
51	MAC0_SBD_RX		High level
52	MAC0_PMT		High level
53	MAC1_SBD		High level
54	MAC1_SBD_TX		High level
55	MAC1_SBD_RX		High level
56	MAC1_PMT		High level
57	OTG0		High level
58	OTG0_BVALID		High level
59	OTG0_ID		High level
60	OTG0_LINESTATE		High level
61	OTG0_DISCONNECT		High level
62	OTG1		High level
63	OTG1_BVALID		High level
64	OTG1_ID	INTMUX2	High level
65	OTG1_LINESTATE		High level
66	OTG1_DISCONNECT		High level
67	SPI2APB		High level
68	FSPI		High level
69	DDRC_AWPOISON[0]		High level
70	DDRC_AWPOISON[1]		High level
71	DDRC_ARPOISON[0]		High level
72	DDRC_ARPOISON[1]		High level
73	DDRC_DFI_ALERT_ERR		High level
74	DDR_MONITOR		High level
75	DDRPHY		High level
76	TIMER0_0		High level
77	TIMER0_1		High level
78	TIMER0_2		High level
79	TIMER0_3		High level
80	TIMER1_0		High level
81	TIMER1_1		High level
82	TIMER1_2		High level
83	TIMER1_3		High level
84	HPTIMER		High level
85	WDT0		High level
86	WDT1		High level
87	Reserved		High level
88	CRYPTO		High level
89	CRYPTO_KLAD		High level
90	CRYPTO_SC		High level
91	NS_TRNG		High level
92	S_TRNG		High level
93	DSMC_SLAVE		High level

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94	A7_PMUIRQ_0		High level
95	A7_PMUIRQ_1		High level
96	A7_PMUIRQ_2	INTMUX3	High level
97	A7_PMUIRQ_3		High level
98	A7_AXIERRIRQ		High level
99	DSMC/TIMER1_5		High level
100	PMU		High level
101	NPOR_POWERGOOD		High level
102	GPIO1_SHADOW_0		High level
103	GPIO1_SHADOW_1/GPIO1_1		High level
104	GPIO1_SHADOW_2/GPIO1_2		High level
105	GPIO1_SHADOW_3/GPIO1_3		High level
106	OTG0_VBUSVALID		High level
107	OTG1_VBUSVALID		High level
108	VOP_LB_INTR		High level
109	DMA2DDR		High level
110	MAILBOX_AP[0]		High level
111	MAILBOX_AP[1]		High level
112	MAILBOX_AP[2]		High level
113	MAILBOX_AP[3]		High level
114	MAILBOX_BB[0]		High level
115	MAILBOX_BB[1]		High level
116	MAILBOX_BB[2]		High level
117	MAILBOX_BB[3]		High level
118	MAC0_MCGR_REQ		High level
119	MAC1_MCGR_REQ		High level
120	DMAC0_MASK_IRQ0		High level
121	DMAC0_MASK_IRQ1		High level
122	DMAC0_MASK_IRQ2		High level
123	DMAC1_MASK_IRQ0		High level
124	DMAC1_MASK_IRQ1		High level
125	DMAC1_MASK_IRQ2		High level
126	Reserved		High level
127	Reserved		High level

1.4 System DMA Hardware Request Connection

RK3506 provides two DMAC in the system. The handshake channel number between peripheral and DMAC is described in this section. For detailed descriptions of DMAC, please refer to DMAC Chapter.

Some DMAC channels may receive multiple peripheral requests but can only receive one at the same time. For detailed configuration, please refer to GRF Chapter.

Table 1-7 RK3506 DMAC0 Hardware Request Connection List

Req Number	Source	Polarity
0	SPI0 TX/CAN0 RX/ASRC0 RX	High level
1	SPI0 RX/CAN1 RX/ASRC0 TX	High level
2	SPI1 TX/DSMC TX/ASRC1 RX	High level
3	SPI1 RX/DSMC RX/ASRC1 TX	High level
4	UART0 TX/CAN0 RX	High level
5	UART0 RX/CAN1 RX/PDM RX	High level
6	UART1 TX/SPDIF_TX	High level
7	UART1 RX/SPDIF_RX	High level
8	UART2 TX/DSMC TX/SAI0 RX	High level
9	UART2 RX/SAI0 TX	High level

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Req Number	Source	Polarity
10	UART3 TX/DSMC RX/SAI1 RX	High level
11	UART3 RX/SAI1 TX	High level

Table 1-8 RK3506 DMAC1 Hardware Request Connection List

Req Number	Source	Polarity
0	SAI0 RX	High level
1	SAI0 TX	High level
2	SAI1 RX	High level
3	SAI1 TX	High level
4	SAI2 RX	High level
5	SAI2 TX	High level
6	SAI3 TX	High level
7	SAI3 RX	High level
8	SAI4 RX	High level
9	PDM RX	High level
10	SPDIF_TX/CAN0 RX	High level
11	SPDIF_RX/CAN1 RX	High level
12	UART4 TX	High level
13	UART4 RX	High level
14	UART5 TX	High level
15	UART5 RX	High level
16	ASRC0 RX	High level
17	ASRC0 TX	High level
18	ASRC1 RX	High level
19	ASRC1 TX	High level

1.5 Rockchip Matrix IO Function List

RK3506 support one Rockchip Matrix IO (RM_IO) which are designed to let numerous functional signals share limited pin interfaces. Within the same matrix, any function signal can be mapped to any pin interface by software configurable.
RM_IO support 98 function signals map to 32 pin interfaces (GPIO0_A0~GPIO0_C7, GPIO1_B1, GPIO1_B2, GPIO1_B3, GPIO1_C2, GPIO1_C3, GPIO1_D1, GPIO1_D2, GPIO1_D3).

Table 1-9 RK3506 Rockchip Matrix IO Function List

Function Index	RM_IO	Function Index	RM_IO
1	UART1_TX	51	SAI0_MCLK
2	UART1_RX	52	SAI0_SCLK
3	UART2_TX	53	SAI0_LRCK
4	UART2_RX	54	SAI0_SDI0
5	UART3_TX	55	SAI0_SDI1
6	UART3_RX	56	SAI0_SDI2
7	UART3_CTSN	57	SAI0_SDI3
8	UART3_RTSN	58	SAI0_SDO
9	UART4_TX	59	SAI1_MCLK
10	UART4_RX	60	SAI1_SCLK
11	UART4_CTSN	61	SAI1_LRCK

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12	UART4_RTSN	62	SAI1_SDI
13	MIPITE	63	SAI1_SDO0
14	CLK_32K	64	SAI1_SDO1
15	I2C0_SCL	65	SAI1_SDO2
16	I2C0_SDA	66	SAI1_SDO3
17	I2C1_SCL	67	SPI0_CLK
18	I2C1_SDA	68	SPI0_MOSI
19	I2C2_SCL	69	SPI0_MISO
20	I2C2_SDA	70	SPI0_CSN0
21	PDM_CLK0	71	SPI0_CSN1
22	PDM_SDI0	72	SPI1_CLK
23	PDM_SDI1	73	SPI1_MOSI
24	PDM_SDI2	74	SPI1_MISO
25	PDM_SDI3	75	SPI1_CSN0
26	CAN1_TX	76	SPI1_CSN1
27	CAN1_RX	77	WDT_TSADC_SHUT
28	CAN0_TX	78	PMU_SLEEP
29	CAN0_RX	79	CORE_POWER_OFF
30	PWM0_CH0	80	SPDIF_TX
31	PWM0_CH1	81	SPDIF_RX
32	PWM0_CH2	82	PWM1_BIP_CNTR_A0
33	PWM0_CH3	83	PWM1_BIP_CNTR_A1
34	PWM1_CH0	84	PWM1_BIP_CNTR_A2
35	PWM1_CH1	85	PWM1_BIP_CNTR_A3
36	PWM1_CH2	86	PWM1_BIP_CNTR_A4
37	PWM1_CH3	87	PWM1_BIP_CNTR_A5
38	PWM1_CH4	88	PWM1_BIP_CNTR_B0
39	PWM1_CH5	89	PWM1_BIP_CNTR_B1
40	PWM1_CH6	90	PWM1_BIP_CNTR_B2
41	PWM1_CH7	91	PWM1_BIP_CNTR_B3
42	TOUCH_KEY_DRIVE	92	PWM1_BIP_CNTR_B4
43	TOUCH_KEY_IN0	93	PWM1_BIP_CNTR_B5
44	TOUCH_KEY_IN1	94	PDM_CLK1
45	TOUCH_KEY_IN2	95	ETH_RMII0_PPSCLK
46	TOUCH_KEY_IN3	96	ETH_RMII0_PPSTRIG
47	TOUCH_KEY_IN4	97	ETH_RMII1_PPSCLK
48	TOUCH_KEY_IN5	98	ETH_RMII1_PPSTRIG

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49	TOUCH_KEY_IN6		
50	TOUCH_KEY_IN7		

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Chapter 2 Clock & Reset Unit (CRU)

2.1 Overview

CRU is an APB slave module that is designed for generating all kinds of internal and system clocks and resets in the chip. CRU generates system clocks from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset, software reset or temperature sensor.
We design a sub module called CRU_PMU inside CRU. Both CRU and CRU_PMU APB slave address space are 64KB, we define higher 32KB as secure address space.
The CRU supports the following features:

- Compliance with AMBA APB interface
- Embedded with 3 fractional PLLs (GPLL, V0PLL and V1PLL)
- Flexible selection of clock source
- Use clock matrix scheme
- Support dividing clock separately
- Support gating clock separately
- Support software reset each module separately

2.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

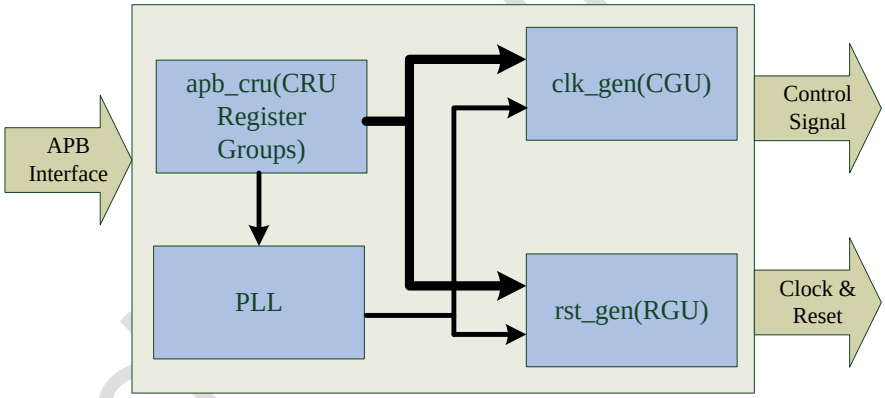

Fig. 2-1 CRU Block Diagram

2.3 Function Description

2.3.1 PLL Introduction

The PLL is a general purpose, high-performance PLL-based clock generator. Also, the PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments. The main features of PLL are as following table.

Table 2-1 PLL Main Features

	FRACPLL(INT Mode)		FRACPLL(FRAC Mode)	
Parameter	Min	Max	Min	Max
FREF(MHz)	1	1200	10	1200M
REFDIV	1	63	1	63
FBDIV	16	3800	20	380
POSTDIV1	1	7	1	7

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POSTDIV2	1	7	1	7
PFD(MHz)	1	FOUTVCO/16	1	FOUTVCO /20
FOUTVCO(MHz)	950	3800	950	3800
FOUTPOSTDIV(MHz)	19	3800	19	3800
lock time(us)		500*REFDIV/FREF		500*REFDIV/FREF

PLL block diagram is shown below:

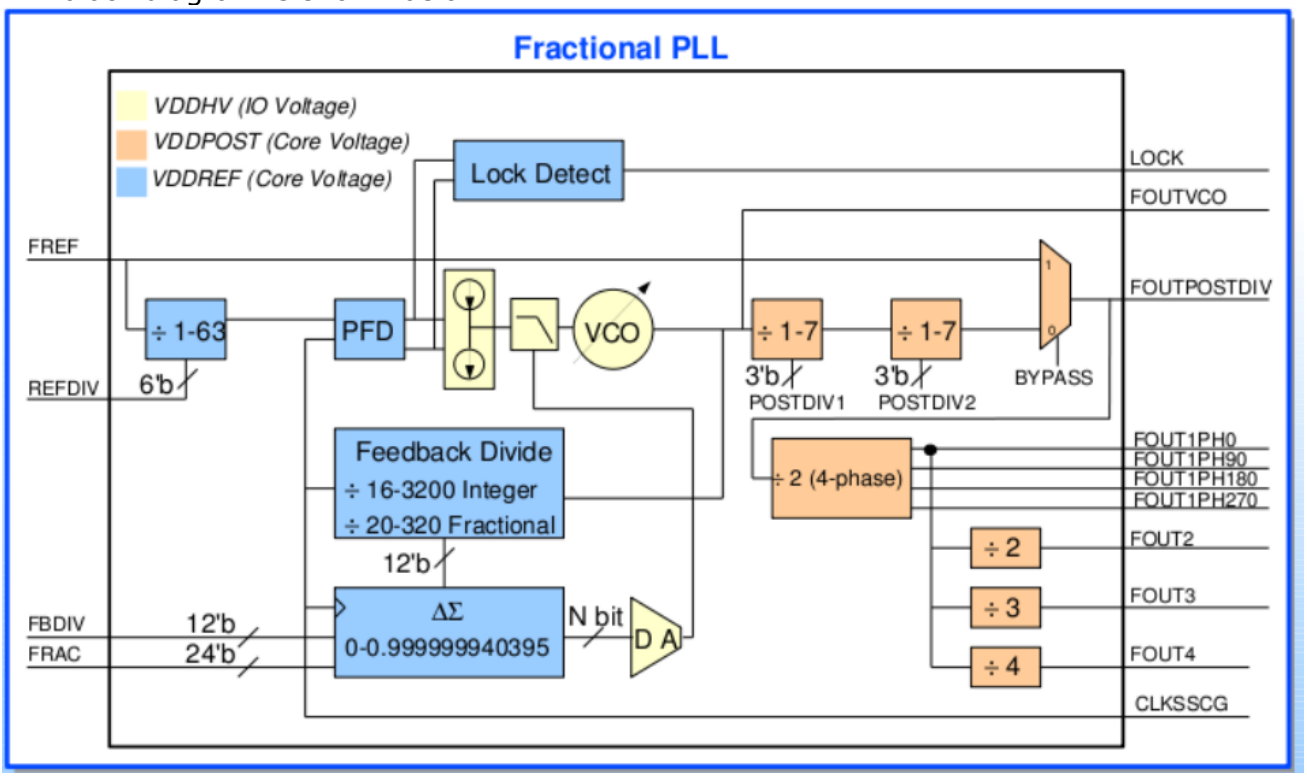

Fig. 2-2 PLL Block Diagram

2.3.2 System Clock Solution

There are 3 fractional PLLs in RK3506: GPLL, V0PLL and V1PLL. All PLLs can receive 24MHz oscillator as input reference clock. In addition, V0PLL and V1PLL supports reference clock from GPIO.

ALL PLLs can be set to three work modes: normal mode, slow mode and deep slow mode. Before power on or changing PLL setting, we must program PLL into slow mode or deep slow mode. To maximize the flexibility, some clocks can select divider source from multiple PLLs. To provide some specific frequency, another solution is integrated: fractional divider and Divfree50 divider are also provided for some modules. All clocks can be gated by software.

The basic units for clock generation are:

- Gating
- MUX (multiplexer)
- Divfree(Glitch free divider)
  - clk_out_freq= clk_in_freq/(divcon + 1)
  - When divcon is even, the clock duty cycle of clk_out is 50%
  - When divcon is odd, the clock duty cycle of clk_out is not 50%
- Fracdiv(Fractional divider)
  - clk_out_freq= clk_in_freq*numerator/denominator, both numerator and denominator are 16 bits
- Divfree50(Glitch free divider for duty cycle 50%)
  - clk_out_freq= clk_in_freq/(divcon +1)
  - When divcon is even or odd, the clock duty cycle of clk_out is 50%

The settings of all basic units are controlled by CRU registers.

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2.3.3 System Reset Solution

Almost all modules have these reset source as the following figure shows. The 'xxx' in the figure is the module name.

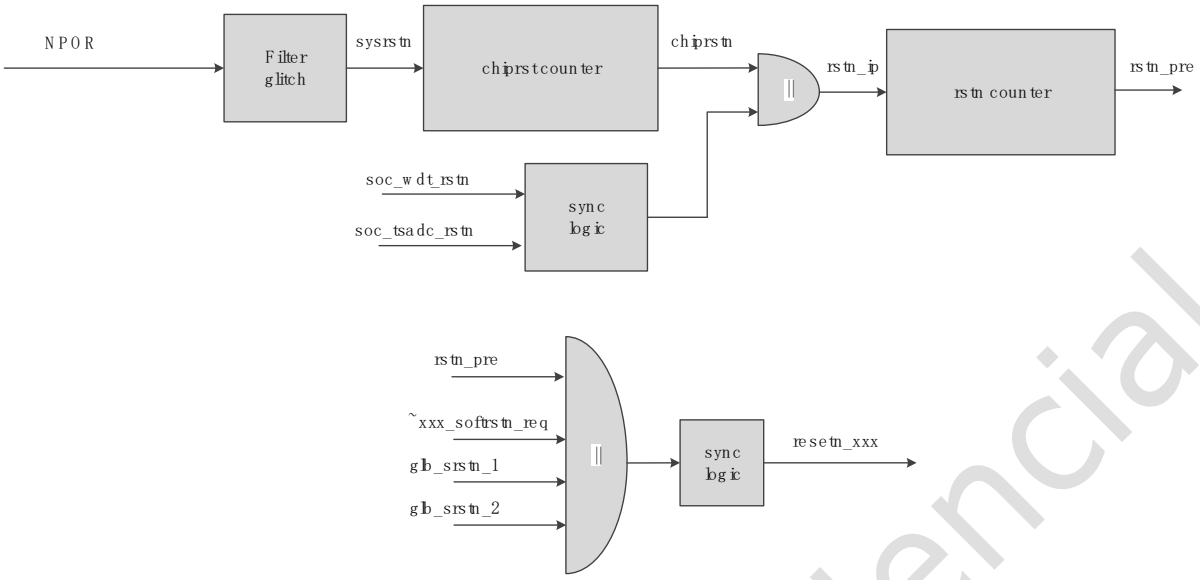

Fig. 2-3 Reset Architecture Diagram

Reset source of each reset signal includes:

- nPOR: External power on reset
- soc_wdt_rstn: Reset from WDT module
- soc_tsadc_rstn: Reset from TSADC module
- softrstn_req: Software reset request by programming CRU_SOFTRST_CON
- glb_srstn_1: First global software reset by programming CRU_GLB_SRST_FST as 0xfdb9
- glb_srstn_2: Second global software reset by programming CRU_GLB_SRST_SND as 0xeca8

2.4 CRU Register Description

2.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_MODE_CON00	0x0280	W	0x00000000	Internal PLL mode select register 0
CRU_CLKSEL_CON00	0x0300	W	0x000004C0	Internal clock select and division register 0
CRU_CLKSEL_CON01	0x0304	W	0x00000B67	Internal clock select and division register 1
CRU_CLKSEL_CON02	0x0308	W	0x00000229	Internal clock select and division register 2
CRU_CLKSEL_CON03	0x030C	W	0x00002A00	Internal clock select and division register 3
CRU_CLKSEL_CON04	0x0310	W	0x00000055	Internal clock select and division register 4
CRU_CLKSEL_CON05	0x0314	W	0x00060019	Internal clock select and division register 5
CRU_CLKSEL_CON06	0x0318	W	0x01200C35	Internal clock select and division register 6

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON07	0x031C	W	0x00C00C35	Internal clock select and division register 7
CRU_CLKSEL_CON08	0x0320	W	0x000003DE	Internal clock select and division register 7
CRU_CLKSEL_CON09	0x0324	W	0x03723D09	Internal clock select and division register 9
CRU_CLKSEL_CON10	0x0328	W	0x001403DE	Internal clock select and division register 8
CRU_CLKSEL_CON11	0x032C	W	0x00800C35	Internal clock select and division register 11
CRU_CLKSEL_CON12	0x0330	W	0x00070064	Internal clock select and division register 12
CRU_CLKSEL_CON13	0x0334	W	0x01290C80	Internal clock select and division register 13
CRU_CLKSEL_CON15	0x033C	W	0x00000240	Internal clock select and division register 15
CRU_CLKSEL_CON16	0x0340	W	0x00000007	Internal clock select and division register 16
CRU_CLKSEL_CON18	0x0348	W	0x00002182	Internal clock select and division register 18
CRU_CLKSEL_CON19	0x034C	W	0x000011A3	Internal clock select and division register 19
CRU_CLKSEL_CON21	0x0354	W	0x00001000	Internal clock select and division register 21
CRU_CLKSEL_CON22	0x0358	W	0x00000001	Internal clock select and division register 22
CRU_CLKSEL_CON23	0x035C	W	0x00000200	Internal clock select and division register 23
CRU_CLKSEL_CON29	0x0374	W	0x00000001	Internal clock select and division register 29
CRU_CLKSEL_CON30	0x0378	W	0x00000000	Internal clock select and division register 30
CRU_CLKSEL_CON31	0x037C	W	0x00000000	Internal clock select and division register 31
CRU_CLKSEL_CON32	0x0380	W	0x00000410	Internal clock select and division register 32
CRU_CLKSEL_CON33	0x0384	W	0x00000050	Internal clock select and division register 33
CRU_CLKSEL_CON34	0x0388	W	0x00004100	Internal clock select and division register 34
CRU_CLKSEL_CON35	0x038C	W	0x000010C0	Internal clock select and division register 35
CRU_CLKSEL_CON36	0x0390	W	0x00000043	Internal clock select and division register 36

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON37	0x0394	W	0x00000020	Internal clock select and division register 37
CRU_CLKSEL_CON38	0x0398	W	0x0000041F	Internal clock select and division register 38
CRU_CLKSEL_CON39	0x039C	W	0x00004620	Internal clock select and division register 39
CRU_CLKSEL_CON40	0x03A0	W	0x00000100	Internal clock select and division register 40
CRU_CLKSEL_CON41	0x03A4	W	0x00000100	Internal clock select and division register 41
CRU_CLKSEL_CON42	0x03A8	W	0x000011A3	Internal clock select and division register 42
CRU_CLKSEL_CON46	0x03B8	W	0x00001111	Internal clock select and division register 46
CRU_CLKSEL_CON47	0x03BC	W	0x00000000	Internal clock select and division register 47
CRU_CLKSEL_CON49	0x03C4	W	0x000041A0	Internal clock select and division register 49
CRU_CLKSEL_CON50	0x03C8	W	0x000007C9	Internal clock select and division register 50
CRU_CLKSEL_CON51	0x03CC	W	0x00000100	Internal clock select and division register 51
CRU_CLKSEL_CON52	0x03D0	W	0x00000100	Internal clock select and division register 52
CRU_CLKSEL_CON53	0x03D4	W	0x00000101	Internal clock select and division register 53
CRU_CLKSEL_CON54	0x03D8	W	0x00000001	Internal clock select and division register 54
CRU_CLKSEL_CON55	0x03DC	W	0x00000007	Internal clock select and division register 55
CRU_CLKSEL_CON58	0x03E8	W	0x000000A3	Internal clock select and division register 58
CRU_CLKSEL_CON59	0x03EC	W	0x00000001	Internal clock select and division register 59
CRU_CLKSEL_CON60	0x03F0	W	0x00000209	Internal clock select and division register 60
CRU_CLKSEL_CON61	0x03F4	W	0x00000113	Internal clock select and division register 61
CRU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
CRU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
CRU_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2

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Name	Offset	Size	Reset Value	Description
CRU_GATE_CON03	0x080C	W	0x00000000	Internal clock gate and division register 3
CRU_GATE_CON04	0x0810	W	0x00000000	Internal clock gate and division register 4
CRU_GATE_CON05	0x0814	W	0x00000000	Internal clock gate and division register 5
CRU_GATE_CON06	0x0818	W	0x00000000	Internal clock gate and division register 6
CRU_GATE_CON07	0x081C	W	0x00000000	Internal clock gate and division register 7
CRU_GATE_CON08	0x0820	W	0x00000000	Internal clock gate and division register 8
CRU_GATE_CON10	0x0828	W	0x00000000	Internal clock gate and division register 10
CRU_GATE_CON11	0x082C	W	0x00000000	Internal clock gate and division register 11
CRU_GATE_CON12	0x0830	W	0x00000000	Internal clock gate and division register 12
CRU_GATE_CON13	0x0834	W	0x00000000	Internal clock gate and division register 13
CRU_GATE_CON14	0x0838	W	0x00000000	Internal clock gate and division register 14
CRU_GATE_CON16	0x0840	W	0x00000000	Internal clock gate and division register 16
CRU_GATE_CON17	0x0844	W	0x00000000	Internal clock gate and division register 17
CRU_GATE_CON18	0x0848	W	0x00000000	Internal clock gate and division register 18
CRU_GATE_CON19	0x084C	W	0x00000000	Internal clock gate and division register 19
CRU_GATE_CON20	0x0850	W	0x00000000	Internal clock gate and division register 20
CRU_GATE_CON21	0x0854	W	0x00000000	Internal clock gate and division register 21
CRU_GATE_CON22	0x0858	W	0x00000000	Internal clock gate and division register 22
CRU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
CRU_SOFTRST_CON02	0x0A08	W	0x00000000	Internal clock reset register 2
CRU_SOFTRST_CON03	0x0A0C	W	0x00000000	Internal clock reset register 3
CRU_SOFTRST_CON04	0x0A10	W	0x00000000	Internal clock reset register 4
CRU_SOFTRST_CON05	0x0A14	W	0x00000000	Internal clock reset register 5
CRU_SOFTRST_CON06	0x0A18	W	0x00000000	Internal clock reset register 6
CRU_SOFTRST_CON07	0x0A1C	W	0x00000000	Internal clock reset register 7
CRU_SOFTRST_CON08	0x0A20	W	0x00000000	Internal clock reset register 8

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Name	Offset	Size	Reset Value	Description
CRU_SOFTRST_CON09	0x0A24	W	0x00000000	Internal clock reset register 9
CRU_SOFTRST_CON10	0x0A28	W	0x00000000	Internal clock reset register 10
CRU_SOFTRST_CON11	0x0A2C	W	0x00000000	Internal clock reset register 11
CRU_SOFTRST_CON12	0x0A30	W	0x00000000	Internal clock reset register 12
CRU_SOFTRST_CON13	0x0A34	W	0x00000000	Internal clock reset register 13
CRU_SOFTRST_CON14	0x0A38	W	0x00000000	Internal clock reset register 14
CRU_SOFTRST_CON17	0x0A44	W	0x00000000	Internal clock reset register 17
CRU_SOFTRST_CON18	0x0A48	W	0x00000000	Internal clock reset register 18
CRU_SOFTRST_CON19	0x0A4C	W	0x00000000	Internal clock reset register 19
CRU_SOFTRST_CON21	0x0A54	W	0x00000000	Internal clock reset register 21
CRU_SOFTRST_CON22	0x0A58	W	0x00000000	Internal clock reset register 22
CRU_GLB_CNT_TH	0x0C00	W	0x00000064	Global reset counter threshold register
CRU_GLB_RST_ST	0x0C04	W	0x00000000	Global reset state register
CRU_GLB_SRST_FST_VALUE	0x0C08	W	0x00000000	Global software first reset register
CRU_GLB_SRST_SND_VALUE	0x0C0C	W	0x00000000	Global software second reset register
CRU_GLB_RST_CON	0x0C10	W	0x00000000	Global reset control register
CRU_COREWFI_CON	0x0C2C	W	0x00000000	Core WFI control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.2 Detail Registers Description

CRU_MODE_CON00

Address: Operational Base(0xFF9A0000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	clk_v1pll_mode clk_v1pll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_v1pll 2'b10: clk_deepslow
3:2	RW	0x0	clk_v0pll_mode clk_v0pll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_v0pll 2'b10: clk_deepslow

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	clk_gpll_mode clk_gpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll 2'b10: clk_deepslow

CRU_CLKSEL_CON00

Address: Operational Base(0xFF9A0000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:10	RW	0x1	clk_gpll_div_100m_div Divide clk_gpll_div_100m by (div_con + 1).
9:6	RW	0x3	clk_gpll_div_div Divide clk_gpll_div by (div_con + 1).
5:0	RO	0x00	reserved

CRU_CLKSEL_CON01

Address: Operational Base(0xFF9A0000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x0b	clk_int_voice_matrix0_div DT50 division register. Divide clk_int_voice_matrix0 by (div_con + 1).
7:4	RW	0x6	clk_v1pll_div_div Divide clk_v1pll_div by (div_con + 1).
3:0	RW	0x7	clk_v0pll_div_div Divide clk_v0pll_div by (div_con + 1).

CRU_CLKSEL_CON02

Address: Operational Base(0xFF9A0000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:5	RW	0x11	clk_int_voice_matrix2_div DT50 division register. Divide clk_int_voice_matrix2 by (div_con + 1).
4:0	RW	0x09	clk_int_voice_matrix1_div DT50 division register. Divide clk_int_voice_matrix1 by (div_con + 1).

CRU_CLKSEL_CON03

Address: Operational Base(0xFF9A0000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x1	clk_frac_voice_matrix0_mux_sel clk_frac_voice_matrix0_mux clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
12:11	RW	0x1	clk_frac_uart_matrix1_mux_sel clk_frac_uart_matrix1_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
10:9	RW	0x1	clk_frac_uart_matrix0_mux_sel clk_frac_uart_matrix0_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
8:5	RW	0x0	clk_testout_sel clk_testout clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_gpll 4'b0010: clk_v0pll 4'b0011: clk_v1pll 4'b0100: clk_deepslow 4'b0101: clk_rc 4'b0110: clk_core_pvtpll_logic 4'b0111: clk_frac_uart_matrix0 4'b1000: clk_frac_voice_matrix0 4'b1001: clk_core_src_pre

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Bit	Attr	Reset Value	Description
			4'b1010: clk_usbotg0_utmi_phy 4'b1011: clk_usbotg1_utmi_phy 4'b1100: dsi_lanebyte_clk_phy 4'b1101: dsi_rxclk_esc_phy 4'b1110: clk_spdifrx_to_asrc 4'b1111: Reserved
4:0	RW	0x00	clk_testout_div Divide clk_testout by (div_con + 1).

CRU_CLKSEL_CON04

Address: Operational Base(0xFF9A0000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x1	clk_frac_common_matrix2_mux_sel clk_frac_common_matrix2_mux clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
5:4	RW	0x1	clk_frac_common_matrix1_mux_sel clk_frac_common_matrix1_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
3:2	RW	0x1	clk_frac_common_matrix0_mux_sel clk_frac_common_matrix0_mux clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
1:0	RW	0x1	clk_frac_voice_matrix1_mux_sel clk_frac_voice_matrix1_mux clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate

CRU_CLKSEL_CON05

Address: Operational Base(0xFF9A0000) + offset (0x0314)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00060019	clk_frac_uart_matrix0_div clk_frac_uart_matrix0 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON06

Address: Operational Base(0xFF9A0000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RW	0x01200c35	clk_frac_uart_matrix1_div clk_frac_uart_matrix1 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON07

Address: Operational Base(0xFF9A0000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00c00c35	clk_frac_voice_matrix0_div clk_frac_voice_matrix0 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON08

Address: Operational Base(0xFF9A0000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RW	0x000000	clk_frac_voice_matrix0_div_high clk_frac_voice_matrix0 fraction division high bits register. bit23-16 for the bit23~16 of numerator bit7-0 for the bit23~16 of denominator

CRU_CLKSEL_CON09

Address: Operational Base(0xFF9A0000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RW	0x03723d09	clk_frac_voice_matrix1_div clk_frac_voice_matrix1 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON10

Address: Operational Base(0xFF9A0000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_frac_voice_matrix1_div_high clk_frac_voice_matrix1 fraction division high bits register. bit23-16 for the bit23~16 of numerator bit7-0 for the bit23~16 of denominator

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CRU_CLKSEL_CON11

Address: Operational Base(0xFF9A0000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800c35	clk_frac_common_matrix0_div clk_frac_common_matrix0 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON12

Address: Operational Base(0xFF9A0000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:0	RW	0x00070064	clk_frac_common_matrix1_div clk_frac_common_matrix1 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON13

Address: Operational Base(0xFF9A0000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:0	RW	0x01290c80	clk_frac_common_matrix2_div clk_frac_common_matrix2 fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON15

Address: Operational Base(0xFF9A0000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:9	RW	0x1	aclk_core_root_div Divide aclk_core_root by (div_con + 1).
8	RW	0x0	clk_core_src_pvtmux_sel clk_core_src_pvtmux clock mux. 1'b0: clk_core_src_pre 1'b1: clk_core_pvtpll_src
7	RW	0x0	clk_core_pvtpll_src_sel clk_core_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_core_pvtpll

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Bit	Attr	Reset Value	Description
6:5	RW	0x2	clk_core_src_div_sel clk_core_src_div clock mux. 2'b00: clk_gpll_mux_gate 2'b01: clk_v0pll_mux_gate 2'b10: clk_v1pll_mux_gate
4:0	RW	0x00	clk_core_src_div_div Divide clk_core_src_div by (div_con + 1).

CRU_CLKSEL_CON16

Address: Operational Base(0xFF9A0000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x7	pclk_core_root_div Divide pclk_core_root by (div_con + 1).

CRU_CLKSEL_CON18

Address: Operational Base(0xFF9A0000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	clk_dsmc_sel clk_dsmc clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
11:7	RW	0x03	clk_dsmc_div DT50 division register. Divide clk_dsmc by (div_con + 1).
6:5	RW	0x0	aclk_core_peri_root_sel aclk_core_peri_root clock mux. 2'b00: clk_gpll_mux_gate 2'b01: clk_v0pll_mux_gate 2'b10: clk_v1pll_mux_gate
4:0	RW	0x02	aclk_core_peri_root_div Divide aclk_core_peri_root by (div_con + 1).

CRU_CLKSEL_CON19

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Address: Operational Base(0xFF9A0000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x1	clk_flexbus_rx_sel clk_flexbus_rx clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
11:7	RW	0x03	clk_flexbus_rx_div DT50 division register. Divide clk_flexbus_rx by (div_con + 1).
6:5	RW	0x1	clk_flexbus_tx_sel clk_flexbus_tx clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
4:0	RW	0x03	clk_flexbus_tx_div DT50 division register. Divide clk_flexbus_tx by (div_con + 1).

CRU_CLKSEL_CON21

Address: Operational Base(0xFF9A0000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x1	hclk_bus_root_sel hclk_bus_root clock mux. 2'b00: clk_gpll_div 2'b01: clk_v0pll_div 2'b10: clk_v1pll_div
11:7	RW	0x00	hclk_bus_root_div Divide hclk_bus_root by (div_con + 1).
6:5	RW	0x0	aclk_bus_root_sel aclk_bus_root clock mux. 2'b00: clk_gpll_div 2'b01: clk_v0pll_div 2'b10: clk_v1pll_div

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	aclk_bus_root_div Divide aclk_bus_root by (div_con + 1).

CRU_CLKSEL_CON22

Address: Operational Base(0xFF9A0000) + offset (0x0358)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	clk_timer0_ch2_sel clk_timer0_ch2 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: sai2_mclk_io_in 3'b101: sai2_sclk_io_in
12:10	RW	0x0	clk_timer0_ch1_sel clk_timer0_ch1 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: sai1_mclk_io_in 3'b101: sai1_sclk_io_in
9:7	RW	0x0	clk_timer0_ch0_sel clk_timer0_ch0 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: sai0_mclk_io_in 3'b101: sai0_sclk_io_in
6:5	RW	0x0	pclk_bus_root_sel pclk_bus_root clock mux. 2'b00: clk_gpll_div 2'b01: clk_v0pll_div 2'b10: clk_v1pll_div
4:0	RW	0x01	pclk_bus_root_div Divide pclk_bus_root by (div_con + 1).

CRU_CLKSEL_CON23

Address: Operational Base(0xFF9A0000) + offset (0x035C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:9	RW	0x01	stclk_m0_div Divide stclk_m0 by (div_con + 1).
8:6	RW	0x0	clk_timer0_ch5_sel clk_timer0_ch5 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: mclk_asrc1
5:3	RW	0x0	clk_timer0_ch4_sel clk_timer0_ch4 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: mclk_asrc0
2:0	RW	0x0	clk_timer0_ch3_sel clk_timer0_ch3 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: sai3_mclk_io_in 3'b101: sai3_sclk_io_in

CRU_CLKSEL_CON29

Address: Operational Base(0xFF9A0000) + offset (0x0374)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	sclk_uart0_sel sclk_uart0 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_mux_gate 3'b010: clk_v0pll_mux_gate 3'b011: clk_frac_uart_matrix0 3'b100: clk_frac_uart_matrix1

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Bit	Attr	Reset Value	Description
			3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
11:7	RW	0x00	sclk_uart0_div Divide sclk_uart0 by (div_con + 1).
6:5	RW	0x0	hclk_lsperi_root_sel hclk_lsperi_root clock mux. 2'b00: clk_gpll_div 2'b01: clk_v0pll_div 2'b10: clk_v1pll_div
4:0	RW	0x01	hclk_lsperi_root_div Divide hclk_lsperi_root by (div_con + 1).

CRU_CLKSEL_CON30

Address: Operational Base(0xFF9A0000) + offset (0x0378)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	sclk_uart2_sel sclk_uart2 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_mux_gate 3'b010: clk_v0pll_mux_gate 3'b011: clk_frac_uart_matrix0 3'b100: clk_frac_uart_matrix1 3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
12:8	RW	0x00	sclk_uart2_div Divide sclk_uart2 by (div_con + 1).
7:5	RW	0x0	sclk_uart1_sel sclk_uart1 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_mux_gate 3'b010: clk_v0pll_mux_gate 3'b011: clk_frac_uart_matrix0 3'b100: clk_frac_uart_matrix1 3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
4:0	RW	0x00	sclk_uart1_div Divide sclk_uart1 by (div_con + 1).

Rockchip Confidencial

CRU_CLKSEL_CON31

Address: Operational Base(0xFF9A0000) + offset (0x037C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	sclk_uart4_sel sclk_uart4 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_mux_gate 3'b010: clk_v0pll_mux_gate 3'b011: clk_frac_uart_matrix0 3'b100: clk_frac_uart_matrix1 3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
12:8	RW	0x00	sclk_uart4_div Divide sclk_uart4 by (div_con + 1).
7:5	RW	0x0	sclk_uart3_sel sclk_uart3 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_mux_gate 3'b010: clk_v0pll_mux_gate 3'b011: clk_frac_uart_matrix0 3'b100: clk_frac_uart_matrix1 3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
4:0	RW	0x00	sclk_uart3_div Divide sclk_uart3 by (div_con + 1).

CRU_CLKSEL_CON32

Address: Operational Base(0xFF9A0000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x1	clk_i2c1_sel clk_i2c1 clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_div 2'b10: clk_v0pll_div 2'b11: clk_v1pll_div

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Bit	Attr	Reset Value	Description
9:6	RW	0x0	clk_i2c1_div Divide clk_i2c1 by (div_con + 1).
5:4	RW	0x1	clk_i2c0_sel clk_i2c0 clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_div 2'b10: clk_v0pll_div 2'b11: clk_v1pll_div
3:0	RW	0x0	clk_i2c0_div Divide clk_i2c0 by (div_con + 1).

CRU_CLKSEL_CON33

Address: Operational Base(0xFF9A0000) + offset (0x0384)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	clk_freq_pwm1_sel clk_freq_pwm1 clock mux. 4'b0000: clk_rc 4'b0001: sai0_mclk_io_in 4'b0010: sai1_mclk_io_in 4'b0011: sai2_mclk_io_in 4'b0100: sai3_mclk_io_in 4'b0101: sai0_sclk_io_in 4'b0110: sai1_sclk_io_in 4'b0111: sai2_sclk_io_in 4'b1000: sai3_sclk_io_in 4'b1001: mclk_asrc0 4'b1010: mclk_asrc1
11:10	RW	0x0	clk_pwm1_sel clk_pwm1 clock mux. 2'b00: clk_gpll_div 2'b01: clk_v0pll_div 2'b10: clk_v1pll_div
9:6	RW	0x1	clk_pwm1_div Divide clk_pwm1 by (div_con + 1).
5:4	RW	0x1	clk_i2c2_sel clk_i2c2 clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_div 2'b10: clk_v0pll_div 2'b11: clk_v1pll_div

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	clk_i2c2_div Divide clk_i2c2 by (div_con + 1).

CRU_CLKSEL_CON34

Address: Operational Base(0xFF9A0000) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	clk_spi1_sel clk_spi1 clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_div 2'b10: clk_v0pll_div 2'b11: clk_v1pll_div
13:10	RW	0x0	clk_spi1_div Divide clk_spi1 by (div_con + 1).
9:8	RW	0x1	clk_spi0_sel clk_spi0 clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_div 2'b10: clk_v0pll_div 2'b11: clk_v1pll_div
7:4	RW	0x0	clk_spi0_div Divide clk_spi0 by (div_con + 1).
3:0	RW	0x0	clk_counter_pwm1_sel clk_counter_pwm1 clock mux. 4'b0000: clk_rc 4'b0001: sai0_mclk_io_in 4'b0010: sai1_mclk_io_in 4'b0011: sai2_mclk_io_in 4'b0100: sai3_mclk_io_in 4'b0101: sai0_sclk_io_in 4'b0110: sai1_sclk_io_in 4'b0111: sai2_sclk_io_in 4'b1000: sai3_sclk_io_in 4'b1001: mclk_asrc0 4'b1010: mclk_asrc1

CRU_CLKSEL_CON35

Address: Operational Base(0xFF9A0000) + offset (0x038C)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:11	RW	0x2	clk_can0_sel clk_can0 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_mux 3'b010: clk_v0pll_mux_gate 3'b011: clk_v1pll_mux_gate 3'b100: clk_frac_voice_matrix1 3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
10:6	RW	0x03	clk_can0_div Divide clk_can0 by (div_con + 1).
5:4	RW	0x0	dbclk_gpio4_sel dbclk_gpio4 clock mux. 2'b00: xin_osc0_func 2'b01: clk_rc 2'b10: clk_deepslow
3:2	RW	0x0	dbclk_gpio3_sel dbclk_gpio3 clock mux. 2'b00: xin_osc0_func 2'b01: clk_rc 2'b10: clk_deepslow
1:0	RW	0x0	dbclk_gpio2_sel dbclk_gpio2 clock mux. 2'b00: xin_osc0_func 2'b01: clk_rc 2'b10: clk_deepslow

CRU_CLKSEL_CON36

Address: Operational Base(0xFF9A0000) + offset (0x0390)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:5	RW	0x2	clk_can1_sel clk_can1 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_mux

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Bit	Attr	Reset Value	Description
			3'b010: clk_v0pll_mux_gate 3'b011: clk_v1pll_mux_gate 3'b100: clk_frac_voice_matrix1 3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
4:0	RW	0x03	clk_can1_div Divide clk_can1 by (div_con + 1).

CRU_CLKSEL_CON37

Address: Operational Base(0xFF9A0000) + offset (0x0394)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8:5	RW	0x1	mclk_pdm_sel mclk_pdm clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in 4'b1101: clk_gpll_div
4:0	RW	0x00	mclk_pdm_div Divide mclk_pdm by (div_con + 1).

CRU_CLKSEL_CON38

Address: Operational Base(0xFF9A0000) + offset (0x0398)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:10	RW	0x1	clkout_pdm_sel clkout_pdm clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in 4'b1101: clk_gpll_div
9:0	RW	0x01f	clkout_pdm_div DT50 division register. Divide clkout_pdm by (div_con + 1).

CRU_CLKSEL_CON39

Address: Operational Base(0xFF9A0000) + offset (0x039C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	mclk_spdifrx_sel mclk_spdifrx clock mux. 2'b00: clk_gpll_mux_gate 2'b01: clk_v0pll_mux_gate 2'b10: clk_v1pll_mux_gate
13:9	RW	0x03	mclk_spdifrx_div Divide mclk_spdifrx by (div_con + 1).
8:5	RW	0x1	mclk_spdiftx_sel mclk_spdiftx clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2

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Bit	Attr	Reset Value	Description
			4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in
4:0	RW	0x00	mclk_spdiftx_div Divide mclk_spdiftx by (div_con + 1).

CRU_CLKSEL_CON40

Address: Operational Base(0xFF9A0000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x1	mclk_sai0_sel mclk_sai0 clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in
7:0	RW	0x00	mclk_sai0_div Divide mclk_sai0 by (div_con + 1).

CRU_CLKSEL_CON41

Address: Operational Base(0xFF9A0000) + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x1	mclk_sai1_sel mclk_sai1 clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in
7:0	RW	0x00	mclk_sai1_div Divide mclk_sai1 by (div_con + 1).

CRU_CLKSEL_CON42

Address: Operational Base(0xFF9A0000) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x1	clk_asrc1_sel clk_asrc1 clock mux. 2'b00: clk_gpll_mux_gate 2'b01: clk_v0pll_mux_gate 2'b10: clk_v1pll_mux_gate
11:7	RW	0x03	clk_asrc1_div Divide clk_asrc1 by (div_con + 1).
6:5	RW	0x1	clk_asrc0_sel clk_asrc0 clock mux. 2'b00: clk_gpll_mux_gate 2'b01: clk_v0pll_mux_gate 2'b10: clk_v1pll_mux_gate
4:0	RW	0x03	clk_asrc0_div Divide clk_asrc0 by (div_con + 1).

CRU_CLKSEL_CON46

Address: Operational Base(0xFF9A0000) + offset (0x03B8)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x1	mclk_asrc3_sel mclk_asrc1 clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in
11:8	RW	0x1	mclk_asrc2_sel mclk_asrc0 clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in
7:4	RW	0x1	mclk_asrc1_sel mclk_asrc1 clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in
3:0	RW	0x1	mclk_asrc0_sel mclk_asrc0 clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in

CRU_CLKSEL_CON47

Address: Operational Base(0xFF9A0000) + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	lrck_asrc1_dst_sel lrck_asrc1_dst clock mux. 4'b0000: mclk_asrc0 4'b0001: mclk_asrc1 4'b0010: mclk_asrc0 4'b0011: mclk_asrc1 4'b0100: mclk_spdiftx 4'b0101: clk_spdifrx_to_asrc 4'b0110: clkout_pdm 4'b0111: sai0_fs 4'b1000: sai1_fs 4'b1001: sai2_fs 4'b1010: sai3_fs 4'b1011: sai4_fs

Rockchip Confidencial

Bit	Attr	Reset Value	Description
11:8	RW	0x0	lrck_asrc1_src_sel lrck_asrc1_src clock mux. 4'b0000: mclk_asrc0 4'b0001: mclk_asrc1 4'b0010: mclk_asrc0 4'b0011: mclk_asrc1 4'b0100: mclk_spdiftx 4'b0101: clk_spdifrx_to_asrc 4'b0110: clkout_pdm 4'b0111: sai0_fs 4'b1000: sai1_fs 4'b1001: sai2_fs 4'b1010: sai3_fs 4'b1011: sai4_fs
7:4	RW	0x0	lrck_asrc0_dst_sel lrck_asrc0_dst clock mux. 4'b0000: mclk_asrc0 4'b0001: mclk_asrc1 4'b0010: mclk_asrc0 4'b0011: mclk_asrc1 4'b0100: mclk_spdiftx 4'b0101: clk_spdifrx_to_asrc 4'b0110: clkout_pdm 4'b0111: sai0_fs 4'b1000: sai1_fs 4'b1001: sai2_fs 4'b1010: sai3_fs 4'b1011: sai4_fs
3:0	RW	0x0	lrck_asrc0_src_sel lrck_asrc0_src clock mux. 4'b0000: mclk_asrc0 4'b0001: mclk_asrc1 4'b0010: mclk_asrc0 4'b0011: mclk_asrc1 4'b0100: mclk_spdiftx 4'b0101: clk_spdifrx_to_asrc 4'b0110: clkout_pdm 4'b0111: sai0_fs 4'b1000: sai1_fs 4'b1001: sai2_fs 4'b1010: sai3_fs 4'b1011: sai4_fs

CRU_CLKSEL_CON49

Address: Operational Base(0xFF9A0000) + offset (0x03C4)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x2	cclk_src_sdmmc_sel cclk_src_sdmmc clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
12:7	RW	0x03	cclk_src_sdmmc_div DT50 division register. Divide cclk_src_sdmmc by (div_con + 1).
6:5	RW	0x1	aclk_hsperi_root_sel aclk_hsperi_root clock mux. 2'b00: clk_gpll_div 2'b01: clk_v0pll_div 2'b10: clk_v1pll_div
4:0	RW	0x00	aclk_hsperi_root_div Divide aclk_hsperi_root by (div_con + 1).

CRU_CLKSEL_CON50

Address: Operational Base(0xFF9A0000) + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:7	RW	0x0f	clk_mac_root_div DT50 division register. Divide clk_mac_root by (div_con + 1).
6:5	RW	0x2	sclk_fspi_sel sclk_fspi clock mux. 2'b00: xin_osc0_func_gate 2'b01: clk_gpll_mux_gate 2'b10: clk_v0pll_mux_gate 2'b11: clk_v1pll_mux_gate
4:0	RW	0x09	sclk_fspi_div DT50 division register. Divide sclk_fspi by (div_con + 1).

CRU_CLKSEL_CON51

Address: Operational Base(0xFF9A0000) + offset (0x03CC)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x1	mclk_sai2_sel mclk_sai2 clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in
7:0	RW	0x00	mclk_sai2_div Divide mclk_sai2 by (div_con + 1).

CRU_CLKSEL_CON52

Address: Operational Base(0xFF9A0000) + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x1	mclk_sai3_src_sel mclk_sai3_src clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			4'b1100: sai3_mclk_io_in
7:0	RW	0x00	mclk_sai3_src_div Divide mclk_sai3_src by (div_con + 1).

CRU_CLKSEL_CON53

Address: Operational Base(0xFF9A0000) + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x1	mclk_sai4_src_sel mclk_sai4_src clock mux. 4'b0000: xin_osc0_func_gate 4'b0001: clk_int_voice_matrix0 4'b0010: clk_int_voice_matrix1 4'b0011: clk_int_voice_matrix2 4'b0100: clk_frac_voice_matrix0 4'b0101: clk_frac_voice_matrix1 4'b0110: clk_frac_common_matrix0 4'b0111: clk_frac_common_matrix1 4'b1000: clk_frac_common_matrix2 4'b1001: sai0_mclk_io_in 4'b1010: sai1_mclk_io_in 4'b1011: sai2_mclk_io_in 4'b1100: sai3_mclk_io_in
7:0	RW	0x01	mclk_sai4_src_div Divide mclk_sai4_src by (div_con + 1).

CRU_CLKSEL_CON54

Address: Operational Base(0xFF9A0000) + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:11	RW	0x0	sclk_uart5_sel sclk_uart5 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_mux_gate 3'b010: clk_v0pll_mux_gate 3'b011: clk_frac_uart_matrix0 3'b100: clk_frac_uart_matrix1

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
10:6	RW	0x00	sclk_uart5_div Divide sclk_uart5 by (div_con + 1).
5:4	RW	0x0	clk_saradc_sel clk_saradc clock mux. 2'b00: xin_osc0_func 2'b01: clk_rc 2'b10: clk_deepslow
3:0	RW	0x1	clk_saradc_div Divide clk_saradc by (div_con + 1).

CRU_CLKSEL_CON55

Address: Operational Base(0xFF9A0000) + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:5	RW	0x0	clk_mac_ptp_root_sel clk_mac_ptp_root clock mux. 2'b00: clk_gpll_mux 2'b01: clk_v0pll_mux 2'b10: clk_v1pll_mux
4:0	RW	0x07	clk_mac_ptp_root_div Divide clk_mac_ptp_root by (div_con + 1).

CRU_CLKSEL_CON58

Address: Operational Base(0xFF9A0000) + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	hclk_vio_root_sel hclk_vio_root clock mux. 2'b00: clk_gpll_div 2'b01: clk_v0pll_div 2'b10: clk_v1pll_div
11:7	RW	0x01	hclk_vio_root_div Divide hclk_vio_root by (div_con + 1).

Rockchip Confidencial

Bit	Attr	Reset Value	Description
6:5	RW	0x1	aclk_vio_root_sel aclk_vio_root clock mux. 2'b00: clk_gpll_mux_gate 2'b01: clk_v0pll_mux_gate 2'b10: clk_v1pll_mux_gate
4:0	RW	0x03	aclk_vio_root_div Divide aclk_vio_root by (div_con + 1).

CRU_CLKSEL_CON59

Address: Operational Base(0xFF9A0000) + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:5	RW	0x0	clk_core_rga_sel clk_core_rga clock mux. 2'b00: clk_gpll_mux_gate 2'b01: clk_v0pll_mux_gate 2'b10: clk_v1pll_mux_gate
4:0	RW	0x01	clk_core_rga_div Divide clk_core_rga by (div_con + 1).

CRU_CLKSEL_CON60

Address: Operational Base(0xFF9A0000) + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x2	dclk_vop_sel dclk_vop clock mux. 3'b000: xin_osc0_func_gate 3'b001: clk_gpll_mux_gate 3'b010: clk_v0pll_mux_gate 3'b011: clk_v1pll_mux_gate 3'b100: clk_frac_voice_matrix1 3'b101: clk_frac_common_matrix0 3'b110: clk_frac_common_matrix1 3'b111: clk_frac_common_matrix2
7:0	RW	0x09	dclk_vop_div Divide dclk_vop by (div_con + 1).

Rockchip Confidencial

CRU_CLKSEL_CON61

Address: Operational Base(0xFF9A0000) + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x1	clk_tsadc_tsen_div Divide clk_tsadc_tsen by (div_con + 1).
7:0	RW	0x13	clk_tsadc_div Divide clk_tsadc by (div_con + 1).

CRU_GATE_CON00

Address: Operational Base(0xFF9A0000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_frac_voice_matrix0_en clk_frac_voice_matrix0 clock gating control. When high, disable clock
14	RW	0x0	clk_frac_uart_matrix1_en clk_frac_uart_matrix1 clock gating control. When high, disable clock
13	RW	0x0	clk_frac_uart_matrix0_en clk_frac_uart_matrix0 clock gating control. When high, disable clock
12	RW	0x0	clk_testout_en clk_testout clock gating control. When high, disable clock
11	RW	0x0	clk_int_voice_matrix2_en clk_int_voice_matrix2 clock gating control. When high, disable clock
10	RW	0x0	clk_int_voice_matrix1_en clk_int_voice_matrix1 clock gating control. When high, disable clock
9	RW	0x0	clk_int_voice_matrix0_en clk_int_voice_matrix0 clock gating control. When high, disable clock
8	RW	0x0	clk_v1pll_div_en clk_v1pll_div clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7	RW	0x0	clk_v0pll_div_en clk_v0pll_div clock gating control. When high, disable clock
6	RW	0x0	clk_gpll_div_100m_en clk_gpll_div_100m clock gating control. When high, disable clock
5	RW	0x0	clk_gpll_div_en clk_gpll_div clock gating control. When high, disable clock
4	RW	0x0	clk_v1pll_mux_en clk_v1pll_mux_gate clock gating control. When high, disable clock
3	RW	0x0	clk_v0pll_mux_en clk_v0pll_mux_gate clock gating control. When high, disable clock
2	RW	0x0	clk_gpll_mux_en clk_gpll_mux_gate clock gating control. When high, disable clock
1	RW	0x0	xin_osc0_func_en xin_osc0_func_gate clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON01

Address: Operational Base(0xFF9A0000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	clk_ref_src_dphy_en clk_ref_dphy_top clock gating control. When high, disable clock
4	RW	0x0	clk_ref_src_usbphy_en clk_ref_usbphy_top clock gating control. When high, disable clock
3	RW	0x0	clk_frac_common_matrix2_en clk_frac_common_matrix2 clock gating control. When high, disable clock
2	RW	0x0	clk_frac_common_matrix1_en clk_frac_common_matrix1 clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
1	RW	0x0	clk_frac_common_matrix0_en clk_frac_common_matrix0 clock gating control. When high, disable clock
0	RW	0x0	clk_frac_voice_matrix1_en clk_frac_voice_matrix1 clock gating control. When high, disable clock

CRU_GATE_CON02

Address: Operational Base(0xFF9A0000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pclk_core_biu_en pclk_core_biu clock gating control. When high, disable clock
13	RW	0x0	aclk_core_biu_en aclk_core_biu clock gating control. When high, disable clock
12	RW	0x0	pclk_core_root_en pclk_core_root clock gating control. When high, disable clock
11	RW	0x0	aclk_core_root_en aclk_core_root clock gating control. When high, disable clock
10:2	RO	0x000	reserved
1	RW	0x0	clk_core_en clk_core clock gating control. When high, disable clock
0	RW	0x0	clk_core_div_en clk_core_src_div clock gating control. When high, disable clock

CRU_GATE_CON03

Address: Operational Base(0xFF9A0000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9	RW	0x0	dbclk_gpio1_en dbclk_gpio1 clock gating control. When high, disable clock
8	RW	0x0	pclk_gpio1_en pclk_gpio1 clock gating control. When high, disable clock
7	RW	0x0	clk_ref_pvtpll_core_en clk_ref_pvtpll_core clock gating control. When high, disable clock
6	RW	0x0	clk_core_ema_detect_en clk_core_ema_detect clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	pclk_core_grf_en pclk_core_grf clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	swclktck_en swclktck clock gating control. When high, disable clock
1	RW	0x0	pclk_dbg_en pclk_dbg clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON04

Address: Operational Base(0xFF9A0000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	hclk_dsmc_slv_en hclk_dsmc_slv clock gating control. When high, disable clock
11	RW	0x0	aclk_dsmc_slv_en aclk_dsmc_slv clock gating control. When high, disable clock
10	RW	0x0	hclk_flexbus_en hclk_flexbus clock gating control. When high, disable clock
9	RW	0x0	aclk_flexbus_en aclk_flexbus clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
8	RW	0x0	clk_flexbus_rx_en clk_flexbus_rx clock gating control. When high, disable clock
7	RW	0x0	clk_flexbus_tx_en clk_flexbus_tx clock gating control. When high, disable clock
6	RW	0x0	pclk_dsmc_en pclk_dsmc clock gating control. When high, disable clock
5	RW	0x0	aclk_dsmc_en aclk_dsmc clock gating control. When high, disable clock
4	RW	0x0	clk_dsmc_en clk_dsmc clock gating control. When high, disable clock
3	RW	0x0	aclk_core_peri_biu_en aclk_core_peri_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_core_peri_root_en pclk_core_peri_root clock gating control. When high, disable clock
1	RW	0x0	hclk_core_peri_root_en hclk_core_peri_root clock gating control. When high, disable clock
0	RW	0x0	aclk_core_peri_root_en aclk_core_peri_root clock gating control. When high, disable clock

CRU_GATE_CON05

Address: Operational Base(0xFF9A0000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hclk_crypto_en hclk_crypto clock gating control. When high, disable clock
14	RW	0x0	aclk_crypto_ns_en aclk_crypto_ns clock gating control. When high, disable clock
13	RW	0x0	clk_pka_crypto_ns_en clk_pka_crypto_ns clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12	RW	0x0	clk_core_crypto_ns_en clk_core_crypto_ns clock gating control. When high, disable clock
11	RW	0x0	swclktck_m0_en swclktck_m0 clock gating control. When high, disable clock
10	RW	0x0	hclk_m0_en hclk_m0 clock gating control. When high, disable clock
9	RW	0x0	aclk_dmac1_en aclk_dmac1 clock gating control. When high, disable clock
8	RW	0x0	aclk_dmac0_en aclk_dmac0 clock gating control. When high, disable clock
7	RW	0x0	hclk_sysram_en hclk_sysram clock gating control. When high, disable clock
6	RW	0x0	aclk_sysram_en aclk_sysram clock gating control. When high, disable clock
5	RW	0x0	pclk_bus_biu_en pclk_bus_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_bus_biu_en hclk_bus_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_bus_biu_en aclk_bus_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_bus_root_en pclk_bus_root clock gating control. When high, disable clock
1	RW	0x0	hclk_bus_root_en hclk_bus_root clock gating control. When high, disable clock
0	RW	0x0	aclk_bus_root_en aclk_bus_root clock gating control. When high, disable clock

CRU_GATE_CON06

Address: Operational Base(0xFF9A0000) + offset (0x0818)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_spinlock_en pclk_spinlock clock gating control. When high, disable clock
14	RW	0x0	pclk_intmux_en pclk_intmux clock gating control. When high, disable clock
13	RW	0x0	pclk_mailbox_en pclk_mailbox clock gating control. When high, disable clock
12	RW	0x0	tclk_wdt1_en tclk_wdt1 clock gating control. When high, disable clock
11	RW	0x0	pclk_wdt1_en pclk_wdt1 clock gating control. When high, disable clock
10	RW	0x0	tclk_wdt0_en tclk_wdt0 clock gating control. When high, disable clock
9	RW	0x0	pclk_wdt0_en pclk_wdt0 clock gating control. When high, disable clock
8	RW	0x0	clk_timer0_ch5_en clk_timer0_ch5 clock gating control. When high, disable clock
7	RW	0x0	clk_timer0_ch4_en clk_timer0_ch4 clock gating control. When high, disable clock
6	RW	0x0	clk_timer0_ch3_en clk_timer0_ch3 clock gating control. When high, disable clock
5	RW	0x0	clk_timer0_ch2_en clk_timer0_ch2 clock gating control. When high, disable clock
4	RW	0x0	clk_timer0_ch1_en clk_timer0_ch1 clock gating control. When high, disable clock
3	RW	0x0	clk_timer0_ch0_en clk_timer0_ch0 clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x0	pclk_timer0_en pclk_timer clock gating control. When high, disable clock
1	RW	0x0	pclk_bus_grf_en pclk_bus_grf clock gating control. When high, disable clock
0	RW	0x0	hclk_rng_en hclk_rng clock gating control. When high, disable clock

CRU_GATE_CON07

Address: Operational Base(0xFF9A0000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	pclk_usbphy_en pclk_usbphy clock gating control. When high, disable clock
10	RW	0x0	clk_usbotg1_adp_en clk_usbotg1_adp clock gating control. When high, disable clock
9	RW	0x0	hclk_usbotg1_pmu_en hclk_usbotg1_pmu clock gating control. When high, disable clock
8	RW	0x0	hclk_usbotg1_en hclk_usbotg1 clock gating control. When high, disable clock
7	RW	0x0	clk_usbotg0_adp_en clk_usbotg0_adp clock gating control. When high, disable clock
6	RW	0x0	hclk_usbotg0_pmu_en hclk_usbotg0_pmu clock gating control. When high, disable clock
5	RW	0x0	hclk_usbotg0_en hclk_usbotg0 clock gating control. When high, disable clock
4	RW	0x0	pclk_ddr_lpc_en pclk_stdby clock gating control. When high, disable clock
3	RW	0x0	clk_ddrmon_osc_en clk_ddrmon_osc clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x0	pclk_ddrmon_en pclk_ddrmon clock gating control. When high, disable clock
1	RW	0x0	hclk_ddrphy_en hclk_ddrphy clock gating control. When high, disable clock
0	RW	0x0	pclk_ddrc_en pclk_ddrc clock gating control. When high, disable clock

CRU_GATE_CON08

Address: Operational Base(0xFF9A0000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	stclk_m0_en stclk_m0 clock gating control. When high, disable clock
1	RW	0x0	pclk_dma2ddr_en pclk_dma2ddr clock gating control. When high, disable clock
0	RW	0x0	aclk_dma2ddr_en aclk_dma2ddr clock gating control. When high, disable clock

CRU_GATE_CON10

Address: Operational Base(0xFF9A0000) + offset (0x0828)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	clk_ddrmon_en clk_ddrmon clock gating control. When high, disable clock
3	RW	0x0	clk_ddrc_en clk_ddrc clock gating control. When high, disable clock
2	RW	0x0	aclk_ddr_biu_en aclk_ddr_biu clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
1	RW	0x0	aclk_ddrc_1_en aclk_ddrc_1 clock gating control. When high, disable clock
0	RW	0x0	aclk_ddrc_0_en aclk_ddrc_0 clock gating control. When high, disable clock

CRU_GATE_CON11

Address: Operational Base(0xFF9A0000) + offset (0x082C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_i2c0_en clk_i2c0 clock gating control. When high, disable clock
14	RW	0x0	pclk_i2c0_en pclk_i2c0 clock gating control. When high, disable clock
13	RW	0x0	sclk_uart4_src_en sclk_uart4 clock gating control. When high, disable clock
12	RW	0x0	sclk_uart3_src_en sclk_uart3 clock gating control. When high, disable clock
11	RW	0x0	sclk_uart2_src_en sclk_uart2 clock gating control. When high, disable clock
10	RW	0x0	sclk_uart1_src_en sclk_uart1 clock gating control. When high, disable clock
9	RW	0x0	sclk_uart0_src_en sclk_uart0 clock gating control. When high, disable clock
8	RW	0x0	pclk_uart4_en pclk_uart4 clock gating control. When high, disable clock
7	RW	0x0	pclk_uart3_en pclk_uart3 clock gating control. When high, disable clock
6	RW	0x0	pclk_uart2_en pclk_uart2 clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	pclk_uart1_en pclk_uart1 clock gating control. When high, disable clock
4	RW	0x0	pclk_uart0_en pclk_uart0 clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	hclk_lsperi_biu_en hclk_lsperi_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_lsperi_root_en pclk_lsperi_root clock gating control. When high, disable clock
0	RW	0x0	hclk_lsperi_root_en hclk_lsperi_root clock gating control. When high, disable clock

CRU_GATE_CON12

Address: Operational Base(0xFF9A0000) + offset (0x0830)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dbclk_gpio2_en dbclk_gpio2 clock gating control. When high, disable clock
14	RW	0x0	pclk_gpio2_en pclk_gpio2 clock gating control. When high, disable clock
13	RW	0x0	clk_spi1_en clk_spi1 clock gating control. When high, disable clock
12	RW	0x0	pclk_spi1_en pclk_spi1 clock gating control. When high, disable clock
11	RW	0x0	clk_spi0_en clk_spi0 clock gating control. When high, disable clock
10	RW	0x0	pclk_spi0_en pclk_spi0 clock gating control. When high, disable clock
9	RW	0x0	clk_counter_pwm1_en clk_counter_pwm1 clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
8	RW	0x0	clk_freq_pwm1_en clk_freq_pwm1 clock gating control. When high, disable clock
7	RW	0x0	clk_rc_pwm1_en clk_rc_pwm1 clock gating control. When high, disable clock
6	RW	0x0	clk_osc_pwm1_en clk_osc_pwm1 clock gating control. When high, disable clock
5	RW	0x0	clk_pwm1_en clk_pwm1 clock gating control. When high, disable clock
4	RW	0x0	pclk_pwm1_en pclk_pwm1 clock gating control. When high, disable clock
3	RW	0x0	clk_i2c2_en clk_i2c2 clock gating control. When high, disable clock
2	RW	0x0	pclk_i2c2_en pclk_i2c2 clock gating control. When high, disable clock
1	RW	0x0	clk_i2c1_en clk_i2c1 clock gating control. When high, disable clock
0	RW	0x0	pclk_i2c1_en pclk_i2c1 clock gating control. When high, disable clock

CRU_GATE_CON13

Address: Operational Base(0xFF9A0000) + offset (0x0834)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mclk_sai0_en mclk_sai0 clock gating control. When high, disable clock
14	RW	0x0	mclk_spdifrx_en mclk_spdifrx clock gating control. When high, disable clock
13	RW	0x0	hclk_spdifrx_en hclk_spdifrx clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12	RW	0x0	hclk_spdiftx_en hclk_spdiftx clock gating control. When high, disable clock
11	RW	0x0	mclk_spdiftx_en mclk_spdiftx clock gating control. When high, disable clock
10	RW	0x0	clkout_pdm_en clkout_pdm clock gating control. When high, disable clock
9	RW	0x0	mclk_pdm_en mclk_pdm clock gating control. When high, disable clock
8	RW	0x0	hclk_pdm_en hclk_pdm clock gating control. When high, disable clock
7	RW	0x0	clk_can1_en clk_can1 clock gating control. When high, disable clock
6	RW	0x0	pclk_can1_en hclk_can1 clock gating control. When high, disable clock
5	RW	0x0	clk_can0_en clk_can0 clock gating control. When high, disable clock
4	RW	0x0	pclk_can0_en hclk_can0 clock gating control. When high, disable clock
3	RW	0x0	dbclk_gpio4_en dbclk_gpio4 clock gating control. When high, disable clock
2	RW	0x0	pclk_gpio4_en pclk_gpio4 clock gating control. When high, disable clock
1	RW	0x0	dbclk_gpio3_en dbclk_gpio3 clock gating control. When high, disable clock
0	RW	0x0	pclk_gpio3_en pclk_gpio3 clock gating control. When high, disable clock

CRU_GATE_CON14

Address: Operational Base(0xFF9A0000) + offset (0x0838)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	pclk_pmu_root_en pclk_pmu_root clock gating control. When high, disable clock
9	RW	0x0	pclk_cru_en pclk_cru clock gating control. When high, disable clock
8	RW	0x0	clk_asrc1_en clk_asrc1 clock gating control. When high, disable clock
7	RW	0x0	hclk_asrc1_en hclk_asrc1 clock gating control. When high, disable clock
6	RW	0x0	clk_asrc0_en clk_asrc0 clock gating control. When high, disable clock
5	RW	0x0	hclk_asrc0_en hclk_asrc0 clock gating control. When high, disable clock
4	RW	0x0	mclk_out_sai1_en mclk_out_sai1 clock gating control. When high, disable clock
3	RW	0x0	hclk_sai1_en hclk_sai1 clock gating control. When high, disable clock
2	RW	0x0	mclk_sai1_en mclk_sai1 clock gating control. When high, disable clock
1	RW	0x0	mclk_out_sai0_en mclk_out_sai0 clock gating control. When high, disable clock
0	RW	0x0	hclk_sai0_en hclk_sai0 clock gating control. When high, disable clock

CRU_GATE_CON16

Address: Operational Base(0xFF9A0000) + offset (0x0840)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	lrck_asrc1_dst_en lrck_asrc1_dst clock gating control. When high, disable clock
6	RW	0x0	lrck_asrc1_src_en lrck_asrc1_src clock gating control. When high, disable clock
5	RW	0x0	lrck_asrc0_dst_en lrck_asrc0_dst clock gating control. When high, disable clock
4	RW	0x0	lrck_asrc0_src_en lrck_asrc0_src clock gating control. When high, disable clock
3	RW	0x0	mclk_asrc3_src_en mclk_asrc1 clock gating control. When high, disable clock
2	RW	0x0	mclk_asrc2_src_en mclk_asrc0 clock gating control. When high, disable clock
1	RW	0x0	mclk_asrc1_src_en mclk_asrc1 clock gating control. When high, disable clock
0	RW	0x0	mclk_asrc0_src_en mclk_asrc0 clock gating control. When high, disable clock

CRU_GATE_CON17

Address: Operational Base(0xFF9A0000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_mac_root_en clk_mac_root clock gating control. When high, disable clock
14	RW	0x0	pclk_mac1_en pclk_mac1 clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
13	RW	0x0	pclk_mac0_en pclk_mac0 clock gating control. When high, disable clock
12	RW	0x0	aclk_mac1_en aclk_mac1 clock gating control. When high, disable clock
11	RW	0x0	aclk_mac0_en aclk_mac0 clock gating control. When high, disable clock
10	RW	0x0	pclk_spi2_en pclk_spi2 clock gating control. When high, disable clock
9	RW	0x0	sclk_fspi_en sclk_fspi clock gating control. When high, disable clock
8	RW	0x0	hclk_fspi_en hclk_fspi clock gating control. When high, disable clock
7	RW	0x0	hclk_sdmmc_en hclk_sdmmc clock gating control. When high, disable clock
6	RW	0x0	cclk_src_sdmmc_en cclk_src_sdmmc clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	hclk_hsperi_biu_en hclk_hsperi_biu clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	pclk_hsperi_root_en pclk_hsperi_root clock gating control. When high, disable clock
1	RW	0x0	hclk_hsperi_root_en hclk_hsperi_root clock gating control. When high, disable clock
0	RW	0x0	aclk_hsperiroot_en aclk_hsperi_root clock gating control. When high, disable clock

CRU_GATE_CON18

Address: Operational Base(0xFF9A0000) + offset (0x0848)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			1'b1: Write access enable
15	RW	0x0	mclk_audio_adc_en mclk_audio_adc clock gating control. When high, disable clock
14	RW	0x0	pclk_audio_adc_en pclk_audio_adc clock gating control. When high, disable clock
13	RW	0x0	mclk_dsm_en mclk_dsm clock gating control. When high, disable clock
12	RW	0x0	hclk_dsm_en hclk_dsm clock gating control. When high, disable clock
11	RW	0x0	mclk_sai4_en mclk_sai4 clock gating control. When high, disable clock
10	RW	0x0	hclk_sai4_en hclk_sai4 clock gating control. When high, disable clock
9	RW	0x0	mclk_sai4_src_en mclk_sai4_src clock gating control. When high, disable clock
8	RW	0x0	mclk_out_sai3_en mclk_out_sai3 clock gating control. When high, disable clock
7	RW	0x0	mclk_sai3_en mclk_sai3 clock gating control. When high, disable clock
6	RW	0x0	hclk_sai3_en hclk_sai3 clock gating control. When high, disable clock
5	RW	0x0	mclk_sai3_src_en mclk_sai3_src clock gating control. When high, disable clock
4	RW	0x0	mclk_out_sai2_en mclk_out_sai2 clock gating control. When high, disable clock
3	RW	0x0	hclk_sai2_en hclk_sai2 clock gating control. When high, disable clock
2	RW	0x0	mclk_sai2_en mclk_sai2 clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
1	RW	0x0	clk_mac1_en clk_mac1 clock gating control. When high, disable clock
0	RW	0x0	clk_mac0_en clk_mac0 clock gating control. When high, disable clock

CRU_GATE_CON19

Address: Operational Base(0xFF9A0000) + offset (0x084C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	clk_mac1_ptp_en clk_mac1_ptp clock gating control. When high, disable clock
10	RW	0x0	clk_mac0_ptp_en clk_mac0_ptp clock gating control. When high, disable clock
9	RW	0x0	clk_mac_ptp_root_en clk_mac_ptp_root clock gating control. When high, disable clock
8	RW	0x0	pclk_gpio234_ioc_en pclk_gpio234_ioc clock gating control. When high, disable clock
7	RW	0x0	sclk_uart5_en sclk_uart5 clock gating control. When high, disable clock
6	RW	0x0	pclk_uart5_en pclk_uart5 clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	clk_sbpi_otpc_ns_en clk_sbpi_otpc_ns clock gating control. When high, disable clock
3	RW	0x0	pclk_otpc_ns_en pclk_otpc_ns clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	clk_saradc_en clk_saradc clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RW	0x0	pclk_saradc_en pclk_saradc clock gating control. When high, disable clock

CRU_GATE_CON20

Address: Operational Base(0xFF9A0000) + offset (0x0850)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	clk_spi2_en clk_spi2 clock gating control. When high, disable clock

CRU_GATE_CON21

Address: Operational Base(0xFF9A0000) + offset (0x0854)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_tsadc_en clk_tsadc clock gating control. When high, disable clock
14	RW	0x0	pclk_tsadc_en pclk_tsadc clock gating control. When high, disable clock
13	RW	0x0	pclk_dsi_host_en pclk_dsi_host clock gating control. When high, disable clock
12	RW	0x0	pclk_dphy_en pclk_dphy clock gating control. When high, disable clock
11	RW	0x0	dclk_vop_en dclk_vop clock gating control. When high, disable clock
10	RW	0x0	hclk_vop_en hclk_vop clock gating control. When high, disable clock
9	RW	0x0	aclk_vop_en aclk_vop clock gating control. When high, disable clock

Rockchip Confidencial

Bit	Attr	Reset Value	Description
8	RW	0x0	clk_core_rga_en clk_core_rga clock gating control. When high, disable clock
7	RW	0x0	aclk_rga_en aclk_rga clock gating control. When high, disable clock
6	RW	0x0	hclk_rga_en hclk_rga clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	hclk_vio_biu_en hclk_vio_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_vio_biu_en aclk_vio_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_vio_root_en pclk_vio_root clock gating control. When high, disable clock
1	RW	0x0	hclk_vio_root_en hclk_vio_root clock gating control. When high, disable clock
0	RW	0x0	aclk_vio_root_en aclk_vio_root clock gating control. When high, disable clock

CRU_GATE_CON22

Address: Operational Base(0xFF9A0000) + offset (0x0858)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	pclk_gpio1_ioc_en pclk_gpio1_ioc clock gating control. When high, disable clock
0	RW	0x0	clk_tsadc_tsen_en clk_tsadc_tsen clock gating control. When high, disable clock

CRU_SOFTRST_CON00

Address: Operational Base(0xFF9A0000) + offset (0x0A00)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	W1T	0x0	hresetn_m0_ac When high, reset relative logic
9	W1T	0x0	aresetn_core_biu_ac When high, reset relative logic
8	W1T	0x0	nl2reset_ac When high, reset relative logic
7	RO	0x0	reserved
6	W1T	0x0	ncoreset2_ac When high, reset relative logic
5	W1T	0x0	ncoreset1_ac When high, reset relative logic
4	W1T	0x0	ncoreset0_ac When high, reset relative logic
3	RO	0x0	reserved
2	W1T	0x0	ncoreporeset2_ac When high, reset relative logic
1	W1T	0x0	ncoreporeset1_ac When high, reset relative logic
0	W1T	0x0	ncoreporeset0_ac When high, reset relative logic

CRU_SOFTRST_CON02

Address: Operational Base(0xFF9A0000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_pmu When high, reset relative logic
14	RW	0x0	presetn_core_biu When high, reset relative logic
13:11	RO	0x0	reserved
10	RW	0x0	ndbgreset When high, reset relative logic
9:0	RO	0x000	reserved

CRU_SOFTRST_CON03

Address: Operational Base(0xFF9A0000) + offset (0x0A0C)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	dbresetn_gpio1 When high, reset relative logic
8	RW	0x0	presetn_gpio1 When high, reset relative logic
7	RW	0x0	resetn_ref_pvtpll_core When high, reset relative logic
6	RW	0x0	resetn_core_ema_detect When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	presetn_core_grf When high, reset relative logic
3	RO	0x0	reserved
2	RW	0x0	potresetn_dbg When high, reset relative logic
1	RW	0x0	presetn_dbg When high, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST_CON04

Address: Operational Base(0xFF9A0000) + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_dsmc_slv When high, reset relative logic
12	RW	0x0	hresetn_dsmc_slv When high, reset relative logic
11	RW	0x0	aresetn_dsmc_slv When high, reset relative logic
10	RW	0x0	hresetn_flexbus When high, reset relative logic
9	RW	0x0	aresetn_flexbus When high, reset relative logic
8	RO	0x0	reserved
7	RW	0x0	resetn_flexbus When high, reset relative logic

Rockchip Confidencial

Bit	Attr	Reset Value	Description
6	RW	0x0	presetn_dsmc When high, reset relative logic
5	RW	0x0	aresetn_dsmc When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	aresetn_core_peri_biu When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON05

Address: Operational Base(0xFF9A0000) + offset (0x0A14)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hresetn_crypto When high, reset relative logic
14:12	RO	0x0	reserved
11	RW	0x0	resetn_m0_jtag When high, reset relative logic
10	RW	0x0	hresetn_m0 When high, reset relative logic
9	RW	0x0	aresetn_dmac1 When high, reset relative logic
8	RW	0x0	aresetn_dmac0 When high, reset relative logic
7	RW	0x0	hresetn_sysram When high, reset relative logic
6	RW	0x0	aresetn_sysram When high, reset relative logic
5	RW	0x0	presetn_bus_biu When high, reset relative logic
4	RW	0x0	hresetn_bus_biu When high, reset relative logic
3	RW	0x0	aresetn_bus_biu When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON06

Address: Operational Base(0xFF9A0000) + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable

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Bit	Attr	Reset Value	Description
			1'b1: Write access enable
15	RW	0x0	presetn_spinlock When high, reset relative logic
14	RW	0x0	presetn_intmux When high, reset relative logic
13	RW	0x0	presetn_mailbox When high, reset relative logic
12	RW	0x0	tresetn_wdt1 When high, reset relative logic
11	RW	0x0	presetn_wdt1 When high, reset relative logic
10	RW	0x0	tresetn_wdt0 When high, reset relative logic
9	RW	0x0	presetn_wdt0 When high, reset relative logic
8	RW	0x0	resetn_timer0_ch5 When high, reset relative logic
7	RW	0x0	resetn_timer0_ch4 When high, reset relative logic
6	RW	0x0	resetn_timer0_ch3 When high, reset relative logic
5	RW	0x0	resetn_timer0_ch2 When high, reset relative logic
4	RW	0x0	resetn_timer0_ch1 When high, reset relative logic
3	RW	0x0	resetn_timer0_ch0 When high, reset relative logic
2	RW	0x0	presetn_timer0 When high, reset relative logic
1	RW	0x0	presetn_bus_grf When high, reset relative logic
0	RW	0x0	hresetn_rng When high, reset relative logic

CRU_SOFTRST_CON07

Address: Operational Base(0xFF9A0000) + offset (0x0A1C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	resetn_usbphy_otg1 When high, reset relative logic

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Bit	Attr	Reset Value	Description
13	RW	0x0	resetn_usbphy_otg0 When high, reset relative logic
12	RW	0x0	resetn_usbphy_por When high, reset relative logic
11	RW	0x0	presetn_usbphy When high, reset relative logic
10	RW	0x0	resetn_usbotg1_adp When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	hresetn_usbotg1 When high, reset relative logic
7	RW	0x0	resetn_usbotg0_adp When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	hresetn_usbotg0 When high, reset relative logic
4	RW	0x0	presetn_ddr_lpc When high, reset relative logic
3	RW	0x0	resetn_ddrmon_osc When high, reset relative logic
2	RW	0x0	presetn_ddrmon When high, reset relative logic
1	RW	0x0	hresetn_ddrphy When high, reset relative logic
0	RW	0x0	presetn_ddrc When high, reset relative logic

CRU_SOFTRST_CON08

Address: Operational Base(0xFF9A0000) + offset (0x0A20)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	presetn_dma2ddr When high, reset relative logic
0	RW	0x0	aresetn_dma2ddr When high, reset relative logic

CRU_SOFTRST_CON09

Address: Operational Base(0xFF9A0000) + offset (0x0A24)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual.

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Bit	Attr	Reset Value	Description
			1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	resetn_usbotg1_utmi When high, reset relative logic
0	RW	0x0	resetn_usbotg0_utmi When high, reset relative logic

CRU_SOFTRST_CON10

Address: Operational Base(0xFF9A0000) + offset (0x0A28)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	resetn_ddrmon When high, reset relative logic
3	RW	0x0	resetn_ddrc When high, reset relative logic
2	RW	0x0	aresetn_ddr_biu When high, reset relative logic
1	RW	0x0	aresetn_ddrc_1 When high, reset relative logic
0	RW	0x0	aresetn_ddrc_0 When high, reset relative logic

CRU_SOFTRST_CON11

Address: Operational Base(0xFF9A0000) + offset (0x0A2C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_i2c0 When high, reset relative logic
14	RW	0x0	presetn_i2c0 When high, reset relative logic
13	RW	0x0	resetn_uart4 When high, reset relative logic
12	RW	0x0	resetn_uart3 When high, reset relative logic
11	RW	0x0	resetn_uart2 When high, reset relative logic

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Bit	Attr	Reset Value	Description
10	RW	0x0	resetn_uart1 When high, reset relative logic
9	RW	0x0	resetn_uart0 When high, reset relative logic
8	RW	0x0	presetn_uart4 When high, reset relative logic
7	RW	0x0	presetn_uart3 When high, reset relative logic
6	RW	0x0	presetn_uart2 When high, reset relative logic
5	RW	0x0	presetn_uart1 When high, reset relative logic
4	RW	0x0	presetn_uart0 When high, reset relative logic
3	RO	0x0	reserved
2	RW	0x0	hresetn_lsperi_biu When high, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON12

Address: Operational Base(0xFF9A0000) + offset (0x0A30)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dbresetn_gpio2 When high, reset relative logic
14	RW	0x0	presetn_gpio2 When high, reset relative logic
13	RW	0x0	resetn_spi1 When high, reset relative logic
12	RW	0x0	presetn_spi1 When high, reset relative logic
11	RW	0x0	resetn_spi0 When high, reset relative logic
10	RW	0x0	presetn_spi0 When high, reset relative logic
9:6	RO	0x0	reserved
5	RW	0x0	resetn_pwm1 When high, reset relative logic
4	RW	0x0	presetn_pwm1 When high, reset relative logic
3	RW	0x0	resetn_i2c2 When high, reset relative logic

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Bit	Attr	Reset Value	Description
2	RW	0x0	presetn_i2c2 When high, reset relative logic
1	RW	0x0	resetn_i2c1 When high, reset relative logic
0	RW	0x0	presetn_i2c1 When high, reset relative logic

CRU_SOFTRST_CON13

Address: Operational Base(0xFF9A0000) + offset (0x0A34)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mresetn_sai0 When high, reset relative logic
14	RW	0x0	resetn_spdifrx When high, reset relative logic
13	RW	0x0	hresetn_spdifrx When high, reset relative logic
12	RW	0x0	hresetn_spdiftx When high, reset relative logic
11	RW	0x0	resetn_spdiftx When high, reset relative logic
10	RW	0x0	resetn_pdm When high, reset relative logic
9	RW	0x0	mresetn_pdm When high, reset relative logic
8	RW	0x0	hresetn_pdm When high, reset relative logic
7	RW	0x0	resetn_can1 When high, reset relative logic
6	RW	0x0	hresetn_can1 When high, reset relative logic
5	RW	0x0	resetn_can0 When high, reset relative logic
4	RW	0x0	hresetn_can0 When high, reset relative logic
3	RW	0x0	dbresetn_gpio4 When high, reset relative logic
2	RW	0x0	presetn_gpio4 When high, reset relative logic
1	RW	0x0	dbresetn_gpio3 When high, reset relative logic

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Bit	Attr	Reset Value	Description
0	RW	0x0	presetn_gpio3 When high, reset relative logic

CRU_SOFTRST_CON14

Address: Operational Base(0xFF9A0000) + offset (0x0A38)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	resetn_asrc1 When high, reset relative logic
7	RW	0x0	hresetn_asrc1 When high, reset relative logic
6	RW	0x0	resetn_asrc0 When high, reset relative logic
5	RW	0x0	hresetn_asrc0 When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	hresetn_sai1 When high, reset relative logic
2	RW	0x0	mresetn_sai1 When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	hresetn_sai0 When high, reset relative logic

CRU_SOFTRST_CON17

Address: Operational Base(0xFF9A0000) + offset (0x0A44)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	aresetn_mac1 When high, reset relative logic
11	RW	0x0	aresetn_mac0 When high, reset relative logic
10	RW	0x0	presetn_spi2 When high, reset relative logic
9	RW	0x0	sresetn_fspi When high, reset relative logic

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Bit	Attr	Reset Value	Description
8	RW	0x0	hresetn_fspi When high, reset relative logic
7	RW	0x0	hresetn_sdmmc When high, reset relative logic
6:5	RO	0x0	reserved
4	RW	0x0	hresetn_hsperi_biu When high, reset relative logic
3:0	RO	0x0	reserved

CRU_SOFTRST_CON18

Address: Operational Base(0xFF9A0000) + offset (0x0A48)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mresetn_audio_adc When high, reset relative logic
14	RW	0x0	presetn_audio_adc When high, reset relative logic
13	RW	0x0	mresetn_dsm When high, reset relative logic
12	RW	0x0	hresetn_dsm When high, reset relative logic
11	RW	0x0	mresetn_sai4 When high, reset relative logic
10	RW	0x0	hresetn_sai4 When high, reset relative logic
9:8	RO	0x0	reserved
7	RW	0x0	mresetn_sai3 When high, reset relative logic
6	RW	0x0	hresetn_sai3 When high, reset relative logic
5:4	RO	0x0	reserved
3	RW	0x0	hresetn_sai2 When high, reset relative logic
2	RW	0x0	mresetn_sai2 When high, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON19

Address: Operational Base(0xFF9A0000) + offset (0x0A4C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	presetn_gpio234_ioc When high, reset relative logic
7	RW	0x0	resetn_uart5 When high, reset relative logic
6	RW	0x0	presetn_uart5 When high, reset relative logic
5	RW	0x0	resetn_user_otpc_ns When high, reset relative logic
4	RW	0x0	resetn_sbpi_otpc_ns When high, reset relative logic
3	RW	0x0	presetn_otpc_ns When high, reset relative logic
2	RW	0x0	resetn_saradc_phy When high, reset relative logic
1	RW	0x0	resetn_saradc When high, reset relative logic
0	RW	0x0	presetn_saradc When high, reset relative logic

CRU_SOFTRST_CON21

Address: Operational Base(0xFF9A0000) + offset (0x0A54)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_tsadc When high, reset relative logic
14	RW	0x0	presetn_tsadc When high, reset relative logic
13	RW	0x0	presetn_dsi_host When high, reset relative logic
12	RW	0x0	presetn_dphy When high, reset relative logic
11	RW	0x0	resetn_vop When high, reset relative logic
10	RW	0x0	hresetn_vop When high, reset relative logic
9	RW	0x0	aresetn_vop When high, reset relative logic

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Bit	Attr	Reset Value	Description
8	RW	0x0	resetn_core_rga When high, reset relative logic
7	RW	0x0	aresetn_rga When high, reset relative logic
6	RW	0x0	hresetn_rga When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	hresetn_vio_biu When high, reset relative logic
3	RW	0x0	aresetn_vio_biu When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON22

Address: Operational Base(0xFF9A0000) + offset (0x0A58)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	presetn_gpio1_ioc When high, reset relative logic
0	RO	0x0	reserved

CRU_GLB_CNT_TH

Address: Operational Base(0xFF9A0000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000064	global_reset_counter_threshold Global soft reset, WDT reset or tsadc_shut reset asserted time counter threshold. Measured in OSC clock cycles.

CRU_GLB_RST_ST

Address: Operational Base(0xFF9A0000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	wdt1_s_src_st If High, global reset by wdt1_s_src
11	RW	0x0	wdt0_s_src_st If High, global reset by wdt0_s_src
10:8	RO	0x0	reserved
7	RW	0x0	glbrst_wdt1_rst_st If High, global reset by WDT1

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Bit	Attr	Reset Value	Description
6	RW	0x0	glbrst_wdt0_rst_st If High, global reset by WDT0
5	RW	0x0	snd_glb_wdt_rst_st Second global WDT triggered reset flag 1'b0: Last hot reset is not second global WDT triggered reset 1'b1: Last hot reset is second global WDT triggered reset
4	RW	0x0	fst_glb_wdt_rst_st First global WDT triggered reset flag 1'b0: Last hot reset is not first global WDT triggered reset 1'b1: Last hot reset is first global WDT triggered reset
3	RW	0x0	snd_glb_tsadc_rst_st Second global TSADC triggered reset flag 1'b0: Last hot reset is not second global TSADC triggered reset 1'b1: Last hot reset is second global TSADC triggered reset
2	RW	0x0	fst_glb_tsadc_rst_st First global TSADC triggered reset flag 1'b0: Last hot reset is not first global TSADC triggered reset 1'b1: Last hot reset is first global TSADC triggered reset
1	RW	0x0	snd_glb_rst_st Second global reset flag 1'b0: Last hot reset is not second global reset 1'b1: Last hot reset is second global reset
0	RW	0x0	fst_glb_rst_st First global reset flag 1'b0: Last hot reset is not first global reset 1'b1: Last hot reset is first global reset

CRU_GLB_SRST_FST_VALUE

Address: Operational Base(0xFF9A0000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	glb_srsc_first_value The first global software reset config value. Set 0xfdb9 enable.

CRU_GLB_SRST_SND_VALUE

Address: Operational Base(0xFF9A0000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	glb_srsc_second_value The second global software reset config value. Set 0xeca8 enable.

CRU_GLB_RST_CON

Address: Operational Base(0xFF9A0000) + offset (0x0C10)

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Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	cru_wdt1_con 1'b0: WDT1 trigger second global reset 1'b1: WDT1 trigger first global reset
11	RW	0x0	cru_wdt0_con 1'b0: WDT0 trigger second global reset 1'b1: WDT0 trigger first global reset
10:8	RO	0x0	reserved
7	RW	0x0	cru_wdt1_en 1'b0: WDT1 trigger global reset disable 1'b1: WDT1 trigger global reset enable
6	RW	0x0	cru_wdt0_en 1'b0: WDT0 trigger global reset disable 1'b1: WDT0 trigger global reset enable
5	RW	0x0	tsadc_wdt_glb_expend_en TSADC and WDT trigger global reset expend enable
4	RW	0x0	pmu_srst_wdt_en 1'b0: Disable WDT reset as PMU reset source 1'b1: Enable WDT reset as PMU reset source
3	RW	0x0	pmu_srst_glb_en 1'b0: Global reset trigger PMU reset disable 1'b1: Global reset trigger PMU reset enable
2	RW	0x0	pmu_srst_glb_ctrl 1'b0: Enable second global reset as PMU reset source 1'b1: Enable first global reset as PMU reset source It active when glb_rst_con[3] enable
1	RW	0x0	tsadc_glb_srst_en 1'b0: TSADC trigger global reset disable 1'b1: TSADC trigger global reset enable
0	RW	0x0	tsadc_glb_srst_ctrl 1'b0: TSADC trigger second global reset 1'b1: TSADC trigger first global reset

CRU_COREWFI_CON

Address: Operational Base(0xFF9A0000) + offset (0x0C2C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	corepo_srst_wfien WFI enable for core power-on soft reset
0	RW	0x0	core_srst_wfien WFI enable for core soft reset

2.5 SCRU Register Description

2.5.1 Registers Summary

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Name	Offset	Size	Reset Value	Description
SCRU_CLKSEL_CON104	0x0010	W	0x00001180	Internal clock select and division register 104
SCRU_CLKSEL_CON105	0x0014	W	0x00000000	Internal clock select and division register 105
SCRU_CLKSEL_CON106	0x0018	W	0x00000000	Internal clock select and division register 106
SCRU_GATE_CON60	0x0040	W	0x00000000	Internal clock gate and division register 60
SCRU_GATE_CON62	0x0048	W	0x00000000	Internal clock gate and division register 62
SCRU_SOFTRST_CON60	0x0080	W	0x00000000	Internal clock reset register 60
SCRU_SOFTRST_CON62	0x0088	W	0x00000000	Internal clock reset register 62

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.5.2 Detail Registers Description

SCRU_CLKSEL_CON104

Address: Operational Base(0xFF9A8000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x1	clk_pka_crypto_sel clk_pka_crypto clock mux. 2'b00: clk_gpll_mux_gate 2'b01: clk_v0pll_mux_gate 2'b10: clk_v1pll_mux_gate
11:7	RW	0x03	clk_pka_crypto_div Divide clk_pka_crypto by (div_con + 1).
6:5	RW	0x0	clk_core_crypto_sel clk_core_crypto clock mux. 2'b00: clk_gpll_div 2'b01: clk_v0pll_div 2'b10: clk_v1pll_div
4:0	RW	0x00	clk_core_crypto_div Divide clk_core_crypto by (div_con + 1).

SCRU_CLKSEL_CON105

Address: Operational Base(0xFF9A8000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable

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Bit	Attr	Reset Value	Description
			1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	clk_timer1_ch4_sel clk_timer1_ch4 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: mclk_asrc0
11:9	RW	0x0	clk_timer1_ch3_sel clk_timer1_ch3 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: sai3_mclk_io_in 3'b101: sai3_sclk_io_in
8:6	RW	0x0	clk_timer1_ch2_sel clk_timer1_ch2 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: sai2_mclk_io_in 3'b101: sai2_sclk_io_in
5:3	RW	0x0	clk_timer1_ch1_sel clk_timer1_ch1 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: sai1_mclk_io_in 3'b101: sai1_sclk_io_in
2:0	RW	0x0	clk_timer1_ch0_sel clk_timer1_ch0 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: sai0_mclk_io_in 3'b101: sai0_sclk_io_in

SCRU_CLKSEL_CON106

Address: Operational Base(0xFF9A8000) + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2:0	RW	0x0	clk_timer1_ch5_sel clk_timer1_ch5 clock mux. 3'b000: xin_osc0_func 3'b001: clk_gpll_div_100m 3'b010: clk_deepslow 3'b011: clk_core_pvtpll_logic 3'b100: mclk_asrc1

SCRU_GATE_CON60

Address: Operational Base(0xFF9A8000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	pclk_keyreader_en pclk_keyreader clock gating control. When high, disable clock
4	RO	0x0	reserved
3	RW	0x0	pclk_otp_mask_en pclk_otp_mask clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	clk_sbpi_otpc_s_en clk_sbpi_otpc_s clock gating control. When high, disable clock
0	RW	0x0	pclk_otpc_s_en pclk_otpc_s clock gating control. When high, disable clock

SCRU_GATE_CON62

Address: Operational Base(0xFF9A8000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	clk_timer1_ch5_en clk_timer1_ch5 clock gating control. When high, disable clock
14	RW	0x0	clk_timer1_ch4_en clk_timer1_ch4 clock gating control. When high, disable clock
13	RW	0x0	clk_timer1_ch3_en clk_timer1_ch3 clock gating control. When high, disable clock
12	RW	0x0	clk_timer1_ch2_en clk_timer1_ch2 clock gating control. When high, disable clock
11	RW	0x0	clk_timer1_ch1_en clk_timer1_ch1 clock gating control. When high, disable clock
10	RW	0x0	clk_timer1_ch0_en clk_timer1_ch0 clock gating control. When high, disable clock
9	RW	0x0	pclk_timer1_en pclk_stimer clock gating control. When high, disable clock
8	RW	0x0	pclk_bus_sgrf_en pclk_bus_sgrf clock gating control. When high, disable clock
7	RW	0x0	hclk_rng_s_en hclk_rng_s clock gating control. When high, disable clock
6	RW	0x0	aclk_crypto_s_en aclk_crypto_s clock gating control. When high, disable clock
5	RW	0x0	clk_pka_crypto_s_en clk_pka_crypto_s clock gating control. When high, disable clock
4	RW	0x0	clk_core_crypto_s_en clk_core_crypto_s clock gating control. When high, disable clock
3	RW	0x0	hclk_keylad_en hclk_keylad clock gating control. When high, disable clock
2	RW	0x0	hclk_crypto_s_en hclk_crypto_s clock gating control. When high, disable clock
1	RW	0x0	pclk_ddr_service_en pclk_ddr_service clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
0	RW	0x0	hclk_bootrom_en hclk_bootrom clock gating control. When high, disable clock

SCRU_SOFTRST_CON60

Address: Operational Base(0xFF9A8000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	presetn_otp_mask When high, reset relative logic
2	RW	0x0	resetn_user_otpc_s When high, reset relative logic
1	RW	0x0	resetn_sbpi_otpc_s When high, reset relative logic
0	RW	0x0	presetn_otpc_s When high, reset relative logic

SCRU_SOFTRST_CON62

Address: Operational Base(0xFF9A8000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_timer1_ch5 When high, reset relative logic
14	RW	0x0	resetn_timer1_ch4 When high, reset relative logic
13	RW	0x0	resetn_timer1_ch3 When high, reset relative logic
12	RW	0x0	resetn_timer1_ch2 When high, reset relative logic
11	RW	0x0	resetn_timer1_ch1 When high, reset relative logic
10	RW	0x0	resetn_timer1_ch0 When high, reset relative logic
9	RW	0x0	presetn_timer1 When high, reset relative logic
8	RO	0x0	reserved
7	RW	0x0	hresetn_rng_s When high, reset relative logic

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Bit	Attr	Reset Value	Description
6	RW	0x0	aresetn_crypto When high, reset relative logic
5	RW	0x0	resetn_pka_crypto When high, reset relative logic
4	RW	0x0	resetn_core_crypto When high, reset relative logic
3	RW	0x0	hresetn_keylad When high, reset relative logic
2	RW	0x0	hresetn_crypto_s When high, reset relative logic
1	RW	0x0	presetn_ddr_service When high, reset relative logic
0	RW	0x0	hresetn_bootrom When high, reset relative logic

2.6 CRU_PMU Register Description

2.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_PMU_GPLL_CON0	0x0000	W	0x000020C8	GPLL configuration register0
CRU_PMU_GPLL_CON1	0x0004	W	0x00001043	GPLL configuration register1
CRU_PMU_GPLL_CON2	0x0008	W	0x00000000	GPLL configuration register2
CRU_PMU_GPLL_CON3	0x000C	W	0x00000007	GPLL configuration register3
CRU_PMU_GPLL_CON4	0x0010	W	0x00007F00	GPLL configuration register4
CRU_PMU_VPLL0_CON0	0x0020	W	0x00001031	V0PLL configuration register0
CRU_PMU_VPLL0_CON1	0x0024	W	0x00000041	V0PLL configuration register1
CRU_PMU_VPLL0_CON2	0x0028	W	0x00000000	V0PLL configuration register2
CRU_PMU_VPLL0_CON3	0x002C	W	0x00000007	V0PLL configuration register3
CRU_PMU_VPLL0_CON4	0x0030	W	0x00007F00	V0PLL configuration register4
CRU_PMU_VPLL1_CON0	0x0040	W	0x0000204B	V1PLL configuration register0
CRU_PMU_VPLL1_CON1	0x0044	W	0x00000041	V1PLL configuration register1
CRU_PMU_VPLL1_CON2	0x0048	W	0x00000000	V1PLL configuration register2
CRU_PMU_VPLL1_CON3	0x004C	W	0x00000007	V1PLL configuration register3
CRU_PMU_VPLL1_CON4	0x0050	W	0x00007F00	V1PLL configuration register4
CRU_PMU_SSGTBL0_3	0x0140	W	0x00000000	External wave table register0
CRU_PMU_SSGTBL4_7	0x0144	W	0x00000000	External wave table register1
CRU_PMU_SSGTBL8_11	0x0148	W	0x00000000	External wave table register2
CRU_PMU_SSGTBL12_15	0x014C	W	0x00000000	External wave table register3
CRU_PMU_SSGTBL16_19	0x0150	W	0x00000000	External wave table register4
CRU_PMU_SSGTBL20_23	0x0154	W	0x00000000	External wave table register5
CRU_PMU_SSGTBL24_27	0x0158	W	0x00000000	External wave table register6
CRU_PMU_SSGTBL28_31	0x015C	W	0x00000000	External wave table register7
CRU_PMU_SSGTBL32_35	0x0160	W	0x00000000	External wave table register8

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Name	Offset	Size	Reset Value	Description
CRU_PMU_SSGTBL36_39	0x0164	W	0x00000000	External wave table register9
CRU_PMU_SSGTBL40_43	0x0168	W	0x00000000	External wave table register10
CRU_PMU_SSGTBL44_47	0x016C	W	0x00000000	External wave table register11
CRU_PMU_SSGTBL48_51	0x0170	W	0x00000000	External wave table register12
CRU_PMU_SSGTBL52_55	0x0174	W	0x00000000	External wave table register13
CRU_PMU_SSGTBL56_59	0x0178	W	0x00000000	External wave table register14
CRU_PMU_SSGTBL60_63	0x017C	W	0x00000000	External wave table register15
CRU_PMU_SSGTBL64_67	0x0180	W	0x00000000	External wave table register16
CRU_PMU_SSGTBL68_71	0x0184	W	0x00000000	External wave table register17
CRU_PMU_SSGTBL72_75	0x0188	W	0x00000000	External wave table register18
CRU_PMU_SSGTBL76_79	0x018C	W	0x00000000	External wave table register19
CRU_PMU_SSGTBL80_83	0x0190	W	0x00000000	External wave table register20
CRU_PMU_SSGTBL84_87	0x0194	W	0x00000000	External wave table register21
CRU_PMU_SSGTBL88_91	0x0198	W	0x00000000	External wave table register22
CRU_PMU_SSGTBL92_95	0x019C	W	0x00000000	External wave table register23
CRU_PMU_SSGTBL96_99	0x01A0	W	0x00000000	External wave table register24
CRU_PMU_SSGTBL100_103	0x01A4	W	0x00000000	External wave table register25
CRU_PMU_SSGTBL104_107	0x01A8	W	0x00000000	External wave table register26
CRU_PMU_SSGTBL108_111	0x01AC	W	0x00000000	External wave table register27
CRU_PMU_SSGTBL112_115	0x01B0	W	0x00000000	External wave table register28
CRU_PMU_SSGTBL116_119	0x01B4	W	0x00000000	External wave table register29
CRU_PMU_SSGTBL120_123	0x01B8	W	0x00000000	External wave table register30
CRU_PMU_SSGTBL124_127	0x01BC	W	0x00000000	External wave table register31
CRU_PMU_CLKSEL_CON00	0x0300	W	0x00007C00	Internal clock select and division register 0
CRU_PMU_CLKSEL_CON01	0x0304	W	0x00000101	Internal clock select and division register 1
CRU_PMU_CLKSEL_CON02	0x0308	W	0x0040B71B	Internal clock select and division register 2
CRU_PMU_CLKSEL_CON03	0x030C	W	0x000002B0	Internal clock select and division register 3
CRU_PMU_CLKSEL_CON04	0x0310	W	0x00000C80	Internal clock select and division register 4
CRU_PMU_CLKSEL_CON06	0x0318	W	0x00000000	Internal clock select and division register 6

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Name	Offset	Size	Reset Value	Description
CRU_PMU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
CRU_PMU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
CRU_PMU_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2
CRU_PMU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
CRU_PMU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.6.2 Detail Registers Description

CRU_PMU_GPLL_CON0

Address: Operational Base(0xFF9B0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x2	postdiv1 First Post Divide Value, (1-7) Should obey the rule: postdiv1 > = postdiv2
11:0	RW	0x0c8	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_PMU_GPLL_CON1

Address: Operational Base(0xFF9B0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	pllpd PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x03	refdiv Reference Clock Divide Value, (1-63)

CRU_PMU_GPLL_CON2

Address: Operational Base(0xFF9B0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_PMU_GPLL_CON3

Address: Operational Base(0xFF9B0000) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread Set modulation depth (spread percentage) of SSMOD 5'h0: 0% 5'h1: 0.1% 5'h2: 0.2% ... 5'h1e: 3% 5'h1f: 3.1%
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs spread 1'b0: Center spread 1'b1: Down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

CRU_PMU_GPLL_CON4

Address: Operational Base(0xFF9B0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs, (0-255)
7:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	ssmod_sel_ext_wave Select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_PMU_VPLL0_CON0

Address: Operational Base(0xFF9B0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7) Should obey the rule: postdiv1 > = postdiv2
11:0	RW	0x031	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_PMU_VPLL0_CON1

Address: Operational Base(0xFF9B0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	pllpd PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x0	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

CRU_PMU_VPLL0_CON2

Address: Operational Base(0xFF9B0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_PMU_VPLL0_CON3

Address: Operational Base(0xFF9B0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread Set modulation depth (spread percentage) of SSMOD 5'h0: 0%

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Bit	Attr	Reset Value	Description
			5'h1: 0.1% 5'h2: 0.2% ... 5'h1e: 3% 5'h1f: 3.1%
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs spread 1'b0: Center spread 1'b1: Down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

CRU_PMU_VPLL0_CON4

Address: Operational Base(0xFF9B0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs, (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave Select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_PMU_VPLL1_CON0

Address: Operational Base(0xFF9B0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable

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Bit	Attr	Reset Value	Description
			1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x2	postdiv1 First Post Divide Value, (1-7) Should obey the rule: postdiv1 > = postdiv2
11:0	RW	0x04b	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_PMU_VPLL1_CON1

Address: Operational Base(0xFF9B0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	pllpd PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x0	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

CRU_PMU_VPLL1_CON2

Address: Operational Base(0xFF9B0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_PMU_VPLL1_CON3

Address: Operational Base(0xFF9B0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread Set modulation depth (spread percentage) of SSMOD 5'h0: 0% 5'h1: 0.1% 5'h2: 0.2% ... 5'h1e: 3% 5'h1f: 3.1%
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs spread 1'b0: Center spread 1'b1: Down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset

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Bit	Attr	Reset Value	Description
			1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

CRU_PMU_VPLL1_CON4

Address: Operational Base(0xFF9B0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs, (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave Select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_PMU_SSGTBL0_3

Address: Operational Base(0xFF9B0000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl0_3 Extern wave table 0-3 7-0: table0 15-8: table1 23-16: table2 31-24: table3

CRU_PMU_SSGTBL4_7

Address: Operational Base(0xFF9B0000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl4_7 Extern wave table 4-7 7-0: table4 15-8: table5 23-16: table6 31-24: table7

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CRU_PMU_SSGTBL8_11

Address: Operational Base(0xFF9B0000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl8_11 Extern wave table 8-11 7-0: table8 15-8: table9 23-16: table10 31-24: table11

CRU_PMU_SSGTBL12_15

Address: Operational Base(0xFF9B0000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl12_15 Extern wave table 12-15 7-0: table12 15-8: table13 23-16: table14 31-24: table15

CRU_PMU_SSGTBL16_19

Address: Operational Base(0xFF9B0000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl16_19 Extern wave table 16-19 7-0: table16 15-8: table17 23-16: table18 31-24: table19

CRU_PMU_SSGTBL20_23

Address: Operational Base(0xFF9B0000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl20_23 Extern wave table 20-23 7-0: table20 15-8: table21 23-16: table22 31-24: table23

CRU_PMU_SSGTBL24_27

Address: Operational Base(0xFF9B0000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl24_27 Extern wave table 24-27 7-0: table24

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Bit	Attr	Reset Value	Description
			15-8: table25 23-16: table26 31-24: table27

CRU_PMU_SSGTBL28_31

Address: Operational Base(0xFF9B0000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl28_31 Extern wave table 28-31 7-0: table28 15-8: table29 23-16: table30 31-24: table31

CRU_PMU_SSGTBL32_35

Address: Operational Base(0xFF9B0000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl32_35 Extern wave table 32-35 7-0: table32 15-8: table33 23-16: table34 31-24: table35

CRU_PMU_SSGTBL36_39

Address: Operational Base(0xFF9B0000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl36_39 Extern wave table 36-39 7-0: table36 15-8: table37 23-16: table38 31-24: table39

CRU_PMU_SSGTBL40_43

Address: Operational Base(0xFF9B0000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl40_43 Extern wave table 40-43 7-0: table40 15-8: table41 23-16: table42 31-24: table43

CRU_PMU_SSGTBL44_47

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Address: Operational Base(0xFF9B0000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl44_47 Extern wave table 44-47 7-0: table44 15-8: table45 23-16: table46 31-24: table47

CRU_PMU_SSGTBL48_51

Address: Operational Base(0xFF9B0000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl48_51 Extern wave table 48-51 7-0: table48 15-8: table49 23-16: table50 31-24: table51

CRU_PMU_SSGTBL52_55

Address: Operational Base(0xFF9B0000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl52_55 Extern wave table 52-55 7-0: table52 15-8: table53 23-16: table54 31-24: table55

CRU_PMU_SSGTBL56_59

Address: Operational Base(0xFF9B0000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl56_59 Extern wave table 56-59 7-0: table56 15-8: table57 23-16: table58 31-24: table59

CRU_PMU_SSGTBL60_63

Address: Operational Base(0xFF9B0000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl60_63 Extern wave table 60-63 7-0: table60 15-8: table61

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Bit	Attr	Reset Value	Description
			23-16: table62 31-24: table63

CRU_PMU_SSGTBL64_67

Address: Operational Base(0xFF9B0000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl64_67 Extern wave table 64-67 7-0: table64 15-8: table65 23-16: table66 31-24: table67

CRU_PMU_SSGTBL68_71

Address: Operational Base(0xFF9B0000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl68_71 Extern wave table 68-71 7-0: table68 15-8: table69 23-16: table70 31-24: table71

CRU_PMU_SSGTBL72_75

Address: Operational Base(0xFF9B0000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl72_75 Extern wave table 72-75 7-0: table72 15-8: table73 23-16: table74 31-24: table75

CRU_PMU_SSGTBL76_79

Address: Operational Base(0xFF9B0000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl76_79 Extern wave table 76-79 7-0: table76 15-8: table77 23-16: table78 31-24: table79

CRU_PMU_SSGTBL80_83

Address: Operational Base(0xFF9B0000) + offset (0x0190)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl80_83 Extern wave table 76-79 7-0: table80 15-8: table81 23-16: table82 31-24: table83

CRU_PMU_SSGTBL84_87

Address: Operational Base(0xFF9B0000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl84_87 Extern wave table 84-87 7-0: table84 15-8: table85 23-16: table86 31-24: table87

CRU_PMU_SSGTBL88_91

Address: Operational Base(0xFF9B0000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl88_91 Extern wave table 88-91 7-0: table88 15-8: table89 23-16: table90 31-24: table91

CRU_PMU_SSGTBL92_95

Address: Operational Base(0xFF9B0000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl92_95 Extern wave table 92-95 7-0: table92 15-8: table93 23-16: table94 31-24: table95

CRU_PMU_SSGTBL96_99

Address: Operational Base(0xFF9B0000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl96_99 Extern wave table 96-99 7-0: table96 15-8: table97 23-16: table98

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Bit	Attr	Reset Value	Description
			31-24: table99

CRU_PMU_SSGTBL100_103

Address: Operational Base(0xFF9B0000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl100_103 Extern wave table 100-103 7-0: table100 15-8: table101 23-16: table102 31-24: table103

CRU_PMU_SSGTBL104_107

Address: Operational Base(0xFF9B0000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl104_107 Extern wave table 104-107 7-0: table104 15-8: table105 23-16: table106 31-24: table107

CRU_PMU_SSGTBL108_111

Address: Operational Base(0xFF9B0000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl108_111 Extern wave table 108-111 7-0: table108 15-8: table109 23-16: table110 31-24: table111

CRU_PMU_SSGTBL112_115

Address: Operational Base(0xFF9B0000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl112_115 Extern wave table 112-115 7-0: table112 15-8: table113 23-16: table114 31-24: table115

CRU_PMU_SSGTBL116_119

Address: Operational Base(0xFF9B0000) + offset (0x01B4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl116_119 Extern wave table 116-119 7-0: table116 15-8: table117 23-16: table118 31-24: table119

CRU_PMU_SSGTBL120_123

Address: Operational Base(0xFF9B0000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl120_123 Extern wave table 120-123 7-0: table120 15-8: table121 23-16: table122 31-24: table123

CRU_PMU_SSGTBL124_127

Address: Operational Base(0xFF9B0000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl124_127 Extern wave table 124-127 7-0: table124 15-8: table125 23-16: table126 31-24: table127

CRU_PMU_CLKSEL_CON00

Address: Operational Base(0xFF9B0000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RW	0x1f	clk_mac_out_div DT50 division register. Divide clk_mac_out by (div_con + 1).
9:6	RW	0x0	clk_pwm0_div Divide clk_pwm0 by (div_con + 1).
5:4	RW	0x0	clk_pmu_hp_timer_sel clk_pmu_hp_timer clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_div_100m 2'b10: clk_core_pvtpll_logic

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	dbclk_gpio1_shadow_sel dbclk_gpio1_shadow clock mux. 2'b00: xin_osc0_func 2'b01: clk_rc 2'b10: clk_deepslow_pmu
1:0	RW	0x0	dbclk_gpio0_sel dbclk_pmu_gpio clock mux. 2'b00: xin_osc0_func 2'b01: clk_rc 2'b10: clk_deepslow_pmu

CRU_PMU_CLKSEL_CON01

Address: Operational Base(0xFF9B0000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_ref_out1_sel clk_ref_out1 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll 2'b10: clk_v0pll 2'b11: clk_v1pll
13:8	RW	0x01	clk_ref_out1_div DT50 division register. Divide clk_ref_out1 by (div_con + 1).
7:6	RW	0x0	clk_ref_out0_sel clk_ref_out0 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll 2'b10: clk_v0pll 2'b11: clk_v1pll
5:0	RW	0x01	clk_ref_out0_div DT50 division register. Divide clk_ref_out0 by (div_con + 1).

CRU_PMU_CLKSEL_CON02

Address: Operational Base(0xFF9B0000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RW	0x0040b71b	clk_deepslow_frac_div clk_deepslow_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

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CRU_PMU_CLKSEL_CON03

Address: Operational Base(0xFF9B0000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:9	RW	0x1	clk_deepslow_pmu_sel clk_deepslow_pmu clock mux. 2'b00: clk_rtc_deepslow_io 2'b01: clk_deepslow_rc 2'b10: clk_deepslow_frac
8:7	RW	0x1	clk_deepslow_sel clk_deepslow clock mux. 2'b00: clk_rtc_deepslow_io 2'b01: clk_deepslow_rc 2'b10: clk_deepslow_frac
6:2	RW	0x0c	clk_deepslow_rc_div Divide clk_deepslow_rc by (div_con + 1).
1:0	RW	0x0	clk_deepslow_frac_sel clk_deepslow_frac clock mux. 2'b00: xin_osc0_func 2'b01: clk_v0pll 2'b10: clk_v1pll 2'b11: clk_rc

CRU_PMU_CLKSEL_CON04

Address: Operational Base(0xFF9B0000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_ref_phy_pmu_mux_sel clk_ref_usbphy_pmu_mux clock mux. 1'b0: xin_osc0_func_phy 1'b1: clk_ref_phy_pll
14:13	RW	0x0	clk_ref_phy_pll_sel clk_ref_phy_pll clock mux. 2'b00: clk_gpll 2'b01: clk_v0pll 2'b10: clk_v1pll
12:6	RW	0x32	clk_ref_phy_pll_div clk_ref_phy_pll interge division register.

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	clk_ddrphy_sel clk_ddrphy clock mux. 2'b00: clk_gpll 2'b01: clk_v0pll 2'b10: clk_v1pll
3:0	RW	0x0	clk_ddrphy_div DT50 division register. Divide clk_ddrphy by (div_con + 1).

CRU_PMU_CLKSEL_CON06

Address: Operational Base(0xFF9B0000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	clk_v1pll_ref_sel clk_v1pll_ref clock mux. 1'b0: xin_osc0_func 1'b1: clk_pll_ref_io
0	RW	0x0	clk_v0pll_ref_sel clk_v0pll_ref clock mux. 1'b0: xin_osc0_func 1'b1: clk_pll_ref_io

CRU_PMU_GATE_CON00

Address: Operational Base(0xFF9B0000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_pwm0_en pclk_pwm0 clock gating control. When high, disable clock
14	RW	0x0	clk_pmu_hp_timer_deepslow_en clk_pmu_hp_timer_deepslow clock gating control. When high, disable clock
13	RW	0x0	clk_pmu_hp_timer_en clk_pmu_hp_timer_ls clock gating control. When high, disable clock
12	RW	0x0	pclk_pmu_hp_timer_en pclk_pmu_hp_timer clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
11	RW	0x0	dbclk_gpio1_shadow_en dbclk_gpio1_shadow clock gating control. When high, disable clock
10	RW	0x0	pclk_gpio1_shadow_en pclk_gpio1_shadow clock gating control. When high, disable clock
9	RW	0x0	dbclk_gpio0_en dbclk_gpio0 clock gating control. When high, disable clock
8	RW	0x0	pclk_gpio0_en pclk_gpio0 clock gating control. When high, disable clock
7	RW	0x0	pclk_gpio0_ioc_en pclk_pmu_ioc clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	pclk_pmu_grf_en pclk_pmu_grf clock gating control. When high, disable clock
4	RW	0x0	pclk_pmu_cru_en pclk_pmu_cru clock gating control. When high, disable clock
3	RW	0x0	clk_pmu_deepslow_en clk_pmu_deepslow clock gating control. When high, disable clock
2	RW	0x0	pclk_pmu_en pclk_pmu clock gating control. When high, disable clock
1	RW	0x0	clk_pmu_en clk_pmu clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_PMU_GATE_CON01

Address: Operational Base(0xFF9B0000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_ref_phy_pll_en clk_ref_phy_pll clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
13	RW	0x0	clk_touch_key_en clk_touch_key clock gating control. When high, disable clock
12	RW	0x0	pclk_touch_key_en pclk_touch_key clock gating control. When high, disable clock
11	RW	0x0	clk_ddrphy_en clk_ddrphy clock gating control. When high, disable clock
10	RW	0x0	clk_uart_jtag_en clk_uart_jtag clock gating control. When high, disable clock
9	RW	0x0	clk_deepslow_pmu_en clk_deepslow_pmu clock gating control. When high, disable clock
8	RW	0x0	clk_deepslow_en clk_deepslow clock gating control. When high, disable clock
7	RW	0x0	clk_deepslow_rc_en clk_deepslow_rc clock gating control. When high, disable clock
6	RW	0x0	clk_deepslow_frac_div_en clk_deepslow_frac clock gating control. When high, disable clock
5	RW	0x0	clk_ref_out1_en clk_ref_out1 clock gating control. When high, disable clock
4	RW	0x0	clk_ref_out0_en clk_ref_out0 clock gating control. When high, disable clock
3	RW	0x0	clk_mac_out_en clk_mac_out clock gating control. When high, disable clock
2	RW	0x0	clk_rc_pwm0_en clk_rc_pwm0 clock gating control. When high, disable clock
1	RW	0x0	clk_osc_pwm0_en clk_osc_pwm0 clock gating control. When high, disable clock
0	RW	0x0	clk_pwm0_en clk_pwm0 clock gating control. When high, disable clock

CRU_PMU_GATE_CON02

Address: Operational Base(0xFF9B0000) + offset (0x0808)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	osc_clk_out_en osc_clk_out clock gating control. When high, disable clock

CRU_PMU_SOFTRST_CON00

Address: Operational Base(0xFF9B0000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_pwm0 When high, reset relative logic
14	RW	0x0	resetn_pmu_hp_timer_deepslow When high, reset relative logic
13	RW	0x0	resetn_pmu_hp_timer When high, reset relative logic
12	RW	0x0	presetn_pmu_hp_timer When high, reset relative logic
11	RW	0x0	dbresetn_gpio1_shadow When high, reset relative logic
10	RW	0x0	presetn_gpio1_shadow When high, reset relative logic
9	RW	0x0	dbresetn_gpio0 When high, reset relative logic
8	RW	0x0	presetn_gpio0 When high, reset relative logic
7	RW	0x0	presetn_gpio0_ioc When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	presetn_pmu_grf When high, reset relative logic
4:0	RO	0x00	reserved

CRU_PMU_SOFTRST_CON01

Address: Operational Base(0xFF9B0000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable

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Bit	Attr	Reset Value	Description
			1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_touch_key When high, reset relative logic
12	RW	0x0	presetn_touch_key When high, reset relative logic
11	RW	0x0	resetn_ddrphy When high, reset relative logic
10:1	RO	0x000	reserved
0	RW	0x0	resetn_pwm0 When high, reset relative logic

2.7 SCRU PMU Register Description

2.7.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.7.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SCRU_PMU_GATE_CON60	0x0040	W	0x00000000	Internal clock gate and division register 60

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.7.3 Detail Registers Description

SCRU_PMU_GATE_CON60

Address: Operational Base(0xFF9B8000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	pclk_pmu_sgrf_en pclk_pmu_sgrf clock gating control. When high, disable clock

2.8 Application Notes

2.8.1 PLL Usage

2.8.1.1 PLL Frequency Configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_xPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_xPLL_CON1.
FRAC can be configured by programming CRU_xPLL_CON2(x= D, G).

- If DSMPD = 1 (DSM is disabled, "integer mode")

FOUTVCO = (FREF/ REFDIV)* FBDIV
FOUTPOSTDIV = FOUTVCO/ (POSTDIV1* POSTDIV2)

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When FREF is 24MHz, and if 800MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 1
REFDIV = 6
FBDIV = 200
POSTDIV1=1
POSTDIV2=1

And then

FOUTVCO = (FREF / REFDIV) * FBDIV = 24/6*200=800
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=800/1/1=800

- If DSMPD = 0 (DSM is enabled, "fractional mode")

FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24))
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)

When FREF is 24MHz, and if 491.52MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 0
REFDIV = 1
FBDIV = 40
FRAC = 24'hf5c28f
POSTDIV1=2
POSTDIV2=1

And then

FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24)) = 983.04
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=983.04/(2*1)=491.52

- POSTDIV1=0, POSTDIV2=0 are unused. We should make sure that POSTDIV1>=POSTDIV2.

2.8.1.2 PLL Setting Consideration

- For lowest power operation, the minimum VCO and FREF frequencies should be used. For minimum jitter operation, the highest VCO and FREF frequencies should be used.
- The supply rejection will be worse at the low end of the VCO range so care should be taken to keep the supply clean for low power applications.
- The PD input places the PLL into the lowest power mode. In this case, all analog circuits are turned off and FREF will be "ignored". The FOUTPOSTDIV and FOUTVCO pins are forced to logic low (0V).
- The BYPASS pin controls FREF to be passed to the FOUTPOSTDIV when active high.

2.8.1.3 PLL Frequency Change And Lock Check

For normal applications, user should configure as following steps to change the PLL output frequency.

- Change PLL from normal to slow mode by programming CRU_MODE_CON00.
- Power down PLL
- Change PLL setting.
- Power up PLL after delay 1us
- Wait until PLL is lock state by checking CRU_xPLL_CON1[10] register (The max lock time is 500*REFDIV/FREF) or just delay about 500 REF_CLK cycles
- Change PLL into normal mode

For special applications, user can use on-the-fly mode. User can change FBDIV and FRAC slightly and don't need to follow above normal changing setups, PLL will simply slew to the new frequency.

2.8.2 Divider Usage

CRU supports multi-dividers for different clock requirement.

- Divider free divider
- Fractional divider
- DivfreeDT50 divider (DT50)

2.8.2.1 DivFree Divider Usage

Using this divider, freq_out =freq_src/(n+1).

2.8.2.2 Fractional Divider Usage

To get specific frequency, matrix array clocks of clk_frac_uart_matrix0/1, clk_frac_voice_matrix0/1, clk_frac_common_matrix0/1/2 can be generated by fractional

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divider. Generally you should ensure that denominator is 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock.

2.8.2.3 DivfreeDT50 Divider Usage

Some modules like SDMMC, FLEXBUS, MAC, PDM and FSPI need clock of 50% duty cycle, divfreeDT50 can generate clock of 50% duty cycle even when divisor value is odd.

2.8.3 Global Software Reset

Two global software resets are designed in the chip. These two software resets are self-de-asserted by hardware. Hold time of global software reset (glb_srstn_1, glb_srstn_2, wdt_rstn, tsadc_rstn) can be programed up to 11.18s.

- CRU_GLB_SRST_FST_VALUE[15:0] = 0xfdb9 to assert the first global software reset glb_srstn_1
- CRU_GLB_SRST_SND_VALUE[15:0] = 0xeca8 to assert the second global software reset glb_srstn_2
- glb_srstn_1 resets almost all logic except some registers just supporting hardware reset
- glb_srstn_2 resets almost all logic except GPIOs, IOCs, SPINLOCK and KEYREADER.

Reset for IP in PD_PMU can be hold if its reset_hold_enable in GRF_PMU_SOC_CON3 is high even if glb_srstn_1 or glb_srstn_2 active.

2.8.4 SSCG Usage

There are some scenes where SSCG should be enabled. One scene is in communication where a fixed frequency is required. Another scene is that the system requires a clock with low long-term jitter. When SSCG is used, the PLL should be configured to fractional mode first for spread spectrum capability.

2.8.4.1 SSCG Use InternalPoint Table

User can use SSCG with internal point table as following steps:

- Setting ssmod_spread (CRU_XPLL_CON3[12:8]) and ssmod_downspread (CRU_XPLL_CON3[3])

The modulation amplitude is controlled by the value of ssmod_spread. A ssmod_spread value of 5'd0 turns off the modulation. A ssmod_spread value of 5'd31 (5'b11111) gives maximum modulation while a value of 5'd1 gives minimum modulation.

The modulation amplitude can be calculated from the value of modulation by:

Modulation Amplitude = ±5'd(ssmod_spread)*0.1%

The modulation direction is determined by the ssmod_downspread bit.

- ssmod_downspread = 1'b1, down spread mode is used. If ssmod_spread = 5'd29, the maximum PLL frequency is the nominally programmed value F_{NOM}, and the minimum value is given by F_{NOM}* (1–0.029).
- ssmod_downspread = 1'b0, center spread mode is used. If ssmod_spread = 5'd29, the maximum PLL frequency would be determined by F_{NOM}* (1+0.029) and the minimum frequency by F_{NOM} * (1–0.029).

Setting the style of modulation (center versus down) and the modulation amplitude depend on the amount of EMI reduction desired and the timing margin for circuits running on the spread clock domain. The larger the spread value, the greater the reduction in EMI amplitude. However, the larger the spread value, the more timing margin needed for correct circuit operation.

- Setting ssmod_sel_ext_wave (CRU_XPLL_CON4[0])=1'b0

When use internal point table, the frequency will change as following during 128 point:

- Change from minimum value to maximum value uniformly within 64 points
- Change from maximum value to minimum value uniformly within 64 points

Spread spectrum modulator is implemented by repeating as above.

- Setting ssmod_divval (CRU_XPLL_CON3[7:4])

The frequency of modulation FMOD= FREF / (Point number*REFDIV * ssmod_divval). The FMOD is typically set above 32KHz and below the maximum frequency for modulation fidelity, which isdetermined by the PLL bandwidth. The maximum modulation frequency is conservatively set at FREF / (200*REFDIV).

When FREF=24MHz and REFDIV= 1, the value of ssmod_divval can be 5, then the FMOD is 37.5KHz.

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- Setting ssmod_bp (CRU_XPLL_CON3[0])=1'b0
- Setting ssmod_disable_sscg (CRU_XPLL_CON3[1])=1'b0
- Setting ssmod_reset (CRU_XPLL_CON3[2])=1'b0

2.8.4.2 SSCG Use External Point Table

In addition to the internal shape table, an external shape table can be used.
This enables customization tables in both shape and the number of sample points for theenvelope wave formup to 128 data points. The external table of 128 data points can be configured from CRU_PMU_SSGTBL0_3 ~ CRU_PMU_SSGTBL124_127.
User can use SSMOD with external point table as following steps:

- Setting ssmod_spread (CRU_XPLL_CON3[12:8]) andssmod_downspread (CRU_XPLL_CON3[3]), same with internal point table usage.
- Setting ssmod_sel_ext_wave (CRU_XPLL_CON4[0])=1'b1
- Setting ssmod_ext_maxaddr (CRU_XPLL_CON4[15:8]) and table0 ~ table127 (CRU_PMU_SSGTBL0_3 ~ CRU_PMU_SSGTBL124_127)

ssmod_ext_maxaddr is the maximum table address. For example, if the number of points describing the envelope shape is 128, the ssmod_ext_maxaddr should be configured to 127. The table address circulate over the range 0 to 127.
The table0 ~ table127 must be 8 bit numbers in the form of sign and magnitude.

  - 1.00 is represented by 8'b01111111, it is corresponded to maximum frequency.
  - -1.00 is represented in the table by 8'b11111111, it is corresponded to minimum frequency.
  - 0.5 is represented in the table by 8'b00111111.
  - -0.5 is represented in the table by 8'b10111111.

The frequency will change base table0~table127 within 128 points, and then repeat.

- Setting ssmod_divval (CRU_XPLL_CON3[7:4])

The frequency of modulation FMOD= FREF/(Point number*REFDIV*ssmod_divval). The point number equals to ssmod_ext_maxaddr+1.

- Setting ssmod_bp (CRU_XPLL_CON3[0])=1'b0
- Setting ssmod_disable_sscg (CRU_XPLL_CON3[1])=1'b0
- Setting ssmod_reset (CRU_XPLL_CON3[2])=1'b0

2.8.5 Others

Based on special requirements, the frequency of aclk_bus_root must be greater than or equal to twice the frequency of pclk_bus_root.

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Chapter 3 Cortex-A7

3.1 Overview

The Cortex-A7 subsystem of the device is based on the ARMv7-A architecture. The Cortex-A7 has three Cortex-A7 central processing unit (CPU). Each processor has 16KB of Level 1 (L1) instruction cache, 16KB of L1 data cache, NEON and FPU. The Cortex-A7 also includes 128KB of Level 2 (L2) cache, Snoop Control Unit(SCU), Generic Interrupt Controller (GIC), and standard CoreSight components to support SMP debug and emulation.
The key features of the Cortex-A7 include:

- ARM Cortex-A7
  - Full implements the ARMv7-A architecture profile that includes the Advanced SIMD and VFP Extensions
  - 3 Cortex-A7 processor cores
  - 16KB L1 I-Cache and 16KB L1 D-Cache per CPU
  - In-order pipeline with direct and indirect branch prediction
  - Harvard L1 memory system with a Memory Management Unit (MMU)
  - SCU ensures memory coherency
  - Interrupt controller with 128 hardware interrupt inputs
- 128KB L2 cache
  - Fixed line length of 64 bytes
  - Physically indexed and tagged cache
  - 8-way set-associative cache structure
  - Pseudo-random cache replacement policy

3.2 Block Diagram

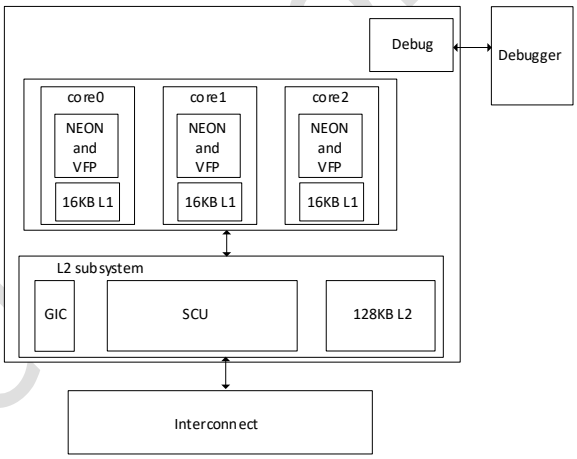

Fig. 3-1 Core Subsystem Architecture

3.3 Function Description

Please refer to the document *Cortex-A7 MPCore Technical Reference Manual* for the CPU detail description.

3.4 Register Description

Please refer to the document *Cortex-A7 MPCore Technical Reference Manual* for the CPU detail description.

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Chapter 4 Cortex-M0

4.1 Overview

The Cortex-M0 processor is a very low gate count, highly energy efficient processor that is intended for micro-controller and deeply embedded applications that require an area optimized processor.

4.1.1 Cortex-M0

The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements. The processor features and benefits are:

- A low gate count processor that features
  - The ARMv6-M Thumb instruction set
  - Thumb-2 technology
  - Load/store-multiples and multi cycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-Maskable Interrupt (NMI) input
  - Optional Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support
- Optional debug support
  - Two hardware breakpoints
  - One watch points
  - Support Serial Wire debug connection
  - single 32-bit AMBA-3 AHB-Lite system interface
- Integrated Interrupt Controller for APB bus, up to 128 IRQ lines with 128to4 INTMUX

4.2 Block Diagram

Cortex-M0 Integration architecture is shown below.

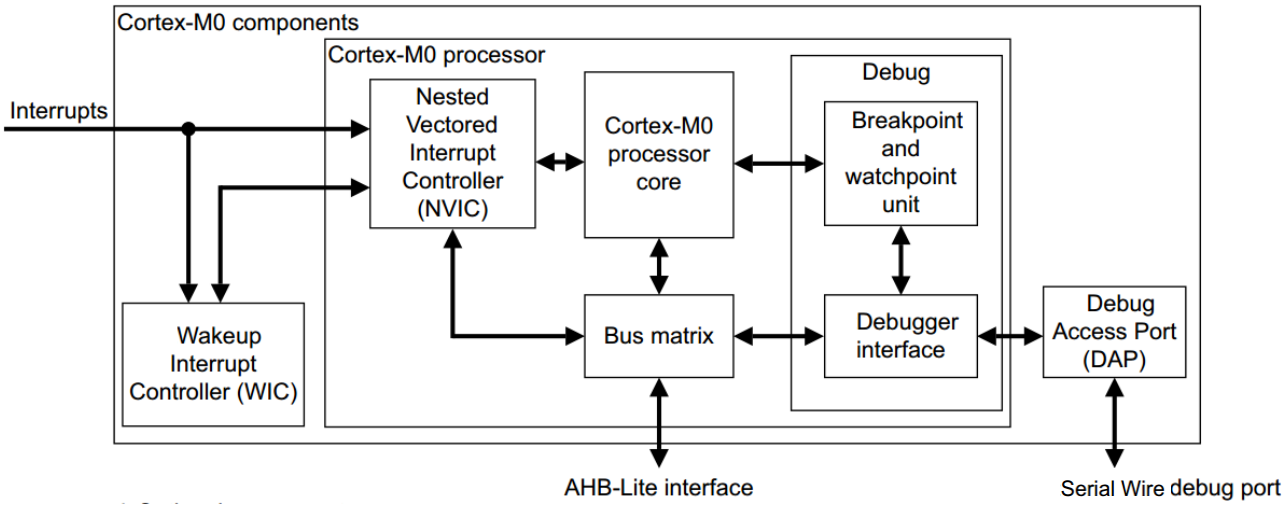

Fig. 4-1 Cortex-M0 Integration Architecture

4.3 Function Description

Please refer to the document Cortex-M0_TechnicalReferenceManualRevC_DDI0432_r0p0-02rel0.pdf and DUI0497A_cortex_m0_r0p0_generic_ug.pdf for the detail description.

4.3.1 Interrupt Multiplexer(INTMUX)

The Interrupt Multiplexer will select 4 interrupts from 125 interrupts using round robin algorithm. You need to configure corresponding enable bit for each interrupt. Also you could read the flag register to obtain the interrupt in service.

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4.4 Register Description

Please refer to the document Cortex-M0_TechnicalReferenceManualRevC_DDI0432_r0p0-02rel0.pdf and DUI0497A_cortex_m0_r0p0_generic_ug.pdf for the detail description.

4.4.1 INTMUX Registers Summary

Operational Base

Name	Base Address
M0 INTMUX base address	0xFF2A0000

Name	Offset	Size	Reset Value	Description
INTMUX_IRQ_MASK0	0x0000	W	0x00000000	IRQ interrupt source mask0 register.
INTMUX_IRQ_MASK1	0x0004	W	0x00000000	IRQ interrupt source mask1 register.
INTMUX_IRQ_MASK2	0x0008	W	0x00000000	IRQ interrupt source mask2 register.
INTMUX_IRQ_MASK3	0x000C	W	0x00000000	IRQ interrupt source mask3 register.
INTMUX_IRQ_FLAG0	0x0080	W	0x00000000	IRQ flag0 register.
INTMUX_IRQ_FLAG1	0x0084	W	0x00000000	IRQ flag1 register.
INTMUX_IRQ_FLAG2	0x0088	W	0x00000000	IRQ flag2 register.
INTMUX_IRQ_FLAG3	0x008C	W	0x00000000	IRQ flag3 register.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4.4.2 Detail Registers Description

INTMUX_IRQ_MASK0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mask0 Interrupt mask bits for the IRQ0~IRQ31 (see Table 1-5) interrupt sources. Set 1 in any bit position unmasks the corresponding interrupt. By default, all bits are masked. 1'b1: unmask interrupt 1'b0: mask interrupt

INTMUX_IRQ_MASK1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mask1 Interrupt mask bits for the IRQ32~IRQ63 (see Table 1-5) interrupt sources. Set 1 in any bit position unmasks the corresponding interrupt. By default, all bits are masked. 1'b1: unmask interrupt 1'b0: mask interrupt

INTMUX_IRQ_MASK2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mask2 Interrupt mask bits for the IRQ64~IRQ95 (see Table 1-5) interrupt sources. Set 1 in any bit position unmasks the corresponding interrupt. By default, all bits are masked. 1'b1: unmask interrupt 1'b0: mask interrupt

INTMUX_IRQ_MASK3

Address: Operational Base + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	Mask3 Interrupt mask bits for the IRQ96~IRQ125 (see Table 1-5) interrupt sources. Set 1 in any bit position unmasks the corresponding interrupt. By default, all bits are masked. 1'b1: unmask interrupt 1'b0: mask interrupt

INTMUX_IRQ_FLAG0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_flag0 Interrupt status after the masking stage. These are the interrupt status signals for the IRQ0~IRQ31 (see Table 1-5) interrupt sources.

INTMUX_IRQ_FLAG1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_flag1 Interrupt status after the masking stage. These are the interrupt status signals for the IRQ32~IRQ63 (see Table 1-5) interrupt sources.

INTMUX_IRQ_FLAG2

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_flag2 Interrupt status after the masking stage. These are the interrupt status signals for the IRQ64~IRQ95 (see Table 1-5) interrupt sources.

INTMUX_IRQ_FLAG3

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	int_flag3 Interrupt status after the masking stage. These are the interrupt status signals for the IRQ96~IRQ125 (see Table 1-5) interrupt sources.

4.5 Interface Description

Table 4-1 Cortex-M0 Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
m0jtag_tck_m0	I	SDMMC_D2/JTAG_TCK_M0/GPIO3_A4_d	GPIO3A_IOMUX_SEL_1[3:0] = 4'h2 GRF_SOC_CON0[4] = 1'b1
m0jtag_tms_m0	I/O	SDMMC_D3/JTAG_TMS_M0/GPIO3_A5_d	GPIO3A_IOMUX_SEL_1[7:4] = 4'h2 GRF_SOC_CON0[4] = 1'b1
m0jtag_tck_m1	I	UART0_TX/JTAG_TCK_M1/RM_IO22/GPIO0_C6_u	GPIO0C_IOMUX_SEL_1[11:8] = 4'h2 GRF_SOC_CON0[5] = 1'b1
m0jtag_tms_m1	I/O	UART0_RX/JTAG_TMS_M1/RM_IO23/GPIO0_C7_u	GPIO0C_IOMUX_SEL_1[15:12] = 4'h2 GRF_SOC_CON0[5] = 1'b1

Notes: I=input, O=output, I/O=input/output, bidirectional

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4.6 Application Notes

4.6.1 Clock and Reset Generation

Please refer to "Chapter CRU" for more detailed information.

4.6.2 Miscellaneous Signals for M0

M0 System Configure Signals

Table 4-2 M0 System Configure Signals

Signal Name	Default	Description
grf_con_mcu_irqlatency[7:0]	0	Minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued
grf_con_mcu_nmi	0	Non-maskable interrupt
grf_con_mcu_dbgrestart	0	External restart request.
grf_con_mcu_edbgrq	0	External debug request.
grf_con_mcu_stcalib[25:0]	0	Systick timer counter
grf_con_mcu_rxev	0	A HIGH level on this input causes the architecture defined Event Register to be set in the Cortex-M0 processor. This causes a WFE instruction to complete. It also awakens the processor if it is sleeping as the result of encountering a WFE instruction when the Event Register is clear.
grf_con_mcu_dbgen	0	SerialWire Debug enable. 0: disable 1: enable
grf_con_mcu_sleepholdreqn	1	Request to extend the processor sleeping state regardless of wake-up events. If the processor acknowledges this request driving SLEEPHOLDACKn Low, this guarantees the processor remains idle even on receipt of a wake-up event

M0 System Status Signals

Table 4-3 M0 System Status Signals

Signal Name	Default	Description
grf_mcu_dbgrestarted	1	Handshake for DBGRESTART
grf_mcu_halted	0	Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state.
grf_mcu_txev	0	M0 transform a event
grf_mcu_lockup	0	Indicates that m0 is locked up
grf_mcu_hclk_gate	0	Indicates that hclk can be gated.
grf_mcu_wakeup	0	Indicates M0 wakeup
grf_mcu_sleepdeep	0	Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or HIGH level on RXEV.
grf_mcu_sleeping	0	Active only when SLEEPING is HIGH. Indicates that the SLEEPDEEP bit in the NVIC is set to 1.
grf_mcu_sleepholdack	1	Indicates M0 sleepholdack

4.6.3 Interrupt for M0

Table 4-4 M0 Interrupt

IRQ ID	IRQ Source	IRQ ID	IRQ Source
0	PMUGPIO_1	16	SARADC
1	PMUGPIO_2	17	SDMMC_EMMC
2	PMUGPIO_3	18	RKTIMER4
3	GPIO1_1	19	RKTIMER5
4	GPIO1_2	20	STIMER4
5	GPIO1_3	21	STIMER5_DSMC
6	GPIO2_3	22	MAILBOX_BB
7	GPIO3_3	23	DMAC0
8	TOUCH_POS	24	DMAC0_ABORT
9	TOUCH_NEG	25	DMAC1

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10	PWM1_6	26	DMAC1_ABORT
11	PWM1_7	27	FLEXBUS
12	UART3	28	INTMUX0
13	UART4	29	INTMUX1
14	I2C2	30	INTMUX2
15	SPI1	31	INTMUX3

Table 4-5 INTMUX Interrupt Source

IRQ ID	IRQ Source
0	PMUGPIO_0
1	GPIO1_0
2	GPIO2_0
3	GPIO2_1
4	GPIO2_2
5	GPIO3_0
6	GPIO3_1
7	GPIO3_2
8	GPIO4_0
9	GPIO4_1
10	GPIO4_2
11	GPIO4_3
12	PWM0_0
13	PWM0_1
14	PWM0_2
15	PWM0_3
16	PWM1_0
17	PWM1_1
18	PWM1_2
19	PWM1_3
20	PWM1_4
21	PWM1_5
22	UART0
23	UART1
24	UART2
25	UART5
26	I2C0
27	I2C1
28	SPI0
29	CAN0
30	CAN1
31	SPDIF_TX
32	SPDIF_RX
33	PDM
34	SAI0
35	SAI1
36	SAI2

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37	SAI3
38	SAI4
39	ASRC0
40	ASRC1
41	TSADC
42	VOP
43	MIPI_DSIHOST
44	RGA
45	OTPC_NS
46	OTPC_S
47	KEYREADER
48	OTPC_MASK
49	GMAC0_SBD
50	GMAC0_SBD_PERCH_TX
51	GMAC0_SBD_PERCH_RX
52	GMAC0_PMT
53	GMAC1_SBD
54	GMAC1_SBD_PERCH_TX
55	GMAC1_SBD_PERCH_RX
56	GMAC1_PMT
57	USB2OTG
58	OTG0_BVALID
59	OTG0_ID
60	OTG0_LINESTATE
61	OTG0_DISCONNECT
62	USB2OTG1
63	OTG1_BVALID
64	OTG1_ID
65	OTG1_LINESTATE
66	OTG1_DISCONNECT
67	SPI2APB
68	SFC
69	DDRC_AWPOISON_0
70	DDRC_AWPOISON_1
71	DDRC_ARPOISON_0
72	DDRC_ARPOISON_1
73	DDRC_DFI_ALERT_ERR
74	DDR_MONITOR
75	DDRPHY
76	RKTIMER0
77	RKTIMER1
78	RKTIMER2
79	RKTIMER3
80	STIMER0
81	STIMER1

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82	STIMER2
83	STIMER3
84	HPTIMER
85	WDT0
86	WDT1
87	MAILBOX_AP
88	CRYPTO
89	CRYPTO_KLAD
90	CRYPTO_SC
91	NSTRNG
92	STRNG
93	DSMC_SLV
94	SYSCORE_0
95	SYSCORE_1
96	SYSCORE_2
97	SYSCORE_3
98	SYSCORE_4
99	STRIMER_DSMC_MUX
100	PMU
101	RKNPOR_POWERNGOOD
102	GPIO1_SHADOW_0
103	GPIO1_1
104	GPIO1_2
105	GPIO1_3
106	OTG0_VBUSVALID
107	OTG1_VBUSVALID
108	VOP_POST_LB
109	DMA2DDR
110	MAILBOX_AP_0
111	MAILBOX_AP_1
112	MAILBOX_AP_2
113	MAILBOX_AP_3
114	MAILBOX_BB_0
115	MAILBOX_BB_1
116	MAILBOX_BB_2
117	MAILBOX_BB_3
118	GMAC0_MCGR_DMA
119	GMAC1_MCGR_DMA
120	DMAC0_MASK0
121	DMAC0_MASK1
122	DMAC0_MASK2
123	DMAC1_MASK0
124	DMAC2_MASK1
125	DMAC3_MASK2

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Chapter 5 General Register Files (GRF)

5.1 Overview

The general register file will be used to do static setting by software, which is composed of many registers for system control. The GRF is located at several addresses.

5.2 Function Description

The function of general register file is：

- Common system control
- Record the system state

5.3 GRF Register Description

5.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_SOC_CON0	0x0000	W	0x00000444	System control register 0
GRF_SOC_CON1	0x0004	W	0x00000000	System control register 1
GRF_SOC_CON2	0x0008	W	0x00000000	System control register 2
GRF_SOC_CON3	0x000C	W	0x00000000	System control register 3
GRF_SOC_CON4	0x0010	W	0x00000000	System control register 4
GRF_SOC_CON5	0x0014	W	0x00000000	System control register 5
GRF_SOC_CON6	0x0018	W	0x00000000	System control register 6
GRF_SOC_CON7	0x001C	W	0x00000000	System control register 7
GRF_SOC_CON8	0x0020	W	0x00000000	System control register 8
GRF_SOC_CON9	0x0024	W	0x00000000	System control register 9
GRF_SOC_CON10	0x0028	W	0x00000000	System control register 10
GRF_SOC_CON11	0x002C	W	0x00000000	System control register 11
GRF_SOC_CON13	0x0034	W	0x00000000	System control register 12
GRF_SOC_CON14	0x0038	W	0x00001FDF	System control register 14
GRF_SOC_CON15	0x003C	W	0x00000000	System control register 15
GRF_SOC_CON16	0x0040	W	0x00000600	System control register 16
GRF_SOC_CON17	0x0044	W	0x00000000	System control register 17
GRF_SOC_CON18	0x0048	W	0x00000000	System control register 18
GRF_SOC_CON19	0x004C	W	0x00000000	System control register 19
GRF_SOC_CON20	0x0050	W	0x00000000	System control register 20
GRF_SOC_CON21	0x0054	W	0x00000021	System control register 21
GRF_SOC_CON22	0x0058	W	0x00000000	System control register 22
GRF_SOC_CON23	0x005C	W	0x00000155	System control register 23
GRF_SOC_CON24	0x0060	W	0x00008C52	System control register 24
GRF_SOC_CON25	0x0064	W	0x00000080	System control register 25
GRF_SOC_CON26	0x0068	W	0x00000000	System control register 26
GRF_SOC_CON27	0x006C	W	0x00000000	System control register 27
GRF_SOC_CON28	0x0070	W	0x00008452	System control register 28
GRF_SOC_CON29	0x0074	W	0x00000080	System control register 29
GRF_SOC_CON30	0x0078	W	0x00000000	System control register 30
GRF_SOC_CON31	0x007C	W	0x00000000	System control register 31
GRF_SOC_CON32	0x0080	W	0x00000000	System control register 32
GRF_SOC_CON33	0x0084	W	0x00000000	System control register 33
GRF_SOC_CON35	0x008C	W	0x00000000	System control register 35
GRF_SOC_CON36	0x0090	W	0x00000000	System control register 36
GRF_SOC_CON37	0x0094	W	0x00000010	System control register 37
GRF_SOC_CON38	0x0098	W	0x00000000	System control register 38
GRF_SOC_CON39	0x009C	W	0x00000000	System control register 39

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Name	Offset	Size	Reset Value	Description
GRF_SOC_CON40	0x00A0	W	0x00000000	System control register 40
GRF_SOC_CON41	0x00A4	W	0x00000000	System control register 41
GRF_SOC_CON42	0x00A8	W	0x00000000	System control register 48
GRF_SOC_CON43	0x00AC	W	0x00000000	System control register 43
GRF_SOC_STATUS0	0x0100	W	0x00000000	System status register 0
GRF_SOC_STATUS1	0x0104	W	0x00000000	System status register 1
GRF_SOC_STATUS2	0x0108	W	0x00000000	System status register 2
GRF_DDR_STATUS0	0x0110	W	0x00000000	DDR status register 0
GRF_DDR_STATUS1	0x0114	W	0x00000000	DDR status register 1
GRF_USBPHY_STATUS	0x0118	W	0x00000708	USB PHY status register
GRF_USBOTG0_SIG_DETECT_CON	0x0150	W	0x00000000	USB OTG0 detection control register
GRF_USBOTG0_SIG_DETECT_STATUS	0x0154	W	0x00000000	USB OTG0 detection status register
GRF_USBOTG0_SIG_DETECT_CLR	0x0158	W	0x00000000	USB OTG0 detection clear register
GRF_USBOTG0_VBUSVALID_DETECT_CON	0x015C	W	0x00030100	USB OTG0 vbusvalid control register
GRF_USBOTG0_LINESTATE_DETECT_CON	0x0160	W	0x00030100	USB OTG0 linestate control register
GRF_USBOTG0_DISCONNECT_DETECT_CON	0x0164	W	0x00030100	USB OTG0 disconnect control register
GRF_USBOTG0_BVALID_DETECT_CON	0x0168	W	0x00030100	USB OTG0 bvalid control register
GRF_USBOTG0_ID_DETECT_CON	0x016C	W	0x00030100	USB OTG0 id control register
GRF_USBOTG1_SIG_DETECT_CON	0x0170	W	0x00000000	USB OTG1 detection control register
GRF_USBOTG1_SIG_DETECT_STATUS	0x0174	W	0x00000000	USB OTG1 detection status register
GRF_USBOTG1_SIG_DETECT_CLR	0x0178	W	0x00000000	USB OTG1 detection clear register
GRF_USBOTG1_VBUSVALID_DETECT_CON	0x017C	W	0x00030100	USB OTG1 vbusvalid control register
GRF_USBOTG1_LINESTATE_DETECT_CON	0x0180	W	0x00030100	USB OTG1 linestate control register
GRF_USBOTG1_DISCONNECT_DETECT_CON	0x0184	W	0x00030100	USB OTG1 disconnect control register
GRF_USBOTG1_BVALID_DETECT_CON	0x0188	W	0x00030100	USB OTG1 bvalid control register
GRF_USBOTG1_ID_DETECT_CON	0x018C	W	0x00030100	USB OTG1 id control register
GRF_MAC0_MCGR_ACK	0x01A0	W	0x00000000	MAC0 MCGR ACK register
GRF_MAC1_MCGR_ACK	0x01A4	W	0x00000000	MAC1 MCGR ACK register
GRF_OS_REG0	0x0200	W	0x00000000	OS register 0
GRF_OS_REG1	0x0204	W	0x00000000	OS register 1
GRF_OS_REG2	0x0208	W	0x00000000	OS register 2
GRF_OS_REG3	0x020C	W	0x00000000	OS register 3
GRF_OS_REG4	0x0210	W	0x00000000	OS register 4
GRF_OS_REG5	0x0214	W	0x00000000	OS register 5
GRF_OS_REG6	0x0218	W	0x00000000	OS register 6
GRF_OS_REG7	0x021C	W	0x00000000	OS register 7
GRF_OS_REG8	0x0220	W	0x00000000	OS register 8

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Name	Offset	Size	Reset Value	Description
GRF_OS_REG9	0x0224	W	0x00000000	OS register 9
GRF_OS_REG10	0x0228	W	0x00000000	OS register 10
GRF_OS_REG11	0x022C	W	0x00000000	OS register 11
GRF_SOC_VERSION	0x0300	W	0x00003506	SOC version register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.3.2 Detail Registers Description

GRF_SOC_CON0

Address: Operational Base(0xFF288000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sdmmc_hprot_bufferable AHB master write bufferable 1'b0: Non bufferable 1'b1: Bufferable
14	RW	0x0	otg1_hprot_bufferable AHB master write bufferable 1'b0: Non bufferable 1'b1: Bufferable
13	RW	0x0	otg0_hprot_bufferable AHB master write bufferable 1'b0: Non bufferable 1'b1: Bufferable
12	RW	0x0	mcu_hprot_bufferable AHB master write bufferable 1'b0: Non bufferable 1'b1: Bufferable
11	RO	0x0	reserved
10	RW	0x1	grf_con_dsm_sel 1'b0: Audio DSM SCLK/LRCK from IO when in slave mode 1'b1: Audio DSM SCLK/LRCK from SAI3 when in slave mode
9	RW	0x0	grf_con_sai3_sel 1'b0: SAI3 SCLK/LRCK from IO when in slave mode 1'b1: SAI3 SCLK/LRCK from AudiDSM when in slave mode
8	RW	0x0	grf_spdif_rx_loopback_tx SPDIF RX loop to SPDIF TX 1'b1: RX loop back to TX 1'b0: Normal mode
7	RW	0x0	ddrmonitor_external_trigger_en 1'b0: Disable 1'b1: Enable
6	RW	0x1	vop_dcf_idle 1'b0: Un-idle 1'b1: Idle

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	grf_jtag_sel JTAG select. 2'b00: When port M0 enable, port M1 enable: port M0 for MCU, port M1 for A7 When port M0 enable, port M1 disable: port M0 for A7 When port M0 disable, port M1 enable: port M1 for A7 2'b01: When port M0 enable, port M1 enable: port M0 for MCU, port M1 for A7 When port M0 enable, port M1 disable: port M0 for MCU When port M0 disable, port M1 enable: port M1 for A7 2'b10: When port M0 enable, port M1 enable: port M0 for A7, port M1 for MCU When port M0 enable, port M1 disable: port M0 for A7 When port M0 disable, port M1 enable: port M1 for MCU 2'b11: Reserved Note: User can set IOMUX GPIO3_GPIO3A_IOMUX_SEL_1[7:0] = 8'h22 to enable JTAG port M0 and set GPIO0_GPIO0C_IOMUX_SEL_1[15:8] = 8'h22 to enable JTAG port M1.
3	RW	0x0	grf_saradc_pd_sel 1'b1: SARADC PHY power down controlled by grf_saradc_pd 1'b0: SARADC PHY power down controlled by SARADC controller
2	RW	0x1	grf_saradc_pd 1'b0: SARADC PHY power up 1'b1: SARADC PHY power down
1:0	RO	0x0	reserved

GRF_SOC_CON1

Address: Operational Base(0xFF288000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	dsmc_slave_rdyn_mode DSMC_SLV_RDYN output mode 1'b0: Open drain output mode 1'b1: Normal mode, user can set gpio1d3_od=1 to enable open drain output.
4	RW	0x0	dsmc_slave_enable DSMC slave enable When DSMC slave is enable, the FLEXBUS can not be used.
3	RW	0x0	grf_sai3_mclk_oen SAI3 MCLK output enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	grf_sai2_mclk_oen SAI2 MCLK output enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	grf_flexbus1_con grf_flexbus1_con[0] 1'b0: FLEXBUS1 input clock invert disable 1'b1: FLEXBUS1 input clock invert enable grf_flexbus1_con[1] 1'b0: FLEXBUS1 input data two flip-flop pipe bypass disable 1'b1: FLEXBUS1 input data two flip-flop pipe bypass

GRF_SOC_CON2

Address: Operational Base(0xFF288000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:4	RW	0x00	grf_vop_ddl_sel Delayline element select
3	RO	0x0	reserved
2	RW	0x0	grf_vop_data_bypass 1'b0: Use two flip-flop pipe in VOP LCD IO 1'b1: Bypass two flip-flop pipe in VOP LCD IO
1	RW	0x0	grf_vop_dclk_bypass 1'b0: Use two flip-flop pipe in VOP LCD IO 1'b1: Bypass two flip-flop pipe in VOP LCD IO
0	RW	0x0	grf_vop_dclk_inv VOP DCLK invert selection 1'b0: Bypass invert 1'b1: Select invert

GRF_SOC_CON3

Address: Operational Base(0xFF288000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	uart5_rts_inv Polarity selection for uart5_rts. 1'b0: Low active 1'b1: High active
12	RW	0x0	uart4_rts_inv Polarity selection for uart4_rts. 1'b0: Low active 1'b1: High active
11	RW	0x0	uart3_rts_inv Polarity selection for uart3_rts. 1'b0: Low active 1'b1: High active
10:6	RO	0x00	reserved
5	RW	0x0	uart5_cts_inv Polarity selection for uart5_cts. 1'b0: Low active 1'b1: High active

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Bit	Attr	Reset Value	Description
4	RW	0x0	uart4_cts_inv Polarity selection for uart4_cts. 1'b0: Low active 1'b1: High active
3	RW	0x0	uart3_cts_inv Polarity selection for uart3_cts. 1'b0: Low active 1'b1: High active
2:0	RO	0x0	reserved

GRF_SOC_CON4

Address: Operational Base(0xFF288000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	tsadc_phy_pd_sel 1'b1: TSADC PHY power down controlled by grf_tsadc_pd 1'b0: TSADC PHY power down controlled by TSADC controller
9	RW	0x0	tsadc_phy_pd 1'b1: TSADC PHY power up 1'b0: TSADC PHY power down
8	RW	0x0	tsadc_tsen_en TSADC enable register. 1'b1: Enable 1'b0: Disable
7:0	RW	0x00	tsadc_ana_reg TSADC configure registers.

GRF_SOC_CON5

Address: Operational Base(0xFF288000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	grf_io_mipi_te_sel VOP MIPI TE selection 1'b0: From DSI controller 1'b1: From IO
2	RW	0x0	grf_dsi_dpiupdatacfg DSI dpi update configuration
1	RW	0x0	grf_dsi_dpicolorm DSI dpi colorm
0	RW	0x0	grf_dsi_dpishutdn DSI dpi shut down

GRF_SOC_CON6

Address: Operational Base(0xFF288000) + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_dsiphy_txskewcalhs_3 Request to transmit skew calibration on lane3. 1'b1: Request 1'b0: Idle
14	RW	0x0	grf_dsiphy_txskewcalhs_2 Request to transmit skew calibration on lane2. 1'b1: Request 1'b0: Idle
13	RW	0x0	grf_dsiphy_txskewcalhs_1 Request to transmit skew calibration on lane1. 1'b1: Request 1'b0: Idle
12	RW	0x0	grf_dsiphy_txskewcalhs_0 Request to transmit skew calibration on lane0. 1'b1: Request 1'b0: Idle
11	RW	0x0	grf_dsiphy_txskewcalhs_ck Request to transmit skew calibration on clock lane. 1'b1: Request 1'b4: Idle
10	RO	0x0	reserved
9	RW	0x0	grf_dsiphy_phyenable_1 DSI TX PHY enable of lane1. 1'b0: Disable 1'b1: Enable
8	RW	0x0	grf_dsiphy_phyenable_0 DSI TX PHY enable of lane0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	grf_dsiphy_lane3_frctxstopm Force DSI TX PHY lane3 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
6	RW	0x0	grf_dsiphy_lane2_frctxstopm Force DSI TX PHY lane2 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
5	RW	0x0	grf_dsiphy_lane1_frctxstopm Force DSI TX PHY lane1 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
4	RW	0x0	grf_dsiphy_lane0_frctxstopm Force DSI TX PHY lane0 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	grf_dsiphy_turndisable Disable Turn-around. This signal is used to prevent Lane from going into transmit mode, even if it observes a turn-around request on the Lane interconnect
1	RO	0x0	reserved
0	RW	0x0	grf_dsiphy_forcerxmode Force DSI TX PHY lane module into Receive mode, wait for stop state 1'b0: Disable 1'b1: Enable

GRF_SOC_CON7

Address: Operational Base(0xFF288000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	otg1_dbnce_fltr_bypass USB OTG1 debounce filter bypass
5:4	RW	0x0	otg1_scaledown_mode USB OTG1 scale down mode
3	RO	0x0	reserved
2	RW	0x0	otg0_dbnce_fltr_bypass USB OTG0 debounce filter bypass
1:0	RW	0x0	otg0_scaledown_mode USB OTG0 scale down mode

GRF_SOC_CON8

Address: Operational Base(0xFF288000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	mac0_ptp_aux_ts_trig Auxiliary Time Stamp Trigger. This signal is asserted to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO. A rising edge on this port is used to trigger the auxiliary snapshot.
7	RW	0x0	mac0_mcg_pst_trig Trigger Input to the DUT to capture presentation time.
6	RW	0x0	mac0_mcg_pst_trig_sel Trigger Input to the DUT to capture presentation time. From IO or software. 1'b1: From IO 1'b0: From mac_mcg_pst_trig.
5	RW	0x0	mac0_extclk_sel 1'b0: select TX clock from CRU 1'b1: select TX clock from IO

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	mac0_rmii_txclk_sel Mac clock divide sel. 2'b00: 2.5Mhz 2'b01: 25Mhz Others: Reserved
2	RW	0x0	mac0_rmii_gate_en If this bit set to 1'b1, this bit will gate RMII clk.
1	RW	0x0	mac0_rmii_mode If using RMII mode, set this bit to 1'b1, otherwise set this bit to 1'b0.
0	RW	0x0	mac0_sbd_flowctrl Sideband signal to transmit control packet or active backpressure.

GRF_SOC_CON9

Address: Operational Base(0xFF288000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	saradc_ana_reg SARADC analog register configuration

GRF_SOC_CON10

Address: Operational Base(0xFF288000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	grf_con_wdt1_reset_to_io_en WDT1 timeout reset to io 1'b0: Disable 1'b1: Enable
8	RW	0x0	grf_con_wdt0_reset_to_io_en WDT0 timeout reset to io 1'b0: Disable 1'b1: Enable
7:4	RO	0x0	reserved
3	RW	0x0	wdt1_speedup WDT1 speed up enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wdt1_pause_en WDT1 pause enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	wdt0_speedup WDT0 speed up enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	wdt0_pause_en WDT0 pause enable. 1'b0: Disable 1'b1: Enable

GRF_SOC_CON11

Address: Operational Base(0xFF288000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	mac1_ptp_aux_ts_trig Auxiliary Time Stamp Trigger. This signal is asserted to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO. A rising edge on this port is used to trigger the auxiliary snapshot.
7	RW	0x0	mac1_mcg_pst_trig Trigger Input to the DUT to capture presentation time.
6	RW	0x0	mac1_mcg_pst_trig_sel Trigger Input to the DUT to capture presentation time. From IO or software. 1'b1: From IO 1'b0: From mac_mcg_pst_trig.
5	RW	0x0	mac1_extclk_sel 1'b0: select TX clock from CRU 1'b1: select TX clock from IO
4:3	RW	0x0	mac1_rmii_txclk_sel Mac clock divide sel. 2'b00: 2.5Mhz 2'b01: 25Mhz Others: Reserved
2	RW	0x0	mac1_rmii_gate_en If this bit set to 1'b1, this bit will gate RMII clk.
1	RW	0x0	mac1_rmii_mode If using RMII mode, set this bit to 1'b1, otherwise set this bit to 1'b0.
0	RW	0x0	mac1_sbd_flowctrl Sideband signal to transmit control packet or active backpressure.

GRF_SOC_CON13

Address: Operational Base(0xFF288000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	timer1ch5_dsmc_intr_intmux_sel TIMER1_CH5 and DSMC interrupt to INTMUX selection 1'b0: DSMC 1'b1: TIMER1_CH5

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Bit	Attr	Reset Value	Description
6	RW	0x0	timer1ch5_dsmc_intr_mcu_sel TIMER1_CH5 and DSMC interrupt to MCU selection 1'b0: DSMC 1'b1: TIMER1_CH5
5	RW	0x0	gpio1_3_intr_intmux_sel GPIO1_3 interrupt to INTMUX selection 1'b0: GPIO1 1'b1: GPIO1_SHADOW
4	RW	0x0	gpio1_2_intr_intmux_sel GPIO1_2 interrupt to INTMUX selection 1'b0: GPIO1 1'b1: GPIO1_SHADOW
3	RW	0x0	gpio1_1_intr_intmux_sel GPIO1_1 interrupt to INTMUX selection 1'b0: GPIO1 1'b1: GPIO1_SHADOW
2	RW	0x0	gpio1_3_intr_mcu_sel GPIO1_3 interrupt to MCU selection 1'b0: GPIO1 1'b1: GPIO1_SHADOW
1	RW	0x0	gpio1_2_intr_mcu_sel GPIO1_2 interrupt to MCU selection 1'b0: GPIO1 1'b1: GPIO1_SHADOW
0	RW	0x0	gpio1_1_intr_mcu_sel GPIO1_1 interrupt to MCU selection 1'b0: GPIO1 1'b1: GPIO1_SHADOW

GRF_SOC_CON14

Address: Operational Base(0xFF288000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	ddr_probe_suspend DDR probe suspend 1'b0: Not suspend 1'b1: Suspend
11	RW	0x1	corep_to_core_stall Response type when BIU_CORE or BIU_DSMC_FLEXBUS in idle state and DSMC_FLEXBUS access CORE. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
10	RW	0x1	core_to_corep_stall Response type when BIU_CORE or BIU_DSMC_FLEXBUS in idle state and CORE access DSMC_FLEXBUS. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted

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Bit	Attr	Reset Value	Description
9	RW	0x1	core_to_ddr_stall Response type when BIU_CORE or BIU_DDR in idle state and CORE access DDR. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
8	RW	0x1	core_to_bus_stall Response type when BIU_CORE or BIU_BUS in idle state and CORE access BUS. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
7	RW	0x1	hsperi_to_bus_stall Response type when BIU_HSPERI or BIU_BUS in idle state and HSPERI access BUS. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
6	RW	0x1	vio_to_ddr_stall Response type when BIU_VIO or BIU_DDR in idle state and VIO access DDR. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
5	RO	0x0	reserved
4	RW	0x1	bus_to_vio_stall Response type when BIU_BUS or BIU_VIO in idle state and BUS access VIO. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
3	RW	0x1	bus_to_lsperi_stall Response type when BIU_BUS or BIU_LSPERI in idle state and BUS access LSPERI. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
2	RW	0x1	bus_to_hsperi_stall Response type when BIU_BUS or BIU_HSPERI in idle state and BUS access HSPERI. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
1	RW	0x1	bus_to_ddr_stall Response type when BIU_BUS or BIU_DDR in idle state and BUS access DDR. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted
0	RW	0x1	mcu_to_core_stall Response type when BIU_MCU or BIU_CORE in idle state and MCU access CORE. 1'b0: BIU return ERROR response 1'b1: BIU hold the bus until the NIU idle state is de-asserted

GRF_SOC_CON15

Address: Operational Base(0xFF288000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	grf_con_ddrc_wr_mask_by_hpr 1'b0: The DDRCTL write commands will go to critical state according to write urgent and ignores the number of HPR credits. 1'b1: The DDRCTL write commands will go to critical state according to write urgent and when the HPR credits is equal to hpr_entry_num.
12:7	RW	0x00	grf_con_ddrc_hpr_entry_num The HPR entry numbers that used to make write command go to critical when wr_mask_by_hpr is set to 1'b1. If wr_mask_by_hpr is set to 1'b0, hpr_entry_num is not used.
6	RW	0x0	grf_con_ddrc_rrbtoken_empty2critical 1'b0: The DDRCTL read commands will go to critical state controlled by read urgent. 1'b1: The DDRCTL read commands will go to critical state controlled by read urgent and when reorder buffer read token is empty.
5	RW	0x0	grf_con_ddrc_wr_full2critical 1'b0: The DDRCTL write commands will go to critical state controlled by write urgent. 1'b1: The DDRCTL write commands will go to critical state controlled by write urgent and when write credits are empty.
4	RW	0x0	grf_con_ddrc_hpr_full2critical 1'b0: The DDRCTL read commands will go to critical state controlled by read urgent. 1'b1: The DDRCTL read commands will go to critical state controlled by read urgent and when HPR credits are empty.
3	RW	0x0	grf_con_ddrc_lpr_full2critical 1'b0: The DDRCTL read commands will go to critical state controlled by read urgent. 1'b1: The DDRCTL read commands will go to critical state controlled by read urgent and when LPR credits are empty.
2:0	RO	0x0	reserved

GRF_SOC_CON16

Address: Operational Base(0xFF288000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	grf_con_selfref_type2_en 1'b0: Only allowed core clock of DDRCTL to be gated when SDRAM's self-refresh is caused by automatic self-refresh. 1'b1: Allowed core clock of DDRCTL to be gated when SDRAM's self-refresh is not caused by automatic self-refresh.
11:8	RW	0x6	grf_con_ddrc_auto_sr_dly When SDRAM is in self-refresh state whose type is indicated by grf_con_selfref_type2_en, the core clock of DDRCTL will be gated after grf_con_ddrc_auto_sr_dly clocks.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	grf_con_ddrctl_syscreq_cg_en 1'b0: Core clock of DDRCTL is allowed to be gated when csysreq_ddrc^csysack_ddrc==1. 1'b1: Core clock of DDRCTL would not be gated when csysreq_ddrc^csysack_ddrc==1.
5	RW	0x0	grf_con_ddrctl_core_cg_en 1'b0: Do not gate core clock of DDRCTL 1'b1: Gate core clock of DDRCTL unless following two case: Case1: grf_con_ddrctl_apb_cg_en==1'b1 and the APB slave select of DDRCTL is asserted Case2: grf_con_ddrctl_syscreq_cg_en==1'b1 and csysreq_ddrc^csysack_ddrc==1
4	RW	0x0	grf_con_ddrctl_apb_cg_en1 1'b0: Axi1 clock and core clock of DDRCTL is allowed to be gated when APB slave select of DDRCTL is asserted. 1'b1: Axi1 clock and core clock of DDRCTL would not be gated when APB slave select of DDRCTL is asserted.
3	RW	0x0	grf_con_ddrctl_apb_cg_en0 1'b0: Axi0 clock and core clock of DDRCTL is allowed to be gated when APB slave select of DDRCTL is asserted. 1'b1: Axi0 clock and core clock of DDRCTL would not be gated when APB slave select of DDRCTL is asserted.
2	RW	0x0	grf_con_ddrctl_axi1_cg_en 1'b0: Do not gate axi1 clock of DDRCTL 1'b1: Gate axi1 clock of DDRCTL unless grf_con_ddrctl_apb_cg_en1==1'b1 and the APB slave select of DDRCTL is asserted.
1	RW	0x0	grf_con_ddrctl_axi0_cg_en 1'b0: Do not gate axi0 clock of DDRCTL 1'b1: Gate axi0 clock of DDRCTL unless grf_con_ddrctl_apb_cg_en0==1'b1 and the APB slave select of DDRCTL is asserted.
0	RW	0x0	grf_con_upctl2_scramble_gate_dis Scramble clock gating disable 1'b0: The clock of scramble is gating controlled scramble_bypass 1'b1: The clock of scramble is always enable

GRF_SOC_CON17

Address: Operational Base(0xFF288000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	grf_con_arautopre Connected to the DDRCTL's input signal 'arautopre'. The 'arautopre' is AXI auto-precharge signal for read command.
13:12	RW	0x0	grf_con_awpoison Connected to the DDRCTL's input signal 'awpoison'. The 'awpoison' is an off-band signal to indicate an invalid write transaction.
11:10	RW	0x0	grf_con_awurgent Connected to the DDRCTL's input AXI write urgent signal 'awurgent'.

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	grf_con_arpoison Connected to the DDRCTL's input signal 'arpoison'. The 'arpoison' is a sideband signal to indicate an invalid read transaction.
7:6	RW	0x0	grf_con_arurgent Connected to the DDRCTL's input AXI read urgent signal 'arurgent'.
5:4	RW	0x0	grf_con_pa_wmask Connected to the DDRCTL's input write port mask signal 'pa_wmask'.
3:0	RW	0x0	grf_con_pa_rmask Connected to DDRCTL's input read port mask signal 'pa_rmask'.

GRF_SOC_CON18

Address: Operational Base(0xFF288000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	grf_con_ddrc_press_queue_wait_limit The press queue wait limit time of DDRCTL's urgent control module.
9:8	RW	0x0	grf_con_ddrc_press_policy The press policy of DDRCTL's urgent control module.
7:6	RW	0x0	grf_con_ddrc_press_rdwr_order Read/write order enable of DDRCTL's urgent control module. Each bit is corresponding to DDRCTL's AXI port 0~1 respectively. For example, press_rdwr_order[0] is used to control AXI port 0, press_rdwr_order[1] is used to control AXI port 1 and so on.
5:4	RW	0x0	grf_con_ddrc_press_cg_en Clock gate enable of DDRCTL's urgent control module. Each bit is corresponding to DDRCTL's AXI port 0~1 respectively. 1'b0: Disable 1'b1: Enable If the DDRCTL's urgent control module is not used, please set press_cg_en[1:0] to 2'h3 to save power.
3:2	RW	0x0	grf_con_ddrc_press_en Press enable, bit0 for port0 and bit1 for port1
1:0	RW	0x0	grf_con_awautopre Connected to the DDRCTL's input signal 'awautopre'. The 'awautopre' is AXI auto-precharge signal for write command.

GRF_SOC_CON19

Address: Operational Base(0xFF288000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	grf_con_ddrc_awqos_urgent_en Enable the urgent mechanism of DDRCTL's AXI write port 0~1 according to the Aw-QoS. Each bit is corresponding to DDRCTL's AXI write port 0~1 respectively. For example, awqos_urgent_en[0] is used to enable AXI write port 0, awqos_urgent_en[1] is used to enable AXI write port 1 and so on. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	grf_con_ddrc_arqos_urgent_en Enable the urgent mechanism of DDRCTL's AXI read port 0~1 according to the Ar-QoS. Each bit is corresponding to DDRCTL's AXI read port 0~1 respectively. For example, arqos_urgent_en[0] is used to enable AXI read port 0, arqos_urgent_en[1] is used to enable AXI read port 1 and so on. 1'b0: Disable 1'b1: Enable
9	RW	0x0	grf_con_csysreq_axi_ddrlpc 1'b0: The hardware low power request signal of AXI block, is not related to DDR_LPC low power module. 1'b1: The hardware low power request signal of AXI block, can be generated by DDR_LPC low power module.
8	RW	0x0	grf_con_csysreq_axi_pmu 1'b0: The hardware low power request signal of AXI block, is not related to PMU. 1'b1: The hardware low power request signal of AXI block, can be generated by PMU.
7	RW	0x0	grf_con_csysreq_ddrc_ddrlpc 1'b0: The hardware low power request signal of DDRCTL, is not related to DDR_LPC low power module. 1'b1: The hardware low power request signal of DDRCTL, can be generated by DDR_LPC low power module.
6	RW	0x0	grf_con_csysreq_ddrc_pmu 1'b0: The hardware low power request signal of DDRCTL, is not related to PMU. 1'b1: The hardware low power request signal of DDRCTL, can be generated by PMU.
5	RO	0x0	reserved
4	RW	0x0	grf_con_dfi_init_complete When grf_con_dfi_init_complete_sel==1'b1, this signal is selected as DDRCTL's input signal, dfi_init_complete.
3	RW	0x0	grf_con_dfi_init_complete_sel 1'b0: DDRCTL's input signal, dfi_init_complete, is generated by DDR PHY. 1'b1: DDRCTL's input signal, dfi_init_complete, is connected from grf_con_dfi_init_complete.
2	RW	0x0	grf_con_dfi_init_start When grf_con_dfi_init_start_sel==1'b1, this signal is selected as DDRPHY's input signal, dfi_init_start.
1	RW	0x0	grf_con_dfi_init_start_sel 1'b0: DDRPHY's input signal, dfi_init_start, is generated by DDR_LPC low power module, dfi_ctl module or DDRCTL. 1'b1: DDRPHY's input signal, dfi_init_start, is connected from grf_con_dfi_init_start.

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Bit	Attr	Reset Value	Description
0	RW	0x0	grf_con_upctl_slverr_enable 1'b0: Disable DDRCTL APB slave error respond. 1'b1: Enable DDRCTL APB slave error respond.

GRF_SOC_CON20

Address: Operational Base(0xFF288000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	grf_con_press_aw_th Write QoS threshold.
7:0	RW	0x00	grf_con_press_ar_th Read QoS threshold.

GRF_SOC_CON21

Address: Operational Base(0xFF288000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x021	mem_cfg_uhdspra Single port memory timing adjustment setting for debug purpose. [1:0]: RTSEL for Standard voltage threshold and all column mux option [3:2]: WTSEL for Standard voltage threshold and all column mux option [5:4]: RTSEL for high voltage threshold and column mux option equal to 1,2 [7:6]: WTSEL for high voltage threshold and column mux option equal to 1,2 [9:8]: RTSEL for high voltage threshold and column mux option equal to 4 [11:10]: WTSEL for high voltage threshold and column mux option equal to 4

GRF_SOC_CON22

Address: Operational Base(0xFF288000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x00	mem_cfg_uhddpra Dual port memory timing adjustment setting for debug purpose. [1:0]: RTSEL [3:2]: WTSEL [5:4]: PTSEL

GRF_SOC_CON23

Address: Operational Base(0xFF288000) + offset (0x005C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x155	mem_cfg_rom ROM memory timing adjustment setting for debug purpose. [1:0]: PTSEL_M [3:2]: RTSEL_M [5:4]: TRB_M [7:6]: PTSEL_F [9:8]: RTSEL_F [11:10]: TRBT_F

GRF_SOC_CON24

Address: Operational Base(0xFF288000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	usbotg0_utmi_bvalid Software configuration for usbotg_utmi_bvalid.
14	RW	0x0	usbotg0_utmi_bvalid_sel usbotg_utmi_bvalid selection. 1'b0: usbotg_utmi_bvalid comes from USB PHY 1'b1: usbotg_utmi_bvalid comes from usbotg0_utmi_bvalid
13:12	RO	0x0	reserved
11	RW	0x1	usbotg0_utmi_idpullup usbotg_utmi_idpullup configuration.
10	RW	0x1	usbotg0_utmi_iddig Software configuration for usbotg_utmi_iddig.
9	RW	0x0	usbotg0_utmi_iddig_sel usbotg_utmi_iddig selection. 1'b0: usbotg_utmi_iddig comes from USB PHY 1'b1: usbotg_utmi_iddig comes from usbotg0_utmi_iddig
8	RW	0x0	usbotg0_utmi_dmpulldown Software configuration for usbotg_utmi_dmpulldown when usbphy_sw_en is high.
7	RW	0x0	usbotg0_utmi_dppulldown Software configuration for usbotg_utmi_dppulldown when usbphy_sw_en is high.
6	RW	0x1	usbotg0_utmi_termselect Software configuration for usbotg_utmi_termselect when usbphy_sw_en is high.
5:4	RW	0x1	usbotg0_utmi_xcvrselect Software configuration for usbotg_utmi_xcvrselect when usbphy_sw_en is high.
3:2	RW	0x0	usbotg0_utmi_opmode Software configuration for usbotg_utmi_opmode when usbphy_sw_en is high.
1	RW	0x1	usbotg0_utmi_suspend_n Software configuration for usbotg_utmi_suspend_n when usbphy_sw_en is high.

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Bit	Attr	Reset Value	Description
0	RW	0x0	usbotg0_sw_en USB OTG0 software configuration enable. 1'b0: Disable 1'b1: Enable

GRF_SOC_CON25

Address: Operational Base(0xFF288000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	usbotg0_utmi_fs_se0 Serial mode communication SE0 data
8	RW	0x0	usbotg0_utmi_fs_data Serial mode communication data
7	RW	0x1	usbotg0_utmi_fs_oe Serial mode communication output enable
6	RW	0x0	usbotg0_utmi_fs_xver_own Serial mode communication enable
5:4	RO	0x0	reserved
3	RW	0x0	usbotg0_utmi_avalid Software configuration for usbhost_utmi_avalid.
2	RW	0x0	usbotg0_utmi_avalid_sel usbotg_utmi_avalid selection. 1'b0: usbotg_utmi_avalid comes from USBPHY 1'b1: usbotg_utmi_avalid comes from usbotg0_utmi_avalid
1	RW	0x0	usbotg0_utmi_sessend Software configuration for usbhost_utmi_senssend.
0	RW	0x0	usbotg0_utmi_sessend_sel usbotg_utmi_sessend selection. 1'b0: usbotg_utmi_sessend comes from USBPHY 1'b1: usbotg_utmi_sessend comes from usbotg0_utmi_sessend

GRF_SOC_CON26

Address: Operational Base(0xFF288000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	usbotg0_utmi_dischrgvbus usbotg_utmi_dischrgvbus configuration.
7	RW	0x0	usbotg0_utmi_chrgvbus usbotg_utmi_chrgvbus configuration.
6	RO	0x0	reserved
5	RW	0x0	usbotg0_utmi_drvvbus Software configuration for usbotg_utmi_drvvbus.
4	RW	0x0	usbotg0_utmi_drvvbus_sel usbotg_utmi_drvvbus selection. 1'b0: usbotg_utmi_drvvbus comes from USB PHY 1'b1: usbotg_utmi_drvvbus comes from usbotg0_utmi_drvvbus
3:0	RO	0x0	reserved

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GRF_SOC_CON27

Address: Operational Base(0xFF288000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	usbphy_bc_weakpulldown_tune Software configuration for usbphy_bc_weakpulldown_tune.
13:12	RW	0x0	usbphy_bc_weakpullup_tune Software configuration for usbphy_bc_weakpullup_tune.
11	RW	0x0	usbphy_bc_weakpulldown_en Software configuration for usbphy_bc_weakpulldown_en.
10	RW	0x0	usbphy_bc_weakpullup_en Software configuration for usbphy_bc_weakpullup_en.
9	RW	0x0	usbphy_force_dcp_det Software configuration for usbphy_force_dcp_det.
8	RW	0x0	usbphy_force_cp_det Software configuration for usbphy_force_cp_det.
7	RW	0x0	usbphy_force_dp_attached Software configuration for usbphy_force_dp_attached.
6	RW	0x0	usbphy_charge_det_byp Software configuration for usbphy_charge_det_byp.
5	RW	0x0	usbphy_vdm_src_en Software configuration for usbphy_vdm_src_en.
4	RW	0x0	usbphy_vdp_src_en Software configuration for usbphy_vdp_src_en.
3	RW	0x0	usbphy_rdm_pdwn_en Software configuration for usbphy_rdm_pdwn_en.
2	RW	0x0	usbphy_idp_src_en Software configuration for usbphy_idp_src_en.
1	RW	0x0	usbphy_idm_sink_en Software configuration for usbphy_idm_sink_en.
0	RW	0x0	usbphy_idp_sink_en Software configuration for usbphy_idp_sink_en.

GRF_SOC_CON28

Address: Operational Base(0xFF288000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	usbotg1_utmi_bvalid Software configuration for usbhost_utmi_bvalid.
14	RW	0x0	usbotg1_utmi_bvalid_sel usbhost_utmi_bvalid selection. 1'b0: usbhost_utmi_bvalid tie high 1'b1: usbhost_utmi_bvalid comes from usbotg1_utmi_bvalid
13:11	RO	0x0	reserved
10	RW	0x1	usbotg1_utmi_iddig Software configuration for usbhost_utmi_iddig.

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Bit	Attr	Reset Value	Description
9	RW	0x0	usbotg1_utmi_iddig_sel usbhost_utmi_iddig selection. 1'b0: usbhost_utmi_iddig comes from USB PHY 1'b1: usbhost_utmi_iddig comes from usbotg1_utmi_iddig
8	RW	0x0	usbotg1_utmi_dmpulldown Software configuration for usbhost_utmi_dmpulldown when usbhost_sw_en is high.
7	RW	0x0	usbotg1_utmi_dppulldown Software configuration for usbhost_utmi_dppulldown when usbhost_sw_en is high.
6	RW	0x1	usbotg1_utmi_termselect Software configuration for usbhost_utmi_termselect when usbhost_sw_en is high.
5:4	RW	0x1	usbotg1_utmi_xcvrselect Software configuration for usbhost_utmi_xcvrselect when usbhost_sw_en is high.
3:2	RW	0x0	usbotg1_utmi_opmode Software configuration for usbhost_utmi_opmode when usbhost_sw_en is high.
1	RW	0x1	usbotg1_utmi_suspend_n Software configuration for usbhost_utmi_suspend_n when usbhost_sw_en is high.
0	RW	0x0	usbotg1_sw_en USB OTG1 software configuration enable. 1'b0: Disable 1'b1: Enable

GRF_SOC_CON29

Address: Operational Base(0xFF288000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	usbotg1_utmi_fs_se0 Serial mode communication SE0 data
8	RW	0x0	usbotg1_utmi_fs_data Serial mode communication data
7	RW	0x1	usbotg1_utmi_fs_oe Serial mode communication output enable
6	RW	0x0	usbotg1_utmi_fs_xver_own Serial mode communication enable
5:4	RO	0x0	reserved
3	RW	0x0	usbotg1_utmi_avalid Software configuration for usbhost_utmi_avalid when usbhost_sw_en is high.
2	RW	0x0	usbotg1_utmi_avalid_sel usbhost_utmi_avalid selection. 1'b0: usbotg_utmi_avalid tie high 1'b1: usbotg_utmi_avalid comes from SOC_CON29[3]
1	RW	0x0	usbotg1_utmi_sessend Software configuration for usbhost_utmi_sessend.

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Bit	Attr	Reset Value	Description
0	RW	0x0	usbotg1_utmi_sessend_sel usbhost_utmi_sessend selection. 1'b0: usbotg_utmi_sessend tie low 1'b1: usbotg_utmi_sessend comes from usbotg1_utmi_sessend

GRF_SOC_CON30

Address: Operational Base(0xFF288000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_dsmc_req0_dmac_sel 1'b0: DMAC0 channel 2 1'b1: DMAC0 channel 8
14	RW	0x0	grf_dsmc_req1_dmac_sel 1'b0: DMAC0 channel 3 1'b1: DMAC0 channel 10
13:12	RW	0x0	grf_can1_rx_dmac_sel 2'b00: DMAC0 channel 1 2'b01: DMAC1 channel 11 2'b10: DMAC0 channel 5 2'b11: Reserved
11:10	RW	0x0	grf_can0_rx_dmac_sel 2'b00: DMAC0 channel 0 2'b01: DMAC1 channel 10 2'b10: DMAC0 channel 4 2'b11: Reserved
9:0	RO	0x000	reserved

GRF_SOC_CON31

Address: Operational Base(0xFF288000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:10	RW	0x00	grf_gpio234_filter_sel1 GPIO select to go through second filter logic 6'h00: GPIO2A0 6'h01: GPIO2A1 6'h02: GPIO2A2 6'h03: GPIO2A3 6'h04: GPIO2A4 6'h05: GPIO2A5 6'h06: GPIO2B0 6'h07: GPIO2B1 6'h08: GPIO2B2 6'h09: GPIO2B3 6'h0a: GPIO2B4 6'h0b: GPIO2B5 6'h0c: GPIO2B6 6'h0d: GPIO2B7 6'h0d: GPIO2C0 6'h0f: GPIO3A0 6'h10: GPIO3A1 6'h11: GPIO3A2 6'h12: GPIO3A3 6'h13: GPIO3A4 6'h14: GPIO3A5 6'h15: GPIO3A6 6'h16: GPIO3A7 6'h17: GPIO3B0 6'h18: GPIO3B1 6'h19: GPIO3B2 6'h1a: GPIO3B3 6'h1b: GPIO3B4 6'h1c: GPIO3B5 6'h1d: GPIO3B6 6'h1e: GPIO4B0 6'h1f: GPIO4B1 6'h20: GPIO4B2 6'h21: GPIO4B3

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Bit	Attr	Reset Value	Description
9:4	RW	0x00	grf_gpio234_filter_sel0 GPIO select to go through first filter logic 6'h00: GPIO2A0 6'h01: GPIO2A1 6'h02: GPIO2A2 6'h03: GPIO2A3 6'h04: GPIO2A4 6'h05: GPIO2A5 6'h06: GPIO2B0 6'h07: GPIO2B1 6'h08: GPIO2B2 6'h09: GPIO2B3 6'h0a: GPIO2B4 6'h0b: GPIO2B5 6'h0c: GPIO2B6 6'h0d: GPIO2B7 6'h0d: GPIO2C0 6'h0f: GPIO3A0 6'h10: GPIO3A1 6'h11: GPIO3A2 6'h12: GPIO3A3 6'h13: GPIO3A4 6'h14: GPIO3A5 6'h15: GPIO3A6 6'h16: GPIO3A7 6'h17: GPIO3B0 6'h18: GPIO3B1 6'h19: GPIO3B2 6'h1a: GPIO3B3 6'h1b: GPIO3B4 6'h1c: GPIO3B5 6'h1d: GPIO3B6 6'h1e: GPIO4B0 6'h1f: GPIO4B1 6'h20: GPIO4B2 6'h21: GPIO4B3
3:2	RO	0x0	reserved
1:0	RW	0x0	grf_gpio234_filter_en There are two filter circuits for GPIO2, GPIO3 and GPIO4, each bit controls the enable of one filter.

GRF_SOC_CON32

Address: Operational Base(0xFF288000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio234_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_SOC_CON33

Address: Operational Base(0xFF288000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio234_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

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GRF_SOC_CON35

Address: Operational Base(0xFF288000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x0000	reserved
9:7	RW	0x0	grf_pwm1_uart_rx_mux_sel PWM1 biphasic counter UART RX mux selection 3'h0: UART0_RX 3'h1: UART1_RX 3'h2: UART2_RX 3'h3: UART3_RX 3'h4: UART4_RX 3'h5: UART5_RX Others: Reserved
6	RW	0x0	grf_pwm1_phase_a6_sel PWM1 biphasic counter phase a6 select. 1'b0: From RMIO PWM1_CH6 1'b1: From UART RX MUX
5	RW	0x0	grf_pwm1_phase_a5_sel PWM1 biphasic counter phase a5 select. 1'b0: From RMIO PWM1_BIP_CNTR_A5 1'b1: From UART5_RX
4	RW	0x0	grf_pwm1_phase_a4_sel PWM1 biphasic counter phase a4 select. 1'b0: From RMIO PWM1_BIP_CNTR_A4 1'b1: From UART4_RX
3	RW	0x0	grf_pwm1_phase_a3_sel PWM1 biphasic counter phase a3 select. 1'b0: From RMIO PWM1_BIP_CNTR_A3 1'b1: From UART3_RX
2	RW	0x0	grf_pwm1_phase_a2_sel PWM1 biphasic counter phase a2 select. 1'b0: From RMIO PWM1_BIP_CNTR_A2 1'b1: From UART2_RX
1	RW	0x0	grf_pwm1_phase_a1_sel PWM1 biphasic counter phase a1 select. 1'b0: From RMIO PWM1_BIP_CNTR_A1 1'b1: From UART1_RX
0	RW	0x0	grf_pwm1_phase_a0_sel PWM1 biphasic counter phase a0 select. 1'b0: From RMIO PWM1_BIP_CNTR_A0 1'b1: From UART0_RX

GRF_SOC_CON36

Address: Operational Base(0xFF288000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	grf_con_m0_stalib MCU system time calibration

GRF_SOC_CON37

Address: Operational Base(0xFF288000) + offset (0x0094)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:7	RW	0x00	grf_con_mcu_irqlatency IRQLATENCY specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface.
6	RO	0x0	reserved
5	RW	0x0	grf_con_mcu_wicenreq Active HIGH request for deep sleep to be WIC-based deep sleep.
4	RW	0x1	grf_con_mcu_sleepholdreqn Request to extend the processor sleeping state regardless of wake-up events. If the processor acknowledges this request driving grf_mcu_sleepholdackn low, this guarantees the processor remains idle even on receipt of a wake-up event.
3	RW	0x0	grf_con_mcu_rxev A HIGH level on this input causes the architecture defined Event Register to be set in the Cortex-M0 processor. This causes a WFE instruction to complete. It also awakens the processor if it is sleeping as the result of encountering a WFE instruction when the Event Register is clear.
2	RW	0x0	grf_con_mcu_nmi Non-maskable interrupt. 1'b1: Assert 1'b0: De-assert
1	RW	0x0	grf_con_mcu_edbgrp External debug restart request. 1'b1: Assert 1'b0: De-assert
0	RW	0x0	grf_con_mcu_dbgrestart External debug restart request. 1'b1: Assert 1'b0: De-assert

GRF_SOC_CON38

Address: Operational Base(0xFF288000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x00	dmac0_intr_mask1 DMAC0 interrupt mask 1, each bit for one interrupt. 1'b0: Not masked 1'b1: Masked
7:6	RO	0x0	reserved
5:0	RW	0x00	dmac0_intr_mask0 DMAC0 interrupt mask 0, each bit for one interrupt. 1'b0: Not masked 1'b1: Masked

GRF_SOC_CON39

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Address: Operational Base(0xFF288000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	dmac1_intr_mask0 DMAC1 interrupt mask 0, each bit for one interrupt. 1'b0: Not masked 1'b1: Masked
7:6	RO	0x0	reserved
5:0	RW	0x00	dmac0_intr_mask2 DMAC0 interrupt mask 2, each bit for one interrupt. 1'b0: Not masked 1'b1: Masked

GRF_SOC_CON40

Address: Operational Base(0xFF288000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	dmac1_intr_mask2 DMAC1 interrupt mask 2, each bit for one interrupt. 1'b0: Not masked 1'b1: Masked
7:0	RW	0x00	dmac1_intr_mask1 DMAC1 interrupt mask 1, each bit for one interrupt. 1'b0: Not masked 1'b1: Masked

GRF_SOC_CON41

Address: Operational Base(0xFF288000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	grf_sai1_tx_dmac_sel 1'b0: DMAC1 channel 3 1'b1: DMAC0 channel 11
9	RW	0x0	grf_sai1_rx_dmac_sel 1'b0: DMAC1 channel 2 1'b1: DMAC0 channel 10
8	RW	0x0	grf_sai0_tx_dmac_sel 1'b0: DMAC1 channel 1 1'b1: DMAC0 channel 9
7	RW	0x0	grf_sai0_rx_dmac_sel 1'b0: DMAC1 channel 0 1'b1: DMAC0 channel 8
6	RW	0x0	grf_spdifrx_dmac_sel 1'b0: DMAC1 channel 11 1'b1: DMAC0 channel 7

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Bit	Attr	Reset Value	Description
5	RW	0x0	grf_spdiftx_dmac_sel 1'b0: DMAC1 channel 10 1'b1: DMAC0 channel 6
4	RW	0x0	grf_pdm_rx_dmac_sel 1'b0: DMAC1 channel 9 1'b1: DMAC0 channel 5
3	RW	0x0	grf_asrc1_tx_dmac_sel 1'b0: DMAC1 channel 19 1'b1: DMAC0 channel 3
2	RW	0x0	grf_asrc1_rx_dmac_sel 1'b0: DMAC1 channel 18 1'b1: DMAC0 channel 2
1	RW	0x0	grf_asrc0_tx_dmac_sel 1'b0: DMAC1 channel 17 1'b1: DMAC0 channel 1
0	RW	0x0	grf_asrc0_rx_dmac_sel 1'b0: DMAC1 channel 16 1'b1: DMAC0 channel 0

GRF_SOC_CON42

Address: Operational Base(0xFF288000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	dmac0_ch7_sel 2'b00: SPDIFRX 2'b01: UART1 RX Others: Reserved
13:12	RW	0x0	dmac0_ch6_sel 2'b00: SPDIFTX 2'b01: UART1 TX Others: Reserved
11:10	RW	0x0	dmac0_ch5_sel 2'b00: CAN1 RX 2'b01: UART0 RX 2'b10: PDM RX 2'b11: Reserved
9:8	RW	0x0	dmac0_ch4_sel 2'b00: CAN0 RX 2'b01: UART0 TX Others: Reserved
7:6	RW	0x0	dmac0_ch3_sel 2'b00: DSMC request 1 2'b01: SPI1 RX 2'b10: ASRC1 TX 2'b11: Reserved
5:4	RW	0x0	dmac0_ch2_sel 2'b00: DSMC request 0 2'b01: SPI1 TX 2'b10: ASRC1 RX 2'b11: Reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	dmac0_ch1_sel 2'b00: CAN1 RX 2'b01: SPI0 RX 2'b10: ASRC0 TX 2'b11: Reserved
1:0	RW	0x0	dmac0_ch0_sel 2'b00: CAN0 RX 2'b01: SPI0 TX 2'b10: ASRC0 RX 2'b11: Reserved

GRF_SOC_CON43

Address: Operational Base(0xFF288000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	dmac1_ch11_sel 2'b00: CAN1 RX 2'b01: SPDIFRX Others: Reserved
9:8	RW	0x0	dmac1_ch10_sel 2'b00: CAN0 RX 2'b01: SPDIFTX Others: Reserved
7:6	RW	0x0	dmac0_ch11_sel 2'b00: SAI1 TX 2'b01: UART3 RX Others: Reserved
5:4	RW	0x0	dmac0_ch10_sel 2'b00: DSMC REQ1 2'b01: UART3 TX 2'b10: SAI1 RX 2'b11: Reserved
3:2	RW	0x0	dmac0_ch9_sel 2'b00: SAI0 TX 2'b01: UART2 RX Others: Reserved
1:0	RW	0x0	dmac0_ch8_sel 2'b00: DSMC REQ0 2'b01: UART2 TX 2'b10: SAI0 RX 2'b11: Reserved

GRF_SOC_STATUS0

Address: Operational Base(0xFF288000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	vccio4_supply_voltage 1'b0: Less than 2.02V 1'b1: More than 2.19V

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Bit	Attr	Reset Value	Description
27	RW	0x0	vccio3_supply_voltage 1'b0: Less than 2.02V 1'b1: More than 2.19V
26	RW	0x0	vccio2_supply_voltage 1'b0: Less than 2.02V 1'b1: More than 2.19V
25	RW	0x0	vccio1_supply_voltage 1'b0: Less than 2.02V 1'b1: More than 2.19V
24	RW	0x0	crypto_idle 1'b0: CRYPTO not idle 1'b1: CRYPTO idle
23	RW	0x0	timer1_ch5_en_status TIMER1 channel 5 active status. 1'b0: Inactive 1'b1: Active
22	RW	0x0	timer1_ch4_en_status TIMER1 channel 4 active status. 1'b0: Inactive 1'b1: Active
21	RW	0x0	timer1_ch3_en_status TIMER1 channel 3 active status. 1'b0: Inactive 1'b1: Active
20	RW	0x0	timer1_ch2_en_status TIMER1 channel 2 active status. 1'b0: Inactive 1'b1: Active
19	RO	0x0	timer1_ch1_en_status TIMER1 channel 1 active status. 1'b0: Inactive 1'b1: Active
18	RO	0x0	timer1_ch0_en_status TIMER1 channel 0 active status. 1'b0: Inactive 1'b1: Active
17	RW	0x0	dfi_init_complete DFI initial complete.
16:15	RO	0x0	reserved
14:13	RW	0x0	grf_st_mac1_speed MAC Speed indication. 2'b10: 10Mbps 2'b11: 100Mbps Others: Reserved
12:11	RW	0x0	grf_st_mac0_speed MAC Speed indication. 2'b10: 10Mbps 2'b11: 100Mbps Others: Reserved
10	RO	0x0	timer0_ch5_en_status TIMER0 channel 5 active status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
9	RO	0x0	timer0_ch4_en_status TIMER0 channel 4 active status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	timer0_ch3_en_status TIMER0 channel 3 active status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	timer0_ch2_en_status TIMER0 channel 2 active status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	timer0_ch1_en_status TIMER0 channel 1 active status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	timer0_ch0_en_status TIMER0 channel 0 active status. 1'b0: Inactive 1'b1: Active
4	RW	0x0	vop_dsp_hold VOP DSP hold
3	RW	0x0	vop_dma_finish VOP DMA finish
2	RW	0x0	gpll_lock GPLL lock status
1	RW	0x0	v1pll_lock V1PLL lock status
0	RW	0x0	v0pll_lock V0PLL lock status

GRF_SOC_STATUS1

Address: Operational Base(0xFF288000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	biu_active_status BIU access active status, high active. [0]: mcu_to_core active [1]: bus_to_ddr active [2]: bus_to_hsperi active [3]: bus_to_lsperi active [4]: bus_to_vio active [5]: reserved [6]: vio_to_ddr active [7]: hsperi_to_bus active [8]: core_to_bus active [9]: core_to_ddr active [10]: core_to_corep active [11]: corep_to_core active

GRF_SOC_STATUS2

Address: Operational Base(0xFF288000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	grf_mcu_wicenack Active high acknowledge signal for grf_con_mcu_wicenreq.
8	RW	0x0	grf_mcu_sleepholdackn Response to grf_con_mcu_sleepholdreqn. If this signal is low, irrespective of the grf_mcu_sleeping signal value, the processor does not advance in execution and does not perform any memory operations.
7	RW	0x0	grf_mcu_sleepdeep Active only when MCU sleeping is high. Indicates that the sleepdeep bit in the NVIC is set to high and MCU is in deep sleep mode.
6	RW	0x0	grf_mcu_sleeping Indicates that MCU is in sleep mode. 1'b1: MCU is idle, waiting for an interrupt 1'b0: MCU isn't idle
5	RW	0x0	grf_mcu_wakeup Indicates MCU wakeup.
4	RW	0x0	grf_mcu_hclk_gate Indicates that HCLK can be gated because MCU is asleep without the debugger being active. 1'b1: MCU HCLK can be safely gated 1'b0: MCU HCLK can't be safely gated
3	RW	0x0	grf_mcu_lockup Indicates that MCU is locked up. 1'b1: MCU is locked up 1'b0: MCU isn't locked up
2	RW	0x0	grf_mcu_txev MCU TXEV
1	RW	0x0	grf_mcu_halt MCU halt
0	RO	0x0	grf_mcu_dbgrestarted Handshake of grf_con_mcu_dbgrestart.

GRF_DDR_STATUS0

Address: Operational Base(0xFF288000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RO	0x00	grf_st_wr_credit_cnt Value of wr_credit_cnt. It indicates the number of available write CAM slots.
15	RO	0x0	reserved
14:8	RO	0x00	grf_st_hpr_credit_cnt Value of hpr_credit_cnt. It Indicates the number of available High priority read CAM slots.
7	RO	0x0	reserved
6:0	RO	0x00	grf_st_lpr_credit_cnt Value of lpr_credit_cnt. It indicates the number of available Low priority read CAM slots.

GRF_DDR_STATUS1

Address: Operational Base(0xFF288000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	grf_st_stat_ddrc_reg_selfref_type Current self-refresh status and type. Equivalent to STAT.selfref_type register.
8	RW	0x0	cactive_axi1 State of AXI low-power clock active, cactive_axi
7	RW	0x0	csysack_axi1 State of AXI low-power request acknowledge, csysack_axi
6	RW	0x0	csysreq_axi1 State of AXI low-power request, csysreq_axi
5	RO	0x0	cactive_axi0 State of AXI low-power clock active, cactive_axi
4	RO	0x0	csysack_axi0 State of AXI low-power request acknowledge, csysack_axi
3	RO	0x0	csysreq_axi0 State of AXI low-power request, csysreq_axi
2	RO	0x0	cactive_ddrc State of DDRC hardware low-power clock active, cactive_ddrc
1	RO	0x0	csysack_ddrc State of DDRC hardware low-power request acknowledge, cactive_ddrc
0	RO	0x0	csysreq_ddrc State of DDRC hardware low-power request, csysreq_ddrc

GRF_USBPHY_STATUS

Address: Operational Base(0xFF288000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	usbotg1_phy_utmi_vpi USBPHY Single ended data received on USB2_OTG_DP in serial mode
25	RO	0x0	usbotg1_utmi_vmi USBPHY Single ended data received on USB2_OTG_DM in serial mode
24	RO	0x0	usbotg1_phy_ls_fs_rcv USBPHY receiver differential output in serial mode
23	RO	0x0	usbotg0_phy_utmi_vpi USBPHY Single ended data received on USB2_OTG_DP in serial mode
22	RO	0x0	usbotg0_utmi_vmi USBPHY Single ended data received on USB2_OTG_DM in serial mode
21	RO	0x0	usbotg0_phy_ls_fs_rcv USBPHY receiver differential output in serial mode
20	RO	0x0	usbphy_dp_attached usbphy_dp_attached status, high active.
19	RO	0x0	usbphy_cp_detected usbphy_cp_detected status, high active.
18	RO	0x0	usbphy_dcp_detected usbphy_dcp_detected status, high active.
17	RO	0x0	usbphy_dp_floatdet usbphy_dp_floatdet status, high active.
16	RO	0x0	usbphy_dm_floatdet usbphy_dm_floatdet status, high active.
15	RW	0x0	usbotg1_utmi_hostdisconnect usbhost_utmi_hostdisconnect status, high active.

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Bit	Attr	Reset Value	Description
14	RW	0x0	usbotg1_utmi_iddig usbhost_utmi_iddig status, high active.
13:12	RO	0x0	usbotg1_utmi_linestate usbotg_utmi_linestate status, high active.
11	RW	0x0	usbotg1_utmi_sessend usbhost_utmi_sessend status, high active.
10	RW	0x1	usbotg1_utmi_vbusvalid usbhost_utmi_vbusvalid status, high active.
9	RW	0x1	usbotg1_utmi_avalid usbhost_utmi_avalid status, high active.
8	RW	0x1	usbotg1_utmi_bvalid usbhost_utmi_bvalid status, high active.
7	RO	0x0	usbotg0_utmi_hostdisconnect usbotg_utmi_hostdisconnect status, high active.
6	RO	0x0	usbotg0_utmi_iddig usbotg_utmi_iddig status, high active.
5:4	RO	0x0	usbotg0_utmi_linestate usbotg_utmi_linestate status, high active.
3	RO	0x1	usbotg0_utmi_sessend usbotg_utmi_sessend status, high active.
2	RO	0x0	usbotg0_utmi_vbusvalid usbotg_utmi_vbusvalid status, high active.
1	RO	0x0	usbotg0_utmi_avalid usbotg_utmi_avalid status, high active.
0	RO	0x0	usbotg0_utmi_bvalid usbotg_utmi_bvalid status, high active.

GRF_USBOTG0_SIG_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	otg0_vbusvalid_fall_irq_en otg_vbusvalid falling edge IRQ enable. 1'b0: Disable 1'b1: Enable
8	RW	0x0	otg0_vbusvalid_rise_irq_en otg_vbusvalid rising edge IRQ enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	otg0_disconnect_fall_irq_en otg_disconnect falling edge IRQ enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	otg0_disconnect_rise_irq_en otg_disconnect rising edge IRQ enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	otg0_id_fall_irq_en otg_id falling edge IRQ enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	otg0_id_rise_irq_en otg_id rising edge IRQ enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	otg0_bvalid_fall_irq_en otg_bvalid falling edge IRQ enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	otg0_bvalid_rise_irq_en otg_bvalid rising edge IRQ enable. 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	otg0_linestate_irq_en otg_linestate change IRQ enable. 1'b0: Disable 1'b1: Enable

GRF_USBOTG0_SIG_DETECT_STATUS

Address: Operational Base(0xFF288000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	otg0_vbusvalid_fall_irq otg_vbusvalid falling edge IRQ status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	otg0_vbusvalid_rise_irq otg_vbusvalid rising edge IRQ status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	otg0_disconnect_fall_irq otg_disconnect falling edge IRQ status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	otg0_disconnect_rise_irq otg_disconnect rising edge IRQ status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	otg0_id_fall_irq otg_id falling edge IRQ status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	otg0_id_rise_irq otg_id rising edge IRQ status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	otg0_bvalid_fall_irq otg_bvalid falling edge IRQ status. 1'b0: Inactive 1'b1: Active
2	RO	0x0	otg0_bvalid_rise_irq otg_bvalid rising edge IRQ status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	otg0_linestate_irq otg_linestate change IRQ status. 1'b0: Inactive 1'b1: Active

GRF_USBOTG0_SIG_DETECT_CLR

Address: Operational Base(0xFF288000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	otg0_disconnect_fall_irq_clr otg_disconnect falling edge IRQ clear. Write 1 to clear IRQ status.
6	RW	0x0	otg0_disconnect_rise_irq_clr otg_disconnect rising edge IRQ clear. Write 1 to clear IRQ status.
5	RW	0x0	otg0_id_fall_irq_clr otg_id falling edge IRQ clear. Write 1 to clear IRQ status.
4	RW	0x0	otg0_id_rise_irq_clr otg_id rising edge IRQ clear. Write 1 to clear IRQ status.
3	RW	0x0	otg0_bvalid_fall_irq_clr otg_bvalid falling edge IRQ clear. Write 1 to clear IRQ status.
2	RW	0x0	otg0_bvalid_rise_irq_clr otg_bvalid rising edge IRQ clear. Write 1 to clear IRQ status.
1	RO	0x0	reserved
0	WO	0x0	otg0_linestate_irq_clr otg_linestate change IRQ clear. Write 1 to clear IRQ status.

GRF_USBOTG0_VBUSVALID_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	otg0_vbusvalid_detect_con OTG vbusvalid filter time control register

GRF_USBOTG0_LINESTATE_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	otg0_linestate_detect_con OTG linestate filter time control register

GRF_USBOTG0_DISCONNECT_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	otg0_disconnect_detect_con OTG disconnect filter time control register

GRF_USBOTG0_BVALID_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:0	RW	0x30100	otg0_bvalid_detect_con OTG bvalid filter time control register

GRF_USBOTG0_ID_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0030100	otg0_id_detect_con OTG id filter time control register

GRF_USBOTG1_SIG_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	otg1_vbusvalid_fall_irq_en otg_vbusvalid falling edge IRQ enable. 1'b0: Disable 1'b1: Enable
8	RW	0x0	otg1_vbusvalid_rise_irq_en otg_vbusvalid rising edge IRQ enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	otg1_disconnect_fall_irq_en otg_disconnect falling edge IRQ enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	otg1_disconnect_rise_irq_en otg_disconnect rising edge IRQ enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	otg1_id_fall_irq_en otg_id falling edge IRQ enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	otg1_id_rise_irq_en otg_id rising edge IRQ enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	otg1_bvalid_fall_irq_en otg_bvalid falling edge IRQ enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	otg1_bvalid_rise_irq_en otg_bvalid rising edge IRQ enable. 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	otg1_linestate_irq_en otg_linestate change IRQ enable. 1'b0: Disable 1'b1: Enable

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GRF_USBOTG1_SIG_DETECT_STATUS

Address: Operational Base(0xFF288000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	otg1_vbusvalid_fall_irq otg_vbusvalid falling edge IRQ status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	otg1_vbusvalid_rise_irq otg_vbusvalid rising edge IRQ status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	otg1_disconnect_fall_irq otg_disconnect falling edge IRQ status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	otg1_disconnect_rise_irq otg_disconnect rising edge IRQ status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	otg1_id_fall_irq otg_id falling edge IRQ status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	otg1_id_rise_irq otg_id rising edge IRQ status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	otg1_bvalid_fall_irq otg_bvalid falling edge IRQ status. 1'b0: Inactive 1'b1: Active
2	RO	0x0	otg1_bvalid_rise_irq otg_bvalid rising edge IRQ status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	reserved
0	RO	0x0	otg1_linestate_irq otg_linestate change IRQ status. 1'b0: Inactive 1'b1: Active

GRF_USBOTG1_SIG_DETECT_CLR

Address: Operational Base(0xFF288000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	otg1_disconnect_fall_irq_clr otg_disconnect falling edge IRQ clear. Write 1 to clear IRQ status.
6	RW	0x0	otg1_disconnect_rise_irq_clr otg_disconnect rising edge IRQ clear. Write 1 to clear IRQ status.

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Bit	Attr	Reset Value	Description
5	RW	0x0	otg1_id_fall_irq_clr otg_id falling edge IRQ clear. Write 1 to clear IRQ status.
4	RW	0x0	otg1_id_rise_irq_clr otg_id rising edge IRQ clear. Write 1 to clear IRQ status.
3	RW	0x0	otg1_bvalid_fall_irq_clr otg_bvalid falling edge IRQ clear. Write 1 to clear IRQ status.
2	RW	0x0	otg1_bvalid_rise_irq_clr otg_bvalid rising edge IRQ clear. Write 1 to clear IRQ status.
1	RO	0x0	reserved
0	WO	0x0	otg1_linestate_irq_clr otg_linestate change IRQ clear. Write 1 to clear IRQ status.

GRF_USBOTG1_VBUSVALID_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	otg1_vbusvalid_detect_con OTG vbusvalid filter time control register

GRF_USBOTG1_LINESTATE_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	otg1_linestate_detect_con OTG linestate filter time control register

GRF_USBOTG1_DISCONNECT_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	otg1_disconnect_detect_con OTG disconnect filter time control register

GRF_USBOTG1_BVALID_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	otg1_bvalid_detect_con OTG bvalid filter time control register

GRF_USBOTG1_ID_DETECT_CON

Address: Operational Base(0xFF288000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0030100	otg1_id_detect_con OTG id filter time control register

GRF_MAC0_MCGR_ACK

Address: Operational Base(0xFF288000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1T	0x0	mac0_mcgr_ack MAC0 media clock generation recovery ACK

GRF_MAC1_MCGR_ACK

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Address: Operational Base(0xFF288000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1T	0x0	mac1_mcgr_ack MAC1 media clock generation recovery ACK

GRF_OS_REG0

Address: Operational Base(0xFF288000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG1

Address: Operational Base(0xFF288000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG2

Address: Operational Base(0xFF288000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG3

Address: Operational Base(0xFF288000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG4

Address: Operational Base(0xFF288000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG5

Address: Operational Base(0xFF288000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG6

Address: Operational Base(0xFF288000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG7

Address: Operational Base(0xFF288000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG8

Address: Operational Base(0xFF288000) + offset (0x0220)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG9

Address: Operational Base(0xFF288000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG10

Address: Operational Base(0xFF288000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_OS_REG11

Address: Operational Base(0xFF288000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register

GRF_SOC_VERSION

Address: Operational Base(0xFF288000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:0	RW	0x00003506	soc_version

5.4 GRF_CORE Register Description

5.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_CORE_PVTPLL_CON0_L	0x0000	W	0x00000000	PVTPLL control register 0 low part
GRF_CORE_PVTPLL_CON0_H	0x0004	W	0x00000000	PVTPLL control register 0 high part
GRF_CORE_PVTPLL_CON1	0x0008	W	0x00000018	PVTPLL control register 1
GRF_CORE_PVTPLL_CON2	0x000C	W	0x00040000	PVTPLL control register 2
GRF_CORE_PVTPLL_CON3	0x0010	W	0x00000000	PVTPLL control register 3
GRF_CORE_PVTPLL_OSC_CNT	0x0014	W	0x00000000	PVTPLL OSC counter register
GRF_CORE_PVTPLL_OSC_CNT_AVG	0x0018	W	0x00000000	PVTPLL OSC counter average register
GRF_CORE_CPU_STATUS	0x0060	W	0x00000000	CPU status register
GRF_CORE_CPU_CON0	0x0064	W	0x0000000F	CPU control register 0
GRF_CORE_CPU_CON1	0x0068	W	0x00000060	CPU control register 1
GRF_CORE_CPU_MEM_CON0	0x006C	W	0x00000001	CPU memory control register 0
GRF_CORE_SOC_CON0	0x0084	W	0x00000000	System control register 0
GRF_CORE_SOC_CON1	0x0088	W	0x00000000	System control register 1
GRF_CORE_SOC_CON2	0x008C	W	0x00000000	System control register 2
GRF_CORE_SOC_CON3	0x0090	W	0x00000000	System control register 3
GRF_CORE_SOC_CON4	0x0094	W	0x00000000	System control register 4

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Name	Offset	Size	Reset Value	Description
GRF_CORE_SOC_CON5	0x0098	W	0x00000000	System control register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.4.2 Detail Registers Description

GRF_CORE_PVTPLL_CON0_L

Address: Operational Base(0xFF840000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass 1'b1: Not support glitch-free frequency switch 1'b0: Support glitch-free frequency switch
14:13	RW	0x0	clk_div_osc Frequency divsion factor for osc_clk
12:11	RW	0x0	clk_div_ref Frequency divsion factor for ref_clk
10:8	RW	0x0	osc_ring_sel Osc ring channel select
7:3	RO	0x00	reserved
2	RW	0x0	out_polar 1'b0: Need to increase when out = 1 1'b1: Need to increase when out = 0
1	RW	0x0	osc_en 1'b1: Osc_ring enable 1'b0: Osc_ring disable
0	RW	0x0	start 1'b1: PVTPLL monitor start 1'b0: PVTPLL monitor doesn't start

GRF_CORE_PVTPLL_CON0_H

Address: Operational Base(0xFF840000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RW	0x00	clk_div_out_logic Frequency division factor for output clock for system logic.
10	RW	0x0	clk_out_sel Clock output selection 1'b0: OSC ring clock without frequency divider 1'b1: OSC ring clock with frequency divider
9:7	RW	0x0	clk_div_out Frequency division factor for output clock.
6:0	RW	0x00	ring_length_sel Osc ring inverter length select

GRF_CORE_PVTPLL_CON1

Address: Operational Base(0xFF840000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000018	cal_cnt Frequency measurement period

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GRF_CORE_PVTPLL_CON2

Address: Operational Base(0xFF840000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	ckg_val Clock gating interval control count value
15:0	RW	0x0000	threshold Count difference threshold value

GRF_CORE_PVTPLL_CON3

Address: Operational Base(0xFF840000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ref_cnt Target reference frequency value

GRF_CORE_PVTPLL_OSC_CNT

Address: Operational Base(0xFF840000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	osc_clk_cnt_val Osc_clk counter value

GRF_CORE_PVTPLL_OSC_CNT_AVG

Address: Operational Base(0xFF840000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	osc_clk_cnt_ave_value Osc_clk counter average value

GRF_CORE_CPU_STATUS

Address: Operational Base(0xFF840000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	jtagnsw High if JTAG selected, low if SWD selected SWJ-DP
14	RW	0x0	jtagtop Indicates TAP in TLR, RTI, Sel-DR or Sel-IR states for SWJ-DP
13	RW	0x0	evento_rising_edge Indicates an event output
12	RW	0x0	standbywfil2 L2 memory system is in wfi state.
11	RO	0x0	reserved
10:8	RW	0x0	smpnamp It signals SMP mode or AMP mode for core.
7	RO	0x0	reserved
6:4	RW	0x0	standbywfi Core is in WFI state.
3	RO	0x0	reserved
2:0	RW	0x0	standbywfe Core is in WFE state.

GRF_CORE_CPU_CON0

Address: Operational Base(0xFF840000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	evento_clr Clear the event output status to 1'b0
12	RW	0x0	eventi Event input for processor wake-up from WFE state.
11:8	RW	0x0	cfgte Controls process state for exception handling (TE bit) at reset 1'b1: Thumb instruction set for exception handling 1'b0: ARM instruction set for exception handling
7:4	RW	0x0	cfgend Controls endianness during dta exception handling (EE-bit) at reset 1'b1: Big-endian data during exception handling 1'b0: Little-endian data during exception handling
3:0	RW	0xf	vinithi Sets the base address of the vector table 1'b1: A vector table base address of 0xFFFF0000 1'b0: A vector table base address of 0x00000000

GRF_CORE_CPU_CON1

Address: Operational Base(0xFF840000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	pvtpll_oen_to_io_sel PVTPLL enable to IO selection 1'b0: Control by PVTPLL 1'b1: Always enable
12	RW	0x0	cpu_ema_detect_en 1'b0: ema detect disable 1'b1: ema detect enable
11:7	RO	0x00	reserved
6	RW	0x1	dbgselfaddrv Debug self-address offset valid
5	RW	0x1	dbgromaddrv Debug ROM physical address valid
4	RW	0x0	l2rstdisable Disable automatic L2 cache invalidate at reset
3:0	RW	0x0	l1rstdisable Disable automatic data cache, instruction cache and TLB invalidate at reset

GRF_CORE_CPU_MEM_CON0

Address: Operational Base(0xFF840000) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	wtsel_hvt_mux4 Timing adjustment setting for debug purpose
9:8	RW	0x0	rtsel_hvt_mux4 Timing adjustment setting for debug purpose
7:4	RO	0x0	reserved
3:2	RW	0x0	wtsel Timing adjustment setting for debug purpose
1:0	RW	0x1	rtsel Timing adjustment setting for debug purpose

GRF_CORE_SOC_CON0

Address: Operational Base(0xFF840000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
14:10	RW	0x00	grf_gpio1_filter_sel1 GPIO select to go through second filter logic 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: GPIO1C0 5'h11: GPIO1C1 5'h12: GPIO1C2 5'h13: GPIO1C3 5'h14: GPIO1C4 5'h15: GPIO1C5 5'h16: GPIO1C6 5'h17: GPIO1C7 5'h18: GPIO1D0 5'h19: GPIO1D1 5'h1a: GPIO1D2 5'h1b: GPIO1D3
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio1_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: GPIO1C0 5'h11: GPIO1C1 5'h12: GPIO1C2 5'h13: GPIO1C3 5'h14: GPIO1C4 5'h15: GPIO1C5 5'h16: GPIO1C6 5'h17: GPIO1C7 5'h18: GPIO1D0 5'h19: GPIO1D1 5'h1a: GPIO1D2 5'h1b: GPIO1D3
3:0	RW	0x0	grf_gpio1_filter_en There are four filter circuits for pad in GPIO1, each bit controls the enable of one filter.

GRF_CORE_SOC_CON1

Address: Operational Base(0xFF840000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio1_filter_sel3 GPIO select to go through fouth filter logic 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: GPIO1C0 5'h11: GPIO1C1 5'h12: GPIO1C2 5'h13: GPIO1C3 5'h14: GPIO1C4 5'h15: GPIO1C5 5'h16: GPIO1C6 5'h17: GPIO1C7 5'h18: GPIO1D0 5'h19: GPIO1D1 5'h1a: GPIO1D2 5'h1b: GPIO1D3
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio1_filter_sel2 GPIO select to go through third filter logic 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: GPIO1C0 5'h11: GPIO1C1 5'h12: GPIO1C2 5'h13: GPIO1C3 5'h14: GPIO1C4 5'h15: GPIO1C5 5'h16: GPIO1C6 5'h17: GPIO1C7 5'h18: GPIO1D0 5'h19: GPIO1D1 5'h1a: GPIO1D2 5'h1b: GPIO1D3
3:0	RO	0x0	reserved

GRF_CORE_SOC_CON2

Address: Operational Base(0xFF840000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_CORE_SOC_CON3

Address: Operational Base(0xFF840000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_CORE_SOC_CON4

Address: Operational Base(0xFF840000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

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GRF_CORE_SOC_CON5

Address: Operational Base(0xFF840000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_filter_count3 Filter counter for fouth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

5.5 GRF_PMU Register Description

5.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_PMU_SOC_CON0	0x0000	W	0x00000001	PMU System control register 0
GRF_PMU_SOC_CON1	0x0004	W	0x00000000	PMU System control register 1
GRF_PMU_SOC_CON2	0x0008	W	0x000007EF	PMU System control register 2
GRF_PMU_SOC_CON3	0x000C	W	0x00000000	PMU System control register 3
GRF_PMU_SOC_CON4	0x0010	W	0x00000000	PMU System control register 4
GRF_PMU_SOC_CON5	0x0014	W	0x00000000	PMU System control register 5
GRF_PMU_SOC_CON6	0x0018	W	0x00000000	PMU System control register 6
GRF_PMU_SOC_CON7	0x001C	W	0x00000000	PMU System control register 7
GRF_PMU_SOC_CON8	0x0020	W	0x00000000	PMU System control register 8
GRF_PMU_SOC_CON9	0x0024	W	0x00000000	PMU System control register 9
GRF_PMU_SOC_CON10	0x0028	W	0x00000000	PMU System control register 10
GRF_PMU_SOC_CON11	0x002C	W	0x00000000	PMU System control register 11
GRF_PMU_SOC_CON12	0x0030	W	0x00000000	PMU System control register 12
GRF_PMU_SOC_CON13	0x0034	W	0x00000000	PMU System control register 13
GRF_PMU_SOC_CON14	0x0038	W	0x00000000	PMU System control register 14
GRF_PMU_SOC_CON15	0x003C	W	0x00000000	PMU System control register 15
GRF_PMU_SOC_CON16	0x0040	W	0x00000000	PMU System control register 16
GRF_PMU_SOC_CON17	0x0044	W	0x00000000	PMU System control register 17
GRF_PMU_SOC_CON18	0x0048	W	0x00000000	PMU System control register 18
GRF_PMU_SOC_STATUS	0x0100	W	0x00000001	PMU System status register
GRF_PMU_OS_REG0	0x0200	W	0x00000000	OS register 0
GRF_PMU_OS_REG1	0x0204	W	0x00000000	OS register 1
GRF_PMU_OS_REG2	0x0208	W	0x00000000	OS register 2
GRF_PMU_OS_REG3	0x020C	W	0x00000000	OS register 3
GRF_PMU_OS_REG4	0x0210	W	0x00000000	OS register 4
GRF_PMU_OS_REG5	0x0214	W	0x00000000	OS register 5
GRF_PMU_OS_REG6	0x0218	W	0x00000000	OS register 6
GRF_PMU_OS_REG7	0x021C	W	0x00000000	OS register 7
GRF_PMU_OS_REG8	0x0220	W	0x00000000	OS register 9
GRF_PMU_OS_REG9	0x0224	W	0x00000000	OS register 9
GRF_PMU_OS_REG10	0x0228	W	0x00000000	OS register 10
GRF_PMU_OS_REG11	0x022C	W	0x00000000	OS register 11
GRF_PMU_RSTFUNC_STATUS	0x0230	W	0x00000000	System reset status register
GRF_PMU_RSTFUNC_CLR	0x0234	W	0x00000000	System reset status clear register
GRF_PMU_MCU_ISO_CON0	0x1000	W	0x00000000	MCU isolation control register 0
GRF_PMU_MCU_ISO_CON1	0x1004	W	0x00000000	MCU isolation control register 1

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Name	Offset	Size	Reset Value	Description
GRF_PMU_MCU_ISO_CON2	0x1008	W	0x00000000	MCU isolation control register 2
GRF_PMU_MCU_ISO_CON3	0x100C	W	0x00000000	MCU isolation control register 3
GRF_PMU_MCU_ISO_CON4	0x1010	W	0x00000000	MCU isolation control register 4
GRF_PMU_MCU_ISO_CON5	0x1014	W	0x00000000	MCU isolation control register 5
GRF_PMU_MCU_ISO_CON6	0x1018	W	0x00000000	MCU isolation control register 6
GRF_PMU_MCU_ISO_CON7	0x101C	W	0x00000000	MCU isolation control register 7
GRF_PMU_MCU_ISO_CON8	0x1020	W	0x00000100	MCU isolation control register 8
GRF_PMU_MCU_ISO_CON9	0x1024	W	0x00000000	MCU isolation control register 9
GRF_PMU_MCU_ISO_CON10	0x1028	W	0x00000000	MCU isolation control register 10
GRF_PMU_MCU_ISO_CON11	0x102C	W	0x00000000	MCU isolation control register 11
GRF_PMU_MCU_ISO_DDR_CON0	0x1400	W	0x00000000	MCU isolation DDR control register 0
GRF_PMU_MCU_ISO_DDR_CON1	0x1404	W	0x00000000	MCU isolation DDR control register 1
GRF_PMU_MCU_ISO_LOCK	0x1500	W	0x00000000	Secure system control register 0
GRF_PMU_CPU_ISO_CON0	0x2000	W	0x00000000	CPU isolation control register 0
GRF_PMU_CPU_ISO_CON1	0x2004	W	0x00000000	CPU isolation control register 1
GRF_PMU_CPU_ISO_CON2	0x2008	W	0x00000000	CPU isolation control register 2
GRF_PMU_CPU_ISO_CON3	0x200C	W	0x00000000	CPU isolation control register 3
GRF_PMU_CPU_ISO_CON4	0x2010	W	0x00000000	CPU isolation control register 4
GRF_PMU_CPU_ISO_CON5	0x2014	W	0x00000000	CPU isolation control register 5
GRF_PMU_CPU_ISO_CON6	0x2018	W	0x00000000	CPU isolation control register 6
GRF_PMU_CPU_ISO_CON7	0x201C	W	0x00000000	CPU isolation control register 7
GRF_PMU_CPU_ISO_CON8	0x2020	W	0x00000200	CPU isolation control register 8
GRF_PMU_CPU_ISO_CON9	0x2024	W	0x00000000	CPU isolation control register 9
GRF_PMU_CPU_ISO_CON10	0x2028	W	0x00000000	CPU isolation control register 10
GRF_PMU_CPU_ISO_CON11	0x202C	W	0x00000000	CPU isolation control register 11
GRF_PMU_CPU_ISO_DDR_CON0	0x2400	W	0x00000000	CPU isolation DDR control register 0
GRF_PMU_CPU_ISO_DDR_CON1	0x2404	W	0x00000000	CPU isolation DDR control register 1

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Name	Offset	Size	Reset Value	Description
GRF_PMU_CPU_ISO_LOCK	0x2500	W	0x00000000	Secure system control register 0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.5.2 Detail Registers Description

GRF_PMU_SOC_CON0

Address: Operational Base(0xFF910000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	ddrphy_addrcmd_hz 1'b0: Disable DDRPHY io high-z 1'b1: Enable DDRPHY io high-z
11	RW	0x0	ddrphy_addrcmd_hz_sel DDRPHY IO state selection. 1'b0: addrcmd_hz comes from PMU 1'b1: addrcmd_hz comes from ddrphy_addrcmd_hz
10	RO	0x0	reserved
9	RW	0x0	ddrphy_io_ret 1'b0: Disable DDRPHY IO retention 1'b1: Enable DDRPHY IO retention
8	RW	0x0	ddrphy_io_ret_sel DDRPHY IO retention control selection. 1'b0: Retention control from PMU 1'b1: Retention control from ddrphy_io_ret
7:2	RO	0x00	reserved
1	RW	0x0	force_jtag_uart0_rxm0 force JTAG select enable when UART0 select and RX keep low a few times 1'b0: Disable 1'b1: Enable
0	RW	0x1	mem_auto_gating_en Enable memory auto gating 1'b0: Disable 1'b1: Enable

GRF_PMU_SOC_CON1

Address: Operational Base(0xFF910000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	rmio_test_mode RMIO test mode enable
10	RW	0x0	clk_32k_oen clk_32k output enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
9	RW	0x0	sai1_mclk_oen sai1_mclk output enable 1'b0: Disable 1'b1: Enable
8	RW	0x0	sai0_mclk_oen sai0_mclk output enable 1'b0: Disable 1'b1: Enable
7:4	RO	0x0	reserved
3	RW	0x0	pmic_core_sleep_pol pmic_core_sleep polarity. This bit can only reset by nPOR. 1'b0: not invert pmic_core_sleep 1'b1: invert pmic_core_sleep
2	RW	0x0	pmic_core_sleep_sel pmic_core_sleep polarity. This bit can only reset by nPOR. 1'b0: nPOR_out2chip_rst, from reset pulse generator. 1'b1: pmu_sleep, from PMU block.
1	RW	0x0	pmic_logic_sleep_pol pmic_logic_sleep polarity. This bit can only reset by nPOR. 1'b0: not invert pmic_logic_sleep 1'b1: invert pmic_logic_sleep
0	RW	0x0	pmic_logic_sleep_sel PMIC_LOGIC_SLEEP source selection. This bit can only reset by nPOR. 1'b0: nPOR_out2chip_rst, from reset pulse generator. 1'b1: pmu_sleep, from PMU block.

GRF_PMU_SOC_CON2

Address: Operational Base(0xFF910000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x07ef	out2chip_rst_init out2chip_rst width configuration. This bit can only reset by nPOR.

GRF_PMU_SOC_CON3

Address: Operational Base(0xFF910000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	resetn_pmu_touch_key_hold_ena Hold resetn_touch_key. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable
8	RW	0x0	resetn_pmu_gpio1_shadow_hold_ena Hold dbresetn_pmu_gpio0. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
7	RW	0x0	presetn_pmu_pwm0_hold_ena Hold presetn_pmu_pwm0. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable
6	RO	0x0	reserved
5	RW	0x0	presetn_pmu_sgrf_hold_ena Hold presetn_pmu_sgrf. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable
4	RW	0x0	presetn_gpio0_ioc_hold_ena Hold presetn_gpio0_ioc. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable
3	RW	0x0	presetn_pmu_grf_hold_ena Hold presetn_pmu_grf. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable
2	RW	0x0	resetn_pmu_gpio0_hold_ena Hold dbresetn_pmu_gpio0. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable
1	RW	0x0	presetn_pmu_cru_hold_ena Hold presetn_pmu_cru. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable
0	RW	0x0	presetn_pmu_hptimer_hold_ena Hold presetn_pmu_hptimer. When enabled, the relative logic cannot be reset. 1'b0: Disable 1'b1: Enable

GRF_PMU_SOC_CON4

Address: Operational Base(0xFF910000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	uart_jtag_dly_cnt force jtag uart keep low counter

GRF_PMU_SOC_CON5

Address: Operational Base(0xFF910000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio0_filter_sel1 GPIO select to go through second filter logic 5'h00: GPIO0A0 5'h01: GPIO0A1 5'h02: GPIO0A2 5'h03: GPIO0A3 5'h04: GPIO0A4 5'h05: GPIO0A5 5'h06: GPIO0A6 5'h07: GPIO0A7 5'h08: GPIO0B0 5'h09: GPIO0B1 5'h0a: GPIO0B2 5'h0b: GPIO0B3 5'h0c: GPIO0B4 5'h0d: GPIO0B5 5'h0e: GPIO0B6 5'h0f: GPIO0B7 5'h10: GPIO0C0 5'h11: GPIO0C1 5'h12: GPIO0C2 5'h13: GPIO0C3 5'h14: GPIO0C4 5'h15: GPIO0C5 5'h16: GPIO0C6 5'h17: GPIO0C7 5'h18: GPIO0D0
9	RO	0x0	reserved
8:4	RW	0x00	grf_gpio0_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIO0A0 5'h01: GPIO0A1 5'h02: GPIO0A2 5'h03: GPIO0A3 5'h04: GPIO0A4 5'h05: GPIO0A5 5'h06: GPIO0A6 5'h07: GPIO0A7 5'h08: GPIO0B0 5'h09: GPIO0B1 5'h0a: GPIO0B2 5'h0b: GPIO0B3 5'h0c: GPIO0B4 5'h0d: GPIO0B5 5'h0e: GPIO0B6 5'h0f: GPIO0B7 5'h10: GPIO0C0 5'h11: GPIO0C1 5'h12: GPIO0C2 5'h13: GPIO0C3 5'h14: GPIO0C4 5'h15: GPIO0C5 5'h16: GPIO0C6 5'h17: GPIO0C7 5'h18: GPIO0D0

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	grf_gpio0_filter_en There are four filter circuits for pad in GPIO0, each bit controls the enable of one filter.

GRF_PMU_SOC_CON6

Address: Operational Base(0xFF910000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
14:10	RW	0x00	grf_gpio0_filter_sel3 GPIO filter select to go through fouth filter logic 5'h00: GPIO0A0 5'h01: GPIO0A1 5'h02: GPIO0A2 5'h03: GPIO0A3 5'h04: GPIO0A4 5'h05: GPIO0A5 5'h06: GPIO0A6 5'h07: GPIO0A7 5'h08: GPIO0B0 5'h09: GPIO0B1 5'h0a: GPIO0B2 5'h0b: GPIO0B3 5'h0c: GPIO0B4 5'h0d: GPIO0B5 5'h0e: GPIO0B6 5'h0f: GPIO0B7 5'h10: GPIO0C0 5'h11: GPIO0C1 5'h12: GPIO0C2 5'h13: GPIO0C3 5'h14: GPIO0C4 5'h15: GPIO0C5 5'h16: GPIO0C6 5'h17: GPIO0C7 5'h18: GPIO0D0
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio0_filter_sel2 GPIO filter select to go through third filter logic 5'h00: GPIO0A0 5'h01: GPIO0A1 5'h02: GPIO0A2 5'h03: GPIO0A3 5'h04: GPIO0A4 5'h05: GPIO0A5 5'h06: GPIO0A6 5'h07: GPIO0A7 5'h08: GPIO0B0 5'h09: GPIO0B1 5'h0a: GPIO0B2 5'h0b: GPIO0B3 5'h0c: GPIO0B4 5'h0d: GPIO0B5 5'h0e: GPIO0B6 5'h0f: GPIO0B7 5'h10: GPIO0C0 5'h11: GPIO0C1 5'h12: GPIO0C2 5'h13: GPIO0C3 5'h14: GPIO0C4 5'h15: GPIO0C5 5'h16: GPIO0C6 5'h17: GPIO0C7 5'h18: GPIO0D0
3:0	RO	0x0	reserved

GRF_PMU_SOC_CON7

Address: Operational Base(0xFF910000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio0_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_PMU_SOC_CON8

Address: Operational Base(0xFF910000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio0_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_PMU_SOC_CON9

Address: Operational Base(0xFF910000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio0_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_PMU_SOC_CON10

Address: Operational Base(0xFF910000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio0_filter_count3 Filter counter for fouth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_PMU_SOC_CON11

Address: Operational Base(0xFF910000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
14:10	RW	0x00	grf_gpio1_shadow_filter_sel1 GPIO select to go through second filter logic 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: GPIO1C0 5'h11: GPIO1C1 5'h12: GPIO1C2 5'h13: GPIO1C3 5'h14: GPIO1C4 5'h15: GPIO1C5 5'h16: GPIO1C6 5'h17: GPIO1C7 5'h18: GPIO1D0 5'h19: GPIO1D1 5'h1a: GPIO1D2 5'h1b: GPIO1D3
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio1_shadow_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: GPIO1C0 5'h11: GPIO1C1 5'h12: GPIO1C2 5'h13: GPIO1C3 5'h14: GPIO1C4 5'h15: GPIO1C5 5'h16: GPIO1C6 5'h17: GPIO1C7 5'h18: GPIO1D0 5'h19: GPIO1D1 5'h1a: GPIO1D2 5'h1b: GPIO1D3
3:0	RW	0x0	grf_gpio1_shadow_filter_en There are four filter circuits for pad in GPIO1_SHADOW, each bit controls the enable of one filter.

GRF_PMU_SOC_CON12

Address: Operational Base(0xFF910000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio1_shadow_filter_sel3 GPIO select to go through fourth filter logic 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: GPIO1C0 5'h11: GPIO1C1 5'h12: GPIO1C2 5'h13: GPIO1C3 5'h14: GPIO1C4 5'h15: GPIO1C5 5'h16: GPIO1C6 5'h17: GPIO1C7 5'h18: GPIO1D0 5'h19: GPIO1D1 5'h1a: GPIO1D2 5'h1b: GPIO1D3
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio1_shadow_filter_sel2 GPIO select to go through third filter logic 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: GPIO1C0 5'h11: GPIO1C1 5'h12: GPIO1C2 5'h13: GPIO1C3 5'h14: GPIO1C4 5'h15: GPIO1C5 5'h16: GPIO1C6 5'h17: GPIO1C7 5'h18: GPIO1D0 5'h19: GPIO1D1 5'h1a: GPIO1D2 5'h1b: GPIO1D3
3:0	RO	0x0	reserved

GRF_PMU_SOC_CON13

Address: Operational Base(0xFF910000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_shadow_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_PMU_SOC_CON14

Address: Operational Base(0xFF910000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_shadow_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_PMU_SOC_CON15

Address: Operational Base(0xFF910000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_shadow_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

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GRF_PMU_SOC_CON16

Address: Operational Base(0xFF910000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_shadow_filter_count3 Filter counter for fourth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GRF_PMU_SOC_CON17

Address: Operational Base(0xFF910000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio1_shadow_enable_low GPIO1_SHADOW enable for GPIO1A0~APIO1B7, each bit for one GPIO.

GRF_PMU_SOC_CON18

Address: Operational Base(0xFF910000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x000	gpio1_shadow_enable_high GPIO1_SHADOW enable for GPIO1C0~APIO1D3, each bit for one GPIO.

GRF_PMU_SOC_STATUS

Address: Operational Base(0xFF910000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	npor_powergood NPOR power state. 1'b0: Power bad state 1'b1: Power good state

GRF_PMU_OS_REG0

Address: Operational Base(0xFF910000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, with reset pin. it's bit0~31 can use to control the signal 0~31 of IO array when io_array_test_mode is asserted.

GRF_PMU_OS_REG1

Address: Operational Base(0xFF910000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, with reset pin. it's bit0~31 can use to control the signal 32~65 of IO array when io_array_test_mode is asserted.

GRF_PMU_OS_REG2

Address: Operational Base(0xFF910000) + offset (0x0208)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, with reset pin. it's bit0~31 can use to control the signal 64~95 of IO array when io_array_test_mode is asserted.

GRF_PMU_OS_REG3

Address: Operational Base(0xFF910000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, with reset pin. it's bit0~1 can use to control the signal 96~97 of IO array when io_array_test_mode is asserted.

GRF_PMU_OS_REG4

Address: Operational Base(0xFF910000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, with reset pin. it's bit0~31 can use to control the signal output enable 0~31 of IO array when io_array_test_mode is asserted.

GRF_PMU_OS_REG5

Address: Operational Base(0xFF910000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, with reset pin. it's bit0~31 can use to control the signal output enable 32~65 of IO array when io_array_test_mode is asserted.

GRF_PMU_OS_REG6

Address: Operational Base(0xFF910000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, with reset pin. it's bit0~31 can use to control the signal output enable 64~95 of IO array when io_array_test_mode is asserted.

GRF_PMU_OS_REG7

Address: Operational Base(0xFF910000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, with reset pin. it's bit0~1 can use to control the signal output enable 96~97 of IO array when io_array_test_mode is asserted.

GRF_PMU_OS_REG8

Address: Operational Base(0xFF910000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, without reset pin

GRF_PMU_OS_REG9

Address: Operational Base(0xFF910000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, without reset pin

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GRF_PMU_OS_REG10

Address: Operational Base(0xFF910000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, without reset pin

GRF_PMU_OS_REG11

Address: Operational Base(0xFF910000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg OS register, without reset pin

GRF_PMU_RSTFUNC_STATUS

Address: Operational Base(0xFF910000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	tsadc_shut_reset_src_stat Reset state. When high, reset by TSADC shut trigger. After power on, user should clear the status once by write 1'b1 to tsadc_shut_reset_src_clr.
1	RO	0x0	wdt_reset_src_stat Reset state. When high, reset by WDT trigger. After power on, user should clear the status once by write 1'b1 to wdt_reset_src_clr.
0	RO	0x0	first_reset_src_stat Reset state. When high, reset by first reset trigger. After power on, user should clear the status once by write 1'b1 to first_reset_src_clr.

GRF_PMU_RSTFUNC_CLR

Address: Operational Base(0xFF910000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	tsadc_shut_reset_src_clr Clear bit for reset by tsadc shut trigger. 1'b1: Clear enable 1'b0: Clear disable
1	WO	0x0	wdt_reset_src_clr Clear bit for reset by wdt trigger. 1'b1: Clear enable 1'b0: Clear disable
0	WO	0x0	first_reset_src_clr Clear bit for reset by first reset trigger. 1'b1: Clear enable 1'b0: Clear disable

GRF_PMU_MCU_ISO_CON0

Address: Operational Base(0xFF910000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	dsmc_mem_iso_ctrl DSMC_MEM control bit. There are 1024MB address space for DSMC_MEM, it is separated into four 256MB space. dsmc_mem_iso_ctrl[0], first 256MB dsmc_mem_iso_ctrl[1], second 256MB dsmc_mem_iso_ctrl[2], third 256MB dsmc_mem_iso_ctrl[3], fourth 256MB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
11	RW	0x0	dsmc_iso_ctrl DSMC isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
10	RO	0x0	reserved
9	RW	0x0	flexbus_iso_ctrl FLEXBUS isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
8:5	RW	0x0	gpio1_iso_ctrl GPIO1 isolation control bit. There are 16KB address space for GPIO1, it is separated into four 4KB space. gpio1_iso_ctrl[0], first 4KB gpio1_iso_ctrl[1], second 4KB gpio1_iso_ctrl[2], third 4KB gpio1_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
4:1	RW	0x0	grf_core_iso_ctrl GRF_CORE slave isolation control bit. There are 16KB address space for GRF_CORE, it is separated into four 4KB space. grf_core_iso_ctrl[0], first 4KB grf_core_iso_ctrl[1], second 4KB grf_core_iso_ctrl[2], third 4KB grf_core_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
0	RW	0x0	a7dbg_iso_ctrl A7 debug isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON1

Address: Operational Base(0xFF910000) + offset (0x1004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	mailbox_iso_ctrl MAILBOX slave isolation control bit, There are 16KB address space for MAILBOX, it is separated into four 4KB space. mailbox_iso_ctrl[0], first 4KB mailbox_iso_ctrl[1], second 4KB mailbox_iso_ctrl[2], third 4KB mailbox_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
11:8	RW	0x0	grf_bus_iso_ctrl GRF_BUS slave isolation control bit. There are 16KB address space for GRF_BUS, it is separated into four 4KB space. grf_bus_iso_ctrl[0], first 4KB grf_bus_iso_ctrl[1], second 4KB grf_bus_iso_ctrl[2], third 4KB grf_bus_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
7	RW	0x0	ddr_lpc_iso_ctrl DDR LPC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
6	RW	0x0	ddr_monitor_iso_ctrl DDR monitor slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
5	RW	0x0	ddrc_iso_ctrl DDR controller slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
4	RW	0x0	dmac1_iso_ctrl DMAC1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
3	RW	0x0	dmac0_iso_ctrl DMAC0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
2	RW	0x0	sgrf_bus_iso_ctrl SGRF_BUS isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
1	RW	0x0	secure_dmac1_iso_ctrl DMAC1 secure only slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
0	RW	0x0	secure_dmac0_iso_ctrl DMAC0 secure only slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON2

Address: Operational Base(0xFF910000) + offset (0x1008)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	timer1_iso_ctrl TIMER1 slave isolation control bit. There are 32KB address space for TIMER1, it is separated into eight 4KB space. timer1_iso_ctrl[0], first 4KB timer1_iso_ctrl[1], second 4KB timer1_iso_ctrl[2], third 4KB timer1_iso_ctrl[3], fourth 4KB timer1_iso_ctrl[4], fifth 4KB timer1_iso_ctrl[5], sixth 4KB timer1_iso_ctrl[6], seventh 4KB timer1_iso_ctrl[7], eighth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
7:0	RW	0x00	timer0_iso_ctrl TIMER0 slave isolation control bit. There are 32KB address space for TIMER0, it is separated into eight 4KB space. timer0_iso_ctrl[0], first 4KB timer0_iso_ctrl[1], second 4KB timer0_iso_ctrl[2], third 4KB timer0_iso_ctrl[3], fourth 4KB timer0_iso_ctrl[4], fifth 4KB timer0_iso_ctrl[5], sixth 4KB timer0_iso_ctrl[6], seventh 4KB timer0_iso_ctrl[7], eighth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON3

Address: Operational Base(0xFF910000) + offset (0x100C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	dma2ddr_iso_ctrl DMA2DDR slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
13	RW	0x0	secure_trng_iso_ctrl Secure RNG slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
12	RW	0x0	secure_keyladder_iso_ctrl Secure keyladder slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
11	RW	0x0	secure_crypto_iso_ctrl Secure CRYPTO slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

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Bit	Attr	Reset Value	Description
10	RW	0x0	bootrom_iso_ctrl BOOTROM slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
9	RW	0x0	ddrphy_iso_ctrl DDRPHY slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
8	RW	0x0	usb2otg1_iso_ctrl USB2.0_OTG1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
7	RW	0x0	usb2otg0_iso_ctrl USB2.0_OTG0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
6	RW	0x0	ns_trng_iso_ctrl RNG non-secure slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
5	RW	0x0	ns_crypto_iso_ctrl Crypto non-secure slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
4	RW	0x0	usbphy_iso_ctrl USBPHY slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
3	RW	0x0	intmux_iso_ctrl INTMUX slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
2	RO	0x0	reserved
1	RW	0x0	wdt1_iso_ctrl WDT1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
0	RW	0x0	wdt0_iso_ctrl WDT0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON4

Address: Operational Base(0xFF910000) + offset (0x1010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	uart4_iso_ctrl UART4 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

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Bit	Attr	Reset Value	Description
14	RW	0x0	uart3_iso_ctrl UART3 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
13	RW	0x0	uart2_iso_ctrl UART2 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
12	RW	0x0	uart1_iso_ctrl UART1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
11	RW	0x0	uart0_iso_ctrl UART0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
10	RW	0x0	spi1_iso_ctrl SPI1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
9	RW	0x0	spi0_iso_ctrl SPI0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
8	RW	0x0	i2c2_iso_ctrl I2C2 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
7	RW	0x0	i2c1_iso_ctrl I2C1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
6	RW	0x0	i2c0_iso_ctrl I2C0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
5:4	RO	0x0	reserved
3:0	RW	0x0	spinlock_iso_ctrl SPINLOCK slave isolation control bit, There are 16KB address space for SPINLOCK, it is separated into four 4KB space. spinlock_iso_ctrl[0], first 4KB spinlock_iso_ctrl[1], second 4KB spinlock_iso_ctrl[2], third 4KB spinlock_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON5

Address: Operational Base(0xFF910000) + offset (0x1014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3_iso_ctrl GPIO3 slave isolation control bit. There are 16KB address space for GPIO3, it is separated into four 4KB space. gpio3_iso_ctrl[0], first 4KB gpio3_iso_ctrl[1], second 4KB gpio3_iso_ctrl[2], third 4KB gpio3_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
11:8	RW	0x0	gpio2_iso_ctrl GPIO2 slave isolation control bit. There are 16KB address space for GPIO2, it is separated into four 4KB space. gpio2_iso_ctrl[0], first 4KB gpio2_iso_ctrl[1], second 4KB gpio2_iso_ctrl[2], third 4KB gpio2_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
7:0	RW	0x00	pwm1_iso_ctrl PWM1 slave isolation control bit. There are 32KB address space for PWM1, it is separated into eight 4KB space. pwm1_iso_ctrl[0], first 4KB pwm1_iso_ctrl[1], second 4KB pwm1_iso_ctrl[2], third 4KB pwm1_iso_ctrl[3], fourth 4KB pwm1_iso_ctrl[4], fifth 4KB pwm1_iso_ctrl[5], sixth 4KB pwm1_iso_ctrl[6], seventh 4KB pwm1_iso_ctrl[7], eighth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON6

Address: Operational Base(0xFF910000) + offset (0x1018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gpio1_ioc_iso_ctrl GPIO1_IOC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
14	RW	0x0	dphy_iso_ctrl DPHY slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
13	RW	0x0	dsi_iso_ctrl DSI slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
12	RW	0x0	spdif_rx_iso_ctrl SPDIF_RX slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

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Bit	Attr	Reset Value	Description
11	RW	0x0	spdif_tx_iso_ctrl SPDIF_TX slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
10	RW	0x0	pdm_iso_ctrl PDM slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
9	RW	0x0	can1_iso_ctrl CAN1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
8	RW	0x0	can0_iso_ctrl CAN0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
7	RW	0x0	sai1_iso_ctrl SAI1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
6	RW	0x0	sai0_iso_ctrl SAI0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
5	RW	0x0	asrc1_iso_ctrl ASRC1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
4	RW	0x0	asrc0_iso_ctrl ASRC0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
3:0	RW	0x0	gpio4_iso_ctrl GPIO4 slave isolation control bit. There are 16KB address space for GPIO4, it is separated into four 4KB space. gpio4_iso_ctrl[0], first 4KB gpio4_iso_ctrl[1], second 4KB gpio4_iso_ctrl[2], third 4KB gpio4_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON7

Address: Operational Base(0xFF910000) + offset (0x101C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	fspi_iso_ctrl FSPI slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

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Bit	Attr	Reset Value	Description
14	RW	0x0	sdmmc_iso_ctrl SDMMC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
13	RW	0x0	audio_adc_iso_ctrl Audio ADC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
12	RW	0x0	gpio234_ioc_iso_ctrl GPIO2_IOC/GPIO3_IOC/GPIO4_IOC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
11	RW	0x0	saradc_iso_ctrl SARADC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
10	RW	0x0	otpc_ns_iso_ctrl Non-secure OTPC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
9	RW	0x0	uart5_iso_ctrl UART5 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
8	RW	0x0	spi2_iso_ctrl SPI2 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
7	RW	0x0	mac1_iso_ctrl MAC1 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
6	RW	0x0	mac0_iso_ctrl MAC0 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
5	RW	0x0	secure_keyreader_iso_ctrl Secure KEYREADER slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
4	RW	0x0	secure_otpc_mask_iso_ctrl Secure OTPC mask slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
3	RW	0x0	secure_otpc_iso_ctrl Secure OTPC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
2	RW	0x0	vop_iso_ctrl VOP slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
1	RW	0x0	rga_iso_ctrl RGA slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

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Bit	Attr	Reset Value	Description
0	RW	0x0	tsadc_iso_ctrl TSADC controller slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON8

Address: Operational Base(0xFF910000) + offset (0x1020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0_iso_ctrl GPIO0 slave isolation control bit. There are 16KB address space for GPIO0, it is separated into four 4KB space. gpio0_iso_ctrl[0], first 4KB gpio0_iso_ctrl[1], second 4KB gpio0_iso_ctrl[2], third 4KB gpio0_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
11	RW	0x0	sgrf_pmu_iso_ctrl sgrf_pmu slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
10:7	RW	0x2	grf_pmu_iso_ctrl GRF_PMU slave isolation control bit. There are 16KB address space for GRF_PMU, it is separated into four 4KB space. grf_pmu_iso_ctrl[0], first 4KB grf_pmu_iso_ctrl[1], second 4KB grf_pmu_iso_ctrl[2], third 4KB grf_pmu_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
6	RW	0x0	secure_cru_pmu_iso_ctrl Secure CRU_PMU slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
5	RW	0x0	cru_pmu_iso_ctrl CRU_PMU slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
4	RW	0x0	pmu_iso_ctrl PMU slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
3	RW	0x0	audio_dsm_iso_ctrl Audio DSM slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
2	RW	0x0	sai4_iso_ctrl SAI4 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

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Bit	Attr	Reset Value	Description
1	RW	0x0	sai3_iso_ctrl SAI3 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
0	RW	0x0	sai2_iso_ctrl SAI2 slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON9

Address: Operational Base(0xFF910000) + offset (0x1024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	secure_cru_iso_ctrl Secure CRU slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
11	RW	0x0	cru_iso_ctrl CRU slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
10	RW	0x0	gpio0_ioc_iso_ctrl GPIO0_IOC slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
9	RW	0x0	touchkey_iso_ctrl Touch key slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
8:5	RW	0x0	pwm0_iso_ctrl PWM0 slave isolation control bit. There are 16KB address space for PWM0, it is separated into four 4KB space. pwm0_iso_ctrl[0], first 4KB pwm0_iso_ctrl[1], second 4KB pwm0_iso_ctrl[2], third 4KB pwm0_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
4	RW	0x0	hptimer_iso_ctrl HPTIMER slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
3:0	RW	0x0	gpio1_shadow_iso_ctrl GPIO1_SHADOW slave isolation control bit. There are 16KB address space for GPIO1_SHADOW, it is separated into four 4KB space. gpio1_shadow_iso_ctrl[0], first 4KB gpio1_shadow_iso_ctrl[1], second 4KB gpio1_shadow_iso_ctrl[2], third 4KB gpio1_shadow_iso_ctrl[3], fourth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

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GRF_PMU_MCU_ISO_CON10

Address: Operational Base(0xFF910000) + offset (0x1028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	nocsrv_firewall_iso_ctrl firewall slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
5	RW	0x0	nocsrv_ddr_iso_ctrl noc service ddr slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
4	RW	0x0	nocsrv_vio_iso_ctrl noc service vio slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
3	RW	0x0	nocsrv_hsperi_iso_ctrl noc service hsperi slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
2	RW	0x0	nocsrv_bus_iso_ctrl noc service bus slave isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
1	RW	0x0	nocsrv_cpup_iso_ctrl noc service cpu peripheral isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU
0	RW	0x0	nocsrv_cpu_iso_ctrl noc service cpu isolation control bit 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_CON11

Address: Operational Base(0xFF910000) + offset (0x102C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sysram_iso_ctrl System sram isolation control bit, There are 48KB address space for System sram, it is separated into eight 4KB space. sysram_iso_ctrl[0], first 4KB sysram_iso_ctrl[1], second 4KB sysram_iso_ctrl[2], third 4KB sysram_iso_ctrl[3], fourth 4KB sysram_iso_ctrl[4], fifth 4KB sysram_iso_ctrl[5], sixth 4KB sysram_iso_ctrl[6], seventh 4KB sysram_iso_ctrl[7], eighth 4KB sysram_iso_ctrl[8], ninth 4KB sysram_iso_ctrl[9], tenth 4KB sysram_iso_ctrl[10], eleventh 4KB sysram_iso_ctrl[11], twelfth 4KB 1'b0: Can be access by MCU 1'b1: Can not be access by MCU

GRF_PMU_MCU_ISO_DDR_CON0

Address: Operational Base(0xFF910000) + offset (0x1400)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb2otg1_ddr_iso_ctrl USB2.0_OTG1 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[15] and CPU_ISO_DDR_CON0[15]. It can not be access when any bit is asserted.
14	RW	0x0	usb2otg0_ddr_iso_ctrl USB2.0_OTG0 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[14] and CPU_ISO_DDR_CON0[14]. It can not be access when any bit is asserted.
13	RW	0x0	spi2_ddr_iso_ctrl SPI2 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[13] and CPU_ISO_DDR_CON0[13]. It can not be access when any bit is asserted.
12	RW	0x0	rga_wr_ddr_iso_ctrl RGA write access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[12] and CPU_ISO_DDR_CON0[12]. It can not be access when any bit is asserted.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
11	RW	0x0	rga_rd_ddr_iso_ctrl RGA read access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[11] and CPU_ISO_DDR_CON0[11]. It can not be access when any bit is asserted.
10	RW	0x0	dma2ddr_ddr_iso_ctrl DMA2DDR access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[10] and CPU_ISO_DDR_CON0[10]. It can not be access when any bit is asserted.
9	RW	0x0	mcu_ddr_iso_ctrl MCU access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[9] and CPU_ISO_DDR_CON0[9]. It can not be access when any bit is asserted.
8	RW	0x0	mac1_ddr_iso_ctrl MAC1 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[8] and CPU_ISO_DDR_CON0[8]. It can not be access when any bit is asserted.
7	RW	0x0	mac0_ddr_iso_ctrl MAC0 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[7] and CPU_ISO_DDR_CON0[7]. It can not be access when any bit is asserted.
6	RW	0x0	fpsi_ddr_iso_ctrl FSPI access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[6] and CPU_ISO_DDR_CON0[6]. It can not be access when any bit is asserted.
5	RW	0x0	sdmmc_ddr_iso_ctrl SDMMC access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[5] and CPU_ISO_DDR_CON0[5]. It can not be access when any bit is asserted.
4	RW	0x0	dmac1_ddr_iso_ctrl DMAC1 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[4] and CPU_ISO_DDR_CON0[4]. It can not be access when any bit is asserted.

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Bit	Attr	Reset Value	Description
3	RW	0x0	dmac0_ddr_iso_ctrl DMAC0 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[3] and CPU_ISO_DDR_CON0[3]. It can not be access when any bit is asserted.
2	RW	0x0	crypto_ddr_iso_ctrl CRYPTO access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[2] and CPU_ISO_DDR_CON0[2]. It can not be access when any bit is asserted.
1	RW	0x0	flexbus_ddr_iso_ctrl FLEXBUS access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[1] and CPU_ISO_DDR_CON0[1]. It can not be access when any bit is asserted.
0	RW	0x0	cpu_ddr_iso_ctrl CPU access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[0] and CPU_ISO_DDR_CON0[0]. It can not be access when any bit is asserted.

GRF_PMU_MCU_ISO_DDR_CON1

Address: Operational Base(0xFF910000) + offset (0x1404)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	vop_ddr_iso_ctrl VOP access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON1[0] and CPU_ISO_DDR_CON1[0]. It can not be access when any bit is asserted.

GRF_PMU_MCU_ISO_LOCK

Address: Operational Base(0xFF910000) + offset (0x1500)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mcu_iso_lock Lock for MCU isolation register program. If it is programmed to 1, MCU isolation register locked and cannot be programmed.

GRF_PMU_CPU_ISO_CON0

Address: Operational Base(0xFF910000) + offset (0x2000)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	dsmc_mem_iso_ctrl DSMC_MEM control bit. There are 1024MB address space for DSMC_MEM, it is separated into four 256MB space. dsmc_mem_iso_ctrl[0], first 256MB dsmc_mem_iso_ctrl[1], second 256MB dsmc_mem_iso_ctrl[2], third 256MB dsmc_mem_iso_ctrl[3], fourth 256MB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
11	RW	0x0	dsmc_iso_ctrl DSMC isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
10	RO	0x0	reserved
9	RW	0x0	flexbus_iso_ctrl FLEXBUS isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
8:5	RW	0x0	gpio1_iso_ctrl GPIO1 isolation control bit. There are 16KB address space for GPIO1, it is separated into four 4KB space. gpio1_iso_ctrl[0], first 4KB gpio1_iso_ctrl[1], second 4KB gpio1_iso_ctrl[2], third 4KB gpio1_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
4:1	RW	0x0	grf_core_iso_ctrl GRF_CORE slave isolation control bit. There are 16KB address space for GRF_CORE, it is separated into four 4KB space. grf_core_iso_ctrl[0], first 4KB grf_core_iso_ctrl[1], second 4KB grf_core_iso_ctrl[2], third 4KB grf_core_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
0	RW	0x0	a7dbg_iso_ctrl A7 debug isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON1

Address: Operational Base(0xFF910000) + offset (0x2004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	mailbox_iso_ctrl MAILBOX slave isolation control bit, There are 16KB address space for MAILBOX, it is separated into four 4KB space. mailbox_iso_ctrl[0], first 4KB mailbox_iso_ctrl[1], second 4KB mailbox_iso_ctrl[2], third 4KB mailbox_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
11:8	RW	0x0	grf_bus_iso_ctrl GRF_BUS slave isolation control bit. There are 16KB address space for GRF_BUS, it is separated into four 4KB space. grf_bus_iso_ctrl[0], first 4KB grf_bus_iso_ctrl[1], second 4KB grf_bus_iso_ctrl[2], third 4KB grf_bus_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
7	RW	0x0	ddr_lpc_iso_ctrl DDR LPC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
6	RW	0x0	ddr_monitor_iso_ctrl DDR monitor slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
5	RW	0x0	ddrc_iso_ctrl DDR controller slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
4	RW	0x0	dmac1_iso_ctrl DMAC1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
3	RW	0x0	dmac0_iso_ctrl DMAC0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
2	RW	0x0	sgrf_bus_iso_ctrl SGRF_BUS isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
1	RW	0x0	secure_dmac1_iso_ctrl DMAC1 secure only slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
0	RW	0x0	secure_dmac0_iso_ctrl DMAC0 secure only slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON2

Address: Operational Base(0xFF910000) + offset (0x2008)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	timer1_iso_ctrl TIMER1 slave isolation control bit. There are 32KB address space for TIMER1, it is separated into eight 4KB space. timer1_iso_ctrl[0], first 4KB timer1_iso_ctrl[1], second 4KB timer1_iso_ctrl[2], third 4KB timer1_iso_ctrl[3], fourth 4KB timer1_iso_ctrl[4], fifth 4KB timer1_iso_ctrl[5], sixth 4KB timer1_iso_ctrl[6], seventh 4KB timer1_iso_ctrl[7], eighth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
7:0	RW	0x00	timer0_iso_ctrl TIMER0 slave isolation control bit. There are 32KB address space for TIMER0, it is separated into eight 4KB space. timer0_iso_ctrl[0], first 4KB timer0_iso_ctrl[1], second 4KB timer0_iso_ctrl[2], third 4KB timer0_iso_ctrl[3], fourth 4KB timer0_iso_ctrl[4], fifth 4KB timer0_iso_ctrl[5], sixth 4KB timer0_iso_ctrl[6], seventh 4KB timer0_iso_ctrl[7], eighth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON3

Address: Operational Base(0xFF910000) + offset (0x200C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	dma2ddr_iso_ctrl DMA2DDR slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
13	RW	0x0	secure_trng_iso_ctrl Secure RNG slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
12	RW	0x0	secure_keyladder_iso_ctrl Secure keyladder slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
11	RW	0x0	secure_crypto_iso_ctrl Secure CRYPTO slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

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Bit	Attr	Reset Value	Description
10	RW	0x0	bootrom_iso_ctrl BOOTROM slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
9	RW	0x0	ddrphy_iso_ctrl DDRPHY slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
8	RW	0x0	usb2otg1_iso_ctrl USB2.0_OTG1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
7	RW	0x0	usb2otg0_iso_ctrl USB2.0_OTG0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
6	RW	0x0	ns_trng_iso_ctrl RNG non-secure slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
5	RW	0x0	ns_crypto_iso_ctrl Crypto non-secure slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
4	RW	0x0	usbphy_iso_ctrl USBPHY slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
3	RW	0x0	intmux_iso_ctrl INTMUX slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
2	RO	0x0	reserved
1	RW	0x0	wdt1_iso_ctrl WDT1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
0	RW	0x0	wdt0_iso_ctrl WDT0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON4

Address: Operational Base(0xFF910000) + offset (0x2010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	uart4_iso_ctrl UART4 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

Rockchip Confidencial

Bit	Attr	Reset Value	Description
14	RW	0x0	uart3_iso_ctrl UART3 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
13	RW	0x0	uart2_iso_ctrl UART2 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
12	RW	0x0	uart1_iso_ctrl UART1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
11	RW	0x0	uart0_iso_ctrl UART0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
10	RW	0x0	spi1_iso_ctrl SPI1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
9	RW	0x0	spi0_iso_ctrl SPI0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
8	RW	0x0	i2c2_iso_ctrl I2C2 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
7	RW	0x0	i2c1_iso_ctrl I2C1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
6	RW	0x0	i2c0_iso_ctrl I2C0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
5:4	RO	0x0	reserved
3:0	RW	0x0	spinlock_iso_ctrl SPINLOCK slave isolation control bit, There are 16KB address space for SPINLOCK, it is separated into four 4KB space. spinlock_iso_ctrl[0], first 4KB spinlock_iso_ctrl[1], second 4KB spinlock_iso_ctrl[2], third 4KB spinlock_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON5

Address: Operational Base(0xFF910000) + offset (0x2014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3_iso_ctrl GPIO3 slave isolation control bit. There are 16KB address space for GPIO3, it is separated into four 4KB space. gpio3_iso_ctrl[0], first 4KB gpio3_iso_ctrl[1], second 4KB gpio3_iso_ctrl[2], third 4KB gpio3_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
11:8	RW	0x0	gpio2_iso_ctrl GPIO2 slave isolation control bit. There are 16KB address space for GPIO2, it is separated into four 4KB space. gpio2_iso_ctrl[0], first 4KB gpio2_iso_ctrl[1], second 4KB gpio2_iso_ctrl[2], third 4KB gpio2_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
7:0	RW	0x00	pwm1_iso_ctrl PWM1 slave isolation control bit. There are 32KB address space for PWM1, it is separated into eight 4KB space. pwm1_iso_ctrl[0], first 4KB pwm1_iso_ctrl[1], second 4KB pwm1_iso_ctrl[2], third 4KB pwm1_iso_ctrl[3], fourth 4KB pwm1_iso_ctrl[4], fifth 4KB pwm1_iso_ctrl[5], sixth 4KB pwm1_iso_ctrl[6], seventh 4KB pwm1_iso_ctrl[7], eighth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON6

Address: Operational Base(0xFF910000) + offset (0x2018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gpio1_ioc_iso_ctrl GPIO1_IOC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
14	RW	0x0	dphy_iso_ctrl DPHY slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
13	RW	0x0	dsi_iso_ctrl DSI slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
12	RW	0x0	spdif_rx_iso_ctrl SPDIF_RX slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

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Bit	Attr	Reset Value	Description
11	RW	0x0	spdif_tx_iso_ctrl SPDIF_TX slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
10	RW	0x0	pdm_iso_ctrl PDM slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
9	RW	0x0	can1_iso_ctrl CAN1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
8	RW	0x0	can0_iso_ctrl CAN0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
7	RW	0x0	sai1_iso_ctrl SAI1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
6	RW	0x0	sai0_iso_ctrl SAI0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
5	RW	0x0	asrc1_iso_ctrl ASRC1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
4	RW	0x0	asrc0_iso_ctrl ASRC0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
3:0	RW	0x0	gpio4_iso_ctrl GPIO4 slave isolation control bit. There are 16KB address space for GPIO4, it is separated into four 4KB space. gpio4_iso_ctrl[0], first 4KB gpio4_iso_ctrl[1], second 4KB gpio4_iso_ctrl[2], third 4KB gpio4_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON7

Address: Operational Base(0xFF910000) + offset (0x201C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	fspi_iso_ctrl FSPI slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

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Bit	Attr	Reset Value	Description
14	RW	0x0	sdmmc_iso_ctrl SDMMC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
13	RW	0x0	audio_adc_iso_ctrl Audio ADC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
12	RW	0x0	gpio234_ioc_iso_ctrl GPIO2_IOC/GPIO3_IOC/GPIO4_IOC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
11	RW	0x0	saradc_iso_ctrl SARADC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
10	RW	0x0	otpc_ns_iso_ctrl Non-secure OTPC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
9	RW	0x0	uart5_iso_ctrl UART5 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
8	RW	0x0	spi2_iso_ctrl SPI2 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
7	RW	0x0	mac1_iso_ctrl MAC1 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
6	RW	0x0	mac0_iso_ctrl MAC0 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
5	RW	0x0	secure_keyreader_iso_ctrl Secure KEYREADER slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
4	RW	0x0	secure_otpc_mask_iso_ctrl Secure OTPC mask slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
3	RW	0x0	secure_otpc_iso_ctrl Secure OTPC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
2	RW	0x0	vop_iso_ctrl VOP slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
1	RW	0x0	rga_iso_ctrl RGA slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

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Bit	Attr	Reset Value	Description
0	RW	0x0	tsadc_iso_ctrl TSADC controller slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON8

Address: Operational Base(0xFF910000) + offset (0x2020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0_iso_ctrl GPIO0 slave isolation control bit. There are 16KB address space for GPIO0, it is separated into four 4KB space. gpio0_iso_ctrl[0], first 4KB gpio0_iso_ctrl[1], second 4KB gpio0_iso_ctrl[2], third 4KB gpio0_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
11	RW	0x0	sgrf_pmu_iso_ctrl sgrf_pmu slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
10:7	RW	0x4	grf_pmu_iso_ctrl GRF_PMU slave isolation control bit. There are 16KB address space for GRF_PMU, it is separated into four 4KB space. grf_pmu_iso_ctrl[0], first 4KB grf_pmu_iso_ctrl[1], second 4KB grf_pmu_iso_ctrl[2], third 4KB grf_pmu_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
6	RW	0x0	secure_cru_pmu_iso_ctrl Secure CRU_PMU slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
5	RW	0x0	cru_pmu_iso_ctrl CRU_PMU slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
4	RW	0x0	pmu_iso_ctrl PMU slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
3	RW	0x0	audio_dsm_iso_ctrl Audio DSM slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
2	RW	0x0	sai4_iso_ctrl SAI4 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

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Bit	Attr	Reset Value	Description
1	RW	0x0	sai3_iso_ctrl SAI3 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
0	RW	0x0	sai2_iso_ctrl SAI2 slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON9

Address: Operational Base(0xFF910000) + offset (0x2024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	secure_cru_iso_ctrl Secure CRU slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
11	RW	0x0	cru_iso_ctrl CRU slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
10	RW	0x0	gpio0_ioc_iso_ctrl GPIO0_IOC slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
9	RW	0x0	touchkey_iso_ctrl Touch key slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
8:5	RW	0x0	pwm0_iso_ctrl PWM0 slave isolation control bit. There are 16KB address space for PWM0, it is separated into four 4KB space. pwm0_iso_ctrl[0], first 4KB pwm0_iso_ctrl[1], second 4KB pwm0_iso_ctrl[2], third 4KB pwm0_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
4	RW	0x0	hptimer_iso_ctrl HPTIMER slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
3:0	RW	0x0	gpio1_shadow_iso_ctrl GPIO1_SHADOW slave isolation control bit. There are 16KB address space for GPIO1_SHADOW, it is separated into four 4KB space. gpio1_shadow_iso_ctrl[0], first 4KB gpio1_shadow_iso_ctrl[1], second 4KB gpio1_shadow_iso_ctrl[2], third 4KB gpio1_shadow_iso_ctrl[3], fourth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

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GRF_PMU_CPU_ISO_CON10

Address: Operational Base(0xFF910000) + offset (0x2028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	nocsrv_firewall_iso_ctrl firewall slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
5	RW	0x0	nocsrv_ddr_iso_ctrl noc service ddr slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
4	RW	0x0	nocsrv_vio_iso_ctrl noc service vio slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
3	RW	0x0	nocsrv_hsperi_iso_ctrl noc service hsperi slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
2	RW	0x0	nocsrv_bus_iso_ctrl noc service bus slave isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
1	RW	0x0	nocsrv_cpup_iso_ctrl noc service cpu peripheral isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU
0	RW	0x0	nocsrv_cpu_iso_ctrl noc service cpu isolation control bit 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_CON11

Address: Operational Base(0xFF910000) + offset (0x202C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sysram_iso_ctrl System sram isolation control bit, There are 48KB address space for System sram, it is separated into eight 4KB space. sysram_iso_ctrl[0], first 4KB sysram_iso_ctrl[1], second 4KB sysram_iso_ctrl[2], third 4KB sysram_iso_ctrl[3], fourth 4KB sysram_iso_ctrl[4], fifth 4KB sysram_iso_ctrl[5], sixth 4KB sysram_iso_ctrl[6], seventh 4KB sysram_iso_ctrl[7], eighth 4KB sysram_iso_ctrl[8], ninth 4KB sysram_iso_ctrl[9], tenth 4KB sysram_iso_ctrl[10], eleventh 4KB sysram_iso_ctrl[11], twelfth 4KB 1'b0: Can be access by CPU 1'b1: Can not be access by CPU

GRF_PMU_CPU_ISO_DDR_CON0

Address: Operational Base(0xFF910000) + offset (0x2400)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb2otg1_ddr_iso_ctrl USB2.0_OTG1 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[15] and CPU_ISO_DDR_CON0[15]. It can not be access when any bit is asserted.
14	RW	0x0	usb2otg0_ddr_iso_ctrl USB2.0_OTG0 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[14] and CPU_ISO_DDR_CON0[14]. It can not be access when any bit is asserted.
13	RW	0x0	spi2_ddr_iso_ctrl SPI2 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[13] and CPU_ISO_DDR_CON0[13]. It can not be access when any bit is asserted.
12	RW	0x0	rga_wr_ddr_iso_ctrl RGA write access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[12] and CPU_ISO_DDR_CON0[12]. It can not be access when any bit is asserted.

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Bit	Attr	Reset Value	Description
11	RW	0x0	rga_rd_ddr_iso_ctrl RGA read access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[11] and CPU_ISO_DDR_CON0[11]. It can not be access when any bit is asserted.
10	RW	0x0	dma2ddr_ddr_iso_ctrl DMA2DDR access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[10] and CPU_ISO_DDR_CON0[10]. It can not be access when any bit is asserted.
9	RW	0x0	mcu_ddr_iso_ctrl MCU access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[9] and CPU_ISO_DDR_CON0[9]. It can not be access when any bit is asserted.
8	RW	0x0	mac1_ddr_iso_ctrl MAC1 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[8] and CPU_ISO_DDR_CON0[8]. It can not be access when any bit is asserted.
7	RW	0x0	mac0_ddr_iso_ctrl MAC0 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[7] and CPU_ISO_DDR_CON0[7]. It can not be access when any bit is asserted.
6	RW	0x0	fpsi_ddr_iso_ctrl FSPI access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[6] and CPU_ISO_DDR_CON0[6]. It can not be access when any bit is asserted.
5	RW	0x0	sdmmc_ddr_iso_ctrl SDMMC access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[5] and CPU_ISO_DDR_CON0[5]. It can not be access when any bit is asserted.
4	RW	0x0	dmac1_ddr_iso_ctrl DMAC1 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[4] and CPU_ISO_DDR_CON0[4]. It can not be access when any bit is asserted.

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Bit	Attr	Reset Value	Description
3	RW	0x0	dmac0_ddr_iso_ctrl DMAC0 access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[3] and CPU_ISO_DDR_CON0[3]. It can not be access when any bit is asserted.
2	RW	0x0	crypto_ddr_iso_ctrl CRYPTO access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[2] and CPU_ISO_DDR_CON0[2]. It can not be access when any bit is asserted.
1	RW	0x0	flexbus_ddr_iso_ctrl FLEXBUS access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[1] and CPU_ISO_DDR_CON0[1]. It can not be access when any bit is asserted.
0	RW	0x0	cpu_ddr_iso_ctrl CPU access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON0[0] and CPU_ISO_DDR_CON0[0]. It can not be access when any bit is asserted.

GRF_PMU_CPU_ISO_DDR_CON1

Address: Operational Base(0xFF910000) + offset (0x2404)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	vop_ddr_iso_ctrl VOP access DDR isolation control bit 1'b0: Can be access 1'b1: Can not be access Notes: The access is controlled by MCU_ISO_DDR_CON1[0] and CPU_ISO_DDR_CON1[0]. It can not be access when any bit is asserted.

GRF_PMU_CPU_ISO_LOCK

Address: Operational Base(0xFF910000) + offset (0x2500)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	cpu_iso_lock Lock for CPU isolation register program. If it is programmed to 1, CPU isolation register locked and cannot be programmed.

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Chapter 6 Power Management Unit (PMU)

6.1 Overview

In order to meet low power requirements, a power management unit (PMU) is designed for controlling power resources in SOC. RK3506 PMU is dedicated for managing the power of the whole chip.

PMU supports the following features:

- Support multi voltage domains: VD_CORE, VD_LOGIC, VD_PMU, VD_PLL
- Support multi virtual power domains in VD_CORE: PD_CPU0, PD_CPU1, PD_CPU2
- Support power down/up all power domains by software or hardware
- Support power down/up all voltage domains by software or hardware
- Support CPU auto power down with two mode
- Support to clamp all VD_CORE output before power off VD_CORE in low power mode
- Support VD_CORE power down, send scu_pwroff output to IO
- Support to clamp all VD_PMU input before power off VD_LOGIC in low power mode
- Support VD_LOGIC power down, send pmu_sleep output to IO
- Support PMU controlled by CPU or MCU for low power management
- Support respective global interrupt disable for CPU and MCU in low power mode
- Support BIU idle operations: BIU_CPU, BIU_CPU_P, BIU_BUS, BIU_DDR, BIU_VIO, BIU_HSPERI, BIU_LSPERI
- Support to send idle request to BIU for each bus domain by software or hardware
- Support clock gate mask for each bus domain by software or hardware
- Support DDR low power management
- Support PLLs power down/up by hardware in low power mode
- Support PMU clock switch to low frequency clock in low power mode
- Support OSC enable/disable request in low power mode
- Support PMU sleep hold with configurable counter
- Support PWM auto switch to GPIO during power mode
- Support wakeup reset control for full chip in power off mode
- Support PMU debug info output to IO with UART interface mode
- Support varies configurable wakeup source for low power mode
- Support combined interrupt output for alarm and second catch interrupt

6.2 Block Diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

- APB Interface and Register: Provide AMBA APB interface for register read and write
- System Power State Control: Provide power management for various low power modes
- Power Gating Control: Provide power gating control for power domains

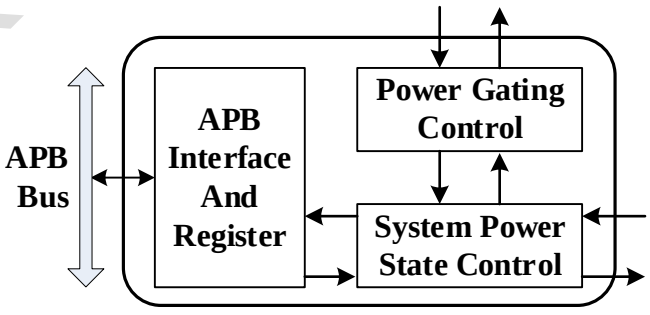

Fig. 6-1 PMU Bock Diagram

6.3 Function Description

6.3.1 Domain Partition

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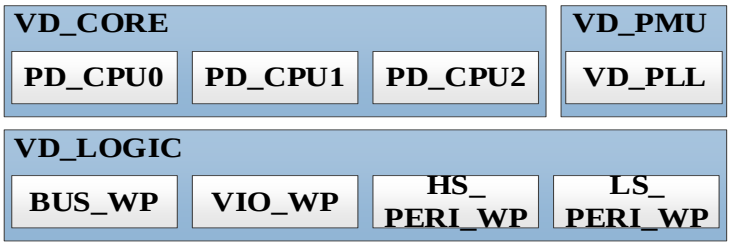

Fig. 6-2 RK3506 Voltage Domain and Power Domain Partition

The above diagram describes the power domain and voltage domain partition.

Table 6-1 RK3506 Voltage Domain and Power Domain Summary

Voltage Domain	Power Domain	Description
VD_CORE	PD_CPU0/1/2	CPU0/1/2 L1 I/D Cache L2 Cache SCU GIC400 CPU Debug CPU_EMA_DETECT PVTPLL_CORE GRF_CORE SGRF_CORE GPIO1 Master DSMC Slave DSMC FLEXBUS
VD_LOGIC		CRU PAD_RING/PMUX
	BUS_WRAPPER	MCU INTMUX Mailbox ROM AXI/AHB Slave SRAM GRF SGRF DMAC0/1 DMA2DDR DDRPHY DDRMON DDR_LPC DDRCTL S/NS Crypto S/NS RNG S KEYLAD SPINLOCK USB2.0_OTG0/1 USBPHY WDT0/1 TIMER0/1 BUS_IOC
	HS_PERI_WRAPPER	SDMMC FSPI S/NS OTPC OTP AP OTP Mask MAC0/1 UART5

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Voltage Domain	Power Domain	Description
		SPI2 SAI2/3/4 Audio DSM Audio ADC SARADC HSPERI_IOC
	LS_PERI_WRAPPER	SAI0/1 PDM SPDIF_TX SPDIF_RX ASRC0/1 CAN0/1 SPI0/1 GPIO2/3/4 Touch Key I2C0/1/2 UART0/1/2/3/4 PWM1/2
	VIO_WRAPPER	RGA DSI Host VOP DPHY TSADC
VD_PMU		system SRAM CRU_PMU GRF_PMU SGRF_PMU PMU HPTIMER PWM0 Touch Key OSC nPOR GPIO0 GPIO1_SHADOW PMU_IOC RM_IO PMU PAD RING/PMUX
	CLK_WRAPPER (VD_PLL)	OSC WiFi REFCLK GPLL VPLL0/1

6.3.2 Operation Mode

First of all, we define two operation modes of PMU, normal mode and low power mode.
When operating at normal mode, that means software can manage power sources directly by accessing PMU registers. For example, CPU can write PMU_PWR_GATE_CON register to determine that power off/on which power domain independently.
When operating at low power mode, software manages power sources indirectly through FSM (Finite States Machine) in PMU and those settings always not take effect immediately. That means software also can configure PMU registers to power down/up some power resources, but these setting will not be executed immediately after configuration. They will be delayed to execute after FSM running in particular phase.
To enter low power mode, after setting some power configurations, the PMU_PWR_CON[0] bit must be set 1 to enable PMU FSM. Then CPU needs to execute a WFI command to perform ready signal. After PMU detects all CPUs in WFI status, the FSM will be fetched. And the specific power sources will be controlled during specific status in FSM. So the low

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power mode is a "delay affect" way to handle power sources inside the RK3506 chip.

6.4 Register Description

6.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU_VERSION	0x0000	W	0x01010002	PMU version register
PMU_PWR_CON	0x0004	W	0x00000000	PMU power control register
PMU_GLB_POWER_STS	0x0008	W	0x00000000	PMU power status register
PMU_INT_MASK_CON	0x000C	W	0x00000000	Interrupt mask control register
PMU_WAKEUP_INT_CON	0x0010	W	0x00000000	Wakeup interrupt control register
PMU_WAKEUP_INT_ST	0x0014	W	0x00000000	Wakeup interrupt status register
PMU_DDR_PWR_CON	0x0020	W	0x00000000	DDR power hardware control register
PMU_DDR_PWR_SFTCON	0x0030	W	0x00000000	DDR power software control register
PMU_DDR_POWER_STS	0x0040	W	0x00000000	DDR power state register
PMU_DDR_STS	0x0044	W	0x00000000	DDR status register
PMU_CRU_PWR_CON0	0x0050	W	0x00000000	Clock and reset hardware power control register 0
PMU_CRU_PWR_CON1	0x0054	W	0x00000000	Clock and reset hardware power control register 1
PMU_CRU_PWR_SFTCON0	0x0058	W	0x00000000	Clock and reset software power control register 0
PMU_CRU_PWR_SFTCON1	0x005C	W	0x00000007	Clock and reset software power control register 1
PMU_CRU_POWER_STS	0x0060	W	0x00000000	Clock and reset power state register
PMU_PLLPD_CON	0x0070	W	0x00000000	PLL power hardware control register
PMU_PLLPD_SFTCON	0x0078	W	0x00000000	PLL power software control register
PMU_INFO_TX_CON	0x0080	W	0x00000000	PMU information transmit control register
PMU_PMIC_STABLE_CNT	0x0090	W	0x000FFFFF	PMIC stable counter register
PMU_OSC_STABLE_CNT	0x0094	W	0x000FFFFF	OSC stable counter register
PMU_WAKEUP_RSTCLR_CNT	0x0098	W	0x000FFFFF	Wakeup reset clear counter register
PMU_PLL_LOCK_CNT	0x009C	W	0x000FFFFF	PLL lock counter register
PMU_WAKEUP_TIMEOUT_CNT	0x00A0	W	0x00005DC0	WAKEUP timeout counter register
PMU_PWM_SWITCH_CNT	0x00A4	W	0x000FFFFF	PWM switch stable counter register
PMU_SLEEP_HOLD_CNT	0x00A8	W	0x000FFFFF	PMU sleep hold counter register

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Name	Offset	Size	Reset Value	Description
PMU_MISC_CON	0x00B0	W	0x00000000	PMU miscellaneous control register
PMU_MISC_INT_ST	0x00B4	W	0x00000000	PMU miscellaneous interrupt status register
PMU_ALARM_CNT	0x00B8	W	0x1FFFFFFF	Alarm counter register
PMU_RTC_ST	0x00BC	W	0x00000000	Real time clock status register
PMU_CLKDIV_CON	0x00C0	W	0x00007FFF	Clock divider control register
PMU_SCU_PWR_CON	0x1000	W	0x00000000	SCU power hardware control register
PMU_SCU_PWR_SFTCON	0x1004	W	0x00000000	SCU power software control register
PMU_SCU_AUTO_CON	0x1008	W	0x00000000	SCU power auto control register
PMU_SCU_POWER_STS	0x100C	W	0x00000000	SCU power state register
PMU_CLUSTER_PWR_ST	0x101C	W	0x00000000	Cluster power state register
PMU_CLUSTER_IDLE_CON	0x1020	W	0x00000000	Cluster idle control register
PMU_CLUSTER_IDLE_SFTCON	0x1024	W	0x00000000	Cluster idle software control register
PMU_CORE_PWRUP_CNT	0x1030	W	0x00005DC0	Core power up counter register
PMU_CORE_PWRDN_CNT	0x1034	W	0x00005DC0	Core power down counter register
PMU_CORE_STABLE_CNT	0x1038	W	0x000FFFFF	Core power stable counter register
PMU_CPU0_AUTO_PWR_CON	0x1040	W	0x00000000	CPU0 power control register
PMU_CPU1_AUTO_PWR_CON	0x1044	W	0x00000000	CPU1 power control register
PMU_CPU2_AUTO_PWR_CON	0x1048	W	0x00000000	CPU2 power control register
PMU_CPU0_PWR_SFTCON	0x1050	W	0x00000000	CPU0 power software control register
PMU_CPU1_PWR_SFTCON	0x1054	W	0x00000000	CPU1 power software control register
PMU_CPU2_PWR_SFTCON	0x1058	W	0x00000000	CPU2 power software control register
PMU_BIU_IDLE_CON	0x1100	W	0x00000000	BIU idle request hardware control register
PMU_BIU_IDLE_SFTCON	0x1110	W	0x00000000	BIU idle request software control register
PMU_BIU_IDLE_ACK	0x1120	W	0x00000000	BIU idle acknowledge status register
PMU_BIU_IDLE_ST	0x1128	W	0x00000000	BIU idle status register
PMU_BIU_GATMASK_CON	0x1130	W	0x00000000	BIU clock gate mask hardware control register
PMU_BIU_GATMASK_SFTCON	0x1140	W	0x00000000	BIU clock gate mask software control register

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

6.4.2 Detail Registers Description

PMU_VERSION

Address: Operational Base(0xFF900000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x01010002	version PMU version number.

PMU_PWR_CON

Address: Operational Base(0xFF900000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	R/WSC	0x0	sft_wakeup_en Low power mode software wakeup enable. When controller enters low power flow, this bit is automatically cleared. 1'b0: Disable 1'b1: Enable
14:8	RO	0x00	reserved
7	RW	0x0	cru_bypass Bypass clock and reset low power flow in low power procedure. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pwrgate_bypass Bypass power gate in low power procedure. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddr_bypass Bypass DDR in low power procedure. 1'b0: Disable 1'b1: Enable
4	RW	0x0	bus_bypass Bypass BIU idle in low power procedure. 1'b0: Disable 1'b1: Enable
3	RW	0x0	mcu_bypass Bypass MCU in low power procedure. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_act_bypass Bypass SCU active in low power procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	scu_bypass Bypass SCU in low power procedure. 1'b0: Disable 1'b1: Enable
0	R/WSC	0x0	powermode_en Low power mode enable. When controller enters low power flow, this bit is automatically cleared. 1'b0: Disable 1'b1: Enable

PMU_GLB_POWER_STS

Address: Operational Base(0xFF900000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	power_state PMU global power state. 4'h0: Normal state 4'h2: SCU low power state 4'h3: MCU low power state 4'h4: BIU low power state 4'h5: DDR low power state 4'h6: Power gate low power state 4'h7: Clock and reset low power state 4'h8: Sleep state 4'h9: Clock and reset active state 4'ha: Power gate active state 4'hb: DDR active state 4'hc: BIU active state 4'hd: MCU active state 4'he: SCU active state Others: Reserved

PMU_INT_MASK_CON

Address: Operational Base(0xFF900000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	mcu_rst_dis_cfg MCU reset disable by software. 1'b0: Disable, MCU reset assert 1'b1: Enable, MCU reset release

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Bit	Attr	Reset Value	Description
1	RW	0x0	glb_int_mask_mcu MCU global interrupt mask during low power procedure. 1'b0: Disable 1'b1: Enable
0	RW	0x0	glb_int_mask Global interrupt mask during low power procedure. 1'b0: Disable 1'b1: Enable

PMU_WAKEUP_INT_CON

Address: Operational Base(0xFF900000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	wakeup_timeout_en Enable PMU timeout interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
28	RW	0x0	wakeup_second_catch_int_en Enable PMU second catch interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
27	RW	0x0	wakeup_alarm_int_en Enable PMU alarm interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
26	RW	0x0	wakeup_saradc_int_en Enable SARADC interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
25	RW	0x0	wakeup_touch_key_int_en Enable Touch Key interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
24	RW	0x0	wakeup_can1_int_en Enable CAN1 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
23	RW	0x0	wakeup_can0_int_en Enable CAN0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
22	RW	0x0	wakeup_timer1_int_en Enable TIMER1 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
21	RW	0x0	wakeup_timer0_int_en Enable TIMER0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
20	RW	0x0	wakeup_mac1_int_en Enable MAC1 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
19	RW	0x0	wakeup_mac0_int_en Enable MAC0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
18	RW	0x0	wakeup_usb1_det_int_en Enable USB1 detect interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
17	RW	0x0	wakeup_usb0_det_int_en Enable USB0 detect interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
16	RW	0x0	wakeup_uart5_int_en Enable UART5 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
15	RW	0x0	wakeup_uart4_int_en Enable UART4 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
14	RW	0x0	wakeup_uart3_int_en Enable UART3 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
13	RW	0x0	wakeup_uart2_int_en Enable UART2 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
12	RW	0x0	wakeup_uart1_int_en Enable UART1 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
11	RW	0x0	wakeup_uart0_int_en Enable UART0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
10	RW	0x0	wakeup_pwm2_int_en Enable PWM2 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
9	RW	0x0	wakeup_pwm1_int_en Enable PWM1 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
8	RW	0x0	wakeup_pwm0_int_en Enable PWM0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
7	RW	0x0	wakeup_gpio4_int_en Enable GPIO4 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
6	RW	0x0	wakeup_gpio3_int_en Enable GPIO3 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
5	RW	0x0	wakeup_gpio2_int_en Enable GPIO2 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
4	RW	0x0	wakeup_gpio1_shadow_int_en Enable GPIO1 shadow interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
3	RW	0x0	wakeup_gpio0_int_en Enable GPIO0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_hptimer_int_en Enable HPTIMER interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
1	RW	0x0	wakeup_mcu_int_en Enable MCU interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
0	RW	0x0	wakeup_cpu_int_en Enable CPU interrupt as wakeup source. 1'b0: Disable 1'b1: Enable

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PMU_WAKEUP_INT_ST

Address: Operational Base(0xFF900000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	sft_wakeup_st PMU software wakeup as wakeup source status. 1'b0: Inactive 1'b1: Active
29	RO	0x0	wakeup_timeout_st PMU timeout interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
28	RO	0x0	wakeup_second_catch_int_st PMU second catch interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
27	RO	0x0	wakeup_alarm_int_st PMU alarm interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
26	RO	0x0	wakeup_saradc_int_st SARADC interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
25	RO	0x0	wakeup_touch_key_int_st Touch Key interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
24	RO	0x0	wakeup_can1_int_st CAN1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
23	RO	0x0	wakeup_can0_int_st CAN0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
22	RO	0x0	wakeup_timer1_int_st TIMER1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
21	RO	0x0	wakeup_timer0_int_st TIMER0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
20	RO	0x0	wakeup_mac1_int_st MAC1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
19	RO	0x0	wakeup_mac0_int_st MAC0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
18	RO	0x0	wakeup_usb1_det_int_st USB1 detect interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
17	RO	0x0	wakeup_usb0_det_int_st USB0 detect interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
16	RO	0x0	wakeup_uart5_int_st UART5 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
15	RO	0x0	wakeup_uart4_int_st UART4 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
14	RO	0x0	wakeup_uart3_int_st UART3 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
13	RO	0x0	wakeup_uart2_int_st UART2 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
12	RO	0x0	wakeup_uart1_int_st UART1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
11	RO	0x0	wakeup_uart0_int_st UART0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
10	RO	0x0	wakeup_pwm2_int_st PWM2 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
9	RO	0x0	wakeup_pwm1_int_st PWM1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	wakeup_pwm0_int_st PWM0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	wakeup_gpio4_int_st GPIO4 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	wakeup_gpio3_int_st GPIO3 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	wakeup_gpio2_int_st GPIO2 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	wakeup_gpio1_shadow_int_st GPIO1 shadow interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	wakeup_gpio0_int_st GPIO0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
2	RO	0x0	wakeup_hptimer_int_st HPTIMER interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	wakeup_mcu_int_st MCU interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	wakeup_cpu_int_st CPU interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active

PMU_DDR_PWR_CON

Address: Operational Base(0xFF900000) + offset (0x0020)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	ddrio_hz_exit_ena Enable DDR IO High-Z de-asserted performed by hardware. 1'b0: Disable 1'b1: Enable
11	RW	0x0	ddrio_hz_ena Enable DDR IO High-Z function performed by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x0	ddrphy_auto_gating_ena Enable DDRPHY auto clock gating function performed by PMU, when DDR enter self-refresh state. 1'b0: Disable 1'b1: Enable
9	RW	0x0	ddrctl_c_auto_gating_ena Enable DDRCTL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode. 1'b0: Disable 1'b1: Enable
8	RW	0x0	ddrctl_a_auto_gating_ena Enable DDRCTL's AXI-clock auto clock gating. AXI-clock can be gated when in self-refresh mode. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	ddrio_ret_exit_ena Enable DDR IO retention de-asserted performed by hardware. 1'b0: Disable 1'b1: Enable
4:3	RO	0x0	reserved
2	RW	0x0	ddrio_ret_ena Enable DDR IO retention function performed by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddr_sref_a_ena Enable DDR self-refresh mode for AXI-clock domain by hardware. 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RW	0x0	ddr_sref_c_ena Enable DDR self-refresh mode for core-clock domain by hardware. 1'b0: Disable 1'b1: Enable

PMU_DDR_PWR_SFTCON

Address: Operational Base(0xFF900000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	ddrio_hz_exit_sftena DDR IO High-Z exit request by software. 1'b0: Disable 1'b1: Enable
12	RW	0x0	ddrio_hz_enter_sftena DDR IO High-Z enter request by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	ddrctl_c_active_wait_enter 1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state
10	RW	0x0	ddrctl_a_active_wait_exit 1'b0: Not need to wait for ddrctl_a_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_a_active high before FSM exit self-refresh state
9	RW	0x0	ddrctl_c_active_wait_exit 1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state
8	RW	0x0	ddrctl_a_active_wait_enter 1'b0: Not need to wait for ddrctl_a_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_a_active low before FSM enter self-refresh state
7:6	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	ddrio_ret_exit_sftena DDR IO retention exit request by software. 1'b0: Disable 1'b1: Enable
4:3	RO	0x0	reserved
2	RW	0x0	ddrio_ret_enter_sftena DDR IO retention enter request by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddr_sref_a_sftena Enable DDR self-refresh mode for AXI-clock domain by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_c_sftena Enable DDR self-refresh mode for core-clock domain by software. 1'b0: Disable 1'b1: Enable

PMU_DDR_POWER_STS

Address: Operational Base(0xFF900000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	ddr_power_state DDR power state. 4'h0: Normal state 4'h1: Enter self-refresh mode for AXI-clock state 4'h2: Enter self-refresh mode core-clock state 4'h3: Enter retention mode state 4'h5: Sleep state 4'h7: Exit retention mode 4'h8: Exit self-refresh mode for core-clock state 4'h9: Exit self-refresh mode for AXI-clock state 4'ha: Enter IO High-Z mode state 4'hb: Exit IO High-Z mode Others: Reserved

PMU_DDR_STS

Address: Operational Base(0xFF900000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	ddrio_hz DDR IO High-Z state. 1'b0: Inactive 1'b1: Active
5	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RO	0x0	ddrctl_a_active DDRCTL AXI clock active. 1'b0: Inactive 1'b1: Active
3	RO	0x0	ddrctl_a_sysack DDRCTL AXI hardware low-power request acknowledge. 1'b0: Inactive 1'b1: Active
2	RO	0x0	ddrio_ret DDR IO retention state. 1'b0: Inactive 1'b1: Active
1	RO	0x0	ddrctl_c_active DDRCTL hardware low-power clock active. 1'b0: Inactive 1'b1: Active
0	RO	0x0	ddrctl_c_sysack DDRCTL hardware low-power request acknowledge. 1'b0: Inactive 1'b1: Active

PMU_CRU_PWR_CON0

Address: Operational Base(0xFF900000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	alive_hptimer_ena HPTIMER switch to 32KHz clock enable by hardware. 1'b0: Disable 1'b1: Enable
13	RW	0x0	vdpll_output_clamp_ena VD_PLL output clamp enable by hardware. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pwm_clk_gate_osc_ena PWM clock source OSC gating enable by hardware. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pwm_clk_gate_pll_ena PWM clock source PLL gating enable by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
10	RW	0x0	sleep_hold_ena PMU sleep hold enable by hardware. 1'b0: Disable 1'b1: Enable
9	RO	0x0	reserved
8	RW	0x0	pwm_switch_iout PWM switch output.
7	RW	0x0	pwm_gpio_ioe_ena PWM output enable by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pwm_switch_ena PWM switch enable by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	power_off_ena Chip power off enable by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	alive_osc_ena Clock of PMU wakeup source switch to oscillator enable by hardware. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_ena VD_PMU input clamp enable by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_ena Wakeup reset enable by hardware. If asserted, the whole chip except IPs supporting reset hold function will be reset. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_ena Invalidate oscillator by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	alive_32k_ena Clock of PMU wakeup source and clk_pmu switch to 32KHz clock enable by hardware. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_CON1

Address: Operational Base(0xFF900000) + offset (0x0054)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	clk_src_gate_mode Auto gate clock mode. 1'b0: Release when CRU_POWER_STS exit sleep state. 1'b1: Release when CRU_POWER_STS exit PLL power up state.
1	RW	0x0	core_clk_src_gate_ena Auto gate clock in VD_CORE when CRU_POWER_STS is in sleep state. 1'b0: Disable 1'b1: Enable
0	RW	0x0	logic_clk_src_gate_ena Auto gate clock in VD_LOGIC when CRU_POWER_STS is in sleep state. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_SFTCON0

Address: Operational Base(0xFF900000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	alive_hptimer_sftena Enable HPTIMER switch to 32KHz clock by software. 1'b0: Disable 1'b1: Enable
14:10	RO	0x00	reserved
9	RW	0x0	core_clk_src_gate_sftena Gate clock in VD_CORE when CRU_POWER_STS is in sleep state by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	logic_clk_src_gate_sftena Gate clock in VD_LOGIC when CRU_POWER_STS is in sleep state by software. 1'b0: Disable 1'b1: Enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7	RW	0x0	vdpll_clamp_sftena VD_PLL output clamp enable by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	power_off_pol Power off polarity. 1'b0: High active 1'b1: Low active
5	RW	0x0	power_off_sftena Power off chip by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	alive_osc_sftena Clock of PMU wakeup source switch to oscillator enable by software. When alive_32k_sftena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_sftena VD_PMU input clamp enable by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_sftena Wakeup reset enable by software. Reset the whole chip, except IPs supporting reset hold function. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_sftena Invalidate oscillator by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	alive_32k_sftena Clock of PMU wakeup source and clk_pmu switch to 32KHz clock enable by software. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_SFTCON1

Address: Operational Base(0xFF900000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable

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Bit	Attr	Reset Value	Description
			1'b1: Write access enable
15:3	RO	0x0000	reserved
2:0	RW	0x7	osc_ds OSC drive strength.

PMU_CRU_POWER_STS

Address: Operational Base(0xFF900000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	cru_power_state Clock and reset power state. 4'h0: Normal state 4'h1: Clock low frequency state 4'h2: PLL power down state 4'h4: Input clamp state 4'h5: Oscillator disable state 4'h6: Sleep state 4'h7: Wake up state 4'h9: Oscillator enable state 4'ha: Input clamp release state 4'hb: Clock high frequency state 4'hc: Wake up reset clear state 4'hd: GPIO switch state 4'he: PLL power up state 4'hf: PWM switch state Others: Reserved

PMU_PLLPD_CON

Address: Operational Base(0xFF900000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	vpll1_pd_ena VPLL1 power down by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	vpll0_pd_ena VPLL0 power down by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpll_pd_ena GPLL power down by hardware. 1'b0: Disable 1'b1: Enable

PMU_PLLPD_SFTCON

Address: Operational Base(0xFF900000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	vpll1_pd_sftena VPLL1 power down by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	vpll0_pd_sftena VPLL0 power down by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpll_pd_sftena GPLL power down by software. 1'b0: Disable 1'b1: Enable

PMU_INFO_TX_CON

Address: Operational Base(0xFF900000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	info_tx_en PMU debug information transmit enable. 1'b0: Disable 1'b1: Enable
7:0	RW	0x00	info_tx_intv_time The interval time from 1 byte sends over to a new byte sends start. The value is the cycle number counted in clk_pmu.

PMU_PMIC_STABLE_CNT

Address: Operational Base(0xFF900000) + offset (0x0090)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	stable_cnt PMIC power stable counter for CRU from power off to wake up.

PMU_OSC_STABLE_CNT

Address: Operational Base(0xFF900000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	stable_cnt OSC stable counter for OSC from disable to enable.

PMU_WAKEUP_RSTCLR_CNT

Address: Operational Base(0xFF900000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	wakeup_rstclr_cnt Stable counter for CRU wakeup reset clear.

PMU_PLL_LOCK_CNT

Address: Operational Base(0xFF900000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pll_lock_cnt Lock counter for PLL from power up to lock.

PMU_WAKEUP_TIMEOUT_CNT

Address: Operational Base(0xFF900000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00005dc0	wakeup_timeout_cnt PMU wakeup timeout counter.

PMU_PWM_SWITCH_CNT

Address: Operational Base(0xFF900000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	stable_cnt PWM switch stable counter.

PMU_SLEEP_HOLD_CNT

Address: Operational Base(0xFF900000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sleep_hold_cnt PMU sleep hold counter.

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PMU_MISC_CON

Address: Operational Base(0xFF900000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	R/WSC	0x0	rtc_en Real time clock enable. 1'b0: Disable 1'b1: Enable
5	R/WSC	0x0	timeout_mode Timeout mode select. 1'b0: timeout counter start once wakeup_timeout_en 1'b1: timeout counter start only when wakeup_timeout_en and PMU enter sleep
4	RO	0x0	reserved
3	R/WSC	0x0	second_catch_int_en Second catch interrupt enable. 1'b0: Disable 1'b1: Enable
2	R/WSC	0x0	second_catch_en Second catch enable. 1'b0: Disable 1'b1: Enable
1	R/WSC	0x0	alarm_int_en Alarm interrupt enable. 1'b0: Disable 1'b1: Enable
0	R/WSC	0x0	alarm_en Alarm enable. 1'b0: Disable 1'b1: Enable

PMU_MISC_INT_ST

Address: Operational Base(0xFF900000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	pmu_int_st PMU interrupt status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
1	RO	0x0	second_catch_int_st Second catch interrupt status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	alarm_int_st Alarm interrupt status. 1'b0: Inactive 1'b1: Active

PMU_ALARM_CNT

Address: Operational Base(0xFF900000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x1fffffff	alarm_cnt Alarm counter.

PMU_RTC_ST

Address: Operational Base(0xFF900000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	rtc_cnt Real time clock status.

PMU_CLKDIV_CON

Address: Operational Base(0xFF900000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x07fff	clkdiv_con PMU clock divider, which is used to get 1Hz clock from 32KHz source. Divide value equal clkdiv_con+1.

PMU_SCU_PWR_CON

Address: Operational Base(0xFF900000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	standbywfil2_bypass_ena L2 STANDBYWFI bypass enable for SCU enter low power mode by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	standbywfi_bypass_ena CPU STANDBYWFI bypass enable for SCU enter low power mode by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	scu_vol_gate_ena SCU voltage gate enable by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	cluster_clk_src_gate_ena CPU clock source gating enable by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	cluster_cpu_pwrdn_ena CPU power down enable by hardware. 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved
3	RW	0x0	scu_pwroff_ena SCU power off enable by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_ena SCU power down enable by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	l2_idle_ena L2 idle enable by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	l2_flush_ena L2 flash enable by hardware. 1'b0: Disable 1'b1: Enable

PMU_SCU_PWR_SFTCON

Address: Operational Base(0xFF900000) + offset (0x1004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	scu_pwroff_pol SCU power off polarity. 1'b0: High active. 1'b1: Low active.
4	RO	0x0	reserved
3	RW	0x0	scu_pwroff_sftena SCU power off enable by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_sftena SCU power down enable by software. 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	l2_flush_sftena L2 flash enable by software. 1'b0: Disable 1'b1: Enable

PMU_SCU_AUTO_CON

Address: Operational Base(0xFF900000) + offset (0x1008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scu_sft_wakeup_cluster_ena SCU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_int_mask_ena SCU interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	scu_int_wakeup_cluster_ena SCU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	scu_lp_ena SCU low power enable. 1'b0: Disable 1'b1: Enable

PMU_SCU_POWER_STS

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Address: Operational Base(0xFF900000) + offset (0x100C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	scu_power_state SCU power state. 4'h0: SCU normal state 4'h1: CPU power down state 4'h2: L2 flush state 4'h3: L2 idle state 4'h4: Cluster transfer idle state 4'h5: SCU power down state 4'h6: SCU sleep state 4'h7: SCU wakeup state 4'h8: SCU power up state 4'h9: Cluster transfer resume state 4'ha: CPU power up state Others: Reserved

PMU_CLUSTER_PWR_ST

Address: Operational Base(0xFF900000) + offset (0x101C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	scu_dwn_state SCU power down state. 1'b0: Inactive 1'b1: Active
11	RO	0x0	cpu2_dwn_state CPU2 power down state. 1'b0: Inactive 1'b1: Active
10	RO	0x0	cpu1_dwn_state CPU1 power down state. 1'b0: Inactive 1'b1: Active
9	RO	0x0	cpu0_dwn_state CPU0 power down state. 1'b0: Inactive 1'b1: Active
8	RO	0x0	idle_ack_cpu_p BIU_CPU_P idle acknowledge state. 1'b0: Inactive 1'b1: Active
7	RO	0x0	idle_cpu_p BIU_CPU_P idle state. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
6	RO	0x0	idle_ack_cpu BIU_CPU idle acknowledge state. 1'b0: Inactive 1'b1: Active
5	RO	0x0	idle_cpu BIU_CPU idle state. 1'b0: Inactive 1'b1: Active
4	RO	0x0	l2flushdone L2 flush done state. 1'b0: Inactive 1'b1: Active
3	RO	0x0	standbywfil2 L2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
2	RO	0x0	cpu2_standbywfi CPU2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
1	RO	0x0	cpu1_standbywfi CPU1 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
0	RO	0x0	cpu0_standbywfi CPU0 STANDBYWFI state. 1'b0: Inactive 1'b1: Active

PMU_CLUSTER_IDLE_CON

Address: Operational Base(0xFF900000) + offset (0x1020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	auto_gate_mask_cpu_p If enable, BIU_CPU_P corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	idle_req_cpu_p Enable sending bus idle request to NIU_CPU_P by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	auto_gate_mask_cpu If enable, BIU_CPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_cpu Enable sending bus idle request to NIU_CPU by hardware. 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

PMU_CLUSTER_IDLE_SFTCON

Address: Operational Base(0xFF900000) + offset (0x1024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	idle_req_cpu_p Enable sending bus idle request to NIU_CPU_P by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_cpu Enable sending bus idle request to NIU_CPU by software. 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

PMU_CORE_PWRUP_CNT

Address: Operational Base(0xFF900000) + offset (0x1030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	core_pwrup_cnt VD_CORE power up counter. The value is the cycle number counted in clk_pmu.

PMU_CORE_PWRDN_CNT

Address: Operational Base(0xFF900000) + offset (0x1034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:0	RW	0x05dc0	core_pwrdn_cnt VD_CORE power down counter. The value is the cycle number counted in clk_pmu.

PMU_CORE_STABLE_CNT

Address: Operational Base(0xFF900000) + offset (0x1038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	core_stable_cnt VD_CORE power stable counter. The value is the cycle number counted in clk_pmu.

PMU_CPU0_AUTO_PWR_CON

Address: Operational Base(0xFF900000) + offset (0x1040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	cpu0_auto_pwrdn_mode CPU0 auto power down mode. 1'b0: Auto power down after WFI. 1'b1: Auto power down after wakeup.
3	RW	0x0	cpu0_sft_wakeup_ena CPU0 software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu0_int_mask_ena CPU0 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu0_int_wakeup_ena CPU0 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu0_auto_pwrdn_ena CPU0 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU1_AUTO_PWR_CON

Address: Operational Base(0xFF900000) + offset (0x1044)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	cpu1_auto_pwrdn_mode CPU1 auto power down mode. 1'b0: Auto power down after WFI. 1'b1: Auto power down after wakeup.
3	RW	0x0	cpu1_sft_wakeup_ena CPU1 software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu1_int_mask_ena CPU1 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu1_int_wakeup_ena CPU1 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu1_auto_pwrdn_ena CPU1 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU2_AUTO_PWR_CON

Address: Operational Base(0xFF900000) + offset (0x1048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	cpu2_auto_pwrdn_mode CPU2 auto power down mode. 1'b0: Auto power down after WFI. 1'b1: Auto power down after wakeup.
3	RW	0x0	cpu2_sft_wakeup_ena CPU2 software wakeup enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	cpu2_int_mask_ena CPU2 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu2_int_wakeup_ena CPU2 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu2_auto_pwrdn_ena CPU2 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU0_PWR_SFTCON

Address: Operational Base(0xFF900000) + offset (0x1050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu0_sft_pwrdn_ena CPU0 power down enable by software. 1'b0: Disable 1'b1: Enable

PMU_CPU1_PWR_SFTCON

Address: Operational Base(0xFF900000) + offset (0x1054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu1_sft_pwrdn_ena CPU1 power down enable by software. 1'b0: Disable 1'b1: Enable

PMU_CPU2_PWR_SFTCON

Address: Operational Base(0xFF900000) + offset (0x1058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable

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Bit	Attr	Reset Value	Description
			1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu2_sft_pwrdn_ena CPU2 power down enable by software. 1'b0: Disable 1'b1: Enable

PMU_BIU_IDLE_CON

Address: Operational Base(0xFF900000) + offset (0x1100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	idle_req_ddr Enable sending bus idle request to BIU_DDR by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_vio Enable sending bus idle request to BIU_VIO by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_lsperi Enable sending bus idle request to BIU_LSPERI by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_hsperi Enable sending idle request to BIU_HSPERI by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_bus Enable sending bus idle request to BIU_BUS by hardware. 1'b0: Disable 1'b1: Enable

PMU_BIU_IDLE_SFTCON

Address: Operational Base(0xFF900000) + offset (0x1110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	idle_req_ddr Enable sending bus idle request to BIU_DDR by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_vio Enable sending bus idle request to BIU_VIO by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_lsperi Enable sending bus idle request to BIU_LSPERI by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_hsperi Enable sending bus idle request to BIU_HSPERI by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_bus Enable sending idle request to BIU_BUS by software. 1'b0: Disable 1'b1: Enable

PMU_BIU_IDLE_ACK

Address: Operational Base(0xFF900000) + offset (0x1120)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	idle_ack_ddr BIU_DDR bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
3	RO	0x0	idle_ack_vio BIU_VIO bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
2	RO	0x0	idle_ack_lsperi BIU_LSPERI bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
1	RO	0x0	idle_ack_hsperi BIU_HSPERI bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
0	RO	0x0	idle_ack_bus BIU_BUS bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

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PMU_BIU_IDLE_ST

Address: Operational Base(0xFF900000) + offset (0x1128)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	idle_ddr BIU_DDR idle state. 1'b0: Not idle 1'b1: Idle
3	RO	0x0	idle_vio BIU_VIO idle state. 1'b0: Not idle 1'b1: Idle
2	RO	0x0	idle_lsperi BIU_LSPERI idle state. 1'b0: Not idle 1'b1: Idle
1	RO	0x0	idle_hsperi BIU_HSPERI idle state. 1'b0: Not idle 1'b1: Idle
0	RO	0x0	idle_bus BIU_BUS idle state. 1'b0: Not idle 1'b1: Idle

PMU_BIU_GATMASK_CON

Address: Operational Base(0xFF900000) + offset (0x1130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	auto_gate_mask_ddr If enable, BIU_DDR corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
3	RW	0x0	auto_gate_mask_vio If enable, BIU_VIO corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	auto_gate_mask_lsperi If enable, BIU_LSPERI corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	auto_gate_mask_hsperi If enable, BIU_HSPERI corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
0	RW	0x0	auto_gate_mask_bus If enable, BIU_BUS corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

PMU_BIU_GATMASK_SFTCON

Address: Operational Base(0xFF900000) + offset (0x1140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	sft_gate_mask_ddr If enable, BIU_DDR corresponding clock can be opened or gated by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	sft_gate_mask_vio If enable, BIU_VIO corresponding clock can be opened or gated by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sft_gate_mask_lsperi If enable, BIU_LSPERI corresponding clock can be opened or gated by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	sft_gate_mask_hsperi If enable, BIU_HSPERI corresponding clock can be opened or gated by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	sft_gate_mask_bus If enable, BIU_BUS corresponding clock can be opened or gated by software. 1'b0: Disable 1'b1: Enable

6.5 Application Notes

6.5.1 Hardware Low Power Mode

PMU can work in low power mode by hardware. After setting some power configurations and setting PMU_PWR_CON[0] to 1, you can execute the WFI command of CPU, then PMU low power FSM will start to run. In this mode, PMU will manage power resources by hardware, such as send idle request to specified power domain, auto clock switch and clock gating, shut down PLLs, and so on. All of above are configurable by setting corresponding registers.

Also, the WFI status of CPU can be bypass if PMU_SCU_PWR_CON[8] is set to 1.

6.5.2 Software Low Power Mode

PMU can work in the low power mode by software. In this application, you can use CPU or MCU to set PMU software power control registers to execute low power procedure.

6.5.3 Power Management IO Usage

There are independent power supplies for different voltage domain. You can communicate with external PMIC (Power Management Integrated Circuits) through IO interface.

Table 6-2 Power Management IO Interface

Module Pin	Direction	Pin Name	IOMUX Setting
core_pwroff/pmu_sleep	O	RM_IO	

Notes: I=input, O=output, I/O=input/output, bidirectional. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

Setting PMUGRF_SOC_CON1[0] to 1 to output pmu_sleep, also, you can select the polarity by setting PMUGRF_SOC_CON1[1]. Setting PMUGRF_SOC_CON1[2] to 1 to output core_pwroff, also, you can select the polarity by setting PMUGRF_SOC_CON1[3].

Each voltage domain can generate one power off request. The voltage domain power off request can be generated as below:

(1) Enable power off control bit: Set corresponding bit to 1 in PMU_VOL_GATE_CON0.

(2) Power down internal power domain: If there is power domain included in the voltage domain, the power domain should be power down firstly. Else, skip this step.

(3) Power down voltage domain: Set corresponding bit to 1 in PMU_PWR_GATE_CON0 by hardware power gating or set corresponding bit to 1 in PMU_PWR_GATE_SFTCON0 by software power gating.

6.5.4 PMU Debug Information

The PMU internal states could be monitored through pmu_debug IO in 8-bit UART interface mode. The transmission can be enabled by setting PMU_INFO_TX_CON[8], and the transmission interval time can be set in PMU_INFO_TX_CON[7:0]. The PMU debug information is decoded as follows.

Table 6-3 PMU Debug Information Decode

Decode Value	PMU State	Description
2	CPU power down state	PMU_SCU_POWER_STS=4'h1
5	CORE transfer idle state	PMU_SCU_POWER_STS=4'h4
6	CORE power down state	PMU_SCU_POWER_STS=4'h5
8	Bus low power state	PMU_GLB_POWER_STS=4'h4
9	DDR enters self-refresh mode for core-clock state	PMU_DDR_POWER_STS=4'h2
10	DDR enters retention mode	PMU_DDR_POWER_STS=4'h3
13	Clock low frequency state	PMU_CRU_POWER_STS=4'h1

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Decode Value	PMU State	Description
14	PLL power down state	PMU_CRU_POWER_STS=4'h2
15	Input clamp state	PMU_CRU_POWER_STS=4'h4
16	Oscillator disable state	PMU_CRU_POWER_STS=4'h5
17	Sleep state	PMU_GLB_POWER_STS=4'h8
18	Wake up state	PMU_CRU_POWER_STS=4'h7
19	Oscillator enable state	PMU_CRU_POWER_STS=4'h9
20	Input clamp release state	PMU_CRU_POWER_STS=4'ha
21	Clock high frequency state	PMU_CRU_POWER_STS=4'hb
22	Wake up reset clear state	PMU_CRU_POWER_STS=4'hc
23	GPIO switch state	PMU_CRU_POWER_STS=4'hd
24	PLL power up state	PMU_CRU_POWER_STS=4'he
25	PWM switch state	PMU_CRU_POWER_STS=4'hf
28	DDR exits retention mode	PMU_DDR_POWER_STS=4'h7
29	DDR exits self-refresh mode for core-clock state	PMU_DDR_POWER_STS=4'h8
30	Bus active state	PMU_GLB_POWER_STS=4'hc
32	CORE wakeup state	PMU_SCU_POWER_STS=4'h7
33	CORE power up state	PMU_SCU_POWER_STS=4'h8
34	CORE transfer resume state	PMU_SCU_POWER_STS=4'h9
35	CPU power up state	PMU_SCU_POWER_STS=4'ha
39	DDR enters self-refresh for AXI-clock state	PMU_DDR_POWER_STS=4'h1
42	DDR exits self-refresh mode for AXI-clock state	PMU_DDR_POWER_STS=4'h9
43	DDR IO High-Z state	PMU_DDR_POWER_STS=4'ha
44	DDR exits IO High-Z state	PMU_DDR_POWER_STS=4'hb
Others	No care	-

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Chapter 7 Internal SRAM

7.1 Overview

There is one Internal SRAM in RK3506, named System SRAM. System SRAM can be divided into three 16KB slices, named System SRAM0/1/2. System SRAM0/1/2 can work as AXI slave devices from System Interconnection, it also supports work as TCM from MCU AHB slave interface. System SRAM supports read and write access to provide system fast access data storage.

7.1.1 Features supported

- System SRAM
  - Support 48KB capacity
  - Include System SRAM0/1/2 internal, each of them with 16KB capacity

7.2 Block Diagram

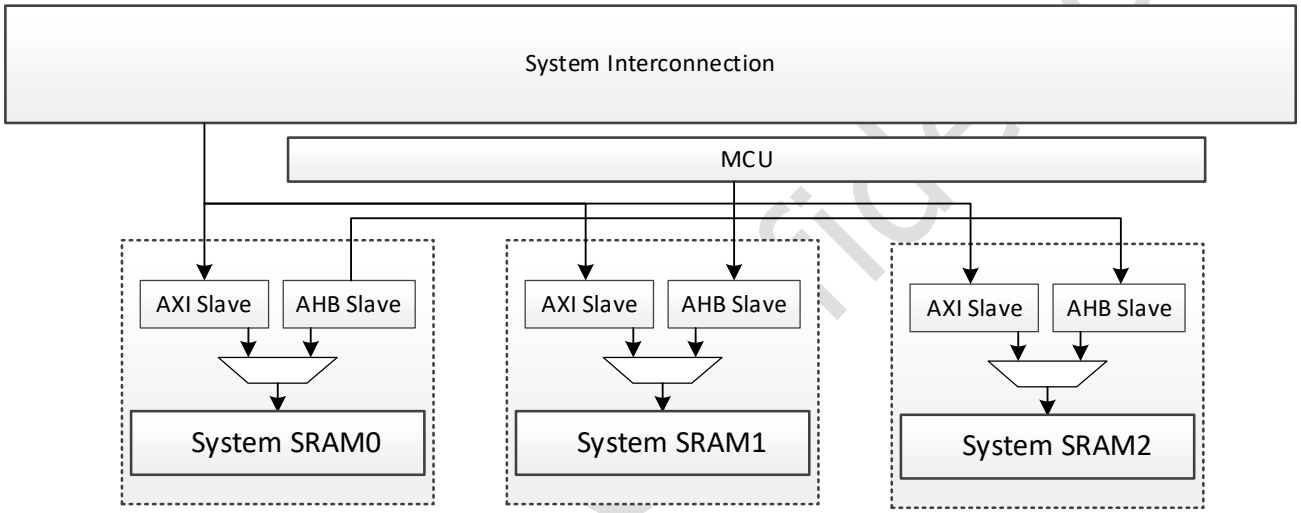

Fig.7-1 System SRAM Block Diagram

7.3 Function Description

7.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
System SRAM before remap address	0xfff80000
System SRAM remap address	0xfff80000
	0xffff0000

7.3.2 System SRAM Access Path

The System SRAM AXI slave device interface can be accessed by CPU, MCU, DMAC0, DMAC1, CRYPTO and SPI2, The System SRAM AHB slave device interface can be accessed by MCU.

7.3.3 System SRAM Restricted Configurations Using as TCM

System SRAM0 using as TCM is configured by mcu_tcm_sel0 in SGRF_PMU. User should configure mcu_tcm_sel0[0], mcu_tcm_sel0[1], mcu_tcm_sel0[2] to 1 in sequence when enable to used as TCM and should configure mcu_tcm_sel0[2], mcu_tcm_sel0[1], mcu_tcm_sel0[0] to 0 in sequence when disable to used as TCM.
System SRAM1 using as TCM is configured by mcu_tcm_sel1 in SGRF_PMU. User should configure mcu_tcm_sel1[0], mcu_tcm_sel1[1], mcu_tcm_sel1[2] to 1 in sequence when

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enable to used as TCM and should configure mcu_tcm_sel1[2], mcu_tcm_sel1[1], mcu_tcm_sel1[0] to 0 in sequence when disable to used as TCM.
System SRAM2 using as TCM is configured by mcu_tcm_sel2 in SGRF_PMU. User should configure mcu_tcm_sel2[0], mcu_tcm_sel2[1], mcu_tcm_sel2[2] to 1 in sequence when enable to used as TCM and should configure mcu_tcm_sel2[2], mcu_tcm_sel2[1], mcu_tcm_sel2[0] to 0 in sequence when disable to used as TCM.

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Chapter 8 DMA Controller (DMAC)

8.1 Overview

RK3506 supports two Direct Memory Access (DMA) Controllers: DAMC0 and DMAC1. Both are support transfers between memory and memory, peripheral and memory. DMAC is under non-secure state after reset, and the secure state can be changed by configuring SGRF.

DMAC0 supports the following features:

- Support Trust-zone technology
- Support 12 peripheral requests
- Support up to 64bits data size
- Support 6 channels at the same time
- Support up to burst 16
- Support 4 interrupt outputs and 1 abort output
- Supports 32 MFIFO depth

Following table shows the DMAC0 request mapping scheme.

Table 8-1 DMAC0 Request Mapping Table

Request number	Source	Polarity
0	SPI0 TX/CAN0_RX/ASRC0_RX	High level
1	SPI0 RX/CAN1_RX/ASRC0_TX	High level
2	SPI1 TX/DSMC_TX/ASRC1_RX	High level
3	SPI1 RX/DSMC_RX/ASRC1_TX	High level
4	UART0 TX/CAN0_RX	High level
5	UART0 RX/CAN1_RX/PDM_RX	High level
6	UART1 TX/SPDIF_TX	High level
7	UART1 RX/SPDIF_RX	High level
8	UART2 TX/DSMC_TX/SAI0_RX	High level
9	UART2 RX/SAI0_TX	High level
10	UART3 TX/DSMC_RX/SAI1_RX	High level
11	UART3 RX/SAI1_TX	High level

DMAC1 supports the following features:

- Support Trust-zone technology
- Support 20 peripheral requests
- Support up to 64bits data size
- Support 8 channels at the same time
- Support up to burst 16
- Support 4 interrupt outputs and 1 abort output
- Support 32 MFIFO depth

Following table shows the DMAC1 request mapping scheme.

Table 8-2 DMAC1 Request Mapping Table

Request number	Source	Polarity
0	SAI0 RX	High level
1	SAI0 TX	High level
2	SAI1 RX	High level
3	SAI1 TX	High level
4	SAI2 RX	High level
5	SAI2 TX	High level
6	SAI3 TX	High level
7	SAI3 RX	High level
8	SAI4 RX	High level
9	PDM_RX	High level
10	SPDIF_TX/CAN0_RX	High level
11	SPDIF_RX/CAN1_RX	High level
12	UART4_TX	High level
13	UART4_RX	High level

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Request number	Source	Polarity
14	UART5_TX	High level
15	UART5_RX	High level
16	ASRC0 RX	High level
17	ASRC0 TX	High level
18	ASRC1 RX	High level
19	ASRC1 TX	High level

DMAC supports incrementing-address burst and fixed-address burst. But in the case of access SPI and UART at byte or half-word size, DMAC only support fixed-address burst and the address must be aligned to word.

8.2 Block Diagram

Following figure shows the block diagram of DMAC.

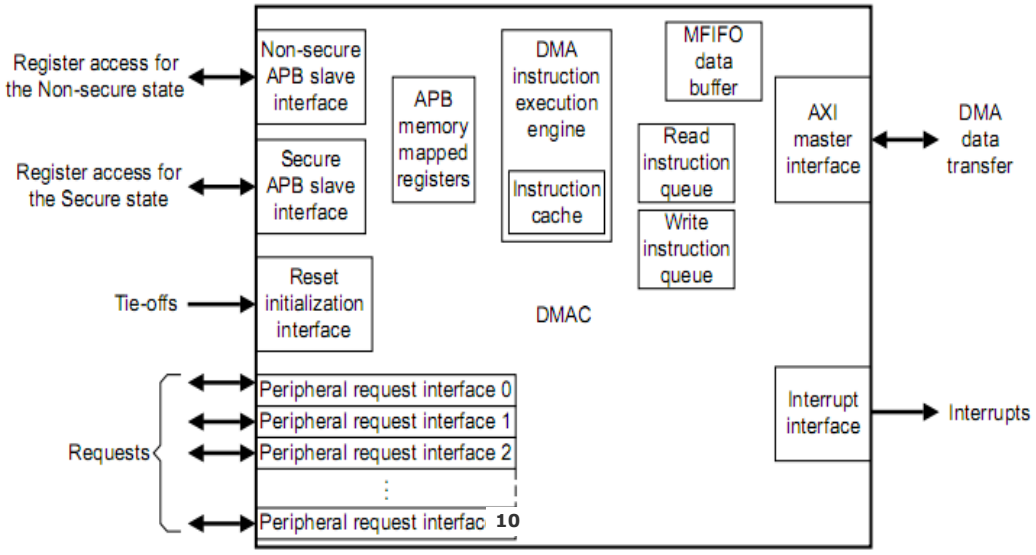

Fig. 8-1 Block diagram of DMAC

As the DMAC supports Trust-zone technology, so dual APB interfaces enable the operation of the DMAC to be partitioned into the secure state and non-secure state. You can use the APB interfaces to access status registers and also directly execute instructions in the DMAC. The default interface after reset is non-secure APB interface.

8.3 Function Description

8.3.1 Introduction

The DMAC contains an instruction processing block that enables it to process program code that controls a DMA transfer. The program code is stored in a region of system memory that the DMAC accesses using its AXI interface. The DMAC stores instructions temporarily in a cache.

DMAC0 supports 6 channels and DMAC1 supports 8 channels, each channel is capable of supporting a single concurrent thread of DMA operation. In addition, a single DMA manager thread exists, and you can use it to initialize the DMA channel threads. The DMAC executes up to one instruction for each AXI clock cycle. To ensure that it regularly executes each active thread, it alternates by processing the DMA manager thread and then a DMA channel thread. It uses a round-robin process when selecting the next active DMA channel thread to execute.

The DMAC uses variable-length instructions that consist of one to six bytes. It provides a separate Program Counter (PC) register for each DMA channel. When a thread requests an instruction from an address, the cache performs a look-up. If a cache hit occurs, then the cache immediately provides the data. Otherwise, the thread is stalled while the DMAC uses the AXI interface to perform a cache line fill. If an instruction is greater than four bytes, or spans the end of a cache line, the DMAC performs multiple cache accesses to fetch the

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instruction.
When a cache line fill is in progress, the DMAC enables other threads to access the cache, but if another cache miss occurs, this stalls the pipeline until the first line fill is complete.
When a DMA channel thread executes a load or store instruction, the DMAC adds the instruction to the relevant read or write queue. The DMAC uses these queues as an instruction storage buffer prior to it issuing the instructions on the AXI bus. The DMAC also contains a Multi First-In-First-Out (MFIFO) data buffer that it uses to store data that it reads, or writes, during a DMA transfer.

8.3.2 Operating states

Following figure shows the operating states for the DMA manager thread and DMA channel threads.

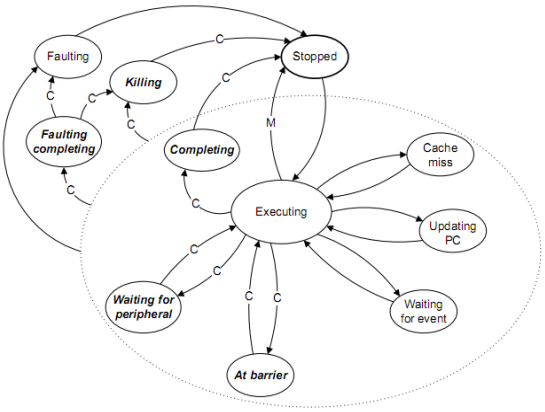

Fig. 8-2 DMAC operation states

Notes:arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:
C DMA channel threads only.
M DMA manager thread only.

8.4 Register Description

DMAC has two APB interfaces, secure APB and no-secure APB. You must ensure that you use the appropriate APB interface depending on the security state in which the boot_manager_ns initializes the DMAC to operate. Secure APB is only access-able from secure master. No-secure APB is access-able both from secure master and no-secure master.

Operational Base

Name	Base Address
DMAC0 secure APB base address	0xFF200000
DMAC0 no-secure APB base address	0xFF000000
DMAC1 secure APB base address	0xFF208000
DMAC1 no-secure APB base address	0xFF008000

8.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DMA_DSR	0x0000	W	0x00000000	DMA Manager Status Register
DMA_DPC	0x0004	W	0x00000000	DMA Program Counter Register
DMA_INTEN	0x0020	W	0x00000000	Interrupt Enable Register
DMA_EVENT_RIS	0x0024	W	0x00000000	Event-Interrupt Raw Status Register
DMA_INTMIS	0x0028	W	0x00000000	Interrupt Status Register
DMA_INTCLR	0x002c	W	0x00000000	Interrupt Clear Register

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Name	Offset	Size	Reset Value	Description
DMA_FSRD	0x0030	W	0x00000000	Fault Status DMA Manager Register
DMA_FSRC	0x0034	W	0x00000000	Fault Status DMA Channel Register
DMA_FTRD	0x0038	W	0x00000000	Fault Type DMA Manager Register
DMA_FTR0	0x0040	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR1	0x0044	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR2	0x0048	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR3	0x004c	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR4	0x0050	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR5	0x0054	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR6	0x0058	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR7	0x005c	W	0x00000000	Fault Type DMA Channel Register
DMA_CSR0	0x0100	W	0x00000000	Channel Status Registers
DMA_CPC0	0x0104	W	0x00000000	Channel Program Counter Registers
DMA_CSR1	0x0108	W	0x00000000	Channel Status Registers
DMA_CPC1	0x010c	W	0x00000000	Channel Program Counter Registers
DMA_CSR2	0x0110	W	0x00000000	Channel Status Registers
DMA_CPC2	0x0114	W	0x00000000	Channel Program Counter Registers
DMA_CSR3	0x0118	W	0x00000000	Channel Status Registers
DMA_CPC3	0x011c	W	0x00000000	Channel Program Counter Registers
DMA_CSR4	0x0120	W	0x00000000	Channel Status Registers
DMA_CPC4	0x0124	W	0x00000000	Channel Program Counter Registers
DMA_CSR5	0x0128	W	0x00000000	Channel Status Registers
DMA_CPC5	0x012c	W	0x00000000	Channel Program Counter Registers
DMA_CSR6	0x0130	W	0x00000000	Channel Status Registers
DMA_CPC6	0x0134	W	0x00000000	Channel Program Counter Registers
DMA_CSR7	0x0138	W	0x00000000	Channel Status Registers
DMA_CPC7	0x013c	W	0x00000000	Channel Program Counter Registers
DMA_SAR0	0x0400	W	0x00000000	Source Address Registers
DMA_DAR0	0x0404	W	0x00000000	Destination Address Registers
DMA_CCR0	0x0408	W	0x00000000	Channel Control Registers
DMA_LC0_0	0x040c	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_0	0x0410	W	0x00000000	Loop Counter 1 Registers

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Name	Offset	Size	Reset Value	Description
DMA_SAR1	0x0420	W	0x00000000	Source Address Registers
DMA_DAR1	0x0424	W	0x00000000	Destination Address Registers
DMA_CCR1	0x0428	W	0x00000000	Channel Control Registers
DMA_LC0_1	0x042c	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_1	0x0430	W	0x00000000	Loop Counter 1 Registers
DMA_SAR2	0x0440	W	0x00000000	Source Address Registers
DMA_DAR2	0x0444	W	0x00000000	Destination Address Registers
DMA_CCR2	0x0448	W	0x00000000	Channel Control Registers
DMA_LC0_2	0x044c	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_2	0x0450	W	0x00000000	Loop Counter 1 Registers
DMA_SAR3	0x0460	W	0x00000000	Source Address Registers
DMA_DAR3	0x0464	W	0x00000000	Destination Address Registers
DMA_CCR3	0x0468	W	0x00000000	Channel Control Registers
DMA_LC0_3	0x046c	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_3	0x0470	W	0x00000000	Loop Counter 1 Registers
DMA_SAR4	0x0480	W	0x00000000	Source Address Registers
DMA_DAR4	0x0484	W	0x00000000	Destination Address Registers
DMA_CCR4	0x0488	W	0x00000000	Channel Control Registers
DMA_LC0_4	0x048c	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_4	0x0490	W	0x00000000	Loop Counter 1 Registers
DMA_SAR5	0x04a0	W	0x00000000	Source Address Registers
DMA_DAR5	0x04a4	W	0x00000000	Destination Address Registers
DMA_CCR5	0x04a8	W	0x00000000	Channel Control Registers
DMA_LC0_5	0x04ac	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_5	0x04b0	W	0x00000000	Loop Counter 1 Registers
DMA_SAR6	0x04c0	W	0x00000000	Source Address Registers
DMA_DAR6	0x04c4	W	0x00000000	Destination Address Registers
DMA_CCR6	0x04c8	W	0x00000000	Channel Control Registers
DMA_LC0_6	0x04cc	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_6	0x04d0	W	0x00000000	Loop Counter 1 Registers
DMA_SAR7	0x04e0	W	0x00000000	Source Address Registers
DMA_DAR7	0x04e4	W	0x00000000	Destination Address Registers
DMA_CCR7	0x04e8	W	0x00000000	Channel Control Registers
DMA_LC0_7	0x04ec	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_7	0x04f0	W	0x00000000	Loop Counter 1 Registers
DMA_DBGSTATUS	0x0d00	W	0x00000000	Debug Status Register
DMA_DBGCMD	0x0d04	W	0x00000000	Debug Command Register
DMA_DBGINST0	0x0d08	W	0x00000000	Debug Instruction-0 Register
DMA_DBGINST1	0x0d0c	W	0x00000000	Debug Instruction-1 Register
DMA_CR0	0x0e00	W	0x00047051	Configuration Register 0
DMA_CR1	0x0e04	W	0x00000057	Configuration Register 1
DMA_CR2	0x0e08	W	0x00000000	Configuration Register 2
DMA_CR3	0x0e0c	W	0x00000000	Configuration Register 3

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Name	Offset	Size	Reset Value	Description
DMA_CR4	0x0e10	W	0x00000006	Configuration Register 4
DMA_CRDn	0x0e14	W	0x02094733	Configuration Register
DMA_WD	0x0e80	W	0x00000000	DMA Watchdog Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

8.4.2 Detail Register Description

DMA_DSR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9	RO	0x0	dns 1'b0: DMA manager operates in the Secure state 1'b1: DMA manager operates in the Non-secure state
8:4	RO	0x00	wakeup_event 5'b00000: event[0] 5'b00001: event[1] 5'b00010: event[2] … 5'b11111: event[31]
3:0	RO	0x0	dma_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101-4'b1110: Reserved 4'b1111: Faulting

DMA_DPC

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_mgr Program counter for the DMA manager thread

DMA_INTEN

Address: **Operational Base** + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	event_irq_select Bit [N] 1'b0: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit [N] to 0 if your system design does not use IRQ[N] to signal an interrupt request 1'b1: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets IRQ[N] HIGH. Set bit [N] to 1 if your system designer requires IRQ[N] to signal an interrupt request

DMA_EVENT_RIS

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dmasev_active Bit [N] 1'b0: Event N is inactive or IRQ[N] is LOW 1'b1: Event N is active or IRQ[N] is HIGH

DMA_INTMIS

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	irq_status Bit [N] 1'b0: Interrupt N is inactive and therefore IRQ[N] is LOW 1'b1: Interrupt N is active and therefore IRQ[N] is HIGH

DMA_INTCLR

Address: **Operational Base** + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	irq_clr Bit [N] 1'b0: The status of IRQ[N] does not change 1'b1: The DMAC sets IRQ[N] LOW if the INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of IRQ[N] does not change

DMA_FSRD

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RO	0x0	fs_mgr 1'b0: The DMA manager thread is not in the Faulting state 1'b1: The DMA manager thread is in the Faulting state

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DMA_FSRC

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	fault_status Bit [N] 1'b0: No fault is present on DMA channel N 1'b1: DMA channel N is in the Faulting or Faulting completing state

DMA_FTRD

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	Reserved
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface
29:17	RO	0x0	Reserved
16	RO	0x0	instr_fetch_err Performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response
15:6	RO	0x0	Reserved
5	RO	0x0	mgr_evnt_err 1'b0: The DMA manager has appropriate security to execute DMAWFE or DMASEV 1'b1: A DMA manager thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt
4	RO	0x0	dmago_err 1'b0: The DMA manager has appropriate security to execute DMAGO 1'b1: A DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state
3:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid The configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand

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Bit	Attr	Reset Value	Description
0	RW	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction

DMA_FTR0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	Reserved
18	RO	0x0	data_read_err Thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is a precise abort.
15:14	RO	0x0	Reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

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Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	Reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMA_FTR1

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	Reserved
18	RO	0x0	data_read_err Thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is a precise abort.
15:14	RO	0x0	Reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

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Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	Reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMA_FTR2

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	Reserved
18	RO	0x0	data_read_err Thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is a precise abort.
15:14	RO	0x0	Reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

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Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	Reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMA_FTR3

Address: **Operational Base** + offset (0x004c)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	Reserved
18	RO	0x0	data_read_err Thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is a precise abort.
15:14	RO	0x0	Reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

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Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	Reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMA_FTR4

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	Reserved
18	RO	0x0	data_read_err Thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is a precise abort.
15:14	RO	0x0	Reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

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Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	Reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMA_FTR5

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	Reserved
18	RO	0x0	data_read_err Thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is a precise abort.
15:14	RO	0x0	Reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	Reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMA_FTR6

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	Reserved
18	RO	0x0	data_read_err Thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is a precise abort.
15:14	RO	0x0	Reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	Reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMA_FTR7

Address: **Operational Base** + offset (0x005c)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface: 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	Reserved
18	RO	0x0	data_read_err Thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR or DECERR response This fault is a precise abort.
15:14	RO	0x0	Reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	Reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	Reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMA_CSR0

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	Reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	Reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event 0 or peripheral 0 5'b00001: DMA channel is waiting for event 1 or peripheral 1 5'b00010: DMA channel is waiting for event 2 or peripheral 2 … 5'b11111: DMA channel is waiting for event 31 or peripheral 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: Reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4’b1010-4’b1101: Reserved 4’b1110: Faulting completing 4’b1111: Faulting

DMA_CPC0

Address: **Operational Base** + offset (0x0104)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 0 thread

DMA_CSR1

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	Reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	Reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event 0 or peripheral 0 5'b00001: DMA channel is waiting for event 1 or peripheral 1 5'b00010: DMA channel is waiting for event 2 or peripheral 2 … 5'b11111: DMA channel is waiting for event 31 or peripheral 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: Reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4’b1010-4’b1101: Reserved 4’b1110: Faulting completing 4’b1111: Faulting

DMA_CPC1

Address: **Operational Base** + offset (0x010c)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 1 thread

DMA_CSR2

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	Reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	Reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event 0 or peripheral 0 5'b00001: DMA channel is waiting for event 1 or peripheral 1 5'b00010: DMA channel is waiting for event 2 or peripheral 2 … 5'b11111: DMA channel is waiting for event 31 or peripheral 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: Reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4’b1010-4’b1101: Reserved 4’b1110: Faulting completing 4’b1111: Faulting

DMA_CPC2

Address: **Operational Base** + offset (0x0114)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 2 thread

DMA_CSR3

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	Reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	Reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event 0 or peripheral 0 5'b00001: DMA channel is waiting for event 1 or peripheral 1 5'b00010: DMA channel is waiting for event 2 or peripheral 2 … 5'b11111: DMA channel is waiting for event 31 or peripheral 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: Reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4’b1010-4’b1101: Reserved 4’b1110: Faulting completing 4’b1111: Faulting

DMA_CPC3

Address: **Operational Base** + offset (0x011c)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 3 thread

DMA_CSR4

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	Reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	Reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event 0 or peripheral 0 5'b00001: DMA channel is waiting for event 1 or peripheral 1 5'b00010: DMA channel is waiting for event 2 or peripheral 2 … 5'b11111: DMA channel is waiting for event 31 or peripheral 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: Reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4’b1010-4’b1101: Reserved 4’b1110: Faulting completing 4’b1111: Faulting

DMA_CPC4

Address: **Operational Base** + offset (0x0124)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 4 thread

DMA_CSR5

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	Reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	Reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event 0 or peripheral 0 5'b00001: DMA channel is waiting for event 1 or peripheral 1 5'b00010: DMA channel is waiting for event 2 or peripheral 2 … 5'b11111: DMA channel is waiting for event 31 or peripheral 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: Reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4’b1010-4’b1101: Reserved 4’b1110: Faulting completing 4’b1111: Faulting

DMA_CPC5

Address: **Operational Base** + offset (0x012c)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 5 thread

DMA_CSR6

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	Reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	Reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event 0 or peripheral 0 5'b00001: DMA channel is waiting for event 1 or peripheral 1 5'b00010: DMA channel is waiting for event 2 or peripheral 2 … 5'b11111: DMA channel is waiting for event 31 or peripheral 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: Reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4’b1010-4’b1101: Reserved 4’b1110: Faulting completing 4’b1111: Faulting

DMA_CPC6

Address: **Operational Base** + offset (0x0134)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 6 thread

DMA_CSR7

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	Reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	Reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event 0 or peripheral 0 5'b00001: DMA channel is waiting for event 1 or peripheral 1 5'b00010: DMA channel is waiting for event 2 or peripheral 2 … 5'b11111: DMA channel is waiting for event 31 or peripheral 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: Reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4’b1010-4’b1101: Reserved 4’b1110: Faulting completing 4’b1111: Faulting

DMA_CPC7

Address: **Operational Base** + offset (0x013c)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 7 thread

DMA_SAR0

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 0

DMA_DAR0

Address: **Operational Base** + offset (0x0404)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the destination data for DMA channel 0

DMA_CCR0

Address: **Operational Base** + offset (0x0408)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH

Rockchip Confidencial

Bit	Attr	Reset Value	Description
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: Writes 1 byte per beat 3'b001: Writes 2 bytes per beat 3'b010: Writes 4 bytes per beat 3'b011: Writes 8 bytes per beat 3'b100: Writes 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: Reads 1 byte per beat 3'b001: Reads 2 bytes per beat 3'b010: Reads 4 bytes per beat 3'b011: Reads 8 bytes per beat 3'b100: Reads 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_0

Address: **Operational Base** + offset (0x040c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_0

Address: **Operational Base** + offset (0x0410)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR1

Address: **Operational Base** + offset (0x0420)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 1

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DMA_DAR1

Address: **Operational Base** + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the destination data for DMA channel 1

DMA_CCR1

Address: **Operational Base** + offset (0x0428)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.

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Bit	Attr	Reset Value	Description
17:15	RO	0x0	dst_burst_size 3'b000: Writes 1 byte per beat 3'b001: Writes 2 bytes per beat 3'b010: Writes 4 bytes per beat 3'b011: Writes 8 bytes per beat 3'b100: Writes 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.

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Bit	Attr	Reset Value	Description
3:1	RO	0x0	src_burst_size 3'b000: Reads 1 byte per beat 3'b001: Reads 2 bytes per beat 3'b010: Reads 4 bytes per beat 3'b011: Reads 8 bytes per beat 3'b100: Reads 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_1

Address: **Operational Base** + offset (0x042c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_1

Address: **Operational Base** + offset (0x0430)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR2

Address: **Operational Base** + offset (0x0440)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 2

DMA_DAR2

Address: **Operational Base** + offset (0x0444)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the destination data for DMA channel 2

DMA_CCR2

Address: **Operational Base** + offset (0x0448)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: Writes 1 byte per beat 3'b001: Writes 2 bytes per beat 3'b010: Writes 4 bytes per beat 3'b011: Writes 8 bytes per beat 3'b100: Writes 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.

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Bit	Attr	Reset Value	Description
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: Reads 1 byte per beat 3'b001: Reads 2 bytes per beat 3'b010: Reads 4 bytes per beat 3'b011: Reads 8 bytes per beat 3'b100: Reads 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_2

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Address: **Operational Base** + offset (0x044c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_2

Address: **Operational Base** + offset (0x0450)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR3

Address: **Operational Base** + offset (0x0460)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 3

DMA_DAR3

Address: **Operational Base** + offset (0x0464)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the destination data for DMA channel 3

DMA_CCR3

Address: **Operational Base** + offset (0x0468)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: Writes 1 byte per beat 3'b001: Writes 2 bytes per beat 3'b010: Writes 4 bytes per beat 3'b011: Writes 8 bytes per beat 3'b100: Writes 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: Reads 1 byte per beat 3'b001: Reads 2 bytes per beat 3'b010: Reads 4 bytes per beat 3'b011: Reads 8 bytes per beat 3'b100: Reads 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_3

Address: **Operational Base** + offset (0x046c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_3

Address: **Operational Base** + offset (0x0470)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR4

Address: **Operational Base** + offset (0x0480)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 4

DMA_DAR4

Address: **Operational Base** + offset (0x0484)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the destination data for DMA channel 4

DMA_CCR4

Address: **Operational Base** + offset (0x0488)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: Writes 1 byte per beat 3'b001: Writes 2 bytes per beat 3'b010: Writes 4 bytes per beat 3'b011: Writes 8 bytes per beat 3'b100: Writes 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: Reads 1 byte per beat 3'b001: Reads 2 bytes per beat 3'b010: Reads 4 bytes per beat 3'b011: Reads 8 bytes per beat 3'b100: Reads 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_4

Address: **Operational Base** + offset (0x048c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_4

Address: **Operational Base** + offset (0x0490)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR5

Address: **Operational Base** + offset (0x04a0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 5

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DMA_DAR5

Address: **Operational Base** + offset (0x04a4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the destination data for DMA channel 5

DMA_CCR5

Address: **Operational Base** + offset (0x04a8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.

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Bit	Attr	Reset Value	Description
17:15	RO	0x0	dst_burst_size 3'b000: Writes 1 byte per beat 3'b001: Writes 2 bytes per beat 3'b010: Writes 4 bytes per beat 3'b011: Writes 8 bytes per beat 3'b100: Writes 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.

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Bit	Attr	Reset Value	Description
3:1	RO	0x0	src_burst_size 3'b000: Reads 1 byte per beat 3'b001: Reads 2 bytes per beat 3'b010: Reads 4 bytes per beat 3'b011: Reads 8 bytes per beat 3'b100: Reads 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_5

Address: **Operational Base** + offset (0x04ac)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_5

Address: **Operational Base** + offset (0x04b0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR6

Address: **Operational Base** + offset (0x04c0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 6

DMA_DAR6

Address: **Operational Base** + offset (0x04c4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the destination data for DMA channel 6

DMA_CCR6

Address: **Operational Base** + offset (0x04c8)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: Writes 1 byte per beat 3'b001: Writes 2 bytes per beat 3'b010: Writes 4 bytes per beat 3'b011: Writes 8 bytes per beat 3'b100: Writes 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.

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Bit	Attr	Reset Value	Description
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: Reads 1 byte per beat 3'b001: Reads 2 bytes per beat 3'b010: Reads 4 bytes per beat 3'b011: Reads 8 bytes per beat 3'b100: Reads 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_6

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Address: **Operational Base** + offset (0x04cc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_6

Address: **Operational Base** + offset (0x04d0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR7

Address: **Operational Base** + offset (0x04e0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 7

DMA_DAR7

Address: **Operational Base** + offset (0x04e4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the destination data for DMA channel 7

DMA_CCR7

Address: **Operational Base** + offset (0x04e8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: Writes 1 byte per beat 3'b001: Writes 2 bytes per beat 3'b010: Writes 4 bytes per beat 3'b011: Writes 8 bytes per beat 3'b100: Writes 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: Reads 1 byte per beat 3'b001: Reads 2 bytes per beat 3'b010: Reads 4 bytes per beat 3'b011: Reads 8 bytes per beat 3'b100: Reads 16 bytes per beat 3'b101-3'b111: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_7

Address: **Operational Base** + offset (0x04ec)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_7

Address: **Operational Base** + offset (0x04f0)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_DBGSTATUS

Address: **Operational Base** + offset (0x0d00)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RO	0x0	dbgstatus 1'b0: Idle 1'b1: Busy

DMA_DBGCMD

Address: **Operational Base** + offset (0x0d04)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	WO	0x0	dbgcmd 2'b00: execute the instruction that the DBGINST [1:0] Registers contain 2'b01: Reserved 2'b10: Reserved 2'b11: Reserved

DMA_DBGINST0

Address: **Operational Base** + offset (0x0d08)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	instruction_byte1 Instruction byte 1
23:16	WO	0x00	instruction_byte0 Instruction byte 0
15:11	RO	0x0	Reserved
10:8	WO	0x0	channel_number 3'b000: DMA channel 0 3'b001: DMA channel 1 3'b010: DMA channel 2 … 3'b111: DMA channel 7
7:1	RO	0x0	Reserved
0	WO	0x0	debug_thread 1'b0: DMA manager thread 1'b1: DMA channel

DMA_DBGINST1

Address: **Operational Base** + offset (0x0d0c)

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Bit	Attr	Reset Value	Description
31:24	WO	0x00	instruction_byte5 Instruction byte 5
23:16	WO	0x00	instruction_byte4 Instruction byte 4
15:8	WO	0x00	instruction_byte3 Instruction byte 3
7:0	WO	0x00	instruction_byte2 Instruction byte 2

DMA_CR0

Address: **Operational Base** + offset (0x0e00)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	Reserved
21:17	RO	0x02	num_events 5'b00000: 1 interrupt output, IRQ[0] 5'b00001: 2 interrupt outputs, IRQ[1:0] 5'b00010: 3 interrupt outputs, IRQ[2:0] … 5'b11111: 32 interrupt outputs, IRQ[31:0]
16:12	RO	0x07	num_periph_req 5'b00000: 1 peripheral request interface 5'b00001: 2 peripheral request interfaces 5'b00010: 3 peripheral request interfaces … 5'b11111: 32 peripheral request interfaces
11:7	RO	0x0	Reserved
6:4	RO	0x5	num_chnls 3'b000: 1 DMA channel 3'b001: 2 DMA channels 3'b010: 3 DMA channels … 3'b111: 8 DMA channels
3	RO	0x0	Reserved
2	RO	0x0	mgr_ns_at_rst 1'b0: boot_manager_ns was LOW 1'b1: boot_manager_ns was HIGH
1	RO	0x0	boot_en 1'b0: boot_from_pc was LOW 1'b1: boot_from_pc was HIGH
0	RO	0x1	periph_req 1'b0: The DMAC does not provide a peripheral request interface 1'b1: The DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies

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DMA_CR1

Address: **Operational Base** + offset (0x0e04)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	Reserved
7:4	RO	0x5	num_i_cache_lines 4'b0000: 1 i-cache line 4'b0001: 2 i-cache lines 4'b0010: 3 i-cache lines … 4'b1111: 16 i-cache lines
3	RO	0x0	Reserved
2:0	RO	0x7	i_cache_len 3'b000-3'b001: Reserved 3'b010: 4 bytes 3'b011: 8 bytes 3'b100: 16 bytes 3'b101: 32 bytes 3'b110-3'b111: Reserved

DMA_CR2

Address: **Operational Base** + offset (0x0e08)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	boot_addr Provides the value of boot_addr[31:0] when the DMAC exited from reset

DMA_CR3

Address: **Operational Base** + offset (0x0e0c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ins Bit [N] 1'b0: Assigns event<N> or IRQ[N] to the Secure state 1'b1: Assigns event<N> or IRQ[N] to the Non-secure state

DMA_CR4

Address: **Operational Base** + offset (0x0e10)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000006	pns Bit [N] 1'b0: Assigns peripheral request interface N to the Secure state 1'b1: Assigns peripheral request interface N to the Non-secure state

DMA_CRDn

Address: **Operational Base** + offset (0x0e14)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:20	RO	0x020	data_buffer_dep 10'b000000000: 1 line 10'b000000001: 2 lines … 10'b111111111: 1024 lines
19:16	RO	0x9	rd_q_dep 4'b0000: 1 line 4'b0001: 2 lines … 4'b1111: 16 lines
15	RO	0x0	Reserved
14:12	RO	0x4	rd_cap 3'b000: 1 3'b001: 2 … 3'b111: 8
11:8	RO	0x7	wr_q_dep 4'b0000: 1 line 4'b0001: 2 lines … 4'b1111: 16 lines
7	RO	0x0	Reserved
6:4	RO	0x3	wr_cap 3'b000: 1 3'b001: 2 … 3'b111: 8
3	RO	0x0	Reserved
2:0	RO	0x3	data_width 3'b000: Reserved 3'b001: Reserved 3'b010: 32-bit 3'b011: 64-bit 3'b100: 128-bit 3'b101-3'b111: Reserved

DMA_WD

Address: **Operational Base** + offset (0x0e80)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	wd_irq_only 1'b0: The DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH 1'b1: The DMAC sets irq_abort HIGH

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8.5 Timing Diagram

Following figure shows the relationship between dma_req and dma_ack.

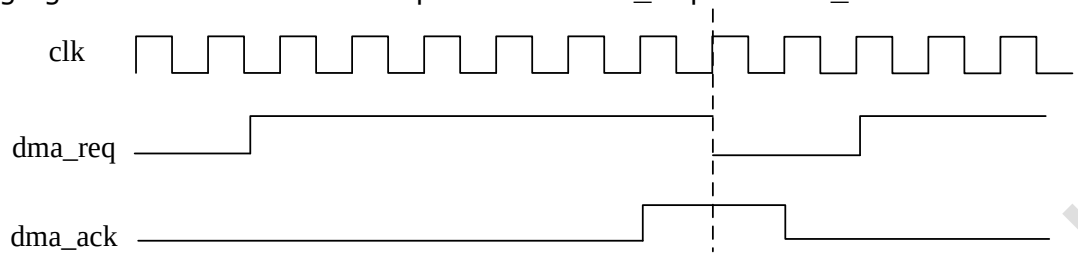

Fig. 8-3 DMAC request and acknowledge timing

8.6 Interface Description

8.6.1 DMAC boot interfaces

DMAC has the following tie-off signals. It can be configured by SGRF register. (Please refer to the chapter to find how to configure)

Table 8-3 DMAC0 boot interface

Interface	Reset value	Control source
boot_addr	0x0	Tie 0
boot_from_pc	0x0	Tie 0
boot_manager_ns	0x1	SGRF_DMAC0_CON3[0]
boot_irq_ns	0xffff	SGRF_DMAC0_CON0[11:0]
boot_periph_ns	0xffffff	SGRF_DMAC_BUS_CON1[11:0]

Table 8-4 DMAC1 boot interface

Interface	Reset value	Control source
boot_addr	0x0	Tie 0
boot_from_pc	0x0	Tie 0
boot_manager_ns	0x1	SGRF_DMAC1_CON3[0]
boot_irq_ns	0xffff	SGRF_DMAC1_CON0[15:0]
boot_periph_ns	0xffffff	{SGRF_DMAC1_CON2[3:0], SGRF_DMAC1_CON1[15:0]}

boot_addr
Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.
boot_from_pc
Controls the location in which the DMAC executes its initial instruction, after it exits from reset:
1'b0: DMAC waits for an instruction from either APB interface
1'b1: DMA manager thread executes the instruction that is located at the address from boot_addr
boot_manager_ns
When the DMAC exits from reset, this signal controls the security state of the DMA manager thread:
1'b0: Assigns DMA manager to the secure state
1'b1: Assigns DMA manager to the non-secure state
boot_irq_ns
Controls the security state of an event-interrupt resource, when the DMAC exits from reset:
If boot_irq_ns[x] is low, the DMAC assigns event<x> or IRQ[x] to the secure state.

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If boot_irq_ns[x] is high, the DMAC assigns event<x> or IRQ[x] to the non-secure state.

boot_periph_ns

Controls the security state of a peripheral request interface, when the DMAC exits from reset:

If boot_periph_ns[x] is low, the DMAC assigns peripheral request interface x to the secure state.

If boot_periph_ns[x] is high, the DMAC assigns peripheral request interface x to the non-secure state.

8.6.2 DMAC IRQ output configure

Both DMAC0 and DMAC1 have 4 interrupt outputs, the details logic refer to the table below.

Table 8-5 DMAC interrupt interface

Interface	Signal logic	maskx source
DMAC0_IRQ	|dmac0_intr[5:0]	
DMAC0_MASK0_IRQ	|((~mask0[5:0])&dmac0_intr[5:0])	GRF_SOC_CON38[5:0]
DMAC0_MASK1_IRQ	|((~mask1[5:0])&dmac0_intr[5:0])	GRF_SOC_CON38[13:8]
DMAC0_MASK2_IRQ	|((~mask2[5:0])&dmac0_intr[5:0])	GRF_SOC_CON39[5:0]
DMAC1_IRQ	|dmac1_intr[7:0]	
DMAC1_MASK0_IRQ	|((~mask0[7:0])&dmac1_intr[7:0])	GRF_SOC_CON39[15:8]
DMAC1_MASK1_IRQ	|((~mask1[7:0])&dmac1_intr[7:0])	GRF_SOC_CON40[7:0]
DMAC1_MASK2_IRQ	|((~mask2[7:0])&dmac1_intr[7:0])	GRF_SOC_CON40[15:8]

8.6.3 DMAC peripheral request

Some of the DMAC0/1 peripheral request interfaces are configure-able for selecting different source.

Table 8-6 DMAC peripheral request

Interface	Signal logic	Control source
DMAC0_CH0_REQ	SPI0 TX/CAN0_RX/ASRC0_RX	GRF_SOC_CON42[1:0]
DMAC0_CH1_REQ	SPI0 RX/CAN1_RX/ASRC0_TX	GRF_SOC_CON42[3:2]
DMAC0_CH2_REQ	SPI1 TX/DSMC_TX/ASRC1_RX	GRF_SOC_CON42[5:4]
DMAC0_CH3_REQ	SPI1 RX/DSMC_RX/ASRC1_TX	GRF_SOC_CON42[7:6]
DMAC0_CH4_REQ	UART0 TX/CAN0_RX	GRF_SOC_CON42[9:8]
DMAC0_CH5_REQ	UART0 RX/CAN1_RX/PDM_RX	GRF_SOC_CON42[11:10]
DMAC0_CH6_REQ	UART1 TX/SPDIF_TX	GRF_SOC_CON42[13:12]
DMAC0_CH7_REQ	UART1 RX/SPDIF_RX	GRF_SOC_CON42[15:14]
DMAC0_CH8_REQ	UART2 TX/DSMC_TX/SAI0_RX	GRF_SOC_CON43[1:0]
DMAC0_CH9_REQ	UART2 RX/SAI0_TX	GRF_SOC_CON43[3:2]
DMAC0_CH10_REQ	UART3 TX/DSMC_RX/SAI1_RX	GRF_SOC_CON43[5:4]
DMAC0_CH11_REQ	UART3 RX/SAI1_TX	GRF_SOC_CON43[7:6]
DMAC1_CH10_REQ	SPDIF_TX/CAN0_RX	GRF_SOC_CON43[9:8]
DMAC1_CH11_REQ	SPDIF_RX/CAN1_RX	GRF_SOC_CON43[11:10]

8.7 Application Notes

8.7.1 Using the APB slave interfaces

You must ensure that you use the appropriate APB interface, depending on the security state in which the boot_manager_ns initializes the DMAC to operate. For example, if the DMAC is in the secure state, you must issue the instruction using the secure APB interface, otherwise the DMAC ignores the instruction. You can use the secure APB interface, or the non-secure APB interface, to start or restart a DMA channel when the DMAC is in the non-secure state.

The necessary steps to start a DMA channel thread using the debug instruction registers as following:

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1. Create a program for the DMA channel.
2. Store the program in a region of system memory.
3. Poll the DBGSTATUS register to ensure that debug is idle, that is, the dbgstatus bit is 0.
4. Write to the DBGINST0 register and enter the:
- Instruction byte 0 encoding for DMAGO.
- Instruction byte 1 encoding for DMAGO.
- Debug thread bit to 0. This selects the DMA manager thread.

5. Write to the DBGINST1 register with the DMAGO instruction byte [5:2] data, see Debug Instruction-1 register description. You must set these four bytes to the address of the first instruction in the program, which was written to system memory in step 2.
6. Writing zero to the DBGCMD Register. The DMAC starts the DMA channel thread and sets the dbgstatus bit to 1.

8.7.2 Security usage

- **DMA manager thread is in the secure state**

If the DNS bit is 0, the DMA manager thread operates in the secure state and it only performs secure instruction fetches. When a DMA manager thread in the secure state processes:

DMAGO

It uses the status of the ns bit, to set the security state of the DMA channel thread by writing to the CNS bit for that channel.

DMAWFE

It halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit.

DMASEV

It sets the corresponding bit in the INT_EVENT_RIS Register, irrespective of the security state of the corresponding INS bit.

DMA manager thread is in the Non-secure state

If the DNS bit is 1, the DMA manager thread operates in the non-secure state, and it only performs non-secure instruction fetches. When a DMA manager thread in the non-secure state processes:

DMAGO

The DMAC uses the status of the ns bit, to control if it starts a DMA channel thread.
If ns = 0, the DMAC does not start a DMA channel thread and instead it:
1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager.
3. Sets the dmago_err bit in the FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

If ns = 1, the DMAC starts a DMA channel thread in the non-secure state and programs the CNS bit to be non-secure.

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it waits for the event.
If INS = 0, the event is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

If INS = 1, the event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it creates the event-interrupt.
If INS = 0, the event-interrupt resource is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the FTRD Register, see Fault Type DMA Manager Register.

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4. Moves the DMA manager to the Faulting state.
If INS = 1, the event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMA channel thread is in the secure state

When the CNS bit is 0, the DMA channel thread is programmed to operate in the secure state and it only performs secure instruction fetches.
When a DMA channel thread in the secure state processes the following instructions:

DMAWFE

The DMAC halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit, in the CR3 Register.

DMASEV

The DMAC creates the event-interrupt, irrespective of the security state of the corresponding INS bit, in the CR3 Register.

DMAWFP

The DMAC halts execution of the thread until the peripheral signals a DMA request. When this occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.

DMALDP, DMASTP

The DMAC sends a message to the peripheral to communicate that data transfer is complete, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.

DMAFLUSHP

The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.
When a DMA channel thread is in the secure state, it enables the DMAC to perform secure and non-secure AXI accesses.

- **DMA channel thread is in the Non-secure state**

When the CNS bit is 1, the DMA channel thread is programmed to operate in the non-secure state and it only performs non-secure instruction fetches.
When a DMA channel thread in the Non-secure state processes the following instructions:

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it waits for the event.
If INS = 0, the event is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
If INS = 1, the event is in the non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it creates the event.
If INS = 0, the event-interrupt resource is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
If INS = 1, the event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMAWFP

The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it

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waits for the peripheral to signal a request.
If PNS = 0, the peripheral is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
If PNS = 1, the peripheral is in the Non-secure state. The DMAC halts execution of the thread and waits for the peripheral to signal a request.

DMALDP, DMASTP

The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it sends an acknowledgement to the peripheral.
If PNS = 0, the peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
If PNS = 1, the peripheral is in the Non-secure state. The DMAC sends a message to the peripheral to communicate when the data transfer is complete.

DMAFLUSHP

The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it sends a flush request to the peripheral.
If PNS = 0, the peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
If PNS = 1, the peripheral is in the Non-secure state. The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status.
When a DMA channel thread is in the Non-secure state, and a DMAMOV CCR instruction attempts to program the channel to perform a secure AXI transaction, the DMAC:
1. Executes a DMANOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_rdwr_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel thread to the Faulting completing state.

8.7.3 Programming restrictions

Fixed unaligned bursts

The DMAC does not support fixed unaligned bursts. If you program the following conditions, the DMAC treats this as a programming error:
Unaligned read
- src_inc field is 0 in the CCRn Register
- the SARn Register contains an address that is not aligned to the size of data that the src_burst_size field contain

Unaligned write
- dst_inc field is 0 in the CCRn Register
- the DARn Register contains an address that is not aligned to the size of data that the dst_burst_size field contains

Endian swap size restrictions

If you program the endian_swap_size field in the CCRn Register, to enable a DMA channel to perform an endian swap then you must set the corresponding SARn Register and the corresponding DARn Register to contain an address that is aligned to the value that the endian_swap_size field contains.

Updating DMA channel control registers during a DMA cycle restriction

Prior to the DMAC executing a sequence of DMALD and DMAST instructions, the values you

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program in to the CCRn Register, SARn Register, and DARn Register control the data byte lane manipulation that the DMAC performs when it transfers the data from the source address to the destination address. You'd better not update these registers during a DMA cycle.

Resource sharing between DMA channels

DMA channel programs share the MFIFO data storage resource. You must not start a set of concurrently running DMA channel programs with a resource requirement that exceeds the configured size of the MFIFO. If you exceed this limit then the DMAC might lock up and generate a Watchdog abort.

8.7.4 Unaligned transfers may be corrupted

For a configuration with more than one channel, if any of channels 1 to 7 is performing transfers between certain types of misaligned source and destination addresses, then the output data may be corrupted by the action of channel 0.

Data corruption might occur if all of the following are true:

1. Two beats of AXI read data are received for one of channels 1 to 7.
2. Source and destination address alignments mean that each read data beat is splited across two lines in the data buffer (see Splitting data, below).
3. There is one idle cycle between the two read data beats.
4. Channel 0 performs an operation that updates channel control information during this idle cycle (see Updates to channel control information, below).

Splitting data

Depending upon the programmed values for the DMA transfer, one beat of read data from the AXI interface need to be splited across two lines in the internal data buffer. This occurs when the read data beat contains data bytes which will be written to addresses that wrap around at the AXI interface data width, so that these bytes could not be transferred by a single AXI write data beat of the full interface width.

Most applications of DMA-330 do not split data in this way, so are NOT vulnerable to data corruption from this defect.

The following cases are not vulnerable to data corruption because they do not split data:

- Byte lane offset between source and destination addresses is 0 when source and destination addresses have the same byte lane alignment, the offset is 0 and a wrap operation that splits data cannot occur.
- Byte lane offset between source and destination addresses is a multiple of source size.

Table 8-7 Source size in CCRn

Source size in CCRn	Allowed offset between SARn and DARn
SS8	Any offset allowed.
SS16	0,2,4,6,8,10,12,14
SS32	0,4,8,12
SS64	0,8

8.7.5 Interrupt shares between channel

As the DMAC does not record which channel (or list of channels) have asserted an interrupt. So it will depend on your program and whether any of the visible information for that program can be used to determine progress, and help identify the interrupt source.

There are 4 likely information sources that can be used to determine the progress made by a program:

- Program counter (PC)
- Source address
- Destination address
- Loop counters (LC)

For example, a program might emit an interrupt each time that it iterates around a loop. In this case, the interrupt service routine (ISR) would need to store the loop value of each channel when it is called, and then compare against the new value when it is next called. A change in value would indicate that the program has progressed.

The ISR must be carefully written to ensure that no interrupts are lost. The sequence of operations is as follows:

1. Disable interrupts

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2. Immediately clear the interrupt in DMA-330
3. Check the relevant registers for both channels to determine which must be serviced
4. Take appropriate action for the channels
5. Re-enable interrupts and exit ISR

8.7.6 Instruction sets

Table 8-8 DMAC Instruction sets

Mnemonic	Instruction	Thread usage
DMAADDH	Add Halfword	C
DMAEND	End	M/C
DMAFLUSHP	Flush and Notify Peripheral	C
DMAGO	Go	M
DMAKILL	Kill	C
DMALD	Load	C
DMALDP	Load Peripheral	C
DMALP	Loop	C
DMALPEND	Loop End	C
DMALPFE	Loop Forever	C
DMAMOV	Move	C
DMANOP	No Operation	M/C
DMARMB	Read Memory Barrier	C
DMASEV	Send Event	M/C
DMAST	Store	C
DMASTP	Store and Notify Peripheral	C
DMASTZ	Store Zero	C
DMAWFE	Wait For Event M	M/C
DMAWFP	Wait For Peripheral	C
DMAWMB	Write Memory Barrier	C
DMAADNH	Add Negative Halfword	C

Notes: Thread usage: C=DMA channel, M=DMA manager

8.7.7 Assembler directives

In this document, only DMMADNH instruction is took as an example to show the way the instruction assembled. For the other instructions, please refer to pl330_trm.pdf.

DMAADNH

Add Negative Halfword adds an immediate negative 16-bit value to the SARn Register or DARn Register, for the DMA channel thread. This enables the DMAC to support 2D DMA operations, or reading or writing an area of memory in a different order to naturally incrementing addresses. See Source Address Registers and Destination Address Registers. The immediate unsigned 16-bit value is one-extended to 32 bits, to create a value that is the two's complement representation of a negative number between -65536 and -1, before the DMAC adds it to the address using 32-bit addition. The DMAC discards the carry bit so that addresses wrap from 0xFFFFFFFF to 0x00000000. The net effect is to subtract between 65536 and 1 from the current value in the Source or Destination Address Register.
Following table shows the instruction encoding.

Table 8-9 DMAC instruction encoding

Imm[15:8]	Imm[7:0]	0	1	0	1	1	1	ra	0

Assembler syntax

DMAADNH <address_register>, <16-bit immediate>
where:
<address_register>
Selects the address register to use. It must be either:
SAR
SARn Register and sets ra to 0.
DAR
DARn Register and sets ra to 1.

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<16-bit immediate>

The immediate value to be added to the <address_register>.

You should specify the 16-bit immediate as the number that is to be represented in the instruction encoding. For example, DMAADNH DAR, 0xFFF0 causes the value 0xFFFFFFF0 to be added to the current value of the Destination Address Register, effectively subtracting 16 from the DAR.

You can only use this instruction in a DMA channel thread.

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Chapter 9 DMA2DDR

9.1 Overview

As an external memory, DDR plays an important role on SOC system. Testing DDR device, determine the DDR grain yield, to eliminate errors in data transmission is very important. Through this module mainly realize the DDR memory test, it still supports memory copy and eye diagram scanning function.

9.1.1 Features

The DMA2DDR supports the following features:

- Support one DMA channel
- Embedded a 128 bitx16 data FIFO storage space for the memory copy of the data
- Support the Word, 2 Word, 4 Word data transmitted bits wide
- Support SINGLE, INCR4, INCR8, INCR16 four bus data transmission mode
- Support data transfer complete interrupt and error interrupt
- Support test data value configuration of X, the length of X is 16 word
- Support comparison data configuration, and comparison data location configurable
- Support three kinds of method of error data processing
  - Software trigger to complete data transmission
  - Direct terminate data transmission
  - Ignore error to complete data transmission
- Support test address increasing/decreasing configurations, require transport address burst length alignment
- Support seven test pattern configuration: WW mode, W2W mode, RR mode, RC mode, RC2RC mode, RCW mode and RW mode
- Support reporting after the interruption of fault data error address, error data and error byte/word counter

9.2 Architecture

This section descripts the functions and behavior under various conditions.

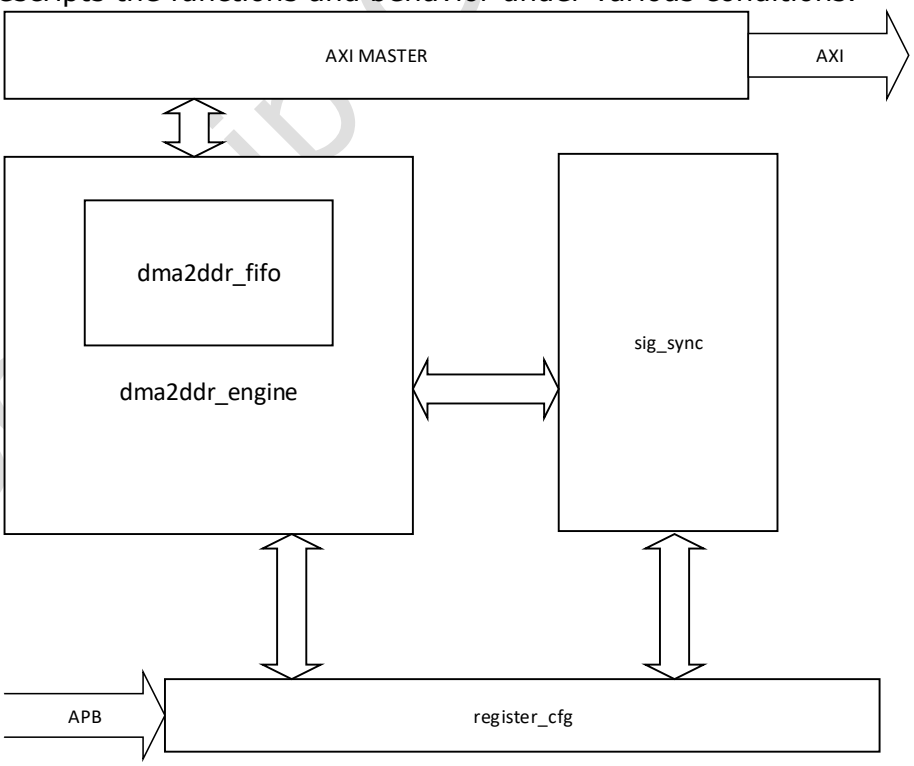

Fig. 9-1 DMA2DDR architecture

9.2.1 Block Diagram

The DMA2DDR comprises with:

- DMA2DDR register configuration block
- DMA2DDR engine block

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- DMA2DDR FIFO block
- DMA2DDR sig_sync block
- DMA2DDR axi_master block

9.2.2 Block Descriptions

DMA2DDR register configuration block

DMA2DDR register configuration block is used to configure the parameters of dma2ddr. This module includes all the registers which are necessary for dma2ddr working.

DMA2DDR engine block

DMA2DDR engine block is the main block of DMA2DDR module. According to the configured message, this module makes the corresponding data processing which test needed, it has write, read and compare functions of data process.

DMA2DDR FIFO block

The dma2ddr FIFO is used to store read data in RW mode, RC mode, RCW mode and RC2RC mode.

DMA2DDR sig_sync block

The sig_sync block is used to handle the signals from different clock domains.

DMA2DDR axi_master block

The axi_master block is used to implement the functions of the AXI master and communicate with engine block.

9.3 Register description

9.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
DMA2DDR secure base address	0x403A0000
DMA2DDR non-secure base address	0x503A0000

9.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DMA2DDR_TMODE	0x0000	W	0x00000000	Test Mode Register
DMA2DDR_TIADDR00	0x0004	W	0x00000000	Address Register 00
DMA2DDR_TIADDR01	0x0008	W	0x00000000	Address Register 01
DMA2DDR_TLENGTH0	0x000C	W	0x00000000	Length Register 0
DMA2DDR_TIADDR10	0x0014	W	0x00000000	Address Register 10
DMA2DDR_TIADDR11	0x0018	W	0x00000000	Address Register 11
DMA2DDR_TLENGTH1	0x001C	W	0x00000000	Length Register 1
DMA2DDR_WADDR0	0x0024	W	0x00000000	Write Address 0
DMA2DDR_WADDR1	0x0028	W	0x00000000	Write Address 1
DMA2DDR_TCTL	0x002C	W	0x00000000	Control Register
DMA2DDR_EDFLAG	0x0030	W	0x00000000	Error Location Register
DMA2DDR_EDLOC	0x0034	W	0x00000000	Data Location Register
DMA2DDR_EADDR0	0x0038	W	0x00000000	Current Address Register 0
DMA2DDR_EADDR1	0x003C	W	0x00000000	Current Address Register 1
DMA2DDR_EDATA0	0x0040	W	0x00000000	Current Data Register 0
DMA2DDR_EDATA1	0x0044	W	0x00000000	Current Data Register 1
DMA2DDR_EDATA2	0x0048	W	0x00000000	Current Data Register 2

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Name	Offset	Size	Reset Value	Description
DMA2DDR_EDATA3	0x004C	W	0x00000000	Current Data Register 3
DMA2DDR_INTEN	0x0050	W	0x00000000	Interrupt Enable Register
DMA2DDR_INTST	0x0054	W	0x00000000	Interrupt Status Register
DMA2DDR_INTCL	0x0058	W	0x00000000	Interrupt Clear Register
DMA2DDR_TSFT	0x005C	W	0x00000000	Soft Trigger Register
DMA2DDR_TDATA00	0x0060	W	0x00000000	Input Data Register 00
DMA2DDR_TDATA01	0x0064	W	0x00000000	Input Data Register 01
DMA2DDR_TDATA02	0x0068	W	0x00000000	Input Data Register 02
DMA2DDR_TDATA03	0x006C	W	0x00000000	Input Data Register 03
DMA2DDR_TDATA10	0x0070	W	0x00000000	Input Data Register 10
DMA2DDR_TDATA11	0x0074	W	0x00000000	Input Data Register 11
DMA2DDR_TDATA12	0x0078	W	0x00000000	Input Data Register 12
DMA2DDR_TDATA13	0x007C	W	0x00000000	Input Data Register 13
DMA2DDR_TDATA20	0x0080	W	0x00000000	Input Data Register 20
DMA2DDR_TDATA21	0x0084	W	0x00000000	Input Data Register 21
DMA2DDR_TDATA22	0x0088	W	0x00000000	Input Data Register 22
DMA2DDR_TDATA23	0x008C	W	0x00000000	Input Data Register 23
DMA2DDR_TDATA30	0x0090	W	0x00000000	Input Data Register 30
DMA2DDR_TDATA31	0x0094	W	0x00000000	Input Data Register 31
DMA2DDR_TDATA32	0x0098	W	0x00000000	Input Data Register 32
DMA2DDR_TDATA33	0x009C	W	0x00000000	Input Data Register 33
DMA2DDR_TRCDATA00	0x00A0	W	0x00000000	Background Data Register 00
DMA2DDR_TRCDATA01	0x00A4	W	0x00000000	Background Data Register 01
DMA2DDR_TRCDATA02	0x00A8	W	0x00000000	Background Data Register 02
DMA2DDR_TRCDATA03	0x00AC	W	0x00000000	Background Data Register 03
DMA2DDR_TRCDATA10	0x00B0	W	0x00000000	Background Data Register 10
DMA2DDR_TRCDATA11	0x00B4	W	0x00000000	Background Data Register 11
DMA2DDR_TRCDATA12	0x00B8	W	0x00000000	Background Data Register 12
DMA2DDR_TRCDATA13	0x00BC	W	0x00000000	Background Data Register 13
DMA2DDR_TRCDATA20	0x00C0	W	0x00000000	Background Data Register 20
DMA2DDR_TRCDATA21	0x00C4	W	0x00000000	Background Data Register 21
DMA2DDR_TRCDATA22	0x00C8	W	0x00000000	Background Data Register 22
DMA2DDR_TRCDATA23	0x00CC	W	0x00000000	Background Data Register 23
DMA2DDR_TRCDATA30	0x00D0	W	0x00000000	Background Data Register 30
DMA2DDR_TRCDATA31	0x00D4	W	0x00000000	Background Data Register 31
DMA2DDR_TRCDATA32	0x00D8	W	0x00000000	Background Data Register 32
DMA2DDR_TRCDATA33	0x00DC	W	0x00000000	Background Data Register 33
DMA2DDR_TDMAST	0x00E0	W	0x00000000	Status Register
DMA2DDR_TEN	0x00E4	W	0x00000000	Enable Register
DMA2DDR_EDBCNT	0x00E8	W	0x00000000	Data Byte Counter Register
DMA2DDR_EDBFLAG	0x00EC	W	0x00000000	Data Flag Register 0
DMA2DDR_EWCNT	0x00F0	W	0x00000000	Data Word Counter Register
DMA2DDR_EDWFLAG	0x00F4	W	0x00000000	Data Flag Register 1

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Name	Offset	Size	Reset Value	Description
DMA2DDR_TRCDATA00M	0x00F8	W	0x00000000	Background Data Location Register 00
DMA2DDR_TRCDATA01M	0x00FC	W	0x00000000	Background Data Location Register 01
DMA2DDR_TRCDATA02M	0x0100	W	0x00000000	Background Data Location Register 02
DMA2DDR_TRCDATA03M	0x0104	W	0x00000000	Background Data Location Register 03
DMA2DDR_TRCDATA10M	0x0108	W	0x00000000	Background Data Location Register 10
DMA2DDR_TRCDATA11M	0x010C	W	0x00000000	Background Data Location Register 11
DMA2DDR_TRCDATA12M	0x0110	W	0x00000000	Background Data Location Register 12
DMA2DDR_TRCDATA13M	0x0114	W	0x00000000	Background Data Location Register 13
DMA2DDR_TRCDATA20M	0x0118	W	0x00000000	Background Data Location Register 20
DMA2DDR_TRCDATA21M	0x011C	W	0x00000000	Background Data Location Register 21
DMA2DDR_TRCDATA22M	0x0120	W	0x00000000	Background Data Location Register 22
DMA2DDR_TRCDATA23M	0x0124	W	0x00000000	Background Data Location Register 23
DMA2DDR_TRCDATA30M	0x0128	W	0x00000000	Background Data Location Register 30
DMA2DDR_TRCDATA31M	0x012C	W	0x00000000	Background Data Location Register 31
DMA2DDR_TRCDATA32M	0x0130	W	0x00000000	Background Data Location Register 32
DMA2DDR_TRCDATA33M	0x0134	W	0x00000000	Background Data Location Register 33

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.3.3 Detail Registers Description

DMA2DDR_TMODE

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	tmode Test mode selection 3'b000: WW mode 3'b001: W2W mode 3'b010: RR mode 3'b011: RC mode 3'b100: RCW mode 3'b101: RW mode 3'b110: RC2RC mode

DMA2DDR_TIADDR00

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	iaddr00 Initial address0[31:0] for DMA2DDR test, this address is used for all the test modes.

DMA2DDR_TIADDR01

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	iaddr01 Initial address0[34:32] for DMA2DDR test, this address is used for all the test modes.

DMA2DDR_TLENGTH0

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tlengh0 The total test length for address0. The unit is word.

DMA2DDR_TIADDR10

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	iaddr10 Initial address1[31:0] for DMA2DDR test, this address is just used for W2W mode, RC2RC mode and RCW mode.

DMA2DDR_TIADDR11

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	iaddr11 Initial address1[34:32] for DMA2DDR test, this address is just used for W2W mode, RC2RC mode and RCW mode.

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DMA2DDR_TLENGTH1

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tlength1 The total test length for address1. The unit is word.

DMA2DDR_WADDR0

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	waddr0 Write address[31:0] for DMA2DDR test, this address is just used for RW mode.

DMA2DDR_WADDR1

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	waddr1 Write address[34:32] for DMA2DDR test, this address is just used for RW mode.

DMA2DDR_TCTL

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:7	RW	0x000000	slen The length of DMA2DDR single time. The unit is word. This register should be configured in RC2RC/W2W/RCW mode. When slen=0, it means the length equals burst length. Except for 0, the minimum value should be 2*BL*SIZE(BL is burst length which is from tburst, and SIZE is bus size which is from tsize).
6:5	RW	0x0	edctrl Error data deal method. 2'b00: Stop the transmission 2'b01: Wait the software trigger to continue the transmission 2'b10: Ignore error data until transmission done This register should be configured in RC/RC2RC/RCW mode, indicate the deal method when error data detected.
4	RW	0x0	torder The order of address arrangement. 1'b0: Ascending order 1'b1: Descending order

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	tburst Burst length of DMA2DDR in transfer. 2'b00: Single transfer 2'b01: Incremental 4 transfers 2'b10: Incremental 8 transfers 2'b11: Incremental 16 transfers
1:0	RW	0x0	tsize Byte size of DMA2DDR in transfer. 2'b00: 4(1Word) 2'b01: 8(2Word) 2'b10: 16(4Word) 2'b11: Reserved

DMA2DDR_EDFLAG

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	eflag Indicate error data location in the burst. 16'h1: Error in the first beat in this burst 16'h2: Error in the second beat in this burst 16'h4: Error in the third beat in this burst 16'h8: Error in the fourth beat in this burst 16'h10: Error in the fifth beat in this burst 16'h20: Error in the sixth beat in this burst 16'h40: Error in the seventh beat in this burst 16'h80: Error in the eighth beat in this burst 16'h100: Error in the ninth beat in this burst 16'h200: Error in the tenth beat in this burst 16'h400: Error in the eleventh beat in this burst 16'h800: Error in the twelfth beat in this burst 16'h1000: Error in the thirteenth beat in this burst 16'h2000: Error in the fourteenth beat in this burst 16'h4000: Error in the fifteenth beat in this burst 16'h8000: Error in the sixteenth beat in this burst

DMA2DDR_EDLOC

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	edloc Configured beat location which the data you needed in burst. 16'h1: Data location in the first beat in this burst 16'h2: Data location in the second beat in this burst 16'h4: Data location in the third beat in this burst 16'h8: Data location in the fourth beat in this burst 16'h10: Data location in the fifth beat in this burst 16'h20: Data location in the sixth beat in this burst 16'h40: Data location in the seventh beat in this burst 16'h80: Data location in the eighth beat in this burst 16'h100: Data location in the ninth beat in this burst 16'h200: Data location in the tenth beat in this burst 16'h400: Data location in the eleventh beat in this burst 16'h800: Data location in the twelfth beat in this burst 16'h1000: Data location in the thirteenth beat in this burst 16'h2000: Data location in the fourteenth beat in this burst 16'h4000: Data location in the fifteenth beat in this burst 16'h8000: Data location in the sixteenth beat in this burst

DMA2DDR_EADDR0

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	eaddr0 Current address[31:0] which data error detected.

DMA2DDR_EADDR1

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	eaddr1 Current address[34:32] which data error detected.

DMA2DDR_EDATA0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	edata0 Detected error data[31:0] situated in which DMA2DDR_EDLOC configured.

DMA2DDR_EDATA1

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	edata1 Detected error data[63:32] situated in which DMA2DDR_EDLOC configured.

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DMA2DDR_EDATA2

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	edata2 Detected error data[95:64] situated in which DMA2DDR_EDLOC configured.

DMA2DDR_EDATA3

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	edata3 Detected error data[127:96] situated in which DMA2DDR_EDLOC configured.

DMA2DDR_INTEN

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	cpinten Completed interrupt enable. 1'b0: Disable the interrupt 1'b1: Enable the interrupt
1	RW	0x0	reinten Error response interrupt enable. 1'b0: Disable the interrupt 1'b1: Enable the interrupt
0	RW	0x0	deinten Data error interrupt enable. 1'b0: Disable the interrupt 1'b1: Enable the interrupt

DMA2DDR_INTST

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	cpintst Completed interrupt status. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
1	RO	0x0	reintst Error response interrupt status. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

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Bit	Attr	Reset Value	Description
0	RO	0x0	deintst Data error interrupt status. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

DMA2DDR_INTCL

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	cpintcl Completed interrupt clear, write 1 clear 0.
1	W1C	0x0	reintcl Error response interrupt clear, write 1 clear 0.
0	W1C	0x0	deintcl Data error interrupt clear, write 1 clear 0.

DMA2DDR_TSFT

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	soften Software trigger DMA2DDR working when data error interrupt happened. 1'b0: Software trigger enable 1'b1: Software trigger disable

DMA2DDR_TDATA00

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata00 Input data0 bits [31:0] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA01

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata01 Input data0 bits [63:32] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA02

Address: **Operational Base** + offset (0x0068)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata02 Input data0 bits [95:64] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA03

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata03 Input data0 bits [127:96] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA10

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata10 Input data1 bits [31:0] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA11

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata11 Input data1 bits [63:32] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA12

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata12 Input data1 bits [95:64] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA13

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata13 Input data0 bits [127:96] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA20

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata20 Input data2 bits [31:0] for DMA2DDR test in WW/W2W/RCW modes.

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DMA2DDR_TDATA21

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata21 Input data2 bits [63:32] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA22

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata22 Input data2 bits [95:64] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA23

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata23 Input data2 bits [127:96] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA30

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata30 Input data3 bits [31:0] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA31

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata31 Input data3 bits [63:32] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA32

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata32 Input data3 bits [95:64] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TDATA33

Address: **Operational Base** + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata33 Input data3 bits [127:96] for DMA2DDR test in WW/W2W/RCW modes.

DMA2DDR_TRCDATA00

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata00 Background data0 bits [31:0] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA01

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata01 Background data0 bits [63:32] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA02

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata02 Background data0 bits [95:64] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA03

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata03 Background data0 bits [127:96] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA10

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata10 Background data1 bits [31:0] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA11

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata11 Background data1 bits [63:32] for RC operation in RC2RC/RC/RCW modes.

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DMA2DDR_TRCDATA12

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata12 Background data1 bits [95:64] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA13

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata13 Background data0 bits [127:96] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA20

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata20 Background data2 bits [31:0] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA21

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata21 Background data2 bits [63:32] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA22

Address: **Operational Base** + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata22 Background data2 bits [95:64] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA23

Address: **Operational Base** + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata23 Background data2 bits [127:96] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA30

Address: **Operational Base** + offset (0x00D0)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata30 Background data3 bits [31:0] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA31

Address: **Operational Base** + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata31 Background data3 bits [63:32] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA32

Address: **Operational Base** + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata32 Background data3 bits [95:64] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA33

Address: **Operational Base** + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata33 Background data3 bits [127:96] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TDMAST

Address: **Operational Base** + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	workst DMA2DDR current work status. 1'b0: DMA2DDR is idle 1'b1: DMA2DDR is busy

DMA2DDR_TEN

Address: **Operational Base** + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	R/WSC	0x0	ten DMA2DDR work enable bit. This bit should be configurable at last. It means all the DMA test registers has been configured. 1'b0: Disable 1'b1: Enable

DMA2DDR_EDBCNT

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Address: **Operational Base** + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ebcnt Indicated error data byte count only when DMA2DDR_TCTL[6:5]=2'b10.

DMA2DDR_EDBFLAG

Address: **Operational Base** + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	lbfalg Indicates data flag which right or wrong by byte unit when DMA2DDR_TCTL[6:5]=2'b10 in the whole transmission. 1'b1: Data is wrong in this byte 1'b0: Data is right in this byte

DMA2DDR_EWCNT

Address: **Operational Base** + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ewcnt Indicated error data word count only when DMA2DDR_TCTL[6:5]=2'b10.

DMA2DDR_EDWFLAG

Address: **Operational Base** + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	lwflag This register include two situation depends on DMA2DDR_TCTL[6] 1. DMA2DDR_TCTL[6]=1 Indicates data flag which right or wrong by word unit in the whole transmission. 2. DMA2DDR_TCTL[6]=0 Indicates data flag which right or wrong by word unit about current dma2ddr_edata0-dma2ddr_edata3, bit[0] mapping to dma2ddr_edata0, and so on. 1'b1: Data is wrong in this word. 1'b0: Data is right in this word.

DMA2DDR_TRCDATA00M

Address: **Operational Base** + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata00m Background data0 read compare location enable bits [31:0] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA01M

Address: **Operational Base** + offset (0x00FC)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata01m Background data0 read compare location enable bits [63:32] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA02M

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata02m Background data0 read compare location enable bits [95:64] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA03M

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata03m Background data0 read compare location enable bits [127:96] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA10M

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata10m Background data1 read compare location enable bits [31:0] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA11M

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata11m Background data1 read compare location enable bits [63:32] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA12M

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata12m Background data1 read compare location enable bits [95:64] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA13M

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata13m Background data1 read compare location enable bits [127:96] for RC operation in RC2RC/RC/RCW modes.

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DMA2DDR_TRCDATA20M

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata20m Background data2 read compare location enable bits [31:0] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA21M

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata21m Background data2 read compare location enable bits [63:32] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA22M

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata22m Background data2 read compare location enable bits [95:64] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA23M

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata23m Background data2 read compare location enable bits [127:96] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA30M

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata30m Background data3 read compare location enable bits [31:0] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA31M

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata31m Background data3 read compare location enable bits [63:32] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA32M

Address: **Operational Base** + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata32m Background data3 read compare location enable bits [95:64] for RC operation in RC2RC/RC/RCW modes.

DMA2DDR_TRCDATA33M

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata33m Background data3 read compare location enable bits [127:96] for RC operation in RC2RC/RC/RCW modes.

9.4 Application Notes

Register configuration should follow:
(1) DMA2DDR_TEN should be configured in the end.
(2) When you use different test modes, the need for a particular configuration register is important, especially DMA2DDR_TCTL register. Inappropriate configuration will lead to the transmission error, you can reference DMA2DDR instruction when using it in different test mode.

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Chapter 10 TIMER

10.1 Overview

TIMER is a programmable timer peripheral. It is usually used for generating a timing interrupt. There are two types of TIMER which are different in channel number. Both of them can be configured as a count-up or count-down timer.

TIMER supports the following features:

- Support two timer mode: free-running and user-defined
- Support two count mode: count-up and count-down
- Support configuration of loading count value
- Support mask interrupt

10.2 Block Diagram

Fig. 10-1 shows the block diagram of TIMER:

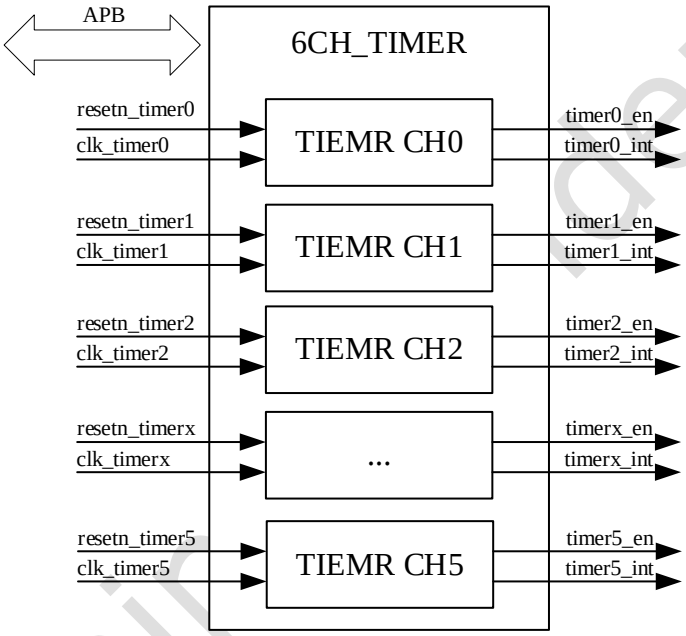

Fig. 10-1 TIMER Block Diagram

10.3 Function Description

10.3.1 TIMER Clock

The frequency of counting clock is switched between 100MHz and 24MHz.

10.3.2 Timer Mode

- **User-defined Count Mode**

TIMER loads TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_LOAD_COUNT0 registers (for count-down TIMER) or zero (for count-up TIMER) as initial value. When the TIMER counts down to 0 (for count-down TIMER) or counts up to the value in TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_LOAD_COUNT0 (for count-up TIMER), it will not automatically reload the count value register. User need to disable timer firstly and follow the programming sequence to make timer work again.

- **Free-running Count Mode**

TIMER loads the TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_COUNT0 (for count-down TIMER) or zero (for count-up TIMER) register as initial value. TIMER will automatically reload the count value register, when timer counts down to 0 (for count-down TIMER) or counts up to the value in TIMER_TIMERn_LOAD_COUNT1 and

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TIMER_TIMERn_LOAD_COUNT0 (for count-up TIMER).

10.4 Register Description

10.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
TIMER0_CH0	0xff250000
TIMER0_CH1	0xff251000
TIMER0_CH2	0xff252000
TIMER0_CH3	0xff253000
TIMER0_CH4	0xff254000
TIMER0_CH5	0xff255000
TIMER1_CH0	0xff258000
TIMER1_CH1	0xff259000
TIMER1_CH2	0xff25a000
TIMER1_CH3	0xff25b000
TIMER1_CH4	0xff25c000
TIMER1_CH5	0xff25d000

10.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TIMER_6CH_TIMERn_LOAD_COUNT0	0x0000	W	0x00000000	Low 32 bits value to be loaded into Timer0
TIMER_6CH_TIMERn_LOAD_COUNT1	0x0004	W	0x00000000	High 32 bits value to be loaded into Timer0.
TIMER_6CH_TIMERn_CURR_VALUE0	0x0008	W	0x00000000	Low 32 bits of current value of Timer0.
TIMER_6CH_TIMERn_CURR_VALUE1	0x000C	W	0x00000000	High 32 bits of current value of Timer0.
TIMER_6CH_TIMERn_CONTROL	0x0010	W	0x00000000	Timer Control Register
TIMER_6CH_TIMERn_INTSTATUS	0x0018	W	0x00000000	Timer Interrupt Status Register
TIMER_6CH_TIMERn_REVISION	0x001C	W	0x2AF60000	Timer Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.4.3 Detail Registers Description

TIMER_6CH_TIMERn_LOAD_COUNT0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count0 Load count low bits

TIMER_6CH_TIMERn_LOAD_COUNT1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count1 Load count high bits

TIMER_6CH_TIMERn_CURR_VALUE0

Address: **Operational Base** + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	current_value0 Current_cnt_low bits

TIMER_6CH_TIMERn_CURR_VALUE1

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	current_value1 Current_cnt_high bits

TIMER_6CH_TIMERn_CONTROL

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	count_mode Count mode 1'b0: Count up counter 1'b1: Count down counter
2	RW	0x0	int_en Timer interrupt enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	timer_mode Timer mode 1'b0: Free-running mode 1'b1: User-defined count mode
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

TIMER_6CH_TIMERn_INTSTATUS

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	int_pd This register contains the interrupt status for Timer. Write 1 to this register will clear the interrupt.

TIMER_6CH_TIMERn_REVISION

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x2af6	svn_revision SVN revision: 16'd10998.
15:9	RO	0x00	reserved
8	RO	0x0	ch_type Indicate the timer count mode 1'b0: Count up counter 1'b1: Count down counter
7:0	RO	0x00	reserved

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10.5 Application Notes

10.5.1 Clock and Reset

There are two different clock domain in TIMER: working clock and APB clock. The frequency of these clocks are as below:

Table 10-1 Clock Source and Frequency

Module	Clock Name	Clock Source	Frequency
TIMER0	clk_timer0	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/sai0_mclk_io_in/sai0_sclk_io_in	100M/24M/32K
	clk_timer1	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/sai1_mclk_io_in/sai1_sclk_io_in	100M/24M/32K
	clk_timer2	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/sai2_mclk_io_in/sai2_sclk_io_in	100M/24M/32K
	clk_timer3	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/sai3_mclk_io_in/sai3_sclk_io_in	100M/24M/32K
	clk_timer4	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/mclk_asrc0	100M/24M/32K
	clk_timer5	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/mclk_asrc1	100M/24M/32K
TIMER1	clk_timer0	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/sai0_mclk_io_in/sai0_sclk_io_in	100M/24M/32K
	clk_timer1	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/sai1_mclk_io_in/sai1_sclk_io_in	100M/24M/32K
	clk_timer2	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/sai2_mclk_io_in/sai2_sclk_io_in	100M/24M/32K
	clk_timer3	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/sai3_mclk_io_in/sai3_sclk_io_in	100M/24M/32K
	clk_timer4	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/mclk_asrc0	100M/24M/32K
	clk_timer5	xin_osc0_func/clk_gpll_div_100m/clk_deepslow/clk_core_pvtpll_logic/mclk_asrc1	100M/24M/32K

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Note that except for xin_osc0_func/clk_gpll_div_100m/clk_deepslow, the frequency of the other clock sources will change. Please refer to Chapter CRU for detail.
When user disables the timer enables bit (bit 0 of TIMER_TIMERn_CONTROL), the timer_en output signal is de-asserted, and timer_clk will stop. When user enables the timer, the timer_en signal is asserted and timer_clk will start running.
The application is only allowed to re-configure registers when timer_en is low.

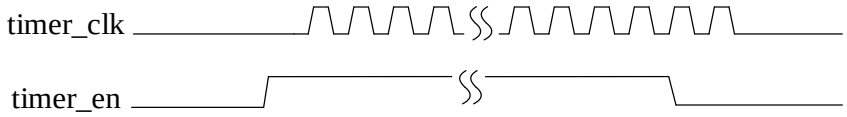

Fig. 10-2 Timing between timer_en and timer_clk

10.5.2 Programming Flow

1. Initialize the TIMER by the TIMER_TIMERn_CONTROL register:
   (1) Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
   (2) Program the timer mode—free-running or user-defined—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
   (3) Program the counting mode—count-up or count-down—by writing a "0" or "1" respectively to the count mode bit (bit 3).
   (4) Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).
2. Load the timer count value into the TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_LOAD_COUNT0 register.
3. Enable the TIMER by writing a "1" to bit 0 of TIMER_TIMERn_CONTROL.

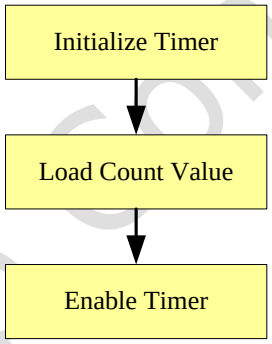

Fig. 10-3 Timer Usage Flow

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Chapter 11 HPTIMER

11.1 Overview

HPTIMER is a programmable timer peripheral which has special calibration function. This component is an APB slave device, and can provide count value for CPU directly.

HPTIMER supports the following features:

- Support three timer mode: normal mode, hardware adjust mode and software adjust mode
- Support two counting mode at normal mode: free-running and user-defined
- Support configuration of loading count value at normal mode
- Support several mask interrupts at different timer mode
- Support calibrate back to exact count value without software calculation in hardware adjust mode
- Support calibrate back to exact count value with software-aided calculation in software adjust mode
- Support common multiple configuration of slow and fast clock period
- Support providing count value for CPU use

11.2 Block Diagram

The following figure shows the block diagram of HPTIMER:

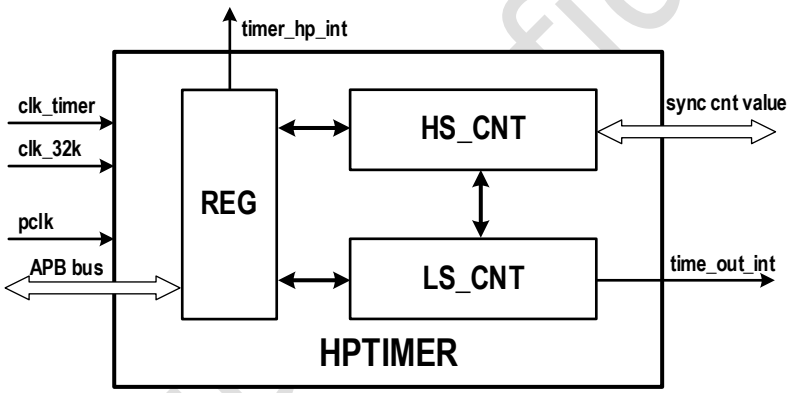

Fig. 11-1 HPTIMER Block Diagram

Register Block(REG)
This block contains several registers which are used for timer configuration, status checking and interrupt generation.
High-Speed Counter(HS_CNT)
This block contains two main counters which are working at high speed clock rate, one is used for record the current counter value that can update to CPU, the other is used to generate timing interrupt.
Low-Speed Counter(LS_CNT)
This block also contains two main counters, the different is that these counters are working at low speed clock rate, one counter is used to record the current counter value at low power mode, the other one is used as a reference counter for anti-attack.

11.3 Function Description

11.3.1 TIMER Clock

The clock frequency of clk_32k is 32KHz, and the clock frequency of clk_timer can be switched among 100MHz, 24MHz and 32KHz.

11.3.2 Timer Mode

- **Normal Mode**

At this mode, HPTIMER works as a normal incremental timer. After configuration of load count, interrupt enable, and control bit. The counter will counts from 0 to load count value step by step, and generate an interrupt when the counter value reaches the load count value. If the count mode is configured as free-running, then the counter will reload to zero,

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after reaching the load count, and begin a new counting loop.

- **Hardware Adjust Mode**

At this mode, HPTIMER works as a special incremental timer with automatic calibration by hardware.

When system is working at normal mode, the counter in high clock domain(hs_cnt) will count up normally. And the counter in low clock domain(ls_cnt) will count plus T24_GCD every T32_GCD low clock period. Since that, the hs_cnt and the ls_cnt will represent the same counter value at every T32_GCD low clock period.

When system enter low power mode, the clock frequency of hs_cnt will also switch to low frequency, but thanks to the ls_cnt, the counter value of current time will not lost. And after system recover from low power mode, the counter value of ls_cnt will automatic calibrate to hs_cnt.

- **Software Adjust Mode**

At this mode, HPTIMER works as a special incremental timer with calibration by software. Which means software can calibrate the counter value as you wish. The hardware will record the counter value when system enter to and recover from low power mode. And software should get this two begin and end counter values to calculate the lost time during the low power mode, and make a compensation to get the correct system time.

11.4 Register Description

11.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
HPTIMER_REVISION	0x0000	W	0x2AF60201	HPTIMER Version Register
HPTIMER_CTRL	0x0004	W	0x00000000	HPTIMER Control Register
HPTIMER_INTR_EN	0x0008	W	0x00000000	Interrupt Mask Register
HPTIMER_T24_GCD	0x000C	W	0x00000000	Common Multiple Divide 24MHz
HPTIMER_T32_GCD	0x0010	W	0x00000000	Common Multiple Divide 32KHz
HPTIMER_LOAD_COUNT0	0x0014	W	0x00000000	Low 32bits of load count value
HPTIMER_LOAD_COUNT1	0x0018	W	0x00000000	High 32bits of load count value
HPTIMER_T24_DELAT_COUNT0	0x001C	W	0x00000000	Low 32bits of 24MHz clock delay time count value
HPTIMER_T24_DELAT_COUNT1	0x0020	W	0x00000000	High 32bits of 24MHz clock delay time count value
HPTIMER_CURR_32K_VALUE0	0x0024	W	0x00000000	Low 32bits of current ls_cnt value
HPTIMER_CURR_32K_VALUE1	0x0028	W	0x00000000	High 32bits of current ls_cnt value
HPTIMER_CURR_TIMER_VALUE0	0x002C	W	0x00000000	Low 32bits of current hs_cnt value
HPTIMER_CURR_TIMER_VALUE1	0x0030	W	0x00000000	High 32bits of current hs_cnt value
HPTIMER_T24_32BEGIN0	0x0034	W	0x00000000	Low 32 bits of low power begin counter value
HPTIMER_T24_32BEGIN1	0x0038	W	0x00000000	High 32 bits of low power begin counter value
HPTIMER_T32_24END0	0x003C	W	0x00000000	Low 32 bits of low power end counter value
HPTIMER_T32_24END1	0x0040	W	0x00000000	High 32 bits of low power end counter value
HPTIMER_RECORD_VALUE_VALID	0x0044	W	0x00000000	Record count value valid
HPTIMER_SYNC_REQ	0x0048	W	0x00000000	Synchronize request control
HPTIMER_INTR_STATUS	0x004C	W	0x00000000	Interrupt Status Register

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Name	Offset	Size	Reset Value	Description
HPTIMER_CURR_ATATK_32K_VALUE0	0x0054	W	0x00000000	Low 32bits of current ATATK counter value
HPTIMER_CURR_ATATK_32K_VALUE1	0x0058	W	0x00000000	High 32bits of current ATATK counter value
HPTIMER_LOAD_COUNT0_32K	0x005C	W	0x00000000	Low 32bits of load count 32k value
HPTIMER_LOAD_COUNT1_32K	0x0060	W	0x00000000	High 32bits of load count 32k value
HPTIMER_CURR_COMP_H_VALUE0	0x0064	W	0x00000000	Low 32bits of hs_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_H_VALUE1	0x0068	W	0x00000000	High 32bits of hs_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_L_VALUE0	0x006C	W	0x00000000	Low 32bits of ls_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_L_VALUE1	0x0070	W	0x00000000	High 32bits of ls_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_H_32K_VALUE0	0x0074	W	0x00000000	Low 32bits of hs_cnt value when compensation enable
HPTIMER_CURR_COMP_H_32K_VALUE1	0x0078	W	0x00000000	High 32bits of hs_cnt value when compensation enable
HPTIMER_CURR_COMP_L_32K_VALUE0	0x007C	W	0x00000000	Low 32bits of ls_cnt value when compensation enable
HPTIMER_CURR_COMP_L_32K_VALUE1	0x0080	W	0x00000000	High 32bits of ls_cnt value when compensation enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.2 Detail Registers Description

HPTIMER_REVISION

Address: Operational Base(0xFF980000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x2af6	svn_revision SVN revision 16'd10998
15:10	RO	0x00	reserved
9:8	RO	0x2	ch_type Channel 0 is a low power recovery self-correction count up counter.
7:0	RO	0x01	ip_function IP function. 16'd1

HPTIMER_CTRL

Address: Operational Base(0xFF980000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable of the lower 16bit 1'b0: Disable 1'b1: Enable
15:8	RO	0x00	reserved
7	RW	0x0	hs_cnt_auto_hold Auto hold the hs_cnt at hard ware adjust mode when system enter low power mode 1'b0: Disable auto hold 1'b1: Enable auto hold

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Bit	Attr	Reset Value	Description
6	RW	0x0	hp_init_mode Control the hs_cnt initial mode 1'b0: hs_cnt will begin count together with ls_cnt 1'b1: hs_cnt will not wait for ls_cnt
5	RW	0x0	extra_cnt_ctrl Control the extra counter 1'b0: Disable 1'b1: Enable
4	RW	0x0	atatk_cnt_ctrl Control the anti-attack counter 1'b0: Enable 1'b1: Disable
3	RW	0x0	count_mode Timer count mode 1'b0: Free-running mode 1'b1: User-defined count mode
2:1	RW	0x0	timer_mode Select timer as which timer mode 2'b00: Normal timer 2'b01: Adjust timer with hardware adjust 2'b10: Adjust timer with software adjust
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

HPTIMER_INTR_EN

Address: Operational Base(0xFF980000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	extra_count_reach_intr_en Extra timer count reach load_count interrupt enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	count_reach_32k_intr_en Low speed count reach interrupt enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	sync_done_intr_en Synchronization done interrupt enable 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	count_reach_intr_en High speed count reach load_count interrupt enable 1'b0: Disable 1'b1: Enable

HPTIMER_T24_GCD

Address: Operational Base(0xFF980000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_gcd The least common multiple of 24MHz (100MHz) and 32KHz clock cycles divided by 24MHz (100MHz) clock cycles.

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HPTIMER_T32_GCD

Address: Operational Base(0xFF980000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t32_gcd The least common multiple of 24MHz (100MHz) and 32KHz clock cycles divided by 32KHz clock cycles.

HPTIMER_LOAD_COUNT0

Address: Operational Base(0xFF980000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count0 Low 32bits of load count value.

HPTIMER_LOAD_COUNT1

Address: Operational Base(0xFF980000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count1 High 32bits of load count value.

HPTIMER_T24_DELAT_COUNT0

Address: Operational Base(0xFF980000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_delay_time_count0 Low 32bits of 24MHz clock delay time count value.

HPTIMER_T24_DELAT_COUNT1

Address: Operational Base(0xFF980000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_delay_time_count1 High 32bits of 24MHz clock delay time count value.

HPTIMER_CURR_32K_VALUE0

Address: Operational Base(0xFF980000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_32k_value0 Low 32bits of current ls_cnt value.

HPTIMER_CURR_32K_VALUE1

Address: Operational Base(0xFF980000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_32k_value1 High 32bits of current ls_cnt value.

HPTIMER_CURR_TIMER_VALUE0

Address: Operational Base(0xFF980000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value0 Low 32bits of current hs_cnt value.

HPTIMER_CURR_TIMER_VALUE1

Address: Operational Base(0xFF980000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value1 High 32bits of current hs_cnt value.

HPTIMER_T24_32BEGIN0

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Address: Operational Base(0xFF980000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t24_32begin0 Low 32 bits of hs_cnt value when 24MHz (100MHz) clock switches to 32KHz clock.

HPTIMER_T24_32BEGIN1

Address: Operational Base(0xFF980000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t24_32begin1 High 32 bits of hs_cnt value when 24MHz (100MHz) clock switches to 32KHz clock.

HPTIMER_T32_24END0

Address: Operational Base(0xFF980000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t32_24end0 Low 32 bits of hs_cnt value when 32KHz clock switches to 24MHz (100MHz) clock.

HPTIMER_T32_24END1

Address: Operational Base(0xFF980000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t32_24end1 High 32 bits of hs_cnt value when 32KHz clock switches to 24MHz (100MHz) clock.

HPTIMER_RECORD_VALUE_VALID

Address: Operational Base(0xFF980000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	W1C	0x0	curr_comp_value_32k_valid CURR_COMP_*_32K_VALUE valid 1'b0: Invalid 1'b1: Valid
2	W1C	0x0	curr_comp_value_valid CURR_COMP_*_VALUE valid 1'b0: Invalid 1'b1: Valid
1	W1C	0x0	t32_24end_valid T32_24END value valid 1'b0: Invalid 1'b1: Valid
0	W1C	0x0	t24_32begin_valid T24_32BEGIN value valid 1'b0: Invalid 1'b1: Valid

HPTIMER_SYNC_REQ

Address: Operational Base(0xFF980000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable of the lower 16bit 1'b0: Disable 1'b1: Enable
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	hw_sync_disable 1'b0: Enable synchronization 1'b1: Disable synchronization When this bit is set to 1'b1, than no matter the value of hs_cnt and ls_cnt, the synchronization will not be executed.
8	RW	0x0	hw_sync_en Control the sync logic of hs_cnt 1'b0: Disable 1'b1: Enable When enable this bit, hardware will record the value of hs_cnt and ls_cnt at the time that a hw_sync_req occurs. And if the value of hs_cnt is larger than ls_cnt, then the synchronization to hs_cnt will not be executed.
7	RO	0x0	reserved
6	RW	0x0	hw_sync_compensation_en Enable the compensation to ls_cnt after a hw_sync_req occurs, the hardware will compare the value of hs_cnt and ls_cnt, if hs_cnt is larger than ls_cnt, then the different will be compensated to ls_cnt. 1'b0: Disable 1'b1: Enable
5	RW	0x0	low_power_compensation_en Enable the compensation to ls_cnt at the time that system enter the low power state, the hardware will compare the value of hs_cnt and ls_cnt, if hs_cnt is larger than ls_cnt, then the different will be compensated to ls_cnt. 1'b0: Disable 1'b1: Enable
4	RW	0x0	compensation_en Control the compensation logic of ls_cnt 1'b0: Disable 1'b1: Enable When enable this bit, hardware will record the value of hs_cnt and ls_cnt at the time that system enter low power state.
3:2	RO	0x0	reserved
1	R/WSC	0x0	hw_sync_req Hs_cnt synchronize request by hardware, which means synchronize hs_cnt by ls_cnt value
0	R/WSC	0x0	sw_sync_req Hs_cnt synchronize request by software, which means directly compensate T24_DELAT_COUNT to hs_cnt

HPTIMER_INTR_STATUS

Address: Operational Base(0xFF980000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	W1C	0x0	extra_count_reach Extra cnt reach the load count value
3	W1C	0x0	count_reach_32k Ls_cnt counter value is more than load_count_32k-t24_gcd, and less than load_count_32k
2	W1C	0x0	sync_done hs_cnt synchronization done
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	W1C	0x0	count_reach Normal counter: hs_cnt reach load_count value

HPTIMER_CURR_ATATK_32K_VALUE0

Address: Operational Base(0xFF980000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	current_atatk_32k_value0 Low 32bits of current atatk_cnt_32k value.

HPTIMER_CURR_ATATK_32K_VALUE1

Address: Operational Base(0xFF980000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	current_atatk_32k_value1 High 32bits of current atatk_cnt_32k value.

HPTIMER_LOAD_COUNT0_32K

Address: Operational Base(0xFF980000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count0_32k Low 32bits of load count 32k value.

HPTIMER_LOAD_COUNT1_32K

Address: Operational Base(0xFF980000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count1_32k High 32bits of load count 32k value.

HPTIMER_CURR_COMP_H_VALUE0

Address: Operational Base(0xFF980000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_value0 Low 32bits of curr_comp_h_value, which indicate the record value of hs_cnt when a hw_sync_req occurs.

HPTIMER_CURR_COMP_H_VALUE1

Address: Operational Base(0xFF980000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_value1 High 32bits of curr_comp_h_value, which indicate the record value of hs_cnt when a hw_sync_req occurs.

HPTIMER_CURR_COMP_L_VALUE0

Address: Operational Base(0xFF980000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_value0 Low 32bits of curr_comp_l_value, which indicate the record value of ls_cnt when a hw_sync_req occurs.

HPTIMER_CURR_COMP_L_VALUE1

Address: Operational Base(0xFF980000) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_value1 High 32bits of curr_comp_l_value, which indicate the record value of ls_cnt when a hw_sync_req occurs.

HPTIMER_CURR_COMP_H_32K_VALUE0

Address: Operational Base(0xFF980000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_32k_value0 Low 32bits of curr_comp_h_32k_value, which indicate the record value of hs_cnt when system enter the low power state.

HPTIMER_CURR_COMP_H_32K_VALUE1

Address: Operational Base(0xFF980000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_32k_value1 High 32bits of curr_comp_h_32k_value, which indicate the record value of hs_cnt when system enter the low power state.

HPTIMER_CURR_COMP_L_32K_VALUE0

Address: Operational Base(0xFF980000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_32k_value0 Low 32bits of curr_comp_l_32k_value, which indicate the record value of ls_cnt when system enter the low power state.

HPTIMER_CURR_COMP_L_32K_VALUE1

Address: Operational Base(0xFF980000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_32k_value1 High 32bits of curr_comp_l_32k_value, which indicate the record value of ls_cnt when system enter the low power state.

11.5 Application Notes

11.5.1 Clock and Reset

There are two different clock domains in HPTIMER: clk_timer, clk_32k. The frequency of these clocks are as below:

Table 11-1 Clock Frequency

Clock Name	Clock Source
clk_timer	100M/24M/32KHz
clk_32k	32KHz

The clock clk_timer can switch to three different frequencies according to different mode. In normal working mode, HPTIMER is working at 100MHz or 24MHz, and the exact working frequency is depending on user needs. In low power mode, HPTIMER is working at 32K. hp_sel is clock control bit to switch between 100MHz and 24MHz, which is related to CRU_PMUCLKSEL_CON00. And lp_ena is clock control bit to switch between 100M/24MHz and 32KHz, which is related to PMU_CRU_PWR_CON0[14].

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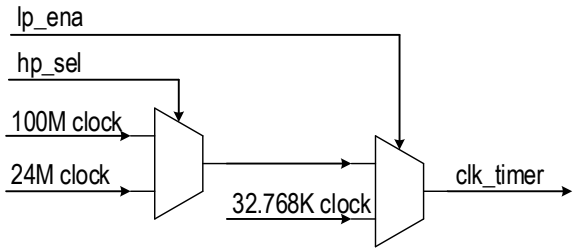

Fig. 11-2 Clock Selection of clk_timer

Please refer to chapter CRU and GRF for detail.

11.5.2 Programming Flow

- **Normal Mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x0 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Load the HPTIMER count value into the HPTIMER_LOAD_COUNT1 and HPTIMER_LOAD_ COUNT0 register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.

If you want to do another count, repeat steps 1 to 3. These bits need to be written with the corresponding write enable bit in the higher 16 bits set to "1", as described in section 1.4.

- **Hardware Adjust Mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x1 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Initialize the HPTIMER by the HPTIMER_INTR_STATUS register. Write 0x1d to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.
3. Configure the HPTIMER GCD register.
   (1) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_timer clock cycle and configure it in HPTIMER_T24_GCD register.
   (2) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_32k clock cycle and configure it in HPTIMER_T32_GCD register.
4. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
5. Configure the PMU_CRU_PWR_CON0 to assert lp_ena before the chip enters low power consumption mode.
6. The chip enters and exits the low power consumption mode at any time in between.
7. Configure the PMU_CRU_PWR_CON0 to de-assert lp_ena after the chip exits low power consumption mode.
8. Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the HPTIMER count is adjusted.
9. Write 0x4 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 6 to 9. Some bits need to be written with the corresponding write enable bit in the higher 16 bits set to "1", as described in section 1.4.

- **Software Adjust Mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.

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(2) Program the timer mode, normal mode by writing a 0x2 to the timer mode bits (bit 1 to bit 2).
(3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).

2. Initialize the HPTIMER by the HPTIMER_INTR_STATUS and BEGIN_END_VALID register. Write 0x1d to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register. write 0x3 to RECORD_VALUE_VALID register to clear RECORD_VALUE_VALID register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
4. Configure the PMU0GRF to assert lp_ena before the chip enters low power consumption mode.
5. The chip enters and exits the low power consumption mode at any time in between.
6. Configure the PMU0GRF to deassert lp_ena after the chip exits low power consumption mode.
7. Read out RECORD_VALUE_VALID register until the value of it is 0x3, which indicates that the chip has entered and exited the low power consumption mode, then you can adjust the timer count value. Then write 0x3 to RECORD_VALUE_VALID register to clear the register.
8. The count value of HPTIMER compensation.
   (1) Read out HPTIMER_T24_32BEGIN1, TIMER_ HP_T24_32BEGIN0, HPTIMER_T32_ 24END1 and HPTIMER_T32_24END0 register.
   (2) configure HPTIMER_T24_DELAT_COUNT1 and HPTIMER_T24_DELAT_COUNT0 registers to compensate for the count values according to the values of these registers read out above.
   (3) Write 0x1 to HPTIMER_SYNC_REQ register to start compensation counting.
   (4) Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the compensation count is completed.
9. Write 0x5 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 5 to 8. Some bits need to be written with the corresponding write enable bit in the higher 16 bits set to "1", as described in section 1.4.

- **Hardware Compensation Configuration**

The hardware compensation configurations are all related to the HPTIMER_SYNC_REQ register.

1. When compensation_en(bit 4) of HPTIMER_SYNC_REQ is asserted, then the hardware will record the value of hs_cnt and ls_cnt at the time that system enters low power mode, and the record value will be stored at HPTIMER_CURR_COMP_*_32K_VALUE.
2. When low_power_compensation_en(bit 5) of HPTIMER_SYNC_REQ is asserted, then the hardware will compare the value of hs_cnt and ls_cnt at the time that system enters low power mode. And if hs_cnt is greater than ls_cnt at this time, the different will be compensated to ls_cnt.
3. When hw_sync_compensation_en(bit 6) of HPTIMER_SYNC_REQ is asserted, then the hardware will compare the value of hs_cnt and ls_cnt at the time that hardware synchronization occurs. And if hs_cnt is larger than ls_cnt at this time, the different will be compensated to ls_cnt.
4. When hw_sync_en(bit 7) of TIMRE_HP_SYNC_REQ is asserted, then the hardware will record the value of hs_cnt and ls_cnt at the time that hardware synchronization occurs, and the record value will be stored at HPTIMER_CURR_COMP_*_VALUE. The other hand, if the value of hs_cnt is greater than ls_cnt，then the synchronization to hs_cnt will not be executed.
5. When hw_sync_disable(bit 8) of HPTIMER_SYNC_REQ is asserted, then no matter the value of hs_cnt and ls_cnt, the synchronization will not be executed.

- **Low Power Mode Wakeup**

This function is used at hardware adjust mode, the programing flow is mainly as hardware adjust mode.

1. Configure HPTIMER to hardware adjust mode.

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2. Configure the HPTIMER GCD register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
4. Prepare to enter low power mode:
   (1) Configure PMU to set HPTIMER as wake up source.
   (2) Configure the bit 3 of HPTIMER_INTR_EN to set count reach interrupt enable at 32K.
   (3) Configure the HPTIMER_LOAD_COUNT1_32K and HPTIMER_LOAD_COUNT0_32K to set the wake up time. (note that user must configure HPTIMER_LOAD_COUNT0_32K at last)
5. Configure the PMU0GRF to assert lp_ena before the chip enters low power consumption mode.
6. Wait for HPTIMER to wake up system.
7. Configure the PMU0GRF to de-assert lp_ena after the chip exits low power consumption mode.
8. Read out the INTR_STATUS register and write 0x8 to HPTIMER_INTR_STATUS register to clear count reach 32k interrupt.
9. Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the HPTIMER count is adjusted.
10. Write 0x4 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 4 to 10.

- **High Performance Timing Interrupt**

HPTIMER provides a 32-bits High performance counter to generate timing interrupt at hardware adjust mode.

1. Configure HPTIMER to hardware adjust mode.
2. Configure the HPTIMER_LOAD_COUNT0 to set the load count.
3. Configure bit 4 of HPTIMER_INTR_EN to enable interrupt.
4. Configure bit 5 of HPTIMER_CTRL to enable the hyper performance counter to work.
5. Wait for the interrupt generate.
6. Write '1' to bit 4 of HPTIMER_INTR_STATUS to clear the interrupt status.

When the count mode of timer is configured to free-running, then the interrupt will assert every load count time, otherwise the interrupt will generate only one time.

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Chapter 12 Watchdog Timer (WDT)

12.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that caused by conflicting parts or programs in a SOC. The WDT would generate interrupt or reset signal when its counter reaches zero, then a reset controller would reset the system.

WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock can be chosen from 24MHz or 32KHz clock
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined ranges of main timeout period
- There are 2 WDTs: WDT0/1
- All the 2 WDTs can drive CRU to generate global software reset

12.2 Block Diagram

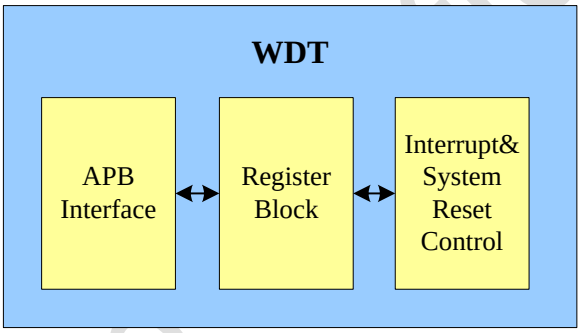

Fig. 12-1 WDT Block Diagram

WDT comprises with:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & System Reset Control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

12.3 Function Description

12.3.1 Operation

Counter

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR).

Interrupts

The WDT can be programmed to generate an interrupt (and then a system reset) when a

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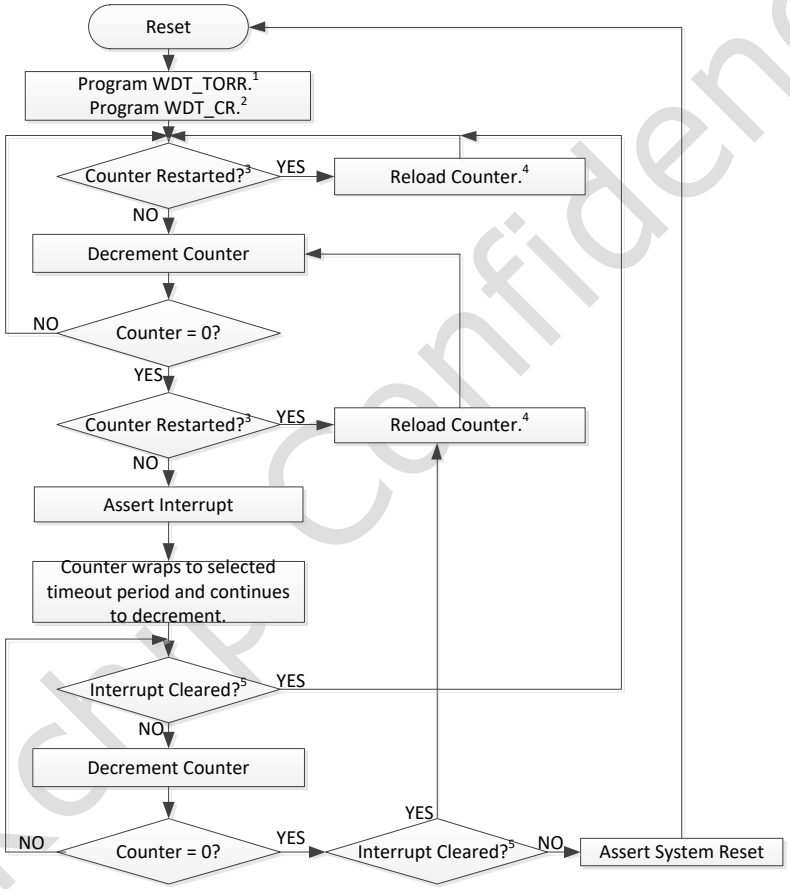
timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

System Resets
When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

Reset Pulse Length
The reset pulse length is the number of APB clock cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

12.3.2 Programming Sequence



1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 12-2 WDT Operation Flow (RMOD=1)

12.4 Register Description

12.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
WDT0	0xFF260000
WDT1	0xFF268000

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12.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
WDT_CR	0x0000	W	0x00000008	Control Register
WDT_TORR	0x0004	W	0x00000000	Timeout Range Register
WDT_CCVR	0x0008	W	0x0000FFFF	Current Counter Value Register
WDT_CRR	0x000C	W	0x00000000	Counter Restart Register
WDT_STAT	0x0010	W	0x00000000	Interrupt Status Register
WDT_EOI	0x0014	W	0x00000000	Interrupt Clear Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

12.4.3 Detail Registers Description

WDT_CR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x2	rst_pluse_length This is used to select the number of APB clock cycles for which the system reset stays asserted. 3'b000: 2 pclk cycles 3'b001: 4 pclk cycles 3'b010: 8 pclk cycles 3'b011: 16 pclk cycles 3'b100: 32 pclk cycles 3'b101: 64 pclk cycles 3'b110: 128 pclk cycles 3'b111: 256 pclk cycles
1	RW	0x0	resp_mode Selects the output response generated to a timeout. 1'b0: Generate a system reset. 1'b1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset.
0	RW	0x0	en This bit is used to enable and disable the WDT. When disabled, the counter does not decrement. Thus, no interrupt or system reset are generated. Once this bit has been enabled, it can be cleared only by a system reset. 1'b0: WDT disabled. 1'b1: WDT enabled.

WDT_TORR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	timeout_period This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values available for a 32-bit watchdog counter are: 4'b0000: 0x0000ffff 4'b0001: 0x0001ffff 4'b0010: 0x0003ffff 4'b0011: 0x0007ffff 4'b0100: 0x000fffff 4'b0101: 0x001fffff 4'b0110: 0x003fffff

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Bit	Attr	Reset Value	Description
			4'b0111: 0x007fffff 4'b1000: 0x00ffffff 4'b1001: 0x01ffffff 4'b1010: 0x03ffffff 4'b1011: 0x07ffffff 4'b1100: 0x0fffffff 4'b1101: 0x1fffffff 4'b1110: 0x3fffffff 4'b1111: 0x7fffffff

WDT_CCVR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000ffff	cur_cnt This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read.

WDT_CRR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	cnt_restart This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

WDT_STAT

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	status This register shows the interrupt status of the WDT. 1'b1: Interrupt is active regardless of polarity. 1'b0: Interrupt is inactive.

WDT_EOI

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	int_clr This can be used to clear the interrupt without restarting the watchdog counter.

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Chapter 13 Mailbox

13.1 Overview

The Mailbox module is a simple APB peripheral that allows MCU and CPU to communicate with each other by writing operation to generate interrupt. The registers are accessible via APB interface.
The Mailbox has the following main features:

- Support APB interface
- Support 4 mailbox groups, each group includes one data word, one command word register and one flag bit that can represent one interrupt
- Support interrupts to MCU and CPU
- Support two type of interrupt: TX done and RX done
- Support two trigger mode for TX done interrupt

13.2 Block Diagram

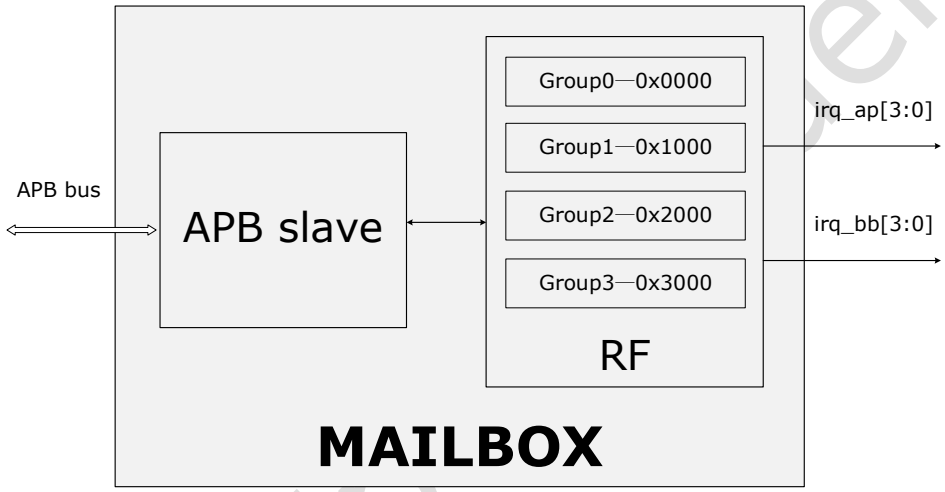

Fig. 13-1 Mailbox Block Diagram

13.3 Function Description

13.3.1 TX Done Interrupt

- Regard CPU as the "AP" side of the Mailbox. The 4 groups TX done interrupt to CPU is:
  - Enabled when MAILBOX_B2A_INTEN.b2a_tx_done_inten is set to 1 and the corresponding IRQ is enabled in GIC of CPU.
  - Generated when
    - there are writing operation to corresponding MAILBOX_B2A_CMD_i and MAILBOX_B2A_DAT_i orderly in normal mode.
    - there are writing operation to corresponding MAILBOX_B2A_CMD_i in fast trigger mode.
  - Cleared when writing 1 to corresponding MAILBOX_B2A_STATUS.b2a_tx_done_int.
- Regard MCU as the "BB" side of the Mailbox. The 4 groups TX done interrupt to MCU is:
  - Enabled when MAILBOX_A2B_INTEN.a2b_tx_done_inten is set to 1 and the corresponding IRQ is enabled in INTC of MCU.
  - Generated when
    - there are writing operation to corresponding MAILBOX_A2B_CMD_i and MAILBOX_A2B_DAT_i orderly.
    - there are writing operation to corresponding MAILBOX_A2B_CMD_i in fast

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trigger mode.
- Cleared when writing 1 to corresponding MAILBOX_A2B_STATUS.a2b_tx_done_int.

13.3.2 RX Done Interrupt

- Regard CPU as the "AP" side of the Mailbox. The 4 groups RX done interrupt to CPU is:
  - Enabled when MAILBOX_B2A_INTEN.b2a_rx_done_inten is set to 1 and the corresponding IRQ is enabled in GIC of CPU.
  - Generated when "BB" side clear the corresponding TX done interrupt by write 1 to MAILBOX_A2B_STATUS.a2b_tx_done_int.
  - Cleared when writing 1 to the corresponding MAILBOX_B2A_STATUS.b2a_rx_done_int.
- Regard MCU as the "BB" side of the Mailbox. The 4 groups RX done interrupt to MCU is:
  - Enabled when MAILBOX_A2B_INTEN.a2b_rx_done_inten is set to 1 and the corresponding IRQ is enabled in INTC of MCU.
  - Generated when "AP" side clear the corresponding TX done interrupt by write 1 to MAILBOX_B2A_STATUS.b2a_tx_done_int.
  - Cleared when writing 1 to the corresponding MAILBOX_A2B_STATUS.a2b_rx_done_int.

- You can also regard CPU as the "BB" side of the Mailbox and regard MCU as the "AP" side of the Mailbox. The configuration flow is similar.
- Note that there are two ways for MAILBOX's interrupt to reach the MCU:
  - The interrupt is sent to the MCU through INTMUX, which needs to be configured accordingly. For details, see Cortex-M0 Chapter.
  - Interrupts are sent to the MCU via the GRF-controlled mux by selecting 1 of 8 (four interrupts each for AP and BB). For details, see SOC_CON13 in the General Register Files (GRF) Chapter.

13.4 Register Description

13.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
MAILBOX_CH0	0xFF290000
MAILBOX_CH1	0xFF291000
MAILBOX_CH2	0xFF292000
MAILBOX_CH3	0xFF293000

13.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MAILBOX_A2B_INTEN	0x0000	W	0x00000100	AP to BB Interrupt Enable Register for Groupx
MAILBOX_A2B_STATUS	0x0004	W	0x00000000	AP to BB Interrupt Status Register for Groupx
MAILBOX_A2B_CMD	0x0008	W	0x00000000	AP to BB Command x Register
MAILBOX_A2B_DATA	0x000C	W	0x00000000	AP to BB Data x Register
MAILBOX_B2A_INTEN	0x0010	W	0x00000100	BB to AP Interrupt Enable Register for Groupx
MAILBOX_B2A_STATUS	0x0014	W	0x00000000	BB to AP Interrupt Status Register for Groupx
MAILBOX_B2A_CMD	0x0018	W	0x00000000	BB to AP Command x Register
MAILBOX_B2A_DATA	0x001C	W	0x00000000	BB to AP Data x Register

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.3 Detail Registers Description

MAILBOX_A2B_INTEN

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for low bit 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8	RW	0x1	a2b_trig_modex Interrupt trigger mode for a2b_tx_done_int of groupx. 1'b0: Write CMD then generate interrupt 1'b1: Write CMD firstly, then Write DATA, and then generate interrupt
7:2	RO	0x00	reserved
1	RW	0x0	a2b_rx_done_inten Interrupt enable for a2b_rx_done_int of groupx. 1'b0: Disable 1'b1: Enable
0	RW	0x0	a2b_tx_done_inten Interrupt enable for a2b_tx_done_int of groupx. 1'b0: Disable 1'b1: Enable

MAILBOX_A2B_STATUS

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	W1C	0x0	a2b_rx_done_int AP rx_done interrupt status of groupx. This interrupt will be set when AP clear the b2a_tx_done_int, and can be used to inform BB that the next message can be sent by BB. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
0	W1C	0x0	a2b_tx_done_int AP tx_done interrupt status of groupx. This interrupt will be set when AP write to A2B_CMD at fast trigger mode or when AP write to A2B_DATA at normal trigger mode. This interrupt can be used to inform BB that the new message from AP is ready. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_A2B_CMD

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command x register

MAILBOX_A2B_DATA

Address: **Operational Base** + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data x register

MAILBOX_B2A_INTEN

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for low bit 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8	RW	0x1	b2a_trig_modex Interrupt trigger mode for b2a_tx_done_int of groupx. 1'b0: Write CMD then generate interrupt 1'b1: Write CMD firstly, then Write DATA, and then generate interrupt
7:2	RO	0x00	reserved
1	RW	0x0	b2a_rx_done_inten Interrupt enable for b2a_rx_done_int of groupx. 1'b0: Disable 1'b1: Enable
0	RW	0x0	b2a_tx_done_inten Interrupt enable for b2a_tx_done_int of groupx. 1'b0: Disable 1'b1: Enable

MAILBOX_B2A_STATUS

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	W1C	0x0	b2a_rx_done_int BB rx_done interrupt status of groupx. This interrupt will be set when BB clear the a2b_tx_done_int, and can be used to inform AP that the next message can be sent. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
0	W1C	0x0	b2a_tx_done_int BB tx_done interrupt status of groupx. This interrupt will be set when BB write to B2A_CMD at fast trigger mode or when BB write to B2A_DATA at normal trigger mode. This interrupt can be used to inform AP that the new message from BB is ready. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_B2A_CMD

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command x register

MAILBOX_B2A_DATA

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Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data x register

13.5 Application Notes

- TX done interrupt is usually used to inform the receiver that the CMD and DATA is ready. It supports two trigger mode:
  - Normal mode
    1. Configure bit 8 of MAILBOX_*_INTEN to '1'(* stands for "A2B" or "B2A")
    2. Configure bit 0 of MAILBOX_*_INTEN to '1'
    3. Write the MAILBOX_*_CMD firstly
    4. Then write the MAILBOX_*_DATA
    5. And then generate a TX done interrupt

    Write to the MAILBOX_*_CMD register before writing to the MAILBOX_*_DATA register. If wrong order is used, then the interrupt cannot be generated successfully.
  - Fast trigger mode
    1. Configure bit 8 of MAILBOX_*_INTEN to '0'
    2. Configure bit 0 of MAILBOX_*_INTEN to '1'
    3. Write the MAILBOX_*_CMD
    4. And then generate a TX done interrupt
  - If you want to clear the interrupt, you can read out the MAILBOX_*_STATUS register and writing 1 to corresponding bit.
- RX done interrupt is usually used to inform the sender that the receiver has read out the CMD and DATA. It is triggered when the receiver has cleared the corresponding TX done interrupt:
  - AP to BB (assume TX done interrupt is set to normal mode)
    1. AP configure bit 1 of MAILBOX_B2A_INTEN to '1'
    2. BB configure bit 8 of MAILBOX_A2B_INTEN to '1'
    3. BB configure bit 0 of MAILBOX_A2B_INTEN to '1'
    4. AP write the MAILBOX_A2B_CMD
    5. AP write the MAILBOX_A2B_DATA
    6. Bit 0 of MAILBOX_A2B_STATUS is automatically set to '1' and TX done interrupt to BB is generated
    7. BB receive the TX done interrupt and read out the message
    8. BB write '1' to bit 0 of MAILBOX_A2B_STATUS
    9. And then bit 1 of MAILBOX_B2A_STATUS is automatically set to '1' and RX done interrupt to AP is generated
    10. AP receive the RX done interrupt which indicate BB has read out the message
    11. AP write '1' to bit 1 of MAILBOX_B2A_STATUS
    12. AP can start a new transfer

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Chapter 14 SARADC

14.1 Overview

The ADC is a 4-channel single-ended 10-bit Successive Approximation Register (SAR) A/D Converter. It uses the supply and ground as its reference which avoids the use of any external reference. The input range is typically 0V to 1.8V.
SARADC controller supports the following features:

- Support single mode and series conversion mode
- In single mode, the conversion operates once each software is accessed
- In series conversion, the controller samples each channel then loops until the software stops conversion
- High/low threshold can be set, higher/lower/between high-low-threshold interrupt can be enabled

14.2 Block Diagram

SARADC block is shown in Fig. 14-1. This includes:

- APB Interface
- Control FSM
- SARADC PHY

The software can configure the SARADC controller by APB interface, then the inter FSM will communicate with SARADC PHY for limited timing requests.

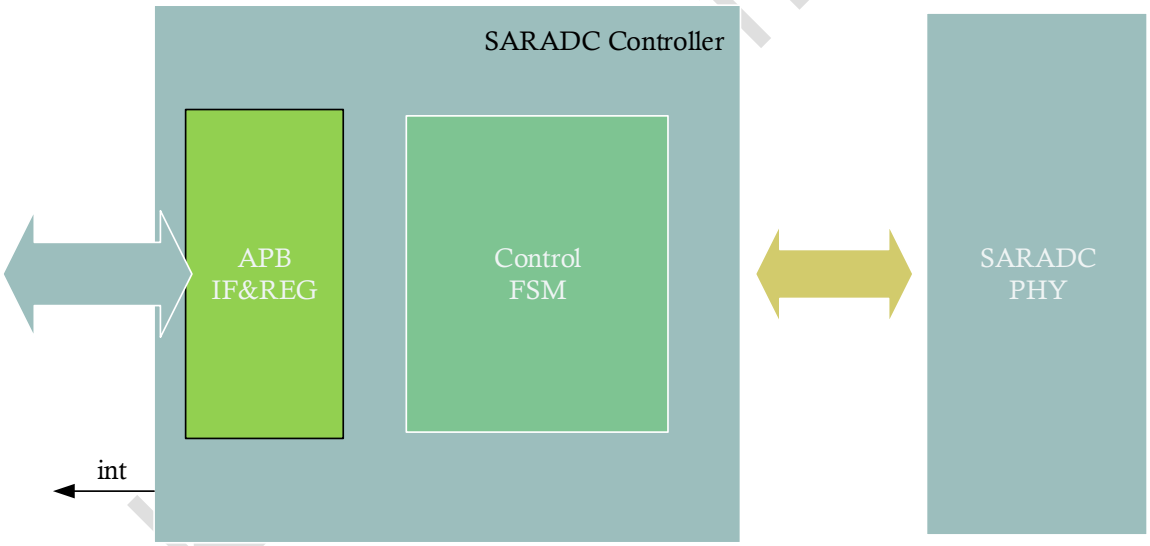

Fig. 14-1 SARADC Block Diagram

14.3 Function Description

SARADC block includes controller and PHY, user cannot directly access SARADC PHY. Software access the SARADC through SARADC controller by APB interface. SARADC controller will sample the conversion result from SARADC PHY.

14.4 Register Description

14.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

14.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SARADC_CONV_CON	0x0000	W	0x00000000	Conversion control

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Name	Offset	Size	Reset Value	Description
SARADC_T_PD_SOC	0x0004	W	0x00000013	Timing control for PD to SOC
SARADC_T_AS_SOC	0x0008	W	0x00000005	Timing control for assert SOC
SARADC_T_DAS_SOC	0x000C	W	0x00000007	Timing control from dis-assert SOC to change channel
SARADC_T_SEL_SOC	0x0010	W	0x00000003	Timing control from change channel select to assert SOC
SARADC_HIGH_COMP0	0x0014	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP1	0x0018	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP2	0x001C	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP3	0x0020	W	0x00000000	High threshold for ADC output data
SARADC_LOW_COMP0	0x0054	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP1	0x0058	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP2	0x005C	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP3	0x0060	W	0x00000000	Low threshold for ADC output data
SARADC_DEBOUNCE	0x0094	W	0x00000003	Threshold debounce
SARADC_HT_INT_EN	0x0098	W	0x00000000	High threshold int enable
SARADC_LT_INT_EN	0x009C	W	0x00000000	Low threshold int enable
SARADC_MT_INT_EN	0x0100	W	0x00000000	Middle threshold int enable
SARADC_END_INT_EN	0x0104	W	0x00000000	End conversion int enable
SARADC_ST_CON	0x0108	W	0x0000001C	ADC static control
SARADC_STATUS	0x010C	W	0x00000002	ADC status
SARADC_END_INT_ST	0x0110	W	0x00000000	End conversion int state
SARADC_HT_INT_ST	0x0114	W	0x00000000	High threshold int state
SARADC_LT_INT_ST	0x0118	W	0x00000000	Low threshold int state
SARADC_MT_INT_ST	0x011C	W	0x00000000	Middle threshold int state
SARADC_DATA0	0x0120	W	0x00000000	ADC output data
SARADC_DATA1	0x0124	W	0x00000000	ADC output data
SARADC_DATA2	0x0128	W	0x00000000	ADC output data
SARADC_DATA3	0x012C	W	0x00000000	ADC output data
SARADC_AUTO_CH_EN	0x0160	W	0x00000000	Channel enable in auto channel mode

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3 Detail Registers Description

SARADC_CONV_CON

Address: Operational Base(0xFF4E8000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	int_lock This is used to lock the sample data when interrupt happened. 1'b0: Disable lock 1'b1: Enable lock

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Bit	Attr	Reset Value	Description
8	RW	0x0	as_pd_mode If this bit is set to 1'b1, each time conversion ends, PD will be asserts. Then next time conversion starts, PD will be set to low automatically. This is not used in signal mode.
7	W1C	0x0	end_conv End conversion, this is not used when CONV_CON[5] is set to 1'b1. If this bit set to 1'b1, PD will set to 1'b1 after the last conversion and this bit will be cleared to 1'b0.
6	RW	0x0	auto_channel_mode Auto channel mode. If this is enable, channel will be round auto according which is set in AUTO_CH_EN.
5	RW	0x0	single_pd_mode Single conversion mode. If this bit is set to 1, conversion only operate once, then PD single will be set to 1.
4	W1C	0x0	start_adc Enable ADC, if this bit set to one, conversion will start. Then this bit will be clear to 0.
3:0	RW	0x0	channel_sel Channel for SARADC, 4 channel is supported. This field is not used when CONV_CON[6] is set to 1. 4'd0: Select channel 0 4'd1: Select channel 1 4'd2: Select channel 2 4'd3: Select channel 3

SARADC_T_PD_SOC

Address: Operational Base(0xFF4E8000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x13	t_pd_soc Timing control between power up to start-of-conversion.

SARADC_T_AS_SOC

Address: Operational Base(0xFF4E8000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000005	t_as_soc Timing control for assert SOC signal.

SARADC_T_DAS_SOC

Address: Operational Base(0xFF4E8000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000007	t_das_soc Timing from dis-assert SOC to channel select change.

SARADC_T_SEL_SOC

Address: Operational Base(0xFF4E8000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0003	t_sel_soc Timing from channel load to SOC assert.

SARADC_HIGH_COMP0

Address: Operational Base(0xFF4E8000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp0 High threshold for ADC output data for channel 0.

SARADC_HIGH_COMP1

Address: Operational Base(0xFF4E8000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp1 High threshold for ADC output data for channel 1.

SARADC_HIGH_COMP2

Address: Operational Base(0xFF4E8000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp2 High threshold for ADC output data for channel 2.

SARADC_HIGH_COMP3

Address: Operational Base(0xFF4E8000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	high_comp3 High threshold for ADC output data for channel 3.

SARADC_LOW_COMP0

Address: Operational Base(0xFF4E8000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp0 Low threshold for ADC output data for channel 0.

SARADC_LOW_COMP1

Address: Operational Base(0xFF4E8000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp1 Low threshold for ADC output data for channel 1.

SARADC_LOW_COMP2

Address: Operational Base(0xFF4E8000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp2 Low threshold for ADC output data for channel 2.

SARADC_LOW_COMP3

Address: Operational Base(0xFF4E8000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	low_comp3 Low threshold for ADC output data for channel 3.

SARADC_DEBOUNCE

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Address: Operational Base(0xFF4E8000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce ADC controller will only generate interrupt data is higher/lower/between setting threshold for "debounce" times.

SARADC_HT_INT_EN

Address: Operational Base(0xFF4E8000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x0	reserved
3	RW	0x0	ht_int_en3 High threshold interrupt for channel 3. 1'b0: Disable interrupt 1'b1: Enable interrupt
2	RW	0x0	ht_int_en2 High threshold interrupt for channel 2. 1'b0: Disable interrupt 1'b1: Enable interrupt
1	RW	0x0	ht_int_en1 High threshold interrupt for channel 1. 1'b0: Disable interrupt 1'b1: Enable interrupt
0	RW	0x0	ht_int_en0 High threshold interrupt for channel 0. 1'b0: Disable interrupt 1'b1: Enable interrupt

SARADC_LT_INT_EN

Address: Operational Base(0xFF4E8000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x0	reserved
3	RW	0x0	lt_int_en3 Low threshold interrupt for channel 3. 1'b0: Disable interrupt 1'b1: Enable interrupt
2	RW	0x0	lt_int_en2 Low threshold interrupt for channel 2. 1'b0: Disable interrupt 1'b1: Enable interrupt
1	RW	0x0	lt_int_en1 Low threshold interrupt for channel 1. 1'b0: Disable interrupt 1'b1: Enable interrupt
0	RW	0x0	lt_int_en0 Low threshold interrupt for channel 0. 1'b0: Disable interrupt 1'b1: Enable interrupt

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SARADC_MT_INT_EN

Address: Operational Base(0xFF4E8000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x0	reserved
3	RW	0x0	mt_int_en3 Middle threshold interrupt for channel3. 1'b0: Disable interrupt 1'b1: Enable interrupt
2	RW	0x0	mt_int_en2 Middle threshold interrupt for channel2. 1'b0: Disable interrupt 1'b1: Enable interrupt
1	RW	0x0	mt_int_en1 Middle threshold interrupt for channel1. 1'b0: Disable interrupt 1'b1: Enable interrupt
0	RW	0x0	mt_int_en0 Middle threshold interrupt for channel0. 1'b0: Disable interrupt 1'b1: Enable interrupt

SARADC_END_INT_EN

Address: Operational Base(0xFF4E8000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	end_int_en End of conversion interrupt. 1'b0: Disable end conversion interrupt 1'b1: Enable end conversion interrupt

SARADC_ST_CON

Address: Operational Base(0xFF4E8000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x3	ictrl Control the bias current of the preamplifier in the SAR-ADC.
2:0	RW	0x4	cctrl Control the capacitance of the capacitor DAC array, which is related to the linearity of the SAR-ADC.

SARADC_STATUS

Address: Operational Base(0xFF4E8000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:2	RO	0x0	sel ADC channel select

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Bit	Attr	Reset Value	Description
1	RO	0x1	pd 1'b1: ADC is power down. 1'b0: ADC is power up and in conversion.
0	RO	0x0	conv_st Conversion status 1'b1: ADC controller FSM is busy. 1'b0: ADC controller FSM is idle.

SARADC_END_INT_ST

Address: Operational Base(0xFF4E8000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	end_int_st ADC end conversion interrupt status. 1'b0: Interrupt not happened 1'b1: Interrupt happened

SARADC_HT_INT_ST

Address: Operational Base(0xFF4E8000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000	reserved
3	W1C	0x0	ht_int_st3 High threshold interrupt state for channel 3. 1'b0: Interrupt not happened 1'b1: Interrupt happened
2	W1C	0x0	ht_int_st2 High threshold interrupt state for channel 2. 1'b0: Interrupt not happened 1'b1: Interrupt happened
1	W1C	0x0	ht_int_st1 High threshold interrupt state for channel 1. 1'b0: Interrupt not happened 1'b1: Interrupt happened
0	W1C	0x0	ht_int_st0 High threshold interrupt state for channel 0. 1'b0: Interrupt not happened 1'b1: Interrupt happened

SARADC_LT_INT_ST

Address: Operational Base(0xFF4E8000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000	reserved
3	W1C	0x0	lt_int_st3 Low threshold interrupt state for channel 3. 1'b0: Interrupt not happened 1'b1: Interrupt happened
2	W1C	0x0	lt_int_st2 Low threshold interrupt state for channel 2. 1'b0: Interrupt not happened 1'b1: Interrupt happened
1	W1C	0x0	lt_int_st1 Low threshold interrupt state for channel 1. 1'b0: Interrupt not happened 1'b1: Interrupt happened

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Bit	Attr	Reset Value	Description
0	W1C	0x0	lt_int_st0 Low threshold interrupt state for channel 0. 1'b0: Interrupt not happened 1'b1: Interrupt happened

SARADC_MT_INT_ST

Address: Operational Base(0xFF4E8000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000	reserved
3	W1C	0x0	mt_int_st3 Between high and low threshold interrupt state for channel 3. 1'b0: Interrupt not happened 1'b1: Interrupt happened
2	W1C	0x0	mt_int_st2 Between high and low threshold interrupt state for channel 2. 1'b0: Interrupt not happened 1'b1: Interrupt happened
1	W1C	0x0	mt_int_st1 Between high and low threshold interrupt state for channel 1. 1'b0: Interrupt not happened 1'b1: Interrupt happened
0	W1C	0x0	mt_int_st0 Between high and low threshold interrupt state for channel 0. 1'b0: Interrupt not happened 1'b1: Interrupt happened

SARADC_DATA0

Address: Operational Base(0xFF4E8000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data0 ADC channel 0 data

SARADC_DATA1

Address: Operational Base(0xFF4E8000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data1 ADC channel 1 data

SARADC_DATA2

Address: Operational Base(0xFF4E8000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data2 ADC channel 2 data

SARADC_DATA3

Address: Operational Base(0xFF4E8000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	data3 ADC channel 3 data

SARADC_AUTO_CH_EN

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Address: Operational Base(0xFF4E8000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	auto_ch_en Enable channel in auto channel mode, each bit can enable for one channel.

14.5 Application Notes

14.5.1 Series Conversion Mode

Steps of ADC conversion in series conversion mode:

- Decide which channel should be used and whether auto_channel mode should be set. In auto_channel mode, the channel will be changed from 0-3 then to 0. Please refer to the SARADC_CONV_CON register.
- Set SARADC_CONV_CON[4] to 1’b1, then the conversion will start.
- If conversion wants to be ended, set SARADC_CONV_CON[7] to 1’b1.
- Conversion could be read from SARADC_DATAn (n is from 0-3).
- If threshold compare interrupt wants to be used, high/low threshold could be set, and interrupt should be set as an application.
- If auto_channel mode is not set, you could set the channel as an application.

14.5.2 Single Mode

Steps of ADC conversion in single mode:

- Decide which channel should be used and set SARADC_CONV_CON[3:0].
- Set SARADC_CONV_CON[5] to 1’b1.
- Set SARADC_CONV_CON[4] to 1’b1, then the conversion will start.
- The conversion only operates once then ends. PD will be asserted and PD status could be got by reading SARADC_STATUS.
- Conversion could be read from SARADC_DATAn (n is from 0-3).

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Chapter 15 Temperature-Sensor ADC (TSADC)

15.1 Overview

TSADC controller is used to control and get the temperature information. TSADC will convert for each enabled channel in loop after the initial setting and can be stopped by software. If you find that the temperature is high in a period of time, an interrupt is generated to the processor down-measures taken; if the temperature over a period of time High, the resulting TSHUT gave CRU module, let it reset the entire chip, or via GPIO give PMIC. Also, if you find that the temperature low in a period of time, an interrupt can be generated.

TSADC controller supports the following features:

- The temperature for high and low interrupt can be configured
- The temperature of system reset can be configured
- The time interval of temperature detection can be configured
- When detecting a high temperature, the time interval of temperature detection can be configured
- High temperature debounce can be configured
- An interrupt can be generated after TSADC converts all setting channel
- -40~125°C temperature range and 0.6°C temperature resolution

15.2 Block Diagram

TSADC controller comprises with:

- APB Interface
- TSADC control logic

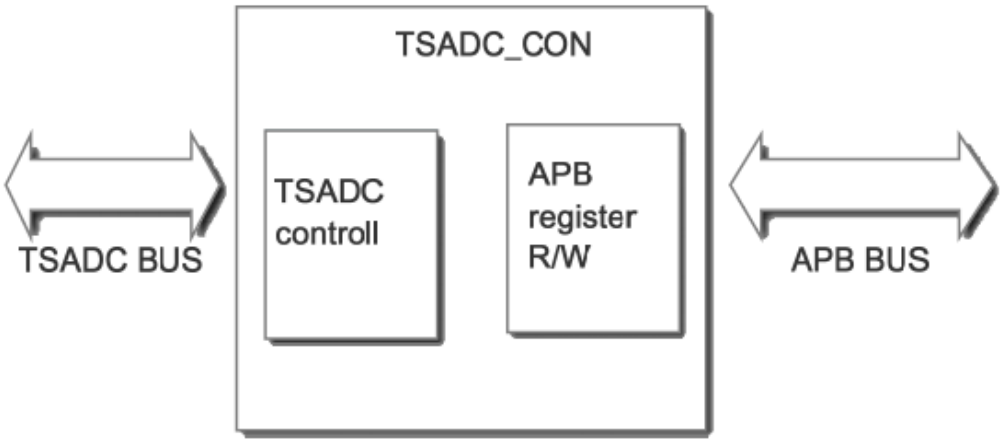

Fig. 15-1 TSADC Controller Block Diagram

15.3 Function Description

15.3.1 APB Interface

There is an APB Slave interface in TSADC controller, which is used to configure the TSADC controller registers and look up the temperature from the temperature sensor.

15.3.2 TSADC Controller

This block is used to control the TSADC PHY to meet the conversion timing and receive the temperature information from TSADC PHY.

15.4 Register Description

15.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

15.4.2 Registers Summary

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Name	Offset	Size	Reset Value	Description
TSADC_USER_CON	0x0000	W	0x00000000	User control
TSADC_AUTO_CON	0x0004	W	0x00000000	Auto control
TSADC_AUTO_STATUS	0x0008	W	0x00000000	Status used in auto mode
TSADC_AUTO_SRC	0x000C	W	0x00000000	Channel select for TSADC in auto mode
TSADC_LT_EN	0x0010	W	0x00000000	Low temperature check logic enable
TSADC_HT_INT_EN	0x0014	W	0x00000000	High temperature interrupt enable
TSADC_GPIO_EN	0x0018	W	0x00000000	Temperature violation to GPIO enable
TSADC_CRU_EN	0x001C	W	0x00000000	Temperature violation to CRU enable
TSADC_LT_INT_EN	0x0020	W	0x00000000	Low temperature interrupt enable
TSADC_HLT_INT_PD	0x0024	W	0x00000000	High and low temperature interrupt status
TSADC_EOC_HSHUT_PD	0x0028	W	0x00000000	High temperature shut and round int status
TSADC_DATA0	0x002C	W	0x00000000	Channel0 data
TSADC_COMP0_INT	0x006C	W	0x00000000	High temperature interrupt threshold for channel0
TSADC_COMP0_SHUT	0x010C	W	0x00000000	High temperature shut threshold for channel0
TSADC_HIGH_INT_DEBOUNCE	0x014C	W	0x00000003	High interrupt debounce
TSADC_HIGH_TSHUT_DEBOUNCE	0x0150	W	0x00000003	High shut debounce
TSADC_AUTO_PERIOD	0x0154	W	0x00010000	Auto conversion period
TSADC_AUTO_PERIOD_HT	0x0158	W	0x00010000	Auto conversion period for high temperature
TSADC_COMP0_LOW_INT	0x015C	W	0x00000000	Low temperature threshold for channel0
TSADC_T_SETUP	0x019C	W	0x0000005F	Timing for setup
TSADC_T_PW_EN	0x0200	W	0x00000000	Timing for pw_en
TSADC_T_EN_CLK	0x0204	W	0x00000001	Timing for en_clk
TSADC_T_NON_OV	0x0208	W	0x00000002	Timing for non_ov
TSADC_T_HOLD	0x020C	W	0x00000013	Timing for hold
TSADC_Q_MAX	0x0210	W	0x00000000	Max data used for data inversion
TSADC_STATIC_CON	0x0214	W	0x0280001B	Static control signal
TSADC_CLK_CH_PERIOD	0x021C	W	0x0000012B	CLK_CH_TS period control
TSADC_T_PW_CLK	0x0220	W	0x00000030	Timing for pw_clk

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

15.4.3 Detail Registers Description

TSADC_USER_CON

Address: Operational Base(0xFF650000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RO	0x0	adc_status 1'b0: ADC stop 1'b1: Conversion in progress
7	R/WSC	0x0	start When software write 1 to this bit, start-of-conversion will be assert. This bit will be cleared after TSADC access finishing. Only when TSADC_USER_CON[5] = 1'b1, this bit takes effect.
6	RW	0x0	eoc_inten Enable end-of-conversion interrupt for each conversion. 1'b0 : Disable 1'b1 : Enable
5	RW	0x0	start_mode Start mode. 1'b0: TSADC controller will assert start_of_conversion after power up. 1'b1: The start_of_conversion will be controlled by TSADC_USER_CON[7].
4	RW	0x0	power_control ADC power control 1'b0: Power down 1'b1: Power up This bit is not enable when TSADC_AUTO_CON[0] is set to 1.
3:0	RW	0x0	input_src_sel ADC input source select in user mode. Should be set at 0.

TSADC_AUTO_CON

Address: Operational Base(0xFF650000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:9	RO	0x00	reserved
8	RW	0x0	tshut_polarity This bit is used to control the output signal polarity to GPIO when the temperature is higher than threshold. 1'b0: Low active 1'b1: High active
7:3	RO	0x00	reserved
2	RW	0x0	round_int_en Int enable for round mode. Used for auto mode all channel set is sampled. 1'b1: Enable 1'b0: Disable
1	RW	0x0	q_sel 1'b0: Use tsadc_q as output (positive temperature coefficient) 1'b1: Use (q_max - tsadc_q) as output (negative temperature coefficient)
0	RW	0x0	auto_en Auto conversion enable 1'b0: TSADC controller works at user-define mode 1'b1: TSADC controller works at auto mode

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TSADC_AUTO_STATUS

Address: Operational Base(0xFF650000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ht_wram High temperature status 1'b0: TSADC data is not higher than high temperature shut value 1'b1: TSADC data is higher than high temperature shut value
2	RW	0x0	auto_status TSADC auto mode status 1'b0: Auto mode stop 1'b1: Auto mode in progress
1	W1C	0x0	last_tshut_cru Status for CRU reset latest temperature shut, write 1 to clear.
0	W1C	0x0	last_tshut_gpio Status for GPIO latest temperature shut, write 1 to clear.

TSADC_AUTO_SRC

Address: Operational Base(0xFF650000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	auto_src Enable channel for TSADC in auto mode, each bit can enable for one channel.

TSADC_LT_EN

Address: Operational Base(0xFF650000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	low_temperature_vio_en Low temperature violation logic enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_HT_INT_EN

Address: Operational Base(0xFF650000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	high_temperature_int_en High temperature interrupt enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_GPIO_EN

Address: Operational Base(0xFF650000) + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	gpio_en Temperature violation to GPIO enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_CRU_EN

Address: Operational Base(0xFF650000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	cru_en Temperature violation to CRU reset enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_LT_INT_EN

Address: Operational Base(0xFF650000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	low_temperature_int_en Low temperature interrupt enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_HLT_INT_PD

Address: **Operational Base(0xFF650000)** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	W1C	0x0000	lt_int_status Low temperature interrupt status for each channel.
15:0	W1C	0x0000	ht_int_status High temperature interrupt status for each channel.

TSADC_EOC_HSHUT_PD

Address: Operational Base(0xFF650000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	W1C	0x0	round_int_pd Auto mode interrupt for each round of all set channel.
16	W1C	0x0	usr_eoc_irq_pd User mode end interrupt status.
15:0	W1C	0x0000	ht_shut_pd High temperature shut down status for each channel.

TSADC_DATA0

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Address: Operational Base(0xFF650000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	adc_data A/D value of the channel 0 last conversion.

TSADC_COMP0_INT

Address: Operational Base(0xFF650000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_h_int_comp_src0 TSADC high temperature level. TSADC output is bigger than or equal to this 10-bit value, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP0_SHUT

Address: Operational Base(0xFF650000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_shut_comp_src0 TSADC high temperature level. TSADC output is bigger than or equal to this 10-bit value, means the temperature is too high. TSHUT will be valid.

TSADC_HIGH_INT_DEBOUNCE

Address: Operational Base(0xFF650000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt when temperature is higher than or equal to COMP_INT for "debounce" times.

TSADC_HIGH_TSHUT_DEBOUNCE

Address: Operational Base(0xFF650000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate TSHUT when temperature is higher than or equal to COMP_SHUT for "debounce" times.

TSADC_AUTO_PERIOD

Address: Operational Base(0xFF650000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period When auto mode is enabled, this register controls the interleave between every conversion for all channel enabled of TSADC.

TSADC_AUTO_PERIOD_HT

Address: **Operational Base(0xFF650000)** + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period This register controls the interleave between every conversion for all channel enabled of TSADC after the temperature is higher than or equal to COMP_SHUT or COMP_INT.

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TSADC_COMP0_LOW_INT

Address: Operational Base(0xFF650000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	tsadc_l_int_comp_src0 TSADC low temperature level. TSADC output is lower than or equal to this 10-bit value, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_T_SETUP

Address: Operational Base(0xFF650000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x005f	t_setup The timing between TSADC power up and start conversion.

TSADC_T_PW_EN

Address: Operational Base(0xFF650000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	t_pw_en The timing assert start conversion signal.

TSADC_T_EN_CLK

Address: Operational Base(0xFF650000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	t_en_clk The timing between dis-assert start conversion signal (EN_TEMP_SEN_TS) and assert CLK_SEN_TS[8].

TSADC_T_NON_OV

Address: Operational Base(0xFF650000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	t_non_ov The timing between each bit assertion of CLK_SENSE_TS.

TSADC_T_HOLD

Address: Operational Base(0xFF650000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0013	t_hold The timing between dis-assert CLK_SENSE_TS and TSADC data valid.

TSADC_Q_MAX

Address: Operational Base(0xFF650000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	q_max This register used for TSADC_AUTO_CON[1] for inversion output data.

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TSADC_STATIC_CON

Address: Operational Base(0xFF650000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	buf_vref_sel Offset control for temperature output code.
26:23	RW	0x5	buf_slope_sel Slope control for temperature output code.
22:21	RW	0x0	comp_i_trim Comparator current timing ports.
20:17	RW	0x0	vbe_i_trm Current timing ports for VBE in PTAT generator.
16:13	RW	0x0	verf_trim Reference voltage trimming ports for reference generator.
12:9	RW	0x0	bgr_r_trim BGR control ports in reference generator.
8:5	RW	0x0	bgr_i_trim BJT emitter current control ports in reference generator.
4:2	RW	0x6	avg_mode Average mode control ports for digital filter.
1	RW	0x1	en_dem Dynamic element matching enable port.
0	RW	0x1	en_ch Digital offset cancellation enable port.

TSADC_CLK_CH_PERIOD

Address: Operational Base(0xFF650000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000012b	clk_ch_period Control the period of CLK_CH_TS.

TSADC_T_PW_CLK

Address: Operational Base(0xFF650000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0030	t_pw_clk The timing for assertion of each bit of CLK_SENSE_TS.

15.5 Interface Description

Table 15-1 TSADC Rockchip Matrix IO Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
tsadc_tshut	O		

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

15.6 Application Notes

15.6.1 Conversion Flow

The system works as follows:

1) Temperature violation and other configurations may be set.
2) Assert tsadc_tsen_en and tsadc_ana_reg0/1/2.
3) Set the bit[0] in register TSADC_AUTO_CON, then TSADC will work.

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4) Then temperature information can be read from the APB interface.
5) If TSADC needs to be closed, set bit[0] in register TSADC_AUTO_CON to 1'b0.

15.6.2 Timing Diagram

When TSADC start to work, the timing will follow the 错误!未找到引用源。
The timing requirement is also listed as follows.

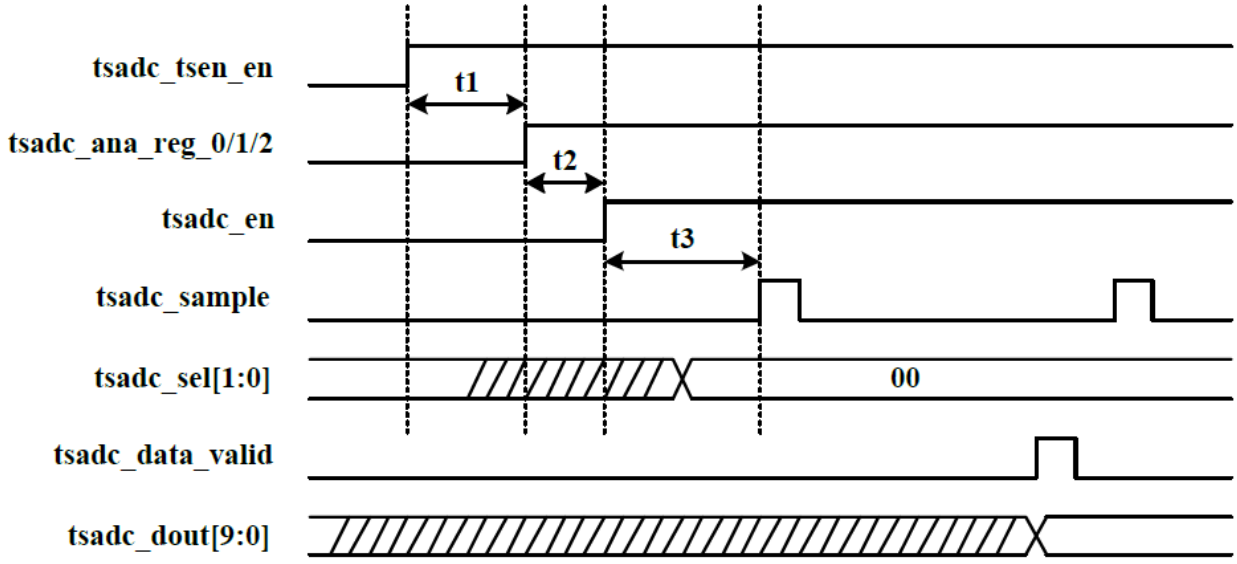

Fig. 15-2 Timing Diagram for TSADC

Table 15-2 TSADC Start Timing

parameter	min
t1	10us
t2	0us
t3	90us

15.6.3 Temperature-to-Code Mapping

Table 15-3 TSADC Lookup Table

temperature (℃)	typical output
-40	395
25	503
40	528
125	679

Note:
Code to Temperature mapping of the Temperature sensor is a linear curve. Any temperature, code falling between to 2 given temperatures can be linearly interpolated.
Code to Temperature mapping should be updated based on silicon results.

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Chapter 16 SPINLOCK

16.1 Overview

The hardware spinlock used for spinlock status storage. All the CPU and MCU can access spinlock to get the lock status.

16.2 Block Diagram

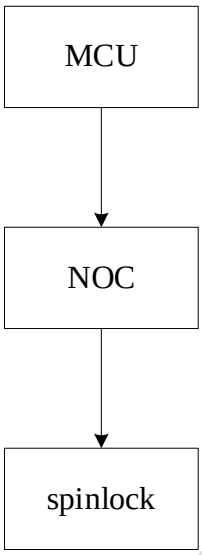

Fig.16-1 Spinlock in System

16.3 Function Description

The CPU and MCU can obtain a lock by writing a non-zero value to the SPINLOCK_STATUS_x register in the spinlock; The CPU and MCU can also read SPINLOCK_STATUS_x to query the status of the lock.

16.4 Register Description

16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SPINLOCK-CH0	0xFF240000
SPINLOCK-CH1	0xFF241000
SPINLOCK-CH2	0xFF242000
SPINLOCK-CH3	0xFF243000

16.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPINLOCK_STATUS_0	0x0000	W	0x00000000	Spinlock Status Controller Register 0
SPINLOCK_STATUS_1	0x0004	W	0x00000000	Spinlock Status Controller Register 1
SPINLOCK_STATUS_2	0x0008	W	0x00000000	Spinlock Status Controller Register 2
SPINLOCK_STATUS_3	0x000C	W	0x00000000	Spinlock Status Controller Register 3

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Name	Offset	Size	Reset Value	Description
SPINLOCK_STATUS_4	0x0010	W	0x00000000	Spinlock Status Controller Register 4
SPINLOCK_STATUS_5	0x0014	W	0x00000000	Spinlock Status Controller Register 5
SPINLOCK_STATUS_6	0x0018	W	0x00000000	Spinlock Status Controller Register 6
SPINLOCK_STATUS_7	0x001C	W	0x00000000	Spinlock Status Controller Register 7

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

16.4.3 Detail Registers Description

SPINLOCK_STATUS_0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'b0000, 4bits clean to 0.

SPINLOCK_STATUS_1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'b0000, 4bits clean to 0.

SPINLOCK_STATUS_2

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'b0000, 4bits clean to 0.

SPINLOCK_STATUS_3

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'b0000, 4bits clean to 0.

SPINLOCK_STATUS_4

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'b0000, 4bits clean to 0.

SPINLOCK_STATUS_5

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'b0000, 4bits clean to 0.

SPINLOCK_STATUS_6

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'b0000, 4bits clean to 0.

SPINLOCK_STATUS_7

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'b0000, 4bits clean to 0.

16.5 Application Notes

The spinlock can be used as follows：

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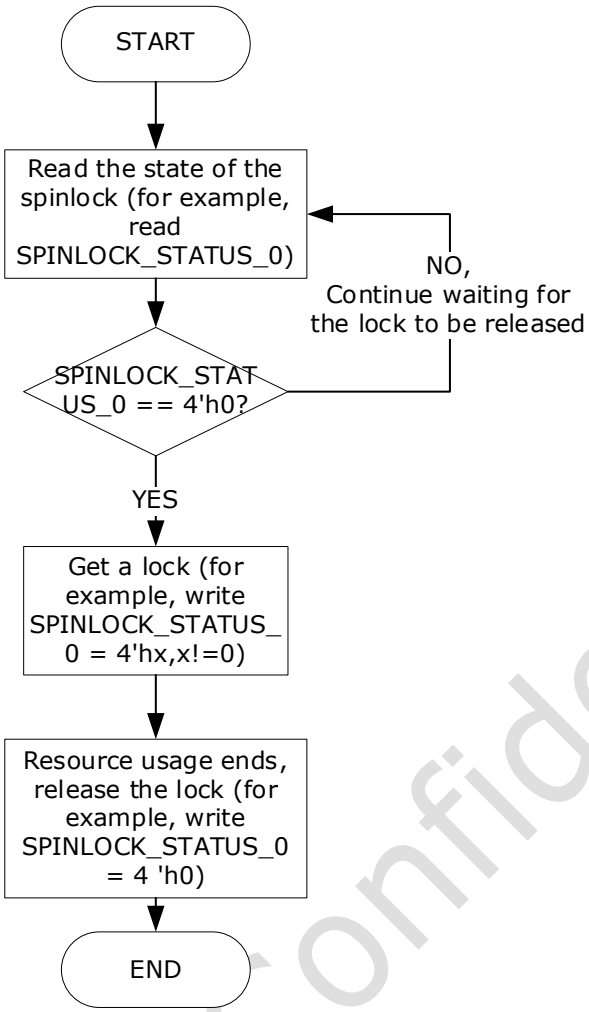

Figure 16-1 spinlock usage flow

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Chapter 17 GPIO

17.1 Overview

GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. GPIO controls the output data and direction of external I/O pads. It can also read back the data on external pads using memory-mapped registers.
GPIO supports the following features:

- 32 bits APB data bus width
- Up to 32 independently configurable signals
- Software control registers with write mask for each bit of each signal
- Configurable debounce logic with a slow clock to debounce interrupts
- Configurable interrupt mode
- Four virtual OS with independent control registers can be supported
- In virtual OS mode, each OS has independent interrupt
- GPIO input is filtered to remove burrs. The filter function is configured using GRF

17.2 Block Diagram

GPIO is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Interrupt Detection

Interrupt interface to or from interrupt controller.

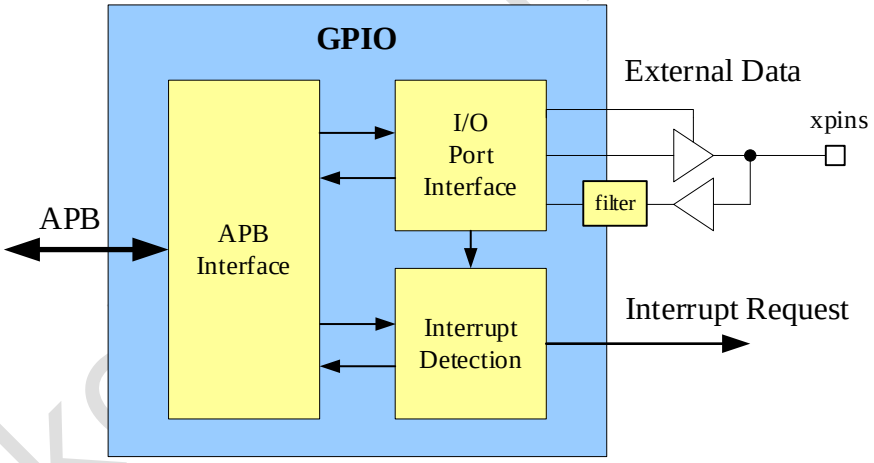

Fig. 17-1 GPIO Block Diagram

17.3 Function Description

17.3.1 Data Control

Under software control, the data and direction control for the signal are sourced from the port data registers (GPIO_SWPORT_DR_L/GPIO_SWPORT_DR_H) and direction control registers (GPIO_SWPORT_DDR_L/GPIO_SWPORT_DRR_H). The direction of the external I/O pad is controlled by the value of the port data direction registers. The data written to these memory-mapped registers gets mapped onto an output signal (gpio_port_ddr) of the GPIO peripheral. This output signal controls the direction of an external I/O pad. The default data direction is Input. The data written to the port data registers drives the output buffer (gpio_port_dr) of the I/O pad.

External data are input on the external data signal (gpio_ext_port). Reading the external signal register (GPIO_EXT_PORT) shows the value of this signal, regardless of the direction.

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This register is read-only, meaning that it cannot be written from the APB software interface.

17.3.2 Interrupts

I/O port can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge
- Both the rising edge and the falling edge

The interrupts can be masked by programming the GPIO_INT_MASK_L/GPIO_INT_MASK_H registers. The interrupt status can be read before masking (GPIO_INT_RAWSTATUS) and after masking (GPIO_INT_STATUS).

For edge-sensitive interrupts, the Interrupt Service Routine (ISR) can clear the interrupt by writing a 1 to the corresponding bit of the GPIO_PORT_EOI_L/GPIO_PORT_EOI_H registers. This write operation also clears the interrupt status and raw status registers. Writing to the interrupt clear registers has no effect on level-sensitive interrupts. If level-sensitive interrupts cause the processor to interrupt, then the ISR can poll the interrupt raw status register until the interrupt source disappears, or it can write to the interrupt mask register to mask the interrupt before exiting the ISR. If the ISR exits without masking or disabling the interrupt prior to exiting, then the level-sensitive interrupt repeatedly requests an interrupt until the interrupt is cleared at the source.

The interrupts are combined into an active-high interrupt output signal. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its own mask bit.

Whenever I/O port is configured for interrupts, the data direction must be set to Input. If the data direction is reprogrammed to Output, then any pending edge-sensitive interrupts are not lost. However, no new interrupts are generated, and level-sensitive interrupts are lost.

Interrupt signals are internally synchronized to a system clock pclk_intr, which is connected to the APB bus clock pclk. Therefore, the pclk needs to be running for interrupt detection.

17.3.3 Debounce Operation

The external signal can be debounced to remove any spurious glitches that are less than half period of the external debouncing clock.

When an input interrupt signal is debounced using a slow debounce clock (external input clock dbclk or internal divided clock dbclk_div), the signal must be active for a minimum of one cycle of the debounce clock to guarantee that it is registered. Any input pulse widths less than half debounce clock period are bounced. A pulse width between half and one debounce clock width may or may not propagate, depending on its phase relationship to the debounce clock. If the input pulse spans rising edges and falling edge of the debounce clock, it is registered. If it spans only one edge, it is not registered.

The debounce function can be controlled by programming the debounce enable registers (GPIO_DEBOUNCE_L/GPIO_DEBOUNCE_H), debounce clock divide enable registers (GPIO_DBCLK_DIV_EN_L/GPIO_DBCLK_DIV_EN_H) and debounce clock divide control register (GPIO_DBCLK_DIV_CON).

17.3.4 Four OS Operation and Four Interrupts

To select this mode, virtual enable register should be set (GPIO_VIRTUAL_EN). Then all the configures can be allotted to four OS (for example OS_A, OS_B, OS_C, OS_D). OS_A will use the original address offset, OS_B will use the offset + 0x1000, OS_C will use the offset + 0x2000, OS_D will use the offset + 0x3000. The 32 bit I/O port should also be allotted to

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the OS by setting reg group registers (GPIO_REG_GROUP_L and GPIO_REG_GROUP_H). Once reg group is set, the I/O operation can only be used by the setting address offset. Each OS has its own interrupt for I/O port, this is depended on reg group.
If virtual enable register is disable, reg group can also be used to allotted I/O interrupt. These four independent interrupts may be used for priority interrupt setting.

17.3.5 Burr filtration

The input signal from the PAD is filtered by filter to remove burrs and then sent to GPIO IP. The filter module can be selected to turn on or off, and the width of the filter burr can be configured. GPIO0-4 is connected to the filter in the table，the table lists the location of the register controlling filter in the GRF. See Chapter GRF for a more detailed description:

Table 17-1 GPIO filter Description

Module	Filter Name	Filter Info
GPIO0	GPIO0_FILTER	PMUGRF_SOC_CON5 [3:0]=gpio0_filter_en PMUGRF_SOC_CON5 [8:4]=gpio0_filter_sel0 PMUGRF_SOC_CON5 [14:10]=gpio0_filter_sel1 PMUGRF_SOC_CON6 [8:4]=gpio0_filter_sel2 PMUGRF_SOC_CON6 [14:10]=gpio0_filter_sel3 PMUGRF_SOC_CON7 [19:0]=gpio0_filter_count0 PMUGRF_SOC_CON8 [19:0]=gpio0_filter_count1 PMUGRF_SOC_CON9 [19:0]=gpio0_filter_count2 PMUGRF_SOC_CON10 [19:0]=gpio0_filter_count3
GPIO1_SHADOW	GPIO1_SHADOW_FILTER	PMUGRF_SOC_CON11 [3:0]=gpio1_shadow_filter_en PMUGRF_SOC_CON11 [8:4]=gpio1_shadow_filter_sel0 PMUGRF_SOC_CON11 [14:10]=gpio1_shadow_filter_sel1 PMUGRF_SOC_CON12 [8:4]=gpio1_shadow_filter_sel2 PMUGRF_SOC_CON12 [14:10]=gpio1_shadow_filter_sel3 PMUGRF_SOC_CON13 [19:0]=gpio1_shadow_filter_count0 PMUGRF_SOC_CON14 [19:0]=gpio1_shadow_filter_count1 PMUGRF_SOC_CON15 [19:0]=gpio1_shadow_filter_count2 PMUGRF_SOC_CON16 [19:0]=gpio1_shadow_filter_count3
GPIO1	GPIO1_FILTER	COREGRF_SOC_CON0 [3:0]=gpio1_filter_en COREGRF_SOC_CON0 [8:4]=gpio1_filter_sel0

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Module	Filter Name	Filter Info
		COREGRF_SOC_CON0 [14:10]=gpio1_filter_sel1 COREGRF_SOC_CON1 [8:4]=gpio1_filter_sel2 COREGRF_SOC_CON1 [14:10]=gpio1_filter_sel3 COREGRF_SOC_CON2 [19:0]=gpio1_filter_count0 COREGRF_SOC_CON3 [19:0]=gpio1_filter_count1 COREGRF_SOC_CON4 [19:0]=gpio1_filter_count2 COREGRF_SOC_CON5 [19:0]=gpio1_filter_count3
GPIO2/GPIO3/GPIO4	GPIO2_FILTER	GRF_SOC_CON31 [3:0]=gpio2_filter_en GRF_SOC_CON31 [9:4]=gpio2_filter_sel0 GRF_SOC_CON31 [15:10]=gpio2_filter_sel1 GRF_SOC_CON32 [19:0]=gpio2_filter_count0 GRF_SOC_CON33 [19:0]=gpio2_filter_count1

GPIOX_FILTER Filters a maximum of four input burrs. Select "gpiox_filter_en" to enable four inputs. "gpiox_filter_selY" controls which pin of gpio corresponds to the Y input; "gpiox_filter_count" controls the width of the filter burrs. GPIO2_FILTER is shared by GPIO2/3/4.

17.3.6 Shadow GPIO

GPIO1 is in PD_CORE, it has a shadow GPIO1 is in PD_PMU. You can select whether IO is controlled by GPIO1 or GPIO1_SHADOW with PMUGRF_SOC_CON17/18.

17.4 Register Description

17.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
GPIO0	0xFF940000
GPIO1	0xFF870000
GPIO1_SHADOW	0xFF948000
GPIO2	0xFF1C0000
GPIO3	0xFF1D0000
GPIO4	0xFF1E0000

17.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO_SWPORT_DR_L	0x0000	W	0x00000000	Port Data Register (Low)
GPIO_SWPORT_DR_H	0x0004	W	0x00000000	Port Data Register (High)
GPIO_SWPORT_DDR_L	0x0008	W	0x00000000	Port Data Direction Register (Low)
GPIO_SWPORT_DDR_H	0x000C	W	0x00000000	Port Data Direction Register (High)
GPIO_INT_EN_L	0x0010	W	0x00000000	Interrupt Enable Register (Low)

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Name	Offset	Size	Reset Value	Description
GPIO_INT_EN_H	0x0014	W	0x00000000	Interrupt Enable Register (High)
GPIO_INT_MASK_L	0x0018	W	0x00000000	Interrupt Mask Register (Low)
GPIO_INT_MASK_H	0x001C	W	0x00000000	Interrupt Mask Register (High)
GPIO_INT_TYPE_L	0x0020	W	0x00000000	Interrupt Level Register (Low)
GPIO_INT_TYPE_H	0x0024	W	0x00000000	Interrupt Level Register (High)
GPIO_INT_POLARITY_L	0x0028	W	0x00000000	Interrupt Polarity Register (Low)
GPIO_INT_POLARITY_H	0x002C	W	0x00000000	Interrupt Polarity Register (High)
GPIO_INT_BOTHEDGE_L	0x0030	W	0x00000000	Interrupt Both Edge Type Register (Low)
GPIO_INT_BOTHEDGE_H	0x0034	W	0x00000000	Interrupt Both Edge Type Register (High)
GPIO_DEBOUNCE_L	0x0038	W	0x00000000	Debounce Enable Register (Low)
GPIO_DEBOUNCE_H	0x003C	W	0x00000000	Debounce Enable Register (High)
GPIO_DBCLK_DIV_EN_L	0x0040	W	0x00000000	DBCLK Divide Enable Register (Low)
GPIO_DBCLK_DIV_EN_H	0x0044	W	0x00000000	DBCLK Divide Enable Register (High)
GPIO_DBCLK_DIV_CON	0x0048	W	0x00000001	DBCLK Divide Control Register
GPIO_INT_STATUS	0x0050	W	0x00000000	Interrupt Status Register
GPIO_INT_RAWSTATUS	0x0058	W	0x00000000	Interrupt Raw Status Register
GPIO_PORT_EOI_L	0x0060	W	0x00000000	Interrupt Clear Register (Low)
GPIO_PORT_EOI_H	0x0064	W	0x00000000	Interrupt Clear Register (High)
GPIO_EXT_PORT	0x0070	W	0x00000000	External Port Data Register
GPIO_VER_ID	0x0078	W	0x010219C8	Version ID Register
GPIO_STORE_ST_L	0x0080	W	0x00000000	Store Status Register(Low)
GPIO_STORE_ST_H	0x0084	W	0x00000000	Store Status Register(High)
GPIO_GPIO_REG_GROUP_L	0x0100	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP_H	0x0104	W	0x0000FFFF	GPIO Group Control
GPIO_GPIO_VIRTUAL_EN	0x0108	W	0x00000000	GPIO Virtual Enable
GPIO_GPIO_REG_GROUP1_L	0x0110	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP1_H	0x0114	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP2_L	0x0118	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP2_H	0x011C	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP3_L	0x0120	W	0x00000000	GPIO Group Control
GPIO_GPIO_REG_GROUP3_H	0x0124	W	0x00000000	GPIO Group Control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

17.4.3 Detail Registers Description

GPIO_SWPORT_DR_L

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	swport_dr_low Output data for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the lower 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DR_H

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_high Output data for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the upper 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DDR_L

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_low Data direction for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the lower 16 bits of I/O Port.

GPIO_SWPORT_DDR_H

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_high Data direction for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the upper 16 bits of I/O Port.

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GPIO_INT_EN_L

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_en_low Allows each bit of the lower 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_EN_H

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_en_high Allows each bit of the upper 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_MASK_L

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_mask_low Controls whether an interrupt on the lower 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_MASK_H

Address: **Operational Base** + offset (0x001C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_mask_high Controls whether an interrupt on the upper 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_TYPE_L

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_type_low Controls the type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_TYPE_H

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_type_high Controls the type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_POLARITY_L

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_polarity_low Controls the polarity of edge or level sensitivity that can occur on the lower 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_POLARITY_H

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_polarity_high Controls the polarity of edge or level sensitivity that can occur on the upper 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_BOTHEDGE_L

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_bothedge_low Controls the edge type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_low and int_polarity_low for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_low and int_polarity_low registers.

GPIO_INT_BOTHEDGE_H

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_bothedge_high Controls the edge type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_high and int_polarity_high for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_high and int_polarity_high registers.

GPIO_DEBOUNCE_L

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_low Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DEBOUNCE_H

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_high Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DBCLK_DIV_EN_L

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	dbclk_div_en_low Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the lower 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_low is set to 0.

GPIO_DBCLK_DIV_EN_H

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_high Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the upper 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_high is set to 0.

GPIO_DBCLK_DIV_CON

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000001	dbclk_div_con dbclk_div = dbclk / (dbclk_div_con + 1)

GPIO_INT_STATUS

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_status Interrupt status of I/O Port.

GPIO_INT_RAWSTATUS

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_rawstatus Interrupt raw status of I/O Port (premasking bits).

GPIO_PORT_EOI_L

Address: **Operational Base** + offset (0x0060)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/WSC	0x0000	port_eoi_low Controls the clearing of edge type interrupts from the lower 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_PORT_EOI_H

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/WSC	0x0000	port_eoi_high Controls the clearing of edge type interrupts from the upper 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_EXT_PORT

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ext_port This register always reflects the value of the signals on the external I/O Port.

GPIO_VER_ID

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x010219c8	ver_id Version ID.

GPIO_STORE_ST_L

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	store_st_l This reigister can store the state for each GPIO by user writting to this register.

GPIO_STORE_ST_H

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	store_st_h This reigister can store the state for each GPIO by user writting to this register.

GPIO_GPIO_REG_GROUP_L

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP0 with offset 0x0000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag0 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP_H

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xffff	gpio_reg_group_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP0 with offset 0x0000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag0 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_VIRTUAL_EN

Address: **Operational Base** + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	gpio_virtual_en 1'b1: Enable virtual, two OS supported 1'b0: Disable virtual. Only in GROUP0 with offset 0x0000.

GPIO_GPIO_REG_GROUP1_L

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group1_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP1 with offset 0x1000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag1 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP1_H

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group1_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP1 with offset 0x1000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag1 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP2_L

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio_reg_group2_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP2 with offset 0x2000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag2 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP2_H

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group2_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP2 with offset 0x2000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag2 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP3_L

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_reg_group3_low This register control the low 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP3 with offset 0x3000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag3 1'b0: GPIO interrupt connect to other interrupt

GPIO_GPIO_REG_GROUP3_H

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio_reg_group3_high This register control the high 16 bit of GPIO and each bit corresponds each GPIO. When virtual_en=1'b1: 1'b1: GPIO control by GROUP3 with offset 0x3000 1'b0: GPIO control by other GROUP. When virtual_en=1'b0: 1'b1: GPIO interrupt connect to gpio_int_flag3 1'b0: GPIO interrupt connect to other interrupt

17.5 Interface Description

Table 17-2 GPIO Interface Description

Module Pin	Pad Name	IOMUX Setting
GPIO0 Interface		
gpio0_port[0]	GPIO0_A0	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[3:0]=4'h0
gpio0_port[1]	GPIO0_A1	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[7:4]=4'h0
gpio0_port[2]	GPIO0_A2	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[11:8]=4'h0
gpio0_port[3]	GPIO0_A3	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[15:12]=4'h0
gpio0_port[4]	GPIO0_A4	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[3:0]=4'h0
gpio0_port[5]	GPIO0_A5	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[7:4]=4'h0
gpio0_port[6]	GPIO0_A6	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[11:8]=4'h0
gpio0_port[7]	GPIO0_A7	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[15:12]=4'h0
gpio0_port[8]	GPIO0_B0	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[3:0]=4'h0
gpio0_port[9]	GPIO0_B1	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[7:4]=4'h0
gpio0_port[10]	GPIO0_B2	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[11:8]=4'h0

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Module Pin	Pad Name	IOMUX Setting
gpio0_port [11]	GPIO0_ B3	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[15:12]=4'h0
gpio0_port [12]	GPIO0_ B4	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[3:0]=4'h0
gpio0_port [13]	GPIO0_ B5	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[7:4]=4'h0
gpio0_port [14]	GPIO0_ B6	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[11:8]=4'h0
gpio0_port [15]	GPIO0_ B7	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[15:12]=4'h0
gpio0_port [16]	GPIO0_ C0	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[3:0]=4'h0
gpio0_port [17]	GPIO0_ C1	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[7:4]=4'h0
gpio0_port [18]	GPIO0_ C2	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[11:8]=4'h0
gpio0_port [19]	GPIO0_ C3	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[15:12]=4'h0
gpio0_port [20]	GPIO0_ C4	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[3:0]=4'h0
gpio0_port [21]	GPIO0_ C5	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[7:4]=4'h0
gpio0_port [22]	GPIO0_ C6	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[11:8]=4'h0
gpio0_port [23]	GPIO0_ C7	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[15:12]=4'h0
gpio0_port [24]	GPIO0_ D0	GPIO0_IOC_GPIO0D_CON[1:0]=2'h0
GPIO1 Interface		
gpio1_port [0]	GPIO1_ A0	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[3:0]=4'h0
gpio1_port [1]	GPIO1_ A1	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[7:4]=4'h0

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Module Pin	Pad Name	IOMUX Setting
gpio1_port [2]	GPIO1_ A2	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[11:8]=4'h0
gpio1_port [3]	GPIO1_ A3	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[15:12]=4'h0
gpio1_port [4]	GPIO1_ A4	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[3:0]=4'h0
gpio1_port [5]	GPIO1_ A5	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[7:4]=4'h0
gpio1_port [6]	GPIO1_ A6	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[11:8]=4'h0
gpio1_port [7]	GPIO1_ A7	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[15:12]=4'h0
gpio1_port [8]	GPIO1_ B0	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[3:0]=4'h0
gpio1_port [9]	GPIO1_ B1	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[7:4]=4'h0
gpio1_port [10]	GPIO1_ B2	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[11:8]=4'h0
gpio1_port [11]	GPIO1_ B3	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[15:12]=4'h0
gpio1_port [12]	GPIO1_ B4	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[3:0]=4'h0
gpio1_port [13]	GPIO1_ B5	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[7:4]=4'h0
gpio1_port [14]	GPIO1_ B6	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[11:8]=4'h0
gpio1_port [15]	GPIO1_ B7	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[15:12]=4'h0
gpio1_port [16]	GPIO1_ C0	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[3:0]=4'h0
gpio1_port [17]	GPIO1_ C1	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[7:4]=4'h0
gpio1_port	GPIO1_	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[11:8]=4'h0

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Module Pin	Pad Name	IOMUX Setting
[18]	C2	
gpio1_port [19]	GPIO1_C3	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[15:12]=4'h0
gpio1_port [20]	GPIO1_C4	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[3:0]=4'h0
gpio1_port [21]	GPIO1_C5	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[7:4]=4'h0
gpio1_port [22]	GPIO1_C6	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[11:8]=4'h0
gpio1_port [23]	GPIO1_C7	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[15:12]=4'h0
gpio1_port [24]	GPIO1_D0	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[3:0]=4'h0
gpio1_port [25]	GPIO1_D1	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[7:4]=4'h0
gpio1_port [26]	GPIO1_D2	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[11:8]=4'h0
gpio1_port [27]	GPIO1_D3	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[15:12]=4'h0
GPIO2 Interface		
gpio2_port [0]	GPIO2_A0	GPIO2_IOC_GPIO2A_IOMUX_SEL_0[3:0]=4'h0
gpio2_port [1]	GPIO2_A1	GPIO2_IOC_GPIO2A_IOMUX_SEL_0[7:4]=4'h0
gpio2_port [2]	GPIO2_A2	GPIO2_IOC_GPIO2A_IOMUX_SEL_0[11:8]=4'h0
gpio2_port [3]	GPIO2_A3	GPIO2_IOC_GPIO2A_IOMUX_SEL_0[15:12]=4'h0
gpio2_port [4]	GPIO2_A4	GPIO2_IOC_GPIO2A_IOMUX_SEL_1[3:0]=4'h0
gpio2_port [5]	GPIO2_A5	GPIO2_IOC_GPIO2A_IOMUX_SEL_1[7:4]=4'h0

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Module Pin	Pad Name	IOMUX Setting
gpio2_port [6]	GPIO2_ B0	GPIO2_IOC_GPIO2B_IOMUX_SEL_0[3:0]=4'h0
gpio2_port [7]	GPIO2_ B1	GPIO2_IOC_GPIO2B_IOMUX_SEL_0[7:4]=4'h0
gpio2_port [8]	GPIO2_ B2	GPIO2_IOC_GPIO2B_IOMUX_SEL_0[11:8]=4'h0
gpio2_port [9]	GPIO2_ B3	GPIO2_IOC_GPIO2B_IOMUX_SEL_0[15:12]=4'h0
gpio2_port [10]	GPIO2_ B4	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[3:0]=4'h0
gpio2_port [11]	GPIO2_ B5	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[7:4]=4'h0
gpio2_port [12]	GPIO2_ B6	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[11:8]=4'h0
gpio2_port [13]	GPIO2_ B7	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[15:12]=4'h0
gpio2_port [14]	GPIO2_ C0	GPIO2_IOC_GPIO2C_IOMUX_SEL_0[3:0]=4'h0
GPIO3 Interface		
gpio3_port [0]	GPIO3_ A0	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[3:0]=4'h0
gpio3_port [1]	GPIO3_ A1	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[7:4]=4'h0
gpio3_port [2]	GPIO3_ A2	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[11:8]=4'h0
gpio3_port [3]	GPIO3_ A3	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[15:12]=4'h0
gpio3_port [4]	GPIO3_ A4	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[3:0]=4'h0
gpio3_port [5]	GPIO3_ A5	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[7:4]=4'h0
gpio3_port [6]	GPIO3_ A6	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[11:8]=4'h0
gpio3_port [7]	GPIO3_ A7	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[15:12]=4'h0
gpio3_port	GPIO3_ B0	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[3:0]=4'h0

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Module Pin	Pad Name	IOMUX Setting
[8]		
gpio3_port [9]	GPIO3_B1	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[7:4]=4'h0
gpio3_port [10]	GPIO3_B2	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[11:8]=4'h0
gpio3_port [11]	GPIO3_B3	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[15:12]=4'h0
gpio3_port [12]	GPIO3_B4	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[3:0]=4'h0
gpio3_port [13]	GPIO3_B5	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[7:4]=4'h0
gpio3_port [14]	GPIO3_B6	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[11:8]=4'h0
GPIO4 Interface		
gpio4_port [0]	GPO4_A1	
gpio4_port [1]	GPO4_A0	
gpio4_port [2]	GPO4_A3	
gpio4_port [3]	GPO4_A2	
gpio4_port [4]	GPO4_A5	
gpio4_port [5]	GPO4_A4	
gpio4_port [6]	GPIO4_B0	GPIO4_IOC_SARADC_CON [4]=1'h1
gpio4_port [7]	GPIO4_B1	GPIO4_IOC_SARADC_CON [5]=1'h1
gpio4_port [8]	GPIO4_B2	GPIO4_IOC_SARADC_CON [6]=1'h1
gpio4_port	GPIO4_	GPIO4_IOC_SARADC_CON [7]=1'h1

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Module Pin	Pad Name	IOMUX Setting
[9]	B3	

Notes: Unused Module Pin is tied to zero!
Notes: I=input, O=output, I/O=input/output, bidirectional
Notes: The corresponding relationship between gpio4_port[5:0] and GPO4_A0~GPO4_A5 is special

17.6 Application Notes

- Reading from an unused location or unused bits in a particular register always returns zeros. There is no error mechanism in the APB.
- Programming the GPIO registers for interrupt detection should be completed prior to enabling the interrupts in order to prevent spurious glitches on the interrupt output signal to the interrupt controller.

17.6.1 GPIO Mode of SARADC

The pad of GPIO4_B0/GPIO4_B1/GPIO4_B2/GPIO4_B3 are shared with SARADC and can be used as 1.8V input/output. Before using GPIO4_B0~ GPIO4_B3 as common GPIO, you must send 0x00F000F0 to register 0xFF4D8840 (GPIO4_IOC_SARADC_CON) first to set GPIO intput enable. And you can configure other GPIO properties in GPIO4_IOC_SARADC_CON (e.g. pull up/down, Schmitter).

17.6.2 GPIO Mode of MIPI D-PHY

The pad of GPO4_A0/GPO4_A1/GPO4_A2/GPO4_A3/GPO4_A4/ GPO4_A5 are shared with MIPI D-PHY and can be used as 1.8V output. To switch mode to GPIO, refer to the MIPI D-PHY Chapter.

17.6.3 Configuration of GPIO0D0

GPIO0D0 is configured using a separate register GPIO0_IOC_GPIO0D_CON (address 0xFF950830). Select the function by the following values:

- GPIO0_IOC_GPIO0D_CON [1:0]==2 'b00 for GPIO mode
- GPIO0_IOC_GPIO0D_CON [1:0]==2' b01 for OSC_CLK_OUT
- GPIO0_IOC_GPIO0D_CON [1:0]==2 'b10 for REF_CLK0_OUT

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Chapter 18 IO Controller (IOC)

18.1 Overview

The IO Controller (IOC) will be used by the software to do some static Settings related to IOs.

18.2 Function Description

The functions of the IO Controller (IOC) are as follows:

- GPIO IOMUX control
- GPIO PAD pull-up/pull-down, drive strength, power supply voltage and other configurations

18.3 GPIO0_IOC Register Description

18.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO0_IOC_GPIO0A_IOMUX_SEL_0	0x0000	W	0x00000000	GPIO0A IOMUX Select Register 0
GPIO0_IOC_GPIO0A_IOMUX_SEL_1	0x0004	W	0x00000000	GPIO0A IOMUX Select Register 1
GPIO0_IOC_GPIO0B_IOMUX_SEL_0	0x0008	W	0x00000000	GPIO0B IOMUX Select Register 0
GPIO0_IOC_GPIO0B_IOMUX_SEL_1	0x000C	W	0x00000000	GPIO0B IOMUX Select Register 1
GPIO0_IOC_GPIO0C_IOMUX_SEL_0	0x0010	W	0x00000000	GPIO0C IOMUX Select Register 0
GPIO0_IOC_GPIO0C_IOMUX_SEL_1	0x0014	W	0x00000070	GPIO0C IOMUX Select Register 1
GPIO0_IOC_GPIO0A_DS_0	0x0100	W	0x00000707	GPIO0A Driver Strength Register 0
GPIO0_IOC_GPIO0A_DS_1	0x0104	W	0x00000707	GPIO0A Driver Strength Register 1
GPIO0_IOC_GPIO0A_DS_2	0x0108	W	0x00000707	GPIO0A Driver Strength Register 2
GPIO0_IOC_GPIO0A_DS_3	0x010C	W	0x00000707	GPIO0A Driver Strength Register 3
GPIO0_IOC_GPIO0B_DS_0	0x0110	W	0x00000707	GPIO0B Driver Strength Register 0
GPIO0_IOC_GPIO0B_DS_1	0x0114	W	0x00000707	GPIO0B Driver Strength Register 1
GPIO0_IOC_GPIO0B_DS_2	0x0118	W	0x00000707	GPIO0B Driver Strength Register 2
GPIO0_IOC_GPIO0B_DS_3	0x011C	W	0x00000707	GPIO0B Driver Strength Register 3
GPIO0_IOC_GPIO0C_DS_0	0x0120	W	0x00000707	GPIO0C Driver Strength Register 0
GPIO0_IOC_GPIO0C_DS_1	0x0124	W	0x00000707	GPIO0C Driver Strength Register 1
GPIO0_IOC_GPIO0C_DS_2	0x0128	W	0x00000707	GPIO0C Driver Strength Register 2
GPIO0_IOC_GPIO0C_DS_3	0x012C	W	0x00000707	GPIO0C Driver Strength Register 3
GPIO0_IOC_GPIO0A_PULL	0x0200	W	0x0000AA99	GPIO0A Pull up/down Register

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Name	Offset	Size	Reset Value	Description
GPIO0_IOC_GPIO0B_PULL	0x0204	W	0x0000AAAA	GPIO0B Pull up/down Register
GPIO0_IOC_GPIO0C_PULL	0x0208	W	0x000052AA	GPIO0C Pull up/down Register
GPIO0_IOC_GPIO0A_IE	0x0300	W	0x000000FF	GPIO0A Input Enable Register
GPIO0_IOC_GPIO0B_IE	0x0304	W	0x000000FF	GPIO0B Input Enable Register
GPIO0_IOC_GPIO0C_IE	0x0308	W	0x000000DF	GPIO0C Input Enable Register
GPIO0_IOC_GPIO0A_SMT	0x0400	W	0x000000FF	GPIO0A Schmitt Trigger Register
GPIO0_IOC_GPIO0B_SMT	0x0404	W	0x000000FF	GPIO0B Schmitt Trigger Register
GPIO0_IOC_GPIO0C_SMT	0x0408	W	0x000000FF	GPIO0C Schmitt Trigger Register
GPIO0_IOC_GPIO0A_SUS	0x0500	W	0x00000000	GPIO0A SUS Register
GPIO0_IOC_GPIO0B_SUS	0x0504	W	0x00000000	GPIO0B SUS Register
GPIO0_IOC_GPIO0C_SUS	0x0508	W	0x00000000	GPIO0C SUS Register
GPIO0_IOC_GPIO0A_SL	0x0600	W	0x0000FFFF	GPIO0A Slew Rate Register
GPIO0_IOC_GPIO0B_SL	0x0604	W	0x0000FFFF	GPIO0B Slew Rate Register
GPIO0_IOC_GPIO0C_SL	0x0608	W	0x0000FFFF	GPIO0C Slew Rate Register
GPIO0_IOC_GPIO0A_OD	0x0700	W	0x00000000	GPIO0A Open-Drain Register
GPIO0_IOC_GPIO0B_OD	0x0704	W	0x00000000	GPIO0B Open-Drain Register
GPIO0_IOC_GPIO0C_OD	0x0708	W	0x00000000	GPIO0C Open-Drain Register
GPIO0_IOC_GPIO0_IDDQ	0x0800	W	0x00000000	GPIO0 IDDQ Register
GPIO0_IOC_GPIO0D_CON	0x0830	W	0x0000072C	GPIO0D0 Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.3.2 Detail Registers Description

GPIO0_IOC_GPIO0A_IOMUX_SEL_0

Address: Operational Base(0xFF950000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0a3_sel 4'h0: GPIO0_A3 4'h1: SAI0_SDO 4'h7: RM_IO3
11:8	RW	0x0	gpio0a2_sel 4'h0: GPIO0_A2 4'h1: SAI0_MCLK 4'h7: RM_IO2
7:4	RW	0x0	gpio0a1_sel 4'h0: GPIO0_A1 4'h1: SAI0_SCLK 4'h7: RM_IO1
3:0	RW	0x0	gpio0a0_sel 4'h0: GPIO0_A0 4'h1: SAI0_LRCK 4'h7: RM_IO0

GPIO0_IOC_GPIO0A_IOMUX_SEL_1

Address: Operational Base(0xFF950000) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0a7_sel 4'h0: GPIO0_A7 4'h1: SAI0_SDI3 4'h2: SPI1_CSN1 4'h7: RM_IO7
11:8	RW	0x0	gpio0a6_sel 4'h0: GPIO0_A6 4'h1: SAI0_SDI2 4'h7: RM_IO6
7:4	RW	0x0	gpio0a5_sel 4'h0: GPIO0_A5 4'h1: SAI0_SDI1 4'h7: RM_IO5
3:0	RW	0x0	gpio0a4_sel 4'h0: GPIO0_A4 4'h1: SAI0_SDI0 4'h7: RM_IO4

GPIO0_IOC_GPIO0B_IOMUX_SEL_0

Address: Operational Base(0xFF950000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0b3_sel 4'h0: GPIO0_B3 4'h1: SAI1_SDI 4'h7: RM_IO11
11:8	RW	0x0	gpio0b2_sel 4'h0: GPIO0_B2 4'h1: SAI1_LRCK 4'h2: SPI1_MISO 4'h7: RM_IO10
7:4	RW	0x0	gpio0b1_sel 4'h0: GPIO0_B1 4'h1: SAI1_SCLK 4'h2: SPI1_MOSI 4'h7: RM_IO9
3:0	RW	0x0	gpio0b0_sel 4'h0: GPIO0_B0 4'h1: SAI1_MCLK 4'h2: SPI1_CLK 4'h7: RM_IO8

GPIO0_IOC_GPIO0B_IOMUX_SEL_1

Address: Operational Base(0xFF950000) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0b7_sel 4'h0: GPIO0_B7 4'h1: SAI1_SDO3 4'h2: SPI0_CSN1 4'h7: RM_IO15
11:8	RW	0x0	gpio0b6_sel 4'h0: GPIO0_B6 4'h1: SAI1_SDO2 4'h2: SPI1_CSN0 4'h7: RM_IO14
7:4	RW	0x0	gpio0b5_sel 4'h0: GPIO0_B5 4'h1: SAI1_SDO1 4'h7: RM_IO13
3:0	RW	0x0	gpio0b4_sel 4'h0: GPIO0_B4 4'h1: SAI1_SDO0 4'h7: RM_IO12

GPIO0_IOC_GPIO0C_IOMUX_SEL_0

Address: Operational Base(0xFF950000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0c3_sel 4'h0: GPIO0_C3 4'h1: ETH_CLK1_25M_OUT 4'h2: SPI0_CSN0 4'h7: RM_IO19
11:8	RW	0x0	gpio0c2_sel 4'h0: GPIO0_C2 4'h1: REF_CLK1_OUT 4'h2: SPI0_MISO 4'h7: RM_IO18
7:4	RW	0x0	gpio0c1_sel 4'h0: GPIO0_C1 4'h2: SPI0_MOSI 4'h7: RM_IO17
3:0	RW	0x0	gpio0c0_sel 4'h0: GPIO0_C0 4'h2: SPI0_CLK 4'h7: RM_IO16

GPIO0_IOC_GPIO0C_IOMUX_SEL_1

Address: Operational Base(0xFF950000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0c7_sel 4'h0: GPIO0_C7 4'h1: UART0_RX 4'h2: JTAG_TMS_M1 4'h7: RM_IO23
11:8	RW	0x0	gpio0c6_sel 4'h0: GPIO0_C6 4'h1: UART0_TX 4'h2: JTAG_TCK_M1 4'h7: RM_IO22
7:4	RW	0x7	gpio0c5_sel 4'h0: GPIO0_C5 4'h1: CPU_AVS 4'h7: RM_IO21
3:0	RW	0x0	gpio0c4_sel 4'h0: GPIO0_C4 4'h1: ETH_CLK0_25M_OUT 4'h2: AUPLL_CLK_IN 4'h7: RM_IO20

GPIO0_IOC_GPIO0A_DS_0

Address: Operational Base(0xFF950000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0a1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0a0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0A_DS_1

Address: Operational Base(0xFF950000) + offset (0x0104)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0a3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0a2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0A_DS_2

Address: Operational Base(0xFF950000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0a5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0a4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

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GPIO0_IOC_GPIO0A_DS_3

Address: Operational Base(0xFF950000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0a7_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0a6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0B_DS_0

Address: Operational Base(0xFF950000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0b1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio0b0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0B_DS_1

Address: Operational Base(0xFF950000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0b3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0b2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0B_DS_2

Address: Operational Base(0xFF950000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio0b5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0b4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0B_DS_3

Address: Operational Base(0xFF950000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0b7_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0b6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0C_DS_0

Address: Operational Base(0xFF950000) + offset (0x0120)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0c1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0c0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0C_DS_1

Address: Operational Base(0xFF950000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0c3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0c2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

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GPIO0_IOC_GPIO0C_DS_2

Address: Operational Base(0xFF950000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0c5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0c4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0C_DS_3

Address: Operational Base(0xFF950000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0c7_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio0c6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO0_IOC_GPIO0A_PULL

Address: Operational Base(0xFF950000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio0a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio0a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio0a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio0a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio0a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x1	gpio0a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio0a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x1	gpio0a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO0_IOC_GPIO0B_PULL

Address: Operational Base(0xFF950000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio0b7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio0b6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio0b5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio0b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio0b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio0b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio0b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio0b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO0_IOC_GPIO0C_PULL

Address: Operational Base(0xFF950000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio0c7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x1	gpio0c6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x0	gpio0c5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio0c4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio0c3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio0c2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio0c1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio0c0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO0_IOC_GPIO0A_IE

Address: Operational Base(0xFF950000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0a7_ie Receiver enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio0a6_ie Receiver enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio0a5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio0a4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio0a3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio0a2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio0a1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio0a0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0B_IE

Address: Operational Base(0xFF950000) + offset (0x0304)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0b7_ie Receiver enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio0b6_ie Receiver enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio0b5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio0b4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio0b3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio0b2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio0b1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio0b0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0C_IE

Address: Operational Base(0xFF950000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0c7_ie Receiver enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio0c6_ie Receiver enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio0c5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio0c4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio0c3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio0c2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio0c1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio0c0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0A_SMT

Address: Operational Base(0xFF950000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0a7_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio0a6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio0a5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio0a4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio0a3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x1	gpio0a2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio0a1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio0a0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0B_SMT

Address: Operational Base(0xFF950000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0b7_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio0b6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio0b5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio0b4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio0b3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio0b2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio0b1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio0b0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0C_SMT

Rockchip Confidencial

Address: Operational Base(0xFF950000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0c7_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio0c6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio0c5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio0c4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio0c3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio0c2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio0c1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio0c0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0A_SUS

Address: Operational Base(0xFF950000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0a7_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio0a6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio0a5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio0a4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio0a3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio0a2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio0a1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio0a0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0B_SUS

Address: Operational Base(0xFF950000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0b7_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio0b6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio0b5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio0b4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio0b3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x0	gpio0b2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio0b1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio0b0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0C_SUS

Address: Operational Base(0xFF950000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0c7_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio0c6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio0c5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio0c4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio0c3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio0c2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio0c1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio0c0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0A_SL

Rockchip Confidencial

Address: Operational Base(0xFF950000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
13:12	RW	0x3	gpio0a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio0a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio0a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
7:6	RW	0x3	gpio0a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio0a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio0a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
1:0	RW	0x3	gpio0a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO0_IOC_GPIO0B_SL

Address: Operational Base(0xFF950000) + offset (0x0604)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0b7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
13:12	RW	0x3	gpio0b6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio0b5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio0b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
7:6	RW	0x3	gpio0b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio0b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio0b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
1:0	RW	0x3	gpio0b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO0_IOC_GPIO0C_SL

Address: Operational Base(0xFF950000) + offset (0x0608)

Rockchip Confidential

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0c7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
13:12	RW	0x3	gpio0c6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio0c5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio0c4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
7:6	RW	0x3	gpio0c3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio0c2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio0c1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
1:0	RW	0x3	gpio0c0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO0_IOC_GPIO0A_OD

Address: Operational Base(0xFF950000) + offset (0x0700)

Rockchip Confidential

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0a7_od For open drain functionality enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio0a6_od For open drain functionality enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio0a5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio0a4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio0a3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio0a2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio0a1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio0a0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0B_OD

Address: Operational Base(0xFF950000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0b7_od For open drain functionality enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio0b6_od For open drain functionality enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio0b5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio0b4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio0b3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio0b2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio0b1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio0b0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0C_OD

Address: Operational Base(0xFF950000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0c7_od For open drain functionality enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio0c6_od For open drain functionality enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio0c5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio0c4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio0c3_od For open drain functionality enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x0	gpio0c2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio0c1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio0c0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO0_IOC_GPIO0_IDDQ

Address: Operational Base(0xFF950000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	gpio0_iddq For IDDQ testing

GPIO0_IOC_GPIO0D_CON

Address: Operational Base(0xFF950000) + offset (0x0830)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:9	RW	0x3	gpio0d0_smt Schmitter trigger enable 2'b00: disable 2'b11: enable Others: Reserved
8	RW	0x1	gpio0d0_sl Slew rate control enable 1'b0: disable 1'b1: enable
7	RW	0x0	gpio0d0_he Hold enable 1'b0: diable 1'b1: enable
6	RW	0x0	gpio0d0_ps Weak pull down/up select for pad 1'b0: down 1'b1: up
5	RW	0x1	gpio0d0_pe Weak pull down/up enable for pad 1'b0: diable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4:3	RW	0x1	gpio0d0_ds The drive strength of IO. The weakest setting is 2'b00 and the strongest setting is 2'b11. 2'b00: Level0 2'b01: Level1 2'b10: Level2 2'b11: Level3
2	RW	0x1	gpio0d0_ie Receiver enable 1'b0: disable 1'b1: enable
1:0	RW	0x0	gpio0d0_sel 2'b00: GPIO0D0 2'b01: OSC_CLK_OUT 2'b10: REF_CLK0_OUT 2'b11: Reserved

18.4 GPIO1_IOC Register Description

18.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO1_IOC_GPIO1A_IOMUX_SEL_0	0x0020	W	0x00000000	GPIO1A IOMUX Select Register 0
GPIO1_IOC_GPIO1A_IOMUX_SEL_1	0x0024	W	0x00000000	GPIO1A IOMUX Select Register 1
GPIO1_IOC_GPIO1B_IOMUX_SEL_0	0x0028	W	0x00000000	GPIO1B IOMUX Select Register 0
GPIO1_IOC_GPIO1B_IOMUX_SEL_1	0x002C	W	0x00000000	GPIO1B IOMUX Select Register 1
GPIO1_IOC_GPIO1C_IOMUX_SEL_0	0x0030	W	0x00000000	GPIO1C IOMUX Select Register 0
GPIO1_IOC_GPIO1C_IOMUX_SEL_1	0x0034	W	0x00000000	GPIO1C IOMUX Select Register 1
GPIO1_IOC_GPIO1D_IOMUX_SEL_0	0x0038	W	0x00000000	GPIO1D IOMUX Select Register 0
GPIO1_IOC_GPIO1A_DS_0	0x0140	W	0x00000707	GPIO1A Driver Strength Register 0
GPIO1_IOC_GPIO1A_DS_1	0x0144	W	0x00000707	GPIO1A Driver Strength Register 1
GPIO1_IOC_GPIO1A_DS_2	0x0148	W	0x00000707	GPIO1A Driver Strength Register 2
GPIO1_IOC_GPIO1A_DS_3	0x014C	W	0x00000707	GPIO1A Driver Strength Register 3
GPIO1_IOC_GPIO1B_DS_0	0x0150	W	0x00000707	GPIO1B Driver Strength Register 0
GPIO1_IOC_GPIO1B_DS_1	0x0154	W	0x00000707	GPIO1B Driver Strength Register 1
GPIO1_IOC_GPIO1B_DS_2	0x0158	W	0x00000707	GPIO1B Driver Strength Register 2
GPIO1_IOC_GPIO1B_DS_3	0x015C	W	0x00000707	GPIO1B Driver Strength Register 3
GPIO1_IOC_GPIO1C_DS_0	0x0160	W	0x00000707	GPIO1C Driver Strength Register 0

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Name	Offset	Size	Reset Value	Description
GPIO1_IOC_GPIO1C_DS_1	0x0164	W	0x00000707	GPIO1C Driver Strength Register 1
GPIO1_IOC_GPIO1C_DS_2	0x0168	W	0x00000707	GPIO1C Driver Strength Register 2
GPIO1_IOC_GPIO1C_DS_3	0x016C	W	0x00000707	GPIO1C Driver Strength Register 3
GPIO1_IOC_GPIO1D_DS_0	0x0170	W	0x00000707	GPIO1D Driver Strength Register 0
GPIO1_IOC_GPIO1D_DS_1	0x0174	W	0x00000707	GPIO1D Driver Strength Register 1
GPIO1_IOC_GPIO1A_PULL	0x0210	W	0x0000AAAA	GPIO1A Pull up/down Register
GPIO1_IOC_GPIO1B_PULL	0x0214	W	0x0000AAAA	GPIO1B Pull up/down Register
GPIO1_IOC_GPIO1C_PULL	0x0218	W	0x0000AAAA	GPIO1C Pull up/down Register
GPIO1_IOC_GPIO1D_PULL	0x021C	W	0x000000AA	GPIO1D Pull up/down Register
GPIO1_IOC_GPIO1A_IE	0x0310	W	0x000000FF	GPIO1A Input Enable Register
GPIO1_IOC_GPIO1B_IE	0x0314	W	0x000000FF	GPIO1B Input Enable Register
GPIO1_IOC_GPIO1C_IE	0x0318	W	0x000000FF	GPIO1C Input Enable Register
GPIO1_IOC_GPIO1D_IE	0x031C	W	0x0000000F	GPIO1D Input Enable Register
GPIO1_IOC_GPIO1A_SMT	0x0410	W	0x000000FF	GPIO1A Schmitt Trigger Register
GPIO1_IOC_GPIO1B_SMT	0x0414	W	0x000000FF	GPIO1B Schmitt Trigger Register
GPIO1_IOC_GPIO1C_SMT	0x0418	W	0x000000FF	GPIO1C Schmitt Trigger Register
GPIO1_IOC_GPIO1D_SMT	0x041C	W	0x0000000F	GPIO1D Schmitt Trigger Register
GPIO1_IOC_GPIO1A_SUS	0x0510	W	0x00000000	GPIO1A SUS Register
GPIO1_IOC_GPIO1B_SUS	0x0514	W	0x00000000	GPIO1B SUS Register
GPIO1_IOC_GPIO1C_SUS	0x0518	W	0x00000000	GPIO1C SUS Register
GPIO1_IOC_GPIO1D_SUS	0x051C	W	0x00000000	GPIO1D SUS Register
GPIO1_IOC_GPIO1A_SL	0x0610	W	0x0000FFFF	GPIO1A Slew Rate Register
GPIO1_IOC_GPIO1B_SL	0x0614	W	0x0000FFFF	GPIO1B Slew Rate Register
GPIO1_IOC_GPIO1C_SL	0x0618	W	0x0000FFFF	GPIO1C Slew Rate Register
GPIO1_IOC_GPIO1D_SL	0x061C	W	0x000000FF	GPIO1D Slew Rate Register
GPIO1_IOC_GPIO1A_OD	0x0710	W	0x00000000	GPIO1A Open-Drain Register
GPIO1_IOC_GPIO1B_OD	0x0714	W	0x00000000	GPIO1B Open-Drain Register
GPIO1_IOC_GPIO1C_OD	0x0718	W	0x00000000	GPIO1C Open-Drain Register
GPIO1_IOC_GPIO1D_OD	0x071C	W	0x00000000	GPIO1D Open-Drain Register
GPIO1_IOC_GPIO1_IDDQ	0x0810	W	0x00000000	GPIO1 IDDQ Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.4.2 Detail Registers Description

GPIO1_IOC_GPIO1A_IOMUX_SEL_0

Address: Operational Base(0xFF660000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio1a3_sel 4'h0: GPIO1_A3 4'h1: VO_LCDC_CLK 4'h2: DSMC_D0 4'h3: FLEXBUS1_D3
11:8	RW	0x0	gpio1a2_sel 4'h0: GPIO1_A2 4'h1: VO_LCDC_HSYNC 4'h2: DSMC_DQS0 4'h3: FLEXBUS1_D2
7:4	RW	0x0	gpio1a1_sel 4'h0: GPIO1_A1 4'h1: VO_LCDC_VSYNC 4'h2: DSMC_CLKN 4'h3: FLEXBUS1_D1 4'h4: DSMC_INT0 4'h8: DSMC_SLV_INT
3:0	RW	0x0	gpio1a0_sel 4'h0: GPIO1_A0 4'h1: VO_LCDC_DEN 4'h2: DSMC_CLKP 4'h3: FLEXBUS1_D0

GPIO1_IOC_GPIO1A_IOMUX_SEL_1

Address: Operational Base(0xFF660000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1a7_sel 4'h0: GPIO1_A7 4'h1: VO_LCDC_D20 4'h2: DSMC_D4 4'h3: FLEXBUS1_D7
11:8	RW	0x0	gpio1a6_sel 4'h0: GPIO1_A6 4'h1: VO_LCDC_D21 4'h2: DSMC_D3 4'h3: FLEXBUS1_D6
7:4	RW	0x0	gpio1a5_sel 4'h0: GPIO1_A5 4'h1: VO_LCDC_D22 4'h2: DSMC_D2 4'h3: FLEXBUS1_D5
3:0	RW	0x0	gpio1a4_sel 4'h0: GPIO1_A4 4'h1: VO_LCDC_D23 4'h2: DSMC_D1 4'h3: FLEXBUS1_D4

GPIO1_IOC_GPIO1B_IOMUX_SEL_0

Address: Operational Base(0xFF660000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1b3_sel 4'h0: GPIO1_B3 4'h1: VO_LCDC_D16 4'h2: DSMC_INT3 4'h3: FLEXBUS1_D11 4'h4: FLEXBUS0_D14 4'h5: FLEXBUS1_CSN_M1 4'h6: SAI2_LRCK_M1 4'h7: RM_IO26
11:8	RW	0x0	gpio1b2_sel 4'h0: GPIO1_B2 4'h1: VO_LCDC_D17 4'h2: DSMC_INT2 4'h3: FLEXBUS1_D10 4'h4: FLEXBUS0_D15 4'h5: FLEXBUS0_CSN_M1 4'h6: SAI2_SCLK_M1 4'h7: RM_IO25
7:4	RW	0x0	gpio1b1_sel 4'h0: GPIO1_B1 4'h1: VO_LCDC_D18 4'h2: DSMC_CSN1 4'h3: FLEXBUS1_D9 4'h5: FLEXBUS1_CSN_M0 4'h6: UART5_CTSN_M1 4'h7: RM_IO24
3:0	RW	0x0	gpio1b0_sel 4'h0: GPIO1_B0 4'h1: VO_LCDC_D19 4'h2: DSMC_D5 4'h3: FLEXBUS1_D8 4'h5: FLEXBUS0_CSN_M0

GPIO1_IOC_GPIO1B_IOMUX_SEL_1

Address: Operational Base(0xFF660000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1b7_sel 4'h0: GPIO1_B7 4'h1: VO_LCDC_D12 4'h2: DSMC_RDYN 4'h3: FLEXBUS1_D15 4'h4: FLEXBUS0_D10 4'h5: FLEXBUS1_CSN_M3

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio1b6_sel 4'h0: GPIO1_B6 4'h1: VO_LCDC_D13 4'h2: DSMC_CSN0 4'h3: FLEXBUS1_D14 4'h4: FLEXBUS0_D11 4'h5: FLEXBUS0_CSN_M3
7:4	RW	0x0	gpio1b5_sel 4'h0: GPIO1_B5 4'h1: VO_LCDC_D14 4'h2: DSMC_D7 4'h3: FLEXBUS1_D13 4'h4: FLEXBUS0_D12 4'h5: FLEXBUS1_CSN_M2
3:0	RW	0x0	gpio1b4_sel 4'h0: GPIO1_B4 4'h1: VO_LCDC_D15 4'h2: DSMC_D6 4'h3: FLEXBUS1_D12 4'h4: FLEXBUS0_D13 4'h5: FLEXBUS0_CSN_M2

GPIO1_IOC_GPIO1C_IOMUX_SEL_0

Address: Operational Base(0xFF660000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1c3_sel 4'h0: GPIO1_C3 4'h1: VO_LCDC_D8 4'h2: DSMC_D10 4'h3: FLEXBUS0_D8 4'h5: FLEXBUS1_CSN_M5 4'h6: SAI2_SDO_M1 4'h7: RM_IO28 4'h8: DSMC_SLV_D1
11:8	RW	0x0	gpio1c2_sel 4'h0: GPIO1_C2 4'h1: VO_LCDC_D9 4'h2: DSMC_D9 4'h3: FLEXBUS0_D9 4'h4: DSM_AUD_RP_M0 4'h5: FLEXBUS0_CSN_M5 4'h6: SAI2_SDI_M1 4'h7: RM_IO27 4'h8: DSMC_SLV_D0

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio1c1_sel 4'h0: GPIO1_C1 4'h1: VO_LCDC_D10 4'h2: DSMC_D8 4'h3: FLEXBUS0_CLK 4'h4: DSM_AUD_RN_M0 4'h5: FLEXBUS1_CSN_M4 4'h6: SAI2_MCLK_M1 4'h8: DSMC_SLV_DQS0
3:0	RW	0x0	gpio1c0_sel 4'h0: GPIO1_C0 4'h1: VO_LCDC_D11 4'h2: DSMC_RESETN 4'h3: FLEXBUS1_CLK 4'h4: DSMC_INT1 4'h5: FLEXBUS0_CSN_M4 4'h8: DSMC_SLV_CLK

GPIO1_IOC_GPIO1C_IOMUX_SEL_1

Address: Operational Base(0xFF660000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1c7_sel 4'h0: GPIO1_C7 4'h1: VO_LCDC_D4 4'h2: DSMC_D14 4'h3: FLEXBUS0_D4 4'h8: DSMC_SLV_D5
11:8	RW	0x0	gpio1c6_sel 4'h0: GPIO1_C6 4'h1: VO_LCDC_D5 4'h2: DSMC_D13 4'h3: FLEXBUS0_D5 4'h8: DSMC_SLV_D4
7:4	RW	0x0	gpio1c5_sel 4'h0: GPIO1_C5 4'h1: VO_LCDC_D6 4'h2: DSMC_D12 4'h3: FLEXBUS0_D6 4'h8: DSMC_SLV_D3
3:0	RW	0x0	gpio1c4_sel 4'h0: GPIO1_C4 4'h1: VO_LCDC_D7 4'h2: DSMC_D11 4'h3: FLEXBUS0_D7 4'h8: DSMC_SLV_D2

GPIO1_IOC_GPIO1D_IOMUX_SEL_0

Address: Operational Base(0xFF660000) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1d3_sel 4'h0: GPIO1_D3 4'h1: VO_LCDC_D0 4'h2: DSMC_CSN3 4'h3: FLEXBUS0_D0 4'h6: UART5_RX_M1 4'h7: RM_IO31 4'h8: DSMC_SLV_RDYN
11:8	RW	0x0	gpio1d2_sel 4'h0: GPIO1_D2 4'h1: VO_LCDC_D1 4'h2: DSMC_CSN2 4'h3: FLEXBUS0_D1 4'h6: UART5_TX_M1 4'h7: RM_IO30 4'h8: DSMC_SLV_CSN0
7:4	RW	0x0	gpio1d1_sel 4'h0: GPIO1_D1 4'h1: VO_LCDC_D2 4'h2: DSMC_DQS1 4'h3: FLEXBUS0_D2 4'h4: DSM_AUD_LP_M0 4'h6: UART5_RTSN_M1 4'h7: RM_IO29 4'h8: DSMC_SLV_D7
3:0	RW	0x0	gpio1d0_sel 4'h0: GPIO1_D0 4'h1: VO_LCDC_D3 4'h2: DSMC_D15 4'h3: FLEXBUS0_D3 4'h4: DSM_AUD_LN_M0 4'h8: DSMC_SLV_D6

GPIO1_IOC_GPIO1A_DS_0

Address: Operational Base(0xFF660000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1a1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio1a0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1A_DS_1

Address: Operational Base(0xFF660000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1a3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1a2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1A_DS_2

Address: Operational Base(0xFF660000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio1a5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1a4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1A_DS_3

Address: Operational Base(0xFF660000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1a7_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1a6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1B_DS_0

Address: Operational Base(0xFF660000) + offset (0x0150)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1b1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1b0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1B_DS_1

Address: Operational Base(0xFF660000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1b3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1b2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

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GPIO1_IOC_GPIO1B_DS_2

Address: Operational Base(0xFF660000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1b5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1b4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1B_DS_3

Address: Operational Base(0xFF660000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1b7_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio1b6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1C_DS_0

Address: Operational Base(0xFF660000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1c1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1c0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1C_DS_1

Address: Operational Base(0xFF660000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio1c3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1c2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1C_DS_2

Address: Operational Base(0xFF660000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1c5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1c4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1C_DS_3

Address: Operational Base(0xFF660000) + offset (0x016C)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1c7_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1c6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1D_DS_0

Address: Operational Base(0xFF660000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1d1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1d0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

Rockchip Confidencial

GPIO1_IOC_GPIO1D_DS_1

Address: Operational Base(0xFF660000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1d3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1d2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO1_IOC_GPIO1A_PULL

Address: Operational Base(0xFF660000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio1a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio1a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio1a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio1a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio1a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio1a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio1a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio1a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO1_IOC_GPIO1B_PULL

Address: Operational Base(0xFF660000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio1b7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio1b6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio1b5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio1b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio1b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio1b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio1b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio1b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO1_IOC_GPIO1C_PULL

Address: Operational Base(0xFF660000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio1c7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio1c6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio1c5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

Rockchip Confidencial

Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio1c4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio1c3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio1c2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio1c1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio1c0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO1_IOC_GPIO1D_PULL

Address: Operational Base(0xFF660000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x2	gpio1d3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio1d2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

Rockchip Confidencial

Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio1d1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio1d0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO1_IOC_GPIO1A_IE

Address: Operational Base(0xFF660000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1a7_ie Receiver enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio1a6_ie Receiver enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio1a5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio1a4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio1a3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio1a2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio1a1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio1a0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1B_IE

Address: Operational Base(0xFF660000) + offset (0x0314)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1b7_ie Receiver enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio1b6_ie Receiver enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio1b5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio1b4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio1b3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio1b2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio1b1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio1b0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1C_IE

Address: Operational Base(0xFF660000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1c7_ie Receiver enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio1c6_ie Receiver enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x1	gpio1c5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio1c4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio1c3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio1c2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio1c1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio1c0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1D_IE

Address: Operational Base(0xFF660000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	gpio1d3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio1d2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio1d1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio1d0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1A_SMT

Address: Operational Base(0xFF660000) + offset (0x0410)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1a7_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio1a6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio1a5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio1a4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio1a3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio1a2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio1a1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio1a0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1B_SMT

Address: Operational Base(0xFF660000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1b7_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio1b6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x1	gpio1b5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio1b4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio1b3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio1b2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio1b1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio1b0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1C_SMT

Address: Operational Base(0xFF660000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1c7_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio1c6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio1c5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio1c4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio1c3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x1	gpio1c2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio1c1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio1c0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1D_SMT

Address: Operational Base(0xFF660000) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	gpio1d3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio1d2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio1d1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio1d0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1A_SUS

Address: Operational Base(0xFF660000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio1a6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio1a5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio1a4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio1a3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio1a2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio1a1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio1a0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1B_SUS

Address: Operational Base(0xFF660000) + offset (0x0514)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio1b6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio1b5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio1b4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio1b3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x0	gpio1b2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio1b1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio1b0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1C_SUS

Address: Operational Base(0xFF660000) + offset (0x0518)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1c7_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio1c6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio1c5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio1c4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio1c3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio1c2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio1c1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio1c0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1D_SUS

Rockchip Confidencial

Address: Operational Base(0xFF660000) + offset (0x051C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	gpio1d3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio1d2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio1d1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio1d0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1A_SL

Address: Operational Base(0xFF660000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio1a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
13:12	RW	0x3	gpio1a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio1a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio1a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7:6	RW	0x3	gpio1a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio1a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio1a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
1:0	RW	0x3	gpio1a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO1_IOC_GPIO1B_SL

Address: Operational Base(0xFF660000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio1b7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
13:12	RW	0x3	gpio1b6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio1b5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio1b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

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Bit	Attr	Reset Value	Description
7:6	RW	0x3	gpio1b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio1b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio1b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
1:0	RW	0x3	gpio1b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO1_IOC_GPIO1C_SL

Address: Operational Base(0xFF660000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio1c7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
13:12	RW	0x3	gpio1c6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio1c5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio1c4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

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Bit	Attr	Reset Value	Description
7:6	RW	0x3	gpio1c3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio1c2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio1c1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
1:0	RW	0x3	gpio1c0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO1_IOC_GPIO1D_SL

Address: Operational Base(0xFF660000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x3	gpio1d3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio1d2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio1d1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

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Bit	Attr	Reset Value	Description
1:0	RW	0x3	gpio1d0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO1_IOC_GPIO1A_OD

Address: Operational Base(0xFF660000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_od For open drain functionality enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio1a6_od For open drain functionality enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio1a5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio1a4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio1a3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio1a2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio1a1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio1a0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1B_OD

Address: Operational Base(0xFF660000) + offset (0x0714)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_od For open drain functionality enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio1b6_od For open drain functionality enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio1b5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio1b4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio1b3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio1b2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio1b1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio1b0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1C_OD

Address: Operational Base(0xFF660000) + offset (0x0718)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1c7_od For open drain functionality enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio1c6_od For open drain functionality enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio1c5_od For open drain functionality enable 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	gpio1c4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio1c3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio1c2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio1c1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio1c0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1D_OD

Address: Operational Base(0xFF660000) + offset (0x071C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	gpio1d3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio1d2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio1d1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio1d0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO1_IOC_GPIO1_IDDQ

Address: Operational Base(0xFF660000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	gpio1_iddq For IDDQ testing

18.5 GPIO2_IOC Register Description

18.5.1 Registers Summary

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Name	Offset	Size	Reset Value	Description
GPIO2_IOC_GPIO2A_IOMUX_SEL_0	0x0040	W	0x00000000	GPIO2A IOMUX Select Register 0
GPIO2_IOC_GPIO2A_IOMUX_SEL_1	0x0044	W	0x00000000	GPIO2A IOMUX Select Register 1
GPIO2_IOC_GPIO2B_IOMUX_SEL_0	0x0048	W	0x00000000	GPIO2B IOMUX Select Register 0
GPIO2_IOC_GPIO2B_IOMUX_SEL_1	0x004C	W	0x00000000	GPIO2B IOMUX Select Register 1
GPIO2_IOC_GPIO2C_IOMUX_SEL_0	0x0050	W	0x00000000	GPIO2C IOMUX Select Register 0
GPIO2_IOC_GPIO2A_DS_0	0x0180	W	0x00000F07	GPIO2A Driver Strength Register 0
GPIO2_IOC_GPIO2A_DS_1	0x0184	W	0x00000707	GPIO2A Driver Strength Register 1
GPIO2_IOC_GPIO2A_DS_2	0x0188	W	0x00000707	GPIO2A Driver Strength Register 2
GPIO2_IOC_GPIO2B_DS_0	0x0190	W	0x00000707	GPIO2B Driver Strength Register 0
GPIO2_IOC_GPIO2B_DS_1	0x0194	W	0x00000707	GPIO2B Driver Strength Register 1
GPIO2_IOC_GPIO2B_DS_2	0x0198	W	0x00000707	GPIO2B Driver Strength Register 2
GPIO2_IOC_GPIO2B_DS_3	0x019C	W	0x00000707	GPIO2B Driver Strength Register 3
GPIO2_IOC_GPIO2C_DS_0	0x01A0	W	0x00000007	GPIO2C Driver Strength Register 0
GPIO2_IOC_GPIO2A_PULL	0x0220	W	0x00000559	GPIO2A Pull up/down Register
GPIO2_IOC_GPIO2B_PULL	0x0224	W	0x0000AAAA	GPIO2B Pull up/down Register
GPIO2_IOC_GPIO2C_PULL	0x0228	W	0x00000002	GPIO2C Pull up/down Register
GPIO2_IOC_GPIO2A_IE	0x0320	W	0x0000003F	GPIO2A Input Enable Register
GPIO2_IOC_GPIO2B_IE	0x0324	W	0x000000FF	GPIO2B Input Enable Register
GPIO2_IOC_GPIO2C_IE	0x0328	W	0x00000001	GPIO2C Input Enable Register
GPIO2_IOC_GPIO2A_SMT	0x0420	W	0x0000003F	GPIO2A Schmitt Trigger Register
GPIO2_IOC_GPIO2B_SMT	0x0424	W	0x000000FF	GPIO2B Schmitt Trigger Register
GPIO2_IOC_GPIO2C_SMT	0x0428	W	0x00000001	GPIO2C Schmitt Trigger Register
GPIO2_IOC_GPIO2A_SUS	0x0520	W	0x00000000	GPIO2A SUS Register
GPIO2_IOC_GPIO2B_SUS	0x0524	W	0x00000000	GPIO2B SUS Register
GPIO2_IOC_GPIO2C_SUS	0x0528	W	0x00000000	GPIO2C SUS Register
GPIO2_IOC_GPIO2A_SL	0x0620	W	0x00000FFF	GPIO2A Slew Rate Register
GPIO2_IOC_GPIO2B_SL	0x0624	W	0x0000FFFF	GPIO2B Slew Rate Register
GPIO2_IOC_GPIO2C_SL	0x0628	W	0x00000003	GPIO2C Slew Rate Register
GPIO2_IOC_GPIO2A_OD	0x0720	W	0x00000000	GPIO2A Open-Drain Register
GPIO2_IOC_GPIO2B_OD	0x0724	W	0x00000000	GPIO2B Open-Drain Register
GPIO2_IOC_GPIO2C_OD	0x0728	W	0x00000000	GPIO2C Open-Drain Register
GPIO2_IOC_GPIO2_IDDQ	0x0820	W	0x00000000	GPIO2 IDDQ Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.5.2 Detail Registers Description

GPIO2_IOC_GPIO2A_IOMUX_SEL_0

Address: Operational Base(0xFF4D8000) + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2a3_sel 4'h0: GPIO2_A3 4'h1: FSPI_D1
11:8	RW	0x0	gpio2a2_sel 4'h0: GPIO2_A2 4'h1: FSPI_D0
7:4	RW	0x0	gpio2a1_sel 4'h0: GPIO2_A1 4'h1: FSPI_CLK
3:0	RW	0x0	gpio2a0_sel 4'h0: GPIO2_A0 4'h1: FSPI_CSN

GPIO2_IOC_GPIO2A_IOMUX_SEL_1

Address: Operational Base(0xFF4D8000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio2a5_sel 4'h0: GPIO2_A5 4'h1: FSPI_D3
3:0	RW	0x0	gpio2a4_sel 4'h0: GPIO2_A4 4'h1: FSPI_D2

GPIO2_IOC_GPIO2B_IOMUX_SEL_0

Address: Operational Base(0xFF4D8000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2b3_sel 4'h0: GPIO2_B3 4'h1: ETH_RMII0_TXD0 4'h2: SPI2_MISO
11:8	RW	0x0	gpio2b2_sel 4'h0: GPIO2_B2 4'h1: ETH_RMII0_CLK 4'h2: SPI2_MOSI
7:4	RW	0x0	gpio2b1_sel 4'h0: GPIO2_B1 4'h1: ETH_RMII0_RXD1 4'h2: SPI2_CSN
3:0	RW	0x0	gpio2b0_sel 4'h0: GPIO2_B0 4'h1: ETH_RMII0_RXD0 4'h2: SPI2_CLK

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GPIO2_IOC_GPIO2B_IOMUX_SEL_1

Address: Operational Base(0xFF4D8000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2b7_sel 4'h0: GPIO2_B7 4'h1: ETH_RMII0_MDIO 4'h2: DSM_AUD_LP_M1 4'h3: SAI3_SDO
11:8	RW	0x0	gpio2b6_sel 4'h0: GPIO2_B6 4'h1: ETH_RMII0_MDC 4'h2: DSM_AUD_LN_M1 4'h3: SAI3_SDI
7:4	RW	0x0	gpio2b5_sel 4'h0: GPIO2_B5 4'h1: ETH_RMII0_TXEN 4'h2: DSM_AUD_RP_M1 4'h3: SAI3_LRCK
3:0	RW	0x0	gpio2b4_sel 4'h0: GPIO2_B4 4'h1: ETH_RMII0_TXD1 4'h2: DSM_AUD_RN_M1 4'h3: SAI3_SCLK

GPIO2_IOC_GPIO2C_IOMUX_SEL_0

Address: Operational Base(0xFF4D8000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x0	gpio2c0_sel 4'h0: GPIO2_C0 4'h1: ETH_RMII0_RXDVCRS 4'h3: SAI3_MCLK

GPIO2_IOC_GPIO2A_DS_0

Address: Operational Base(0xFF4D8000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio2a1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio2a0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO2_IOC_GPIO2A_DS_1

Address: Operational Base(0xFF4D8000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio2a3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio2a2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO2_IOC_GPIO2A_DS_2

Address: Operational Base(0xFF4D8000) + offset (0x0188)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio2a5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio2a4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO2_IOC_GPIO2B_DS_0

Address: Operational Base(0xFF4D8000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio2b1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio2b0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

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GPIO2_IOC_GPIO2B_DS_1

Address: Operational Base(0xFF4D8000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio2b3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio2b2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO2_IOC_GPIO2B_DS_2

Address: Operational Base(0xFF4D8000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio2b5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio2b4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO2_IOC_GPIO2B_DS_3

Address: Operational Base(0xFF4D8000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio2b7_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio2b6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO2_IOC_GPIO2C_DS_0

Address: Operational Base(0xFF4D8000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio2c0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO2_IOC_GPIO2A_PULL

Address: Operational Base(0xFF4D8000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x1	gpio2a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x1	gpio2a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x1	gpio2a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x1	gpio2a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio2a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x1	gpio2a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

Rockchip Confidencial

GPIO2_IOC_GPIO2B_PULL

Address: Operational Base(0xFF4D8000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio2b7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio2b6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio2b5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio2b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio2b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio2b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio2b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio2b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO2_IOC_GPIO2C_PULL

Rockchip Confidencial

Address: Operational Base(0xFF4D8000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x2	gpio2c0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO2_IOC_GPIO2A_IE

Address: Operational Base(0xFF4D8000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio2a5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio2a4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio2a3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio2a2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio2a1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio2a0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2B_IE

Address: Operational Base(0xFF4D8000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
7	RW	0x1	gpio2b7_ie Receiver enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio2b6_ie Receiver enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio2b5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio2b4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio2b3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio2b2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio2b1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio2b0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2C_IE

Address: Operational Base(0xFF4D8000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	gpio2c0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2A_SMT

Address: Operational Base(0xFF4D8000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x1	gpio2a5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio2a4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio2a3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio2a2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio2a1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio2a0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2B_SMT

Address: Operational Base(0xFF4D8000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio2b7_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio2b6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio2b5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio2b4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio2b3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x1	gpio2b2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio2b1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio2b0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2C_SMT

Address: Operational Base(0xFF4D8000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	gpio2c0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2A_SUS

Address: Operational Base(0xFF4D8000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	gpio2a5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio2a4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio2a3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio2a2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio2a1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RW	0x0	gpio2a0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2B_SUS

Address: Operational Base(0xFF4D8000) + offset (0x0524)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio2b7_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio2b6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio2b5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio2b4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio2b3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio2b2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio2b1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio2b0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2C_SUS

Address: Operational Base(0xFF4D8000) + offset (0x0528)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpio2c0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2A_SL

Address: Operational Base(0xFF4D8000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x3	gpio2a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio2a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
7:6	RW	0x3	gpio2a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio2a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio2a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
1:0	RW	0x3	gpio2a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO2_IOC_GPIO2B_SL

Address: Operational Base(0xFF4D8000) + offset (0x0624)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio2b7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
13:12	RW	0x3	gpio2b6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio2b5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio2b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
7:6	RW	0x3	gpio2b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio2b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio2b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
1:0	RW	0x3	gpio2b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO2_IOC_GPIO2C_SL

Address: Operational Base(0xFF4D8000) + offset (0x0628)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x3	gpio2c0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO2_IOC_GPIO2A_OD

Address: Operational Base(0xFF4D8000) + offset (0x0720)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	gpio2a5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio2a4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio2a3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio2a2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio2a1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio2a0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2B_OD

Address: Operational Base(0xFF4D8000) + offset (0x0724)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	gpio2b7_od For open drain functionality enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio2b6_od For open drain functionality enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio2b5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio2b4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio2b3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio2b2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio2b1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio2b0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2C_OD

Address: Operational Base(0xFF4D8000) + offset (0x0728)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	gpio2c0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO2_IOC_GPIO2_IDDQ

Address: Operational Base(0xFF4D8000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	gpio2bc_iddq For IDDQ testing
0	RW	0x0	gpio2a_iddq For IDDQ testing

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18.6 GPIO3_IOC Register Description

18.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO3_IOC_GPIO3A_IOMUX_SEL_0	0x0060	W	0x00000000	GPIO3A IOMUX Select Register 0
GPIO3_IOC_GPIO3A_IOMUX_SEL_1	0x0064	W	0x00000022	GPIO3A IOMUX Select Register 1
GPIO3_IOC_GPIO3B_IOMUX_SEL_0	0x0068	W	0x00000000	GPIO3B IOMUX Select Register 0
GPIO3_IOC_GPIO3B_IOMUX_SEL_1	0x006C	W	0x00000000	GPIO3B IOMUX Select Register 1
GPIO3_IOC_GPIO3A_DS_0	0x01C0	W	0x0000070F	GPIO3A Driver Strength Register 0
GPIO3_IOC_GPIO3A_DS_1	0x01C4	W	0x00000707	GPIO3A Driver Strength Register 1
GPIO3_IOC_GPIO3A_DS_2	0x01C8	W	0x00000707	GPIO3A Driver Strength Register 2
GPIO3_IOC_GPIO3A_DS_3	0x01CC	W	0x00000707	GPIO3A Driver Strength Register 3
GPIO3_IOC_GPIO3B_DS_0	0x01D0	W	0x00000707	GPIO3B Driver Strength Register 0
GPIO3_IOC_GPIO3B_DS_1	0x01D4	W	0x00000707	GPIO3B Driver Strength Register 1
GPIO3_IOC_GPIO3B_DS_2	0x01D8	W	0x00000707	GPIO3B Driver Strength Register 2
GPIO3_IOC_GPIO3B_DS_3	0x01DC	W	0x00000007	GPIO3B Driver Strength Register 3
GPIO3_IOC_GPIO3A_PULL	0x0230	W	0x0000AAAA	GPIO3A Pull up/down Register
GPIO3_IOC_GPIO3B_PULL	0x0234	W	0x00002AAA	GPIO3B Pull up/down Register
GPIO3_IOC_GPIO3A_IE	0x0330	W	0x000000FF	GPIO3A Input Enable Register
GPIO3_IOC_GPIO3B_IE	0x0334	W	0x0000007F	GPIO3B Input Enable Register
GPIO3_IOC_GPIO3A_SMT	0x0430	W	0x000000FF	GPIO3A Schmitt Trigger Register
GPIO3_IOC_GPIO3B_SMT	0x0434	W	0x0000007F	GPIO3B Schmitt Trigger Register
GPIO3_IOC_GPIO3A_SUS	0x0530	W	0x00000000	GPIO3A SUS Register
GPIO3_IOC_GPIO3B_SUS	0x0534	W	0x00000000	GPIO3B SUS Register
GPIO3_IOC_GPIO3A_SL	0x0630	W	0x0000FFFF	GPIO3A Slew Rate Register
GPIO3_IOC_GPIO3B_SL	0x0634	W	0x00003FFF	GPIO3B Slew Rate Register
GPIO3_IOC_GPIO3A_OD	0x0730	W	0x00000000	GPIO3A Open-Drain Register
GPIO3_IOC_GPIO3B_OD	0x0734	W	0x00000000	GPIO3B Open-Drain Register
GPIO3_IOC_GPIO3_IDDQ	0x0820	W	0x00000000	GPIO3 IDDQ Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.6.2 Detail Registers Description

GPIO3_IOC_GPIO3A_IOMUX_SEL_0

Address: Operational Base(0xFF4D8000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3a3_sel 4'h0: GPIO3_A3 4'h1: SDMMC_D1 4'h2: TEST_CLK_OUT
11:8	RW	0x0	gpio3a2_sel 4'h0: GPIO3_A2 4'h1: SDMMC_D0
7:4	RW	0x0	gpio3a1_sel 4'h0: GPIO3_A1 4'h1: SDMMC_CMD
3:0	RW	0x0	gpio3a0_sel 4'h0: GPIO3_A0 4'h1: SDMMC_CLK

GPIO3_IOC_GPIO3A_IOMUX_SEL_1

Address: Operational Base(0xFF4D8000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3a7_sel 4'h0: GPIO3_A7 4'h1: SAI2_SCLK_M0 4'h2: ETH_RMII1_RXD1
11:8	RW	0x0	gpio3a6_sel 4'h0: GPIO3_A6 4'h1: SAI2_SDI_M0 4'h2: ETH_RMII1_RXD0
7:4	RW	0x2	gpio3a5_sel 4'h0: GPIO3_A5 4'h1: SDMMC_D3 4'h2: JTAG_TMS_M0
3:0	RW	0x2	gpio3a4_sel 4'h0: GPIO3_A4 4'h1: SDMMC_D2 4'h2: JTAG_TCK_M0

GPIO3_IOC_GPIO3B_IOMUX_SEL_0

Address: Operational Base(0xFF4D8000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3b3_sel 4'h0: GPIO3_B3 4'h1: UART5_RX_M0 4'h2: ETH_RMII1_TXEN
11:8	RW	0x0	gpio3b2_sel 4'h0: GPIO3_B2 4'h1: UART5_CTSN_M0 4'h2: ETH_RMII1_TXD1

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio3b1_sel 4'h0: GPIO3_B1 4'h1: SAI2_LRCK_M0 4'h2: ETH_RMII1_TXD0
3:0	RW	0x0	gpio3b0_sel 4'h0: GPIO3_B0 4'h1: SAI2_SDO_M0 4'h2: ETH_RMII1_CLK

GPIO3_IOC_GPIO3B_IOMUX_SEL_1

Address: Operational Base(0xFF4D8000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x0	gpio3b6_sel 4'h0: GPIO3_B6 4'h1: SAI2_MCLK_M0 4'h2: ETH_RMII1_RXDVCRS
7:4	RW	0x0	gpio3b5_sel 4'h0: GPIO3_B5 4'h1: UART5_RTSN_M0 4'h2: ETH_RMII1_MDIO
3:0	RW	0x0	gpio3b4_sel 4'h0: GPIO3_B4 4'h1: UART5_TX_M0 4'h2: ETH_RMII1_MDC

GPIO3_IOC_GPIO3A_DS_0

Address: Operational Base(0xFF4D8000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3a1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio3a0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO3_IOC_GPIO3A_DS_1

Address: Operational Base(0xFF4D8000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3a3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3a2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO3_IOC_GPIO3A_DS_2

Address: Operational Base(0xFF4D8000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio3a5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3a4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO3_IOC_GPIO3A_DS_3

Address: Operational Base(0xFF4D8000) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3a7_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3a6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO3_IOC_GPIO3B_DS_0

Address: Operational Base(0xFF4D8000) + offset (0x01D0)

Rockchip Confidencial

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3b1_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3b0_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO3_IOC_GPIO3B_DS_1

Address: Operational Base(0xFF4D8000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3b3_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3b2_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

Rockchip Confidencial

GPIO3_IOC_GPIO3B_DS_2

Address: Operational Base(0xFF4D8000) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3b5_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3b4_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO3_IOC_GPIO3B_DS_3

Address: Operational Base(0xFF4D8000) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x07	gpio3b6_ds The drive strength of IO. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0 6'b000011: Level1 6'b000111: Level2 6'b001111: Level3 6'b011111: Level4 6'b111111: Level5

GPIO3_IOC_GPIO3A_PULL

Address: Operational Base(0xFF4D8000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x2	gpio3a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio3a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio3a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio3a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio3a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio3a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio3a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio3a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO3_IOC_GPIO3B_PULL

Address: Operational Base(0xFF4D8000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:12	RW	0x2	gpio3b6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio3b5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio3b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio3b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio3b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio3b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio3b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO3_IOC_GPIO3A_IE

Address: Operational Base(0xFF4D8000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3a7_ie Receiver enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
6	RW	0x1	gpio3a6_ie Receiver enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio3a5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio3a4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio3a3_ie Receiver enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio3a2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio3a1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio3a0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO3_IOC_GPIO3B_IE

Address: Operational Base(0xFF4D8000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x1	gpio3b6_ie Receiver enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio3b5_ie Receiver enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio3b4_ie Receiver enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio3b3_ie Receiver enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
2	RW	0x1	gpio3b2_ie Receiver enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio3b1_ie Receiver enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio3b0_ie Receiver enable 1'b0: disable 1'b1: enable

GPIO3_IOC_GPIO3A_SMT

Address: Operational Base(0xFF4D8000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3a7_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
6	RW	0x1	gpio3a6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio3a5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio3a4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio3a3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio3a2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio3a1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio3a0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO3_IOC_GPIO3B_SMT

Rockchip Confidencial

Address: Operational Base(0xFF4D8000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x1	gpio3b6_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
5	RW	0x1	gpio3b5_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
4	RW	0x1	gpio3b4_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
3	RW	0x1	gpio3b3_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
2	RW	0x1	gpio3b2_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
1	RW	0x1	gpio3b1_smt Schmitt trigger enable 1'b0: disable 1'b1: enable
0	RW	0x1	gpio3b0_smt Schmitt trigger enable 1'b0: disable 1'b1: enable

GPIO3_IOC_GPIO3A_SUS

Address: Operational Base(0xFF4D8000) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio3a6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio3a5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
4	RW	0x0	gpio3a4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio3a3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio3a2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio3a1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio3a0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO3_IOC_GPIO3B_SUS

Address: Operational Base(0xFF4D8000) + offset (0x0534)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	gpio3b6_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio3b5_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio3b4_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio3b3_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio3b2_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio3b1_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
0	RW	0x0	gpio3b0_sus Weak pull keeper for pad enable 1'b0: disable 1'b1: enable

GPIO3_IOC_GPIO3A_SL

Address: Operational Base(0xFF4D8000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio3a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
13:12	RW	0x3	gpio3a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio3a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio3a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
7:6	RW	0x3	gpio3a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio3a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio3a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

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Bit	Attr	Reset Value	Description
1:0	RW	0x3	gpio3a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO3_IOC_GPIO3B_SL

Address: Operational Base(0xFF4D8000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x3	gpio3b6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
11:10	RW	0x3	gpio3b5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
9:8	RW	0x3	gpio3b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
7:6	RW	0x3	gpio3b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
5:4	RW	0x3	gpio3b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest
3:2	RW	0x3	gpio3b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

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Bit	Attr	Reset Value	Description
1:0	RW	0x3	gpio3b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: slowest 2'b11: fastest

GPIO3_IOC_GPIO3A_OD

Address: Operational Base(0xFF4D8000) + offset (0x0730)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_od For open drain functionality enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio3a6_od For open drain functionality enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio3a5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio3a4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio3a3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio3a2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio3a1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio3a0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO3_IOC_GPIO3B_OD

Address: Operational Base(0xFF4D8000) + offset (0x0734)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Rockchip Confidencial

Bit	Attr	Reset Value	Description
15:7	RO	0x000	reserved
6	RW	0x0	gpio3b6_od For open drain functionality enable 1'b0: disable 1'b1: enable
5	RW	0x0	gpio3b5_od For open drain functionality enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio3b4_od For open drain functionality enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio3b3_od For open drain functionality enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio3b2_od For open drain functionality enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio3b1_od For open drain functionality enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio3b0_od For open drain functionality enable 1'b0: disable 1'b1: enable

GPIO3_IOC_GPIO3_IDDQ

Address: Operational Base(0xFF4D8000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	gpio3_iddq For IDDQ testing
1:0	RO	0x0	reserved

18.7 GPIO4_IOC Register Description

18.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO4_IOC_SARADC_CON	0x0840	W	0x00001700	GPIO SARADC Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.7.2 Detail Registers Description

GPIO4_IOC_SARADC_CON

Address: Operational Base(0xFF4D8000) + offset (0x0840)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Rockchip Confidencial

Bit	Attr	Reset Value	Description
14	RW	0x0	gpio_saradc_ps Weak pull down/up select of IO SARADC_IN0_BOOT/GPIO4_B0_z~SARADC_IN3/GPIO4_B3_z. 1'b0: down 1'b1: up
13	RW	0x0	gpio_saradc_pe Weak pull down/up enable of IO SARADC_IN0_BOOT/GPIO4_B0_z~SARADC_IN3/GPIO4_B3_z. 1'b0: disable 1'b1: enable
12	RW	0x1	gpio_saradc_sl Slew rate control enable of IO SARADC_IN0_BOOT/GPIO4_B0_z~SARADC_IN3/GPIO4_B3_z. 1'b0: disable 1'b1: enable
11:10	RW	0x1	gpio_saradc_ds The drive strength of IO SARADC_IN0_BOOT/GPIO4_B0_z~SARADC_IN3/GPIO4_B3_z. The weakest setting is 2'b00 and the strongest setting is 2'b11. 2'b00: Level0 2'b01: Level1 2'b10: Level2 2'b11: Level3
9:8	RW	0x3	gpio_saradc_smt Schmitter trigger enable of IO SARADC_IN0_BOOT/GPIO4_B0_z~SARADC_IN3/GPIO4_B3_z. 2'b00: disable 2'b11: enable Others: Reserved
7:4	RW	0x0	gpio_saradc_ie Receiver enable of IO SARADC_IN0_BOOT/GPIO4_B0_z~SARADC_IN3/GPIO4_B3_z, each bits for one IO. 1'b0: disable 1'b1: enable
3:0	RW	0x0	gpio_saradc_he Hold enable of IO SARADC_IN0_BOOT/GPIO4_B0_z~SARADC_IN3/GPIO4_B3_z, each bits for one IO. 1'b0: disable 1'b1: enable

18.8 Application Notes

IOC is usually connected to a functional IP in the following ways (take input as an example):

1) As shown in following figure, the IO PAD connects directly to the function IP through IOC, and IOC_IOMUX_SEL (for example, GPIO0_IOC_GPIO0A_IOMUX_SEL_0) controls which IP the signal is input to.

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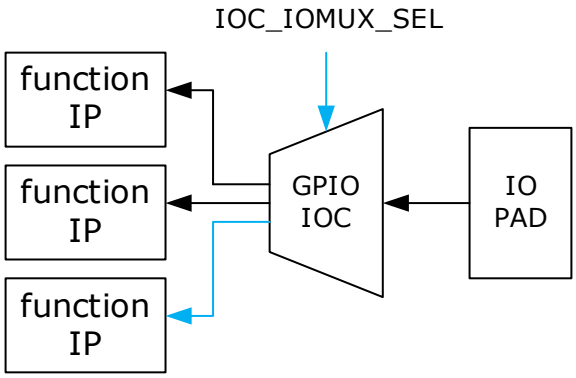

Fig. 18-1 Connect directly from IOC to function IP

2) As shown in following figure, some IP will be connected to the IO PAD via RMIO and IOC. In this case, you need to configure IOC_IOMUX_SEL to select RMIO (for example, GPIO0_IOC_GPIO0A_IOMUX_SEL_0=4 'h7) and then configure RMIO FUNC_SEL so that one of the IP in the orange box is selected to complete stroking with the IO PAD.

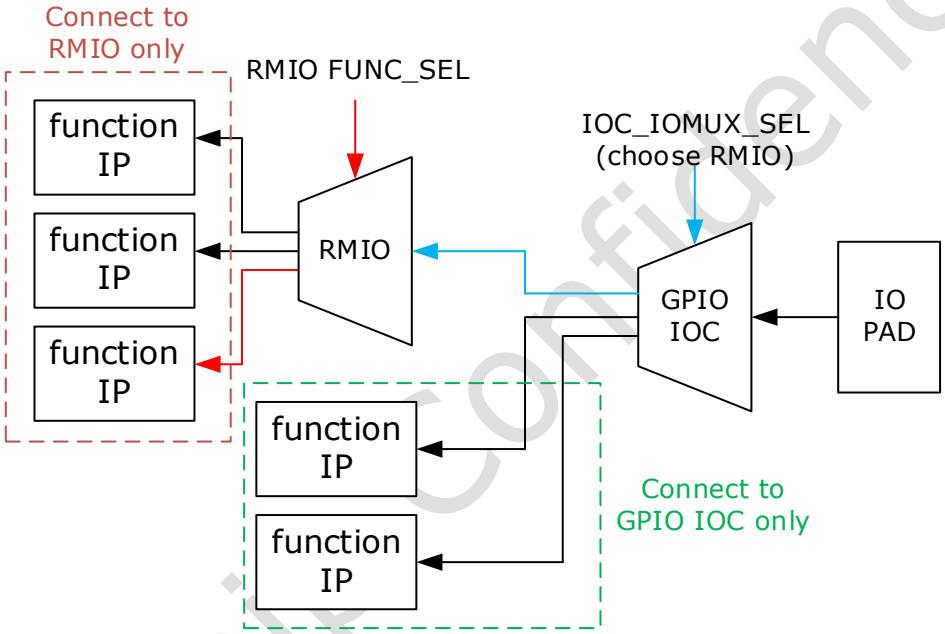

Fig. 18-2 Some IPs are connected to the IO PAD through RMIO and IOC

3) As shown in following figure, the IP can be connected to the IO PAD only through IOC, or through RMIO+IOC. In this case, you need to configure RMIO_FUNC_SEL, and IOC_IOMUX_SEL to select one of the paths. The IOC will have a higher priority.

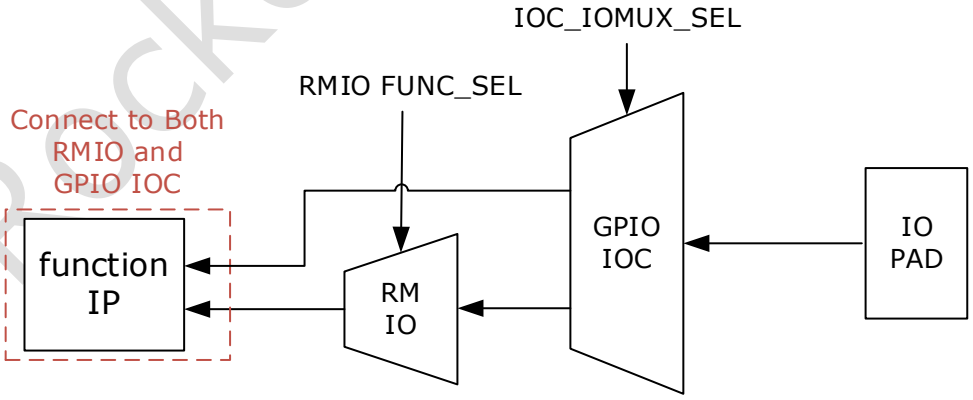

Fig. 18-3 IP which has multiple paths connecting to the I/O PAD

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Chapter 19 Rockchip Matrix IO

19.1 Overview

The Rockchip Matrix IO (RM_IO) can be configured with registers to route arbitrary signals from low-speed IP, such as UART/I2C, to the selected IO PAD.
RM_IO has the following features:

- Supports routing any IP signal in the optional range to the IO PAD
- The IP signal that is not routed to the IO PAD is tied to the default value

19.2 Block Diagram

RM_IO is comprised of:

- Config Interface

This interface controls which IP pins Rockchip Matrix IO routes to RM_IOx.

- IP Interface

IP interfaces connect signals from peripheral IP, including input/output/output enablement.

- RM_IO0~RM_IOx

These signals are connected to IOMUX. When IOMUX's SEL signal is configured to a specific value, RM_IOx connects to the IO PAD. That is, RM_IO0 is connected to PAD0 through IOMUX, and RM_IO1 is connected to PAD1 through IOMUX.

- Test Interface

This interface controls the behavior in test mode.

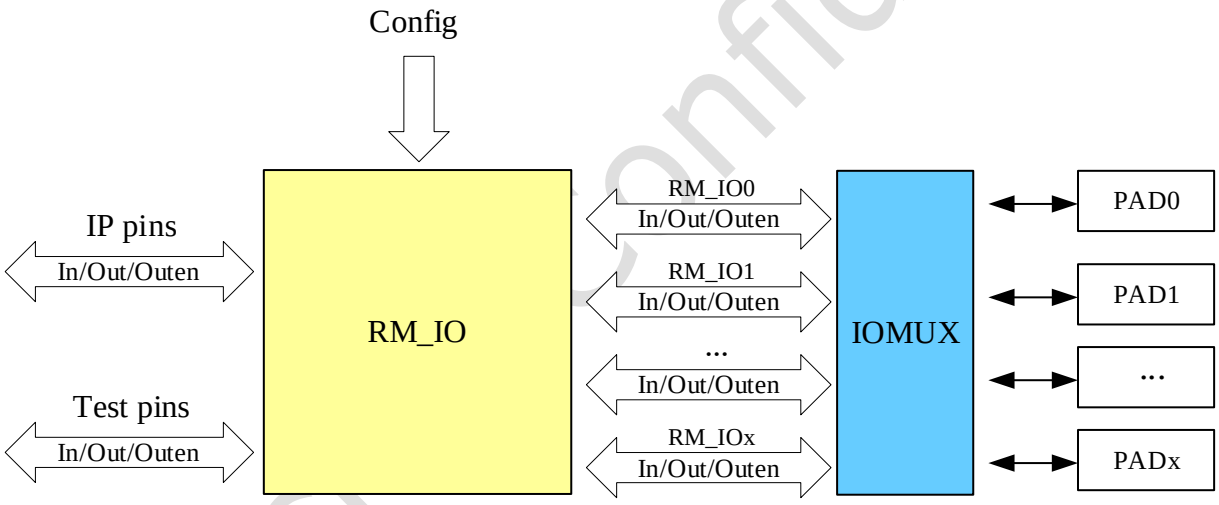

Fig. 19-1 RM_IO Block Diagram

19.3 Function Description

19.3.1 IP signal routing

The number of peripheral IP signals connected to RM_IO is greater than the number of pads. RM_IO can be configured by software to connect an IP signal to any PAD. The following is an example:

1) Write a value to RM_IO_rm_gpio0a0_sel by referring to the RM_IO register description in section 19.4 to configure the IP function pin of the RM_IO0 connection. The selected function pins can be viewed in 19.4.2 Detail Registers Description.
2) View the PAD name that RM_IO0 connects to by referring to Table 19-1. Set the value in IOMUX Setting to enable RM_IO0 to connect to the PAD through IOMUX.
3) You can perform steps 1 and 2 to configure any RM_IOx. Note that the function selection of multiple RM_IO cannot be the same; otherwise, conflicts will occur, causing the IP function pins to fail to connect to the PAD.

19.3.2 Test Mode

RM_IO can switch to the test mode through the register, which is used to find connection problems faster; after entering the Test mode, the value of the IP pins in Fig. 19-1 does not affect the input and output of RM_IO. Instead, the Test pins connect to the PAD through RM_IO. To use it, follow the following steps:

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1. Switch to test mode by setting GRF_PMU_SOC_CON1[11].
2. Repeat steps 1 and 2 in Section 1.3.1 to connect the Test pins to the PAD.
3. The value of Test pins (output/output enable driven to RM_IO) is controlled by registers PMUGRF_OS_REG0/1/2/3 (To control output0 ~97) and PMUGRF_OS_REG4/5/6/7(To control output enable0 ~ 97). The RM_IO_test_status register can be used to obtain the Test pins (the value driven to the Test pins by RM_IO) and the values of the RM_IO0~RM_IOx pins.

19.4 Register Description

19.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
RM_IO_rm_gpio0a0_sel	0x0080	W	0x00000000	Configure the rm_io0 function
RM_IO_rm_gpio0a1_sel	0x0084	W	0x00000000	Configure the rm_io1 function
RM_IO_rm_gpio0a2_sel	0x0088	W	0x00000000	Configure the rm_io2 function
RM_IO_rm_gpio0a3_sel	0x008C	W	0x00000000	Configure the rm_io3 function
RM_IO_rm_gpio0a4_sel	0x0090	W	0x00000000	Configure the rm_io4 function
RM_IO_rm_gpio0a5_sel	0x0094	W	0x00000000	Configure the rm_io5 function
RM_IO_rm_gpio0a6_sel	0x0098	W	0x00000000	Configure the rm_io6 function
RM_IO_rm_gpio0a7_sel	0x009C	W	0x00000000	Configure the rm_io7 function
RM_IO_rm_gpio0b0_sel	0x00A0	W	0x00000000	Configure the rm_io8 function
RM_IO_rm_gpio0b1_sel	0x00A4	W	0x00000000	Configure the rm_io9 function
RM_IO_rm_gpio0b2_sel	0x00A8	W	0x00000000	Configure the rm_io10 function
RM_IO_rm_gpio0b3_sel	0x00AC	W	0x00000000	Configure the rm_io11 function
RM_IO_rm_gpio0b4_sel	0x00B0	W	0x00000000	Configure the rm_io12 function
RM_IO_rm_gpio0b5_sel	0x00B4	W	0x00000000	Configure the rm_io13 function
RM_IO_rm_gpio0b6_sel	0x00B8	W	0x00000000	Configure the rm_io14 function
RM_IO_rm_gpio0b7_sel	0x00BC	W	0x00000000	Configure the rm_io15 function
RM_IO_rm_gpio0c0_sel	0x00C0	W	0x00000000	Configure the rm_io16 function
RM_IO_rm_gpio0c1_sel	0x00C4	W	0x00000000	Configure the rm_io17 function
RM_IO_rm_gpio0c2_sel	0x00C8	W	0x00000000	Configure the rm_io18 function
RM_IO_rm_gpio0c3_sel	0x00CC	W	0x00000000	Configure the rm_io19 function
RM_IO_rm_gpio0c4_sel	0x00D0	W	0x00000000	Configure the rm_io20 function
RM_IO_rm_gpio0c5_sel	0x00D4	W	0x00000000	Configure the rm_io21 function
RM_IO_rm_gpio0c6_sel	0x00D8	W	0x00000000	Configure the rm_io22 function
RM_IO_rm_gpio0c7_sel	0x00DC	W	0x00000000	Configure the rm_io23 function
RM_IO_rm_gpio1b1_sel	0x00E0	W	0x00000000	Configure the rm_io24 function
RM_IO_rm_gpio1b2_sel	0x00E4	W	0x00000000	Configure the rm_io25 function
RM_IO_rm_gpio1b3_sel	0x00E8	W	0x00000000	Configure the rm_io26 function
RM_IO_rm_gpio1c2_sel	0x00EC	W	0x00000000	Configure the rm_io27 function
RM_IO_rm_gpio1c3_sel	0x00F0	W	0x00000000	Configure the rm_io28 function
RM_IO_rm_gpio1d1_sel	0x00F4	W	0x00000000	Configure the rm_io29 function
RM_IO_rm_gpio1d2_sel	0x00F8	W	0x00000000	Configure the rm_io30 function
RM_IO_rm_gpio1d3_sel	0x00FC	W	0x00000000	Configure the rm_io31 function
RM_IO_test_status0	0x0300	W	0x00000000	Status of RM_IO output in test mode
RM_IO_test_status1	0x0304	W	0x00000000	Status of RM_IO output in test mode
RM_IO_test_status2	0x0308	W	0x00000000	Status of RM_IO output in test mode
RM_IO_test_status3	0x030C	W	0x00000000	Status of RM_IO output in test mode
RM_IO_test_status4	0x0310	W	0x00000000	Status of output from PAD to RM_IO in test mode

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

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Double WORD (64 bits) access

19.4.2 Detail Registers Description

RM_IO_rm_gpio0a0_sel

Address: Operational Base(0xFF910000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

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6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

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Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0a1_sel

Address: Operational Base(0xFF910000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

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6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

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Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0a2_sel

Address: Operational Base(0xFF910000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

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6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

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Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0a3_sel

Address: Operational Base(0xFF910000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

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6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0a4_sel

Address: Operational Base(0xFF910000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0a5_sel

Address: Operational Base(0xFF910000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0a6_sel

Address: Operational Base(0xFF910000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0a7_sel

Address: Operational Base(0xFF910000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0b0_sel

Address: Operational Base(0xFF910000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0b1_sel

Address: Operational Base(0xFF910000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0b2_sel

Address: Operational Base(0xFF910000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0b3_sel

Address: Operational Base(0xFF910000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0b4_sel

Address: Operational Base(0xFF910000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0b5_sel

Address: Operational Base(0xFF910000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0b6_sel

Address: Operational Base(0xFF910000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0b7_sel

Address: Operational Base(0xFF910000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0c0_sel

Address: Operational Base(0xFF910000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0c1_sel

Address: Operational Base(0xFF910000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0c2_sel

Address: Operational Base(0xFF910000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0c3_sel

Address: Operational Base(0xFF910000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0c4_sel

Address: Operational Base(0xFF910000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0c5_sel

Address: Operational Base(0xFF910000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0c6_sel

Address: Operational Base(0xFF910000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio0c7_sel

Address: Operational Base(0xFF910000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio1b1_sel

Address: Operational Base(0xFF910000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio1b2_sel

Address: Operational Base(0xFF910000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio1b3_sel

Address: Operational Base(0xFF910000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio1c2_sel

Address: Operational Base(0xFF910000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio1c3_sel

Address: Operational Base(0xFF910000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio1d1_sel

Address: Operational Base(0xFF910000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio1d2_sel

Address: Operational Base(0xFF910000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_rm_gpio1d3_sel

Address: Operational Base(0xFF910000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Rockchip Confidencial

6:0	RW	0x00	func_sel Select different function pins 7'h0: No pins are selected 7'h1: UART1_TX 7'h2: UART1_RX 7'h3: UART2_TX 7'h4: UART2_RX 7'h5: UART3_TX 7'h6: UART3_RX 7'h7: UART3_CTSN 7'h8: UART3_RTSN 7'h9: UART4_TX 7'hA: UART4_RX 7'hB: UART4_CTSN 7'hC: UART4_RTSN 7'hD: MIPI_DPHY_DSI_TX_TE 7'hE: CLK_32K 7'hF: I2C0_SCL 7'h10: I2C0_SDA 7'h11: I2C1_SCL 7'h12: I2C1_SDA 7'h13: I2C2_SCL 7'h14: I2C2_SDA 7'h15: PDM_CLK0 7'h16: PDM_SDI0 7'h17: PDM_SDI1 7'h18: PDM_SDI2 7'h19: PDM_SDI3 7'h1A: CAN1_TX 7'h1B: CAN1_RX 7'h1C: CAN0_TX 7'h1D: CAN0_RX 7'h1E: PWM0_CH0 7'h1F: PWM0_CH1 7'h20: PWM0_CH2 7'h21: PWM0_CH3 7'h22: PWM1_CH0 7'h23: PWM1_CH1 7'h24: PWM1_CH2 7'h25: PWM1_CH3 7'h26: PWM1_CH4 7'h27: PWM1_CH5 7'h28: PWM1_CH6 7'h29: PWM1_CH7 7'h2A: TOUCH_KEY_DRIVE 7'h2B: TOUCH_KEY_IN0 7'h2C: TOUCH_KEY_IN1 7'h2D: TOUCH_KEY_IN2 7'h2E: TOUCH_KEY_IN3 7'h2F: TOUCH_KEY_IN4 7'h30: TOUCH_KEY_IN5 7'h31: TOUCH_KEY_IN6 7'h32: TOUCH_KEY_IN7 7'h33: SAI0_MCLK 7'h34: SAI0_SCLK 7'h35: SAI0_LRCK 7'h36: SAI0_SDI0

Rockchip Confidencial

Bit	Attr	Reset Value	Description
			7'h37: SAI0_SDI1 7'h38: SAI0_SDI2 7'h39: SAI0_SDI3 7'h3A: SAI0_SDO 7'h3B: SAI1_MCLK 7'h3C: SAI1_SCLK 7'h3D: SAI1_LRCK 7'h3E: SAI1_SDI 7'h3F: SAI1_SDO0 7'h40: SAI1_SDO1 7'h41: SAI1_SDO2 7'h42: SAI1_SDO3 7'h43: SPI0_CLK 7'h44: SPI0_MOSI 7'h45: SPI0_MISO 7'h46: SPI0_CSN0 7'h47: SPI0_CSN1 7'h48: SPI1_CLK 7'h49: SPI1_MOSI 7'h4A: SPI1_MISO 7'h4B: SPI1_CSN0 7'h4C: SPI1_CSN1 7'h4D: TSADC_CTRL 7'h4E: PMU_SLEEP 7'h4F: CORE_POWER_OFF 7'h50: SPDIF_TX 7'h51: SPDIF_RX 7'h52: PWM1_BIP_CNTR_A0 7'h53: PWM1_BIP_CNTR_A1 7'h54: PWM1_BIP_CNTR_A2 7'h55: PWM1_BIP_CNTR_A3 7'h56: PWM1_BIP_CNTR_A4 7'h57: PWM1_BIP_CNTR_A5 7'h58: PWM1_BIP_CNTR_B0 7'h59: PWM1_BIP_CNTR_B1 7'h5A: PWM1_BIP_CNTR_B2 7'h5B: PWM1_BIP_CNTR_B3 7'h5C: PWM1_BIP_CNTR_B4 7'h5D: PWM1_BIP_CNTR_B5 7'h5E: PDM_CLK1 7'h5F: ETH_RMII0_PPSCLK 7'h60: ETH_RMII0_PPSTRIG 7'h61: ETH_RMII1_PPSCLK 7'h62: ETH_RMII1_PPSTRIG

RM_IO_test_status0

Address: Operational Base(0xFF910000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sig_to_ip Signal status 0~31 to IP.

RM_IO_test_status1

Address: Operational Base(0xFF910000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sig_to_ip Signal status 32~63 to IP.

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RM_IO_test_status2

Address: Operational Base(0xFF910000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sig_to_ip Signal status 64~95 to IP.

RM_IO_test_status3

Address: Operational Base(0xFF910000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	sig_to_ip Signal status 96~97 to IP.

RM_IO_test_status4

Address: Operational Base(0xFF910000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sig_from_pad Signal status from PAD.

19.5 Interface Description

RM_IO0~31 connects to different I/O pads. For details, see Table 19-1.

Table 19-1 RM_IO Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
RM0_IO Interface			
RM_IO0	I/O	GPIO0_A0	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[3:0]=4'h7
RM_IO1	I/O	GPIO0_A1	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[7:4]=4'h7
RM_IO2	I/O	GPIO0_A2	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[11:8]=4'h7
RM_IO3	I/O	GPIO0_A3	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[15:12]=4'h7
RM_IO4	I/O	GPIO0_A4	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[3:0]=4'h7
RM_IO5	I/O	GPIO0_A5	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[7:4]=4'h7
RM_IO6	I/O	GPIO0_A6	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[11:8]=4'h7
RM_IO7	I/O	GPIO0_A7	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[15:12]=4'h7
RM_IO8	I/O	GPIO0_B0	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[3:0]=4'h7
RM_IO9	I/O	GPIO0_B1	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[7:4]=4'h7
RM_IO10	I/O	GPIO0_B2	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[11:8]=4'h7
RM_IO11	I/O	GPIO0_B3	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[15:12]=4'h7
RM_IO12	I/O	GPIO0_B4	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[3:0]=4'h7
RM_IO13	I/O	GPIO0_B5	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[7:4]=4'h7
RM_IO1	I/O	GPIO0_B6	GPIO0_IOC_GPIO0B_IOMUX_SE

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Module Pin	Dir	Pad Name	IOMUX Setting
4			L_1[11:8]=4'h7
RM_IO15	I/O	GPIO0_B7	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[15:12]=4'h7
RM_IO16	I/O	GPIO0_C0	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[3:0]=4'h7
RM_IO17	I/O	GPIO0_C1	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[7:4]=4'h7
RM_IO18	I/O	GPIO0_C2	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[11:8]=4'h7
RM_IO19	I/O	GPIO0_C3	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[15:12]=4'h7
RM_IO20	I/O	GPIO0_C4	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[3:0]=4'h7
RM_IO21	I/O	GPIO0_C5	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[7:4]=4'h7
RM_IO22	I/O	GPIO0_C6	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[11:8]=4'h7
RM_IO23	I/O	GPIO0_C7	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[15:12]=4'h7
RM_IO24	I/O	GPIO1_B1	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[7:4]=4'h7
RM_IO25	I/O	GPIO1_B2	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[11:8]=4'h7
RM_IO26	I/O	GPIO1_B3	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[15:12]=4'h7
RM_IO27	I/O	GPIO1_C2	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[11:8]=4'h7
RM_IO28	I/O	GPIO1_C3	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[15:12]=4'h7
RM_IO29	I/O	GPIO1_D1	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[7:4]=4'h7
RM_IO30	I/O	GPIO1_D2	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[11:8]=4'h7
RM_IO31	I/O	GPIO1_D3	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[15:12]=4'h7

Notes: I=input, O=output, I/O=input/output

19.6 Application Notes

- If multiple RM_IO configurations are configured for the same function (for example, RM_GPIO0A0_SEL == RM_GPIO0A1_SEL), a conflict will occur. The input and output of both RM_IO are fixed to their default values.

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Chapter 20 Audio Subsystem

20.1 Overview

The audio subsystem is dedicated for managing the audio resources of the whole chip. In RK3506, the audio subsystem consists of three pieces: BUS_WRAPPER, LS_PERI wrapper and HS_PERI wrapper. With the audio subsystem, we can combine audio components and the embedded SOC platform together and provide an audio system solution.

20.2 Block Diagram

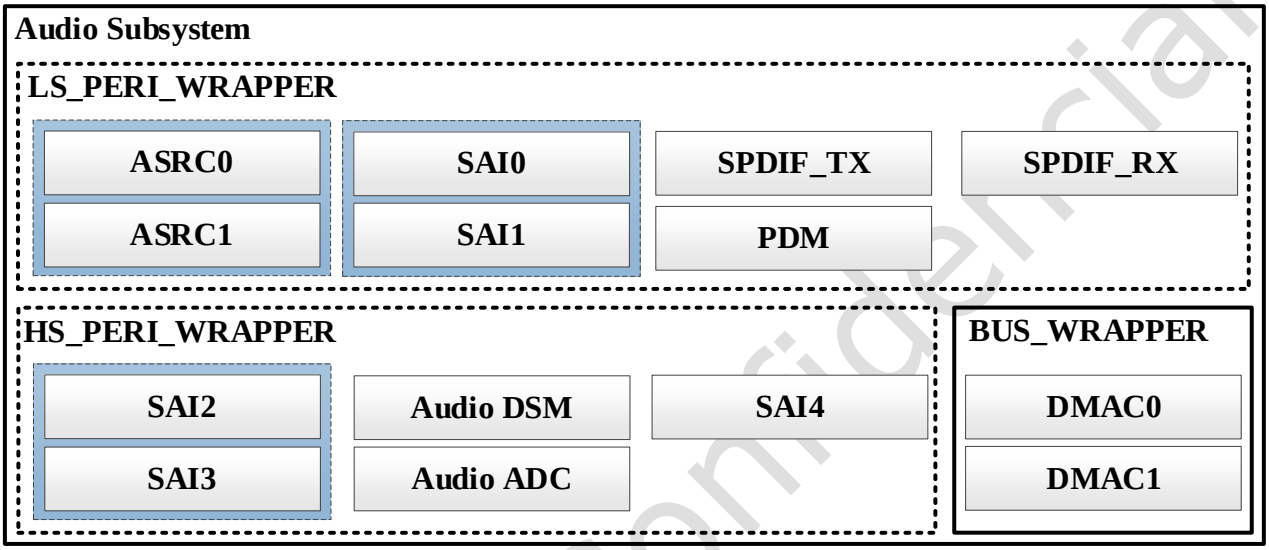

Fig. 20-1 Audio Subsystem Block Diagram

LS_PERI Wrapper

LS_PERI Wrapper consists of audio components shown as follow:

- One PDM
- One SPDIF_TX
- One SPDIF_RX
- SAI0 (1 tx, 4 rx lanes) and SAI1 (4 tx, 1 rx lanes), which can be combined together
- Two 4 channel ASRC0/1, which can be combined together. Audio components in the HS_PERI wrapper can also converted using ASRC0/1, not just the audio components in LS_PERI wrapper.

HS_PERI Wrapper

HS_PERI Wrapper consists of audio components shown as follow:

- One Audio ADC
- One Audio DSM, which can be used to play audio data from SAI3
- SAI2/3 (1 lane), which can be combined together
- SAI4 (1 rx lane), which can be used to receive data from Audio ADC

BUS Wrapper

BUS Wrapper consists of two multichannel DMA called DMAC0 and DMAC1, which can be used to transmit audio data.

20.3 Function Description

In this chapter, we will only cover the interconnection of these audio components. For the detail of audio components, please refer to the following chapters: Audio DSM, Audio ADC, SPDIF Transmitter, SPDIF Receiver, PDM, Serial Audio Interface (SAI) and Asynchronous Sample Rate Converter (ASRC).

20.3.1 SAI Series Mode

In series mode, SAIs in LS_PERI wrapper or HS_PERI wrapper can be combined together to

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enhance throughput. We can appoint the SAI at the front as master and other SAIs as slave. In RK3506, SAI0 as master and SAI1 as slave when combined, SAI2 as master and SAI3 as slave when combined.
In series mode, the following internal signals interact to ensure that the combined SAIs stay synchronized. Meanwhile, the FS interface and SCLK interface of slave SAI are derived from master SAI instead. Besides, all combined SAIs can be viewed as a whole and interact with the outside world using their respective interface. We can take LS_PERI wrapper series mode as an example in the following figure.

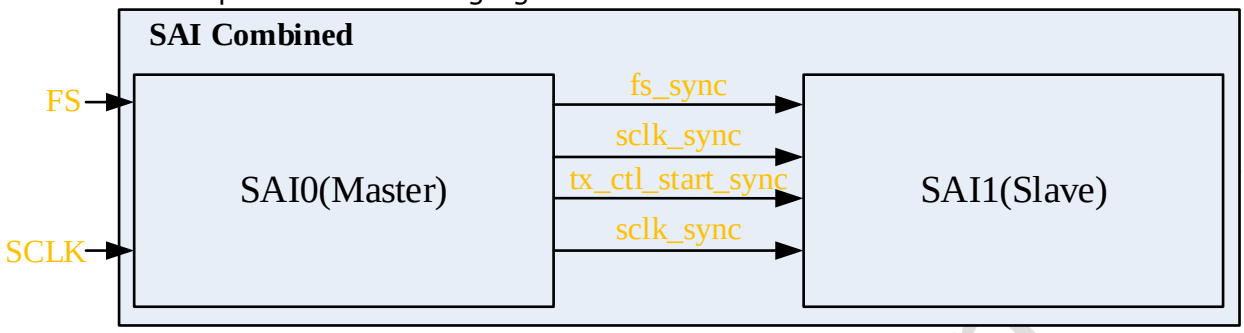

Fig. 20-2 SAI Series Mode Structure

20.3.2 ASRC Series Mode

In series mode, adjacent ASRCs in LS_PERI wrapper can be combined together to enhance throughput. We can appoint the ASRC at the front as master and other ASRCs as slave. In RK3506, ASRC0 as master and ASRC1 as slave when combined.
In series mode, all combined ASRCs can be viewed as a whole and interact with the outside world using the interface of master ASRC only. We can take MEM2MEM series mode in audio0 wrapper as an example in the following figure.

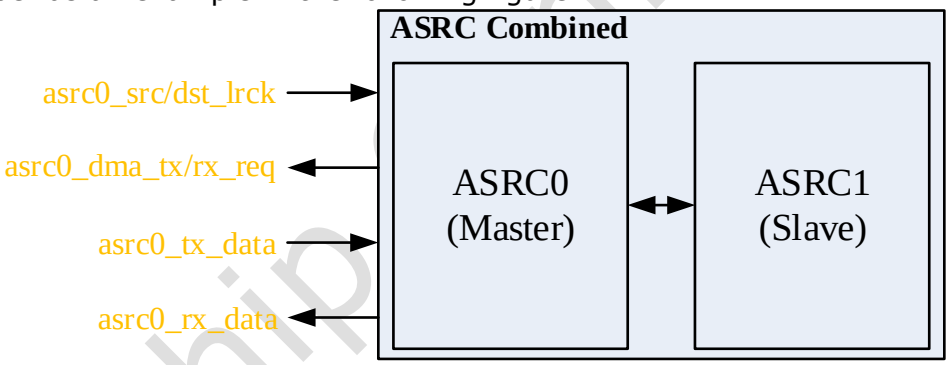

Fig. 20-3 ASRC MEM2MEM Series Mode Structure

In series mode of SAI and ASRC, only the clock source of master is used. Combined SAIs using their own DMA handshake interface and interrupt interface, but only the interface of master ASRC is used when combined.

20.3.3 SPDIF Mux

Usually, the output of SPDIF_TX is sent to IO. But for debug purpose, we can send the input of SPDIF_RX to IO instead using the following selector.

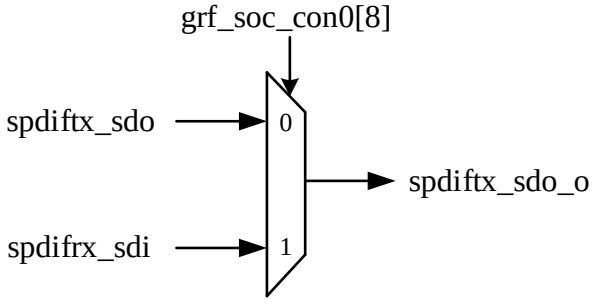

Fig. 20-4 SPDIF SDO Selector

20.3.4 Audio DSM and SAI3

Audio DSM can be used to play audio data from SAI3. Three possible application can be shown as follow.

- Audio DSM acts as slave and SAI3 as master

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Clock source of audio DSM is from SAI3, and clock source of SAI3 is from CRU.

- Audio DSM acts as master and SAI3 as slave
  Clock source of audio DSM is from CRU, and clock source of SAI3 is from audio DSM.
- Both audio DSM and SAI3 acts as slave
  Clock source of audio DSM and SAI3 is from IO.

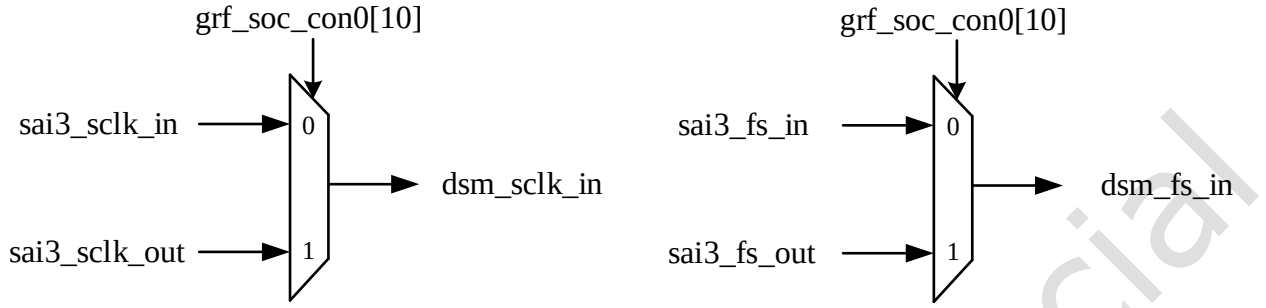

Fig. 20-5 Audio DSM Input Clock Selector

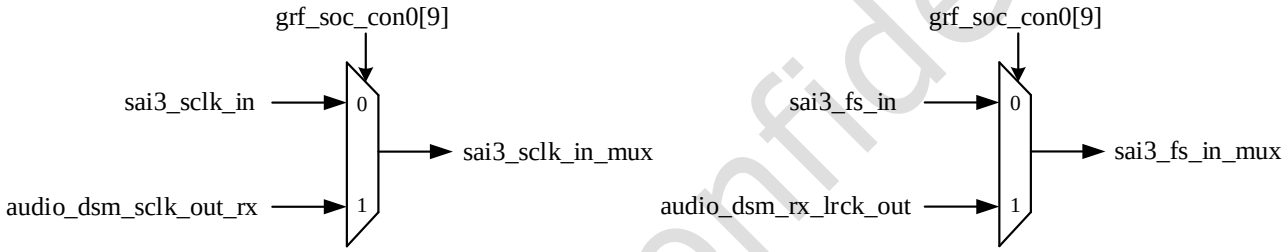

Fig. 20-6 SAI Input Clock Selector

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Chapter 21 Audio DSM

21.1 Overview

Audio DSM is a 16-bit digital audio encoder which supports multiple sample rates. It is mainly composed of digital DAC. The aim of digital DAC is to process the data received from I2S/PCM interface through filters, volume control and modulation.
The RK DSM supports the following features.

- Support 8-bit APB and AHB bus slave interface
- Support 2-channel digital DAC
- Support I2S/PCM interface
- Support I2S/PCM master and slave mode
- Support 2-channel audio receiving in I2S mode
- Support 2-channel audio receiving in PCM mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and LRCK polarity
- Support 16 bit sample resolution
- Support programmable left and right channel exchangeable in I2S mode and PCM mode
- Support three modes of mixing for every digital DAC channel
- Support volume control
- Support programmable negative and positive volume gain

21.2 Block Diagram

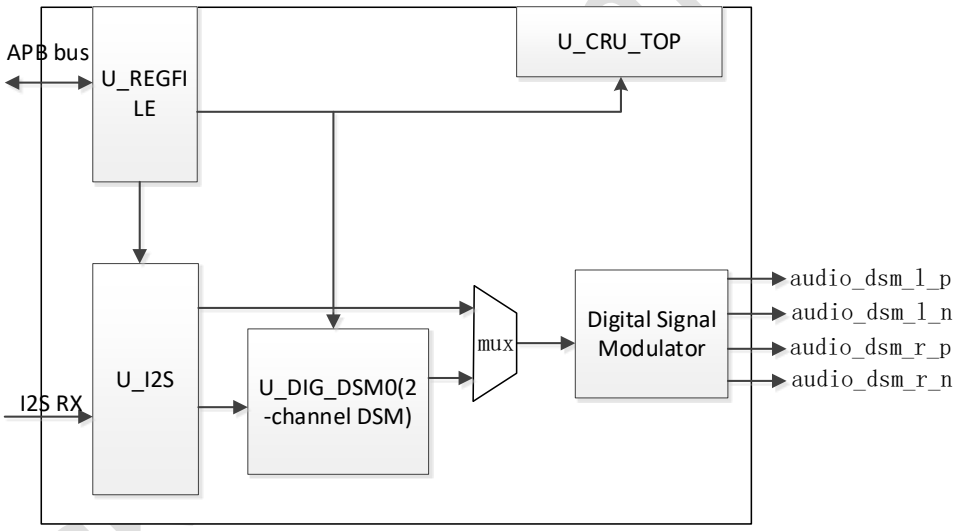

Fig.21-1 RK DSM Block Diagram

RK DSM_RF
The RK DSM_RF implements the 8-bit APB/AHB slave operation through APB/AHB bus. It is responsible for configuring the operation registers of other modules.
RK DSM_CRU
The RK DSM_CRU implements clock and reset generation function. It is responsible for generating sample clock, digital DAC operation clock and I2S operation clock.
RK DSM
There are 2 digital DAC channels. The digital DAC receives audio data from ACDC_I2S module. It includes one CIC filter, one high-pass filter, several low-pass decimation filters and other audio signal processing related modules. The output of digital DAC is sent to DSM modular before transmitting outside.
RK DSM_I2S
The I2S/PCM audio interface can be configured to master mode or slave mode. In Master Mode, SCLK and LRCK are configured as output. In slave mode, SCLK and LRCK are

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configured as input. The RK DSM_I2S module can only operate in RX mode. When in RX mode, it receives audio data from I2S RX interface and sends it to digital DAC.

DSM Modulator

It is a modulator that converts 16 bits audio sample data to 1 bit audio data.

21.3 Function description

The I2S/PCM interface of Digital Audio Codec is connected to the I2S1 controller. Please refer to the I2S chapter for detailed information about I2S and PCM format that Digital Audio Codec supports.

21.3.1 Filters of Digital DAC

I2S module receives two-channel audio data from I2S RX interface and drives it to the digital DAC which supports mixing function or directly to the DSM modulator. How to pour 2-channel audio data into 2-channel digital DAC can be achieved by programming mixing mode.

The 2-channel digital DAC includes a high-pass filter and a maximum of 5 half-band filters. The high-pass filter is used to filter DC components in audio data stream. Result of high-pass filter is sent to the digital DAC volume control module. The input of 5 half-band filters comes from output of volume control module with each perform 2-times interpolation. But not all of them are working all the time. How many of them are needed to work depends on the sample rate of digital DAC. The result of half-band filters is sent to a modulator.

21.3.2 Volume Control

For digital DAC, output of high-pass filters is fed into volume control module. The volume control module inside digital DAC contains several sub-modules such as peak detect, frequency cross zero detect, LIMITER and digital gain control. It can be digitally attenuated over a range of -96dB~0dB in 0.375dB/step for negative gain and amplified over a range of 0dB~96dB in 0.375dB/step for positive gain. Whether is attenuated or amplified can be software programmed.

21.4 Register Description

21.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

21.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKDSM_DSMVUCTL	0x0000	W	0x00000001	DAC Volume Control Register
RKDSM_DSMVUCTIME	0x0004	W	0x00000000	DAC Volume Control Time Limit Register
RKDSM_DSMDIGEN	0x0008	W	0x00000000	DAC Digital Enable Register
RKDSM_DSMCLKCTRL	0x000C	W	0x00000000	DAC Clock Control Register
RKDSM_DSMINTMOD_DIV	0x0014	W	0x00000007	DAC Integer Clock Divider Register
RKDSM_DSMINTSCLK_DIV	0x0020	W	0x0000001F	I2S SCLK RX Integer Divider Register
RKDSM_DSM_DIV	0x0024	W	0x00000003	DSM Mode Integer Divider Register
RKDSM_DSM_CTRL	0x0028	W	0x00000000	DSM Mode Control Register
RKDSM_DSMCFG1	0x0044	W	0x00000004	DAC Configure Register 1
RKDSM_DSMMUTE	0x0048	W	0x00000000	DAC Mute Control Register
RKDSM_DSMMUTEST	0x004C	W	0x00000000	DAC Mute Status Register
RKDSM_DSMVOLL0	0x0050	W	0x00000000	Volume of DAC Left Channel 0 Register
RKDSM_DSMVOLL1	0x0054	W	0x00000000	Volume of DAC Left Channel 0 Register

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Name	Offset	Size	Reset Value	Description
RKDSM_DSMVOLL2	0x0058	W	0x00000000	Volume of DAC Left Channel 0 Register
RKDSM_DSMVOLL3	0x005C	W	0x00000000	Volume of DAC Left Channel 0 Register
RKDSM_DSMVOLR0	0x0060	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOLR1	0x0064	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOLR2	0x0068	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOLR3	0x006C	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOGP	0x0070	W	0x00000000	DAC Volume Gain Polarity Register
RKDSM_DSMRVOLL0	0x0074	W	0x000000FF	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLL1	0x0078	W	0x00000000	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLL2	0x007C	W	0x00000000	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLL3	0x0080	W	0x00000000	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLR0	0x0084	W	0x000000FF	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMRVOLR1	0x0088	W	0x00000000	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMRVOLR2	0x008C	W	0x00000000	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMRVOLR3	0x0090	W	0x00000000	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMLMT0	0x0094	W	0x00000000	DAC Limiter Register 0
RKDSM_DSMLMT1	0x0098	W	0x00000000	DAC Limiter Register 1
RKDSM_DSMLMT2	0x009C	W	0x00000000	DAC Limiter Register 2
RKDSM_DSMMIXCTRLL	0x00A0	W	0x00000000	DAC Mixing Control Register Of Left Channels
RKDSM_DSMMIXCTRLR	0x00A4	W	0x00000000	DAC Mixing Control Register Of right Channels
RKDSM_DSMHPF	0x00A8	W	0x00000000	DAC High-pass Filter Control Register
RKDSM_DSM_I2S_RXCR0	0x010C	W	0x0000000F	Receive Operation Control Register 0
RKDSM_DSM_I2S_RXCR1	0x0110	W	0x00000000	Receive Operation Control Register 1
RKDSM_DSM_I2S_CKR0	0x0114	W	0x00000000	Clock Generation Register 0
RKDSM_DSM_I2S_CKR1	0x0118	W	0x00000000	Clock Generation Register 1
RKDSM_DSM_I2S_XFER	0x011C	W	0x00000000	Transfer Start Register
RKDSM_DSM_I2S_CLR	0x0120	W	0x00000000	SCLK Domain Logic Clear Register
RKDSM_DSM_VERSION	0x0140	W	0x00000010	Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

21.4.3 Detail Registers Description

RKDSM_DSMVUCTL

Address: Operational Base(0xFF4B0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	dac_byps Digital DAC volume control bypass. 1'b0: Digital DAC volume control enable 1'b1: Digital DAC volume control bypass
1	RW	0x0	dacfade Digital DAC volume adjust mode. 1'b0: Update to new volume immediately. 1'b1: Update volume as daczdt field describes.
0	RW	0x1	daczdt Digital DAC volume cross zero detect enable. It works when dac_byps is 1'b0 and dacfade is 1'b1. 1'b0: Volume adjusts every sample. 1'b1: Volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets.

RKDSM_DSMVUCTIME

Address: Operational Base(0xFF4B0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacvuct Volume control time limit, valid only in fade cross zero mode. Time limit = dacvuct*(1/sample rate) Unit: Sample rate

RKDSM_DSMDIGEN

Address: Operational Base(0xFF4B0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	dacglben Global enable of all Digital DAC channels. Only when dacglben and the enable signal corresponding to each Digital DAC channel is valid before starting work. 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	dacen_l0r1 Digital DAC left channel 0 and right channel 1 enable. 1'b0: Disable 1'b1: Enable

RKDSM_DSMCLKCTRL

Address: Operational Base(0xFF4B0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	dac_cke Digital DAC operation clock enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	i2srx_cke Clock enable of internal I2S RX channel. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	cke_bclkrx Clock enable of sclk_out_rx. 1'b0: Disable 1'b1: Enable
2	RW	0x0	dac_sync_ena Enable of the synchronization signal used internally generated by Digital DAC. 1'b0: Disable 1'b1: Enable
1	RO	0x0	dac_sync_status There is a counter to generate synchronization signal of Digital DAC. In order to ensure the integrity of synchronization signal, it is necessary to read back dac_sync_status to judge whether the counter stops working when dac_sync_ena is set from 1'b1 to 1'b0. If the signal is read back to 1'b0, it means that the counter stops working and the synchronization signal of Digital DAC is complete.
0	RW	0x0	dac_mod_attenu_en When enabled, the input of the Digital DAC modulator is attenuated by 6dB, and the output of the Digital DAC modulator is increased by 6dB. 1'b0: Disable 1'b1: Enable

RKDSM_DSMINTMOD_DIV

Address: Operational Base(0xFF4B0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x07	int_div_con Integer clock divider to provide 6.144/5.644/4.096MHz sample clock for internal filters. Make sure that int_div_con is an odd number between 7(8 times division) and 15(16 times division).

RKDSM_DSMINTSCLK_DIV

Address: Operational Base(0xFF4B0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	sckrxdiv Integer clock divider to generate sclk_out_rx when I2S RX works in master mode. It is ignored when in slave mode. Sckrxdiv=((frequency of input operation clock)/(frequency of sclk_out_rx))-1. Sckrxdiv can be any value from 0 to 255.

RKDSM_DSM_DIV

Address: Operational Base(0xFF4B0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	audio_dsm_div DSM mode division of Digital DAC's operation clock. The operation clock frequency of DSM module is equal to the input operation clock frequency of Digital DAC's divided by audio_dsm_div+1. It's recommended that audio_dsm_div is set 8'h3.

RKDSM_DSM_CTRL

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Address: Operational Base(0xFF4B0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	dsm_mode_cke Clock enable of 1-bit DSM modulator 1'b0: Disable 1'b1: Enable
5:4	RW	0x0	dsm_mode Audio DSM mode selection 2'b01: Audio DSM mode 0. The input of 1-bit DSM modulator is from the last filter of Audio DAC. 2'b10: Audio DSM mode 1. The input of 1-bit DSM modulator is directly from output of I2S RX inside the ACDCDIG. Others: Reserved
3	RW	0x0	dsm_en 1-bit DSM modulator enable 1'b0: Disable 1'b1: Enable
2:0	RW	0x0	dith_sel Dith mode selection of 1-bit DSM modulator.

RKDSM_DSMCFG1

Address: Operational Base(0xFF4B0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x1	dacsrt Sample rates of Digital DAC when in audio DSM mode 0. This field is ignored when in audio DSM mode 1. 3'b000: 12kHz/11.024kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 32kHz/48kHz/44.1kHz 3'b011: 96kHz/88.2kHz/64kHz 3'b100: 192kHz/176.4kHz/128kHz 3'b101~3'b111: Reserved
1:0	RO	0x0	reserved

RKDSM_DSMMUTE

Address: Operational Base(0xFF4B0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dacunmt 1'b0: DAC normal mode 1'b1: DAC unmute mode. In this mode, DAC volume control block will adjust volume to match the value in DACVOLL* and DACVOLR*.
0	RW	0x0	dacmt 1'b0: DAC normal mode 1'b1: DAC mute mode

RKDSM_DSMMUTEST

Address: Operational Base(0xFF4B0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4	RO	0x0	unmutest_l0r1 Unmute status for Digital DAC left channel 0 and right channel 1. When unmute is done, it indicates that internal volume is equal to the value programmed in DACVOLL* and DACVOLR*. 1'b0: Unmute not done 1'b1: Unmute done
3:1	RO	0x0	reserved
0	RO	0x0	mutest_l0r1 Mute status for Digital DAC left channel 0 and right channel 1. 1'b0: Not mute 1'b1: Mute

RKDSM_DSMVOLL0

Address: Operational Base(0xFF4B0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv0 Volume of Digital DAC left channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL1

Address: Operational Base(0xFF4B0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv1 Volume of Digital DAC left channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL2

Address: Operational Base(0xFF4B0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	daclv2 Volume of Digital DAC left channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL3

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Address: Operational Base(0xFF4B0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	daclv3 Volume of Digital DAC left channel 3. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR0

Address: Operational Base(0xFF4B0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacrv0 Volume of Digital DAC right channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR1

Address: Operational Base(0xFF4B0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv1 Volume of Digital DAC right channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR2

Address: Operational Base(0xFF4B0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv2 Volume of Digital DAC right channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR3

Address: Operational Base(0xFF4B0000) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv3 Volume of Digital DAC right channel 3. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOGP

Address: Operational Base(0xFF4B0000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	volgpr1 Gain polarity for the volume of Digital DAC right channel 1. 1'b0: Negative gain 1'b1: Positive gain
0	RW	0x0	volgpl0 Gain polarity for the volume of Digital DAC left channel 0. 1'b0: Negative gain 1'b1: Positive gain

RKDSM_DSMRVOLL0

Address: Operational Base(0xFF4B0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvoll0 Internal real-time volume of Digital DAC left channel 0.

RKDSM_DSMRVOLL1

Address: Operational Base(0xFF4B0000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll1 Internal real-time volume of Digital DAC left channel 1.

RKDSM_DSMRVOLL2

Address: Operational Base(0xFF4B0000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll2 Internal real-time volume of Digital DAC left channel 2.

RKDSM_DSMRVOLL3

Address: Operational Base(0xFF4B0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll3 Internal real-time volume of Digital DAC left channel 3.

RKDSM_DSMRVOLR0

Address: Operational Base(0xFF4B0000) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvolr0 Internal real-time volume of Digital DAC right channel 0.

RKDSM_DSMRVOLR1

Address: Operational Base(0xFF4B0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr1 Internal real-time volume of Digital DAC right channel 1.

RKDSM_DSMRVOLR2

Address: Operational Base(0xFF4B0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr2 Internal real-time volume of Digital DAC right channel 2.

RKDSM_DSMRVOLR3

Address: Operational Base(0xFF4B0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr3 Internal real-time volume of Digital DAC right channel 3.

RKDSM_DSMLMT0

Address: Operational Base(0xFF4B0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	limen LIMITER enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	limdct Limiter detect mode. 1'b0: (Left channel + right channel)/2 1'b0: Left channel or right channel independently

RKDSM_DSMLMT1

Address: Operational Base(0xFF4B0000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	atk_rate LIMITER attack rate=(power(2, atk_rate)*(8*clk)), clk is such as 4.096Mhz, 5.6448Mhz, 6.144Mhz.
3:0	RW	0x0	rls_rate LIMITER release rate=(power(2, rls_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz.

RKDSM_DSMLMT2

Address: Operational Base(0xFF4B0000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	max_lilmt The highest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step
3	RO	0x0	reserved
2:0	RW	0x0	min_lilmt The lowest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step

RKDSM_DSMMIXCTRLL

Address: Operational Base(0xFF4B0000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_l0 Digital DAC left channel 0 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

RKDSM_DSMMIXCTRLR

Address: Operational Base(0xFF4B0000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_r0 Digital DAC right channel 1 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

RKDSM_DSMHPF

Address: Operational Base(0xFF4B0000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	hpfcf High-pass filter control. 2'b00: 80Hz 2'b01: 100Hz 2'b10: 120Hz 2'b11: 140Hz
3:1	RO	0x0	reserved
0	RW	0x0	hpfen_l0r1 High-pass filter enable for left channel 0 and right channel 1. 1'b0: High-pass filter is disabled. 1'b1: High-pass filter is enabled.

RKDSM_DSM_I2S_RXCR0

Address: Operational Base(0xFF4B0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	pbm PCM bus mode 2'b00: PCM no delay mode 2'b01: PCM delay 1 mode 2'b10: PCM delay 2 mode 2'b11: PCM delay 3 mode
5	RW	0x0	tfs Transfer format select 1'b0: I2S format 1'b1: PCM format
4:0	RW	0x0f	vdw Valid data width 5'b00000~5'b01110: Reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit ..... 5'b11100: 29bit 5'b11101: 30bit 5'b11110: 31bit 5'b11111: 32bit

RKDSM_DSM_I2S_RXCR1

Address: Operational Base(0xFF4B0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	rcsr Channel select 2'b00: Two channel Others: Reserved
5	RO	0x0	reserved
4	RW	0x0	cex Exchange left channel and right channel in the every receive line. 1'b0: Not exchange 1'b1: Exchange
3	RO	0x0	reserved
2	RW	0x0	fbm First bit mode 1'b0: MSB 1'b1: LSB
1:0	RW	0x0	ibm I2S bus mode 2'b00: I2S normal 2'b01: I2S Left justified 2'b10: I2S Right justified 2'b11: Reserved

RKDSM_DSM_I2S_CKR0

Address: Operational Base(0xFF4B0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	rsd I2S rx sclk divider for rx_lrck generator. 2'b00: 64 2'b01: 128 2'b10~2'b11: 256
1:0	RO	0x0	reserved

RKDSM_DSM_I2S_CKR1

Address: Operational Base(0xFF4B0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	mss Master/slave mode select 1'b0: Master mode(sclk output) 1'b1: Slave mode(sclk input)
2	RW	0x0	ckp Sclk polarity 1'b0: Sample data at posedge sclk and drive data at negedge sclk. 1'b1: Sample data at negedge sclk and drive data at posedge sclk.
1	RW	0x0	rlp 1'b0: Normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal: high valid) 1'b1: Opposite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal: low valid)
0	RO	0x0	reserved

RKDSM_DSM_I2S_XFER

Address: Operational Base(0xFF4B0000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
0	RO	0x0	reserved

RKDSM_DSM_I2S_CLR

Address: Operational Base(0xFF4B0000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxc This is a self-cleared bit. Write 1'b1 to clear all receive logic. This bit can be set only when rxs is 1'b0. After writing rxc to 1'b1, wait until rxc become 1'b0 by polling rxc.
0	RO	0x0	reserved

RKDSM_DSM_VERSION

Address: Operational Base(0xFF4B0000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x10	ver Version of DSM.

21.5 Interface Description

The I2S RX interface of Digital Audio Codec is connected to the TX interface of I2S1 when GRF_AUDIO_CON[14] is set to 1'b1.
When operating in audio DSM mode 0 or 1, Digital Audio Codec outputs two pairs of differential signals encoded in DSM format. The following table shows the RK DSM interface description for audio DSM mode.

Table 21-1 Audio DSM M0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
AUDIO_DSM_L_P	O	GPIO1_D1	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[7:4]=4
AUDIO_DSM_L_N	O	GPIO1_D0	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[3:0]=4
AUDIO_DSM_R_P	O	GPIO1_C2	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[11:8]=4
AUDIO_DSM_R_N	O	GPIO1_C1	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[7:4]=4

Table 21-2 Audio DSM M1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
AUDIO_DSM_L_P	O	GPIO2_B7	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[15:12]=2
AUDIO_DSM_L_N	O	GPIO2_B6	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[11:8]=2
AUDIO_DSM_R_P	O	GPIO2_B5	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[7:4]=2
AUDIO_DSM_R_N	O	GPIO2_B4	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[3:0]=2

21.6 Application Notes

21.6.1 Software Application Notes

Steps to configure Digital DAC to work in audio DSM mode 0 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program DSMINTMOD_DIV to 0x07.
3. Program DSMCLKCTRL to 0x3d.
4. Program DSMINTSCLK_DIV if Digital DAC I2S RX acts as master.
5. Program DSMDSM_CTRL to 0x58.
6. Program DSM_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S RX related registers.
7. Program DSM_I2S_CLR to clear RX logic.
8. Program DSM_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
9. Program GRF_AUDIO_CON[14] to 1'b1 and program registers of I2S1 that is connected to Digital Audio Codec. Don't start transfer at this time.
10. Program DAC related registers such as DSMHPF, DSMVUCTL and DSMCFG1 to achieve basic configuration.
11. Program ACDCDIG_I2S_XFER to start I2S RX.
12. Program registers of I2S1 outside Digital Audio Codec to start TX.
13. Program DSMDIGEN to enable digital DAC channels. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio DSM mode 0 transfer are as follows.
1. Program registers of I2S1 to stop TX and ACDCDIG_I2S_XFER to stop RX.
2. Program DSMDSM_CTRL to 0x0.
3. Program DSMDIGEN to disable digital DAC channels.
4. Program DSMCLKCTRL to 0x0. Wait DSMCLKCTRL.dac_sync_status until read back to be 1'b0.

Steps to configure Digital DAC to work in audio DSM mode 1 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.

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2. Program DSMCLKCTRL to 0x3d.
3. Program DSMSCLKRXINT_DIV if Digital DAC I2S RX acts as master.
4. Program DSMDSM_CTRL to 0x68.
5. Program DSM_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S RX related registers.
6. Program DSM_I2S_CLR to clear RX logic.
7. Program DSM_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
8. Program GRF_AUDIO_CON[14] to 1'b1 and program registers of I2S1 to start TX.
9. Program DSM_I2S_XFER to start I2S RX. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio DSM mode 1 transfer are as follows.

1. Program registers of I2S1 to stop TX and DSM_I2S_XFER to stop RX.
2. Program DSMDSM_CTRL to 0x0.
3. Program DSMCLKCTRL to 0x0. Wait DSMCLKCTRL.dac_sync_status until read back to be 1'b0.

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Chapter 22 Audio ADC

22.1 Overview

Audio ADC is a 24-bit digital audio decoder which supports multiple sample rates. The function of Audio ADC is to convert external MIC input analog signal to I2S/PCM format audio data through a series of filters and volume control. The coding process of Audio ADC is controlled by the register through the APB Bus.
Audio ADC supports the following features.

- Support APB bus slave interface
- Support Analog gain between 0~48dB with 3db/step
- Support 1-channel Differential-mode/Single-mode/Pseudo-differential mode ADC
- Support I2S/PCM master and slave mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support 16 ~32bit sample resolution
- Support sample rate: 8kHz, 16kHz, 32kHz, 64kHz, 128kHz, 11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz, 176.4kHz, 12kHz, 24kHz, 48kHz, 96kHz, 192kHz
- The passband of filters is 0.45625*fs
- Support passband ripple within +/-0.1dB
- The stopband of filters is 0.5*fs
- Support stopband attenuation at least 60dB
- Support Digital Audio ADC volume control
- Support programmable negative volume gain and positive volume gain.

22.2 Block Diagram

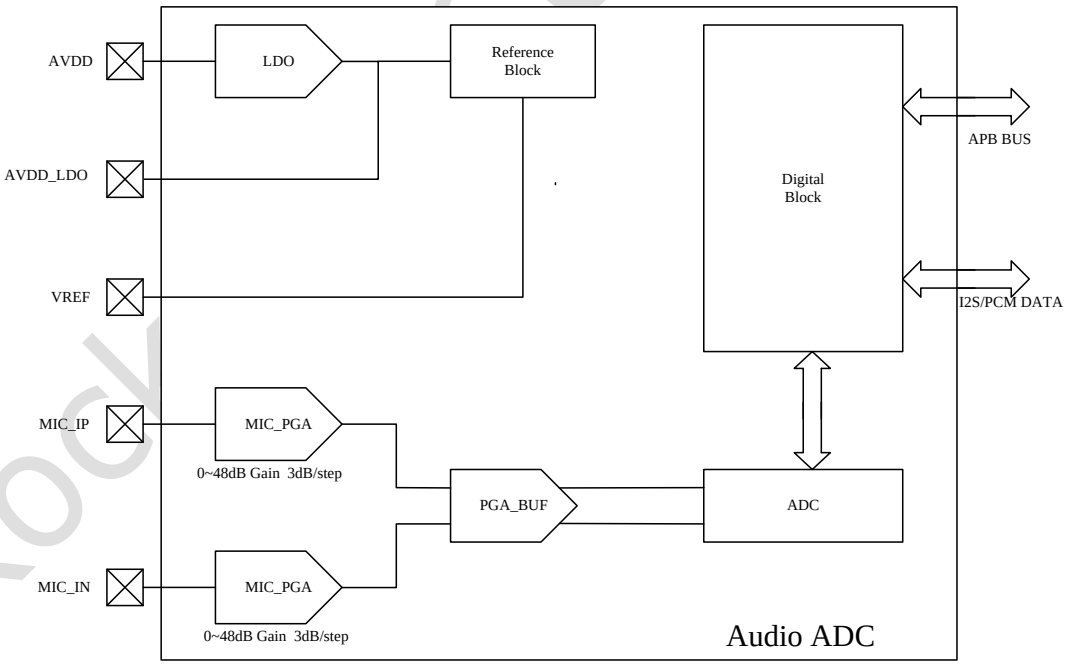

Fig. 22-1 Audio ADC Block Diagram

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22.3 Function Description

22.3.1 I2S normal mode

This is the waveform of I2S normal mode. For LRCK (i2s_lrck_tx) signal, it goes low to indicate left channel and high to right channel. For SD (i2s_sdo) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after LRCK changes. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

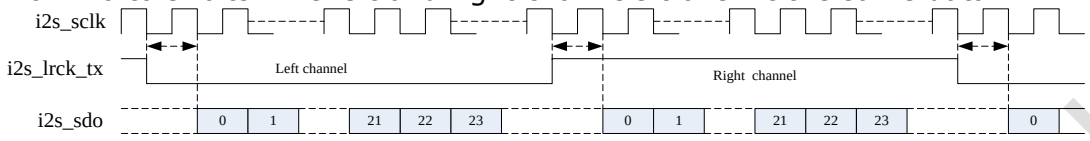

Fig.22-2 I2S Normal Mode Timing Format

22.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo) signal, it starts sending the first bit (MSB or LSB) at the same time when LRCK changes. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

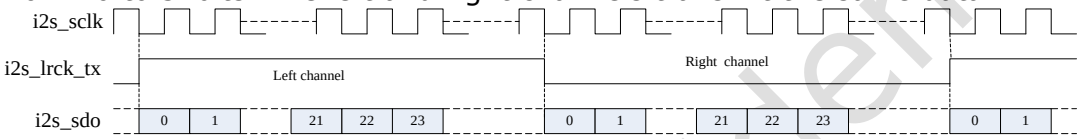

Fig.22-3 I2S Left Justified Mode Timing Format

22.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the LRCK signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

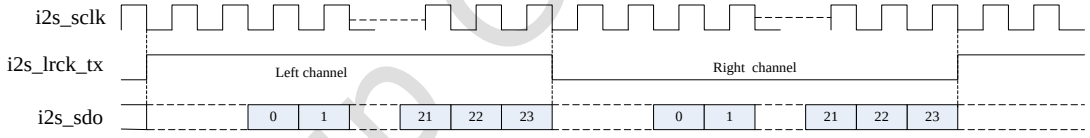

Fig.22-4 I2S Right Justified Mode Timing Format

22.3.4 PCM early mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo) signal, it sends the first bit (MSB or LSB) at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

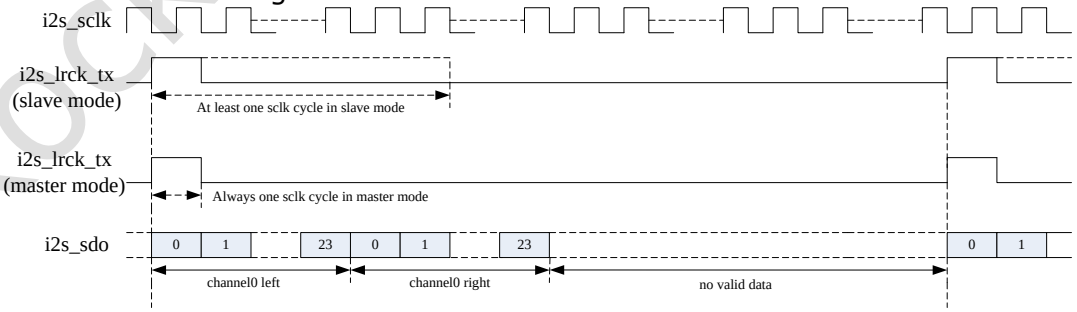

Fig.22-5 PCM Early Mode Timing Format

22.3.5 PCM late1 mode

This is the waveform of PCM late1 mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo) signal, it sends the first bit (MSB or LSB) one SCLK clock cycle after LRCK goes high. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

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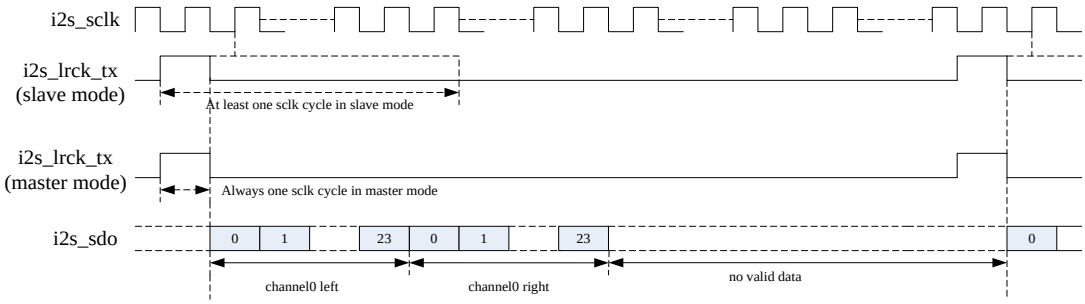

Fig.22-6 PCM Late1 Mode Timing Format

22.3.6 PCM late2 mode

This is the waveform of PCM late2 mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo) signal, it sends the first bit (MSB or LSB) two SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

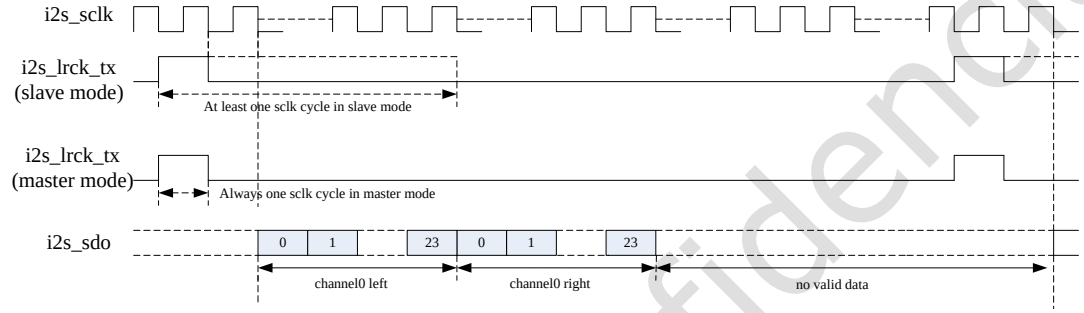

Fig.22-7 PCM Late2 Mode Timing Format

22.3.7 PCM late3 mode

This is the waveform of PCM late3 mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo) signal, it sends the first bit (MSB or LSB) three SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

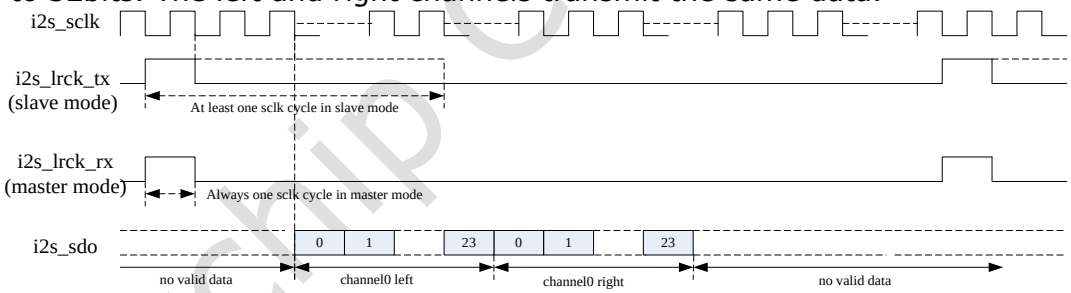

Fig.22-8 PCM Late3 Mode Timing Format

22.3.8 Digital Filters

In order to achieve PCM format audio data from input 1-bit data stream, a total of 5 filters are embedded in ADC module. It includes a CIC decimation filter, a compensation filter, 2 half-band filters and a high pass filter.

The CIC decimation filter achieves 8-timse or 16-times or 32-times or 64-times or 128-times decimation. Which decimation rate is selected depends on the sample rate. For example, in order to output a 12K sample rate signal, 128-times decimation rate need to be selected.

Compensation filter is connected in series following CIC filter. Its function is to reduce the ripple of CIC filter output. It can be software enabled or disabled. It is valid only when CIC decimation filter works in 32-times or 64-times decimation.

The 2 half-band filters each perform 2-times decimation.

The high pass filter is used to filter DC components in audio data stream. The result of high pass filter is sent to the volume control.

22.3.9 Volume Control

The PCM format data output from the high pass filter are fed into the volume control. It can be digitally attenuated over a range of -95.625dB~0dB in 0.375dB/step for negative gain.

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The ADC IP has an 8-bit register for volume control. For negative gain, 0xff corresponds to digital mute while 0x00 corresponds to 0dB.

22.3.10 Frequency Configuration

ACDC_CLK is the input clock of Audio ADC. All internal clocks are generated by ACDC_CLK if the I2S module acts as a master. ACDC_CLK must be homologous to the operation clock of I2S master when the I2S module of Audio ADC acts as a slave. There is another clock named ADC_CLK acting as sample clock generated from ACDC_CLK and sent out to the Analogy Audio ADC. The relationship of ACDC_CLK, ADC_CLK and sample rates is as follows where the ACDC_CLK is 8 times of ADC_CLK. Make sure that the frequency of ACDC_CLK is at least 8 times of ADC_CLK.

Table 22-1 Relationship of ACDC_CLK, ADC_CLK and Sample Rates in Normal Mode

ACDC_CLK	ADC_CLK	Sample rate supported
49.152MHz	6.144MHz	12k/24k/48k/96k/192k
45.1584 MHz	5.6448 MHz	11.025k/22.05k/44.1k/88.2k/176.4k
32.768MHz	4.096MHz	8k/16k/32k/64k/128k

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22.4 Register Description

22.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
Audio_ADC_ADC_0	0x0008	W	0x00000001	Main ADC Function Setting Register 0
Audio_ADC_ADC_1	0x000C	W	0x00000021	Main ADC Function Setting Register 1
Audio_ADC_ADC_2	0x0010	W	0x00000002	Main ADC Function Setting Register 2
Audio_ADC_MIC_PGA_0	0x0014	W	0x00000001	MIC_PGA Block Setting Register 0
Audio_ADC_MIC_PGA_1	0x0018	W	0x00000000	MIC_PGA Block Setting Register 1
Audio_ADC_MIC_PGA_2	0x001C	W	0x00000000	MIC_PGA Block Setting Register 2
Audio_ADC_ADC_LDO	0x0020	W	0x00000008	ADC LDO Setting Register
Audio_ADC_ADC_HK_0	0x0024	W	0x00000000	ADC Housekeeping Block Setting Register 0
Audio_ADC_ADC_HK_1	0x0028	W	0x00000000	ADC Housekeeping Block Setting Register 1
Audio_ADC_DIG_CLKEN	0x002C	W	0x00000000	Digital Enable and Clock Control Register
Audio_ADC_VOL_CTL	0x0030	W	0x00000000	Volume of Digital ADC Configure Register
Audio_ADC_ADC_AGC0	0x0034	W	0x00000002	Digital AGC Configure Register 0
Audio_ADC_ADC_AGC1	0x0038	W	0x00000000	Digital AGC Configure Register 1
Audio_ADC_ADC_AGC2	0x003C	W	0x00000070	Digital AGC Configure Register 2
Audio_ADC_ADC_AGC3	0x0040	W	0x00000006	Digital AGC Configure Register 3
Audio_ADC_ADC_AGC4	0x0044	W	0x00000060	Digital AGC Configure Register 4
Audio_ADC_ADC_AGC5	0x0048	W	0x00000007	Digital AGC Configure Register 5
Audio_ADC_ADC_AGC6	0x004C	W	0x0000005A	Digital AGC Configure Register 6
Audio_ADC_ADC_AGC7	0x0050	W	0x00000004	Digital AGC Configure Register 7
Audio_ADC_ADC_AGC8	0x0054	W	0x00000066	Digital AGC Configure Register 8
Audio_ADC_ADC_STATUS0	0x0058	W	0x00000000	ADC Status Register 0
Audio_ADC_ADC_STATUS1	0x005C	W	0x00000000	ADC Status Register 1
Audio_ADC_ADC_FILTER	0x0060	W	0x0000000B	Digital Filter Configure Register
Audio_ADC_I2S_CKM	0x0064	W	0x00000001	I2S Clock Control Register
Audio_ADC_I2S_TXCR0	0x0068	W	0x000000B8	I2S TX Control Register 0
Audio_ADC_I2S_TXCR1	0x006C	W	0x00000000	I2S TX Control Register 1
Audio_ADC_I2S_TXCMD	0x0070	W	0x00000000	I2S TX Command Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

22.4.2 Detail Registers Description

Audio_ADC_ADC_0

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Address: Operational Base(0xFF4F8000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	adc_delay_clksel ADC sample clock delay control 2'b00: Delay 100% 2'b01: Delay 75% 2'b10: Delay 50% 2'b11: Delay 25%
5:4	RW	0x0	adc_delay_intsel Internal ADC delay control 2'b00: Delay 100% 2'b01: Delay 75% 2'b10: Delay 50% 2'b11: Delay 25%
3:2	RW	0x0	adc_meth_ctrl Meth code select 2'b00: Thermometer code 2'b01: Normal math code 2'b10: One-direction math code 2'b11: Dual-direction math code
1	RW	0x0	adc_zero ADC integrator reset 1'b0: ADC working 1'b1: ADC reset to zero
0	RW	0x1	adc_pwd Analog ADC power down configure 1'b0: Power on 1'b1: Power down

Audio_ADC_ADC_1

Address: Operational Base(0xFF4F8000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	adc_stop_rtz Turn off the RTZ function 1'b0: RTZ on 1'b1: RTZ off

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Bit	Attr	Reset Value	Description
6:4	RW	0x2	adc_ibctrl ADC ibias control 3'b000: 133% 3'b001: 114% 3'b010: 100% 3'b011: 89% 3'b100: 80% 3'b101: 73% 3'b110: 67% 3'b111: 62%
3	RW	0x0	adc_ibop3_inc Increasing ibias of the 3rd integrator 1'b0: 100% 1'b1: 150%
2	RW	0x0	adc_ibop2_inc Increasing ibias of the 2nd integrator 1'b0: 100% 1'b1: 200%
1:0	RW	0x1	adc_ibop1_ctrl Ibias of the 1st integrator control 2'b00: 50% 2'b01: 100% 2'b10: 150% 2'b11: 200%

Audio_ADC_ADC_2

Address: Operational Base(0xFF4F8000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	adc_out_sel ADC output data select 1'b0: Select SDM output as output data 1'b1: Select one clock as output data
5	RW	0x0	adc_chop_sel ADC chop frequency control 1'b0: High speed 1'b1: Low speed
4	RW	0x0	adc_chop_en ADC chop enable 1'b0: Chop on 1'b1: Chop off
3	RW	0x0	adc_eld_off ADC ELD disable control 1'b0: ELD on 1'b1: ELD off

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Bit	Attr	Reset Value	Description
2:0	RW	0x2	adc_captrim Integrator cap calibration control 3'b000: 80% 3'b001: 90% 3'b010: 100% 3'b011: 110% 3'b100: 120% 3'b101: 130% 3'b110: 140% 3'b111: 150%

Audio_ADC_MIC_PGA_0

Address: Operational Base(0xFF4F8000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x00	mic_pga_gain mic_pga output gain increase 5'b00000: 0dB 5'b10000: 3dB 5'b10001: 6dB 5'b10010: 9dB 5'b10011: 12dB 5'b10100: 15dB 5'b10101: 18dB 5'b10110: 21dB 5'b10111: 24dB 5'b11000: 27dB 5'b11001: 30dB 5'b11010: 33dB 5'b11011: 36dB 5'b11100: 39dB 5'b11101: 42dB 5'b11110: 45dB 5'b11111: 48dB others: 0dB
2:1	RW	0x0	mic_pga_input_dec mic_pga input gain decrease 2'b00: -1.34dB 2'b01: -4.34dB 2'b10: -7.34dB 2'b11: -10.34dB
0	RW	0x1	mic_pga_pwd mic_pga and pga_buf power down 1'b0: mic_pga and pga_buf enable 1'b1: mic_pga and pga_buf disable

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Audio_ADC_MIC_PGA_1

Address: Operational Base(0xFF4F8000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	mic_pga_ibias_ctrl mic_pga ibias ctrl 2'b00: 100% (default) 2'b01: 67% 2'b10: 133% 2'b11: 167%
1:0	RW	0x0	mic_pga_chop_sel mic_pga chop clock select 2'b00: No chop (default) 2'b01: fchop=200K 2'b10: fchop=400K 2'b11: fchop=800K

Audio_ADC_MIC_PGA_2

Address: Operational Base(0xFF4F8000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:3	RW	0x0	pga_buf_chop_sel pga_buf chop clock select 2'b00: No chop 2'b01: fchop=200K 2'b10: fchop=400K 2'b11: fchop=800K
2:1	RW	0x0	pga_buf_ib_sel mic_pga ibias ctrl 2'b00: 100% 2'b01: 67% 2'b10: 133% 2'b11: 167%
0	RW	0x0	pga_buf_gain_sel pga_buf gain select 1'b0: 0dB for differential mod 1'b1: 6dB for single mod

Audio_ADC_ADC_LDO

Address: Operational Base(0xFF4F8000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	adc_ip_en ADC enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6:4	RO	0x0	reserved
3:2	RW	0x2	ldo_vsel LDO 1P6V output voltage select 2'b00: 1.5V 2'b01: 1.55V 2'b10: 1.6V 2'b11: 1.65V
1	RW	0x0	ldo_bypass_en LDO_1P6V bypass mode control. 1'b0: Off 1'b1: On
0	RW	0x0	Reserved

Audio_ADC_ADC_HK_0

Address: Operational Base(0xFF4F8000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	hk_ibias_sel hk_ibias_current control: 4'b0000: 100% 4'b0001: 80% 4'b0010: 66% 4'b0111: 36% 4'b1000: 200% 4'b1001: 160% 4'b1010: 133% 4'b1011: 114%
3	RW	0x0	hk_adc_buf_en adc_buf enable control 1'b0: Disable 1'b1: Enable
2	RW	0x0	hk_vag_buf_en vag_buf enable control 1'b0: Disable 1'b1: Enable
1	RW	0x0	hk_half_adc_buf adc_buf_bias_half enable control 1'b0: Disable 1'b1: Enable
0	RW	0x0	hk_half_vag_buf vag_buf_bias_half enable control 1'b0: Disable 1'b1: Enable

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Audio_ADC_ADC_HK_1

Address: Operational Base(0xFF4F8000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	hk_vag_cur_sel hk_vag_buf_cur_sel control 2'b00: 6uA 2'b01: 4uA 2'b10: 3uA 2'b11: 1uA
1:0	RW	0x0	hk_vref_1p2v_sel hk_vref_1p2v_sel<1:0>: 2'b00: normal (default=1.2) 2'b01: normal - 10m 2'b10: normal + 10m 2'b11: normal - 20m

Audio_ADC_DIG_CLKEN

Address: Operational Base(0xFF4F8000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	adc_cke ADC clock enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	i2stx_cke Clock enable of internal I2S TX channel. 1'b0: Disable 1'b1: Enable
5	RW	0x0	adc_en ADC channel enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	i2stx_en I2S TX channel enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	srst Soft reset, write 1 to reset all registers to default value. 1'b0: Not reset 1'b1: Reset

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	adcsrt Selects which kind of sample rate. 3'b000: 12kHz/11.025kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 48kHz/44.1kHz/32kHz 3'b011: 96kHz/88.2kHz/64kHz 3'b100~3'b111: 192kHz/176.4kHz/128kHz

Audio_ADC_VOL_CTL

Address: Operational Base(0xFF4F8000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	adc_volume ADC path Digital Volume Register. 0dB~-95.625dB, -0.375dB/step. 8'h0: 0dB 8'h1: -0.375dB 8'h2: -0.75dB 8'h3: -1.125dB ... 8'hff: -95.625dB

Audio_ADC_ADC_AGC0

Address: Operational Base(0xFF4F8000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	adc_agc_offset LSB 4bits of adc_agc_offset; adc_agc_offset: Adjust calculated received signal power in dB, it is represented by two's complement with 1 sign bit, 4 integer bits, 4 fractional bits. 9'h000: 0 dB 9'h001: 0.0625 dB 9'h002: 0.125 dB 9'h003: 0.1875 dB 9'h004: 0.25 dB ... 9'h0FF: 15.9375 dB 9'h100: -16 dB 9'h101: -15.9375 dB 9'h102: -15.875 dB ... 9'h1FF: -0.0625 dB

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Bit	Attr	Reset Value	Description
3	RW	0x0	adc_byps ADC volume control bypass. 1'b0: ADC volume control enable 1'b1: ADC volume control bypass
2	RW	0x0	agc_zerocren Gain adjusting at zero-crossing enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	adc_ng_mode_en Noise gate enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	adc_agc_ena Automatic Gain control enable. 1'b0: Disable 1'b1: Enable

Audio_ADC_ADC_AGC1

Address: Operational Base(0xFF4F8000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	adc_agc_offset MSB 5bits of adc_agc_offset; adc_agc_offset: Adjust calculated received signal power in dB, it is represented by two's complement with 1 sign bit, 4 integer bits, 4 fractional bits. 9'h000: 0 dB 9'h001: 0.0625 dB 9'h002: 0.125 dB 9'h003: 0.1875 dB 9'h004: 0.25 dB ... 9'h0FF: 15.9375 dB 9'h100: -16 dB 9'h101: -15.9375 dB 9'h102: -15.875 dB ... 9'h1FF: -0.0625 dB

Audio_ADC_ADC_AGC2

Address: Operational Base(0xFF4F8000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x70	adc_ng_rssi_db LSB 8bits of adc_ng_rssi_db; adc_ng_rssi_db: noise gate threshold in dB, it is represented by two's complement with 1 sign bit, 7 integer bits, 3 fractional bits. 11'h000: 0 dB 11'h001: 0.125 dB 11'h002: 0.25 dB ... 11'h400: -128 dB 11'h401: -127.875 dB 11'h402: -127.75 dB ... 11'h7FF: -0.125 dB

Audio_ADC_ADC_AGC3

Address: Operational Base(0xFF4F8000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x00	adc_ng_pga_gain Analog ADC PGA gain configure when in noise gate mode. 5'b00000: 0dB 5'b10000: 3dB 5'b10001: 6dB 5'b10010: 9dB 5'b10011: 12dB 5'b10100: 15dB 5'b10101: 18dB 5'b10110: 21dB 5'b10111: 24dB 5'b11000: 27dB 5'b11001: 30dB 5'b11010: 33dB 5'b11011: 36dB 5'b11100: 39dB 5'b11101: 42dB 5'b11110: 45dB 5'b11111: 48dB others: 0dB

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Bit	Attr	Reset Value	Description
2:0	RW	0x6	adc_ng_rssi_db MSB 3bits of adc_ng_rssi_db; adc_ng_rssi_db: noise gate threshold in dB, it is represented by two's complement with 1 sign bit, 7 integer bits, 3 fractional bits. 11'h000: 0 dB 11'h001: 0.125 dB 11'h002: 0.25 dB ... 11'h400: -128 dB 11'h401: -127.875 dB 11'h402: -127.75 dB ... 11'h7FF: -0.125 dB

Audio_ADC_ADC_AGC4

Address: Operational Base(0xFF4F8000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	adc_tar_db LSB 8bits of adc_tar_db; adc_tar_db: target output signal power in dB, it is represented by two's complement with 1 sign bit, 7 integer bits, 3 fractional bits. 11'h000: 0 dB 11'h001: 0.125 dB 11'h002: 0.25 dB ... 11'h400: -128 dB 11'h401: -127.875 dB 11'h402: -127.75 dB ... 11'h7FF: -0.125 dB

Audio_ADC_ADC_AGC5

Address: Operational Base(0xFF4F8000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:3	RW	0x00	adc_ini_pga_gain Initial Analog ADC PGA gain configure when AGC enable. 5'b00000: 0dB 5'b10000: 3dB 5'b10001: 6dB 5'b10010: 9dB 5'b10011: 12dB 5'b10100: 15dB 5'b10101: 18dB 5'b10110: 21dB 5'b10111: 24dB 5'b11000: 27dB 5'b11001: 30dB 5'b11010: 33dB 5'b11011: 36dB 5'b11100: 39dB 5'b11101: 42dB 5'b11110: 45dB 5'b11111: 48dB others: 0dB
2:0	RW	0x7	adc_tar_db MSB 3bits of adc_tar_db; adc_tar_db: target output signal power in dB, it is represented by two's complement with 1 sign bit, 7 integer bits, 3 fractional bits. 11'h000: 0 dB 11'h001: 0.125 dB 11'h002: 0.25 dB ... 11'h400: -128 dB 11'h401: -127.875 dB 11'h402: -127.75 dB ... 11'h7FF: -0.125 dB

Audio_ADC_ADC_AGC6

Address: Operational Base(0xFF4F8000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x5a	adc_ng_vol_ctrl Digital volume configure when in noise gate mode. 0dB~-96dB, -0.375dB/step. 8'h0: 0dB 8'h1: -0.375dB 8'h2: -0.75dB 8'h3: -1.125dB ... 8'hff: -95.625dB

Audio_ADC_ADC_AGC7

Address: Operational Base(0xFF4F8000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x04	adc_ini_vol_ctrl Initial Digital volume configure when AGC enable. 0dB~-96dB, -0.375dB/step. 8'h0: 0dB 8'h1: -0.375dB 8'h2: -0.75dB 8'h3: -1.125dB ... 8'hff: -95.625dB

Audio_ADC_ADC_AGC8

Address: Operational Base(0xFF4F8000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x6	adc_prattrate_win Attack/release rate = 2^adc_prattrate_win.
3:0	RW	0x6	adc_powdet_win AGC power detect length = 2^adc_powdet_win.

Audio_ADC_ADC_STATUS0

Address: Operational Base(0xFF4F8000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	adcrlv ADC internal volume.

Audio_ADC_ADC_STATUS1

Address: Operational Base(0xFF4F8000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5	RO	0x0	adc_ngvalid Noise gates valid status. 1'b0: Not in NG status 1'b1: Now in NG status
4:0	RO	0x00	adc_pga_gain_r Gain of ADC PGA block.

Audio_ADC_ADC_FILTER

Address: Operational Base(0xFF4F8000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	hpf_cf HPF Cut Frequency Select. 2'b00: 3.79HZ 2'b01: 60HZ 2'b10: 243HZ 2'b11: 493HZ
5	RO	0x0	reserved
4	RW	0x0	hpfl Digital ADC High Pass Filter Enable. 1'b0: Disable 1'b1: Enable
3:2	RW	0x2	ciccomp_cf CIC Compensation Filter Output Scale Coefficient. 2'h0: 3/8 2'h1: 6/8 2'h2,2'h3: 1
1	RW	0x1	ciccomp_ena64 CIC compensation filter enable, valid when sample rate is 24kHz/22.05kHz/16kHz. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ciccomp_ena32 CIC compensation filter enable, valid when sample rate is 48kHz/44.1kHz/32kHz. 1'b0: Disable 1'b1: Enable

Audio_ADC_I2S_CKM

Address: Operational Base(0xFF4F8000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sck_div Interger clock divider to generate sclk when I2S TX works in master mode. It is ignored when in slave mode. sck_div = F(mclk2x)/F(sclk) - 1
3	RO	0x0	reserved
2	RW	0x0	sck_en SCLK clock enable, active in master mode. 1'b0: Disable 1'b1: Enable
1	RW	0x0	sck_p SCLK polarity. 1'b0: Normal 1'b1: Inverted
0	RW	0x1	i2s_mst I2S TX acts as master or slave. 1'b0: Slave mode 1'b1: Master mode

Audio_ADC_I2S_TXCR0

Address: Operational Base(0xFF4F8000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x17	vdw_tx I2S TX valid data width. 5'b00000-5'b01110: reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit ... 5'10111: 24bit 5'b10111: 25bit 5'b10111: 26bit 5'b10111: 27bit 5'b10111: 28bit 5'b10111: 29bit 5'b10111: 30bit 5'b10111: 31bit 5'b10111: 32bit
2:1	RW	0x0	sckd_tx Sclk divider for tx_lrck generator. 2'b00: 64 2'b01: 128 2'b10~2'b11: 256 2'b01 valid only if LRCK <= 96k, 2'b10 valid only if LRCK <= 48k

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Bit	Attr	Reset Value	Description
0	RW	0x0	txrl_p I2S TX LRCK polarity. 1'b0: Normal 1'b1: Inverted

Audio_ADC_I2S_TXCR1

Address: Operational Base(0xFF4F8000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	tfs_tx I2S TX transfer mode. 1'b0: I2S 1'b1: PCM
5:4	RW	0x0	pbm_tx I2S TX PCM bus mode. 2'b00: PCM early mode 2'b01: PCM late 1 mode 2'b10: PCM late 2 mode 2'b11: PCM late 3 mode
3:2	RW	0x0	ibm_tx I2S TX bus mode. 2'b00: Normal 2'b01: Left 2'b10: Right
1	RW	0x0	exrl_tx Exchange right/left channel for I2S TX 1'b0: Normal 1'b1: Exchange right and left channel
0	RW	0x0	lsb_tx I2S TX MSB/LSB send first. 1'b0: MSB send first 1'b1: LSB send first

Audio_ADC_I2S_TXCMD

Address: Operational Base(0xFF4F8000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txs I2S TX transfer start. 1'b0: Stop I2S TX transfer 1'b1: Start I2S TX transfer
6	RW	0x0	txc This is a self-cleared bit. Write 1 to clear all I2S TX transmit logic. 1'b0: No clean the I2STX transmit logic 1'b1: Clean the I2STX transmit logic

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	rcnt_tx Right justified counter for I2S right justified slave mode only.

22.5 Application Notes

22.5.1 Hardware Application Notes:

1. Put the LDO filter cap close to the output Pin of ADC_LDO.
2. Give a Clean ground to the LDO filter cap and AVSS.

22.5.2 Software Application Notes

Steps to configure Audio ADC operates in I2S mode are as follows.

1. Program Audio_ADC_ADC_LDO to power up the HK circuit and LDO circuit.
2. Program the gain of PGA_Block and PGA_Buffer by Audio_ADC_MIC_PGA_0, Audio_ADC_MIC_PGA_1, Audio_ADC_MIC_PGA_2.
3. Program Audio_ADC_DIG_CLKEN to enable operation clocks of I2S module and ADC.
4. Program Audio_ADC_I2S_CKM to select sample rate.
5. Program Audio_ADC_ADC_0 to power up the analog ADC circuit.
6. Enable high pass filter if necessary by Programming Audio_ADC_ADC_FILTER.

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Chapter 23 Serial Audio Interface (SAI)

23.1 Overview

The SAI controller is designed for interfacing between the AHB bus and the serial audio interface bus. The SAI is a serial link for digital audio data transfer between devices in the system. The SAI interface (Serial Audio Interface) offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted. I2S standards, PCM, and TDM may be addressed.
SAI is widely used in the devices such as ADC, DAC, DSP, CPU, etc. With the SAI interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.

23.1.1 Features

- Support eight internal 32-bit wide and 32-location deep FIFOs, four for transmitting and the other for receiving audio data
- Support AHB bus interface
- Support 8 ~ 32 bits audio data transfer
- Support master and slave mode
- Support DMA handshaking interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combined interrupt output
- Support 8 to 32 bit audio data left or right justified in 32-bit wide FIFO
- Support two 16-bit audio data store together in one 32-bit wide location and support four 8-bit audio data store together in one 32-bit wide location
- Support TX to RX loopback bypass mode
- Support audio protocol: I2S, PCM, TDM
- Support number of bits by frame can be configurable
- Support first active slot position in the frame is configurable
- Support up to 128 slots available with configurable size
- Support slot length 8 to 32 bits configurable
- Support slot valid data length 8 to 32 bits configurable
- Support mono audio mode
- Support slot mask configurable
- Support first active bit position in the slot is configurable
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and FS polarity
- Support up to four lanes parallel transceivers
- Support SDI, SDO IOMUX

23.2 Block Diagram

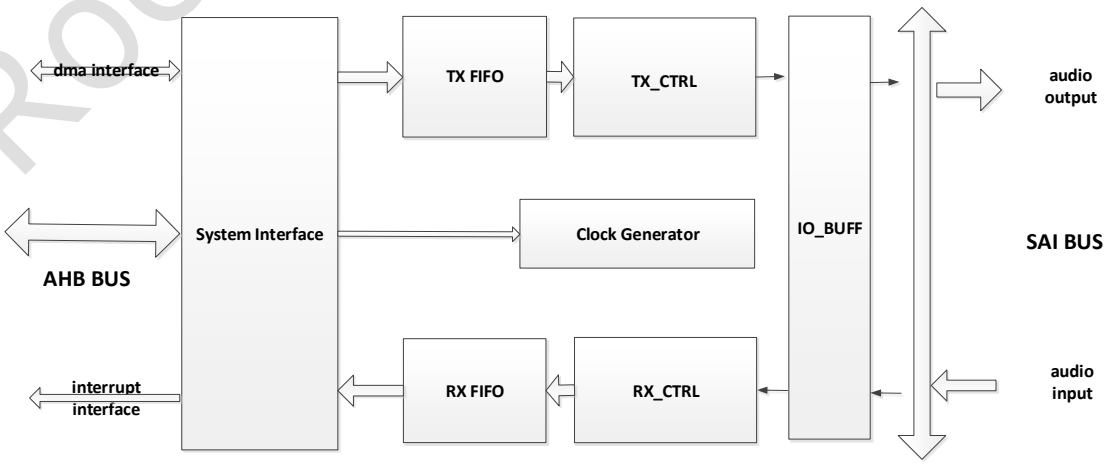

Fig. 23-1 SAI Block Diagram

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System Interface
The system interface implements the AHB slave operation. It contains not only control registers of transmitter and receiver inside but also interrupt and DMA handshaking interface.
Clock Generator
The Clock Generator implements clock generation function. The input source clock to the module is MCLK_SAI, and by the divider of the module, the clock generator generates SCLK and FS to transmitter and receiver.
Transmitters
The Transmitters implement transmission operation. The transmitters can act as either a master or a slave, with I2S, PCM or TDM mode surround serial audio interface.
Receiver
The Receiver implements receive operation. The receiver can act as either a master or a slave, with I2S, PCM or TDM mode stereo serial audio interface.
Transmit FIFO
The Transmit FIFO is the buffer to store transmitted audio data. The size of the FIFO is 32bits x 32.
Receive FIFO
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 32.
IO_BUFF
SDO, SDI, LRCK_IN and LRCK_OUT register output.

23.3 Function Description

In the SAI controller, there are two types:
transmitter-master &receiver-master, transmitter-slave & receiver-slave.
In broadcasting application, the SAI controller is used as a transmitter and external or internal audio CODEC is used as a receiver. In recording application, the SAI controller is used as a receiver and external or internal audio CODEC is used as a transmitter. Either the SAI controller or the audio CODEC can act as a master or a slave, but if one is master, the other must be slave.

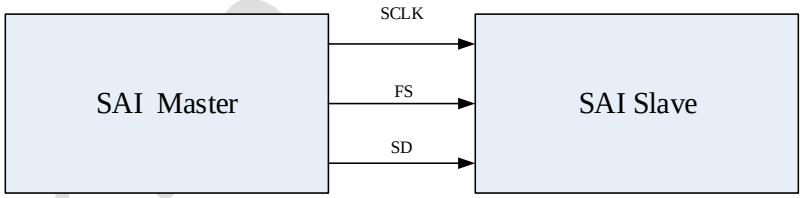

Fig.23-2 SAI transmitter-master & receiver-slave condition

When the transmitter acts as a master, it sends all signals to the receiver (the slave), and CPU controls when to send clock and data to the receiver. When acts as a slave, SD signal still goes from transmitter to receiver, but SCLK and FS signals are from the receiver (the master) to the transmitter. Based on three interface specifications, transmitting data should be ready before transmitter receives SCLK and FS signals. CPU should know when the receiver to initialize a transaction and when the transmitter to send data.
When the receiver acts as a master, it sends SCLK and FS signals to the transmitter (the slave) and receives serial data. So CPU must tell the transmitter when to start a transaction for it to prepare transmitting data then start a transfer and send clock and channel-select signals. When the receiver acts as a slave, CPU should only do initial setting and wait for all signals and then start reading data.
Before transmitting or receiving data, CPU need do initial setting to the SAI register. These includes CPU settings, SAI interface registers settings, and maybe the embedded SoC platform settings. These registers must be set before starting data transfer.
The SAI interface offers a wide set of audio protocols due to its flexibility and wide range of configurations. It can support I2S/PCM/TDM audio protocol by different configuration.

23.3.1 I2S normal mode

This is the waveform of I2S normal mode. For FS (sai_fs_rx/sai_fs_tx) signal, it goes low to

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indicate left channel and high to right channel. For SD (sai_sdo, sai_sdi) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after FS changes. The range of SD signal width is from 8 to 32bits.

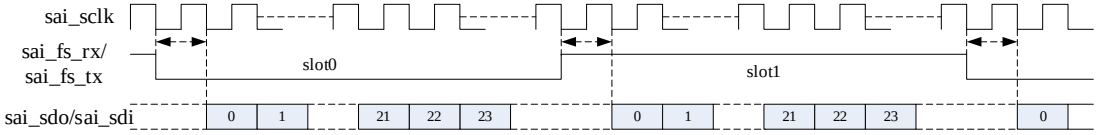

Fig.23-3 I2S Normal Mode Timing Format

23.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sai_sdo/ sai_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when FS changes. The range of SD signal width is from 8 to 32bits.

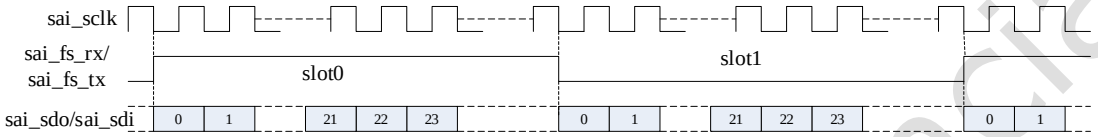

Fig.23-4 I2S Left Justified Mode Timing Format

23.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sai_sdo, sai_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the FS signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 8 to 32bits.

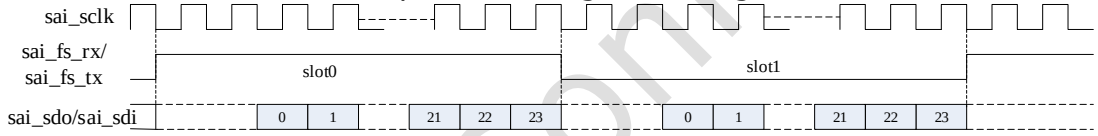

Fig.23-5 I2S Right Justified Mode Timing Format

23.3.4 PCM early mode

This is the waveform of PCM early mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (sai_sdo, sai_sdi) signal, it sends the first bit (MSB or LSB) at the same time when FS goes high. The range of SD signal width is from 8 to 32bits.

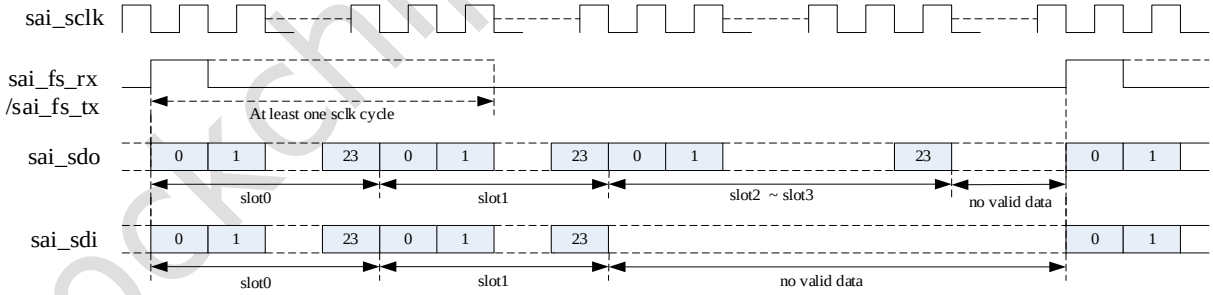

Fig.23-6 PCM Early Mode Timing Format

23.3.5 Flexibility and wide range of configurations

The SAI interface offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted. I2S standards, PCM, and TDM may be addressed.

This is the waveform of PCM mode (SBW==VDW,FW >=SBW *SNB). For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate the start of a group of audio data.

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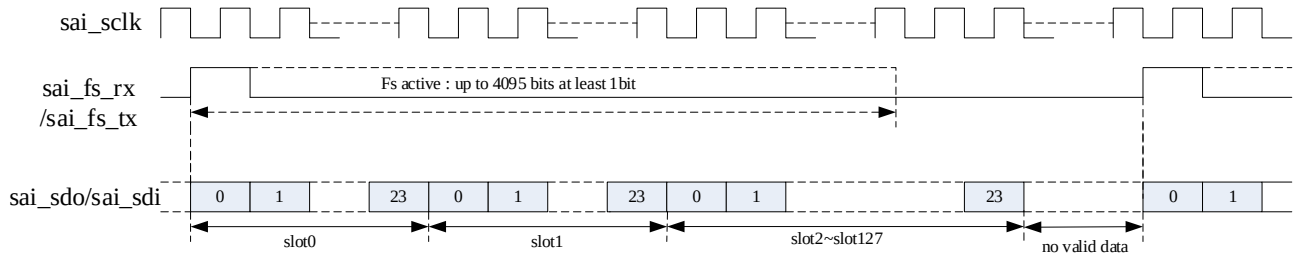

Fig.23-7 SAI PCM mode timing format

This is the waveform of I2S left mode(SBW>=VDW,FW >=SBW *SNB,VDJ==1'b1).

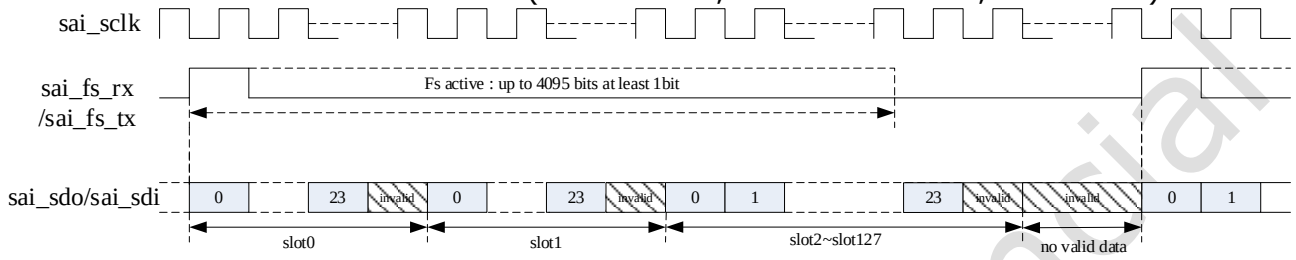

Fig.23-8 SAI I2S left mode timing format

This is the waveform of I2S right mode(SBW>=VDW,FW >=SBW *SNB,VDJ==1'b0).

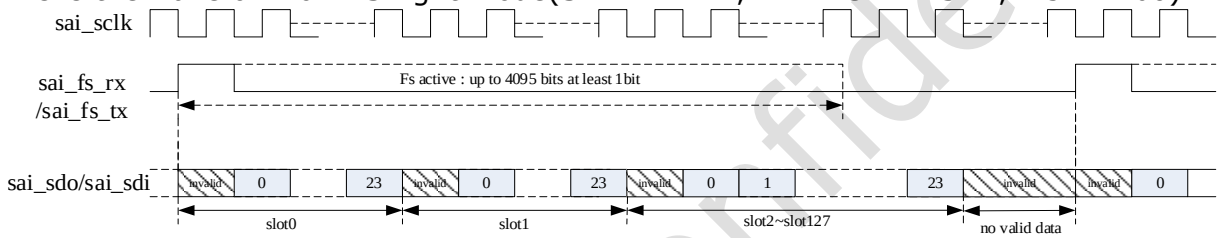

Fig.23-9 SAI I2S right mode timing format

This is the waveform of FS and SD delay time, as the posedge of FS (sai_fs_rx / sai_fs_tx) signal, we can send data at different time, The time between the FS rise edge and the first valid bit can be configured using the fs_shift register, when fs_shift[0] == 1'b0, data send at posedge of sclk,when fs_shift[0] == 1'b1, data send at negedge of sclk.

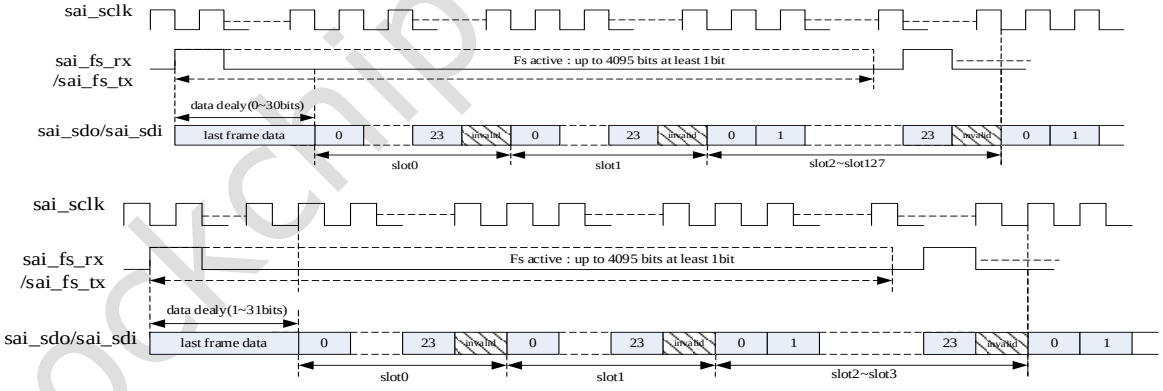

Fig.23-10 fs shift timing format

23.4 Register Description

23.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SAI0	0xFF300000
SAI1	0xFF310000
SAI2	0xFF498000
SAI3	0xFF4A0000

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Name	Base Address
SAI4	0xFF4A8000

23.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SAI_TXCR	0x0000	W	0x00000FFF	Transmit Operation Control Register
SAI_FSCR	0x0004	W	0x0001F03F	Transmit Frame Sync Operation Control Register
SAI_RXCR	0x0008	W	0x00000FFF	Receive Operation Control Register
SAI_MONO_CR	0x000C	W	0x00000000	Mono mode control
SAI_XFER	0x0010	W	0x00000000	Transfer Start Register
SAI_CLR	0x0014	W	0x00000000	Sclk Domain Logic Clear Register
SAI_CKR	0x0018	W	0x00000000	Clock Generation Register
SAI_TXFIFOLR	0x001C	W	0x00000000	TX FIFO Level Register
SAI_RXFIFOLR	0x0020	W	0x00000000	RX FIFO Level Register
SAI_DMACR	0x0024	W	0x00000000	DMA Control Register
SAI_INTCR	0x0028	W	0x01F00000	Interrupt Control Register
SAI_INTSR	0x002C	W	0x00000000	Interrupt Status Register
SAI_TXDR	0x0030	W	0x00000000	Transmit FIFO Data Register
SAI_RXDR	0x0034	W	0x00000000	Receive FIFO Data Register
SAI_PATH_SEL	0x0038	W	0x0000E4E4	Path Select Register
SAI_TX_SLOT_MASK0	0x003C	W	0x00000000	Transmit Slot 0~31 Mask State
SAI_TX_SLOT_MASK1	0x0040	W	0x00000000	Transmit Slot 32~63 Mask State
SAI_TX_SLOT_MASK2	0x0044	W	0x00000000	Transmit Slot 64~95 Mask State
SAI_TX_SLOT_MASK3	0x0048	W	0x00000000	Transmit Slot 96~127 Mask State
SAI_RX_SLOT_MASK0	0x004C	W	0x00000000	Receive Slot 0~31 Mask State
SAI_RX_SLOT_MASK1	0x0050	W	0x00000000	Receive Slot 32~63 Mask State
SAI_RX_SLOT_MASK2	0x0054	W	0x00000000	Receive Slot 64~95 Mask State
SAI_RX_SLOT_MASK3	0x0058	W	0x00000000	Receive Slot 96~127 Mask State
SAI_TX_DATA_CNT	0x005C	W	0x00000000	Tx Data Counter Register
SAI_RX_DATA_CNT	0x0060	W	0x00000000	Rx Data Counter Register
SAI_SAI_TX_SHIFT	0x0064	W	0x00000000	Tx Shift Register
SAI_SAI_RX_SHIFT	0x0068	W	0x00000000	Rx Shift Register
SAI_SAI_RD_STATUS	0x006C	W	0x0000000F	
SAI_VERSION	0x0070	W	0x24013506	Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.4.3 Detail Registers Description

SAI_TXCR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	tx_delay_en 1'b0: NO DELAY 1'b1: DELAY fsync pos
21:20	RW	0x0	tcsr Transmit channel select register 2'b00: One channel parallel 2'b01: Two channel parallel 2'b10: Three channel parallel 2'b11: Four channel parallel

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Bit	Attr	Reset Value	Description
19	RW	0x0	sjm Store justified mode (Can be written only when XFER[0] bit is 0.) 8bit~31bit DATA stored in 32 bits width FIFO. 1'b0: Right justified 1'b1: Left justified
18	RW	0x0	fbm first bit mode (Can be written only when XFER[0] bit is 0.) 1'b0: MSB 1'b1: LSB
17:11	RW	0x01	snb Transfer slot number (Can be written only when XFER[0] bit is 0.) Number of slots in a frame 7'h00: 1slot 7'h01: 2slot 7'h02: 3slot 7'h03: 4slot ..... 7'h7e: 127slot 7'h7f: 128slot
10	RW	0x1	vdj Valid data justified mode (Can be written only when XFER[0] bit is 0.) 1'b0: Right justified 1'b1: Left justified
9:5	RW	0x1f	sbw Transfer slot bits width (Can be written only when XFER[0] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit
4:0	RW	0x1f	vdw Slot valid data width (Can be written only when XFER[0] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit

SAI_FSCR

Address: **Operational Base** + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	edge_sel 1'h0: pos 1'h1: pos and neg
23:12	RW	0x01f	fpw Transfer frame pulse width (Can be written only when XFER[0] is 0.) 12'h000: 1bit 12'h001: 2bit 12'h002: 3bit ..... 12'hffe:4095bit 12'hfff:res
11:0	RW	0x03f	fw Transfer frame width (Can be written only when XFER[0] is 0.) 12'h000~12'h006: Reserved 12'h007: 8bit 12'h008: 9bit ..... 12'hffe: 4095bit 12'hfff: 4096bit

SAI_RXCR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	rx_delay_en 1'b0: NO DELAY 1'b1: DELAY fsync pos
21:20	RW	0x0	rcsr receive channel select register 2'b00: One channel parallel 2'b01: Two channel parallel 2'b10: Three channel parallel 2'b11: Four channel parallel
19	RW	0x0	sjm Store justified mode (Can be written only when XFER[2] bit is 0.) 8bit~31bit DATA stored in 32 bits width FIFO. 1'b0: Right justified 1'b1: Left justified
18	RW	0x0	fbm first bit mode (Can be written only when XFER[2] bit is 0.) 1'b0: MSB 1'b1: LSB

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Bit	Attr	Reset Value	Description
17:11	RW	0x01	snb receive slot number (Can be written only when XFER[2] bit is 0.) number of slots in a frame 7'h00: 1slot 7'h01: 2slot 7'h02: 3slot 7'h03: 4slot ..... 7'h7e: 127slot 7'h7f: 128slot
10	RW	0x1	vdj Valid data justified mode (Can be written only when XFER[2] bit is 0.) 1'b0: Right justified 1'b1: Left justified
9:5	RW	0x1f	sbw receive slot bits width (Can be written only when XFER[2] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit
4:0	RW	0x1f	vdw Valid fata width (Can be written only when XFER[2] bit is 0.) 5'h00~5'b0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1c: 29bit 5'h1d: 30bit 5'h1e: 31bit 5'h1f: 32bit

SAI_MONO_CR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:2	RW	0x00	rx_mono_slot_sel Receive mono mode valid slot data select 7'h00: First slot data valid 7'h01: Second slot data valid ..... 7'h7f: Slot128 data valid

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Bit	Attr	Reset Value	Description
1	RW	0x0	rx_mono_en Receive mono audio data enable bit 1'b0: Normal mode 1'b1: Mono mode
0	RW	0x0	tx_mono_en Transmit mono audio data enable bit 1'b0: Normal mode 1'b1: Mono mode

SAI_XFER

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	rx_data_cnt_en 1'b0: Stop cnt 1'b1: Start cnt
4	RW	0x0	tx_data_cnt_en 1'b0: Stop cnt 1'b1: Start cnt
3	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
2	RW	0x0	txs 1'b0: Stop TX transfer 1'b1: Start TX transfer
1	RW	0x0	fss 1'b0: Stop frame sync 1'b1: Start frame sync
0	RW	0x0	clk_gate_en 1'b0: Stop clk 1'b1: Start clk

SAI_CLR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	fsc This is a self-cleared bit. write 1 to clear all receive logic.
1	W1C	0x0	rxc RX logic clear This is a self-cleared bit. write 1 to clear all receive logic.
0	W1C	0x0	txc TX logic clear This is a self-cleared bit. write 1 to clear all transmit logic.

SAI_CKR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:3	RW	0x000	mdiv (Can be written only when XFER[0] bit is 0.) mclk divider = (mclk/sclk)-1. For example, if mclk divider is 5, then the frequency of sclk is mclk/6.

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Bit	Attr	Reset Value	Description
2	RW	0x0	mss Transmit master/slave mode select (Can be written only when XFER[0] bit is 0.) 1'b0: Master mode(sclk output) 1'b1: Slave mode(sclk input)
1	RW	0x0	ckp Transmit sclk polarity (Can be written only when XFER[2] or XFER[0] bit is 0.) 1'b0: Sample data at posedge sclk and drive data at negedge sclk 1'b1: Sample data at negedge sclk and drive data at posedge sclk
0	RW	0x0	fsp Transmit fs polarity (Can be written only when XFER[2] or XFER[0] bit is 0.) 1'b0: Frame sync low active 1'b1: Frame sync high active

SAI_TXFIFOLR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	tfl3 Transmit fifo3 level Contains the number of valid data entries in the transmit fifo3.
17:12	RO	0x00	tfl2 Transmit fifo2 level Contains the number of valid data entries in the transmit fifo2.
11:6	RO	0x00	tfl1 Transmit fifo1 level Contains the number of valid data entries in the transmit fifo1.
5:0	RO	0x00	tfl0 Transmit fifo0 level Contains the number of valid data entries in the transmit fifo0.

SAI_RXFIFOLR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	rfl3 Receive fifo3 level Contains the number of valid data entries in the receive fifo3.
17:12	RO	0x00	rfl2 Receive fifo2 level Contains the number of valid data entries in the receive fifo2.
11:6	RO	0x00	rfl1 Receive fifo1 level Contains the number of valid data entries in the receive fifo1.
5:0	RO	0x00	rfl0 Receive fifo0 level Contains the number of valid data entries in the receive fifo0.

SAI_DMACR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	rde Receive DMA enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
23:21	RO	0x0	reserved
20:16	RW	0x00	rdl Receive data level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
15:9	RO	0x00	reserved
8	RW	0x0	tde Transmit DMA enable 1'b0: Transmit DMA disabled 1'b1: Transmit DMA enabled
7:5	RO	0x0	reserved
4:0	RW	0x00	tdl Transmit data level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the TX FIFO(TX FIFO0 if CSR=00;TX FIFO1 if CSR=01,TX FIFO2 if CSR=10,TX FIFO3 if CSR=11)is equal to or below this field value.

SAI_INTCR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RW	0x1f	rft Receive fifo threshold When the number of receive fifo entries is more than or equal to this threshold plus 1, the receive fifo full interrupt is triggered.
19	RO	0x0	reserved
18	WO	0x0	rxoic RX overrun interrupt clear Write 1 to clear RX overrun interrupt.
17	RW	0x0	rxoie RX overrun interrupt enable 1'b0: Disable 1'b1: Enable
16	RW	0x0	rxfie RX full interrupt enable 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8:4	RW	0x00	tft Transmit fifo threshold When the number of transmit fifo entries is less than or equal to this threshold, the transmit fifo empty interrupt is triggered.
3	RO	0x0	reserved
2	W1C	0x0	txuic TX underrun interrupt clear Write 1 to clear TX underrun interrupt.

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Bit	Attr	Reset Value	Description
1	RW	0x0	txuie TX underrun interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	txeie TX empty interrupt enable 1'b0: Disable 1'b1: Enable

SAI_INTSR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	rxoi RX overrun interrupt 1'b0: Inactive 1'b1: Active
16	RO	0x0	rxfi RX full interrupt 1'b0: Inactive 1'b1: Active
15:2	RO	0x0000	reserved
1	RO	0x0	txui TX underrun interrupt 1'b0: Inactive 1'b1: Active
0	RO	0x0	txei TX empty interrupt 1'b0: Inactive 1'b1: Active

SAI_TXDR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdr Transmit fifo fata register When it is written, data are moved into the transmit fifo.

SAI_RXDR

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxdr Receive fifo data register When the register is read, data in the receive fifo is accessed.

SAI_PATH_SEL

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:22	RW	0x00	sdo_to_sdi_path_sel SDO_TO_SDI_PATH_SEL [23:22]:sdi0 sel sdo0 or sdo1 or sdo2 or sdo3 [25:24]:sdi1 sel sdo0 or sdo1 or sdo2 or sdo3 [27:26]:sdi2 sel sdo0 or sdo1 or sdo2 or sdo3 [29:28]:sdi3 sel sdo0 or sdo1 or sdo2 or sdo3

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Bit	Attr	Reset Value	Description
21:18	RW	0x0	loopback_bypass Loopback by pass enable bit Tx_sdo -> Rx_sdi loopback mode should work at fs_tx_as_common mode and tx=rx=master [18]:Loopback_en0 [19]:Loopback_en1 [20]:Loopback_en2 [21]:Loopback_en3 1'b0: No active 1'b1: Active
17	RW	0x0	sync_out_sel Tx sync out select bit 1'b0: Tx sclk and fs sync out use out signal 1'b1: Tx sclk and fs sync out use in signal
16	RW	0x0	sync_in_sel Tx sync in select bit 1'b0: Tx sclk and fs use pad signal 1'b1: Tx sclk and fs use sync input port
15:14	RW	0x3	rx_path_select3 Rx path select 2'b00: Path3 data from sdi0 2'b01: Path3 data from sdi1 2'b10: Path3 data from sdi2 2'b11: Path3 data from sdi3
13:12	RW	0x2	rx_path_select2 Rx path select 2'b00: Path2 data from sdi0 2'b01: Path2 data from sdi1 2'b10: Path2 data from sdi2 2'b11: Path2 data from sdi3
11:10	RW	0x1	rx_path_select1 Rx path select 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3
9:8	RW	0x0	rx_path_select0 Rx path select 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3
7:6	RW	0x3	tx_path_select3 TX path select 2'b00: Sdo3 output data from path0 2'b01: Sdo3 output data from path1 2'b10: Sdo3 output data from path2 2'b11: Sdo3 output data from path3
5:4	RW	0x2	tx_path_select2 TX path select 2'b00: Sdo2 output data from path0 2'b01: Sdo2 output data from path1 2'b10: Sdo2 output data from path2 2'b11: Sdo2 output data from path3

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	tx_path_select1 TX path select 2'b00: Sdo1 output data from path0 2'b01: Sdo1 output data from path1 2'b10: Sdo1 output data from path2 2'b11: Sdo1 output data from path3
1:0	RW	0x0	tx_path_select0 TX path select 2'b00: Sdo0 output data from path0 2'b01: Sdo0 output data from path1 2'b10: Sdo0 output data from path2 2'b11: Sdo0 output data from path3

SAI_TX_SLOT_MASK0

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask0 Transmit slot 0~31 mask state slot 0~31 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK1

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask1 Transmit slot 32~63 mask state slot 32~63 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK2

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask2 Transmit slot 64~95 mask state slot 64~95 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_SLOT_MASK3

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask3 Transmit slot 96~127 mask state slot 96~127 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK0

Address: **Operational Base** + offset (0x004C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask0 Receive slot 0~31 mask state Slot 0~31 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK1

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask1 Receive slot 32~63 mask state slot 32~63 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK2

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask2 Receive slot 64~95 mask state slot 64~95 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_RX_SLOT_MASK3

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask3 Receive Slot 96~127 mask state slot 96~127 mask state 0: Slot active 1: Slot mask,data is invalid

SAI_TX_DATA_CNT

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	tx_data_cnt Tx data counter

SAI_RX_DATA_CNT

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data_cnt Rx data counter

SAI_SAI_TX_SHIFT

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:0	RW	0x000000	fs_shift Transfer frame sync pulse shift control 24'h00: Normal mode 24'h01: Fs 1/2 cycle shift left. 24'h02: Fs 1 cycle shift left. 24'h03: Fs 3/2 cycle shift left. .....

SAI_SAI_RX_SHIFT

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	fs_shift Transfer frame sync pulse shift control 24'h00: Normal mode 24'h01: Fs 1/2 cycle shift left. 24'h02: Fs 1 cycle shift left. 24'h03: Fs 3/2 cycle shift left. .....

SAI_SAI_RD_STATUS

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x1	rx_idle Rx idle status 1'b0:Busy 1'b1:idle
2	RW	0x1	tx_idle Tx idle status 1'b0:Busy 1'b1:idle
1	RW	0x1	fs_idle Fs idle status 1'b0:Busy 1'b1:idle
0	RW	0x1	clk_idle Clk idle status 1'b0:Busy 1'b1:idle

SAI_VERSION

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x24013506	sai_vertion SAI version

23.5 Interface Description

The following table shows the SAI interface description.

Table 23-1 SAI0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai0_mclk	I/O	GPIO0_A2	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[11:8]=1

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Module Pin	Direction	Pad Name	IOMUX Setting
sai0_sclk	I/O	GPIO0_A1	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[7:4]=1
sai0_lrck	I/O	GPIO0_A0	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[3:0]=1
sai0_sdo	O	GPIO0_A3	GPIO0_IOC_GPIO0A_IOMUX_SEL_0[15:12]=1
sai0_sdi0	I	GPIO0_A4	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[3:0]=1
sai0_sdi1	I	GPIO0_A5	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[7:4]=1
sai0_sdi2	I	GPIO0_A6	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[11:8]=1
sai0_sdi3	I	GPIO0_A7	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[15:12]=1

Table 23-2 SAI0 Rm Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai0_mclk	I/O	RM_IO	
sai0_sclk	I/O	RM_IO	
sai0_lrck	I/O	RM_IO	
sai0_sdo	O	RM_IO	
sai0_sdi0	I	RM_IO	
sai0_sdi1	I	RM_IO	
sai0_sdi2	I	RM_IO	
sai0_sdi3	I	RM_IO	

Table 23-3 SAI1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai1_mclk	I/O	GPIO0_B0	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[3:0]=1
sai1_sclk	I/O	GPIO0_B1	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[7:4]=1
sai1_lrck	I/O	GPIO0_B2	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[11:8]=1
sai1_sdo0	O	GPIO0_B4	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[3:0]=1
sai1_sdo1	O	GPIO0_B5	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[7:4]=1
sai1_sdo2	O	GPIO0_B6	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[11:8]=1
sai1_sdo3	O	GPIO0_B7	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[15:12]=1
sai1_sdi	I	GPIO0_B3	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[15:12]=1

Table 23-4 SAI1 Rm Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai1_mclk	I/O	RM_IO	
sai1_sclk	I/O	RM_IO	
sai1_lrck	I/O	RM_IO	
sai1_sdo0	O	RM_IO	
sai1_sdo1	O	RM_IO	
sai1_sdo2	O	RM_IO	
sai1_sdo3	O	RM_IO	
sai1_sdi	I	RM_IO	

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Table 23-5 SAI2 M0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai2_mclk	I/O	GPIO3_B6	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[11:8]=1
sai2_sclk	I/O	GPIO3_A7	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[15:12]=1
sai2_lrck	I/O	GPIO3_B1	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[7:4]=1
sai2_sdo	O	GPIO3_B0	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[3:0]=1
sai2_sdi	I	GPIO3_A6	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[11:8]=1

Table 23-6 SAI2 M1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai2_mclk	I/O	GPIO1_C1	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[7:4]=6
sai2_sclk	I/O	GPIO1_B2	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[11:8]=6
sai2_lrck	I/O	GPIO1_B3	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[15:12]=6
sai2_sdo	O	GPIO1_C3	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[15:12]=6
sai2_sdi	I	GPIO1_C2	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[11:8]=6

Table 23-7 SAI3 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai3_mclk	I/O	GPIO2_C0	GPIO2_IOC_GPIO2C_IOMUX_SEL_0[3:0]=3
sai3_sclk	I/O	GPIO2_B4	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[3:0]=3
sai3_lrck	I/O	GPIO2_B5	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[7:4]=3
sai3_sdo	O	GPIO2_B7	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[15:12]=3
sai3_sdi	I	GPIO2_B6	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[11:8]=3

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

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23.6 Application Notes

23.6.1 Software Application Notes

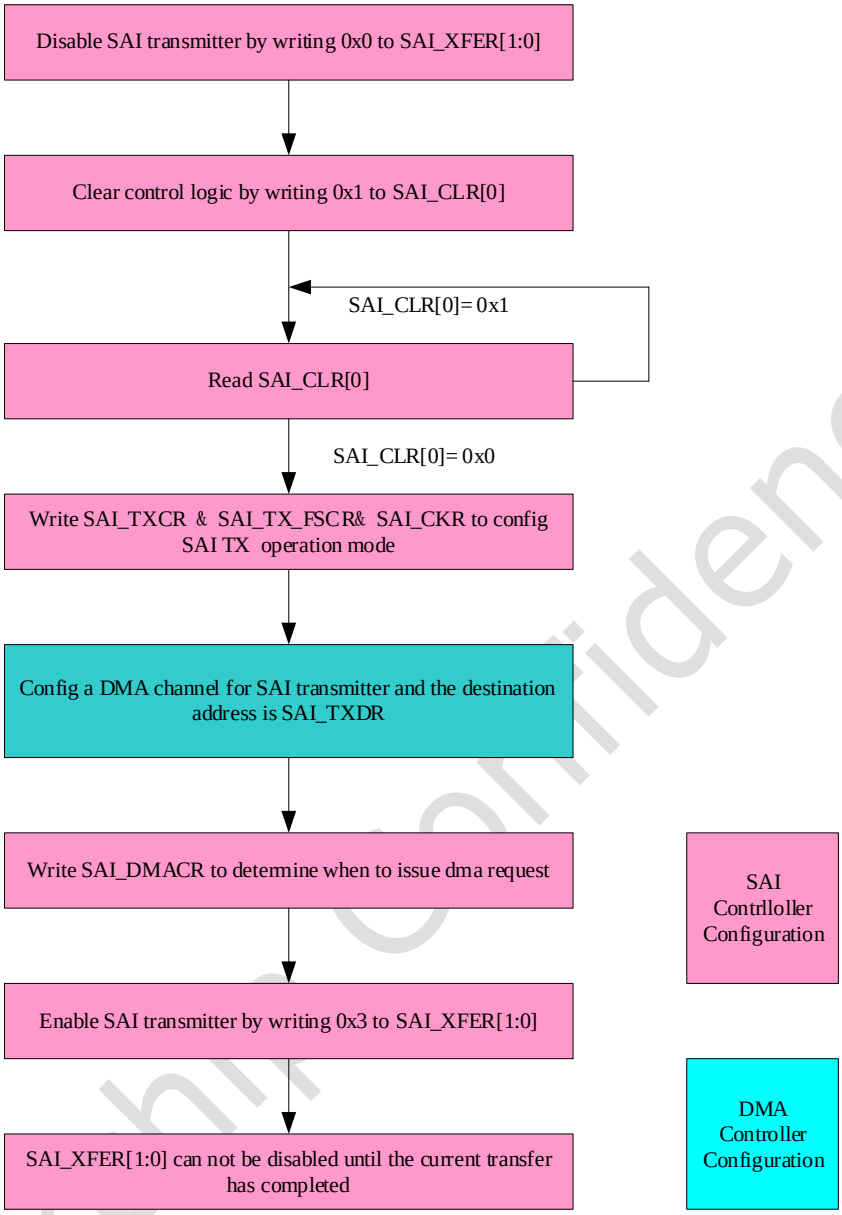

Fig. 23-11 SAI controller transmit operation flow chart

Note: User should clear TX/RX logical by CLR[0]/CLR[1] and wait clear operation done before configure the other registers.

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Chapter 24 Pulse Density Modulation (PDM)

24.1 Overview

The Pulse Density Modulation (PDM) is a PDM interface controller that supports mono PDM format. It integrates a clock generator driving the PDM microphone and embeds filters which decimate the incoming bit stream to obtain most common audio rates.
PDM supports the following features:

- Support one internal 32-bit wide and 128-location deep FIFOs for receiving audio data
- Support receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of receive FIFO full interrupt
- Support combined interrupt output
- Support AHB bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support PDM master receive mode
- Support 4 paths. Each path is composed of two digital microphone channels, the PDM can be used with four stereo or eight mono microphones. Each path is enabled or disabled independently
- Support 16 ~24 bit sample resolution
- Support sample rate:
  8KHz, 16KHz, 32KHz, 64KHz, 128KHz, 11.025KHz, 22.05KHz, 44.1KHz, 88.2KHz, 176.4KHz, 12KHz, 24KHz, 48KHz, 96KHz, 192KHz
- Support two 16-bit audio data store together in one 32-bit wide location
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support programmable data sampling sensibility (rising or falling edge)
- Support mute function
- Support gain control
- Support 2.4MHz pdm clock

24.2 Block Diagram

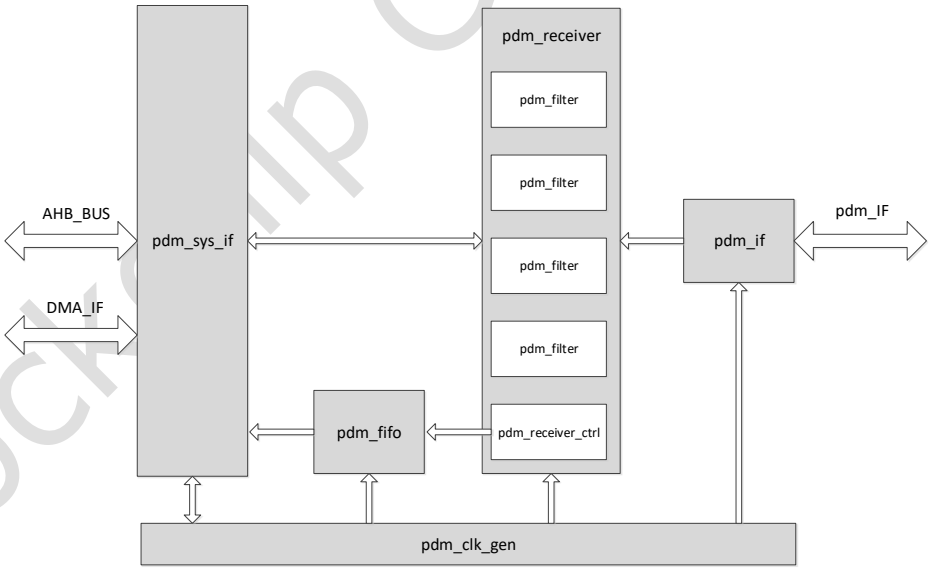

Fig. 24-1 PDM Block Diagram

System Interface
The system interface implements the APB slave operation. It contains not only control registers of receiver inside but also interrupt and DMA handshaking interface.
Receiver
The receiver can act as a decimation filter of PDM. And export PCM format data.
Receive FIFO
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 128.
PDM interface
The PDM interface implements PDM bit streams receive operation.

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24.3 Function Description

24.3.1 AHB Interface

There is an AHB slave interface in PDM. It is responsible for accessing registers and internal memories.

24.3.2 PDM Interface

The PDM interface is a 5-wire interface. The PDM module can support up to four external stereo and eight digital microphones.

The following figures show two cases of use of the PDM, but all configurations are possible with stereo and mono digital microphones.

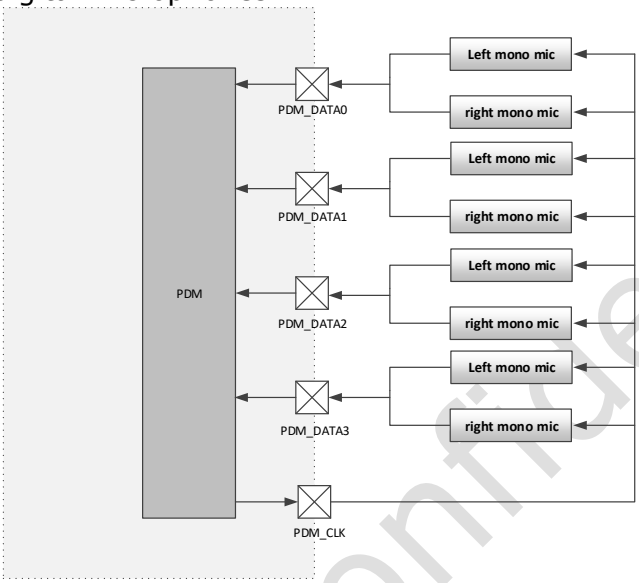

Fig. 24-2 PDM with Eight Mono MIC

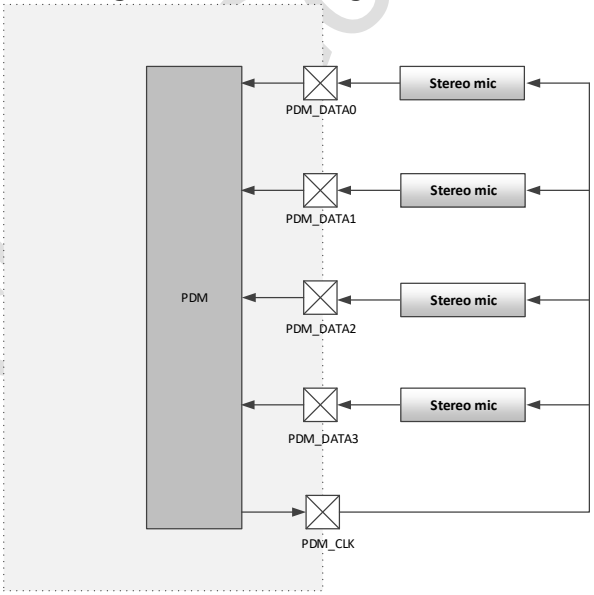

Fig. 24-3 PDM with Four Stereo MIC

The PDM interface consists of a serial-data shift clock output (PDM_CLK) and a serial data input (PDM_DATA). The clock is fanned out to both digital mics, and both digital mics' data (left channel and right channel) outputs share a single signal line. To share a single line, the digital mics tristate their output during one phase of the clock (high or low part of cycle, depending on how they are configured via their L/R input).

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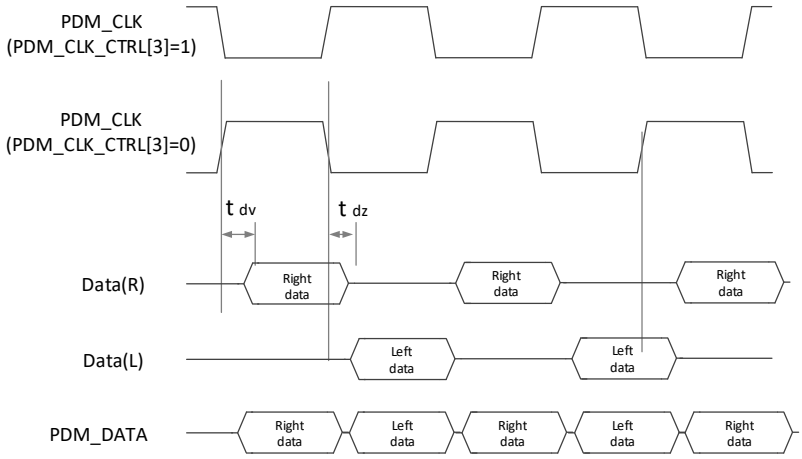

Fig. 24-4 PDM interface diagram with external MIC

24.3.3 Digital Filter

The external PDM generates a PDM stream of bits and transfers it in one period or one half-period of the clock provided by the PDM. The aim of the PDM is to process data from the PDM interface, decimate and filter the data, and store the processed data in the FIFO.
The four paths are identical. Each path is composed of a left and a right channel. The PDM interface delivers eight parallel data of 1bit. Each bit goes to a filter. The aim of the filter is to limit the noise and export PCM format audio data.

24.3.4 Clock Configuration

MCLK is the source clock signal. PDM_CLK is the output clocks generated in the PDM and is fed to the external microphones. They are also the internal clock of the external microphones. User must take care about the value of PDM_CLK when selecting the source clock (MCLK).

Table 24-1 Relation between PDM_CLK and sample rate

PDM_CLK	Sample rate
3.072MHz	12KHz,24KHz,48KHz,96KHz,192KHz
2.8224MHz	11.025KHz,22.05KHz,44.1KHz,88.2KHz,176.4KHz
2.048MHz	8KHz,16KHz,32KHz,64KHz,128KHz

MCLK/PDM_CLK is more than 10;

24.4 Register Description

24.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

24.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PDM_SYSCONFIG	0x0000	W	0x00000002	PDM System Configure Register
PDM_CTRL	0x0004	W	0x001C8797	PDM Control Register
PDM_FILTER_CTRL	0x0008	W	0x00000000	PDM Filter Control Register
PDM_FIFO_CTRL	0x000C	W	0x0003E000	PDM FIFO Control Register
PDM_DATA_VALID	0x0010	W	0x00000000	PDM Path Data Valid Register
PDM_RXFIFO_DATA_REG	0x0014	W	0x00000000	PDM Receive FIFO Data Register
PDM_DATA0R	0x0018	W	0x00000000	PDM Path 0 Right Channel Data Register
PDM_DATA0L	0x001C	W	0x00000000	PDM Path 0 Left Channel Data Register
PDM_DATA1R	0x0020	W	0x00000000	PDM Path 1 Right Channel Data Register
PDM_DATA1L	0x0024	W	0x00000000	PDM Path 1 Left Channel Data Register

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Name	Offset	Size	Reset Value	Description
PDM_DATA2R	0x0028	W	0x00000000	PDM Path 2 Right Channel Data Register
PDM_DATA2L	0x002C	W	0x00000000	PDM Path 2 Left Channel Data Register
PDM_DATA3R	0x0030	W	0x00000000	PDM Path 3 Right Channel Data Register
PDM_DATA3L	0x0034	W	0x00000000	PDM Path 3 Left Channel Data Register
PDM_VERSION	0x0038	W	0x23113506	PDM Version Register
PDM_GAIN_CTRL	0x003C	W	0x00000000	PDM Gain Control Register
PDM_INCR_RXDR	0x0400	W	0x00000000	Increment Address Receive FIFO Data Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

24.4.3 Detail Registers Description

PDM_SYSCONFIG

Address: Operational Base(0xFF380000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:5	RW	0x00	mute mute[0]: ch0 mute mute[1]: ch1 mute mute[2]: ch2 mute mute[3]: ch3 mute mute[4]: ch4 mute mute[5]: ch5 mute mute[6]: ch6 mute mute[7]: ch7 mute
4	RW	0x0	filter_gate_en Filter gate enable If some filters not work, the filter and its corresponding memory clock will be gated if filter_gate_en is 1'b1, otherwise the clock will be still active.
3	RW	0x0	num_start Software configuration enable bit. This bit only vaild data when num_start = 1'b1.
2	RW	0x0	rx_start RX transfer start bit 1'b0: Stop RX transfer 1'b1: Start RX transfer
1	RW	0x1	mem_gate_en 1: Memory interface clock auto gating enable 0: Memory interface clock auto gating disable
0	RW	0x0	rx_clr PDM RX logic clear This is a self-cleared bit. High active. Write 1'b1: Clear RX logic Write 1'b0: No action Read 1'b1: Clear ongoing Read 1'b0: Clear done

PDM_CTRL

Address: Operational Base(0xFF380000) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:27	RW	0x0	path1_ch_sel Left and right channel data sel If path_mode_select = 2'b00 3'b000: path3 left (R ch) and path2 left (L ch) 3'b001: path3 right (R ch) and path2 left (L ch) 3'b010: path3 left (R ch) and path2 right (L ch) 3'b011: path3 right (R ch) and path2 right (L ch) 3'b100: path2 left (R ch) and path3 left (L ch) 3'b101: path2 right (R ch) and path3 left (L ch) 3'b110: path2 left (R ch) and path3 right (L ch) 3'b111: path2 right (R ch) and path3 right (L ch) If path_mode_select = 2'b01 3'b000: path3 left (R ch) and path1 left (L ch) 3'b001: path3 right (R ch) and path1 left (L ch) 3'b010: path3 left (R ch) and path1 right (L ch) 3'b011: path3 right (R ch) and path1 right (L ch) 3'b100: path1 left (R ch) and path3 left (L ch) 3'b101: path1 right (R ch) and path3 left (L ch) 3'b110: path1 left (R ch) and path3 right (L ch) 3'b111: path1 right (R ch) and path3 right (L ch) If path_mode_select = 2'b10 3'b000: path2 left (R ch) and path1 left (L ch) 3'b001: path2 right (R ch) and path1 left (L ch) 3'b010: path2 left (R ch) and path1 right (L ch) 3'b011: path2 right (R ch) and path1 right (L ch) 3'b100: path1 left (R ch) and path2 left (L ch) 3'b101: path1 right (R ch) and path2 left (L ch) 3'b110: path1 left (R ch) and path2 right (L ch) 3'b111: path1 right (R ch) and path2 right (L ch)

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	path0_ch_sel Left and right channel data sel If path_mode_select = 2'b00 3'b000: path1 left (R ch) and path0 left (L ch) 3'b001: path1 right (R ch) and path0 left (L ch) 3'b010: path1 left (R ch) and path0 right (L ch) 3'b011: path1 right (R ch) and path0 right (L ch) 3'b100: path0 left (R ch) and path1 left (L ch) 3'b101: path0 right (R ch) and path1 left (L ch) 3'b110: path0 left (R ch) and path1 right (L ch) 3'b111: path0 right (R ch) and path1 right (L ch) If path_mode_select = 2'b01 3'b000: path2 left (R ch) and path0 left (L ch) 3'b001: path2 right (R ch) and path0 left (L ch) 3'b010: path2 left (R ch) and path0 right (L ch) 3'b011: path2 right (R ch) and path0 right (L ch) 3'b100: path0 left (R ch) and path2 left (L ch) 3'b101: path0 right (R ch) and path2 left (L ch) 3'b110: path0 left (R ch) and path2 right (L ch) 3'b111: path0 right (R ch) and path2 right (L ch) If path_mode_select = 2'b10 3'b000: path3 left (R ch) and path0 left (L ch) 3'b001: path3 right (R ch) and path0 left (L ch) 3'b010: path3 left (R ch) and path0 right (L ch) 3'b011: path3 right (R ch) and path0 right (L ch) 3'b100: path0 left (R ch) and path3 left (L ch) 3'b101: path0 right (R ch) and path3 left (L ch) 3'b110: path0 left (R ch) and path3 right (L ch) 3'b111: path0 right (R ch) and path3 right (L ch)
23:22	RW	0x0	path_mode_select path Select 2'b00: Path0 data and path1 data (path2 data and path3 data) 2'b01: Path0 data and path2 data (path1 data and path3 data) 2'b10: Path0 data and path3 data (path1 data and path2 data)
21	RW	0x0	split_en Split enable 1'b1: Enable 1'b0: Disable
20:19	RW	0x3	rx_path_select3 RX Path Select 2'b00: Path3 data from PDM data0 2'b01: Path3 data from PDM data1 2'b10: Path3 data from PDM data2 2'b11: Path3 data from PDM data3
18:17	RW	0x2	rx_path_select2 RX Path Select 2'b00: Path2 data from PDM data0 2'b01: Path2 data from PDM data1 2'b10: Path2 data from PDM data2 2'b11: Path2 data from PDM data3

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Bit	Attr	Reset Value	Description
16:15	RW	0x1	rx_path_select1 RX Path Select 2'b00: Path1 data from PDM data0 2'b01: Path1 data from PDM data1 2'b10: Path1 data from PDM data2 2'b11: Path1 data from PDM data3
14:13	RW	0x0	rx_path_select0 RX Path Select 2'b00: Path0 data from PDM data0 2'b01: Path0 data from PDM data1 2'b10: Path0 data from PDM data2 2'b11: Path0 data from PDM data3
12	RW	0x0	pdm_ch_ex Left and right channel data exchange 1'b0: Not inverted, if mono_path_en, the output path is the Left path. 1'b1: Inverted, if mono_path_en, the output path is the Right path.
11	RW	0x0	sjm_sel Store justified mode This bit can be written only when SYSCONFIG[2] is 0. 16bit~31bit DATA stored in 32 bits width FIFO. If VDW select 16bit data, this bit is valid only when HWT select 1. Because if HWT is 0, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 1'b0: Right justified 1'b1: Left justified
10	RW	0x1	path3_en Path 3 enable 1'b1: Enable 1'b0: Disable
9	RW	0x1	path2_en Path 2 enable 1'b1: Enable 1'b0: Disable
8	RW	0x1	path1_en Path 1 enable 1'b1: Enable 1'b0: Disable
7	RW	0x1	path0_en Path 0 enable 1'b1: Enable 1'b0: Disable
6	RW	0x0	hwt_en Halfword word transform Only valid when VDW select 16bit data. 1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid.
5	RW	0x0	mono_path_enable Mono path enable bit. If mono path enable, path0/path1/path2/path3 only one path enable, and the right or left path depended on the lr_ch_ex reg. If data_vld_width cfg right/left data only 16bit, the data write to memory is combined by two data, {L1, L0} or {R1, R0}.

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Bit	Attr	Reset Value	Description
4:0	RW	0x17	data_vld_width Can be written only when SYSCONFIG[2] is 0. Valid Data width 0~14: Reserved 15: 16bit 16: 17bit 17: 18bit 18: 19bit ..... n: (n+1)bit 23: 24bit

PDM_FILTER_CTRL

Address: Operational Base(0xFF380000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:21	RW	0x0	hpf_cfg High-pass filter configure 4'd0: 0.234Hz 4'd1: 0.468Hz 4'd2: 0.937Hz 4'd3: 1.875Hz 4'd4: 3.75Hz 4'd5: 7.5Hz 4'd6: 15Hz 4'd7: 30Hz 4'd8: 60Hz 4'd9: 122Hz 4'd10: 251Hz 4'd11: 528Hz 4'd12: 1183Hz 4'd13: 3152Hz 4'd14: 23999Hz 4'd15: high frequency
20	RW	0x0	hpf_ctrll High-pass filter enable for left channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
19	RW	0x0	hpf_ctrlr High-pass filter enable for right channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
18	RW	0x0	fir_com_bps FIR compensate filter bypass 1'b0: Not bypass 1'b1: Bypass
17	RW	0x0	sig_scale_mode Signal scale mode select 1'b0: CIC outputs the normal latitude. 1'b1: Scale the CIC outputs to half of the normal latitude and scale 2 times after hpf-filter.
16:10	RW	0x00	cic_scale CIC scale bits
9:1	RW	0x000	cic_value CIC filter extract value

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Bit	Attr	Reset Value	Description
0	RW	0x0	filter_en Contrl hb2 filter en 1'b0: Off 1'b1:On

PDM_FIFO_CTRL

Address: Operational Base(0xFF380000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RO	0x00	rfl Receive FIFO level Contains the number of valid data entries in the receive FIFO.
19:13	RW	0x1f	rdl Receive data level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
12	RW	0x0	rde Receive DMA enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
11	RO	0x0	rxoi RX overflow interrupt 1'b0: Inactive 1'b1: Active
10	RO	0x0	rxfi RX full interrupt 1'b0: Inactive 1'b1: Active
9	RW	0x0	rxoic RX overflow interrupt clear (high active, auto clear).
8:2	RW	0x00	rft Receive FIFO threshold When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO threshold interrupt is triggered.
1	RW	0x0	rxoie RX overflow interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	rxftie RX full threshold interrupt enable 1'b0: Disable 1'b1: Enable

PDM_DATA_VALID

Address: Operational Base(0xFF380000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RC	0x0	path0_vld 1'b0: DATA0R_REG, DATA0L_REG value is invalid. 1'b1: DATA0R_REG, DATA0L_REG value is valid.

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Bit	Attr	Reset Value	Description
2	RC	0x0	path1_vld 1'b0: DATA1R_REG, DATA1L_REG value is invalid. 1'b1: DAT1R_REG, DATA1L_REG value is valid.
1	RC	0x0	path2_vld 1'b0: DATA2R_REG, DATA2L_REG value is invalid. 1'b1: DATA2R_REG, DATA2L_REG value is valid.
0	RC	0x0	path3_vld 1'b0: DATA3R_REG, DATA3L_REG value is invalid. 1'b1: DATA3R_REG, DATA3L_REG value is valid.

PDM_RXFIFO_DATA_REG

Address: Operational Base(0xFF380000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdr Receive FIFO shadow register When the register is read, data in the receive FIFO is accessed.

PDM_DATA0R

Address: Operational Base(0xFF380000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0r Data of the path 0 right channel

PDM_DATA0L

Address: Operational Base(0xFF380000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0l Data of the path 0 left channel

PDM_DATA1R

Address: Operational Base(0xFF380000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1r Data of the path 1 right channel

PDM_DATA1L

Address: Operational Base(0xFF380000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1l Data of the path 1 left channel

PDM_DATA2R

Address: Operational Base(0xFF380000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2r Data of the path 2 right channel

PDM_DATA2L

Address: Operational Base(0xFF380000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2l Data of the path 2 left channel

PDM_DATA3R

Address: Operational Base(0xFF380000) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3r Data of the path 3 right channel

PDM_DATA3L

Address: Operational Base(0xFF380000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3l Data of the path 3 left channel

PDM_VERSION

Address: Operational Base(0xFF380000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x23113506	ver PDM version

PDM_GAIN_CTRL

Address: Operational Base(0xFF380000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	gain_ctrl 0: -65.625dB 1: -65.25dB .... 175: 0dB 255: 30dB step:0.375dB

PDM_INCR_RXDR

Address: Operational Base(0xFF380000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	receive_fifo_data FIFO data can be read from these registers. This register is used when the access address is increment.

24.5 Interface Description

The following table shows the PDM interface description.

Table 24-2 PDM Interface Description

Module Pin	Direction	Rockchip matrix IO	IOMUX Setting
O_pdm_clk(0)	O	RM_IO	
O_pdm_clk(1)	O	RM_IO	
I_pdm_data0	I	RM_IO	
I_pdm_data1	I	RM_IO	
I_pdm_data2	I	RM_IO	
I_pdm_data3	I	RM_IO	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

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24.6 Application Notes

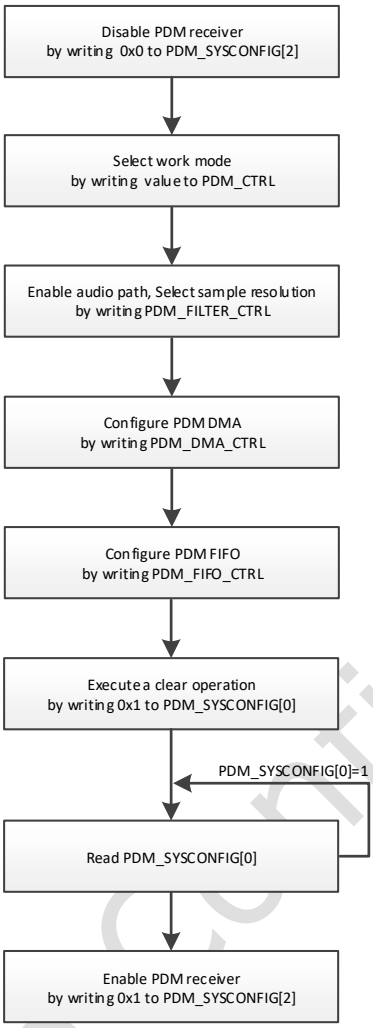

Fig. 24-5 PDM operation flow

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Chapter 25 SPDIF TX

25.1 Overview

The SPDIF transmitter is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to carry stereophonic programmes, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible.
When used for other purposes, the interface is primarily intended to carry audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to carry data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
In all cases, the clock references and auxiliary information are transmitted along with the programme. MCLK is the operation clock of SPDIF transmitter.

Table 25-1 Maximum Frequency of MCLK for the SPDIF Transmitter

SPDIF transmitter	Maximum frequency of MCLK
SPDIF	100MHz

Each SPDIF transmitter supports following features.

- Support one internal 32-bit wide and 32-location deep sample data buffer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support AHB or APB bus interface
- Support biphase format stereo audio data output
- Support DMA handshake interface and configurable DMA water level
- Support sample data buffer empty and block terminate interrupt
- Support combine interrupt output
- Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
- Support 48, 44.1, 32kHz sample rate
- Support MCLK frequencies of 12.288Mhz, 8.192Mhz and 11.2896MHz
- Support 16, 20, 24 bits audio data transfer
- Support frame transmission frequency, fixed to 128 times of audio data sampling rate

25.2 Block Diagram

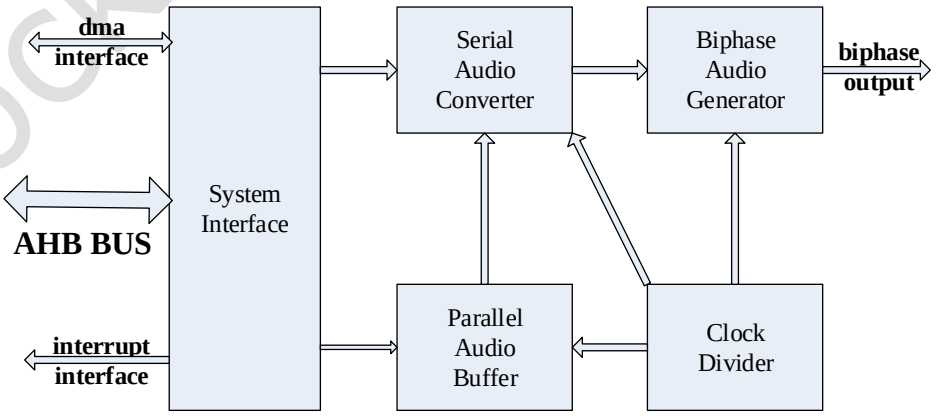

Fig.25-1 SPDIF transmitter Block Diagram

The SPDIF transmitter is composed of following module.

System Interface

The system interface implements the AHB slave operation. It contains not only control

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registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

Clock Divider

The clock divider implements clock generation function. It divides the source clock MCLK to generate the working clock used for the digital audio data transformation and transmission.

Parallel Audio Buffer

The parallel audio buffer stores the audio data to be transmitted. The size of the FIFO is 32bits x 32.

Serial Audio Converter

The serial audio converter converts the parallel audio data from the parallel audio buffer to the serial audio data.

Biphase Audio Generator

The biphase audio generator reads serial audio data from the serial audio converter and generates biphase audio data based on IEC-60958 standard.

25.3 Function Description

25.3.1 Frame Format

A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of transmission of frames corresponds exactly to the source sampling frequency.
In the 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. The first sub-frame (left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information.
The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

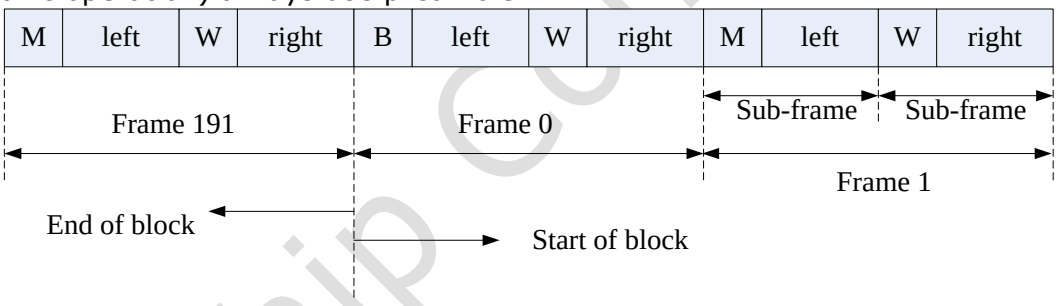

Fig.25-2 SPDIF Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

25.3.2 Sub-frame Format

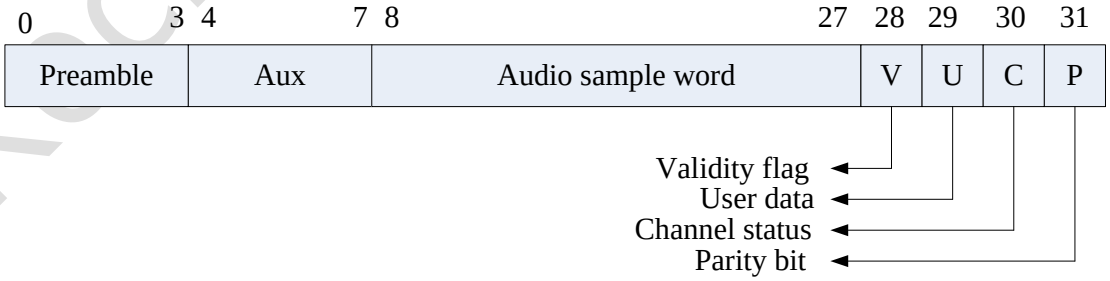

Fig.25-3 SPDIF Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8. Time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to

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7 are designated auxiliary sample bits.
If the source provides fewer bits than the interface allows (either 24 or 20), the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

25.3.3 Channel Coding

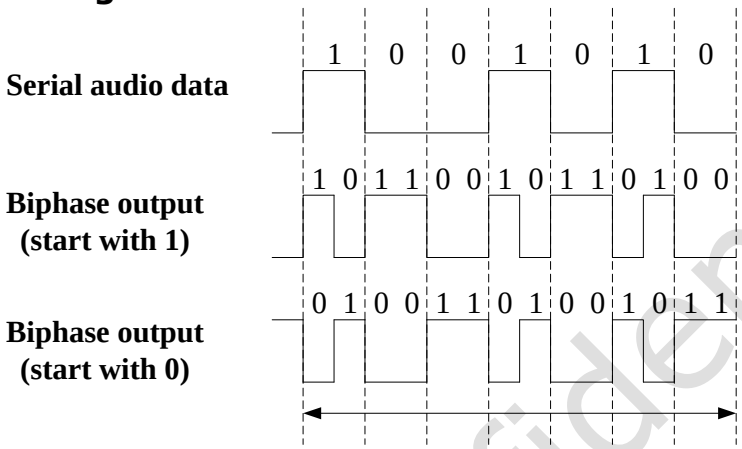

Fig.25-4 SPDIF Channel Coding

To minimize the direct current component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.
Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'. However, it is different from the first if the bit is logical '1'.

25.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.
To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.
A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

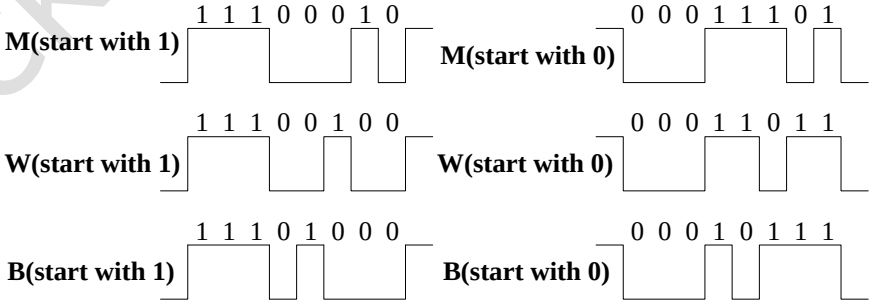

Fig.25-5 SPDIF Preamble

Like biphase code, these preambles are DC free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

25.4 Register Description

25.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as

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follows.

Operational Base

Name	Base Address
SPDIF_TX SECURE BASE ADDRESS	0x40900000
SPDIF_TX NO-SECURE BASE ADDRESS	0x50900000

25.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPDIF_TX_CFGR	0x0000	W	0x00000000	Configuration Register
SPDIF_TX_SDBLR	0x0004	W	0x00000000	Sample Date Buffer Level Register
SPDIF_TX_DMACR	0x0008	W	0x00000000	DMA Control Register
SPDIF_TX_INTCR	0x000C	W	0x00000000	Interrupt Control Register
SPDIF_TX_INTSR	0x0010	W	0x00000000	Interrupt Status Register
SPDIF_TX_XFER	0x0018	W	0x00000000	Transfer Start Register
SPDIF_TX_SMPDR	0x0020	W	0x00000000	Sample Data Register
SPDIF_TX_VLDFRn	0x0060	W	0x00000000	Validity Flag Register n
SPDIF_TX_USRDRn	0x0090	W	0x00000000	User Data Register n
SPDIF_TX_CHNSRn	0x00C0	W	0x00000000	Channel Status Register n
SPDIF_TX_BURTSINFO	0x00D0	W	0x00000000	This define the channel burst info when the channel conveys non-linear PCM.
SPDIF_TX_REPETTION	0x0104	W	0x00000000	This register provides the repetition of the bitstream when channel conveys non-linear PCM. In the design, it is define the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design.
SPDIF_TX_BURTSINFO_SHD	0x0108	W	0x00000000	This define the channel burst info when the channel conveys non-linear PCM.
SPDIF_TX_REPETTION_SHD	0x010C	W	0x00000000	This register provides the repetition of the bitstream when channel conveys non-linear PCM.
SPDIF_TX_USRDR_SHDn	0x0190	W	0x00000000	Shadow User Data Register n

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

25.4.3 Detail Registers Description

SPDIF_TX_CFGR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	MCD Fmclk/Fsdo This parameter can be calculated by Fmclk/(Fs*128). Fs is the sample frequency be wanted
15:10	RO	0x00	reserved
9	RW	0x0	PRECHANGE 0: No linear PCM length 1: 192 block
8	RW	0x0	PCMTYPE 0: linear PCM 1: non-linear PCM

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Bit	Attr	Reset Value	Description
7	WO	0x0	CLR Write 1 to clear MCLK domain logic. Read returns zero.
6	RW	0x0	CSE 0: Disable 1: Enable The bit should be set to 1 when the channel conveys non-linear PCM
5	RW	0x0	UDE 0: Disable 1: Enable
4	RW	0x0	VFE 0: Disable 1: Enable
3	RW	0x0	ADJ 0: Right justified 1: Left justified
2	RW	0x0	HWT 0: Disable 1: Enable It is valid only when the valid data width is 16bit.
1:0	RW	0x0	VDW 00: 16bit 01: 20bit 10: 24bit 11: reserved The valid data width is 16bit only for non-linear PCM.

SPDIF_TX_SDBLR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	SDBLR Contains the number of valid data entries in the sample data buffer.

SPDIF_TX_DMACR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	TDE 0: Transmit DMA disabled 1: Transmit DMA enabled
4:0	RW	0x00	TDL This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the Sample Date Buffer is equal to or below this field value.

SPDIF_TX_INTCR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	W1C	0x0	UDTIC Write '1' to clear the user data interrupt.

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Bit	Attr	Reset Value	Description
16	W1C	0x0	BTTIC Write '1' to clear the interrupt.
15:10	RO	0x00	reserved
9:5	RW	0x00	SDBT Sample Date Buffer Threshold for empty interrupt.
4	RW	0x0	SDBEIE 0: Disable 1: Enable
3	RW	0x0	BTTIE When enabled, an interrupt will be asserted when the block transfer is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM. 0: Disable 1: Enable
2	RW	0x0	UDTIE 0: Disable 1: Enable If enabled, an interrupt will be asserted when the content of the user data register is fed into the corresponding shadow register.
1:0	RO	0x0	reserved

SPDIF_TX_INTSR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SDBEIS 0: Inactive 1: Active
3	RW	0x0	BTTIS 0: Inactive 1: Active
2	RW	0x0	UDTIS 0: Inactive 1: Active
1:0	RO	0x0	reserved

SPDIF_TX_XFER

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	XFER Transfer Start Register

SPDIF_TX_SMPDR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SMPDR Sample Data Register

SPDIF_TX_VLDFRn

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VLDFR_SUB_1 Validity Flag Register 0

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	VLDFR_SUB_0 Validity Flag for Subframe 0

SPDIF_TX_USRDRn

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	USR_SUB_1 User Data Bit for Subframe 1
15:0	RW	0x0000	USR_SUB_0 User Data Bit for Subframe 0

SPDIF_TX_CHNSRn

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CHNSR_SUB_1 Channel Status Bit for Subframe 1
15:0	RW	0x0000	CHNSR_SUB_0 Channel Status Bit for Subframe 0

SPDIF_TX_BURTSINFO

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PD Preamble Pd for non-linear PCM, indicating the length of burst payload in unit of bytes or bits.
15:13	RW	0x0	BSNUM This field indicates the bitstream number. Usually the birstream number is 0.
12:8	RW	0x00	DATAINFO This field gives the data-type-dependent info.
7	RW	0x0	ERRFLAG 0: Indicates a valid burst-payload 1: Indicates that the burst-payload may contain errors

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	DATATYPE 0000000: null data 0000001: AC-3 data 0000011: Pause data 0000100: MPEG-1 layer 1 data 0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 0000110: MPEG-2 data with extension 0000111: MPEG-2 AAC 0001000: MPEG-2, layer-1 low sampling frequency 0001001: MPEG-2, layer-2 low sampling frequency 0001010: MPEG-2, layer-3 low sampling frequency 0001011: DTS type I 0001100: DTS type II 0001101: DTS type III 0001110: ATRAC 0001111: ATRAC 2/3 0010000: ATRAC-X 0010001: DTS type IV 0010010: WMA professional type I 0110010: WMA professional type II 1010010: WMA professional type III 1110010: WMA professional type IV 0010011: MPEG-2 AAC low sampling frequency 0110011: MPEG-2 AAC low sampling frequency 1010011: MPEG-2 AAC low sampling frequency 1110011: MPEG-2 AAC low sampling frequency 0010100: MPEG-4 AAC 0110100: MPEG-4 AAC 1010100: MPEG-4 AAC 1110100: MPEG-4 AAC 0010101: Enhanced AC-3 0010110: MAT others: reserved

SPDIF_TX_REPETTION

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	REPETTION This define the repetition period when the channel conveys non-linear PCM.

SPDIF_TX_BURTSINFO_SHD

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	PD Preamble Pd for non-linear PCM, indicating the length of burst payload in unit of bytes or bits.
15:13	RO	0x0	BSNUM This field indicates the bitstream number. Usually the birstream number is 0.
12:8	RO	0x00	DATAINFO This field gives the data-type-dependent info
7	RO	0x0	ERRFLAG 0: Indicates a valid burst-payload 1: Indicates that the burst-payload may contain errors

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Bit	Attr	Reset Value	Description
6:0	RO	0x00	DATATYPE 0000000: null data 0000001: AC-3 data 0000011: Pause data 0000100: MPEG-1 layer 1 data 0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 0000110: MPEG-2 data with extension 0000111: MPEG-2 AAC 0001000: MPEG-2, layer-1 low sampling frequency 0001001: MPEG-2, layer-2 low sampling frequency 0001010: MPEG-2, layer-3 low sampling frequency 0001011: DTS type I 0001100: DTS type II 0001101: DTS type III 0001110: ATRAC 0001111: ATRAC 2/3 0010000: ATRAC-X 0010001: DTS type IV 0010010: WMA professional type I 0110010: WMA professional type II 1010010: WMA professional type III 1110010: WMA professional type IV 0010011: MPEG-2 AAC low sampling frequency 0110011: MPEG-2 AAC low sampling frequency 1010011: MPEG-2 AAC low sampling frequency 1110011: MPEG-2 AAC low sampling frequency 0010100: MPEG-4 AAC 0110100: MPEG-4 AAC 1010100: MPEG-4 AAC 1110100: MPEG-4 AAC 0010101: Enhanced AC-3 0010110: MAT others: reserved

SPDIF_TX_REPETTION_SHD

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	REPETTION This register provides the repetition of the bitstream when channel conveys non-linear PCM. In the design, it is define the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design.

SPDIF_TX_USRDR_SHDn

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	USR_SUB_1 User Data Bit for Subframe 1
15:0	RO	0x0000	USR_SUB_0 User Data Bit for Subframe 0

25.5 Interface Description

SPDIF are used to communicate with audio equipment outside this chip. Following table

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shows the interface of SPDIF.

Table 25-2 SPDIF TX Interface Description

Module Pin	Direction	Rockchip matrix IO	IOMUX Setting
spdif_sdo	O	RM_IO	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

25.6 Application Notes

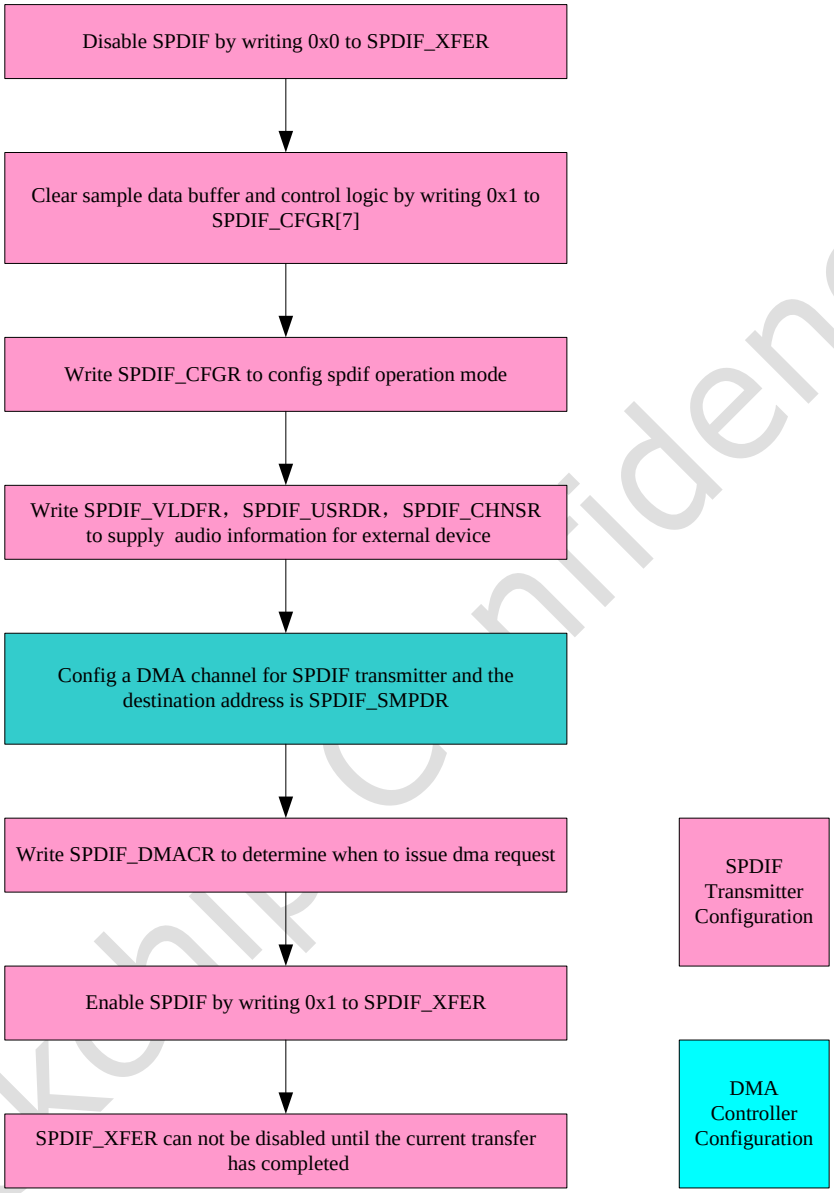

Fig.25-6 SPDIF transmitter operation flow chart

The above figure shows the operation flow of SPDIF operation. Note that the configuration register can be written only when the transfer is stopped.

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Chapter 26 SPDIF RX

26.1 Overview

The SPDIF receiver is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to receive monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to receive signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to receive stereophonic programmes, with a resolution of up to 24 bits per sample.
When used for other purposes, the interface is primarily intended to receive audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to receive data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
It supports following features.

- Support AHB bus interface
- Support one internal 30-bit wide and 32-location deep FIFO for receiving audio data
- Support combined interrupt output
- Support DMA handshaking interface and configurable DMA water level
- Support linear PCM(IEC60958) and non-linear PCM(IEC61937)
- Support 16~24 bits audio sample length for liner PCM application
- Support 16 bits audio sample length for non-liner PCM application
- Support up to 192kHz sample rate with the corresponding reference clock equal to 384KHz*64*2*10, that is 245.76MHz
- Support the frequency of reference clock is at least 10 times the frequency of the biphase encoding clock, but not more than 256 times
- Support recovering clock and audio data from input bitstream

26.2 Block Diagram

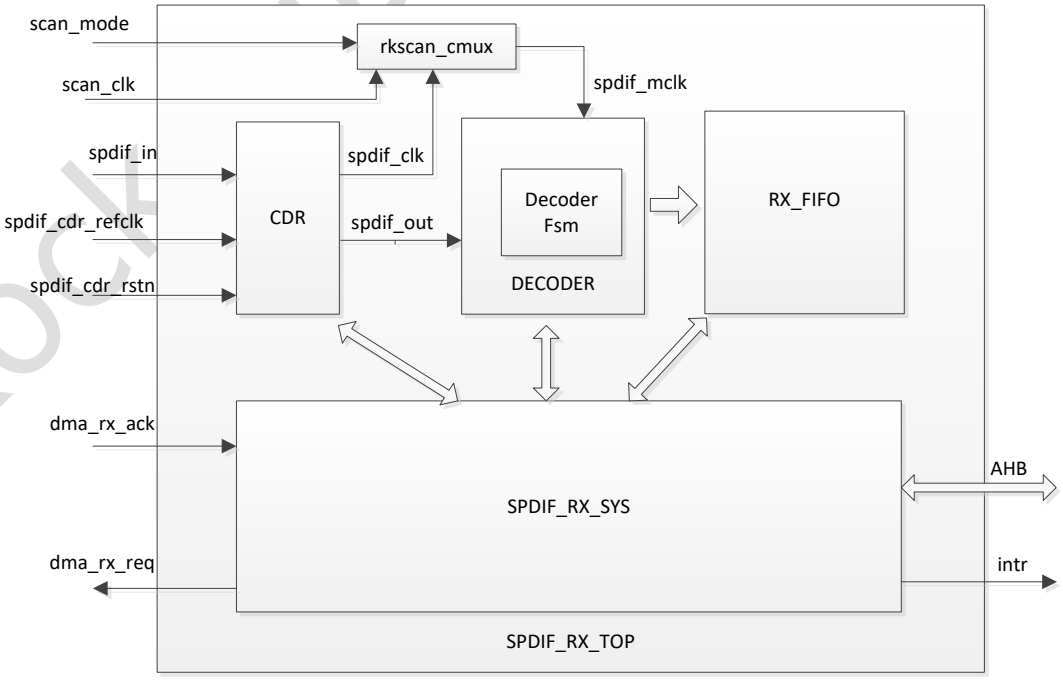

Fig.26-1 SPDIF receiver Block Diagram

The SPDIF receiver is composed of following modules.
SPDIF_RX_SYS

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The module implements the AHB slave operation. It contains not only control registers of SPDIF receiver inside but also interrupt and DMA handshaking interface.

CDR

The CDR is short for clock and data recovery. Clock and data can be recovered from the input bitstream by using a high frequency reference clock.

DECODER

The clock recovered from the CDR is used as the working clock to decode the input bitstream such as extracting audio data, the corresponding preamble code, V/U/C/P flags and other audio information.

RX_FIFO

The RX FIFO stores the audio data extracted from input bitstream. The size of the FIFO is 30bitsx32.

26.3 Function description

26.3.1 Frame Format

SPDIF receiver follows the same protocol (IEC60958/IEC61937) as SPDIF transmitter. A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of receiving of frames corresponds exactly to the source sampling frequency.

In the 2-channel operation mode, the samples received from both channels are arranged by time multiplexing in consecutive sub-frames. The first subframe (left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information. The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

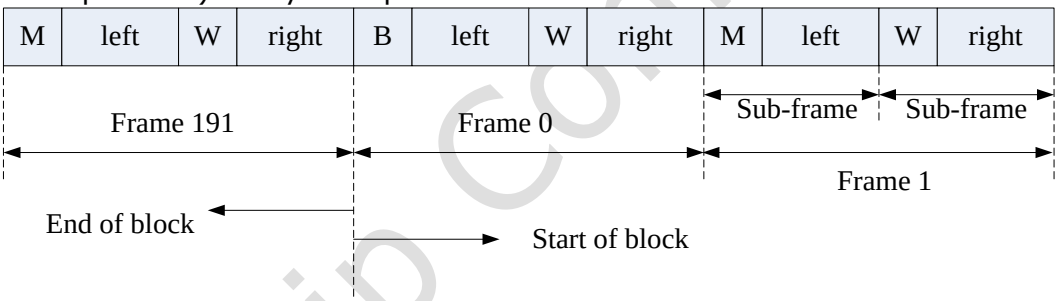

Fig.26-2 SPDIF Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

26.3.2 Sub-frame Format

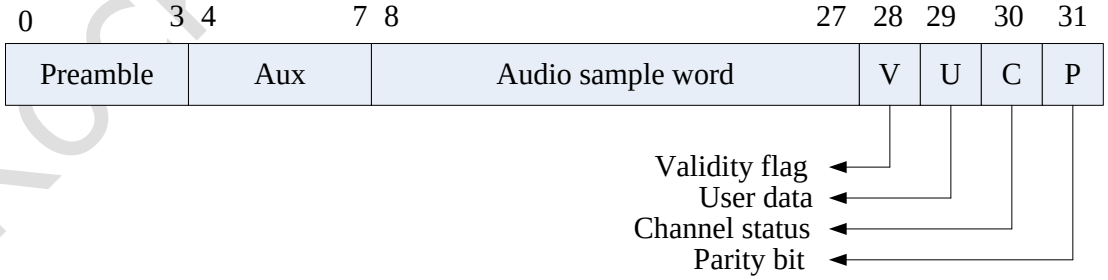

Fig.26-3 SPDIF Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8. Time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to 7 are designated auxiliary sample bits.

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If the source provides fewer bits than the interface allows (either 24 or 20), the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

26.3.3 Channel Coding

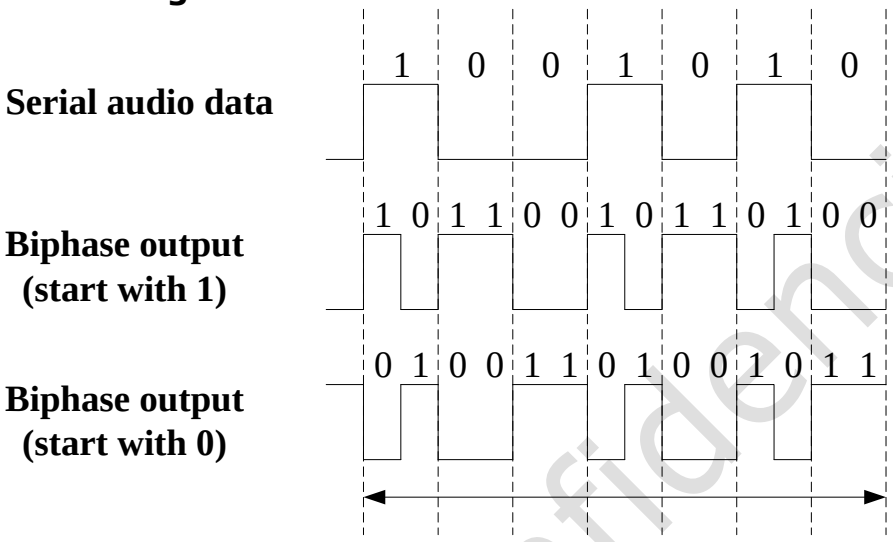

Fig.26-4 SPDIF Channel Coding

To minimize the direct current component on the transmission/receiving line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.

Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'. However, it is different from the first if the bit is logical '1'.

26.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.

To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.

A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

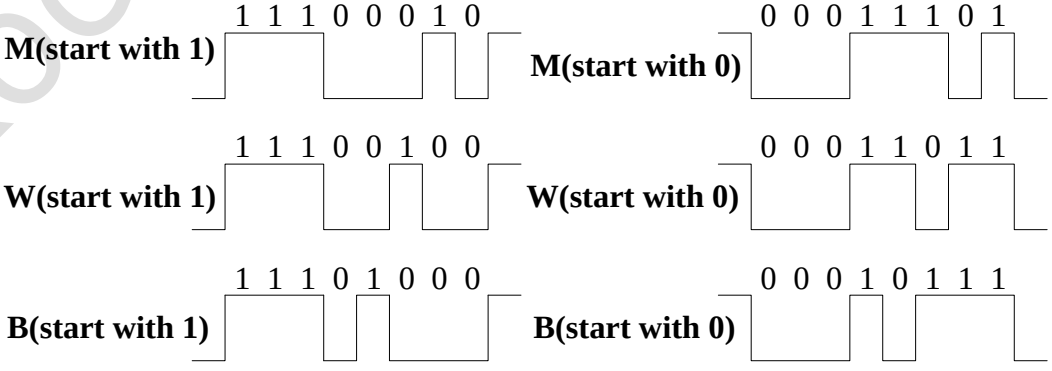

Fig.26-5 SPDIF Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

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26.4 Register Description

26.4.1 Internal Address Mapping

26.4.2 Slave address can be divided into different length for different usage, which is shown as follows.

26.4.3 Registers Summary

Name	Offset	Size	Reset Value	Description
SPDIF_RX_VERSION	0x0000	W	0x23123506	Version Register
SPDIF_RX_CFGR	0x0004	W	0x00000000	Configuration Register
SPDIF_RX_CLR	0x0008	W	0x00000000	Clear Register
SPDIF_RX_CDR	0x000C	W	0x000000A1	Clock And Data Recovery Register
SPDIF_RX_CDRST	0x0010	W	0x03FF00FF	Clock And Data Recovery Status Register
SPDIF_RX_DMACR	0x0014	W	0x00000000	DMA Control Register
SPDIF_RX_FIFOCTRL	0x0018	W	0x00000000	FIFO Control Register
SPDIF_RX_INTEN	0x001C	W	0x00000000	Interrupt Enable Register
SPDIF_RX_INTMASK	0x0020	W	0x00000000	Interrupt Mask Register
SPDIF_RX_INTSR	0x0024	W	0x00000000	Interrupt Status Register
SPDIF_RX_INTCLR	0x0028	W	0x00000000	Interrupt Clear Register
SPDIF_RX_SMPDR	0x002C	W	0x00000000	Sample Data Register
SPDIF_RX_USRDRn	0x0030	W	0x00000000	User Data Register n(n=0~11)
SPDIF_RX_CHNSRn	0x0060	W	0x00000000	Channel Status Register n(n=0~11)
SPDIF_RX_CDR_TIME	0x0090	W	0x03FF03FF	CDR Time Register
SPDIF_RX_RX_STATUS	0x0094	W	0x00000000	Status Register
SPDIF_RX_BURTSINFO	0x0100	W	0x00000000	Channel Burst Info Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.4.4 Detail Registers Description

SPDIF_RX_VERSION

Address: Operational Base(0xFF3B0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x23123506	VER Version of SPDIF_RX.

SPDIF_RX_CFGR

Address: Operational Base(0xFF3B0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	DAT 1'b0: Disable data join 1'b1: Enable data join
1	RW	0x0	TWAD 1'b0: Only audio data transmitted to FIFO. 1'b1: Block start, channel number and VUCP transmitted with audio data to FIFO.
0	RW	0x0	EN 1'b0: Disable SPDIF_RX 1'b1: Enable SPDIF_RX

SPDIF_RX_CLR

Address: Operational Base(0xFF3B0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	RXSC This is a software self-cleared bit. Write 1'b1 to clear all receive logic.

SPDIF_RX_CDR

Address: Operational Base(0xFF3B0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	JITTRSH CDR jitter threshold. It is valid only when BYPASS is 1'b0.
23:16	RW	0x00	MIDRGE CDR jitter middle range. It is valid only when BYPASS is 1'b0.
15:11	RO	0x00	reserved
10:9	RO	0x0	CS CDR state 2'b00: Idle state. CDR is idle and waits for rising edge of SPDIF_RX input bitstream. 2'b01: Detect state 2'b10: Measurement state 2'b11: Synchronization state
8:7	RO	0x1	JITST CDR jitter status 2'b01: Low 2'b10: High 2'b11: Normal It is valid only when BYPASS is 1'b0.
6	RO	0x0	FULL CDR FIFO full status 1'b0: Not full 1'b1: Full It is valid only when BYPASS is 1'b0.
5	RO	0x1	EMPTY CDR FIFO empty status 1'b0: Not empty 1'b1: Empty It is valid only when BYPASS is 1'b0.
4:2	RW	0x0	AVGWIN Average the non-jitter recovered clock from bitstream at a period of AVGWIN time.
1	RW	0x0	AVGSEL Select if the minimum or average number of cycles from the calculation of SPDIF_RX input bitstream pulse width. 1'b0: Minimum number of cycles 1'b1: Average number of cycles, that is (max+min)/4.
0	RW	0x1	BYPASS Write 1'b1 to enable CDR non-jitter bypass mode. It's recommended that this bit set to 1'b1. Please ensure that this bit is set to 1'b1 before starting receiving data.

SPDIF_RX_CDRST

Address: Operational Base(0xFF3B0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x03ff	NOSTRTHR The threshold counter determines the latency between input bitstream idle and exit synchronous status. Make sure that this value is large than 16'h03ff.

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	MAXCNT The value indicates the number of reference clock cycles to oversample the maximum pulse width of bitstream.
7:0	RO	0xff	MINCNT The value indicates the number of reference clock cycles to oversample the minimum pulse width of bitstream.

SPDIF_RX_DMACR

Address: Operational Base(0xFF3B0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	RDE 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
4:0	RW	0x00	RDL This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1. That is, dma_rx_req is generated when the number of valid data entries in the sample date buffer is equal to or above this field value + 1.

SPDIF_RX_FIFOCTRL

Address: Operational Base(0xFF3B0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RO	0x00	RFL Contains the number of valid data entries in the receive FIFO.
7:5	RO	0x0	reserved
4:0	RW	0x00	RFT When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO full interrupt is triggered.

SPDIF_RX_INTEN

Address: Operational Base(0xFF3B0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	CHERRIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if current data channel err.
12	RW	0x0	TYPEIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if current type bit is different from previous one.
11	RW	0x0	VCGIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if current valid width bit is different from previous one.
10	RW	0x0	UBCIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if current user bit is different from previous one.

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Bit	Attr	Reset Value	Description
9	RW	0x0	ESYNCIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate when entering synchronous state.
8	RW	0x0	BTEIE 1'b0: Disable 1'b1: Enable When enabled, an interrupt will generate when the block receive is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM.
7	RW	0x0	NSYNCIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if CDR change from synchronization state to idle state.
6	RW	0x0	BMDEIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if a biphase mark decoding error has occurred.
5	RW	0x0	RXOIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if FIFO is overrun.
4	RW	0x0	RXFIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if FIFO is full.
3	RW	0x0	NPSPIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if non-liner PCM sync word is received.
2	RW	0x0	NVLDIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if validity bit received from bitstream is 1'b1.
1	RW	0x0	CSCIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if current channel status bit is different from previous one.
0	RW	0x0	PEIE 1'b0: Disable 1'b1: Enable If enabled, an interrupt will generate if a parity error has occurred.

SPDIF_RX_INTMASK

Address: Operational Base(0xFF3B0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	CHERRMASK 1'b0: Unmask 1'b1: Mask
12	RW	0x0	TYPEMASK 1'b0: Unmask 1'b1: Mask
11	RW	0x0	VCGMASK 1'b0: Unmask 1'b1: Mask
10	RW	0x0	UBCIMSK 1'b0: Unmask 1'b1: Mask
9	RW	0x0	ESYNCIMSK 1'b0: Unmask 1'b1: Mask
8	RW	0x0	BTEIMSK 1'b0: Unmask 1'b1: Mask
7	RW	0x0	NSYNCIMSK 1'b0: Unmask 1'b1: Mask
6	RW	0x0	BMDEIMSK 1'b0: Unmask 1'b1: Mask
5	RW	0x0	RXOIMSK 1'b0: Unmask 1'b1: Mask
4	RW	0x0	RXFIMSK 1'b0: Unmask 1'b1: Mask
3	RW	0x0	NPSPIMSK 1'b0: Unmask 1'b1: Mask
2	RW	0x0	NVLDIMSK 1'b0: Unmask 1'b1: Mask
1	RW	0x0	CSCIMSK 1'b0: Unmask 1'b1: Mask
0	RW	0x0	PEIMSK 1'b0: Unmask 1'b1: Mask

SPDIF_RX_INTSR

Address: Operational Base(0xFF3B0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	CHERRISR 1'b0: Inactive 1'b1: Active
12	RW	0x0	TYPEISR 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
11	RW	0x0	VCGISR 1'b0: Inactive 1'b1: Active
10	RO	0x0	UBCISR 1'b0: Inactive 1'b1: Active
9	RO	0x0	ESYNCISR 1'b0: Inactive 1'b1: Active
8	RO	0x0	BTEISR 1'b0: Inactive 1'b1: Active
7	RO	0x0	NSYNCISR 1'b0: Inactive 1'b1: Active
6	RO	0x0	BMDEISR 1'b0: Inactive 1'b1: Active
5	RO	0x0	RXOIS 1'b0: Inactive 1'b1: Active
4	RO	0x0	RXFIS 1'b0: Inactive 1'b1: Active
3	RO	0x0	NPSPIS 1'b0: Inactive 1'b1: Active
2	RO	0x0	NVLDIS 1'b0: Inactive 1'b1: Active
1	RO	0x0	CSCIS 1'b0: Inactive 1'b1: Active
0	RO	0x0	PEIS 1'b0: Inactive 1'b1: Active

SPDIF_RX_INTCLR

Address: Operational Base(0xFF3B0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	CHERRICLR Write 1'b1 to clear user bit change interrupt.
12	RW	0x0	TYPEICLR Write 1'b1 to clear user bit change interrupt.
11	RW	0x0	VCGICLR Write 1'b1 to clear user bit change interrupt.
10	RW	0x0	UBCICLR Write 1'b1 to clear user bit change interrupt.
9	RW	0x0	ESYNCICLR Write 1'b1 to clear entering synchronous state interrupt.
8	RW	0x0	BTEICLR Write 1'b1 to clear block transfer/repetition period end interrupt.
7	RW	0x0	NSYNCICLR Write 1'b1 to clear CDR not synchronization interrupt.

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Bit	Attr	Reset Value	Description
6	RW	0x0	BMDEICLR Write 1'b1 to clear bi-phase mark decoding interrupt.
5	RW	0x0	RXOICLR Write 1'b1 to clear receive overrun interrupt.
4	RW	0x0	RXFICLR Write 1'b1 to clear receive full interrupt.
3	RW	0x0	NPSPICLR Write 1'b1 to clear non-liner PCM sync word received interrupt.
2	RW	0x0	NVLDICLR Write 1'b1 to clear validity bit received interrupt.
1	RW	0x0	CSCICLR Write 1'b1 to clear channel status change interrupt.
0	RW	0x0	PEICLR Write 1'b1 to clear parity error interrupt.

SPDIF_RX_SMPDR

Address: Operational Base(0xFF3B0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	SMPDR Sample Data Register

SPDIF_RX_USRDRn

Address: Operational Base(0xFF3B0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	USR_SUB_1 User data bit for subframe 1
15:0	RO	0x0000	USR_SUB_0 User data bit for subframe 0

SPDIF_RX_CHNSRn

Address: Operational Base(0xFF3B0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CHNSR_SUB_1 Channel status bit for subframe 1
15:0	RO	0x0000	CHNSR_SUB_0 Channel status bit for subframe 0

SPDIF_RX_CDR_TIME

Address: Operational Base(0xFF3B0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x03ff	cdr_count_time Count time cycle value
15:0	RW	0x03ff	cdr_wait_time Wait time cycle value

SPDIF_RX_RX_STATUS

Address: Operational Base(0xFF3B0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8:5	RW	0x0	CH1_DATA_VLD The S/PDIF word length for channel 1. May be decoded as follows (from the S/PDIF standard). 0: Reserved 1: Reserved 2: SPDIF_LENGTH_16 3: Reserved 4: SPDIF_LENGTH_18 5: SPDIF_LENGTH_22 6: Reserved 7: Reserved 8: SPDIF_LENGTH_19 9: SPDIF_LENGTH_23 10: SPDIF_LENGTH_20 11: SPDIF_LENGTH_24 12: SPDIF_LENGTH_17 13: SPDIF_LENGTH_21 14: Reserved 15: Reserved
4:1	RW	0x0	CH0_DATA_VLD The S/PDIF word length for channel 0. May be decoded as follows (from the S/PDIF standard). 0: Reserved 1: Reserved 2: SPDIF_LENGTH_16 3: Reserved 4: SPDIF_LENGTH_18 5: SPDIF_LENGTH_22 6: Reserved 7: Reserved 8: SPDIF_LENGTH_19 9: SPDIF_LENGTH_23 10: SPDIF_LENGTH_20 11: SPDIF_LENGTH_24 12: SPDIF_LENGTH_17 13: SPDIF_LENGTH_21 14: Reserved 15: Reserved
0	RW	0x0	AUDIO_TYPE 0:PCM data 1:Compressd data

SPDIF_RX_BURTSINFO

Address: Operational Base(0xFF3B0000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PD Preamble Pd for non-linear PCM, indicating the length of burst payload in unit of bytes or bits.
15:13	RW	0x0	BSNUM This field indicates the bitstream number. Usually the bitstream number is 0.
12:8	RO	0x00	DATAINFO This field gives the data-type-dependent info.
7	RO	0x0	ERRFLAG 1'b0: Indicates a valid burst-payload. 1'b1: Indicates that the burst-payload may contain errors.

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Bit	Attr	Reset Value	Description
6:0	RO	0x00	DATATYPE 7'b0000000: Null data 7'b0000001: AC-3 data 7'b0000011: Pause data 7'b0000100: MPEG-1 layer 1 data 7'b0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 7'b0000110: MPEG-2 data with extension 7'b0000111: MPEG-2 AAC 7'b0001000: MPEG-2, layer-1 low sampling frequency 7'b0001001: MPEG-2, layer-2 low sampling frequency 7'b0001010: MPEG-2, layer-3 low sampling frequency 7'b0001011: DTS type I 7'b0001100: DTS type II 7'b0001101: DTS type III 7'b0001110: ATRAC 7'b0001111: ATRAC 2/3 7'b0010000: ATRAC-X 7'b0010001: DTS type IV 7'b0010010: WMA professional type I 7'b0110010: WMA professional type II 7'b1010010: WMA professional type III 7'b1110010: WMA professional type IV 7'b0010011: MPEG-2 AAC low sampling frequency 7'b0110011: MPEG-2 AAC low sampling frequency 7'b1010011: MPEG-2 AAC low sampling frequency 7'b1110011: MPEG-2 AAC low sampling frequency 7'b0010100: MPEG-4 AAC 7'b0110100: MPEG-4 AAC 7'b1010100: MPEG-4 AAC 7'b1110100: MPEG-4 AAC 7'b0010101: Enhanced AC-3 7'b0010110: MAT Others: Reserved

26.5 Interface Description

Table 26-1 SPDIF RX Interface Description

Module Pin	Direction	Rockchip matrix IO	IOMUX Setting
spdif_sdi	O	RM_IO	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

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26.6 Application Notes

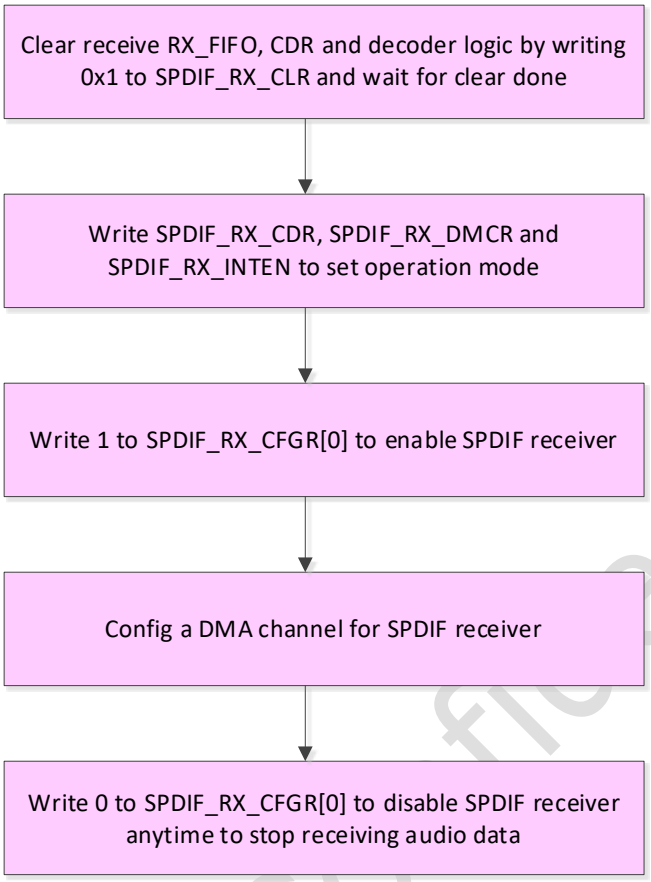

Fig.26-6 SPDIF receiver operation flow chart

The above figure shows the operation flow of SPDIF receiver operation.

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Chapter 27 Asynchronous Sample Rate Converter (ASRC)

27.1 Overview

ASRC converts digital audio data from one sample frequency to another. The input sample frequency can be an arbitrary fraction of the output frequency or the same frequency, but based on different clock sources. ASRC fetches audio data through AHB bus and acts as an intermediary for audio interfaces such as SAI, PDM, SPDIF, etc. With the help of ASRC, we can connect audio components with the embedded SOC platform together and provide an audio interface solution for the system.

27.1.1 Features

- Support two 4-channel ASRC0/1
- Support series mode which combines adjacent ASRC (ASRC0~1) into maximum 8-channel
- Support one 32-bit AHB-Lite bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support up to 4-channel with same ratio for ASRC0/1, which can be set to 2/4
- Support sample rate and resample rate range from 8 to 384KHz, mainly include three typical rate groups:
  1) 8KHz, 16KHz, 32KHz, 64KHz, 128KHz
  2) 12KHz, 24KHz, 48KHz, 96KHz, 192KHz, 384KHz
  3) 11.025KHz, 22.05KHz, 44.1KHz, 88.2KHz, 176.4KHz, 352.8KHz
- Support up-conversion, down-conversion, and 1:1 asynchronous conversion
- Support conversion ratio ranging from 1:8 (down) to 8:1 (up) with 22-bit resolution
- Support low deterministic latency related to ratio
- Support hard mute and soft mute
- Support typical THD+N below -120dB
- Support real-time transmission mode, which transmits or receives audio data from either audio component or memory with ratio tracking
- Support memory fetch mode, which transmits or receives audio data from memory with manual ratio without tracking
- Support input/output 16/20/24-bit wide audio data transfer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support audio data left or right justified in 32-bit wide FIFO
- Support half channels internal 48-bit wide and 16-location deep FIFOs for transmitting, and half channels 48-bit wide and 64-location deep FIFOs for receiving audio data
- Support fixed and incremental address access to transmit and receive FIFOs
- Support ratio_init/update_done, asrc_out_start, conv_done/error, fifo_in_empty/full, fifo_out_empty/full, ratio/src_lrck/dst_lrck_unlock interrupt, which can be masked
- Support combined interrupt output

27.2 Block Diagram

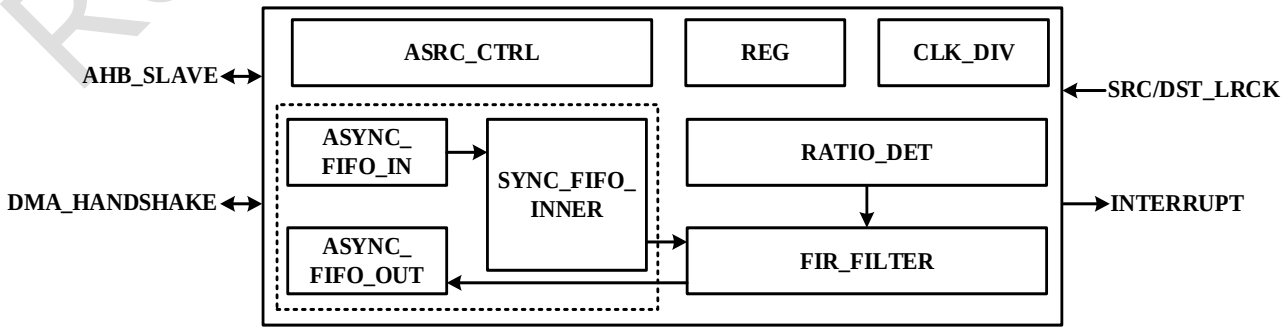

Fig. 27-1 ASRC Block Diagram

System Interface

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System interface implements the interactions with SOC platform. It contains not only AHB slave interface which controls registers and audio data transfer, but also LRCK interface, DMA handshaking interface and interrupt interface.

Clock Divider Block (CLK_DIV)

Clock divider block implements clock frequency divide function. The source clock of the divider block are src_lrck and dst_lrck, and by the divider, it generates clocks with the same frequency as sample rate or resample rate.

Register Block (REG)

Register block is responsible for the main ASRC functionality including control, status and interrupt generation.

Controller Block (ASRC_CTRL)

Controller block is the main control block of variable sampling filter, its main functions include filtering output judgment, coefficient position calculation and interpolation filtering.

Ratio Detector Block (RATIO_DET)

The main function of ratio detector block is to initialize and track ratio related parameters. In the initialization stage, related parameters is fetched directly from register configuration. Then in the tracking stage, ratio tracking is realized through periodic detection of src_lrck and dst_lrck. In the meantime, the water level of output FIFO is monitored for negative feedback adjustment.

FIR Block (FIR_FILTER)

FIR block acts as a poly-phase filter, which interpolates the correct phase and applies the calculated filter coefficients to the set of input samples to form an output sample.

Inner FIFO Block (SYNC_FIFO_INNER)

Inner FIFO block is the buffer to store audio data for FIR Filter. The size is 48bits x 512 and the number is half channels.

Input FIFO Block (ASYNC_FIFO_IN)

Input FIFO block is the buffer to store received audio data. The size is 48bits x 16 and the number is half channels.

Output FIFO Block (ASYNC_FIFO_OUT)

Output FIFO block is the buffer to store transmitted audio data. The size is 48bits x 64 and the number is half channels.

27.3 Function Description

Firstly, we define two basic modes of ASRC, memory fetch mode and real-time transmission mode. Then to enhance throughput, we define an enhancement mode called series mode, which can combine adjacent ASRCs together.

27.3.1 Memory Fetch Mode

In memory fetch mode, ASRC is working based on manual ratio, ratio tracking is disabled, so src_lrck or dst_lrck is unused. ASRC acts as peripheral when transmitting or receiving audio data from memory, so both dma_tx_req and dma_rx_req are started by ASRC. The faster the frequency of working clock, the faster the conversion will be completed.

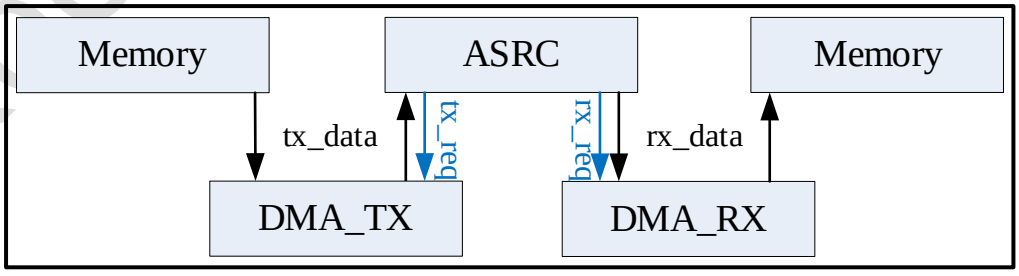

Fig. 27-2 ASRC Memory Fetch Mode Structure

Based on memory fetch mode, we extends a new sub-pattern called loop mode. With loop mode, multiple discrete audio files can be converted by only one configuration, or one continuous audio files can be split into multiple parts and converted by one configuration. The most significant application of loop mode is to convert more channel real-time audio data than ASRC defined by time division multiplexing. Audio data in the middle part of file

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should be recalled additionally for continuous output.

27.3.2 Real-time Transmission Mode

In real-time transmission mode, ASRC is working based on both manual ratio and tracking ratio, ratio tracking is enabled, so src_lrck or dst_lrck is needed. The faster the frequency of working clock, the more precise the tracking will be completed. Real-time transmission mode can be divided into four sub-patterns based on the component types at the source and destination ends, called MEM2MEM, MEM2DST, SRC2MEM and SRC2DST for short.

- **MEM2MEM**

In MEM2MEM mode, memory serves as both source and destination component. ASRC acts as peripheral when receiving audio data from memory or transmitting audio data to memory. Hence, both dma_tx_req and dma_rx_req are started by ASRC. Besides, both src_lrck and dst_lrck originate from CRU.

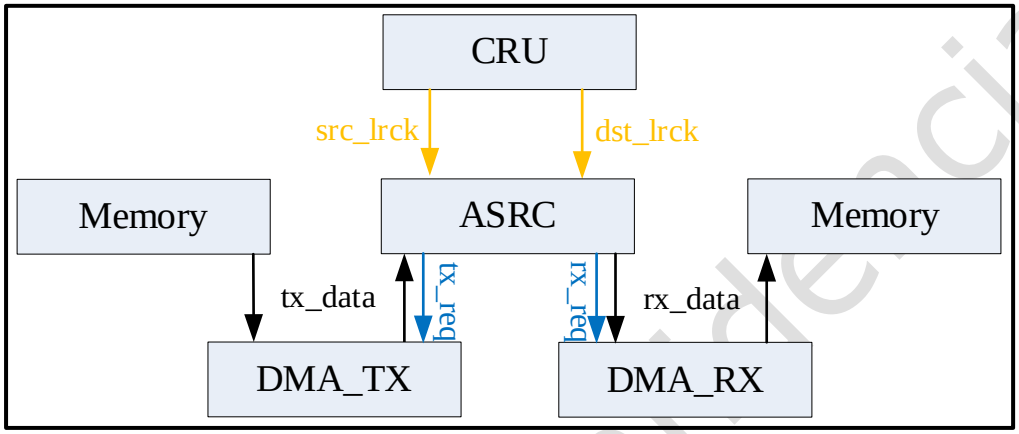

Fig. 27-3 ASRC MEM2MEM Mode Structure

- **MEM2DST**

In MEM2DST mode, memory serves as source component, and audio component serves as destination component. ASRC acts as peripheral when receiving audio data from memory, but as memory when transmitting audio data to peripheral. Hence, dma_tx_req is started by ASRC, but dma_rx_req is started by audio component. Besides, src_lrck originates from CRU, but dst_lrck originates from audio component.

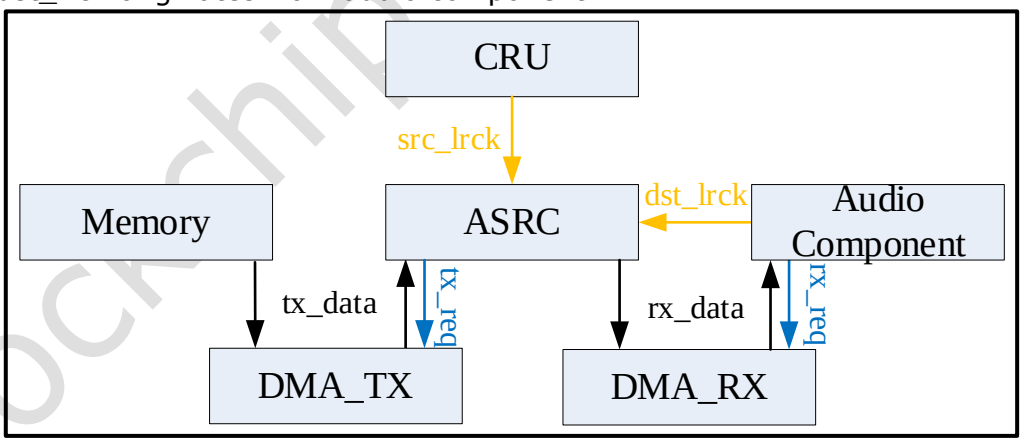

Fig. 27-4 ASRC MEM2DST Mode Structure

- **SRC2MEM**

In SRC2MEM mode, audio component serves as source component, and memory serves as destination component. ASRC acts as memory when receiving audio data from audio component, but as peripheral when transmitting audio data to memory. Hence, dma_tx_req is started by audio component, but dma_rx_req is started by ASRC. Besides, src_lrck originates from audio component, but dst_lrck originates from CRU.

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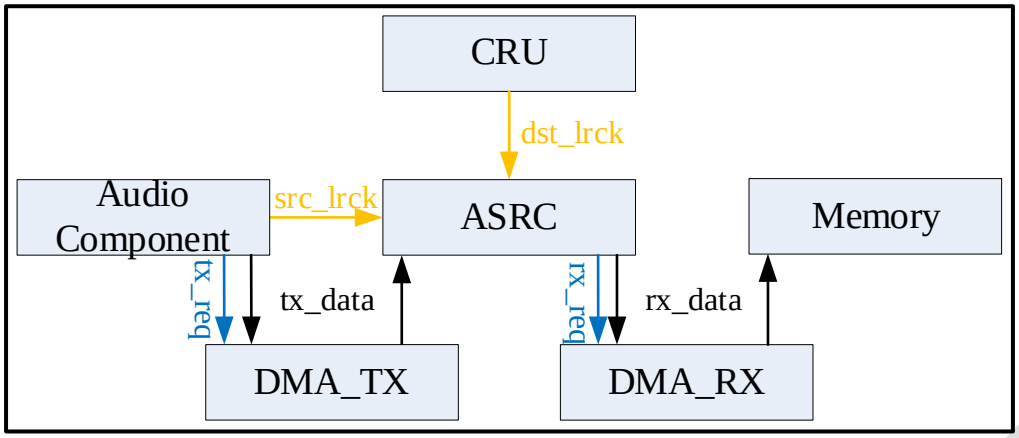

Fig. 27-5 ASRC SRC2MEM Mode Structure

- **SRC2DST**

In SRC2DST mode, audio component serves as both source component and destination component. ASRC acts as memory when receiving audio data from audio component or transmitting audio data to audio component. Hence, both dma_tx_req and dma_rx_req are started by audio component. Besides, both src_lrck and dst_lrck originate from audio component.

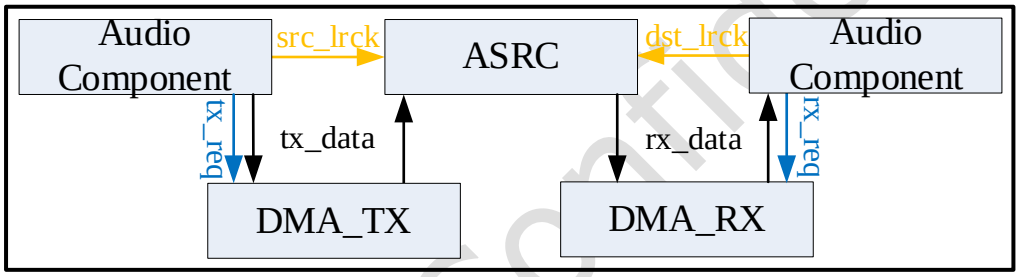

Fig. 27-6 ASRC SRC2DST Mode Structure

27.3.3 Series Mode

In series mode, adjacent ASRCs can be combined together to enhance throughput. We can appoint the ASRC at the front as master and other ASRCs as slave. All combined ASRCs can be viewed as a whole and interact with the outside world using the interface of master only. We can take MEM2MEM series mode as an example in the following figure. Note, the letter M stands for master and the letter S stands for slave.

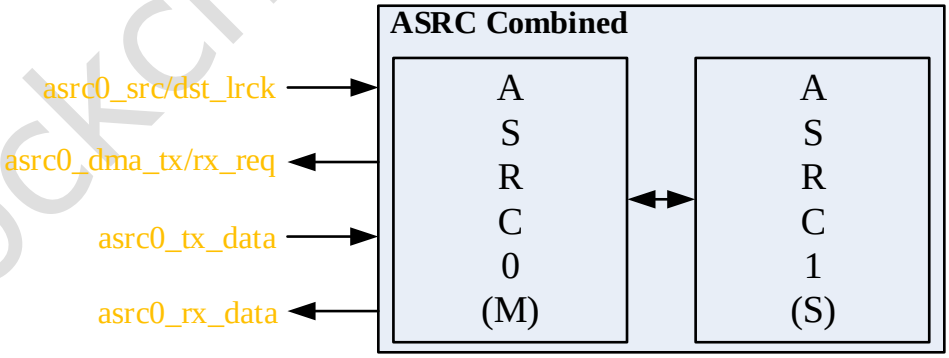

Fig. 27-7 ASRC MEM2MEM Series Mode Structure

In RK3506, ASRC0 and ASRC1 can be combined together into maximum 8-channel.

27.3.4 ASRC Latency

In real-time transmission mode, the latency of ASRC is determined by the phase delay of the FIR filter and fill level of the FIFO. For any given configuration and ratio, the latency of ASRC is fixed as follow:

Latency = phase delay + FIFO delay

Where phase delay equals 32 input sample periods when ratio is not more than one, or equals (32*ratio) input sample periods otherwise. FIFO delay equals (asrc_in_thresh+1)

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input sample periods plus (asrc_out_thresh+1) output sample periods.
In memory fetch mode, the conversion will be completed as fast as possible according to working clock only, regardless of src_lrck and dst_lrck, the latency can be ignored.

27.4 Register Description

27.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
ASRC4CH0 base address	0xFF3C0000
ASRC4CH1 base address	0xFF3D0000

27.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
ASRC_VERSION	0x0000	W	0x01010000	Version register
ASRC_ASRC_CON	0x0004	W	0x00280030	ASRC control register
ASRC_CLKDIV_CON	0x0008	W	0x00000000	LRCK divider control register
ASRC_DATA_FMT	0x000C	W	0x00000000	Data format register
ASRC_LOOP_CON0	0x0010	W	0x00000000	Loop control register 0
ASRC_LOOP_CON1	0x0014	W	0x00000000	Loop control register 1
ASRC_LOOP_CON2	0x0018	W	0x00000000	Loop control register 2
ASRC_MANUAL_RATIO	0x0020	W	0x00000000	Manual ratio register
ASRC_SAMPLE_RATE	0x0024	W	0x0002EE00	Sample rate register
ASRC_RESAMPLE_RATE	0x0028	W	0x0002EE00	Resample rate register
ASRC_TRACK_PERIOD	0x002C	W	0x000003FF	Track period register
ASRC_RATIO_MARGIN	0x0030	W	0x003FFFFF	Ratio margin register
ASRC_LRCK_MARGIN	0x0034	W	0x7FFF7FFF	LRCK margin register
ASRC_FETCH_LEN	0x0040	W	0x3F000000	Fetch length register
ASRC_DMA_THRESH	0x0050	W	0xEC40B333	DMA thresh register
ASRC_INT_CON	0x0060	W	0x00000000	Interrupt control register
ASRC_INT_ST	0x0064	W	0x00000000	Interrupt status register
ASRC_ASRC_ST0	0x0070	W	0x00000000	ASRC status register 0
ASRC_ASRC_ST1	0x0074	W	0x00000000	ASRC status register 1
ASRC_RATIO_ST	0x0080	W	0x00000000	Ratio status register
ASRC_RESAMPLE_RATE_ST	0x0084	W	0x00000000	Resample rate status register
ASRC_THETA_CNT_ST	0x0090	W	0x00000000	Theta counter status register
ASRC_DECI_THETA_ACC_ST	0x0094	W	0x00000000	Decimal theta accumulator status register
ASRC_FIFO_IN_WRCNT	0x00A0	W	0x00000000	Input FIFO write counter register
ASRC_FIFO_IN_RDCNT	0x00A4	W	0x00000000	Input FIFO read counter register
ASRC_FIFO_OUT_WRCNT	0x00B0	W	0x00000000	Output FIFO write counter register
ASRC_FIFO_OUT_RDCNT	0x00B4	W	0x00000000	Output FIFO read counter register
ASRC_FIFO_IN_FIXED_DR	0x00C0	W	0x00000000	Input FIFO fixed address data register
ASRC_FIFO_OUT_FIXED_DR	0x00C4	W	0x00000000	Output FIFO fixed address data register
ASRC_FIFO_IN_INCR_DR	0x1000	W	0x00000000	Input FIFO increment address data register
ASRC_FIFO_OUT_INCR_DR	0x5000	W	0x00000000	Output FIFO increment address data register

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

27.4.3 Detail Registers Description

ASRC_VERSION

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x01010000	version ASRC version number.

ASRC_ASRC_CON

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	soft_mute_en Soft mute enable. Each lane is controlled independently, bit 0~3 is corresponding to lane 0~3. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	hard_mute_en Hard mute enable. Each lane is controlled independently, bit 0~3 is corresponding to lane 0~3. 1'b0: Disable 1'b1: Enable
23:22	RO	0x0	reserved
21:20	RW	0x2	ratio_filt_win Ratio filter sliding window select. 2'b00: window width 2 2'b01: window width 4 2'b10: window width 8 2'b11: window width 16
19	RW	0x1	ratio_track_mode Ratio track mode select. 1'b0: Update src_lrck_cnt and dst_lrck_cnt once track period reached 1'b1: Update src_lrck_cnt and dst_lrck_cnt only when track period reached and the value change by more than one from the previous value
18	RW	0x0	ratio_exc_dis Ratio exceed detect disable. This bit works only when ratio_track_dis equal 0. 1'b0: Disable 1'b1: Enable
17	RW	0x0	ratio_filt_dis Ratio track filter disable. This bit works only when ratio_track_dis equal 0. 1'b0: Disable 1'b1: Enable
16	RW	0x0	ratio_track_dis Ratio track disable. 1'b0: Disable 1'b1: Enable
15	RW	0x0	series_rx_apart ASRC series enable but use respective rx request.
14	RW	0x0	series_tx_apart ASRC series enable but use respective tx request.

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	series_en ASRC series enable. 2'b00: series disable 2'b01: serve as series master 2'b10: serve as series slave
11	RW	0x0	series_post_end ASRC series post end flag. This bit works only when asrc_mode equal 1.
10	RO	0x0	reserved
9	RW	0x0	asrc_out_stop ASRC stop transmitting data to destination component. This bit works only when asrc_mode equal 0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	asrc_in_stop ASRC stop receiving data from source component. This bit works only when asrc_mode equal 0. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:4	RW	0x3	chan_num Channel number select. 2'b00: 2 channel used 2'b01: 4 channel used 2'b10: 6 channel used 2'b11: 8 channel used
3:2	RW	0x0	real_time_mode Real-time transmission mode select. This bit works only when asrc_mode equal 0. 2'b00: Memory as both source and destination component 2'b01: Peripheral as source component, Memory as destination component 2'b10: Memory as source component, Peripheral as destination component 2'b11: Peripheral as both source and destination component
1	RW	0x0	asrc_mode ASRC mode select. 1'b0: Real-time transmission mode 1'b1: Memory fetch mode
0	RW	0x0	asrc_en ASRC enable. 1'b0: Disable 1'b1: Enable In loop mode, this bit must be set after loop_en. When asrc_en equal 0, FIFOs in ASRC are self-cleared.

ASRC_CLKDIV_CON

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	dst_lrck_div_en dst_lrck divider enable. 1'b0: Disable 1'b1: Enable
30:16	RW	0x0000	dst_lrck_div_con dst_lrck divider. dst_lrck_div_con=Fdst_lrck/resample_rate-1.

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Bit	Attr	Reset Value	Description
15	RW	0x0	src_lrck_div_en src_lrck divider enable. 1'b0: Disable 1'b1: Enable
14:0	RW	0x0000	src_lrck_div_con src_lrck divider. src_lrck_div_con=Fsrc_lrck/sample_rate-1.

ASRC_DATA_FMT

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	OSJM Output data store justified mode, which indicate LSB of output data.
23:21	RO	0x0	reserved
20:16	RW	0x00	ISJM Input data store justified mode, which indicate LSB of input data.
15:13	RO	0x0	reserved
12	RW	0x0	OFMT Output data format. 1'b0: low bits data valid to AHB bus, high bits data invalid. 1'b1: 32 bit data valid to AHB bus. Low 16 bit for left channel and high 16 bit for right channel.
11:9	RO	0x0	reserved
8	RW	0x0	IFMT Input data format. 1'b0: low bits data valid from AHB bus, high bits data invalid. 1'b1: 32 bit data valid from AHB bus. Low 16 bit for left channel and high 16 bit for right channel.
7:6	RO	0x0	reserved
5:4	RW	0x0	OWL Output data bit wide. 2'b00: 24 bits 2'b01: 20 bits 2'b10: 16 bits 2'b01: Reserved
3:2	RO	0x0	reserved
1:0	RW	0x0	IWL Input data bit wide. 2'b00: 24 bits 2'b01: 20 bits 2'b10: 16 bits 2'b01: Reserved

ASRC_LOOP_CON0

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	loop_end_con Loop end mode. Each loop is controlled independently, bit 0~7 is corresponding to loop time 0~7. 1'b0: Convert the end part of a file 1'b1: Not convert the end part of a file

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Bit	Attr	Reset Value	Description
7:0	R/W SC	0x00	loop_start_con Loop start mode. Each loop is controlled independently, bit 0~7 is corresponding to loop time 0~7. 1'b0: Convert the start part of a file 1'b1: Not convert the start part of a file

ASRC_LOOP_CON1

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	chan_times Channel times, which means the actual channel to be converted is (chan_times+1) much as (chan_num+1).
7	RO	0x0	reserved
6:4	RW	0x0	loop_times Loop times, which means (loop_times+1) conversion is done continuously.
3:1	RO	0x0	reserved
0	R/W SC	0x0	loop_en ASRC loop enable. This bit is automatically cleared when loop conversion done. 1'b0: Disable 1'b1: Enable

ASRC_LOOP_CON2

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	R/W SC	0x0000	loop_gap_thresh ASRC loop gap thresh, which sets the interval between two conversion.

ASRC_MANUAL_RATIO

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	manual_ratio Manual ratio with fixed-point 26Q22. High 4 bits shows integer part, low 22 bits shows decimal part. manual_ratio=sample_rate/resample_rate.

ASRC_SAMPLE_RATE

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x2ee00	sample_rate Sample rate ranges from 8KHz to 384KHz.

ASRC_RESAMPLE_RATE

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x2ee00	resample_rate Resample rate ranges from 8KHz to 384KHz.

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ASRC_TRACK_PERIOD

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ratio_track_div Ratio track divider, which scale down the frequency of src_lrck and dst_lrck for higher precision of ratio tracking.
15:12	RO	0x0	reserved
11:0	RW	0x3ff	ratio_track_period Ratio track period, which means tracking information updates every (ratio_track_period+1)*(ratio_track_div+1) clock.

ASRC_RATIO_MARGIN

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x3fffff	ratio_margin Ratio margin with fixed-point 22Q22, which shows decimal part of ratio. Ratio unlock occurs when the difference between ratio_st and manual_ratio exceeds ratio_margin.

ASRC_LRCK_MARGIN

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RW	0x0	dst_lrck_margin_dis Dst_lrck drift detect disable. 1'b0: Disable 1'b1: Enable
30:16	RW	0x7fff	dst_lrck_margin Dst_lrck drift margin. Dst_lrck unlock occurs when the variation of dst_lrck exceeds dst_lrck_margin.
15	RW	0x0	src_lrck_margin_dis Src_lrck drift detect disable. 1'b0: Disable 1'b1: Enable
14:0	RW	0x7fff	src_lrck_margin Src_lrck drift margin. Src_lrck unlock occurs when the variation of src_lrck exceeds src_lrck_margin.

ASRC_FETCH_LEN

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x3f	mem_fetch_ext_cnt Memory fetch extend counter, is used only when asrc_mode equal 1. It extends the interval of filter operation, which works only when series_en not equal 0.
23:20	RO	0x0	reserved
19:0	RW	0x00000	fetch_length Memory fetch length, is used only when asrc_mode equal 1. It indicates the number of input data per channel. As input data is written by AHB bus in word, if the number written is called INPUT_WORD_NUM, the equation is as follows: fetch_length=INPUT_WORD_NUM*(IFMT+1)/(2*(chan_num+1))

ASRC_DMA_THRESH

Address: **Operational Base** + offset (0x0050)

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Bit	Attr	Reset Value	Description
31:26	RW	0x3b	asrc_pos_thresh Output FIFO positive thresh, unit channel_num. Exceed positive occurs once the number of valid data entries in the output FIFO is above this field value. Note, asrc_pos_thresh had better be higher than 59.
25:20	RW	0x04	asrc_neg_thresh Output FIFO negative thresh, unit channel_num. Exceed negative occurs once the number of valid data entries in the output FIFO is below this field value. Note, asrc_neg_thresh had better be lower than 4.
19:18	RO	0x0	reserved
17:12	RW	0x0b	asrc_out_thresh ASRC start output thresh, unit channel_num. Output will start once the number of valid data entries in the output FIFO is above this field value. Note, asrc_out_thresh must be higher than dma_rx_thresh.
11:8	RW	0x3	asrc_in_thresh ASRC start conversion thresh, unit channel_num. Conversion will start once the number of valid data entries in the input FIFO is above this field value. Note, asrc_in_thresh must be no more than dma_tx_thresh.
7:4	RW	0x3	dma_rx_thresh DMA rx request thresh, unit channel_num. The watermark level = dma_rx_thresh+1; that is, dma_rx_req is generated when the number of valid data entries in the output FIFO is equal to or above this field value + 1.
3:0	RW	0x3	dma_tx_thresh DMA tx request thresh, unit channel_num. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the input FIFO is equal to or below this field value.

ASRC_INT_CON

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	dst_lrck_unlock_en Enable dst_lrck unlock interrupt. 1'b0: Disable 1'b1: Enable
11	RW	0x0	src_lrck_unlock_en Enable src_lrck unlock interrupt. 1'b0: Disable 1'b1: Enable
10	RW	0x0	ratio_unlock_en Enable ratio unlock interrupt. 1'b0: Disable 1'b1: Enable
9	RW	0x0	fifo_out_empty_en Enable output FIFO empty interrupt. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	fifo_out_full_en Enable output FIFO full interrupt. 1'b0: Disable 1'b1: Enable
7	RW	0x0	fifo_in_empty_en Enable input FIFO empty interrupt. 1'b0: Disable 1'b1: Enable
6	RW	0x0	fifo_in_full_en Enable input FIFO full interrupt. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ratio_update_done_en Enable ratio update done interrupt. 1'b0: Disable 1'b1: Enable
4	RW	0x0	ratio_change_done_en Enable ratio change done interrupt. 1'b0: Disable 1'b1: Enable
3	RW	0x0	ratio_init_done_en Enable ratio initial done interrupt. 1'b0: Disable 1'b1: Enable
2	RW	0x0	conv_error_en Enable conversion error interrupt. 1'b0: Disable 1'b1: Enable
1	RW	0x0	conv_done_en Enable conversion done interrupt. 1'b0: Disable 1'b1: Enable
0	RW	0x0	asrc_out_start_en Enable ASRC output start interrupt. 1'b0: Disable 1'b1: Enable

ASRC_INT_ST

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	dst_lrck_unlock_st Dst_lrck unlock interrupt status. Level interrupt which can be clear by mask dst_lrck_unlock_en of INT_CON.
11	RO	0x0	src_lrck_unlock_st Src_lrck unlock interrupt status. Level interrupt which can be clear by mask src_lrck_unlock_en of INT_CON.
10	RO	0x0	ratio_unlock_st Ratio unlock interrupt status. Level interrupt which can be clear by mask ratio_unlock_en of INT_CON.
9	W1C	0x0	fifo_out_empty_st Output FIFO empty interrupt status.

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Bit	Attr	Reset Value	Description
8	W1C	0x0	fifo_out_full_st Output FIFO full interrupt status.
7	W1C	0x0	fifo_in_empty_st Input FIFO empty interrupt status.
6	W1C	0x0	fifo_in_full_st Input FIFO full interrupt status.
5	W1C	0x0	ratio_update_done_st Ratio update interrupt status.
4	W1C	0x0	ratio_change_done_st Ratio change interrupt status.
3	RO	0x0	ratio_init_done_st Ratio initial done interrupt status. Level interrupt which can be clear by mask ratio_init_done_en of INT_CON.
2	W1C	0x0	conv_error_st Conversion error interrupt status.
1	RO	0x0	conv_done_st Conversion done interrupt status. Level interrupt which can be clear by mask conv_done_en of INT_CON.
0	RO	0x0	asrc_out_start_st ASRC output start interrupt status. Level interrupt which can be clear by mask asrc_out_start_en of INT_CON.

ASRC_ASRC_ST0

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RO	0x00	chan_num_series Used channel number status in series mode.
7	RO	0x0	dma_rx_ack DMA rx acknowledge status.
6	RO	0x0	dma_rx_req DMA rx request status.
5	RO	0x0	dma_tx_ack DMA tx acknowledge status.
4	RO	0x0	dma_tx_req DMA tx request status.
3	RO	0x0	reserved
2	RO	0x0	filt_delay_done ASRC filter delay done status.
1	RO	0x0	asrc_out_start ASRC out start status.
0	RO	0x0	asrc_in_start ASRC in start status.

ASRC_ASRC_ST1

Address: **Operational Base** + offset (0x0074)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	ratio_state Ratio track state. 2'h0: IDLE 2'h1: RATIO_INIT 2'h2: RATIO_TRACK 2'h3: RATIO_STOP
29	RO	0x0	exceed_pos Output FIFO positive exceed status.
28	RO	0x0	exceed_neg Output FIFO negative exceed status.
27:26	RO	0x0	reserved
25:20	RO	0x00	pos_thresh Output FIFO positive thresh status, unit channel_num.
19:18	RO	0x0	reserved
17:12	RO	0x00	neg_thresh Output FIFO negative thresh status, unit channel_num.
11:10	RO	0x0	reserved
9:4	RO	0x00	fifo_out_level Output FIFO level, contains the number of valid data entries in the receive FIFO, unit channel_num.
3:0	RO	0x0	fifo_in_level Input FIFO level, contains the number of valid data entries in the transmit FIFO, unit channel_num.

ASRC_RATIO_ST

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RO	0x0000000	ratio_st Calculate ratio with fixed-point 26Q22. High 4 bits shows integer part, low 22 bits shows decimal part.

ASRC_RESAMPLE_RATE_ST

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	resample_rate_st Calculate resample rate status.

ASRC_THETA_CNT_ST

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RO	0x0000000	theta_cnt_st Theta counter status.

ASRC_DECI_THETA_ACC_ST

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	deci_theta_acc_st Decimal theta accumulator status.

ASRC_FIFO_IN_WRCNT

Address: **Operational Base** + offset (0x00A0)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_in_wrcnt Input FIFO write counter status, unit channel_num.

ASRC_FIFO_IN_RDCNT

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_in_rdcnt Input FIFO read counter status, unit channel_num.

ASRC_FIFO_OUT_WRCNT

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_out_wrcnt Output FIFO write counter status, unit channel_num.

ASRC_FIFO_OUT_RDCNT

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_out_rdcnt Output FIFO read counter status, unit channel_num.

ASRC_FIFO_IN_FIXED_DR

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_in_data Input FIFO fixed address data register.

ASRC_FIFO_OUT_FIXED_DR

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fifo_out_data Output FIFO fixed address data register.

ASRC_FIFO_IN_INCR_DR

Address: **Operational Base** + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_in_data Input FIFO increment address data register, which ranges from 0x1000 to 0x4FFF.

ASRC_FIFO_OUT_INCR_DR

Address: **Operational Base** + offset (0x5000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fifo_out_data Output FIFO increment address data register, which ranges from 0x5000 to x8FFF.

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27.5 Application Notes

27.5.1 LRCK Multiplexing Setting

There are src_lrck and dst_lrck interface which source from audio component or CRU. In real-time transmission mode, the following multiplexing selector need to be set.

Table 27-1 ASRC4ch0 Src_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
CRU_CLKSEL_CON47	3:0	5'd0: mclk_asrc0 5'd1: mclk_asrc1 5'd2: mclk_asrc2 5'd3: mclk_asrc3 5'd4: mclk_spdiftx_to_asrc 5'd5: mclk_spdifrx_to_asrc 5'd6: clkout_pdm 5'd7: sai0_fs 5'd8: sai1_fs 5'd9: sai2_fs 5'd10: sai3_fs 5'd11: sai4_fs

Table 27-2 ASRC4ch0 Dst_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
CRU_CLKSEL_CON47	7:4	5'd0: mclk_asrc0 5'd1: mclk_asrc1 5'd2: mclk_asrc2 5'd3: mclk_asrc3 5'd4: mclk_spdiftx_to_asrc 5'd5: mclk_spdifrx_to_asrc 5'd6: clkout_pdm 5'd7: sai0_fs 5'd8: sai1_fs 5'd9: sai2_fs 5'd10: sai3_fs 5'd11: sai4_fs

Table 27-3 ASRC4ch1 Src_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
CRU_CLKSEL_CON47	11:8	5'd0: mclk_asrc0 5'd1: mclk_asrc1 5'd2: mclk_asrc2 5'd3: mclk_asrc3 5'd4: mclk_spdiftx_to_asrc 5'd5: mclk_spdifrx_to_asrc 5'd6: clkout_pdm 5'd7: sai0_fs 5'd8: sai1_fs 5'd9: sai2_fs 5'd10: sai3_fs 5'd11: sai4_fs

Table 27-4 ASRC4ch1 Dst_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
CRU_CLKSEL_CON47	15:12	5'd0: mclk_asrc0 5'd1: mclk_asrc1 5'd2: mclk_asrc2 5'd3: mclk_asrc3 5'd4: mclk_spdiftx_to_asrc

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Register Name	MUX Setting	LRCK Source Select
		5'd5: mclk_spdifrx_to_asrc 5'd6: clkout_pdm 5'd7: sai0_fs 5'd8: sai1_fs 5'd9: sai2_fs 5'd10: sai3_fs 5'd11: sai4_fs

27.5.2 LRCK Divider Setting

In real-time transmission mode, src_lrck and dst_lrck are treated as data and sampled by working clock to realize periodic detection for ratio tracking. Frequency of src_lrck must be the same as sample rate of audio data, and frequency of dst_lrck must be the same as resample rate of audio data. To guarantee this, two clock dividers are integrating into ASRC. In the following condition, the corresponding divider ought to be set and we ought to wait for the generated clock to stabilize before starting ASRC.

- Using PDM as source component, set src_lrck_div_con to (pdm_oversample_rate-1)
- Using SPDIF_RX as source component, set src_lrck_div_con to 127
- Using SPDIF_TX as destination component, set dst_lrck_div_con to (128*spdiftx_div-1)

27.5.3 Tracking Period Setting

In real-time transmission mode, ratio tracking is enabled. Tracking period is determined by the value of ratio_track_period and ratio_track_div, which means track information updates every (ratio_track_period+1)*(ratio_track_div+1) working clock. The longer the period, the more precise the tracking. Besides, the following format must be meet to ensure ratio resolution:

(ratio_track_period+1)*(ratio_track_div+1) >=

Twclk*Fsrc_lrck*(1/Resolution+Fsrc_lrck/(Resolution*Fdst_lrck)+1)

Where Twclk is the period of working clock, Resolution is the bit wide of ratio, Fsrc_lrck is the frequency of src_lrck, and Fdst_lrck is the frequency of dst_lrck. Note that the smaller ratio_track_div is, the better, given the equation.

Besides, once lrck sources from CRU for audio component like USB or MAC, the fractional divider in the clock path of src_lrck or dst_lrck ought to be used for seamless switching. In this scenario, tracking period must be an integer multiple of the frequency division period, to guarantee ratio tracking accuracy.

27.5.4 DMA Setting

For transmitting data to ASRC and receiving data from ASRC, two DMA channels are need called DMA_TX and DMA_RX here. DMA mode used for various ASRC mode is shown below.

Table 27-5 ASRC DMA Mode Description

ASRC Mode	DMA_TX	DMA_RX
Memory Fetch Mode	M2P	P2M
MEM2MEM	M2P	P2M
MEM2DST	M2P	M2P
SRC2MEM	P2M	P2M
SRC2DST	P2M	M2P

In a word, once interacting with audio component, ASRC acts as memory and audio component issues DMA request, once interacting with memory, ASRC acts as peripheral and issues DMA request according to dma_tx_thresh and dma_rx_thresh.

Both dma_tx_thresh and dma_rx_thresh are in the unit of chan_num. That is, the relation between real DMA burst (called dma_tx/rx_burst) and dma_tx/rx_thresh is shown below:

dma_tx_thresh = dma_tx_burst*(IFMT+1)/(chan_num+1)/2-1

dma_rx_thresh = dma_rx_burst*(OFMT+1)/(chan_num+1)/2-1

27.5.5 Memory Fetch Mode Setting

- **Setting order**
  - Set and start DMA_TX and DMA_RX.
  - Set and start ASRC.

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- **ASRC start Flow**
  - Set used channel number, chan_num.
  - Set data format, OFMT, IFMT, OWL, IWL, OSJM and ISJM.
  - Set manual_ratio, sample_rate and resample_rate.
  - Set thresh, dma_rx_thresh, dma_tx_thresh, asrc_out_thresh and asrc_in_thresh;
  - Set asrc_mode to 1.
  - Set conversion length, fetch_length.
  - Set conv_done_en to enable conversion done interrupt.
  - In loop mode, set continuous conversion times (loop_times), file channel number divided by used channel number (chan_times), file type (loop_start/end_mode) and conversion interval (loop_gap_thresh), then enable loop_en.
  - Set asrc_en to enable ASRC.
- **ASRC end Flow**
  - Wait for conv_done and DMA_RX done interrupt.
  - Set asrc_en to disable ASRC.

27.5.6 Real-time Transmission Mode Setting

- **Setting order**
  - Set the source of src_lrck and dst_lrck.
  - Set src_lrck_div_con, src_lrck_div_en, dst_lrck_div_con, dst_lrck_div_en if needed.
  - Set and start DMA_TX and DMA_RX.
  - Set and start ASRC; ASRC must be set before source and destination component to make sure audio data is aligned by channel.
  - Set and start source component in the mode SRC2MEM or SRC2DST.
  - Set and start destination component in the mode MEM2DST or SRC2DST. Destination component had better start when asrc_out_start interrupt assert which means destination data is ready.
- **ASRC start Flow**
  - Set used channel number, chan_num.
  - Set data format, OFMT, IFMT, OWL, IWL, OSJM and ISJM.
  - Set manual_ratio, sample_rate and resample_rate.
  - Set thresh, dma_rx_thresh, dma_tx_thresh, asrc_out_thresh and asrc_in_thresh.
  - Set asrc_mode to 0; set real_time_mode.
  - Set ratio_track_period and ratio_track_div.
  - Set ratio_track_dis to disable ratio tracking, ratio_filt_dis to disable ratio tracking filter, or ratio_exc_dis to disable ratio tracking feedback if needed.
  - Set conv_done_en to enable conversion done interrupt.
- **ASRC end Flow**
  - Set asrc_in_stop to end conversion if source component stop.
  - Set asrc_out_stop to end conversion if destination component stop.
  - Wait for conv_done and DMA_RX done interrupt.
  - Set asrc_en to disable ASRC.

27.5.7 Series Mode Setting

In series mode, we can set each ASRC as mentioned above. Several additional setting is needed shown as follow:

- Set series_en to appoint master and slave; Note that series_en can’t be set if series mode is disabled.
- Set series_post_end to appoint the last slave if memory fetch mode is selected.
- Set asrc_en of the series master at the end after all other configurations are set.

The following table shows all the cascading combinations in RK3506. Note, the letter M stands for master and the letter S stands for slave.

Table 27-6 ASRC Series Description

Series Setting	Series Combination
ASRC0_ASRC_CON[13:12]=2’h1 ASRC1_ASRC_CON[13:12]=2’h2	ASRC0(M), ASRC1(S)

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Chapter 28 Flexible Serial Peripheral Interface（FSPI）

28.1 Overview

The FSPI is a flexible serial peripheral interface host controller to interface with external device.

The FSPI supports the following features:

- Support various vendor devices with flexible command sequencer engine
  - Serial NOR Flash
  - Serial NAND Flash
  - Serial pSRAM
  - Serial SRAM
- Support SDR mode
- Support Single/Dual/Quad IO mode
- Support a 32-bit AHB slave to read and write controller register bank and initiate command sequence, including transfer data from/to external device indirectly
- Support a 32-bit AHB master with embedded DMA engine to transfer data from/to external device indirectly
- Support independent clock for system bus HCLK and controller core SCLK
- Support maskable interrupts generation
- Support sampling clock with optionally configurable delay line
- Support 1 CS# operation

28.2 Block Diagram

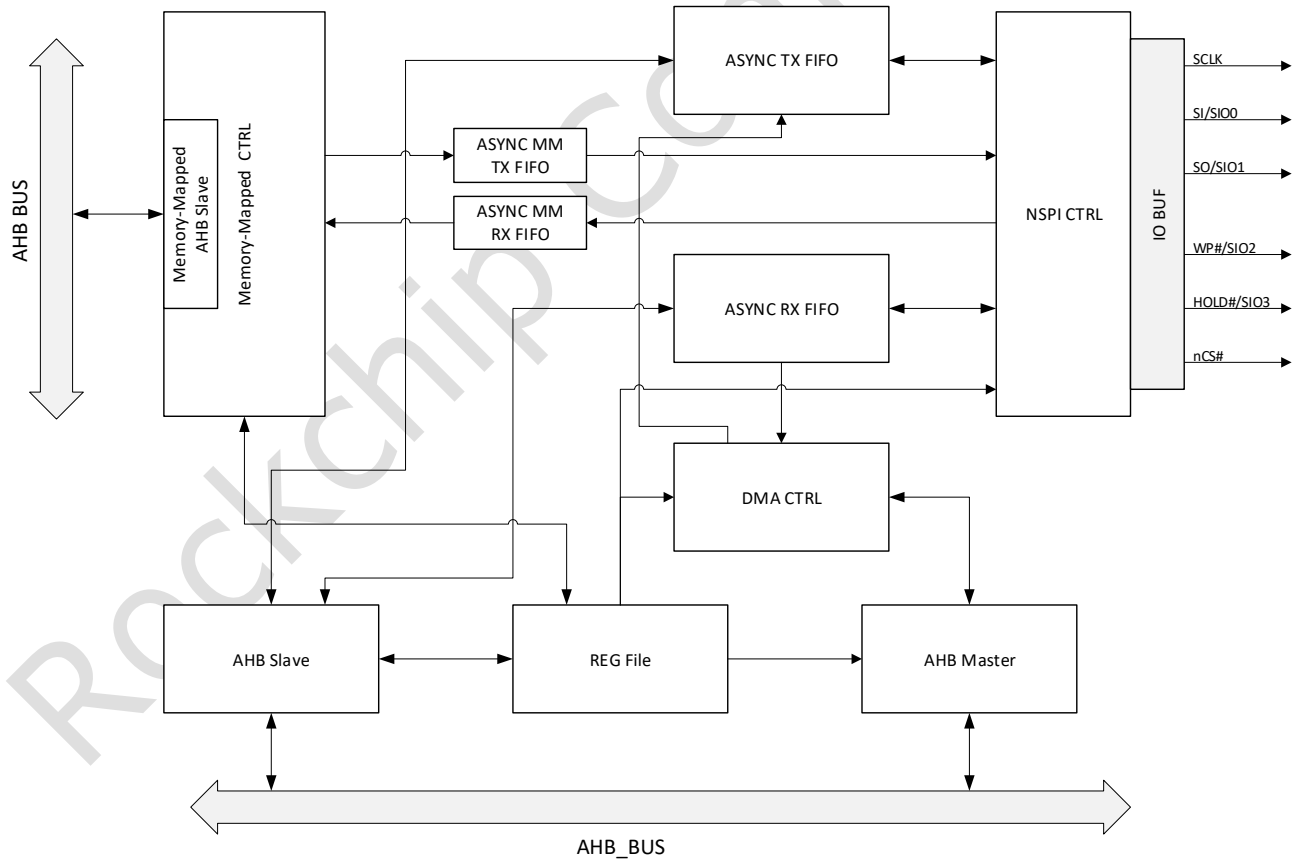

Fig. 28-1 FSPI Architecture

Memory-Mapped AHB slave is available when XIP feature is present. In current chip, this feature is not provided.

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28.3 Function Description

28.3.1 AHB Slave

The AHB slave block is used to configure the register of controller to generate flexible command sequence, process the interrupt exception, target various device feature and AC timing specification. It is also used to write CMD/ADDR/DATA to TX FIFO and read DATA from RX FIFO which buffer the DATA from external device.

28.3.2 AHB Master

When the embedded DMA CTRL is used to transfer DATA, the AHB master is used to transfer data to other system region, such as internal SRAM, peripheral, external DRAM.

28.3.3 REG File

The REG File is configurable register bank to control the store the static configuration and dynamic status of controller.

28.3.4 DMA CTRL

The block is responsible for splitting a long length transfer trans into AHB bus transaction and interfacing with ASYNC TX or RX FIFO.

28.3.5 FIFO

There are four FIFO in the FSPI controller. ASYNC TX FIFO and ASYNC RX FIFO is for normal transaction that initiated by command sequence driver. The ASYNC MM (Memory-Mapped) TX FIFO and ASYNC MM (Memory-Mapped) RX FIFO is only used to buffer DATA from or to external device initiated by system bus master directly.

28.3.6 NSPI CTRL

Sequence decode engine which generates specialized timing sequence for various device. The NSPI decode the transaction from TX FIFO and Memory-Mapped Controller and convert it to relative CMD/ADDR/DATA frame based on the configuration.

28.4 Register Description

28.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

28.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
FSPI_CTRL0	0x0000	W	0x00000000	Control Register for CS0 Device
FSPI_IMR	0x0004	W	0x000001FF	Interrupt Mask Register
FSPI_ICLR	0x0008	W	0x00000000	Interrupt Clear Register
FSPI_FTLR	0x000C	W	0x00001010	FIFO Threshold Level Register
FSPI_RCVR	0x0010	W	0x00000000	FSPI Recover Register
FSPI_AX0	0x0014	W	0x00000000	FSPI Auxiliary Data Value for CS0 Device
FSPI_ABIT0	0x0018	W	0x00000000	Extend Address Bits for CS0 Device
FSPI_ISR	0x001C	W	0x00000000	Interrupt Status
FSPI_FSR	0x0020	W	0x00000001	FIFO Status Register
FSPI_SR	0x0024	W	0x00000000	FSPI Status Register
FSPI_RISR	0x0028	W	0x00000000	Raw Interrupt Status Register
FSPI_VER	0x002C	W	0x00000009	Version Register
FSPI_QOP	0x0030	W	0x00000000	Quad Line Operation IO Level Pre-set Register
FSPI_EXT_CTRL	0x0034	W	0x00004023	Extend Control Register

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Name	Offset	Size	Reset Value	Description
FSPI_DLL_CTRL0	0x003C	W	0x00000001	Delay Line Control Register for CS0 Device
FSPI_EXT_AX	0x0044	W	0x0000F0FF	Extend Auxiliary Data Control Register
FSPI_SCLK_INATM_CNT	0x0048	W	0xFFFFFFFF	SCLK Inactive Timeout Counter
FSPI_XMMC_WCMD0	0x0050	W	0x00000000	Memory Mapped Control Write Command Register for CS0 Device
FSPI_XMMC_RCMD0	0x0054	W	0x00000000	Memory Mapped Control Read Command Register for CS0 Device
FSPI_XMMC_CTRL	0x0058	W	0x000072E0	Memory Mapped Control Register
FSPI_MODE	0x005C	W	0x00000000	Controller Working Mode Register
FSPI_DEVRGN	0x0060	W	0x00000017	Device Region Size Register
FSPI_DEVSIZE0	0x0064	W	0x00000012	Device Size Register for CS0 Device
FSPI_TME0	0x0068	W	0x00000000	Timeout Enable Control Register for CS0 Device
FSPI_XMMC_RX_WTMRK	0x0070	W	0x00000002	Memory Mapped Mode Receiver FIFO Water Mark Register
FSPI_DMATR	0x0080	W	0x00000000	DMA Trigger Register
FSPI_DMAADDR	0x0084	W	0x00000000	DMA Address Register
FSPI_LEN_CTRL	0x0088	W	0x00000000	Length Control Register
FSPI_LEN_EXT	0x008C	W	0x00000000	Length Extended Register
FSPI_XMMCSR	0x0094	W	0x00000000	Memory Mapped Status Register
FSPI_CMD	0x0100	W	0x00000000	Indirect Command Register
FSPI_ADDR	0x0104	W	0x00000000	Address Register
FSPI_DATA	0x0108	W	0x00000000	Data Register
FSPI_CTRL1	0x0200	W	0x00000000	Control Register for CS1 Device
FSPI_AX1	0x0214	W	0x00000000	FSPI Auxiliary Data Value for CS1 Device
FSPI_ABIT1	0x0218	W	0x00000000	Extend Address Bits for CS1 Device
FSPI_DBG_IO_CTRL	0x022C	W	0x00000000	Debug IO Control
FSPI_DLL_CTRL1	0x023C	W	0x00000001	Delay Line Control Register for CS1 Device
FSPI_XMMC_WCMD1	0x0250	W	0x00000000	Memory Mapped Control Write Command Register for CS1 Device
FSPI_XMMC_RCMD1	0x0254	W	0x00000000	Memory-Mapped Command Control Register for CS1 Device
FSPI_DEVSIZE1	0x0264	W	0x00000012	Device Size Register for CS1 Device
FSPI_TME1	0x0268	W	0x00000000	Timeout Enable Control Register for CS1 Device

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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28.4.3 Detail Registers Description

FSPI_CTRL0

Address: Operational Base(0xFF488000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	WP_EN WP# Port Enable 1'b0: Disable 1'b1: Enable. The WP# port will always be drived by QOP[SO123] when QOP[SO123BP] is setted to disable.
28:14	RO	0x0000	reserved
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_IMR

Address: Operational Base(0xFF488000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	DMAM DMA Finish Interrupt Mask 1'b0: DMA finish interrupt is not masked 1'b1: DMA finish interrupt is masked Only valid in indirect access mode.
6	RW	0x1	NSPIM NSPI Interrupt Mask 1'b0: NSPI interrupt is not masked 1'b1: NSPI interrupt is masked Valid in indirect access mode and memory mapped mode.
5	RW	0x1	AHBM AMBA AHB Error Interrupt Mask 1'b0: AMBA AHB Error interrupt is not masked 1'b1: AMBA AHB Error interrupt is masked Only valid in indirect access mode.
4	RW	0x1	TRANSM Transfer Finish Interrupt Mask 1'b0: Transfer finish interrupt is not masked 1'b1: Transfer finish interrupt is masked Only valid in indirect access mode.
3	RW	0x1	TXEM Transmit FIFO Empty Interrupt Mask 1'b0: Transmit FIFO empty interrupt is not masked 1'b1: Transmit FIFO empty interrupt is masked Only valid in indirect access mode.

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Bit	Attr	Reset Value	Description
2	RW	0x1	TXOM Transmit FIFO Overflow Interrupt Mask 1'b0: Transmit FIFO overflow interrupt is not masked 1'b1: Transmit FIFO overflow interrupt is masked Only valid in indirect access mode.
1	RW	0x1	RXUM Receive FIFO Underflow Interrupt Mask 1'b0: Receive FIFO underflow interrupt is not masked 1'b1: Receive FIFO underflow interrupt is masked Only valid in indirect access mode.
0	RW	0x1	RXFM Receive FIFO Full Interrupt Mask 1'b0: Receive FIFO full interrupt is not masked 1'b1: Receive FIFO full interrupt is masked Only valid in indirect access mode.

FSPI_ICLR

Address: Operational Base(0xFF488000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	DMAC DMA Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the DMAS
6	W1C	0x0	NSPIC NSPI Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the NSPIS.
5	W1C	0x0	AHBC AMBA AHB Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the AHBS.
4	W1C	0x0	TRANSC Transfer Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TRANSS.
3	W1C	0x0	TXEC Transmit FIFO Empty Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXES.

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Bit	Attr	Reset Value	Description
2	W1C	0x0	TXOC Transmit FIFO Overflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXOS.
1	W1C	0x0	RXUC Receive FIFO Underflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXUS.
0	W1C	0x0	RXFC Receive FIFO Full Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXFS.

FSPI_FTLR

Address: Operational Base(0xFF488000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x10	RXFTLR Receive FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of receive FIFO entries is bigger than or equal to this value, the receive FIFO full interrupt is triggered.
7:0	RW	0x10	TXFTLR Transmit FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

FSPI_RCVR

Address: Operational Base(0xFF488000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	R/WSC	0x0	RCVR FSPI Recover Write any values to trigger the recovery of SMC NSPI state machine, FIFO state and other logic state.

FSPI_AX0

Address: Operational Base(0xFF488000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT0

Address: Operational Base(0xFF488000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	ABIT Address Bits Extend 5'h0: 1 bit 5'h1: 2 bits ... 5'h1f: 32 bits Only valid when ADDRB is set to 2'b11.

FSPI_ISR

Address: Operational Base(0xFF488000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
6	RO	0x0	NSPIS NSPI Transaction Decode Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

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Bit	Attr	Reset Value	Description
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
0	RW	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

FSPI_FSR

Address: Operational Base(0xFF488000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	RXWLVL RX FIFO Water Level 5'h0: FIFO is empty 5'h1: 1 entry is taken ... 5'h10: 16 entry is taken, FIFO is full
15:13	RO	0x0	reserved
12:8	RO	0x00	TXWLVL TX FIFO Water Level 5'h0: FIFO is full 5'h1: 1 entry is left ... 5'h10: 16 entry is left, FIFO is empty
7:4	RO	0x0	reserved
3	RO	0x0	RXFS Receive FIFO Full Status 1'b0: RX FIFO is not full 1'b1: RX FIFO is full

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Bit	Attr	Reset Value	Description
2	RO	0x0	RXES Receive FIFO Empty Status 1'b0: RX FIFO is not empty 1'b1: RX FIFO is empty
1	RO	0x0	TXES Transmit FIFO Empty Status 1'b0: TX FIFO is not empty 1'b1: TX FIFO is empty
0	RO	0x1	TXFS Transmit FIFO Full Status 1'b0: TX FIFO is not full 1'b1: TX FIFO is full

FSPI_SR

Address: Operational Base(0xFF488000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	SR Status Register 1'b0: NSPI Controller is idle 1'b1: NSPI Controller is busy When controller is busy, don't change the setting of control register. When NSPI is idle, the software can initiate new transaction to external device.

FSPI_RISR

Address: Operational Base(0xFF488000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
6	RO	0x0	NSPIS NSPI Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

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Bit	Attr	Reset Value	Description
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
0	RO	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

FSPI_VER

Address: Operational Base(0xFF488000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0009	VER The Version ID of FSPI

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Address: Operational Base(0xFF488000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SO123BP SO123 Bypass Mode 1'b0: Disable bypass 1'b1: Enable bypass Default is enabled.
0	RW	0x0	SO123 D1/D2/D3 Data Value During Inactive When CS is Active 1'b0: Set to "0" 1'b1: Set to "1" The value of SO1, SO2 and SO3 during command and address bits input.

FSPI_EXT_CTRL

Address: Operational Base(0xFF488000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	SR_GEN_MODE Status Register Generation Mode 1'b0: Compatible mode with old controller 1'b1: Robust generation to indicates the status of controller If set to "1", the controller will only clear the SR bit after operation sequence done and CS is high.
13	RW	0x0	TRANS_INT_MODE Transmit Done Interrupt Generation Mode 1'b0: Trigger NSPI end in data done 1'b1: Trigger NSPI end in CS inactive Default Generation is compatible with old controller.
12	RO	0x0	reserved
11:8	RW	0x0	SWITCH_IO_O2I_CNT Switch IO Attribute Cycles in O2I Idle Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in O2I idle phase.

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Bit	Attr	Reset Value	Description
7:4	RW	0x2	SWITCH_IO_DUMM_CNT Switch IO Attribute Cycles in Dummy Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in Dummy data phase.
3:0	RW	0x3	CS_DESEL_CTRL CS Inactive Control 4'h0: Not support 4'h1: 2 cycles 4'h2: 3 cycles 4'h3: 4 cycles ... 4'hf: 16 cycles The target cycles to hold CS inactive after de-assert the CS. Default value are 4 SCLK cycles that is enough for normal device.

FSPI_DLL_CTRL0

Address: Operational Base(0xFF488000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	SCLK_SMP_SEL SCLK Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_EXT_AX

Address: Operational Base(0xFF488000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0xf0	AX_SETUP_PAT Auxiliary Setup Data Pattern The AX data pattern that setup the continuous/enhance/XIP read mode
7:0	RW	0xff	AX_CANCEL_PAT Auxiliary Cancel Data Pattern The AX data pattern that cancel the continuous/enhance/XIP read mode.

FSPI_SCLK_INATM_CNT

Address: Operational Base(0xFF488000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	SCLK_INATM_CNT SCLK Inactive Timeout Counter When CS is active and SCLK is hold in high or low due to TX FIFO is empty or RX FIFO is full, if SCLK_INATM_EN is enabled, and timeout occurs, the controller will go back to idle and RX FIFO is flushed.

FSPI_XMMC_WCMD0

Address: Operational Base(0xFF488000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.

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Bit	Attr	Reset Value	Description
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD0

Address: Operational Base(0xFF488000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_CTRL

Address: Operational Base(0xFF488000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	PFT_EN Prefetch Enable 1'b0: Disable 1'b1: Enable Should disable prefetch if controller communicate with pSRAM which need refresh.

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Bit	Attr	Reset Value	Description
5	RW	0x1	DEV_HWEN Device AMBA AHB HWRITE Enable 1'b0: Disable 1'b1: Enable
4:0	RO	0x00	reserved

FSPI_MODE

Address: Operational Base(0xFF488000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	XMMC_MODE_EN Memory Mapped Mode Enable 1'b0: Disable, indirect access mode 1'b1: Enable, Memory-Mapped mode Before switching from indirect access mode to Memory-Mapped mode, the application should make sure the controller is in idle state and no pending transaction. If switch from Memory-Mapped to indirect access mode, software should initiate a dummy read by CPU before that.

FSPI_DEVRGN

Address: Operational Base(0xFF488000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DEC_CTRL Decode Control 2'b00: 1 CS# 2'b01: 2 CS# 2'b10: 4 CS# 2'b11: Reserved Only valid in XMMC mode.
7:5	RO	0x0	reserved
4:0	RW	0x17	RSIZE Region Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes In Memory-Mapped mode, the CS is controlled by AHB address bus, region size is used to generate CS.

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FSPI_DEVSIZE0

Address: Operational Base(0xFF488000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G byte Device size is used to generate slop over status.

FSPI_TME0

Address: Operational Base(0xFF488000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

FSPI_XMMC_RX_WTMRK

Address: Operational Base(0xFF488000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	RX_FULL_WTMRK Memory Mapped Mode Receiver FIFO Water Mark. Default is enough.

FSPI_DMATR

Address: Operational Base(0xFF488000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	DMATR DMA Trigger Write "1" to start the DMA transfer.

FSPI_DMAADDR

Address: Operational Base(0xFF488000) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAADDR DMA Address The destination or source data address in current system.

FSPI_LEN_CTRL

Address: Operational Base(0xFF488000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	TRB_SEL Total Transfer Bytes Selection 1'b0: TRB controlled by CMD[TRB] 1'b1: TRB controlled by LEN_EXT

FSPI_LEN_EXT

Address: Operational Base(0xFF488000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRB_EXT Total Transfer Bytes Extended 32'd0: No data 32'd1: 1 Byte 32'd2: 2 Bytes ... Total data bytes number that will write to /read from the device.

FSPI_XMMCSR

Address: Operational Base(0xFF488000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/WSC	0x0	SLOPOVER1 Slop Over Register for CS1 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.
0	R/WSC	0x0	SLOPOVER0 Slop Over Register for CS0 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.

FSPI_CMD

Address: Operational Base(0xFF488000) + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:30	WO	0x0	CS Device Chip Select. 2'b00: Chip select 0 2'b01: Chip select 1 2'b10: Reserved 2'b11: Reserved
29:16	WO	0x0000	TRB Total Transfer Bytes 14'd0: No data 14'd1: 1 Byte 14'd2: 2 Bytes ... Total data bytes number that will write to or read from the device.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in indirect access mode. If there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	WO	0x0	WR Write or Read 1'b0: Read 1'b1: Write
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in indirect access mode.
7:0	WO	0x00	CMD Command Command data in indirect access mode.

FSPI_ADDR

Address: Operational Base(0xFF488000) + offset (0x0104)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ADDR Address Register Indirect access start address data for current command sequence.

FSPI_DATA

Address: Operational Base(0xFF488000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DATA Data Register Device data read or write from/to device.

FSPI_CTRL1

Address: Operational Base(0xFF488000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	WP_EN WP# Port Enable 1'b0: Disable 1'b1: Enable. The WP# port will always be drived by QOP[SO123] when QOP[SO123BP] is setted to disable.
28:14	RO	0x0000	reserved
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode.

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3:2	RO	0x0	reserved
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_AX1

Address: Operational Base(0xFF488000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT1

Address: Operational Base(0xFF488000) + offset (0x0218)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	ABIT Address Bits Extend 5'h0: 1 bit 5'h1: 2 bits ... 5'h1f: 32 bits Only valid when ADDRB is set to 2'b11.

FSPI_DBG_IO_CTRL

Address: Operational Base(0xFF488000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	DLL_DBG_EN Delayline IO Debug Enable 1'b0 : Disable 1'b1 : Enable
15:4	RO	0x000	reserved
3:2	RW	0x0	DBG_OUT1_MUX Debug IO1 Output Mux 2'b00 : Output Data[2] ; 2'b01 : Output Data[3] ; 2'b10 : Output CLK .
1:0	RW	0x0	DBG_OUT0_MUX Debug IO0 Output Mux 2'b00 : Output Data[0] ; 2'b01 : Output Data[1] ; 2'b10 : Output CLK .

FSPI_DLL_CTRL1

Address: Operational Base(0xFF488000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	SCLK_SMP_SEL SCLK sampling selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_XMMC_WCMD1

Address: Operational Base(0xFF488000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD1

Address: Operational Base(0xFF488000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_DEVSIZE1

Address: Operational Base(0xFF488000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes Device size is used to generate slop over status.

FSPI_TME1

Address: Operational Base(0xFF488000) + offset (0x0268)

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Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

28.5 Interface Description

Table 28-1 FSPI Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sfc_sclk	O	FSPI_CLK/GPIO2_A1	GPIO2_IOC_GPIO2A_IOMUX_SEL_0[3:0] =4'h1
sfc_cs0n	O	FSPI_CSN/GPIO2_A0	GPIO2_IOC_GPIO2A_IOMUX_SEL_0[7:4] =4'h1
sfc_sio0	I/O	FSPI_D0/GPIO2_A2	GPIO2_IOC_GPIO2A_IOMUX_SEL_0[11:8] =4'h1
sfc_sio1	I/O	FSPI_D1/GPIO2_A3	GPIO2_IOC_GPIO2A_IOMUX_SEL_0[15:12] =4'h1
sfc_sio2	I/O	FSPI_D2/GPIO2_A4	GPIO2_IOC_GPIO2A_IOMUX_SEL_1[3:0] =4'h1
sfc_sio3	I/O	FSPI_D3/GPIO2_A5	GPIO2_IOC_GPIO2A_IOMUX_SEL_1[7:4] =4'h1=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

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28.6 Application Notes

28.6.1 Typical Program Flow without DMA

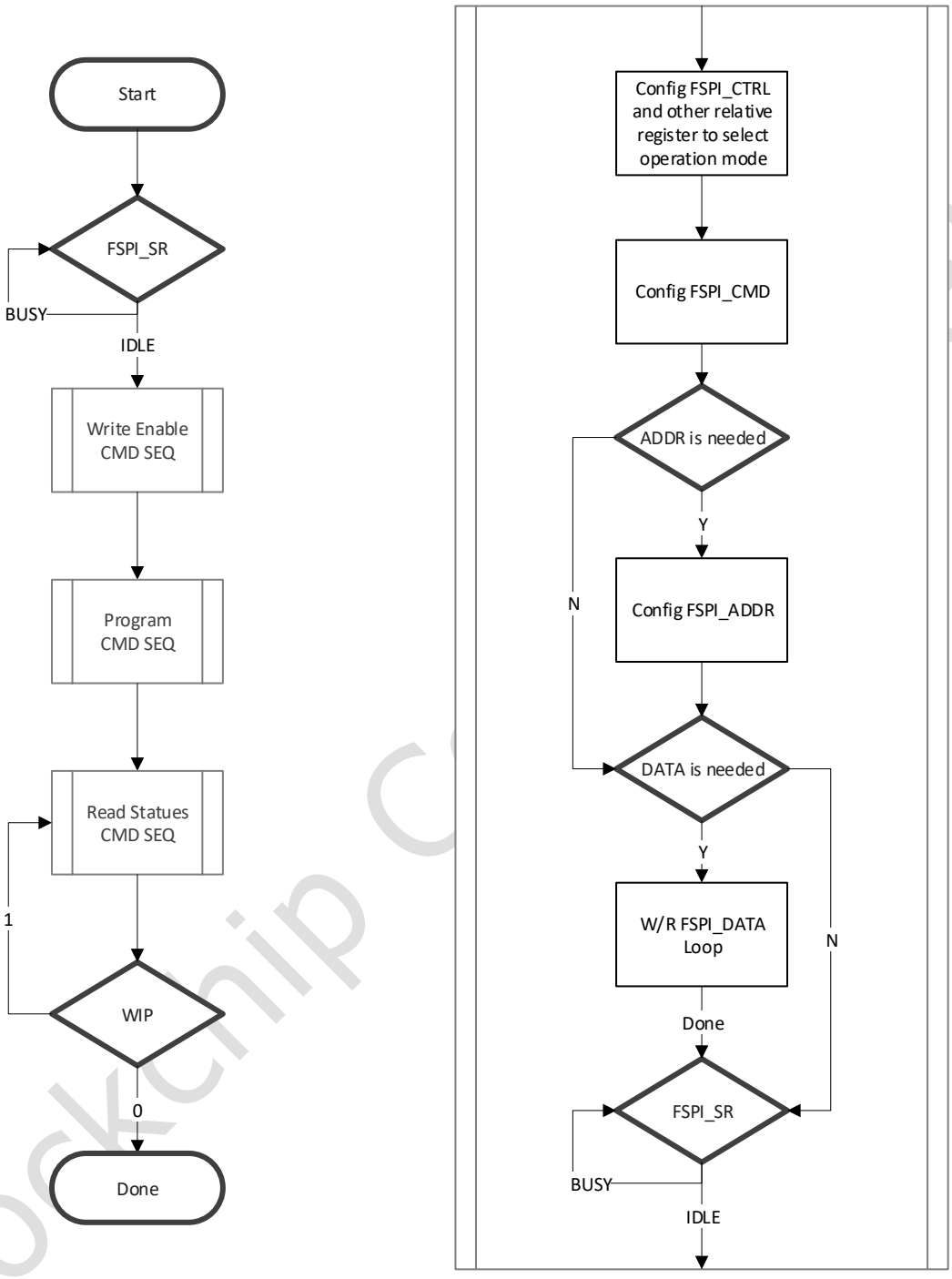

Fig. 28-2 Program Flow

All the AHB bus write data to FSPI_CMD, FSPI_ADDR and FSPI_DATA will be marked with different header and then pushed into transmit FIFO by writing order.

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28.6.2 Typical READ Flow without DMA

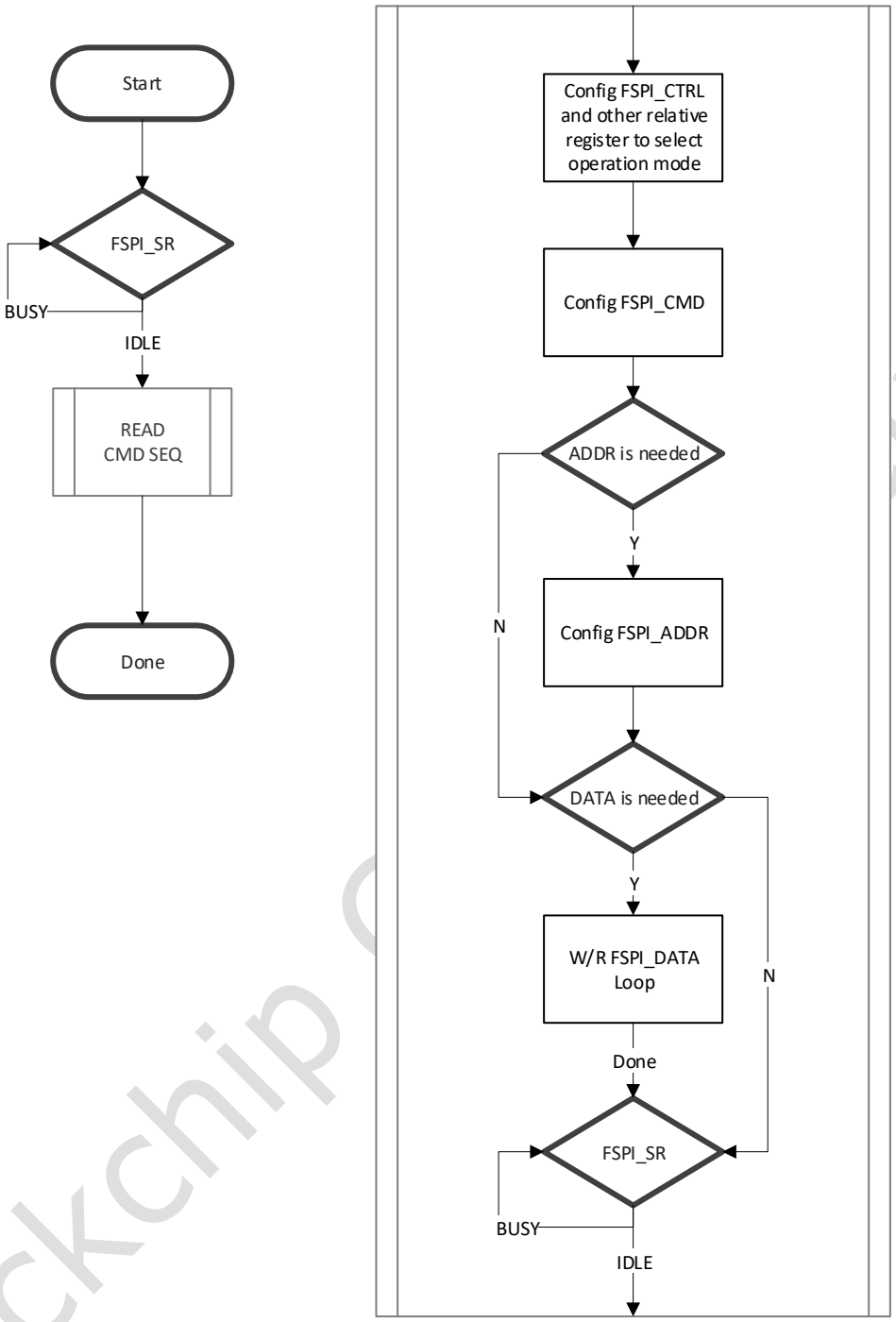

Fig. 28-3 Read Flow

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28.6.3 Command Flow with DMA

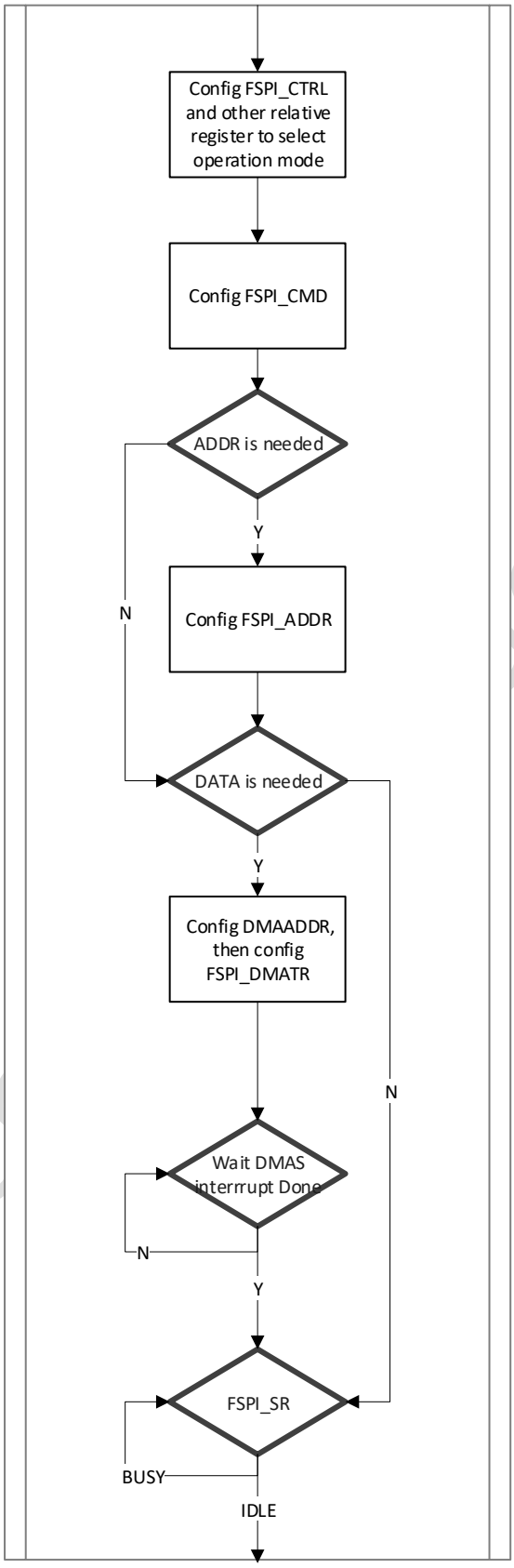

Fig. 28-4 Command with DMA Flow

The total transfer bytes is decided by TRB register in FSPI_CMD and must be aligned to 2 bytes.

28.6.4 SPI Mode and Sampling Phase Control

The register SPIM in FSPI_CTRL will decide the default value of SCLK when CS# is inactive. When SPIM=0, the default value is 0, means Mode 0. When SPIM=1, the default value is 1,

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means SPI Mode 3.

The register SHIFTPAHSE in FSPI_CTRL will decide when to sample the SIO data. If SHIFTPAHSE=0, it will sample the data at the posedge of SCLK sampling clock. If SHIFTPHASE=1, it will sample the data at the negedge of SCLK sampling. The phase delay of sampling clock SCLK is configurable by SMP_DLL_CFG. It is strongly recommended that the SMP_DLL_CFG is set to 1 when SCLK_SMP_SEL is in bypass mode.

Individual FSPI_DLL_CTRL[n] allows flexibly control the DLL for each CSN channel, and the DLL is switched dynamically when the CSN is in operation.

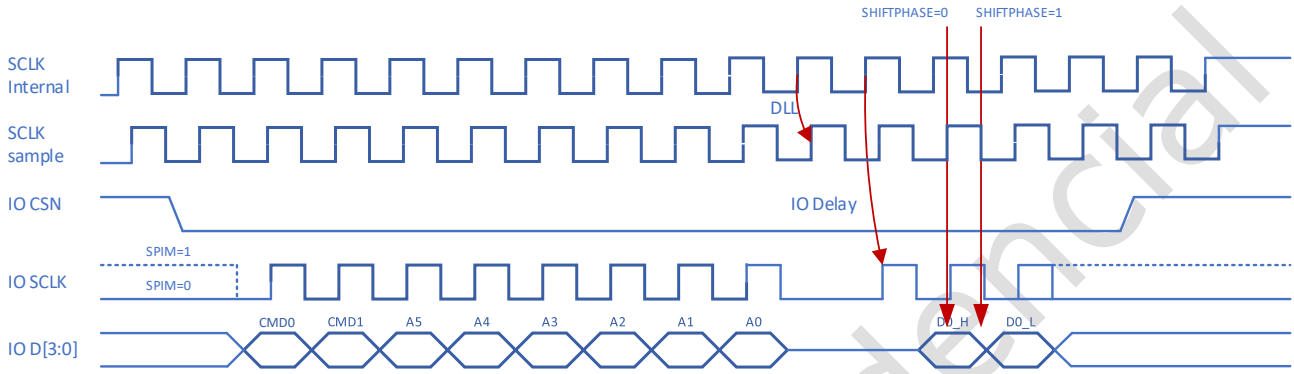

Fig. 28-5 SPI mode

28.6.5 Idle Cycles

The FSPI_CTRL register is a global control register, when the controller is in busy state (FSPI_SR), FSPI_CTRL cannot be set. The field IDLE_CYCLE (FSPI_CTRL[7:4]) of this register are used to configure the idle level cycles of FSPI core clock (SCLK) before reading the first bit of the read command.

Like the following picture shows, the highlighted line of the SCLK is the idle cycles, during these cycles, the chip pad is switched to output. When IDLE_CYCLE =0, it means there will be no idle level cycles.

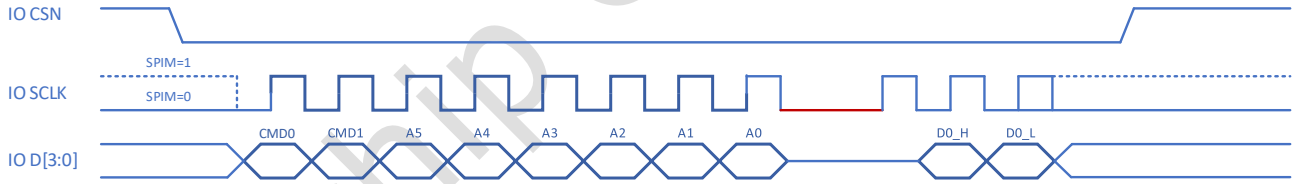

Fig. 28-6 Idle cycles

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Chapter 29 Serial Peripheral Interface (SPI)

29.1 Overview

The Serial Peripheral Interface is an APB slave device. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of slave select signals or the first edge of the serial clock. The slave select line is held high when the SPI is idle or disabled. This SPI controller can work as either master or slave mode.

SPI Controller supports the following features:

- Support Motorola SPI, TI Synchronous Serial Protocol and National Semiconductor Micro wire interface
- Support 32-bit APB bus
- Support two internal 16-bit wide and 64-location deep FIFOs, one for transmitting and the other for receiving serial data
- Support two chip select signals in master mode
- Support 4,8,16 bit serial data transfer
- Support configurable interrupt polarity
- Support asynchronous APB bus and SPI clock
- Support master and slave mode
- Support DMA handshake interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow, interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combining interrupt output
- Support up to half of SPI clock frequency transfer in master mode and one quarter of SPI clock frequency transfer in slave mode
- Support full and half duplex mode transfer
- Stop transmitting SCLK if transmit FIFO is empty or receive FIFO is full in master mode
- Support configurable delay from chip select active to SCLK active in master mode
- Support configurable period of chip select inactive between two parallel data in master mode
- Support big and little endian, MSB and LSB first transfer
- Support two 8-bit audio data store together in one 16-bit wide location
- Support sample MISO 0~3 SPI clock cycles later at master mode
- Support configurable SCLK polarity and phase
- Support fix and incremental address access to transmit and receive FIFO
- Support timeout mechanism in slave mode
- Support BYPASS slave mode, in which MISO and MOSI logic are driven by SCLK_IN directly instead of spi_clk

29.2 Block Diagram

The SPI Controller comprises with:

- AMBA APB interface and DMA Controller Interface
- Transmit and receive FIFO controllers and an FSM controller
- Register block
- Shift control and interrupt

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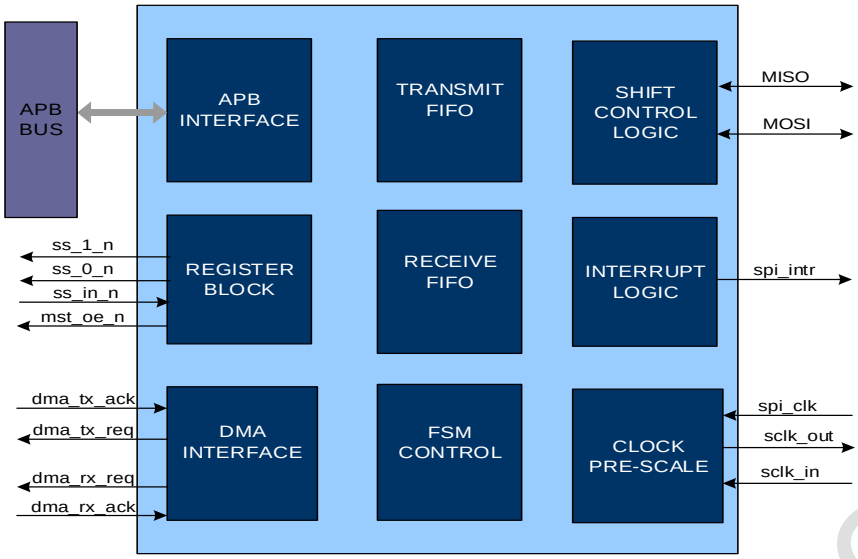

Fig. 29-1 SPI Controller Block Diagram

APB INTERFACE

The host processor accesses data, control, and status information on the SPI through the APB interface. The SPI supports APB data bus widths of 32 bits and 8 or 16 bits when reading or writing internal FIFO if data frame size (SPI_CTRL0[1:0]) is set to 8 bits.

DMA INTERFACE

This block has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA Controller.

FIFO LOGIC

For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the transmit FIFO. Data received from the external serial device into the SPI is pushed into the receive FIFO. Both FIFOs are 64x16bits.

FSM CONTROL

Control the state's transformation of the design.

REGISTER BLOCK

All registers in the SPI are addressed at 32-bit boundaries to remain consistent with the APB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

SHIFT CONTROL

Shift control logic shift the data from the transmit FIFO or to the receive FIFO. This logic automatically right-justifies receive data in the receive FIFO buffer.

INTERRUPT CONTROL

The SPI supports combined and individual interrupt requests, each of which can be masked. The combined interrupt request is the OR relationship between all other SPI interrupts after masking.

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29.3 Function Description

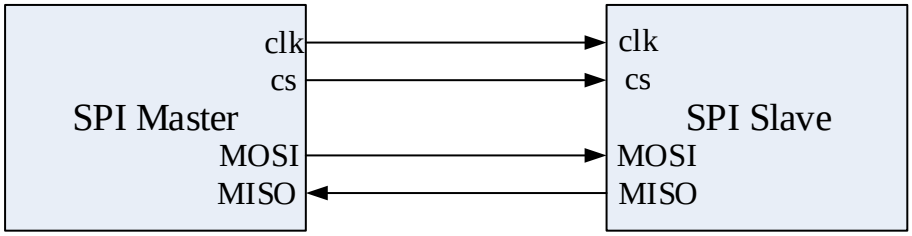

Fig. 29-2 SPI Master and Slave Interconnection

The SPI controller support dynamic switching between master and slave in a system. The diagram shows how the SPI controller connects with other SPI devices.

Operation Modes

The SPI can be configured in the following two fundamental modes of operation: Master Mode when SPI_CTRLR0 [20] is 1'b0, Slave Mode when SPI_CTRLR0 [20] is 1'b1, bypass Slave Mode when SPI_BYPASS[0] is 1'b1, additionally.

Transfer Modes

The SPI operates in the following three modes when transferring data on the serial bus.
1) Transmit and Receive
When SPI_CTRLR0 [19:18] == 2'b00, both transmit and receive logic are valid.
2) Transmit Only
When SPI_CTRLR0 [19:18] == 2'b01, the receive data are invalid and should not be stored in the receive FIFO.
3) Receive Only
When SPI_CTRLR0 [19:18] == 2'b10, the transmit data are invalid.

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as:
When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})
When SPI Controller works as normal slave, the F_{spi_clk}>= 4 × (maximum F_{sclk_in})
When SPI Controller works as bypass slave, no frequency ratio restrictions

With the SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical serial clock phase (SCPH) and clock polarity (SCPOL) values. The data frame can be 4/8/16 bits in length.

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the MISO and MOSI lines prior to the first serial clock edge. The following two figures show a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for configuration parameters SCPOL = 0 and SCPOL = 1.

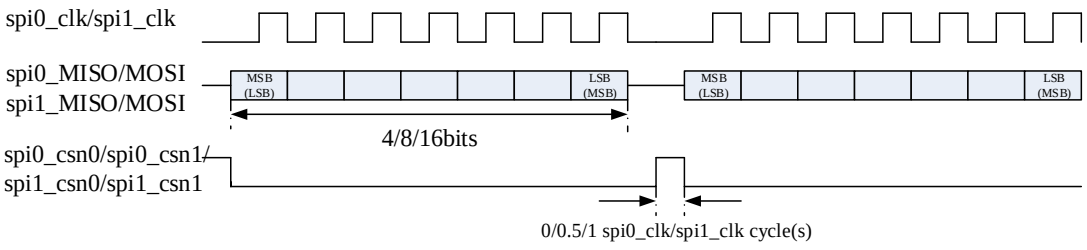

Fig. 29-3 SPI Format (SCPH=0 SCPOL=0)

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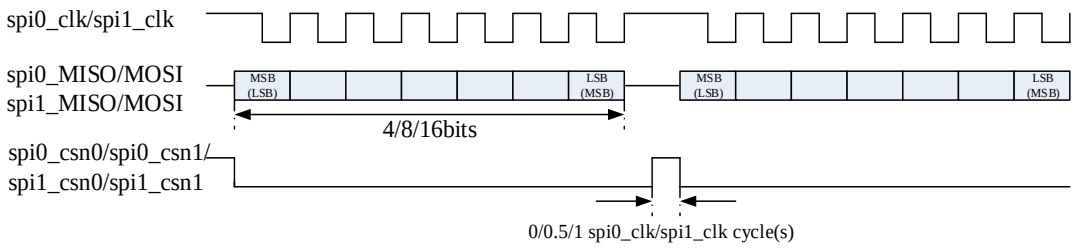

Fig. 29-4 SPI Format (SCPH=0 SCPOL=1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the SPI format when the configuration parameter SCPH = 1.

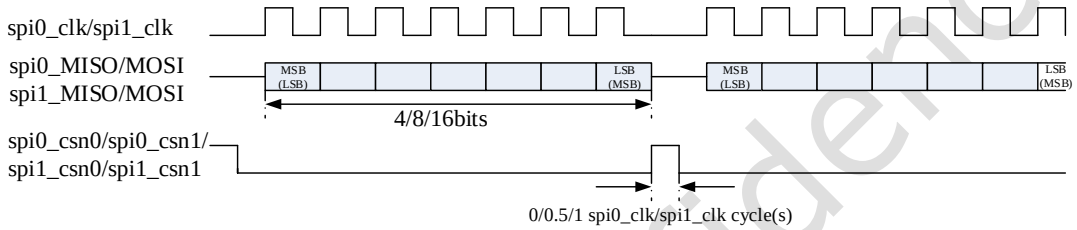

Fig. 29-5 SPI Format (SCPH=1 SCPOL=0)

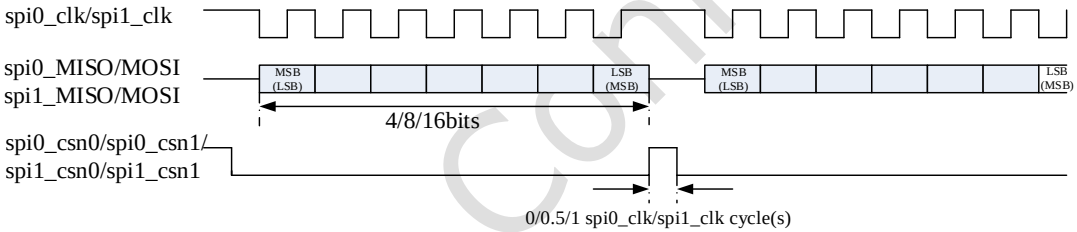

Fig. 29-6 SPI Format (SCPH=1 SCPOL=1)

29.4 Register Description

29.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SPI0	0xff120000
SPI1	0xff130000

29.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI_CTRLR0	0x0000	W	0x00000002	Control Register 0
SPI_CTRLR1	0x0004	W	0x00000000	Control Register 1
SPI_ENR	0x0008	W	0x00000000	SPI Enable Register
SPI_SER	0x000C	W	0x00000000	Slave Enable Register
SPI_BAUDR	0x0010	W	0x00000000	Baud Rate Select
SPI_TXFTLR	0x0014	W	0x00000000	Transmit FIFO Threshold Level
SPI_RXFTLR	0x0018	W	0x00000000	Receive FIFO Threshold Level
SPI_TXFLR	0x001C	W	0x00000000	Transmit FIFO Level
SPI_RXFLR	0x0020	W	0x00000000	Receive FIFO Level
SPI_SR	0x0024	W	0x0000004C	SPI Status
SPI_IPR	0x0028	W	0x00000000	Interrupt Polarity

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Name	Offset	Size	Reset Value	Description
SPI_IMR	0x002C	W	0x00000000	Interrupt Mask
SPI_ISR	0x0030	W	0x00000000	Interrupt Status
SPI_RISR	0x0034	W	0x00000001	Raw Interrupt Status
SPI_ICR	0x0038	W	0x00000000	Interrupt Clear
SPI_DMACR	0x003C	W	0x00000000	DMA Control
SPI_DMATDLR	0x0040	W	0x00000000	DMA Transmit Data Level
SPI_DMARDLR	0x0044	W	0x00000000	DMA Receive Data Level
SPI_VERSION	0x0048	W	0x03110003	IP version
SPI_TIMEOUT	0x004C	W	0x00000000	Timeout control register
SPI_BYPASS	0x0050	W	0x00000000	BYPASS control register
SPI_BPENR	0x0054	W	0x00000000	SPI BYPASS Enable Register
SPI_TXDR	0x0400	W	0x00000000	Transmit FIFO Data
SPI_RXDR	0x0800	W	0x00000000	Receive FIFO Data

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

29.4.3 Detail Registers Description

SPI_CTRLR0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	lbk Loop back mode select. 1'b0: Normal mode. 1'b1: Loop back mode, rxd is connected to txd.
24:23	RW	0x0	soi SS_N output inverted. 1'b0: Corresponding bit of ss_in is not inverted. 1'b1: Corresponding bit of ss_in is inverted.
22	RW	0x0	sm SCLK_IN is masked by SS_N or not. 1'b0: SCLK_IN is masked 1'b1: SCLK_IN is not masked
21	RW	0x0	mtm Valid when frame format is set to National Semiconductors Microwire. 1'b0: Non-sequential transfer 1'b1: Sequential transfer
20	RW	0x0	opm Master and slave mode select. 1'b0: Master Mode 1'b1: Slave Mode
19:18	RW	0x0	xfm Transmit and receive mode select. 2'b00 : Transmit & Receive 2'b01 : Transmit Only 2'b10 : Receive Only 2'b11 : Reserved
17:16	RW	0x0	frf 2'b00: Motorola SPI 2'b01: Texas Instruments SSP 2'b10: National Semiconductors Microwire 2'b11: Reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	rsd When SPI is configured as a master, if the rxd data cannot be sampled by the sclk_out edge at the right time, this register should be configured to define the number of the spi_clk cycles after the active sclk_out edge to sample rxd data later when SPI works at high frequency. 2'b00: Do not delay 2'b01: 1 cycle delay 2'b10: 2 cycles delay 2'b11: 3 cycles delay
13	RW	0x0	bht Valid when data frame size is 8bit. 1'b0: APB 16bit write/read, spi 8bit write/read. 1'b1: APB 8bit write/read, spi 8bit write/read.
12	RW	0x0	fbm 1'b0: First bit is MSB. 1'b1: First bit is LSB.
11	RW	0x0	em Serial endian mode can be configured by this bit. APB endian mode is always little endian. 1'b0: Little endian 1'b1: Big endian
10	RW	0x0	ssd Valid when the frame format is set to Motorola SPI and SPI used as a master. 1'b0: The period between ss_n active and sclk_out active is half sclk_out cycles. 1'b1: The period between ss_n active and sclk_out active is one sclk_out cycle.
9:8	RW	0x0	csm Valid when the frame format is set to Motorola SPI and SPI used as a master. 2'b00: ss_n keep low after every frame data is transferred. 2'b01: ss_n be high for half sclk_out cycles after every frame data is transferred. 2'b10: ss_n be high for one sclk_out cycle after every frame data is transferred. 2'b11: Reserved
7	RW	0x0	scpol Valid when the frame format is set to Motorola SPI. 1'b0: Inactive state of serial clock is low. 1'b1: Inactive state of serial clock is high.
6	RW	0x0	scph Valid when the frame format is set to Motorola SPI. 1'b0: Serial clock toggles in middle of first data bit. 1'b1: Serial clock toggles at start of first data bit.

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Bit	Attr	Reset Value	Description
5:2	RW	0x0	cfs Selects the length of the control word for the Microwire frame format. 4'b0000~0010: Reserved 4'b0011: 4-bit serial data transfer 4'b0100: 5-bit serial data transfer 4'b0101: 6-bit serial data transfer 4'b0110: 7-bit serial data transfer 4'b0111: 8-bit serial data transfer 4'b1000: 9-bit serial data transfer 4'b1001: 10-bit serial data transfer 4'b1010: 11-bit serial data transfer 4'b1011: 12-bit serial data transfer 4'b1100: 13-bit serial data transfer 4'b1101: 14-bit serial data transfer 4'b1110: 15-bit serial data transfer 4'b1111: 16-bit serial data transfer
1:0	RW	0x2	dfs Selects the data frame length. Therein, the slave bypass mode does not support the 4bits data length. 2'b00: 4bit data 2'b01: 8bit data 2'b10: 16bit data 2'b11: Reserved

SPI_CTRLR1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ndm When Transfer Mode is receive only, this register field sets the number of data frames to be continuously received by the SPI. The SPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 4GB of data in a continuous transfer.

SPI_ENR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	enr Enables and disables all SPI operations. Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_SER

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	ser Slave enable register. The register enable the individual slave select output lines, 2 slave-select output pins are available. This register is valid only when SPI is configured as a master device.

SPI_BAUDR

Address: Operational Base + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	baudr SPI Clock Divider. This register is valid only when the SPI is configured as a master device. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fspi_clk/ SCKDV Where SCKDV is any even value between 2 and 65534. For example: for Fspi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2= 1.8432MHz

SPI_TXFTLR

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	txftlr When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

SPI_RXFTLR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rxftlr When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

SPI_TXFLR

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	txflr Contains the number of valid data entries in the transmit FIFO. (Note: When the bypass slave scph is 1, the master cannot provide redundant clocks according to the SPI protocol. Therefore, The actual value is the read value minus one.)

SPI_RXFLR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	rxflr Contains the number of valid data entries in the receive FIFO.

SPI_SR

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x1	ssi 1'b0: ss_in_n is low. 1'b1: ss_in_n is high.

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Bit	Attr	Reset Value	Description
5	RO	0x0	stb 1'b0: Slave tx not busy. 1'b1: Slave tx busy.
4	RO	0x0	rff 1'b0: Receive FIFO is not full. 1'b1: Receive FIFO is full.
3	RO	0x1	rfe 1'b0: Receive FIFO is not empty. 1'b1: Receive FIFO is empty.
2	RO	0x1	tfe 1'b0: Transmit FIFO is not empty. 1'b1: Transmit FIFO is empty.
1	RO	0x0	tff 1'b0: Transmit FIFO is not full. 1'b1: Transmit FIFO is full.
0	RO	0x0	bsf When set, indicates that a serial transfer is in progress; when cleared, indicates that the SPI is idle or disabled. 1'b0: SPI is idle or disabled. 1'b1: SPI is actively transferring data.

SPI_IPR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ipr Interrupt Polarity Register. 1'b0: Active Interrupt Polarity Level is HIGH. 1'b1: Active Interrupt Polarity Level is LOW.

SPI_IMR

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfim 1'b0: TX finish interrupt is masked. 1'b1: TX finish interrupt is not masked.
6	RW	0x0	sspim 1'b0: ss_in_n posedge interrupt is masked. 1'b1: ss_in_n posedge interrupt is not masked.
5	RW	0x0	toim 1'b0: spi timeout interrupt is masked. 1'b1: spi timeout interrupt is not masked.
4	RW	0x0	rffim 1'b0: spi_rxf_intr interrupt is masked. 1'b1: spi_rxf_intr interrupt is not masked.
3	RW	0x0	rfoim 1'b0: spi_rxo_intr interrupt is masked. 1'b1: spi_rxo_intr interrupt is not masked.
2	RW	0x0	rfuim 1'b0: spi_rxu_intr interrupt is masked. 1'b1: spi_rxu_intr interrupt is not masked.
1	RW	0x0	tfoim 1'b0: spi_txo_intr interrupt is masked. 1'b1: spi_txo_intr interrupt is not masked.

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Bit	Attr	Reset Value	Description
0	RW	0x0	tfeim 1'b0: spi_txe_intr interrupt is masked. 1'b1: spi_txe_intr interrupt is not masked.

SPI_ISR

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfis 1'b0: TX finish interrupt is not active after masking. 1'b1: TX finish interrupt is active after masking.
6	RW	0x0	sspis 1'b0: ss_in_n posedge interrupt is not active after masking. 1'b1: ss_in_n posedge interrupt is active after masking.
5	RW	0x0	tois 1'b0: spi timeout interrupt is not active after masking. 1'b1: spi timeout interrupt is active after masking.
4	RO	0x0	rffis 1'b0: spi_rxf_intr interrupt is not active after masking. 1'b1: spi_rxf_intr interrupt is full after masking.
3	RO	0x0	rfois 1'b0: spi_rxo_intr interrupt is not active after masking. 1'b1: spi_rxo_intr interrupt is active after masking.
2	RO	0x0	rfuis 1'b0: spi_rxu_intr interrupt is not active after masking. 1'b1: spi_rxu_intr interrupt is active after masking.
1	RO	0x0	tfois 1'b0: spi_txo_intr interrupt is not active after masking. 1'b1: spi_txo_intr interrupt is active after masking.
0	RO	0x0	tfeis 1'b0: spi_txe_intr interrupt is not active after masking. 1'b1: spi_txe_intr interrupt is active after masking.

SPI_RISR

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfris 1'b0: TX finish interrupt is not active prior to masking. 1'b1: TX finish interrupt is active prior to masking.
6	RW	0x0	sspris 1'b0: ss_in_n posedge interrupt is not active prior to masking. 1'b1: ss_in_n posedge interrupt is active prior to masking.
5	RW	0x0	toris 1'b0: spi_timeout interrupt is not active prior to masking. 1'b1: spi_timeout interrupt is active prior to masking.
4	RO	0x0	rffris 1'b0: spi_rxf_intr interrupt is not active prior to masking. 1'b1: spi_rxf_intr interrupt is full prior to masking.
3	RO	0x0	rforis 1'b0: spi_rxo_intr interrupt is not active prior to masking. 1'b1: spi_rxo_intr interrupt is active prior to masking.
2	RO	0x0	rfuris 1'b0: spi_rxu_intr interrupt is not active prior to masking. 1'b1: spi_rxu_intr interrupt is active prior to masking.

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Bit	Attr	Reset Value	Description
1	RO	0x0	tforis 1'b0: spi_txo_intr interrupt is not active prior to masking. 1'b1: spi_txo_intr interrupt is active prior to masking.
0	RO	0x1	tferis 1'b0: spi_txe_intr interrupt is not active prior to masking. 1'b1: spi_txe_intr interrupt is active prior to masking.

SPI_ICR

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	WO	0x0	ctxfi Write 1 to Clear tx finish Interrupt.
5	WO	0x0	csspi Write 1 to Clear ss_in_n posedge Interrupt.
4	WO	0x0	ctoi Write 1 to Clear Timeout Interrupt.
3	WO	0x0	ctfoi Write 1 to Clear Transmit FIFO Overflow Interrupt.
2	WO	0x0	crfoi Write 1 to Clear Receive FIFO Overflow Interrupt.
1	WO	0x0	crfui Write 1 to Clear Receive FIFO Underflow Interrupt.
0	WO	0x0	cci Write 1 to Clear Combined Interrupt.

SPI_DMACR

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	tde 1'b0: Transmit DMA disabled. 1'b1: Transmit DMA enabled.
0	RW	0x0	rde 1'b0: Receive DMA disabled. 1'b1: Receive DMA enabled.

SPI_DMATDLR

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	tdl This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and transmit DMA is enabled (DMACR[1] = 1).

SPI_DMARDLR

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	rdl This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and receive DMA is enabled(DMACR[0]=1).

SPI_VERSION

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x03110003	version IP version

SPI_TIMEOUT

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	dtsr DMA Timeout single request enable. 1'b0: DMA Timeout single request disable. 1'b1: DMA Timeout single request enable.
17	RW	0x0	tsb Timeout sclkcnt_bypass 1'b0: Timeout counter will be active after the first rising edge of sclk_in. 1'b1: Timeout counter will be active after the first rising edge of pclk.
16	RW	0x0	toe Timeout enable. 1'b0: Timeout counter is inactive. 1'b1: Timeout counter will be active after the first rising edge of sclk_in.
15:0	RW	0x0000	tov Timeout threshold value. If sclk_in keep inactive for a threshold time , timeout interrupt will be triggered .The timeout threshold time is TOV*pclk_period*16.

SPI_BYPASS

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	ckgen clock gating enable. 2'b00: no gating works. 2'b01: gating sclk for bypass module, when work at normal mode. 2'b10: gating spi_clk, when work at bypass mode. 2'b11: gating sclk and spi_clk, when spi is idle.
1	RW	0x0	txfie Bypass Slave TX Finish Interrupt Enable 1'b0: TX finish interrupt disable. 1'b1: TX finish interrupt enable.

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Bit	Attr	Reset Value	Description
0	RW	0x0	byen Bypass enable. 1'b0: Normal mode. 1'b1: Bypass mode, SPI serial/parallel convert logic is driven by SCLK.

SPI_BPENR

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	bpenr Enable and disable all SPI operations at bypass mode. Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_TXDR

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	WO	0x0000	txdr When it is written to, data are moved into the transmit FIFO.

SPI_RXDR

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rxdr When the register is read, data in the receive FIFO is accessed.

29.5 Interface Description

Table 29-1 SPI Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
IOMUX0			
spi0_sclk	I/O	GPIO0_C0	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[3:0] = 4'h2
spi0_mosi	I/O	GPIO0_C1	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[7:4] = 4'h2
spi0_miso	I/O	GPIO0_C2	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[11:8] = 4'h2
spi0_csn0	I/O	GPIO0_C3	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[15:12] = 4'h2
spi0_csn1	O	GPIO0_B7	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[15:12] = 4'h2
spi1_sclk	I/O	GPIO0_B0	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[3:0] = 4'h2
spi1_mosi	I/O	GPIO0_B1	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[7:4] = 4'h2
spi1_miso	I/O	GPIO0_B2	GPIO0_IOC_GPIO0B_IOMUX_SEL_0[11:8] = 4'h2
spi1_csn0	I/O	GPIO0_B6	GPIO0_IOC_GPIO0B_IOMUX_SEL_1[11:8] = 4'h2
spi1_csn1	O	GPIO0_A7	GPIO0_IOC_GPIO0A_IOMUX_SEL_1[15:12] = 4'h2

Notes: I=input, O=output, I/O=input/output.

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Table 29-2 SPI Rockchip Matrix IO Interface Description

Module Pin	Dir	Rockchip Matrix IO	IOMUX Setting
IOMUX1			
spi0_sclk	I/O	RM_I0	
spi0_mosi	I/O	RM_I0	
spi0_miso	I/O	RM_I0	
spi0_csn0	I/O	RM_I0	
spi0_csn1	O	RM_I0	
spi1_sclk	I/O	RM_I0	
spi1_mosi	I/O	RM_I0	
spi1_miso	I/O	RM_I0	
spi1_csn0	I/O	RM_I0	
spi1_csn1	O	RM_I0	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

29.6 Application Notes

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as:

When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})

When SPI Controller works as slave, the F_{spi_clk}>= 4 × (maximum F_{sclk_in})

When SPI Controller works as bypass slave, no frequency ratio restrictions

Master Transfer Flow

When configured as a serial-master device, the SPI initiates and controls all serial transfers. The serial bit-rate clock, generated and controlled by the SPI, is driven out on the sclk_out line. When the SPI is disabled (SPI_ENR = 0), no serial transfers can occur and sclk_out is held in "inactive" state, as defined by the serial protocol under which it operates.

Slave Transfer Flow

When the SPI is configured as a slave device, all serial transfers are initiated and controlled by the serial bus master.

When the SPI serial slave is selected during configuration, it enables its transmit data onto the serial bus. All data transfers to and from the serial slave are regulated on the serial clock line (sclk_in), driven from the serial-master device. Data are propagated from the serial slave on one edge of the serial clock line and sampled on the opposite edge.

Note that when the SPI works at bypass slave mode, since MISO and MOSI are directly driven by sclk_in, data can be received and transmit quickly, and spi_clk can be gated by configuring SPI_BYPASS[3:2].

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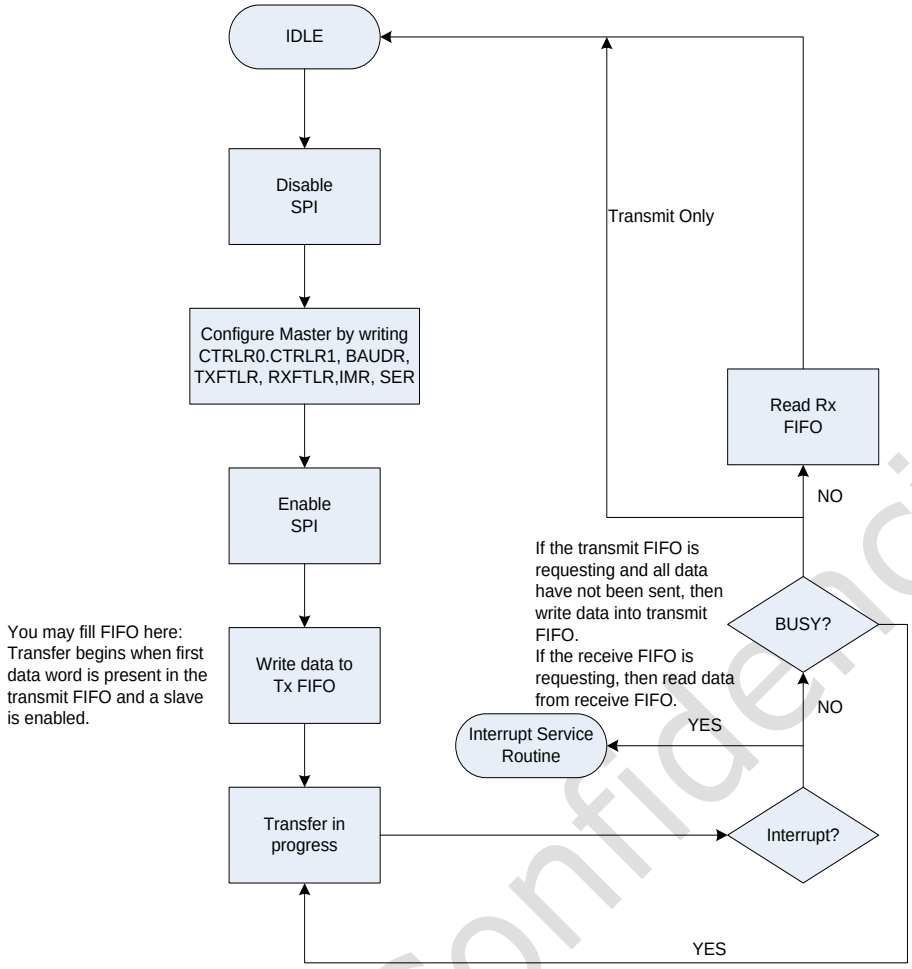

Fig. 29-7 SPI Master Transfer Flow Diagram

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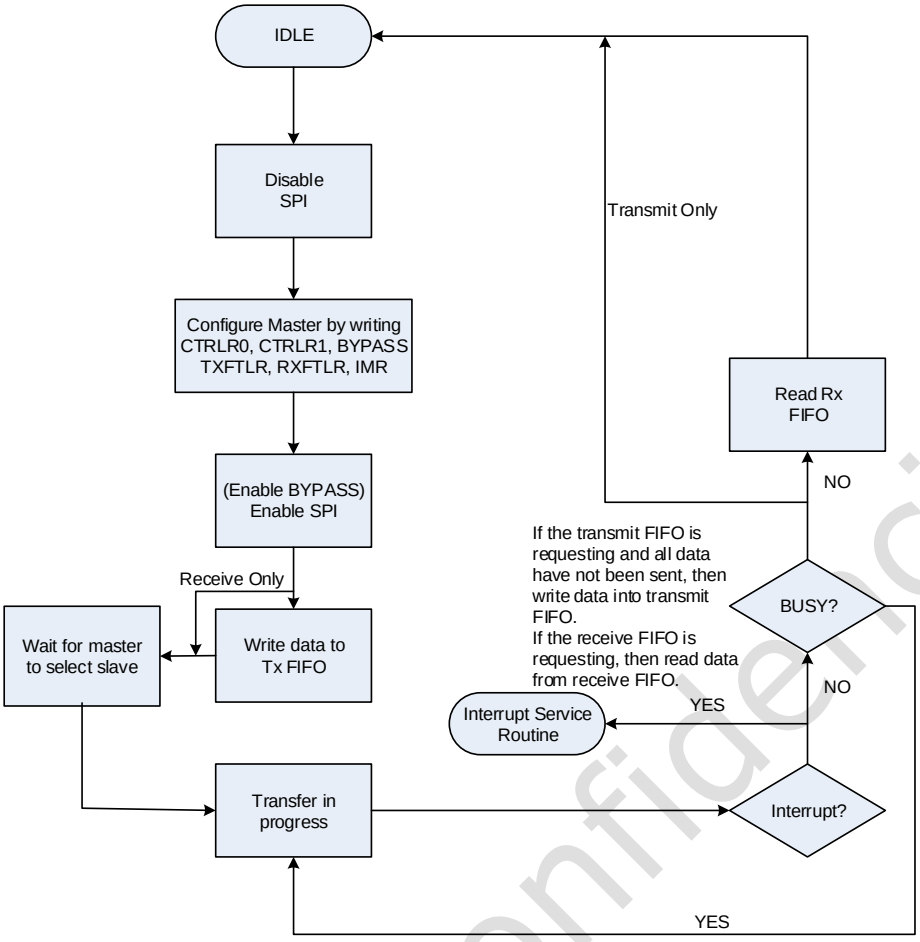

Fig. 29-8 SPI Slave Transfer Flow Diagram

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Chapter 30 SPI2APB

30.1 Overview

SPI2 is an alias for SPI2APB in this system. The SPI2APB module supports the following features:

- External SPI master can access the accessible address space in the chip through SPI2APB convertor
- Support two groups of registers in SGRF to control accessible address space in the chip
- A transaction states register and a message register can be read by external SPI master by query operation
- Two 32 bit registers can be written by external SPI master, and one of them can generate an interrupt after been written. This two register can be read by masters such as CPU and MCU

30.2 Block Diagram

The figure below shows SPI2APB block structure.

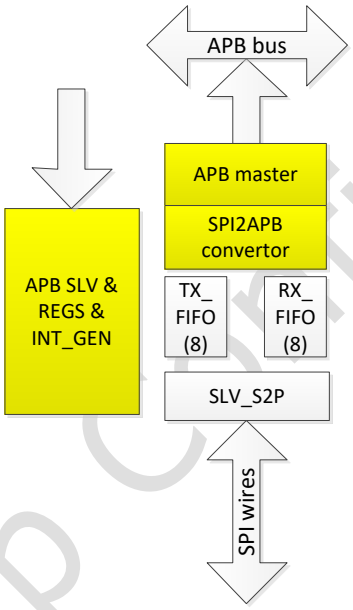

Fig. 30-1 SPI2APB Block Diagram

30.3 Function Description

30.3.1 Overview

SPI2APB convertor receives data from SPI wires, parses the command, and operates according to the protocol.

30.3.2 Protocol Description

SPI2APB supports four types of operation: Write, Read, Query and Write Message. By default, the command, address and data are all transferred in 32 bits packets in little endian, and the first bit to be transferred is the LSB. The operations begin at the negative edge of CS and end at the positive edge of CS. Between two operation, CS should keep high for a time longer than one SCLK period.

Write

External SPI master should dessert CS firstly. The Write command, address and data packets should be transferred according to the order of the figure. The first data (data0 in the Fig. 30-2) will be written to the address ADDR, the second data will be written to the address ADDR+4, and so on. External SPI master can terminate the write operation by setting the CS to high level.

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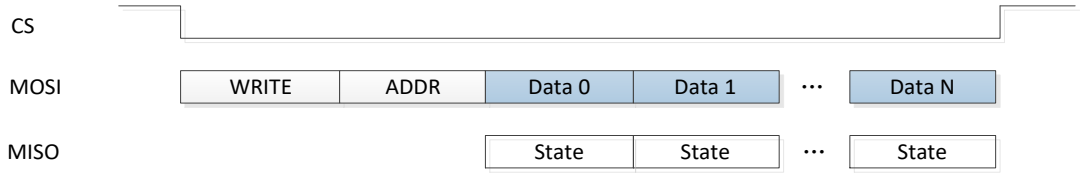

Fig. 30-2 Write Operation

Read

After receiving READ command and address, the convertor will read N data from the address and push the data into the RD_FIFO (N is a parameter in READ command). Dummy packets can be insert to ensure there is available data in the RD_FIFO. When SPI master is ready to receive data, it should send a RD_BEGIN command packet. The first packets following RD_BEGIN packets (data0 in the Fig. 30-3) is the data read from address ADDR, the second packets is the data read from address ADDR+4, and so on. After N data packets has been transferred, SPI2APB will begin to transfer state information.

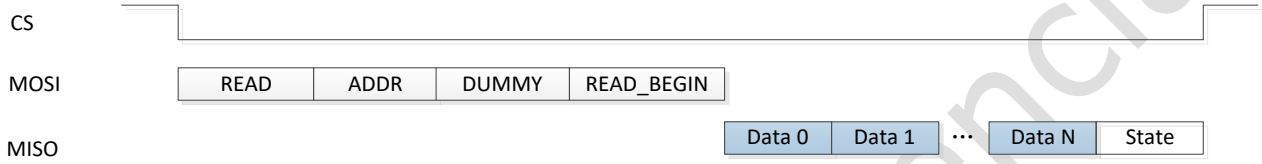

Fig. 30-3 Read Operation

Query

There are two registers can be queried: State Register and Message Register 2. State register contains transfer state information such as whether the transfer is complete or not, detail is showed in the Table 30-1. Message Register 2 can be written by DSP. The query result is immediately following the query command without delay.

Fig. 30-4 Query Operation

Table 30-1 State Register Information

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Bit	Attr	Reset Value	Description
31:16	RW	0x1608	Chip ID
15:11	RW	0x0	reserved
10	RW	0x0	pre_err Error response is received when APB master is doing pre-read transaction.
9	RW	0x0	rd_udflw Read FIFO is underflow.
8	RW	0x0	rd_err Data with error response has been transmitted.
7:4	RW	0x0	reserved
3	RW	0x0	trans_cfl Transaction conflict. Previous transaction is unfinished and new transaction is launched by SPI master.
2	RW	0x0	trans_unfi Transaction is unfinished.
1	RW	0x0	wr_ovfl Write FIFO is overflow
0	RW	0x0	wr_err Error response is received when APB master is writing

Write Message

There are two message registers can be written by external SPI master: Message Register 0 and Message Register 1. These two registers can be read by DSP. After Message Register 1 has been written, an interrupt will be generated.

The control register (CTRL0) can be written by using this command too.

Fig. 30-5 Write Message Operation

Command Encoding

All command are 32bits.

Table 30-2 Command Encoding Information

Command	Format	Description
READ	0x0077+(PRE_NUM <<16)	PRE_NUM is pre_read number. For example, 0x00100077 indicates pre_read number is 16. If PRE_NUM is 0, convertor will read data when RD_FIFO is not full and read transaction is not terminated.
READ_BEGIN	0x000000aa	Command for read begin.
WRITE	0x00000011	Command for write data.
WRITE MESSAGE (Message Reg0)	0x00010011	Write message register 0.
WRITE MESSAGE (Message Reg1)	0x00020011	Write message register 1 will generate an interrupt.
WRITE MESSAGE (CTRL0)	0x00030011	Write the ctrl0 register.

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Command	Format	Description
QUERY (State)	0x000000ff	Query the state register.
QUERY (Message Register 2)	0x000001ff	Query the message register 2

30.4 Register Description

30.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SPI2APB	0xff4c0000

30.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI2APB_CTRL0	0x0000	W	0x00000000	Control Register 0
SPI2APB_SR	0x0024	W	0x00000014	SPI2APB status
SPI2APB_IMR	0x002C	W	0x00000000	Interrupt Mask
SPI2APB_RISR	0x0034	W	0x00000000	Raw Interrupt Status
SPI2APB_ICR	0x0038	W	0x00000000	Interrupt Clear
SPI2APB_VERSION	0x0048	W	0x063B0002	Version
SPI2APB_QUICK_REG0	0x0050	W	0x00000000	Quick Write Register0
SPI2APB_QUICK_REG1	0x0054	W	0x00000000	Quick Write Register1
SPI2APB_QUICK_REG2	0x0058	W	0x00000000	Quick Read Register2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

30.4.3 Detail Registers Description

SPI2APB_CTRL0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TXCP 1'b0: TX clock is not inverted 1'b1: TX clock is inverted
2	RW	0x0	RXCP 1'b0: RX clock is not inverted 1'b1: RX clock is inverted
1	RW	0x0	EM Serial endian mode can be configured by this bit. APB endian mode is always little endian. 1'b0: little endian 1'b1: big endian
0	RW	0x0	FBM 1'b0: first bit is LSB 1'b1: first bit is MSB

SPI2APB_SR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x1	RFE 1'b0: Receive FIFO is not empty 1'b1: Receive FIFO is empty

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Bit	Attr	Reset Value	Description
3	RO	0x0	RFF 1'b0: Receive FIFO is not full 1'b1: Receive FIFO is full
2	RO	0x1	TFE 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty
1	RO	0x0	TFF 1'b0: Transmit FIFO is not full 1'b1: Transmit FIFO is full
0	RO	0x0	BSF When set, indicates that the ss_in signal is active low. 1'b0: ss_in is not active 1'b1: ss_in is active low

SPI2APB_IMR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	QWIM 1'b0: spi2apb reg1 quick write interrupt is masked 1'b1: spi2apb reg1 quick write interrupt is not masked

SPI2APB_RISR

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	QWRIS 1'b0: spi2apb reg1 quick write interrupt is not active 1'b1: spi2apb reg1 quick write interrupt is active

SPI2APB_ICR

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	CQWI Write 1 to clear spi2apb quick write reg1 interrupt

SPI2APB_VERSION

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x063b0002	VER Version

SPI2APB_QUICK_REG0

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	QWV0 SPI master write to this register, and CPU read it.

SPI2APB_QUICK_REG1

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	QWV1 SPI master write to this register, generate a interrupt, and CPU read it.

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SPI2APB_QUICK_REG2

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	QRV CPU write a value to this register, and SPI master read it.

30.5 Interface Description

Table 30-3 SPI0 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
SPI2_CSN	I/O	GPIO2_B1	GPIO2_IOC_GPIO2B_IOMUX_SEL_0 [7:4]=4'h2
SPI2_CLK	I/O	GPIO2_B0	GPIO2_IOC_GPIO2B_IOMUX_SEL_0 [3:0]=4'h2
SPI2_MOSI	I/O	GPIO2_B2	GPIO2_IOC_GPIO2B_IOMUX_SEL_0 [11:8]=4'h2
SPI2_MISO	I/O	GPIO2_B3	GPIO2_IOC_GPIO2B_IOMUX_SEL_0 [15:12]=4'h2

Notes: I=input, O=output, I/O=input/output.

30.6 Application Notes

1. External SPI master should query the transaction state after every write and read operation to ensure the operation is completed correctly.
2. The frequency of clock for APB should be higher or equal to the frequency of SCLK_IN.

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Chapter 31 Pulse Width Modulation (PWM)

31.1 Overview

The Pulse-Width Modulator (PWM) provides a way to generate a pulse periodic waveform for motor control, it can also act as a digital-to-analog converter with some external components.

The PWM Module supports the following common features:

- Support input capture mode
  - Support measures the high/low polarity effective cycles of input waveform
  - Support generates an interrupt at the transition of input waveform polarity
  - Support a 32-bits high polarity capture counter
  - Support a 32-bits low polarity capture counter
  - Support an input filter to remove glitch
- Support continuous mode and one-shot output mode
  - Support a 32-bits period counter
  - Support a 32-bits duty counter
  - Support configure the polarity in inactive state and duty cycle
  - Support center or left aligned mode
  - Support a 16-bit first dimensional repeat counter and an interrupt for reload operation
  - Support a 16-bit second dimensional repeat counter and an interrupt for one-shot operation
  - Support global synchronization of various channels
- Supports two-stage frequency division of working clock

RK3506 support two PWM controllers, they support some individual feature as following:

- PWM0
  - Support 4 channels
  - Support power key capture mode
  - Support generates waveform through lookup table
- PWM1
  - Support 8 channels
  - Support biphasic counter
  - Support clock frequency meter
  - Support clock counter
  - Support IR transmission in NEC with full repeat, NEC with simple repeat, TC9012 or SONY mode

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31.2 Block Diagram

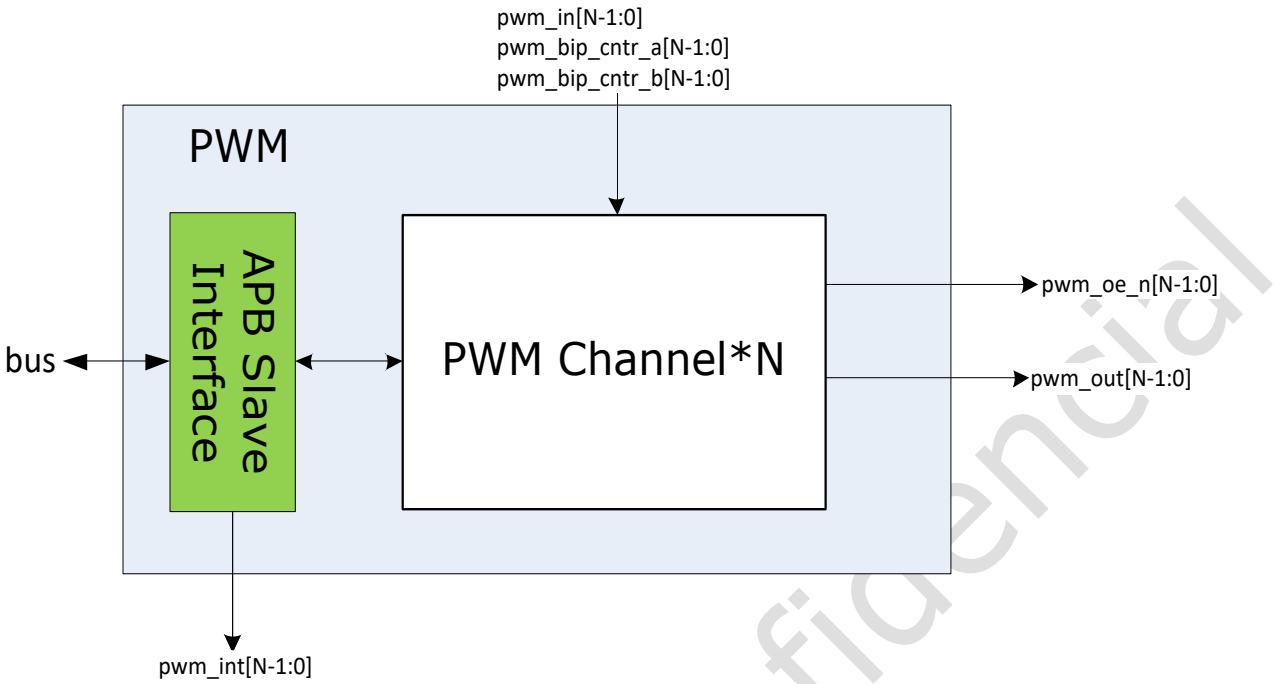

Fig. 31-1 PWM Block Diagram

The host processor gets access to PWM register through the APB slave interface with 32-bit bus width. PWM controller support 1~8 channels, and the offset address of each channel is 4k-byte as interval. PWM supports one interrupt for each channel, user should refer to interrupt register to know the raw interrupt status when an interrupt is asserted.

31.3 Function Description

The PWM supports three operation modes: capture mode, one-shot mode and continuous mode. For the one-shot mode and the continuous mode, the PWM output can be configured as the left-aligned mode or the center-aligned mode.

PWM also supports some additional function, such as clock counter, clock frequency meter and biphasic Counter.

31.3.1 Capture Mode

The capture mode is used to measure the PWM channel input waveform high/low effective cycles with the PWM channel clock and asserts an interrupt when the polarity of the input waveform changes. The number of the high effective cycles is recorded in the PWM_HPC register, while the number of the low effective cycles is recorded in the PWM_LPC register.

Notes: the PWM input waveform is doubled buffered when the PWM channel is working in order to filter unexpected shot-time polarity transition, and therefore the interrupt is asserted several cycles after the input waveform polarity changes, and so does the change of the values of PWM_HPC and PWM_LPC.

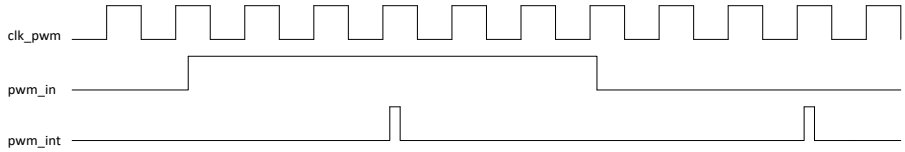

Fig. 31-2 PWM Capture Mode

The PWM supports 32-bits power key capture mode. User can configure 16 power keys to match, the interrupt will be asserted when the capture value matches any one.

31.3.2 Continuous Mode

In continuous mode, the PWM channel generates a series of the pulses continuously as expected once the channel is enabled. It supports left-aligned mode or center-aligned mode.

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For the left-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWM_CTRL.duty_pol). Once duty cycle number (PWM_DUTY) is reached, the output is switched to the opposite polarity. After the period number (PWM_PERIOD) is reached, the output is again switched to the opposite polarity to start another period of desired pulse.

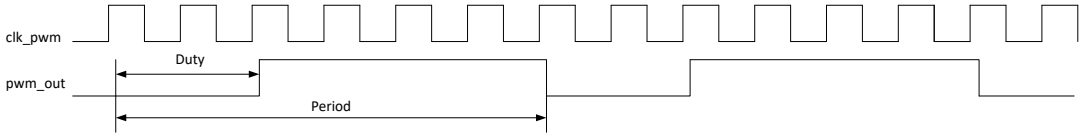

Fig. 31-3 PWM Continuous Left-aligned Output Mode

For the center-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWM_CTRL.duty_pol). Once one half of duty cycle number (PWM_DUTY) is reached, the output is switched to the opposite polarity. Then if there is one half of duty cycle left for the whole period, the output is again switched to the opposite polarity. Finally, after the period number (PWM_PERIOD) is reached, the output starts another period of desired pulse.

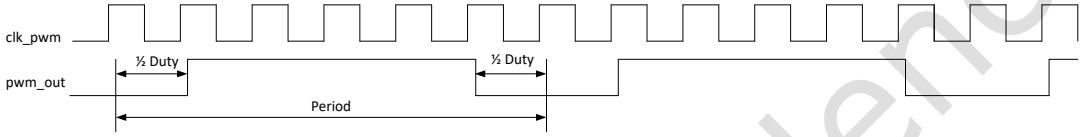

Fig. 31-4 PWM Continuous Center-aligned Output Mode

PWM support a 16 bits first dimensional repeat counter. A reload interrupt is generated every N+1 periods of the waveform when PWM_RPT.rpt_first_dimensional is configured to N. User can update the duty and period configuration for next N+1 periods when receive the interrupt.

PWM also support generates waveform through lookup table, the duty and period can be updated by lookup table automatic every N+1 periods of the waveform.

Continuous mode will generate the waveform continuously until disabled by user. It's will fix to inactive polarity (PWM_CTRL.inactive_pol) when it's disabled.

31.3.3 One-shot Mode

In one-shot mode, the PWM channel generates limited periods of waveforms.

In addition to the first dimensional repeat counter, it also supports a 16 bits second dimensional repeat counter. PWM channel will stop and assert an interrupt after second dimensional counter reach M+1 when PWM_RPT.rpt_second_dimensional is configured to M. The total waveform periods are (N + 1) multi by (M + 1).

The reload interrupt and lookup table is also supported in one-shot mode.

The left-aligned and the center-aligned is also supported in one-shot mode.

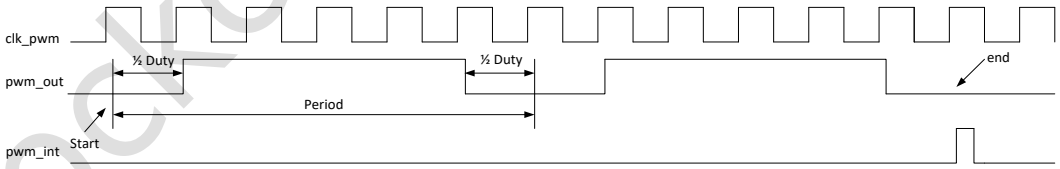

Fig. 31-5 PWM One-shot Center-aligned Output Mode

31.3.4 Clock Counter

PWM support a 64-bits counter which clock can select from any PWM channel input and a clock from system CRU.

31.3.5 Clock Frequency Meter

PWM support a 32-bits frequency meter which clock can select from any PWM channel input and a clock from system CRU. It supports a reference clock and timer to schedule a period time, user can calculate the frequency by getting the counter value that counted by the measured clock in the period time.

31.3.6 Biphasic Counter

PWM supports biphasic counter which uses two IO to compose an A/B phase channel.

PWM1 controller support 7 channel biphasic counters.

For channel 0~channel5, the A phase is from PWM1_BIP_CNTR_A0~A5 (RM_IO), the B

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phase is from PWM1_BIP_CNTR_B0~B5 (RM_IO).
For channel 6, the A phase is from PWM1_CH6 (RM_IO), the B phase is from PWM1_CH7 (RM_IO). The biphasic counter register is only located at PWM1_CH6. User only needs to configure the IOMUX of PWM1_CH7.
Biphasic counter support 5 modes as following:

- Mode 0: Single phase increase mode with A-phase.

When A-phase input is OFF->ON, the count increases by 1. In this mode, it can be used as clock frequency meter or clock counter.

- Mode 1: Single phase increase/decrease mode with A-phase.

When the B-phase input is OFF and the A-phase input is OFF->ON, the count increases by 1.
When the B-phase input is ON and the A-phase input is OFF->ON, the count decreases by 1.

- Mode 2: Dual phase with A/B-phase mode.

When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1.

- Mode 3: Dual phase with A/B-phase 2 times frequency mode.

When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1.
When the A-phase input is OFF and the B-phase input is ON->OFF, the count increases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1.
When the A-phase input is OFF and the B-phase input is OFF ->ON, the count decreases by 1.

- Mode 4: Dual phase with A/B-phase 4 times frequency mode.

When the input of phase B is OFF and phase A is OFF->ON, the count increases by 1.
When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1.
When the input of phase B is ON and phase A is ON->OFF, the count increases by 1.
When the A-phase input is OFF and the B-phase input is ON_.OFF, the count increases by 1.
When the A-phase input is OFF and the B-phase input is OFF->ON, the count decreases by 1.
When the input of phase B is ON and phase A is OFF->ON, the count decreases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1.
When the input of phase B is OFF and the input of phase A is ON->OFF, the count decreases by 1.

31.4 Register Description

31.4.1 Internal Address Mapping

Slave address can be divided into different length for different controller, which is shown as follows.

Operational Base

Name	Base Address
PWM0	0xFF930000
PWM1	0xFF170000

Slave address can be divided into different length for different channels in one controller, which is shown as follows.

Table 31-1 PWM Channel Address Map

Channel	Offset Address
Channel 0	0x0000

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Channel 1	0x1000
Channel 2	0x2000
Channel 3	0x3000
Channel 4	0x4000
Channel 5	0x5000
Channel 6	0x6000
Channel 7	0x7000

31.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PWM_VERSION_ID	0x0000	W	0x04000044	Version ID Register
PWM_ENABLE	0x0004	W	0x00000000	Enable Register
PWM_CLK_CTRL	0x0008	W	0x00000000	Clock Control Register
PWM_CTRL	0x000C	W	0x00000000	Control Register
PWM_PERIOD	0x0010	W	0x00000000	Period Register
PWM_DUTY	0x0014	W	0x00000000	Duty Register
PWM_OFFSET	0x0018	W	0x00000000	Output Offset Register
PWM_RPT	0x001C	W	0x00000000	Repeat Register
PWM_FILTER_CTRL	0x0020	W	0x00000000	Filter Control Register
PWM_CNT	0x0024	W	0x00000000	Counter Register
PWM_ENABLE_DELAY	0x0028	W	0x00000000	Enable Delay Register
PWM_HPC	0x002C	W	0x00000000	High Polarity Capture Register
PWM_LPC	0x0030	W	0x00000000	Low Polarity Capture Register
PWM_BIPHASIC_COUNTER_CTRL0	0x0040	W	0x00000000	Biphasic counter control 0 register
PWM_BIPHASIC_COUNTER_CTRL1	0x0044	W	0x00000000	Biphasic counter control 1 register
PWM_BIPHASIC_COUNTER_TIMER_VALUE	0x0048	W	0x00000000	Biphasic counter timer value register
PWM_BIPHASIC_COUNTER_RESULT_VALUE	0x004C	W	0x00000000	Biphasic counter result value register
PWM_BIPHASIC_COUNTER_RESULT_VALUE_SYNC	0x0050	W	0x00000000	Biphasic counter result value register
PWM_INTSTS	0x0070	W	0x00000000	Interrupt Status Register
PWM_INT_EN	0x0074	W	0x00000000	Interrupt Enable Register
PWM_INT_MASK	0x0078	W	0x00000000	Interrupt Mask Register
PWM_WAVE_MEM_ARBITER	0x0080	W	0x00000000	Waveform Generator Memory Arbiter Register
PWM_WAVE_MEM_STATUS	0x0084	W	0x00000000	Waveform Generator Memory Status Register
PWM_WAVE_CTRL	0x0088	W	0x00000010	Waveform Generator control register
PWM_WAVE_MAX	0x008C	W	0x00000000	Waveform Generator maximum register

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Name	Offset	Size	Reset Value	Description
PWM_WAVE_MIN	0x0090	W	0x00000000	Waveform Generator minimum register
PWM_WAVE_OFFSET	0x0094	W	0x00000000	Waveform Generator offset register
PWM_WAVE_MIDDLE	0x0098	W	0x00000000	Waveform Generator middle register
PWM_WAVE_HOLD	0x009C	W	0x00000000	Waveform Generator hold register
PWM_GLOBAL_ARBITER	0x00C0	W	0x00000000	Global Arbiter Register
PWM_GLOBAL_CTRL	0x00C4	W	0x00000000	Global Control Register
PWM_PWRMATCH_ARBITER	0x0100	W	0x00000000	Power Key Match Arbiter Register
PWM_PWRMATCH_CTRL	0x0104	W	0x00000000	Power Key Match Control Register
PWM_PWRMATCH_LPRE	0x0108	W	0x238C22C4	Power Key Match of Low Preload Register
PWM_PWRMATCH_HPRE	0x010C	W	0x11F81130	Power Key Match of High Preload Register
PWM_PWRMATCH_LD	0x0110	W	0x029401CC	Power Key Match of Low Data Register
PWM_PWRMATCH_HD_ZERO	0x0114	W	0x029401CC	Power Key Match of High Data for Zero Register
PWM_PWRMATCH_HD_ONE	0x0118	W	0x06FE0636	Power Key Match of High Data for One Register
PWM_PWRMATCH_VALUE0	0x011C	W	0x00000000	Power Key Match Value 0 Register
PWM_PWRMATCH_VALUE1	0x0120	W	0x00000000	Power Key Match Value 1 Register
PWM_PWRMATCH_VALUE2	0x0124	W	0x00000000	Power Key Match Value 2 Register
PWM_PWRMATCH_VALUE3	0x0128	W	0x00000000	Power Key Match Value 3 Register
PWM_PWRMATCH_VALUE4	0x012C	W	0x00000000	Power Key Match Value 4 Register
PWM_PWRMATCH_VALUE5	0x0130	W	0x00000000	Power Key Match Value 5 Register
PWM_PWRMATCH_VALUE6	0x0134	W	0x00000000	Power Key Match Value 6 Register
PWM_PWRMATCH_VALUE7	0x0138	W	0x00000000	Power Key Match Value 7 Register
PWM_PWRMATCH_VALUE8	0x013C	W	0x00000000	Power Key Match Value 8 Register
PWM_PWRMATCH_VALUE9	0x0140	W	0x00000000	Power Key Match Value 9 Register
PWM_PWRMATCH_VALUE10	0x0144	W	0x00000000	Power Key Match Value 10 Register

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Name	Offset	Size	Reset Value	Description
PWM_PWRMATCH_VALUE11	0x0148	W	0x00000000	Power Key Match Value 11 Register
PWM_PWRMATCH_VALUE12	0x014C	W	0x00000000	Power Key Match Value 12 Register
PWM_PWRMATCH_VALUE13	0x0150	W	0x00000000	Power Key Match Value 13 Register
PWM_PWRMATCH_VALUE14	0x0154	W	0x00000000	Power Key Match Value 14 Register
PWM_PWRMATCH_VALUE15	0x0158	W	0x00000000	Power Key Match Value 15 Register
PWM_PWRCAPTURE_VALUE	0x015C	W	0x00000000	Power Key Capture Value Register
PWM_IR_TRANS_ARBITER	0x0180	W	0x00000000	Power Key Match Control Register
PWM_IR_TRANS_CTRL0	0x0184	W	0x00001F00	IR Transmission control 0 register
PWM_IR_TRANS_CTRL1	0x0188	W	0x00000000	IR Transmission control 1 register
PWM_IR_TRANS_PRE	0x018C	W	0x11942328	IR transmission preload period
PWM_IR_TRANS_SPRE	0x0190	W	0x000008CA	IR transmission simple preload low period
PWM_IR_TRANS_LD	0x0194	W	0x00000230	IR Trans Out Data Low Period
PWM_IR_TRANS_HD	0x0198	W	0x069A0230	IR Trans Out High Period
PWM_IR_TRANS_BURST_FRAME	0x019C	W	0x2261A5E0	IR transmission frame and burst period
PWM_IR_TRANS_DATA_VALUE	0x01A0	W	0x00000000	IR Trans Output Data Value
PWM_IR_TRANS_STATUS	0x01A4	W	0x00000001	IR Trans Status
PWM_FREQ_ARBITER	0x01C0	W	0x00000000	Frequency Meter Arbiter Control Register
PWM_FREQ_CTRL	0x01C4	W	0x00000000	Frequency Meter control register
PWM_FREQ_TIMER_VALUE	0x01C8	W	0x00000000	Frequency Meter timer value register
PWM_FREQ_RESULT_VALUE	0x01CC	W	0x00000000	Frequency Meter result value register
PWM_COUNTER_ARBITER	0x0200	W	0x00000000	Counter Arbiter Control Register
PWM_COUNTER_CTRL	0x0204	W	0x00000000	Counter control register
PWM_COUNTER_LOW	0x0208	W	0x00000000	Counter Low register
PWM_COUNTER_HIGH	0x020C	W	0x00000000	Counter High register
PWM_WAVE_MEM	0x0400	W	0x00000000	Waveform Generator Memory Arbiter Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

31.4.3 Detail Registers Description

PWM_VERSION_ID

Address: **Operational Base** + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:24	RO	0x04	main_version Main version
23:16	RO	0x00	minor_version Minor version
15	RO	0x0	reserved
14	RO	0x0	biphasic_counter_support Biphasic counter support
13	RO	0x0	filter_support Filter support
12	RO	0x0	wave_support Waveform generator support
11	RO	0x0	counter_support Counter support
10	RO	0x0	freq_meter_support Frequency meter support
9	RO	0x0	power_key_support Power key support
8	RO	0x0	ir_trans_support IR transmission support
7:4	RO	0x4	channel_index Channel index
3:0	RO	0x4	channel_num_support Channel number support

PWM_ENABLE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	pwm_cnt_rd_en PWM channel CNT read enable. The CNT can be read for debug. 1'b0: Disabled 1'b1: Enabled
4	W1T	0x0	pwm_global_join_en PWM join global control enable. When this bit is set to 1, the PWM channel is enabled by pwm_global_en instead of pwm_en, and the following register can be updated at the posedge of pwm_global_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET

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Bit	Attr	Reset Value	Description
3	RW	0x0	force_clk_en 1'b0: Disabled, when PWM channel is inactive state, the clk_pwm to PWM Clock pre-scale module is blocked to reduce power consumption. 1'b1: Enabled, the clk_pwm to PWM Clock pre-scale module is always enabled.
2	W1T	0x0	pwm_ctrl_update_en PWM control update enable. The bit will be auto cleaned. The following register can be updated at the posedge of pwm_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET
1	RW	0x0	pwm_en PWM enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.
0	RW	0x0	pwm_clk_en PWM clock enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_CLK_CTRL

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_global_sel Clock global selection 1'b0: Select current channel scale clock 1'b1: Select global channel scale clock
14:13	RW	0x0	clk_src_sel Clock source selection 2'b00: Select clk_pwm as root clock source, Clock is from PLL and the frequency can be configured. 2'b01: Select clk_pwm_osc as root clock source, Clock is from crystal oscillator and the frequency is fixed. 2'b10: Select clk_pwm_rc as root clock source, Clock is from RC oscillator and the frequency is fixed.

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Bit	Attr	Reset Value	Description
12:4	RW	0x000	scale This field defines the scale factor applied to pre-scaled clock. The value N means the clock is divided by 2*N. it is valid from 1~256.
3	RO	0x0	reserved
2:0	RW	0x0	prescale This field defines the pre-scale factor applied to input clock. The value N means that the input clock is divided by 2^N.

PWM_CTRL

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8:6	RW	0x0	pwm_in_sel PWM in channel selection, the default value is corresponding channel, User can configure to another channel. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5 3'b110: PWM channel 6 3'b111: PWM channel 7
5	RW	0x0	aligned_vld_n 0: Aligned Mode Valid 1: Aligned Mode Invalid
4	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
3	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive

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Bit	Attr	Reset Value	Description
2	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
1:0	RW	0x0	pwm_mode 2'b00: One shot mode, PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt. 2'b01: Continuous mode, PWM produces the waveform continuously. 2'b10: Capture mode, PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved

PWM_PERIOD

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD This value defines the period of the output waveform for continuous mode or one-shot mode. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is considered and bit [0] always considered as 0.

PWM_DUTY

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY This value defines the duty cycle of the output waveform for continuous mode or one-shot mode. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is considered.

PWM_OFFSET

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	channel_output_offset If PWM is operated at the continuous mode or one-shot mode, this value defines the offset of the output waveform. This value is based on the PWM clock. The value ranges from 0 to (period-duty). This register takes effective when output aligned mode is invalid.

PWM_RPT

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Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rpt_second_dimensional This field defines the second dimensional repeated effective periods of output waveform. It can be used only in one-shot mode. The second dimensional waveform counter will increase 1 when first dimensional waveform counter reach rpt_first_dimensional. When reach rpt_second_dimensional, the PWM channel will be disabled and the one-shot interrupt will be asserted. The value N means N+1 repeated effective periods. The total waveform number will be (rpt_first_dimensional+1) multiply by (rpt_second_dimensional+1).
15:0	RW	0x0000	rpt_first_dimensional This field defines the first dimensional repeated effective periods of output waveform. When reach rpt_first_dimensional, the waveform counter will wrap back to 0 and restart counting and the reload interrupt will be asserted. User can update the configuration in the interrupt. It can be used in one-shot mode and Continuous mode. The value N means N+1 repeated effective periods.

PWM_FILTER_CTRL

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:4	RW	0x00	filter_number Filter window number
3:1	RO	0x0	reserved
0	RW	0x0	filter_enable 1'b0: Disabled 1'b1: Enabled

PWM_CNT

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_ENABLE_DELAY

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Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	pwm_enable_delay PWM enable delay

PWM_HPC

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HPC This value indicates the effective high polarity cycles of input waveform for capture mode. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_LPC

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LPC This value indicates the effective low polarity cycles of input waveform for capture mode. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_BIPHASIC_COUNTER_CTRL0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	biphasic_counter_mode0_edge_sel biphasic counter phase edge selection for mode 0 1'b0: Posedge 1'b1: Negedge
8	RW	0x0	biphasic_counter_clk_force_en Biphasic counter clock force enable
7	W1T	0x0	biphasic_counter_sync_en Biphasic counter synchronous enable

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Bit	Attr	Reset Value	Description
6	W1T	0x0	timer_clk_switch_mode Timer clock switch mode, it can set to 1'b1 only when biphasic_counter_mode is mode0. 1'b0: Normal mode 1'b1: Switch timer clock and measured clock. It can be used to provide testing accuracy or reduce testing time when the frequency of measured clock is low. It can also be used in scenarios where the start time of the measured clock is uncertain
5:3	RW	0x0	biphasic_counter_mode Biphasic counter mode 3'h0: Mode0 3'h1: Mode1 3'h2: Mode2 3'h3: Mode3 3'h4: Mode4 Other: Reserved
2	RW	0x0	biphasic_counter_clk_sel Biphasic counter clock selection 1'b0: Select clk_pwm, clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_osc, clock is from crystal oscillator and the frequency is fixed.
1	RW	0x0	biphasic_counter_continuous_mode Biphasic counter continuous mode
0	W1T	0x0	biphasic_counter_en Biphasic counter enable.

PWM_BIPHASIC_COUNTER_CTRL1

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:4	RW	0x00	biphasic_counter_filter_number Filter window number
3:1	RO	0x0	reserved
0	RW	0x0	biphasic_counter_filter_enable 1'b0: Disabled 1'b1: Enabled

PWM_BIPHASIC_COUNTER_TIMER_VALUE

Address: **Operational Base** + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	biphasic_counter_timer_value Biphasic counter timer value, the unit is one cycle of biphasic counter timer clock.

PWM_BIPHASIC_COUNTER_RESULT_VALUE

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	biphasic_counte_result_value Biphasic counter result value, it can read only after interrupt biphasic_counter_intsts is asserted.

PWM_BIPHASIC_COUNTER_RESULT_VALUE_SYNC

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	biphasic_counte_result_value_sync Biphasic counter result value with synchronized processing, it can read in real time when biphasic_counter_sync_en is set to 1.

PWM_INTSTS

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	W1C	0x0	biphasic_counter_intsts Biphasic counter interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
8	W1C	0x0	wave_middle_intsts Waveform address access middle address value interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
7	W1C	0x0	wave_max_intsts Waveform address access maximum address interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
6	W1C	0x0	it_trans_end_intsts IR Transmission end interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
5	W1C	0x0	pwr_intsts Power key match interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated

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Bit	Attr	Reset Value	Description
4	W1C	0x0	freq_intsts Frequency meter interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
3	W1C	0x0	reload_intsts Reload interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
2	W1C	0x0	oneshot_end_intsts Waveform end interrupt status for one-shot mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated
1	W1C	0x0	cap_hpc_intsts HPC interrupt status for capture mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated
0	W1C	0x0	cap_lpc_intsts LPC interrupt status for capture mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated

PWM_INT_EN

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	biphasic_couner_int_en Biphasic counter interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
8	RW	0x0	wave_middle_int_en Waveform address access middle address enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
7	RW	0x0	wave_max_int_en Waveform address access maximum address interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
6	RW	0x0	it_trans_end_int_en IR Transmission end interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled

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Bit	Attr	Reset Value	Description
5	RW	0x0	pwr_int_en Power key match interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
4	RW	0x0	freq_int_en Frequency meter interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
3	RW	0x0	reload_int_en Reload interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
2	RW	0x0	oneshot_end_int_en Waveform end interrupt enable for one-shot mode. 1'b0: Interrupt disabled 1'b1: Interrupt enabled
1	RW	0x0	cap_hpc_int_en HPC interrupt enable for capture mode 1'b0: Interrupt disabled 1'b1: Interrupt enabled
0	RW	0x0	cap_lpc_int_en LPC interrupt enable for capture mode 1'b0: Interrupt disabled 1'b1: Interrupt enabled

PWM_INT_MASK

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	biphasic_counter_int_mask Biphasic counter interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
8	RW	0x0	wave_middle_int_mask Waveform address access middle address mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
7	RW	0x0	wave_max_int_mask Waveform address access maximum address interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
6	RW	0x0	it_trans_end_int_mask IR Transmission end interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
5	RW	0x0	pwr_int_mask Power key match interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
4	RW	0x0	freq_int_mask Frequency meter interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
3	RW	0x0	reload_Int_mask Reload interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
2	RW	0x0	oneshot_end_mask Waveform end interrupt mask for one-shot mode. 1'b0: Interrupt not mask 1'b1: Interrupt mask
1	RW	0x0	cap_hpc_int_mask HPC interrupt mask for capture mode 1'b0: Interrupt not mask 1'b1: Interrupt mask
0	RW	0x0	cap_lpc_int_mask LPC interrupt mask for capture mode 1'b0: Interrupt not mask 1'b1: Interrupt mask

PWM_WAVE_MEM_ARBITER

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	wave_mem_read_lock Each bit controls the read lock of waveform generator memory. Once one channel obtains arbitration, other channels cannot read waveform generator memory. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	wave_mem_grant Each bit controls the grant of waveform generator memory for one channel. Once one channel obtains arbitration, other channels cannot write waveform generator memory. 1'b0: Don't Grant 1'b1: Grant

PWM_WAVE_MEM_STATUS

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	access_done Indicate the access to waveform generator memory is done.

PWM_WAVE_CTRL

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RW	0x00	wave_period_amplify Waveform generator table period value amplify, the value N means amplify by 2^N.
10:6	RW	0x00	wave_duty_amplify Waveform generator table duty value amplify, the value N means amplify by 2^N.
5:4	RW	0x1	wave_mem_clk_sel Waveform generator memory clock selection 2'b00: Select clk_pwm 2'b01: Select clk_pwm_osc 2'b10: Select clk_pwm_rc
3	RW	0x0	wave_update_mode Waveform generator update mode 1'b0: The address will wrap back to minimum address when increase to maximum address, and then increase again. 1'b1: The address will change to decreasing when increasing to the maximum address. it will return to increasing when decrease to the minimum value.
2	RW	0x0	wave_width_mode Waveform generator width mode 1'b0: 8bits 1'b1: 16bits Note: The table is 8bit, User can compose 16 bits with two adjacent addresses

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Bit	Attr	Reset Value	Description
1	RW	0x0	wave_period_en Waveform generator period enable. The period cycle of the output waveform is controlled by waveform generator table instead of register PWM_PERIOD when this bit is set to 1. The period will be updated every waveform number of rpt_first_dimensional.
0	RW	0x0	wave_duty_en Waveform generator duty enable. The duty cycle of the output waveform is controlled by waveform generator table instead of register PWM_DUTY when this bit is set to 1. The duty will be updated every waveform number of rpt_first_dimensional.

PWM_WAVE_MAX

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	wave_period_max The maximum index of period.
15:10	RO	0x00	reserved
9:0	RW	0x000	wave_duty_max The maximum index of duty.

PWM_WAVE_MIN

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	wave_period_min The minimum index of period.
15:10	RO	0x00	reserved
9:0	RW	0x000	wave_duty_min The minimum index of duty.

PWM_WAVE_OFFSET

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	wave_offset The initial offset index of duty and period

PWM_WAVE_MIDDLE

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	wave_middle The middle index of duty and period.

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PWM_WAVE_HOLD

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	middle_hold The time to hold at middle index. the unit is waveform number of rpt_first_dimensional
15:8	RW	0x00	min_hold The time to hold at minimum index. the unit is waveform number of rpt_first_dimensional
7:0	RW	0x00	max_hold The time to hold at maximum index. the unit is waveform number of rpt_first_dimensional

PWM_GLOBAL_ARBITER

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	global_read_lock Each bit controls the read lock of global control registers. Once one channel obtains arbitration, other channels cannot read global registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	global_grant Each bit controls the grant of global control for one channel. Once one channel obtains arbitration, other channels cannot write global registers. 1'b0: Don't Grant 1'b1: Grant

PWM_GLOBAL_CTRL

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	W1T	0x0	global_pwm_ctrl_update_en PWM global control update enable. The bit will be auto cleaned. The following register can be updated at the posedge of pwm_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET

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Bit	Attr	Reset Value	Description
0	RW	0x0	global_pwm_en Global PWM enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWRMATCH_ARBITER

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	pwrkey_read_lock Each bit controls the read lock of power key function. Once one channel obtains arbitration, other channels cannot read power key registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	pwrkey_grant Each bit controls the grant of power key function for one channel. Once one channel obtains arbitration, other channels cannot write power key registers. 1'b0: Don't Grant 1'b1: Grant

PWM_PWRMATCH_CTRL

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	pwrkey_int_ctrl 1'b0: Assert interrupt after key capture with power key match 1'b1: Assert interrupt after key capture without power key match
2	RW	0x0	pwrkey_capture_ctrl 1'b0: Capture the value after interrupt 1'b1: Capture the value directly
1	RW	0x0	pwrkey_polarity 1'b0: PWM in polarity is positive 1'b1: PWM in polarity is negative
0	RW	0x0	pwrkey_enable 1'b0: Disabled 1'b1: Enabled

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PWM_PWRMATCH_LPRE

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x238c	cnt_max The maximum counter value
15:0	RW	0x22c4	cnt_min The minimum counter value

PWM_PWRMATCH_HPRE

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x11f8	cnt_max The maximum counter value
15:0	RW	0x1130	cnt_min The minimum counter value

PWM_PWRMATCH_LD

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value
15:0	RW	0x01cc	cnt_min The minimum counter value

PWM_PWRMATCH_HD_ZERO

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value
15:0	RW	0x01cc	cnt_min The minimum counter value

PWM_PWRMATCH_HD_ONE

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x06fe	cnt_max The maximum counter value
15:0	RW	0x0636	cnt_min The minimum counter value

PWM_PWRMATCH_VALUE0

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value0 Power key match value 0

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PWM_PWRMATCH_VALUE1

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value1 Power key match value 1

PWM_PWRMATCH_VALUE2

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value2 Power key match value 2

PWM_PWRMATCH_VALUE3

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value3 Power key match value 3

PWM_PWRMATCH_VALUE4

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value4 Power key match value 4

PWM_PWRMATCH_VALUE5

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value5 Power key match value 5

PWM_PWRMATCH_VALUE6

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value6 Power key match value 6

PWM_PWRMATCH_VALUE7

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value7 Power key match value 7

PWM_PWRMATCH_VALUE8

Address: **Operational Base** + offset (0x013C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value8 Power key match value 8

PWM_PWRMATCH_VALUE9

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value9 Power key match value 9

PWM_PWRMATCH_VALUE10

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value10 Power key match value 10

PWM_PWRMATCH_VALUE11

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value11 Power key match value 11

PWM_PWRMATCH_VALUE12

Address: **Operational Base** + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value12 Power key match value 12

PWM_PWRMATCH_VALUE13

Address: **Operational Base** + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value13 Power key match value 13

PWM_PWRMATCH_VALUE14

Address: **Operational Base** + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value14 Power key match value 14

PWM_PWRMATCH_VALUE15

Address: **Operational Base** + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value15 Power key match value 15

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PWM_PWRCAPTURE_VALUE

Address: **Operational Base** + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pwrkey_capture_value Power key capture value

PWM_IR_TRANS_ARBITER

Address: **Operational Base** + offset (0x0180)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	it_trans_read_lock Each bit controls the read lock of IR transmission function. Once one channel obtains arbitration, other channels cannot read power key registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	ir_trans_grant Each bit controls the grant of IR transmission function for one channel. Once one channel obtains arbitration, other channels cannot write power key registers. 1'b0: Don't Grant 1'b1: Grant

PWM_IR_TRANS_CTRL0

Address: **Operational Base** + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	ir_trans_clk_en_force PWM IR Trans Out Function clock enable force.
12:8	RW	0x1f	ir_trans_length_within_one_frame 0x00~0x1F is corresponding to data length 1~32
7:4	RW	0x0	ir_trans_format PWM IR Trans format 4'h0: NEC with simple repeat code 4'h1: NEC with full repeat code 4'h2: TC9012 4'h3: SONY Others: reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	it_trans_mode 1'b0: One shot mode, PWM produces the waveform within the repeated times defined by ir_trans_rtp_cnt. 1'b1: Continuous mode, PWM produces the waveform continuously.
2	RW	0x0	it_trans_inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
1	RW	0x0	ir_trans_duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
0	RW	0x0	ir_trans_out_enable 1'b0: disable PWM IR Trans Out Function 1'b1: enable PWM IR Trans Out Function

PWM_IR_TRANS_CTRL1

Address: **Operational Base** + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	ir_trans_rpt This field defines the repeated number for IR transmission. The value N means N+1 repeated effective periods.

PWM_IR_TRANS_PRE

Address: **Operational Base** + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RW	0x1194	ir_trans_out_high_preload IR Trans Out High Preload Register
15:0	RW	0x2328	ir_trans_out_low_preload IR Trans Out Low Preload Register

PWM_IR_TRANS_SPRE

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x08ca	ir_trans_out_high_simple_preload PWM IR Trans Out High Simple Preload Register

PWM_IR_TRANS_LD

Address: **Operational Base** + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0230	ir_trans_out_data_low_period IR Trans Out Data Low Period Register

PWM_IR_TRANS_HD

Address: **Operational Base** + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x069a	ir_trans_out_high_period_for_one IR Trans Out High Period for One Register
15:0	RW	0x0230	ir_trans_out_high_period_for_zero IR Trans Out High Period for Zero Register

PWM_IR_TRANS_BURST_FRAME

Address: **Operational Base** + offset (0x019C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x226	ir_trans_out_burst_period PWM IR Trans Out Burst Period Register
19:18	RO	0x0	reserved
17:0	RW	0x1a5e0	ir_trans_out_frame_period PWM IR Trans Out Frame Period

PWM_IR_TRANS_DATA_VALUE

Address: **Operational Base** + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ir_trans_out_value PWM IR Trans Out Value Register

PWM_IR_TRANS_STATUS

Address: **Operational Base** + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	ir_state_idle 1'b0: PWM IR Trans Busy 1'b1: PWM IR Trans Idle

PWM_FREQ_ARBITER

Address: **Operational Base** + offset (0x01C0)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	freq_read_lock Each bit controls the read lock of frequency meter function. Once one channel obtains arbitration, other channels cannot read frequency meter registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	freq_grant Each bit controls the grant of frequency meter function for one channel. Once one channel obtains arbitration, other channels cannot write frequency meter registers. 1'b0: Don't Grant 1'b1: Grant

PWM_FREQ_CTRL

Address: **Operational Base** + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	freq_timer_clk_sel Frequency meter timer clock selection 1'b0: Select clk_pwm, clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_osc, clock is from crystal oscillator and the frequency is fixed.
6	W1T	0x0	freq_timer_clk_switch_mode Timer clock switch mode 1'b0: Normal mode 1'b1: Switch timer clock and measured clock. It Can be used to provide testing accuracy or reduce testing time when the frequency of measured clock is low. It can also be used in scenarios where the start time of the measured clock is uncertain
5:3	RW	0x0	freq_channel_sel Frequency Meter channel selection. It's valid only when freq_clk_sel set to 1'b0. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5

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Bit	Attr	Reset Value	Description
			3'b110: PWM channel 6 3'b111: PWM channel 7
2	RO	0x0	reserved
1	RW	0x0	freq_clk_sel Frequency Meter clock selection 1'b0: Input from PWM IO 1'b1: Frequency clock from CRU
0	W1T	0x0	freq_en Frequency Meter enable.

PWM_FREQ_TIMER_VALUE

Address: **Operational Base** + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	freq_timer_value Frequency Meter timer value, the unit is one cycle frequency meter timer clock.

PWM_FREQ_RESULT_VALUE

Address: **Operational Base** + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	freq_result_value The frequency result value, the unit is one cycle of tested clock. Once the freq_intsts interrupt is asserted, User can get the frequency by this value. When timer_clk_switch_mode set to 1'b0, the frequency result is (freq_timer*freq_result_value)/freq_timer_value. When timer_clk_switch_mode set to 1'b1, the frequency result is (freq_timer*freq_timer_value)/freq_result_value. Notes: freq_osc is the frequency of SOC crystal oscillator.

PWM_COUNTER_ARBITER

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	counter_read_lock Each bit controls the read lock of counter function. Once one channel obtains arbitration, other channels cannot read counter registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	counter_grant Each bit controls the grant of counter for one channel. Once one channel obtains arbitration, other channels cannot write counter registers. 1'b0: Don't Grant 1'b1: Grant

PWM_COUNTER_CTRL

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	W1T	0x0	counter_clr Counter value clear.
5:3	RW	0x0	counter_channel_sel Counter channel selection. It's valid only when counter_clk_sel set to 1'b00. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5 3'b110: PWM channel 6 3'b111: PWM channel 7
2:1	RW	0x0	counter_clk_sel Counter clock selection 1'b0: Input from PWM IO 1'b1: Counter clock from CRU
0	RW	0x0	counter_en Counter enable.

PWM_COUNTER_LOW

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	counter_low_bits Indicates low 32bits of counter value. The value of counter ranges from 0 to 2^64-1, The unit is one cycle of tested clock

PWM_COUNTER_HIGH

Address: **Operational Base** + offset (0x020C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	counter_high_bits Indicates high 32bits of the counter value. The value of counter ranges from 0 to 2^64-1, The unit is one cycle of tested clock

PWM_WAVE_MEM

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	wave_mem_base_address Waveform Generator memory base address

31.5 Interface Description

Table 31-2 PWM Rockchip Matrix IO Interface Description

Module Pin	Direction	Rockchip Matrix IO	IOMUX Setting
PWM0_CH0~CH3	I/O	RM_IO	
PWM1_CH0~CH7	I/O	RM_IO	
PWM1_BIP_CNTR_A0~A5	I	RM_IO	
PWM1_BIP_CNTR_B0~B5	I	RM_IO	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

31.6 Application Notes

31.6.1 PWM Capture Mode Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.pwm_mode to 2'b10 to select capture mode.
4. Set PWM_INT_EN.cap_lpc_int_en/cap_hpc_int_en to 1'b1 to enable the interrupt.
5. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
6. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt status. User should read the PWM_HPC register to know the effective high cycles of input waveforms when cap_hpc_intsts is asserted and read the PWM_LPC register to know the effective low cycles when cap_lpc_intsts is asserted. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
7. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

31.6.2 PWM Power Key Capture Mode Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division. The clock frequency should be 1 MHz after division.
3. Set PWM_CTRL.pwm_mode to 2'b10 to select capture mode.
4. Set PWM_PWRMATCH_ARBITER.pwrkey_grant to 8'b01 to set channel 0 for capture.
5. Set PWM_INT_EN.pwr_int_en to 1'b1 to enable the interrupt.
6. Set PWM_PWRMATCH_VALUE0~15 registers for the 16 power key match value.
7. Set max_cnt and min_cnt of follow register: PWM_PWRMATCH_LPRE, PWM_PWRMATCH_HPRE, PWM_PWRMATCH_LD, PWM_PWRMATCH_HD_ZERO, PWM_PWRMATCH_HD_ONE. It doesn't need to set these registers if the default value can meet the requirement.

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8. Set PWM_PWRMATCH_CTRL.pwrkey_polarity for the polarity of power key signal.
9. Set PWM_PWRMATCH_CTRL.pwrkey_enable to 1'b1 to enable power key mode.
10. Set PWM_FILTER_CTRL.filter_number/filter_enable to enable filter. (Optional).
11. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
12. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt status, and refer to PWM_PWRCAPTURE_VALUE to know the power key capture value. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
13. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

31.6.3 PWM Continuous Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD and PWM_DUTY register.
5. Set PWM_RPT.rpt_first_dimensional for reload operation (Optional).
6. Set PWM_CTRL.pwm_mode to 2'b01 to select continuous mode.
7. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
8. Set PWM_PERIOD and DUTY, then set PWM_ENABLE.pwm_ctrl_update_en to 1'b1 to update configuration (Optional).
9. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

31.6.4 PWM One-shot Mode Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD and PWM_DUTY register.
5. Set PWM_RPT.rpt_first_dimensional for reload operation (Option).
6. Set PWM_RPT.rpt_second_dimensional.
7. Set PWM_CTRL.pwm_mode to 2'b00 to select one shot mode.
8. Set INT_EN.oneshot_end_int_en to 1'b1 to enable interrupt.
9. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
10. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt. PWM_CTRL.pwm_en/pwm_clk_en is automatically cleared.

31.6.5 Multi-channel Synchronous Start Usage Flow

1. Set PWM_ENABLE.pwm_en of all synchronous channels to 1'b0 to disable the PWM channel.
2. Set PWM_CTRL.pwm_mode/output_mode/duty_pol/inactive_pol, PWM_PERIOD and PWM_DUTY register of all synchronous channels.
3. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel of channel 0 to configure the clock selection and division.
4. Set PWM_Enable.pwm_global_join_en of all synchronous channels to 1'b1.
5. Enable the INT_EN.oneshot_end_int_en of channel 0 to enable interrupt generation if the channel is desired to work in the one-shot mode.
6. Set PWM_ENABLE.pwm_clk_en of channel 0 to 1'b1 to enable clock.
7. Set PWM_GLOBAL_ARBITER.global_grant to 8'h01 to set channel 0 as main channel.
8. Set PWM_GLOBAL_CTRL.global_pwm_en to enable all synchronous channels.
9. Set PWM_PERIOD and DUTY to all synchronous channel, then set PWM_GLOBAL_CTRL.global_pwm_ctrl_update_en to 1'b1 to update configuration of all synchronous channels (Optional).
10. If user want to disable PWM channel, set PWM_GLOBAL_CTRL.global_pwm_en to 1'b0, then set PWM_CTRL.pwm_clk_en of channel 0 to 1'b0 to disable clock.

31.6.6 IR transmission Usage Flow

1. Set PWM_CTRL.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and

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division. The clock frequency should be 1 MHz after division.
3. Set PWM_CTRL.pwm_clk_en to 1'b1 to enable clock.
4. Set PWM_IR_TRANS_ARBITER.ir_trans_grant to 8'b01 to set channel 0 for transmission.
5. Set PWM_IR_TRANS_CTRL0.format/it_trans_mode/ir_trans_duty_pol/ ir_trans_length_within_one_frame/it_trans_inactive_pol
6. Set PWM_IR_TRANS_DATA_VALUE.ir_trans_out_value to the data which need to transmit.
7. Set the PWM_IR_TRANS_CTRL0.ir_trans_rpt if the channel is desired to work in the one-shot mode.
8. Set PWM_IR_TRANS_CTRL0.transout_en to 1'b1 to enable PWM IR transmission.
9. If user want to disable the output waveform, set PWM_IR_TRANS_CTRL0.transout_en to 1'b0, the channel will be disable at the end of one frame.

31.6.7 Clock Counter Usage Flow

1. Set PWM_COUNTER_ARBITER.counter_grant to 8'h01 to use channel 0.
2. Set PWM_COUNTER_CTRL.counter_clk_sel/counter_channel_sel to select clock.
3. Set PWM_COUNTER_CTRL.counter_en to 1'b1 to enable clock counter.
4. Refer to PWM_COUNTER_LOW/ PWM_COUNTER_HIGH to gets the counter value.
5. If user want to disable clock counter, set PWM_COUNTER_CTRL.counter_en to 1'b0, then set PWM_COUNTER_ARBITER.counter_grant to 8'h0.

31.6.8 Clock Frequency Meter Usage Flow

1. Set PWM_FREQ_ARBITER.freq_grant to 8'h01 to use channel 0.
2. Set PWM_FREQ_CTRL.freq_clk_sel/freq_channel_sel to select clock.
3. Set PWM_FREQ_CTRL.freq_timer_clk_sel to select timer clock.
4. Set PWM_FREQ_TIMER_VALUE.freq_timer_value to set timer.
5. Set PWM_INT_EN.freq_int_en to enable interrupt.
6. Set PWM_FREQ_CTRL.freq_en to 1'b1 to enable clock frequency meter.
7. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. Then refer PWM_FREQ_RESULT_VALUE.freq_result_value to get result. The frequency can be calculated as formula: frequency_timer* freq_result_value/ freq_timer_value. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
8. If user want to disable clock frequency meter, set PWM_FREQ_ARBITER.freq_grant to 8'h0.

31.6.9 Biphasic Counter Usage Flow

1. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_clk_sel to select clock.
2. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_mode to select mode.
3. Set PWM_BIPHASIC_COUNTER_CTRL1.biphasic_counter_filter_number/ biphasic_counter_filter_enable to set the filter.
4. Set PWM_BIPHASIC_COUNTER_TIMER_VALUE. biphasic_counter_timer_value to set timer.
5. Set PWM_INT_EN.biphasic_couner_int_en to enable interrupt.
6. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_en to 1'b1 to enable biphasic counter.
7. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. Then refer PWM_BIPHASIC_COUNTER_RESULT_VALUE to get the result. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.

31.6.10 Generates Waveform Through Lookup Table Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD register, the value should be 1~256.
5. Set PWM_WAVE_CTRL.wave_duty_en to 1'b1 to enable duty to reload through lookup table.
6. Set PWM_WAVE_CTRL.wave_update_mode to 1'b1.
7. Set PWM_WAVE_MAX.wave_duty_max.
8. Set PWM_WAVE_MIN.wave_duty_min.

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9. Set the duty value in lookup table from offset address wave_duty_min to wave_duty_max. The base address of lookup table is PWM_WAVE_MEM.
10. Set PWM_RPT.rpt_first_dimensional for reloading interval.
11. Set PWM_CTRL.pwm_mode to 2'b01 to select continuous mode.
12. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.

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Chapter 32 Inter-Integrated Circuit (I2C)

32.1 Overview

The Inter-Integrated Circuit (I2C) is a two wired (SCL and SDA), bi-directional serial bus that provides an efficient and simple method of information exchange between devices. This I2C bus controller supports master mode acting as a bridge between AMBA protocol and generic I2C bus system.

I2C Controller supports the following features:

- Support 3 independent I2C: I2C0~2
- Item Compatible with I2C-bus
- AMBA APB slave interface
- Support master mode of I2C bus
- Software programmable clock frequency and transfer rate up to 400Kbit/sec
- Support 7 bits and 10 bits addressing modes
- Interrupt or polling driven multiple bytes data transfer
- Clock stretching and wait state generation
- Filter out glitch on SCL and SDA

32.2 Block Diagram

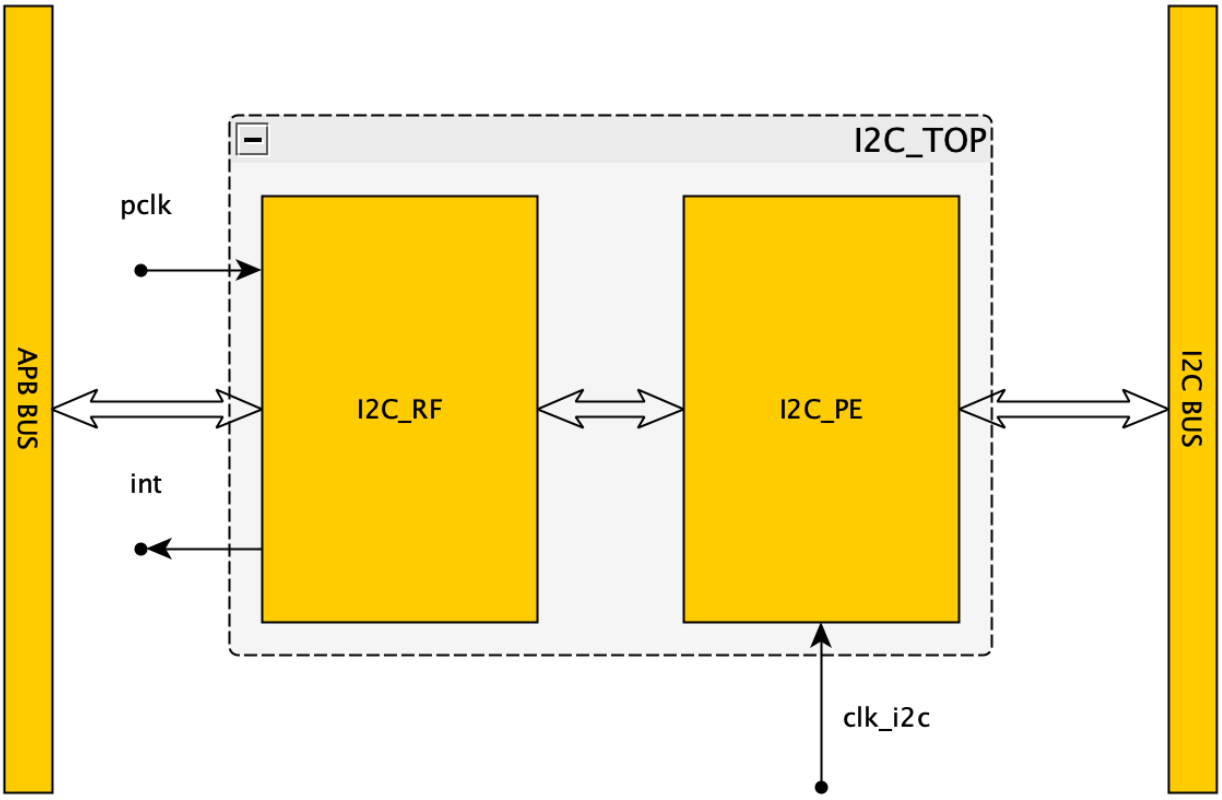

Fig.32-1 I2C Architecture

32.2.1 I2C_RF

I2C_RF module is used to control the I2C controller operation by the host with APB interface. It implements the register set and the interrupt functionality. The I2C_RF component operates synchronously with the APB clock.

32.2.2 I2C_PE

I2C_PE module implements the I2C master operation for transmit data to and receive data from other I2C devices. The I2C master controller operates synchronously with the clk_i2c.

32.2.3 I2C_TOP

I2C_TOP module is the top module of the I2C controller.

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32.3 Function Description

This chapter provides a description about the functions and behavior under various conditions.
The I2C controller supports only Master function. It supports the 7-bits/10-bits addressing mode and supports general call address. The maximum clock frequency and transfer rate can be up to 400Kbit/sec.
The operations of I2C controller is divided to 2 parts and described separately: initialization and master mode programming.

32.3.1 Initialization

The I2C controller is based on AMBA APB bus architecture and usually is part of a SOC. So before I2C operates, some system setting and configuration must be conformed, which includes:

- I2C interrupt connection type: CPU interrupt scheme should be considered. If the I2C interrupt is connected to extra Interrupt Controller module, we need decide the INTC vector.
- I2C Clock Rate: The I2C controller uses the APB clock to configure controller and uses clk_i2c as the working clock. The correct register setting is subject to the system requirement.

32.3.2 Master Mode Programming

- SCL Clock
  When the I2C controller is programmed in Master mode, the SCL frequency is determined by I2C_CLKDIV register. The SCL frequency is calculated by the following formula:
  SCL Divisor = 8*(CLKDIVL + 1 + CLKDIVH + 1); clk_i2c = 100MHz~200MHz.
  SCL = clk_i2c/ SCLK Divisor.

- Data Receiver Register Access
  When the I2C controller received MRXCNT bytes data, CPU can get the data through register RXDATA0 ~ RXDATA7. The controller can receive up to 32 bytes' data in one transaction.
  When MRXCNT register is written, the I2C controller will start to drive SCL to receive data.

- Transmit Transmitter Register
  Data to transmit are written to TXDATA0~7 by CPU. The controller can transmit up to 32 bytes' data in one transaction. The lower byte will be transmitted first.
  When MTXCNT register is written, the I2C controller will start to transmit data.

- Start Command
  Write 1 to I2C_CON[3], the controller will send I2C start command.

- Stop Command
  Write 1 to I2C_CON[4], the controller will send I2C stop command.

- I2C Operation mode
  There are four i2c operation modes.
  - When I2C_CON[2:1] is 2'b00, the controller will transmit all valid data in TXDATA0~TXDATA7 byte by byte. The controller will transmit lower byte first.
  - When I2C_CON[2:1] is 2'b01, the controller will transmit device address in MRXADDR first (Write/Read bit = 0) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enters receive mode.

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- When I2C_CON[2:1] is 2'b10, the controller is in receive mode, it will trigger clock to read MRXCNT byte data.
- When I2C_CON[2:1] is 2'b11, the controller will transmit device address in MRXADDR first (Write/Read bit = 1) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enters receive mode.

- Read/Write Command
  - When I2C_OPMODE (I2C_CON[2:1]) is 2'b01 or 2'b11, the Read/Write command bit is decided by controller itself.
  - In RX only mode (I2C_CON[2:1] is 2'b10), the Read/Write command bit is decided by MRXADDR[0].
  - In TX only mode (I2C_CON[2:1] is 2'b00), the Read/Write command bit is decided by TXDATA[0].

- Master Interrupt Condition

  There are 7 interrupt bits in I2C_ISR register related to master mode.
  - Byte transmitted finish interrupt (Bit 0): The bit is asserted when Master completed transmitting a byte.
  - Byte received finish interrupt (Bit 1): The bit is asserted when Master completed receiving a byte.
  - MTXCNT bytes data transmitted finish interrupt (Bit 2): The bit is asserted when Master completed transmitting MTXCNT bytes.
  - MRXCNT bytes data received finish interrupt (Bit 3): The bit is asserted when Master completed receiving MRXCNT bytes.
  - Start interrupt (Bit 4): The bit is asserted when Master finished asserting start command to I2C bus.
  - Stop interrupt (Bit 5): The bit is asserted when Master finished asserting stop command to I2C bus.
  - NAK received interrupt (Bit 6): The bit is asserted when Master received a NAK handshake.

- Last byte acknowledge control
  - If I2C_CON[5] is 1, the I2C controller will transmit NAK handshake to slave when the last byte received in RX only mode.
  - If I2C_CON[5] is 0, the I2C controller will transmit ACK handshake to slave when the last byte received in RX only mode.

- How to handle NAK handshake received
  - If I2C_CON[6] is 1, the I2C controller will stop all transactions when NAK handshake received. And the software should take responsibility to handle the problem.
  - If I2C_CON[6] is 0, the I2C controller will ignore all NAK handshake received.

- I2C controller data transfer waveform
  - Bit transferring
    - Data Validity

      The SDA line must be stable during the high period of SCL, and the data on SDA line can only be changed when SCL is in low state.

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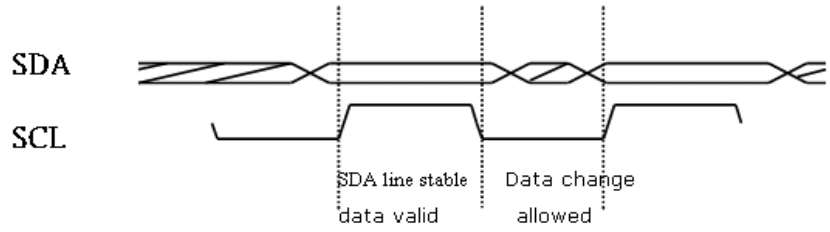

Fig.32-2 I2C DATA Validity

- START and STOP conditions
  START condition occurs when SDA goes low while SCL is in high period. STOP condition is generated when SDA line goes high while SCL is in high state.

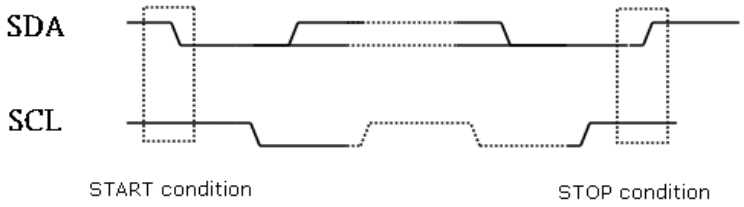

Fig.32-3 I2C Start and Stop Conditions

- Data transfer
  - Acknowledge
    After a byte of data transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK signal on SDA line, if the receiver pulls SDA line to low, it means "ACK", on the contrary, it's "NOT ACK".

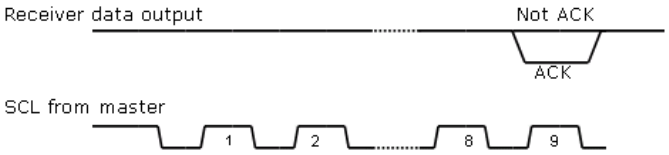

Fig.32-4 I2C Acknowledge

  - Byte transfer
    The master owns I2C bus might initiate multi byte to transfer to a slave. The transfer starts from a "START" command and ends in a "STOP" command. After every byte transfer, the receiver must reply an ACK to transmitter.

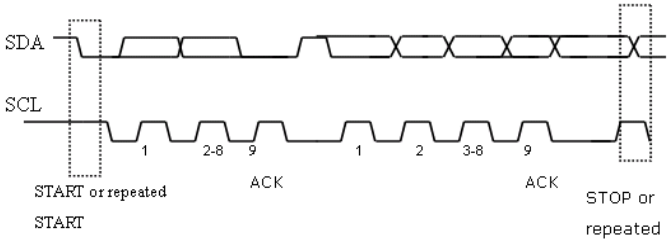

Fig.32-5 I2C Byte Transfer

32.4 Register Description

32.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

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Name	Base Address
I2C0	0xff040000
I2C1	0xff050000
I2C2	0xff060000

32.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKI2C_CON	0x0000	W	0x00060000	Control register
RKI2C_CLKDIV	0x0004	W	0x00000001	Clock divider register I2C CLK = PCLK / (16*CLKDIV)
RKI2C_MRXADDR	0x0008	W	0x00000000	The slave address accessed for master rx mode
RKI2C_MRXRADDR	0x000C	W	0x00000000	The slave register address accessed for master rx mode
RKI2C_MTXCNT	0x0010	W	0x00000000	Master transmit count, specify the total bytes to be transmit (0~32)
RKI2C_MRXCNT	0x0014	W	0x00000000	Master rx count, specify the total bytes to be received(0~32)
RKI2C_IEN	0x0018	W	0x00000000	Interrupt enable register
RKI2C_IPD	0x001C	W	0x00000000	Interrupt pending register
RKI2C_FCNT	0x0020	W	0x00000000	Finished count: the count of data which has been transmitted or received for debug purpose
RKI2C_SCL_OE_DB	0x0024	W	0x00000020	Slave hold debounce configure register
RKI2C_TXDATA0	0x0100	W	0x00000000	I2C tx data register 0
RKI2C_TXDATA1	0x0104	W	0x00000000	I2C tx data register 1
RKI2C_TXDATA2	0x0108	W	0x00000000	I2C tx data register 2
RKI2C_TXDATA3	0x010C	W	0x00000000	I2C tx data register 3
RKI2C_TXDATA4	0x0110	W	0x00000000	I2C tx data register 4
RKI2C_TXDATA5	0x0114	W	0x00000000	I2C tx data register 5
RKI2C_TXDATA6	0x0118	W	0x00000000	I2C tx data register 6
RKI2C_TXDATA7	0x011C	W	0x00000000	I2C tx data register 7
RKI2C_RXDATA0	0x0200	W	0x00000000	I2C rx data register 0
RKI2C_RXDATA1	0x0204	W	0x00000000	I2C rx data register 1
RKI2C_RXDATA2	0x0208	W	0x00000000	I2C rx data register 2
RKI2C_RXDATA3	0x020C	W	0x00000000	I2C rx data register 3
RKI2C_RXDATA4	0x0210	W	0x00000000	I2C rx data register 4
RKI2C_RXDATA5	0x0214	W	0x00000000	I2C rx data register 5
RKI2C_RXDATA6	0x0218	W	0x00000000	I2C rx data register 6
RKI2C_RXDATA7	0x021C	W	0x00000000	I2C rx data register 7
RKI2C_ST	0x0220	W	0x00000000	Status debug register
RKI2C_DBGCTRL	0x0224	W	0x00000000	Debug configuration register
RKI2C_CON1	0x0228	W	0x00000000	Control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

32.4.3 Detail Registers Description

RKI2C_CON

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0006	version Rki2c version information.
15:14	RW	0x0	stop_setup Stop setup configuration. TSU;sto = (stop_setup + 1) * T(SCL_HIGH) + Tclk_i2c.

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	start_setup Start setup config. TSU;sta = (start_setup + 1) * T(SCL_HIGH) + Tclk_i2c. THD;sta = (start_setup + 2) * T(SCL_HIGH) - Tclk_i2c.
11:8	RW	0x0	data_upd_st SDA update point config. Used to config sda change state when scl is low, used to adjust setup/hold time. 4'bn: Thold = (n + 1) * Tclk_i2c. Note: 0 <= n <= 5
7	RO	0x0	reserved
6	RW	0x0	act2nak Operation when NAK handshake is received. 1'b0: Ignored. 1'b1: Stop transaction.
5	RW	0x0	ack Last byte acknowledge control in master receive mode. 1'b0: ACK 1'b1: NAK
4	RW	0x0	stop Stop enable, when this bit is written to 1, I2C will generate stop signal.
3	RW	0x0	start Start enable, when this bit is written to 1, I2C will generate start signal.
2:1	RW	0x0	i2c_mode I2c mode select. 2'b00: Transmit only. 2'b01: Transmit address (device + register address) --> Restart --> Transmit address -> Receive only. 2'b10: Receive only. 2'b11: Transmit address (device + register address, write/read bit is 1) --> Restart --> Transmit address (device address) --> Receive data.
0	RW	0x0	i2c_en I2c module enable. 1'b0: Disable 1'b1: Enable

RKI2C_CLKDIV

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CLKDIVH SCL high level clock count. T(SCL_HIGH) = Tclk_i2c * (CLKDIVH + 1) * 8.
15:0	RW	0x0001	CLKDIVL SCL low level clock count. T(SCL_LOW) = Tclk_i2c * (CLKDIVL + 1) * 8.

RKI2C_MRXADDR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26	RW	0x0	addhvld Address high byte valid. 1'b0: Invalid 1'b1: Valid
25	RW	0x0	addmvld Address middle byte valid. 1'b0: Invalid 1'b1: Valid
24	RW	0x0	addlvld Address low byte valid. 1'b0: Invalid 1'b1: Valid
23:0	RW	0x000000	saddr Master address register. The lowest bit indicate write or read. 24 bits address register.

RKI2C_MRXRADDR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	sraddhvld Address high byte valid. 1'b0: Invalid 1'b1: Valid
25	RW	0x0	sraddmvld Address middle byte valid. 1'b0: Invalid 1'b1: Valid
24	RW	0x0	sraddlvld Address low byte valid. 1'b0: Invalid 1'b1: Valid
23:0	RW	0x000000	sraddr Slave register address accessed. 24 bits register address

RKI2C_MTXCNT

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	mtxcnt Master transmit count. 6 bits counter

RKI2C_MRXCNT

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	mrxcnt Master rx count. 6 bits counter

RKI2C_IEN

Address: **Operational Base** + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	slavehdsdaen Slave hold sda interrupt enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	slavehdsclen Slave hold scl interrupt enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	nakrcvien NAK handshake received interrupt enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	stopien Stop operation finished interrupt enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	startien Start operation finished interrupt enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	mbrfien MRXCNT data received finished interrupt enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	mbtfien MTXCNT data transfer finished interrupt enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	brfien Byte rx finished interrupt enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	btfien Byte tx finished interrupt enable. 1'b0: Disable 1'b1: Enable

RKI2C_IPD

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	slavehdsdaipd Slave hold sda interrupt pending bit. 1'b0: No interrupt available. 1'b1: Slave hold sda interrupt appear, write 1 to clear.
7	RW	0x0	slavehdsclipd Slave hold scl interrupt pending bit. 1'b0: No interrupt available. 1'b1: Slave hold scl interrupt appear, write 1 to clear.
6	W1C	0x0	nakrcvipd NAK handshake received interrupt pending bit. 1'b0: No interrupt available. 1'b1: NAK handshake received interrupt appear, write 1 to clear.

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Bit	Attr	Reset Value	Description
5	W1C	0x0	stopipd Stop operation finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Stop operation finished interrupt appear, write 1 to clear.
4	W1C	0x0	startipd Start operation finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Start operation finished interrupt appear, write 1 to clear.
3	W1C	0x0	mbrfipd MRXCNT data received finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: MRXCNT data received finished interrupt appear, write 1 to clear.
2	W1C	0x0	mbtfipd MTXCNT data transfer finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: MTXCNT data transfer finished interrupt appear, write 1 to clear.
1	W1C	0x0	brfipd Byte rx finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Byte rx finished interrupt appear, write 1 to clear.
0	W1C	0x0	btfipd Byte tx finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Byte tx finished interrupt appear, write 1 to clear.

RKI2C_FCNT

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	fcnt The count of data which has been transmitted or received for debug purpose.

RKI2C_SCL_OE_DB

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x20	scl_oe_db Slave hold scl debounce. Cycles for debounce (unit: Tclk_i2c).

RKI2C_TXDATA0

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata0 Data0 to be transmitted. 32 bits data

RKI2C_TXDATA1

Address: **Operational Base** + offset (0x0104)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata1 Data1 to be transmitted. 32 bits data

RKI2C_TXDATA2

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata2 Data2 to be transmitted. 32 bits data

RKI2C_TXDATA3

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata3 Data3 to be transmitted. 32 bits data

RKI2C_TXDATA4

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata4 Data4 to be transmitted. 32 bits data

RKI2C_TXDATA5

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata5 Data5 to be transmitted. 32 bits data

RKI2C_TXDATA6

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata6 Data6 to be transmitted. 32 bits data

RKI2C_TXDATA7

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata7 Data7 to be transmitted. 32 bits data

RKI2C_RXDATA0

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata0 Data0 received. 32 bits data

RKI2C_RXDATA1

Address: **Operational Base** + offset (0x0204)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata1 Data1 received. 32 bits data

RKI2C_RXDATA2

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata2 Data2 received. 32 bits data

RKI2C_RXDATA3

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata3 Data3 received. 32 bits data

RKI2C_RXDATA4

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata4 Data4 received. 32 bits data

RKI2C_RXDATA5

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata5 Data5 received. 32 bits data

RKI2C_RXDATA6

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata6 Data6 received. 32 bits data

RKI2C_RXDATA7

Address: **Operational Base** + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata7 Data7 received. 32 bits data

RKI2C_ST

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	scl_st SCL status. 1'b0: SCL status low. 1'b0: SCL status high.

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Bit	Attr	Reset Value	Description
0	RO	0x0	sda_st SDA status. 1'b0: SDA status low. 1'b0: SDA status high.

RKI2C_DBGCTRL

Address: **Operational Base** + offset (0x0224)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	h0_check_scl 1'b0: Check if scl been pull down by slave at the whole SCL_HIGH. 1'b1: Check if scl been pull down by slave only at the h0 of SCL_HIGH(SCL_HIGH including h0~h7).
13	RW	0x0	nak_release_scl 1'b0: Hold scl as low when received nack. 1'b1: Release scl as high when received nack.
12	RW	0x0	flt_en SCL edge glitch filter enable. 1'b0: Disable 1'b1: Enable
11:8	RW	0x0	slv_hold_scl_th Slave hold scl threshold = slv_hold_scl_db * Tclk_i2c.
7:4	RW	0x0	flt_r Filter scl rising edge glitches of width less than flt_r * Tclk_i2c.
3:0	RW	0x0	flt_f Filter scl falling edge glitches of width less than flt_f * Tclk_i2c.

RKI2C_CON1

Address: **Operational Base** + offset (0x0228)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	auto_stop_nak Auto stop when i2c master received nak from slave. Work when CON1[0]=1'b1. 1'b0: Do not auto stop when received nak. 1'b1: Auto stop when received nak.
1	RW	0x0	auto_stop_tx_end Auto stop when i2c master tx end. Work when CON1[0]=1'b1. 1'b0: Do not auto stop when tx end. 1'b1: Auto stop when tx end.
0	RW	0x0	auto_stop Auto stop when i2c master received nak from slave or tx end. 1'b0: Do not auto stop when received nak or tx end. 1'b1: Auto stop when received nak or tx end.

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32.5 Interface Description

Table 32-1 I2C Rockchip Matrix IO Interface Description

Module pin	Rockchip Matrix IO	IOMUX Setting
IOMUX0		
I2C0_SCL	RM_IO	
I2C0_SDA	RM_IO	
I2C1_SCL	RM_IO	
I2C1_SDA	RM_IO	
I2C2_SCL	RM_IO	
I2C2_SDA	RM_IO	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

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32.6 Application Notes

The I2C controller core operation flow chart below is to describe how the software configures and performs an I2C transaction through this I2C controller core. Descriptions are divided into 3 sections, transmit only mode, receive only mode, and mix mode. Users are strongly advised to follow:

- Transmit only mode (I2C_CON[1:0]=2'b00)

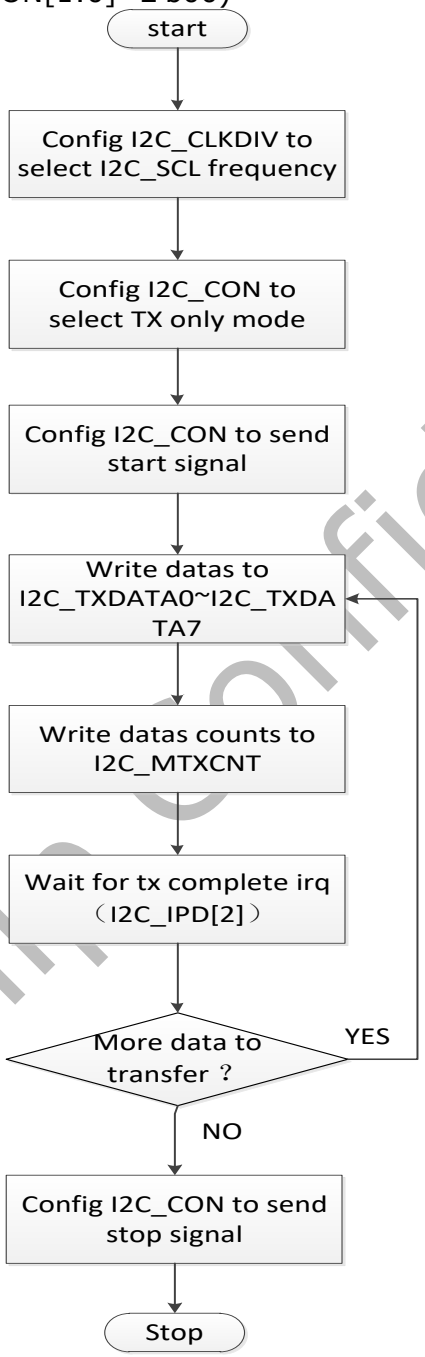

Fig.32-6 I2C Flow Chat for Transmit Only Mode

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- Receive only mode (I2C_CON[1:0]=2'b10)

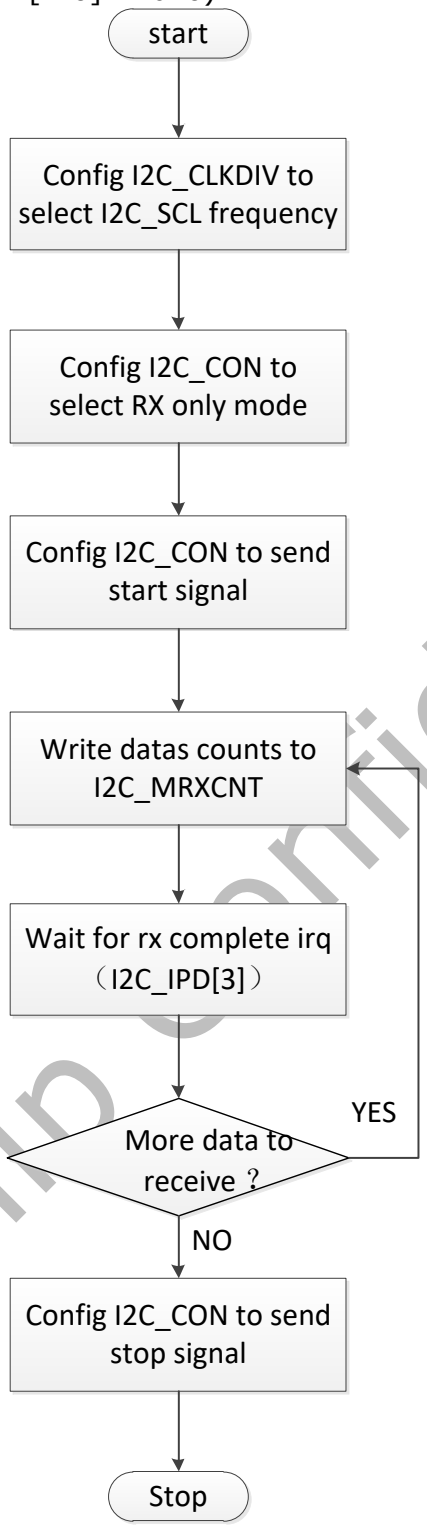

Fig.32-7 I2C Flow Chat for Receive Only Mode

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- Mix mode (I2C_CON[1:0]=2'b01 or I2C_CON[1:0]=2'b11)

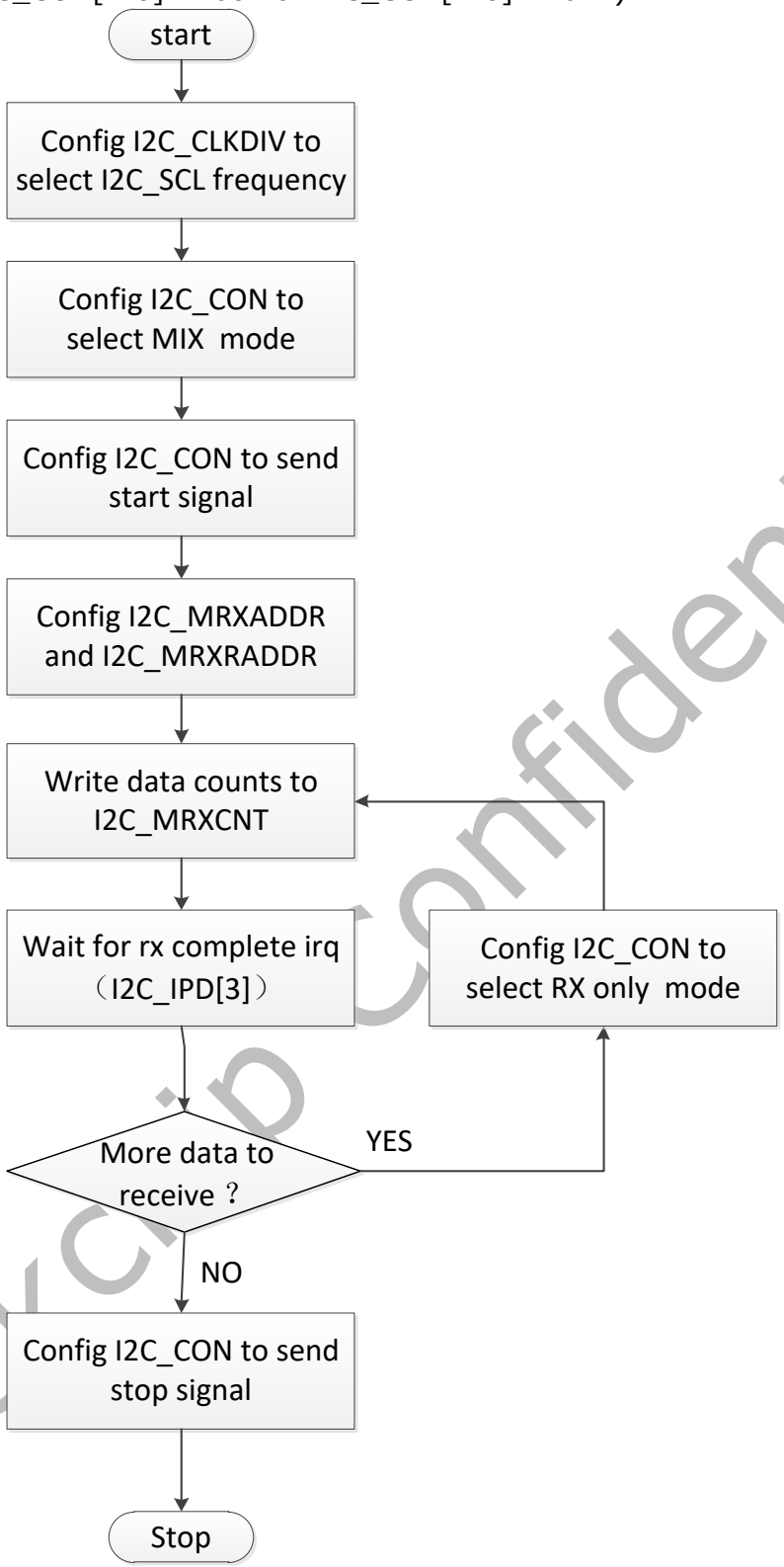

Fig.32-8 I2C Flow Chat for Mix Mode

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Chapter 33 Universal Asynchronous Receiver/Transmitter

33.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

UART Controller supports the following features:

- Support 6 independent UART controllers: UART0-UART5
- Support APB Slave configuration interface of 8, 16, 32bits
- All contain two 64 Bytes FIFOs for data receive and transmit
- UART3-UART5 support auto flow-control
- UART3-UART5 support RS485 function
- Support bit rates 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps, 8Mbps
- Support programmable baud rates, even with non-integer clock divider
- Standard asynchronous communication bits (start, stop and parity)
- Support interrupt-based or DMA-based mode
- Support 5-8 bits width transfer

33.2 Block Diagram

This section provides a description about the functions and behavior under various conditions. The UART Controller comprises with:

- AMBA APB interface
- FIFO controllers
- Register block
- Modem synchronization block and baud clock generation block
- Serial receiver and serial transmitter

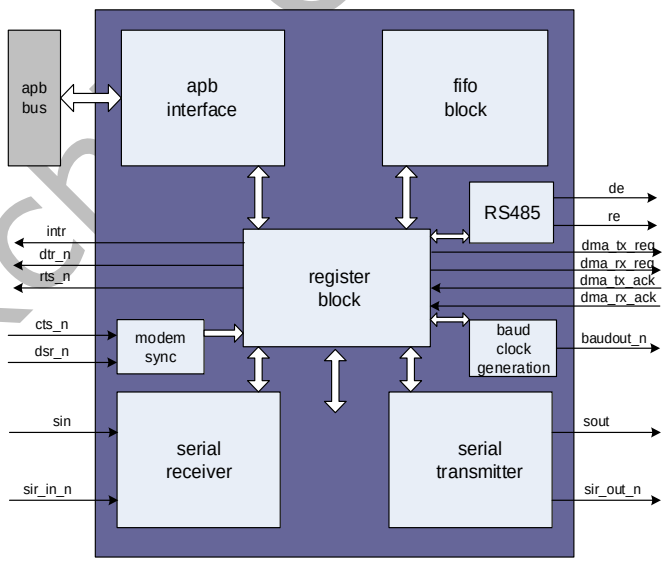

Fig. 33-1 UART Architecture

APB INTERFACE

The host processor accesses data, control, and status information on the UART through the APB interface. The UART supports APB data bus widths of 8, 16, and 32 bits.

Register block

Be responsible for the main UART functionality including control, status and interrupt generation.

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Modem Synchronization block
Synchronizes the modem input signal.

FIFO block
Be responsible for FIFO control and storage (when using internal RAM) or signaling to control external RAM (when used).

Baud Clock Generator
Generates the transmitter and receiver baud clock along with the output reference clock signal (baudout_n).

Serial Transmitter
Converts the parallel data, written to the UART, into serial form and adds all additional bits, as specified by the control register, for transmission.

Serial Receiver
Converts the serial data character (as specified by the control register) received to parallel form. Parity error detection, framing error detection and line break detection is carried out in this block.

33.3 Function Description

UART Serial Protocol
Because the serial communication is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. An additional parity bit may be added to the serial character. This bit appears after the last data bit and before the stop bit(s) in the character structure to perform simple error checking on the received data, as shown in Figure.

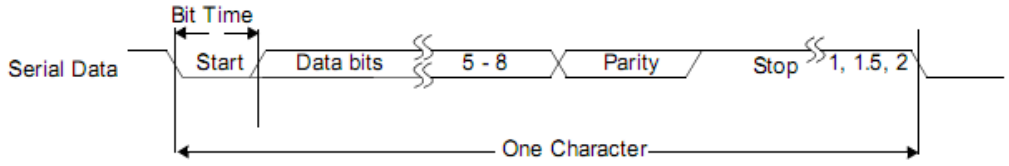

Fig. 33-2 UART Serial protocol

Baud Clock
The baud rate is controlled by the serial clock (sclk or pclk in a single clock implementation) and the Divisor Latch Register (DLH and DLL). As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit.

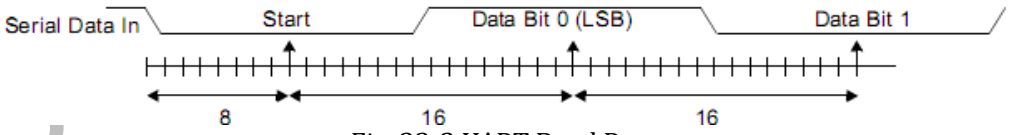

Fig. 33-3 UART Baud Rate

FIFO Support
1. NONE FIFO MODE
If FIFO support is not selected, then no FIFOs are implemented and only a single receive data byte and transmit data byte can be stored at a time in the RBR and THR.

2. FIFO MODE
The FIFO depth of is 64bytes. The FIFO mode of all the UART is enabled by register FCR[0].

Interrupts
The following interrupt types can be enabled with the IER register.
- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)

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- Transmitter Holding Register Empty at/below threshold (in Programmable THRE Interrupt mode)
- Modem Status

DMA Support

The UART supports DMA signaling with the use of two output signals (dma_tx_req_n and dma_rx_req_n) to indicate when data is ready to be read or when the transmit FIFO is empty.

The dma_tx_req_n signal is asserted under the following conditions:

- When the Transmitter Holding Register is empty in non-FIFO mode.
- When the transmitter FIFO is empty in FIFO mode with Programmable THRE interrupt mode disabled.
- When the transmitter FIFO is at, or below the programmed threshold with Programmable THRE interrupt mode enabled.

The dma_rx_req_n signal is asserted under the following conditions:

- When there is a single character available in the Receive Buffer Register in non-FIFO mode.
- When the Receiver FIFO is at or above the programmed trigger level in FIFO mode.

Auto Flow Control

The UART can be configured to have a 16750-compatible Auto RTS and Auto CTS serial data flow control mode available. If FIFOs are not implemented, then this mode cannot be selected. When Auto Flow Control mode has been selected, it can be enabled with the Modem Control Register (MCR[5]). Following figure shows a block diagram of the Auto Flow Control functionality.

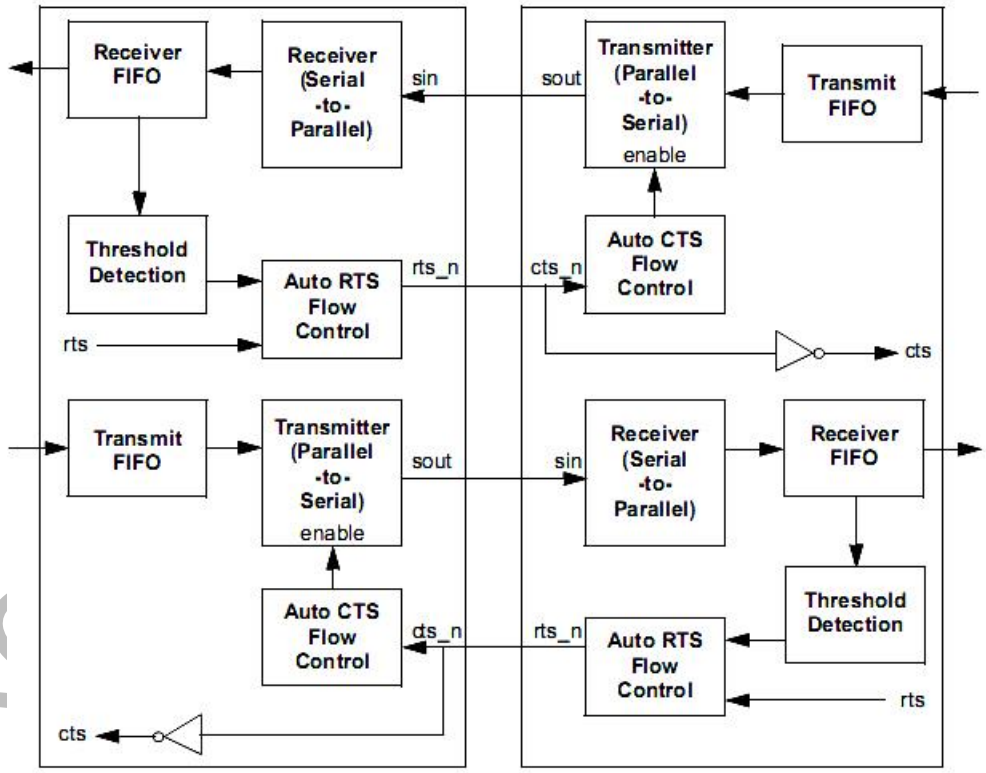

Fig. 33-4 UART Auto Flow Control Block Diagram

Auto RTS – Becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- RTS (MCR[1] bit and MCR[5]bit are both set)
- FIFOs are enabled (FCR[0]) bit is set)
- SIR mode is disabled (MCR[6] bit is not set)

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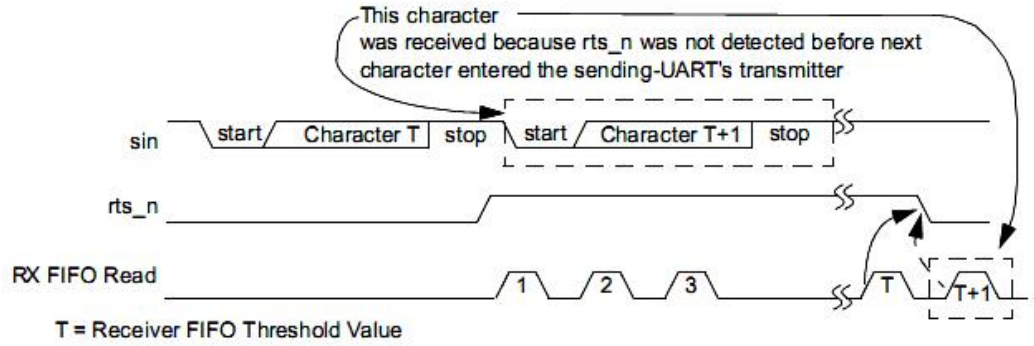

Fig. 33-5 UART AUTO RTS TIMING

Auto CTS – becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- AFCE (MCR[5] bit is set)
- FIFOs are enabled through FIFO Control Register FCR[0] bit
- SIR mode is disabled (MCR[6] bit is not set)

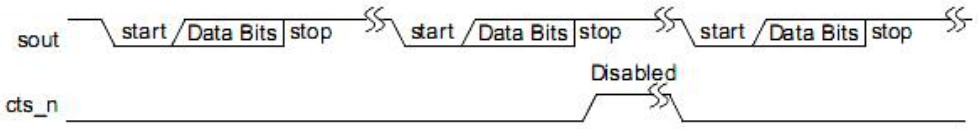

Fig. 33-6 UART AUTO CTS TIMING

RS485 Mode

The RS485 standard supports serial communication over a twisted pair configuration. The difference between the RS232 and RS485 standards is its use of a balanced line for transmission. This usage is also known as the differential format that sends the same signal on two separate lines with phase delay and then compares the signals at the end, subtracts any noise, and adds them to regain signal strength. This process allows the RS485 standard to be viable over significantly longer distances than its short range RS232 counterpart.

UART supports hardware mode and software mode.

- Hardware mode, DE and RE are mutually exclusive. By default 'de' and 're' will be disabled. When at user mode, user should programs the DE to active the 'de', while at auto mode, DE will assert when transfer starts. Once the TX FIFO becomes empty and the stop bit be sampled, 're' signal gets enabled and 'de' signal will be disabled, automatically. In this mode, hardware will consider the de-inactive timing and turn around timing, which are programmed in the DET and TAT register, respectively. When 'de' is valid, it is useless to configure RE, and vice versa.
- Software mode, transmit and receive can happen simultaneously. The user can enable DE, RE at any point of time. Turn around timing as programmed in the TAT register and de-inactive timing as programmed in the DET are not applicable in this mode.

33.4 Register Description

33.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
UART0	0xff0a0000
UART1	0xff0b0000
UART2	0xff0c0000
UART3	0xff0d0000
UART4	0xff0e0000

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Name	Base Address
UART5	0xff4e0000

33.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
UART_RBR	0x0000	W	0x00000000	Receive Buffer Register
UART_DLL	0x0000	W	0x00000000	Divisor Latch Low
UART_THR	0x0000	W	0x00000000	Transmit Buffer Register
UART_DLH	0x0004	W	0x00000000	Divisor Latch High
UART_IER	0x0004	W	0x00000000	Interrupt Enable Register
UART_FCR	0x0008	W	0x00000000	FIFO Enable
UART_IIR	0x0008	W	0x00000001	Interrupt Identity Register
UART_LCR	0x000C	W	0x00000000	Line Control Register
UART_MCR	0x0010	W	0x00000000	Modem Control Register
UART_LSR	0x0014	W	0x00000060	Line Status Register
UART_MSR	0x0018	W	0x00000000	Modem Status Register
UART_SCR	0x001C	W	0x00000000	Scratchpad Register
UART_SRBR	0x0030	W	0x00000000	Shadow Receive Buffer Register
UART_STHR	0x0030	W	0x00000000	Shadow Transmit Holding Register
UART_FAR	0x0070	W	0x00000000	FIFO Access Register
UART_TFR	0x0074	W	0x00000000	Transmit FIFO Read
UART_RFW	0x0078	W	0x00000000	Receive FIFO write
UART_USR	0x007C	W	0x00000006	UART Status Register
UART_TFL	0x0080	W	0x00000000	Transmit FIFO level
UART_RFL	0x0084	W	0x00000000	Receive FIFO level
UART_SRR	0x0088	W	0x00000000	Software Reset Register
UART_SRTS	0x008C	W	0x00000000	Shadow Request to Send
UART_SBCR	0x0090	W	0x00000000	Shadow Break Control Register
UART_SDMAM	0x0094	W	0x00000000	Shadow DMA Mode
UART_SFE	0x0098	W	0x00000000	Shadow FIFO enable
UART_SRT	0x009C	W	0x00000000	Shadow RCVR Trigger
UART_STET	0x00A0	W	0x00000000	Shadow TX Empty Trigger
UART_HTX	0x00A4	W	0x00000000	Halt TX
UART_DMASA	0x00A8	W	0x00000000	DMA Software Acknowledge
UART_TCR	0x00AC	W	0x00000000	Transceiver Control Register
UART_DE	0x00B0	W	0x00000000	Driver Output Enable Register
UART_RE	0x00B4	W	0x00000000	Receiver Output Enable Register
UART_DET	0x00B8	W	0x00000000	Driver Output Enable Timing Register
UART_TAT	0x00BC	W	0x00000000	Turn Around Timing Register
UART_CPR	0x00F4	W	0x00043FF2	Component Parameter Register
UART_UCV	0x00F8	W	0x3430322A	UART Component Version
UART_CTR	0x00FC	W	0x44570110	Component Type Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

33.4.3 Detail Registers Description

UART_RBR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	data_input Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

UART_DLL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	baud_rate_divisor_l Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

UART_THR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	data_output Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full.. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_DLH

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	baud_rate_divisor_h Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

UART_IER

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	prog_thre_int_en Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. 1'b0: Disabled 1'b1: Enabled
6:4	RO	0x0	reserved
3	RW	0x0	modem_status_int_en Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	receive_line_status_int_en Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
1	RW	0x0	trans_hold_empty_int_en Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	receive_data_available_int_en Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1'b0: Disabled 1'b1: Enabled

UART_FCR

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Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	WO	0x0	rcvr_trigger At which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to "DMA Support". The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full
5:4	WO	0x0	tx_empty_trigger TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to "DMA Support". The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full
3	WO	0x0	dma_mode DMA Mode. This determines the DMA signaling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support. 1'b0: Mode 0 1'b1: Mode 1
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	fifo_en FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

UART_IIR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	fifos_en FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 2'b00: Disabled 2'b11: Enabled
5:4	RO	0x0	reserved
3:0	RO	0x1	int_id Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 4'b0000: Modem status 4'b0001: No interrupt pending 4'b0010: THR empty 4'b0100: Received data available 4'b0110: Receiver line status 4'b0111: Busy detect 4'b1100: Character timeout The interrupt priorities are split into four levels that are detailed in Table X. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

UART_LCR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	div_lat_access Divisor Latch Access Bit. Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	RW	0x0	break_ctrl Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	RW	0x0	stick_parity If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	RW	0x0	even_parity_sel Even Parity Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.

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Bit	Attr	Reset Value	Description
3	RW	0x0	parity_en Parity Enable. Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 1'b0: Parity disabled 1'b1: Parity enabled
2	RW	0x0	stop_bits_num Number of stop bits. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 1'b0: 1 stop bit. 1'b1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit.
1:0	RW	0x0	data_length_sel Data Length Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 2'b00: 5 bits 2'b01: 6 bits 2'b10: 7 bits 2'b11: 8 bits

UART_MCR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sir_mode_en SIR Mode Enable. Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in "IrDA 1.0 SIR Protocol". 1'b0: IrDA SIR Mode disabled 1'b1: IrDA SIR Mode enabled
5	RW	0x0	auto_flow_ctrl_en Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in "Auto Flow Control". 1'b0: Auto Flow Control Mode disabled 1'b1: Auto Flow Control Mode enabled

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Bit	Attr	Reset Value	Description
4	RW	0x0	loopback LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	RW	0x0	out2 OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 1'b0: Out2_n de-asserted (logic 1) 1'b1: Out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	RW	0x0	out1 OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 1'b0: Out1_n de-asserted (logic 1) 1'b1: Out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	RW	0x0	req_to_send Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	RW	0x0	data_terminal_ready Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 1'b0: dtr_n de-asserted (logic 1) 1'b1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive

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UART_LSR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	receiver_fifo_error Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 1'b0: No error in RX FIFO 1'b1: Error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	RO	0x1	trans_empty Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	RO	0x1	trans_hold_reg_empty Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	RO	0x0	break_int Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.

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Bit	Attr	Reset Value	Description
3	RO	0x0	framing_error Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No framing error 1'b1: Framing error Reading the LSR clears the FE bit.
2	RO	0x0	parity_error Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No parity error 1'b1: Parity error Reading the LSR clears the PE bit.
1	RO	0x0	overrun_error Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 1'b0: No overrun error 1'b1: Overrun error Reading the LSR clears the OE bit.
0	RO	0x0	data_ready Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 1'b0: No data ready 1'b1: Data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

UART_MSR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RO	0x0	data_carrior_detect Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 1'b0: dcd_n input is de-asserted (logic 1) 1'b1: dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	RO	0x0	ring_indicator Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 1'b0: ri_n input is de-asserted (logic 1) 1'b1: ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	RO	0x0	data_set_ready Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the UART. 1'b0: dsr_n input is de-asserted (logic 1) 1'b1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	RO	0x0	clear_to_send Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART. 1'b0: cts_n input is de-asserted (logic 1) 1'b1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RO	0x0	delta_data_carrier_detect Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 1'b0: No change on dcd_n since last read of MSR 1'b1: Change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.

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Bit	Attr	Reset Value	Description
2	RO	0x0	trailing_edge_ring_indicator Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 1'b0: No change on ri_n since last read of MSR 1'b1: Change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	RO	0x0	delta_data_set_ready Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 1'b0: No change on dsr_n since last read of MSR 1'b1: Change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RO	0x0	delta_clear_to_send Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 1'b0: No change on ctsdsr_n since last read of MSR 1'b1: Change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

UART_SCR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	temp_store_space Scratchpad register. This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

UART_SRBR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	shadow_rbr This is a shadow register for the RBR and has been allocated sixteen 32-bit locations (0x30-0x6c) so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE !=

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Bit	Attr	Reset Value	Description
			NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs.

UART_STHR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	shadow_thr This is a shadow register for the THR and has been allocated sixteen 32-bit locations(0x30-0x6c) so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_FAR

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fifo_access_test_en Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 1'b0: FIFO access mode disabled 1'b1: FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty.

UART_TFR

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	trans_fifo_read Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR.

UART_RFW

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	WO	0x0	receive_fifo_framing_error Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	WO	0x0	receive_fifo_parity_error Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	WO	0x00	receive_fifo_write Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

UART_USR

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	receive_fifo_full Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. 1'b0: Receive FIFO not full 1'b1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	RO	0x0	receive_fifo_not_empty Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. 1'b0: Receive FIFO is empty 1'b1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.

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Bit	Attr	Reset Value	Description
2	RO	0x1	trasn_fifo_empty Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	RO	0x1	trans_fifo_not_full Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. 1'b0: Transmit FIFO is full 1'b1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	RO	0x0	uart_busy UART Busy. This is indicates that a serial transfer is in progress, when cleared indicates that the UART is idle or inactive. 1'b0: UART is idle or inactive 1'b1: UART is busy (actively transferring data) Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the UART has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the UART. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock.

UART_TFL

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	trans_fifo_level Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.

UART_RFL

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	receive_fifo_level Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.

UART_SRR

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	uart_reset UART Reset. This asynchronously resets the UART and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.

UART_SRTS

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_req_to_send Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.

UART_SBCR

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	shadow_break_ctrl Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver.

UART_SDMAM

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_dma_mode Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). 1'b0: Mode 0 1'b1: Mode 1

UART_SFE

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_fifo_en Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.

UART_SRT

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	shadow_rcvr_trigger Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported:

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Bit	Attr	Reset Value	Description
			2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full

UART_STET

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	shadow_tx_empty_trigger Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full

UART_HTX

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	halt_tx_en This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 1'b0: Halt TX disabled 1'b1: Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation.

UART_DMASA

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	dma_software_ack This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

UART_TCR

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	auto_de Assert DE Automatically Enable. When data is written to the TXFIFO, the DE will automatically asserted, meanwhile, the RE will automatically de-asserted. 1'b0: Disable. 1'b1: Enable.
4	RW	0x0	re_pol Receiver Enable Polarity. 1'b0: re signal is active low. 1'b1: re signal is active high.
3	RW	0x0	de_pol Driver Enable Polarity. 1'b0: de signal is active high. 1'b1: de signal is active low.
2	RW	0x0	xfer_mode Transfer Mode. 1'b0: Hardware mode, DE and RE are mutually exclusive. By default 'de' and 're' will be disabled. User should programs the DE to active the 'de'. Once the TX FIFO becomes empty and the stop bit be sampled, 're' signal gets enabled and 'de' signal will be disabled, automatically. In this mode, hardware will consider the de-inactive timing and turn around timing (applied for 4 wire mode only), which are programmed in the DET and TAT register, respectively. When 'de' is valid, it is useless to configure RE, and vice versa. 1'b1: Software mode, transmit and receive can happen simultaneously. The user can enable DE, RE at any point of time. Turn around timing as programmed in the TAT register and de-inactive timing as programmed in the DET are not applicable in this mode.
1	RW	0x0	re_en Receiver Enable. 1'b0: RE signal disable, DE control both transmit and receive process. Correspondingly, assert DE for transmit state, while de-assert DE for receive state. In this scenario, RE-associated logics and TAT register will hold constant for lower power consumption. 1'b1: RE signal enable, DE control the transmit process, and RE control the receive process.
0	RW	0x0	rs485_en RS485 Enable. 1'b0: In this mode, the transfers are still in the RS232 mode. The registers of DE, RE, DET and TAT are reserved. 1'b1: In this mode, the transfers will happen in RS485 mode.

UART_DE

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	de The 'de' register bit is used to control assertion and de-assertion of 'de' signal. 1'b0: De-assert 'de' signal. 1'b1: Assert 'de' signal.

UART_RE

Address: **Operational Base** + offset (0x00B4)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	re The 're' register bit is used to control assertion and de-assertion of 're' signal. 1'b0: De-assert 're' signal. 1'b1: Assert 're' signal.

UART_DET

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	de_inact_time This field controls the amount of time (in terms of number of pclk periods) between the finish flag after the sampling point of the stop bit on the sout to the falling edge of Driver output enable signal. Note that, the mentioned finish flag, i.e. the actual starting effective point of the count, is located at the position of (DLL+1) sclk periods before the full stop bit ends, followed by 3~4 synchronization pclk periods. The actual time is the programmed value + 1.

UART_TAT

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	de2re_time Turn around time (in terms of pclk) for DE De-assertion to RE assertion. The actual time is the programmed value + 1.

UART_CPR

Address: **Operational Base** + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x04	fifo_mode 8'h4 means FIFO mode is 64.
15:14	RO	0x0	reserved
13	RO	0x1	dma_extra 1'b1 means DMA_EXTRA enabled.
12	RO	0x1	uart_add_encoded_params 1'b1 means UART_ADD_ENCODED_PARAMS enabled.
11	RO	0x1	shadow 1'b1 means SHADOW mode enabled.
10	RO	0x1	fifo_stat 1'b1 means FIFO_STAT enabled.
9	RO	0x1	fifo_access 1'b1 means FIFO ACCESS enabled.
8	RO	0x1	new_feat 1'b1 means Additional features enabled.
7	RO	0x1	sir_lp_mode 1'b1 means SIR_LP mode enabled.
6	RO	0x1	sir_mode 1'b1 means SIR mode enabled.
5	RO	0x1	thre_mode 1'b1 means THRE mode enabled.

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Bit	Attr	Reset Value	Description
4	RO	0x1	afce_mode 1'b1 means AFCE mode enabled.
3:2	RO	0x0	reserved
1:0	RO	0x2	apb_data_width 2'b10 means APB data width is 32bit.

UART_UCV

Address: **Operational Base** + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3430322a	ver ASCII value for each number in the version.

UART_CTR

Address: **Operational Base** + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x44570110	peripheral_id This register contains the peripherals identification code.

33.5 Interface Description

Table 33-1 UART0 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
uart0_rx	I	GPIO0_C7	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[15:12]=4'h2
uart0_tx	O	GPIO0_C6	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[11:8]=4'h2

Notes: I=input, O=output, I/O=input/output.

Table 33-2 UART1 Rockchip Matrix IO Interface Description

Module Pin	Dir	Rockchip Matrix IO	IOMUX Setting
IOMUX0			
uart_rx	I	RM_IO	
uart_tx	O	RM_IO	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

Table 33-3 UART2 Rockchip Matrix IO Interface Description

Module Pin	Dir	Rockchip Matrix IO	IOMUX Setting
IOMUX0			
uart_rx	I	RM_IO	
uart_tx	O	RM_IO	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

Table 33-4 UART3 Rockchip Matrix IO Interface Description

Module Pin	Dir	Rockchip Matrix IO	IOMUX Setting
IOMUX0			
uart_rx	I	RM_IO	
uart_tx	O	RM_IO	
uart_cts_n	I	RM_IO	
uart_re	O		
uart_rts_n	O	RM_IO	
uart_de			

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

Table 33-5 UART4 Rockchip Matrix IO Interface Description

Module Pin	Dir	Rockchip Matrix IO	IOMUX Setting

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IOMUX0			
uart_rx	I	RM_IO	
uart_tx	O	RM_IO	
uart_cts_n	I	RM_IO	
uart_re	O		
uart_rts_n	O	RM_IO	
uart_de	O		

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

Table 33-6 UART5 Rockchip Matrix IO Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
uart_rx	I	GPIO3_B4	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[15:12] = 4'h1
uart_tx	O	GPIO3_B3	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[3:0] = 4'h1
uart_cts_n	I	GPIO3_B2	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[11:8] = 4'h1
uart_re	O		
uart_rts_n	O	GPIO3_B5	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[7:4] = 4'h1
uart_de	O		
IOMUX1			
uart_rx	I	GPIO1_D3	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[15:12] = 4'h6
uart_tx	O	GPIO1_D2	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[11:8] = 4'h6
uart_cts_n	I	GPIO1_B1	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[7:4] = 4'h6
uart_re	O		
uart_rts_n	O	GPIO1_D1	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[7:4] = 4'h6
uart_de	O		

Notes: I=input, O=output, I/O=input/output.

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33.6 Application Notes

33.6.1 No FIFO Mode Transfer Flow

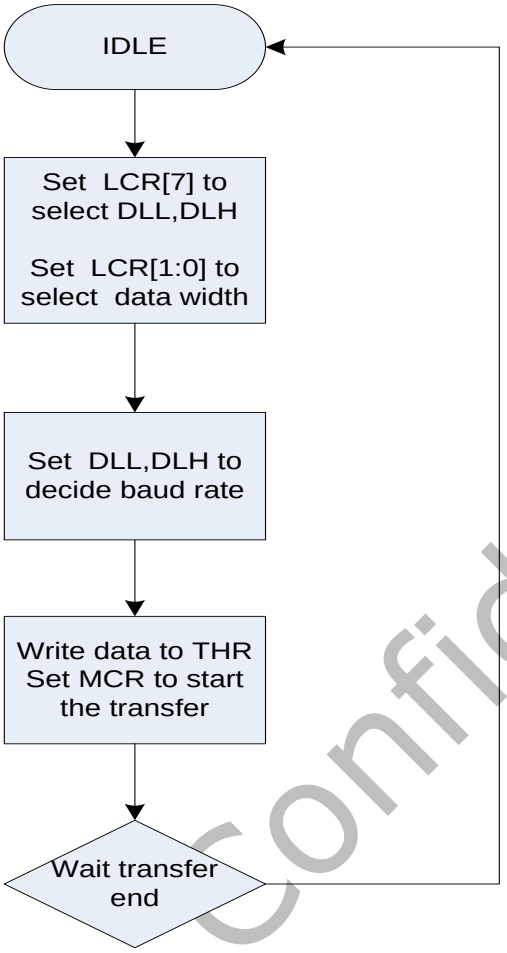

Fig. 33-7 UART None FIFO Mode

33.6.2 FIFO Mode Transfer Flow

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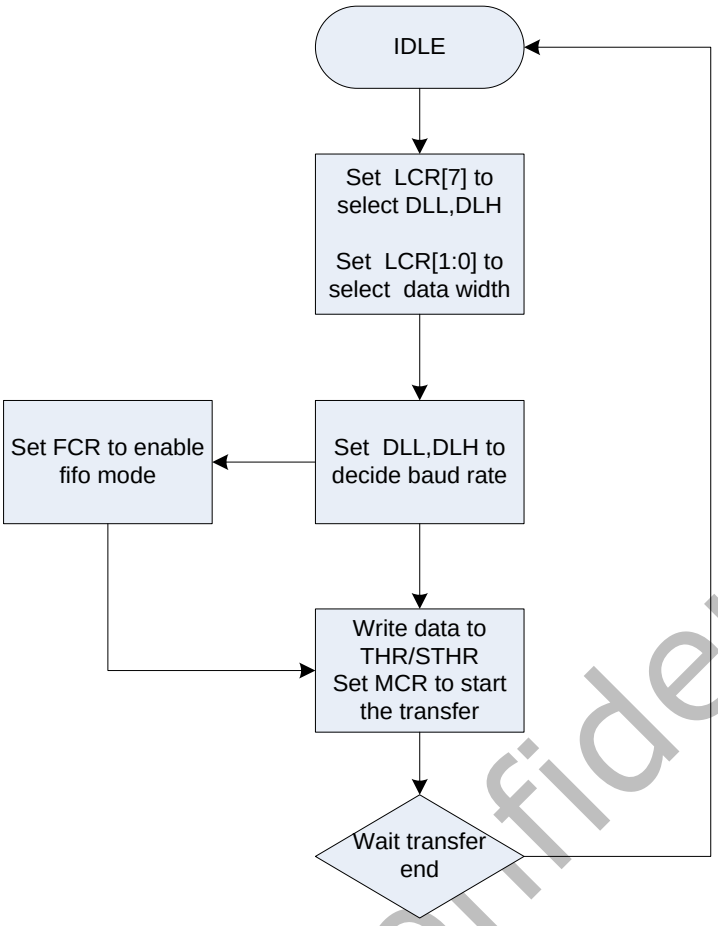

Fig. 33-8 UART FIFO Mode

The UART is an APB slave performing:

Serial-to-parallel conversion on data received from a peripheral device. Parallel-to-serial conversion on data transmitted to the peripheral device. The CPU reads and writes data and control/status information through the APB interface. The transmitting and receiving paths are buffered with internal FIFO memories enabling up to 64-bytes to be stored independently in both transmit and receive modes. A baud rate generator can generate a common transmit and receive internal clock input. The baud rates will depend on the internal clock frequency. The UART will also provide transmit, receive and exception interrupts to system. A DMA interface is implemented for improving the system performance.

33.6.3 Baud Rate Calculation

UART clock generation

UARTs source clocks (SCLK) can be selected from different PLL outputs, or from XIN24M. SCLK can be divided to different frequency, please refer to CRU chapter.

UART baud rate configuration

The following table provides some reference configuration for different UART baud rates.

Table 33-7 UART Baud Rate Configuration

Baud Rate	Reference Configuration
115.2 Kbps	Configure PLL to get 1188MHz clock output; Divide 1188MHz clock by 1536/24750 to get 73.728MHz clock by shared fractional divider; Divide 73.728MHz clock by 20 to get 3.6864MHz clock by independent integer divider; Configure UART_DLL to 2.
460.8 Kbps	Configure PLL to get 1188MHz clock output; Divide 1188MHz clock by 1536/24750 to get 73.728MHz clock by shared fractional divider; Divide 73.728MHz clock by 10 to get 460.8KHz clock by independent integer divider; Configure UART_DLL to 1.

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921.6 Kbps	Configure PLL to get 1188MHz clock output; Divide 1188MHz clock by 1536/24750 to get 73.728MHz clock by shared fractional divider; Divide 73.728MHz clock by 5 to get 921.6KHz clock by independent integer divider; Configure UART_DLL to 1.
1.5 Mbps	Configure PLL to get 800MHz clock output; Divide 1000MHz clock by 24/100 to get 192MHz clock by shared fractional divider; Divide 192MHz clock by 8 to get 24MHz clock by independent integer divider; Configure UART_DLL to 1.
3 Mbps	Configure PLL to get 800MHz clock output; Divide 1000MHz clock by 24/100 to get 192MHz clock by shared fractional divider; Divide 192MHz clock by 4 to get 48MHz clock by independent integer divider; Configure UART_DLL to 1.
4 Mbps	Configure PLL to get 800MHz clock output; Divide 1000MHz clock by 24/100 to get 192MHz clock by shared fractional divider; Divide 192MHz clock by 3 to get 64MHz clock by independent integer divider; Configure UART_DLL to 1.
8 Mbps	Configure PLL to get 800MHz clock output; Divide 800MHz clock by 16/100 to get 128MHz clock by shared fractional divider; Divide 128MHz clock by 1 to get 128MHz clock by independent integer divider; Configure UART_DLL to 1.

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Chapter 34 Controller Area Network (CAN)

34.1 Overview

CAN (Rockchip Controller Area Network) bus is a robust vehicle bus standard designed to allow microcontrollers and devices to communicate with each other in applications without a host computer. It is a message-based protocol, designed originally for multiplex electrical wiring within automobiles to save on copper, but is also used in many other contexts.
RKCAN controller supports the following features:

- Support CAN and CANFD protocol
- Support AHB slave interface
- Not support AHB master interface
- Support classical and can-fd transmit or receive standard frame
- Support classical and can-fd transmit or receive extended frame
- Support transmit or receive data frame, remote frame, overload frame, error frame and frame interval
- Support transmit or receive error count
- Support acceptance filter
- Support bit error, bit stuffing error, form error, ack error and crc error
- Support interrupt and all interrupt can be masked
- Support controller status query
- Support error code check
- Support self test mode
- Support single sample and three sample configurable
- Support SJW(reSynchronization Jump Width) configurable
- Support BRP(system prescaler coefficient) configurable
- Support bit timing configurable
- Support loop-back mode for self-test operation
- Support silent mode for debug
- Support auto retransmission mode
- Support auto bus on after bus-off state
- Support 2 transmit buffers
- Support Internal Storage Mode
- Support protocol exception event
- Support DMA

34.2 Function Description

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

34.2.1 Block Diagram

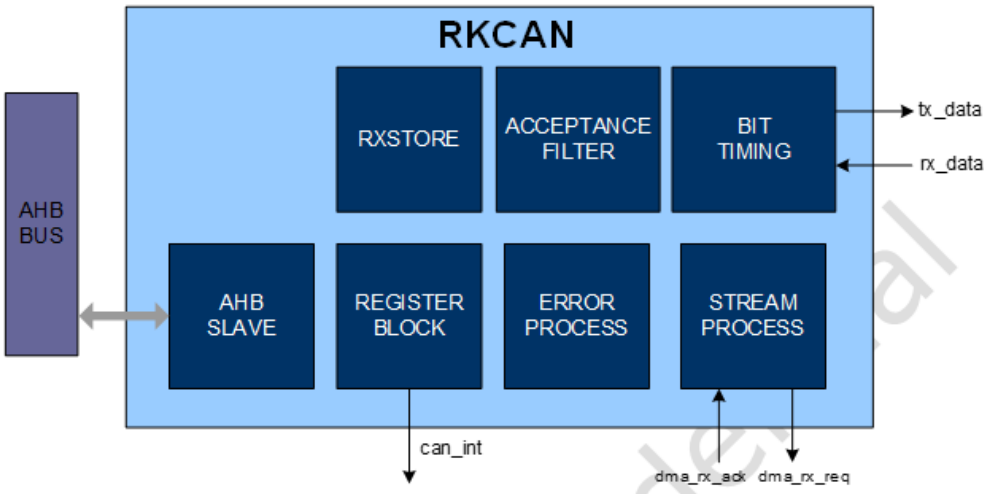

Fig. 34-1 RKCAN Controller Block Diagram

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This version of RKCAN controller includes the previous version of CAN logic in compliance with old software application and also includes new CANFD logic which support transmitting and receiving both CAN and CANFD frame.

34.2.2 ACCEPTANCE FILTER

The Acceptance Filter (ATF) is a receive filter module. RKCAN can filter the received CAN frames based on four identifiers: ID, RTR, and DLC. There are five sets of ID_RTR registers and one set of DLC registers for configuring the filter mode of RKCAN.The filtering mode based on ID and RTR has two types: List Mode and Mask Mode. The current ATF Mask register can be configured as either a mask mode or a list mode through the ATFMn.mask bit.

(1) Mask Mode: ATFM is used as the mask register of ATF, and RKCAN provides five sets of configurable 'filter-mask' registers.

(2) List Mode: ATFM is used as the filter register, and RKCAN provides ten configurable 'filter' registers."

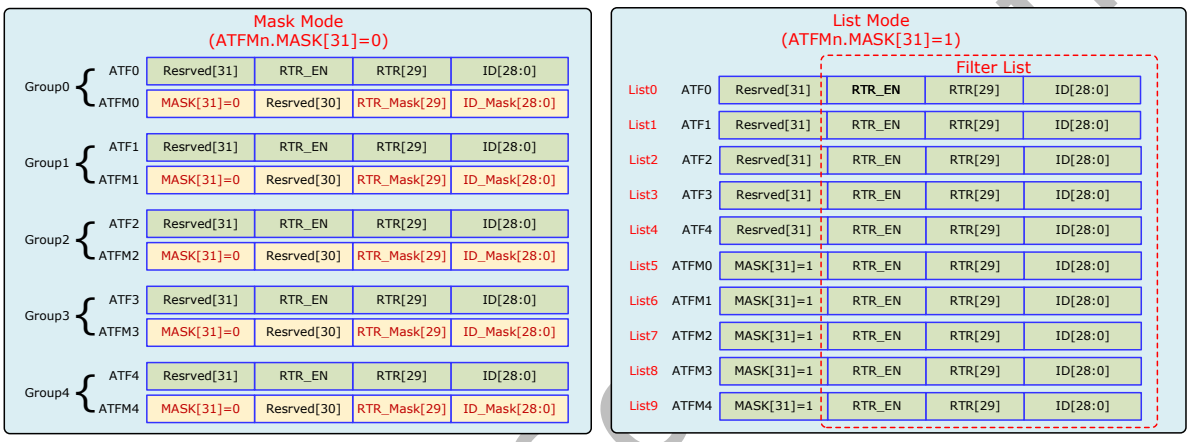

Fig. 34-2 ATF Mode

When filtering based on DLC, there are also two modes: Over Mode and Less Mode. The ATF_DLC.en bit is used to enable the DLC filter, the ARF_DLC.mode bit is used to select between the two modes, and the ATF_DLC.dlc[3:0] is used to configure the filter threshold.

(1) Over Mode: When ARF_DLC.mode is 0, if the dlc value of the received CAN frame is greater than or equal to ATF_DLC.dlc[3:0], the CAN frame can be received by RKCAN and stored in memory.

(2) Less Mode: When ARF_DLC.mode is 1, if the dlc value of the received CAN frame is less than or equal to ATF_DLC.dlc[3:0], the CAN frame can be received by RKCAN and stored in memory.

ATF_CTL[9:0] is used to control the switch status of ATF0~4 and ATFM0~4.

34.2.3 BIT TIMING

34.2.3.1 Bit Timing Logic

The CAN FD protocol defines two bit rates, the first for the ARBITRATION-PHASE with a longer bit time and the second for the data phase with the same or with a shorter bit time. The definition for the first bit rate is the same as for the NOMINAL BIT RATE and the NOMINAL BIT TIME in the CAN protocol specification. The definition for the second bit rate, the DATA BIT RATE WITH the DATA BIT TIME, requires a separate configuration register set.

The bit timing logic controls the sampling point position through the buffer bits in the timing register to ensure the accuracy of the data sampling. The bit timing logic receives the clock frequency division signal for identification, sets the bus timing parameters, establishes synchronization parameters, and adjusts the bus transmission rate. At the same time, the bus is monitored and the message to be sent is transmitted to the bus at the set timing.

According to the provisions of the CAN protocol: the CAN bus is always at a high level when no message is sent, and the continuous recessive bit is monitored on the bus. At this time,

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the bus is in an idle state, and the arbitration priority is low, ready to receive data at any time. When the bus detects a transition from a recessive bit to a dominant bit, it is proved that the frame start bit starts transmitting, and the bus performs a hard synchronization in the bit start sync segment. Then, in the process of receiving the message, once the edge of the transition close to the sampling point is detected and the edge of the edge and the synchronization segment have a phase error lower than the synchronization width (SJW is taken when the value exceeds SJW), the controller executes once resynchronization, resynchronization can be performed multiple times during one data transmission.

34.2.3.2 Bit Timing Definition

The transmission time of each bit is divided into 4 parts:

$$t_{nbt} = t_{sync_seg} + t_{prop_seg} + t_{phase_seg1} + t_{phase_seg2}$$

t_{sync_seg}, t_{prop_seg}, t_{phase_seg1} and t_{phase_seg2} are integer multiples of the unit time(t_{sclk}), and this unit time is a specific multiple of the system clock, which is determined by the division factor BRP in the bus timing register: 1. The counter is obtained by the BRP operation; 2. The system clock clk is counted by the counter; 3. When the limit is reached, a clock with a period of t_{sclk} is generated.

In the system design, considering the cyclical occurrence of each time period, a state machine with three states is used in the bit timing design. The three states correspond to the sync segment(sync_seg) and the phase buffer segment 1 (phase_seg1=phase_seg1+prog_seg) and the phase buffer segment 2 (phase_seg2), respectively. Where PHASE_SEG1 range: 1~16; PHASE_SEG2 range: 1~8; BRP range: 1~64.

$$t_{sync_seg} = 1 \times t_{sclk}$$

$$t_{prop_seg} + t_{phase_seg1} = t_{sclk} \times (8 \times TSEG1.3 + 4 \times TSEG1.2 + 2 \times TSEG1.1 + TSEG1.0 + 1)$$

$$t_{phase_seg2} = t_{sclk} \times (4 \times TSEG2.2 + 2 \times TSEG2.1 + TSEG1.0 + 1)$$

Define a counter to count t_{sclk}. When the count reaches the TSEG1, TSEG2 defined in the bus timing register and the length of the synchronization segment defined in the design, the system will generate the corresponding transition conditions: go_seg1, go_seg2, go_sync.

By judging these transition conditions, the control state machine cycles through the above three states.

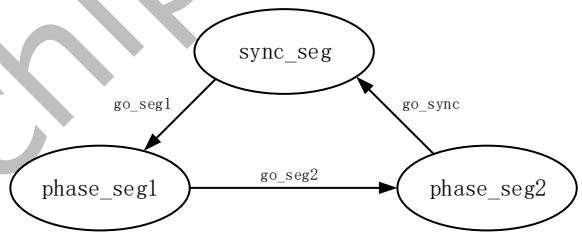

Fig. 34-3 Bit timing FSM

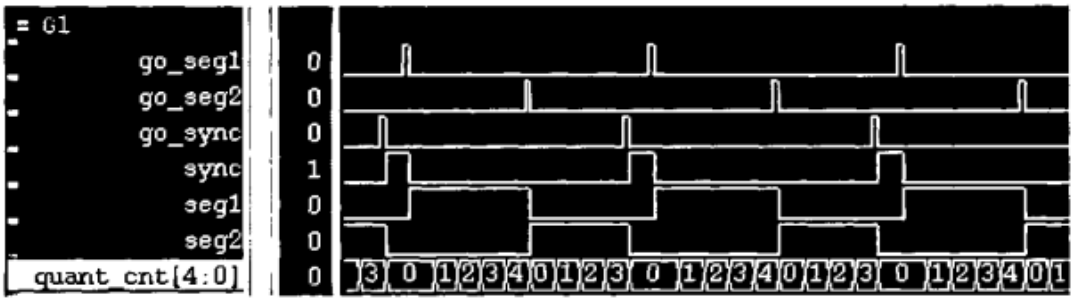

Fig. 34-4 Bit timing waveform diagram

34.2.3.3 Bit time transition

The first part of a CAN FD frame, until the BRS bit, is transmitted with the NOMINAL BIT RATE. The bit rate is switched if the BRS bit is recessive, until the CRC DELIMITER is reached or until the CAN FD controller sees an error condition that results in the starting

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of an ERROR FRAME. CAN FD ERROR FRAMES, as well as ACK FIELD, END OF FRAME, OVERLOAD FRAMES, and all frames in CAN format are transmitted with the NOMINAL BIT RATE.

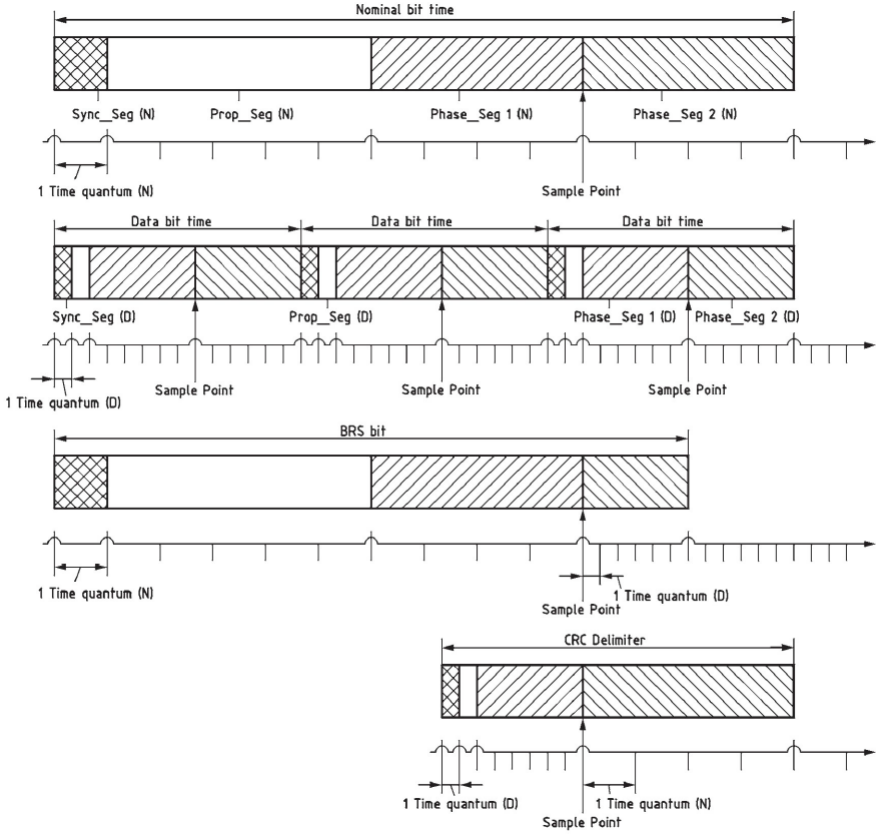
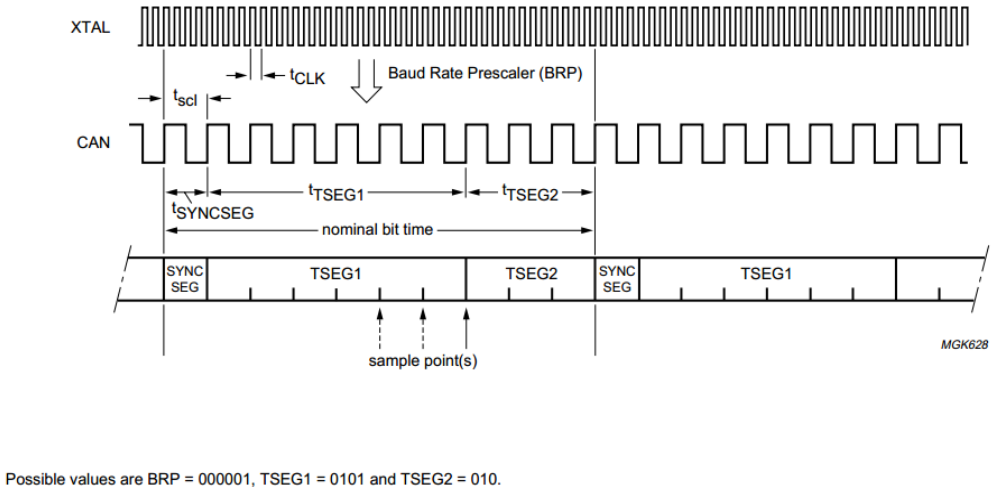


Fig. 34-5 Bit Timing

34.2.3.4 Sampling Point and Sending Point

Sampling Point: According to the agreement, the sample point sample_point should be between phase_seg1 and phase_seg2. It is designed to be in the position of phase_seg2 synchronization. The sampling pulse width is defined as one system clock cycle. Considering the accuracy of sampling, you can use the method of taking three samples to take the mean. The interval between each sample point is one t_{sclk}.



Possible values are BRP = 000001, TSEG1 = 0101 and TSEG2 = 010.

Fig. 34-6 Three sampling diagram

Sending Point: The location of the transmission point(tx_point) should be at the beginning of each bit time according to the protocol, and it is designed to synchronize it with the go_sync signal. In addition, if it is in sync or resynchronize, tx_point will be valid immediately.

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34.2.3.5 Bit Synchronization

With the synchronization method, one or more nodes that satisfy the synchronization condition align their synchronization segments with the transmission data on the bus at a specific time. Synchronization occurs on the 1-to-0 transition edge in order to control the distance from the transition edge to the sample point. Two synchronization methods are defined in the CAN bus communication protocol: hard synchronization and resynchronization.

Hard_sync: All nodes must be synchronized to the leading edge of the starting frame of the node that first started transmitting the message. At the beginning of each frame of data, a synchronization action is taken between the nodes.

Hard synchronization implementation method: determine whether the bus state meets the frame start condition specified in the protocol, and the node is not in the state of the data to be transmitted. At this time, a hard synchronization flag signal hard_sync is generated, and the pulse width is a system clock; The hard_sync entry is added to the control condition of the go_seg1 signal, and go_seg1 is valid immediately when the hard_sync signal is '1'. Therefore, once the hard synchronization condition is met, the system enters the phase_seg1 segment, thereby achieving synchronization.

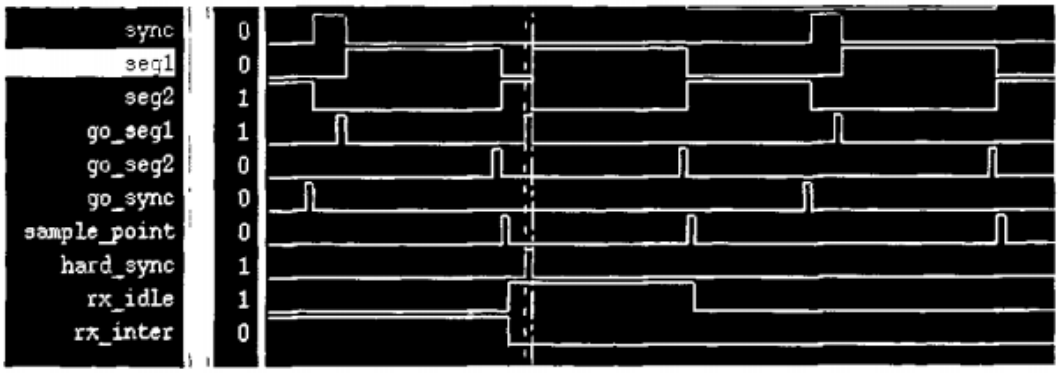

Fig. 34-7 Hard_sync waveform diagram

Resynchronization: In addition to generating hard synchronization at the beginning of each frame of data, the CAN bus communication protocol also specifies the transmission of data for each frame. When the timing coordination between the nodes is not ideal, it will be resynchronized, so that the cooperation between the nodes is in a good state.

For the receiver, the bus changes it received should occur in the sync segment. Once the receiver's status violates this rule, the receiver will perform a resynchronization.

Two situations that require resynchronization:

1. The jump of the bus value '1' to '0' occurs between the sync segment and the sample point, which is a delay jump;
2. The jump of the bus value '1' to '0' occurs between the sample point and the sync segment, which is an early jump.

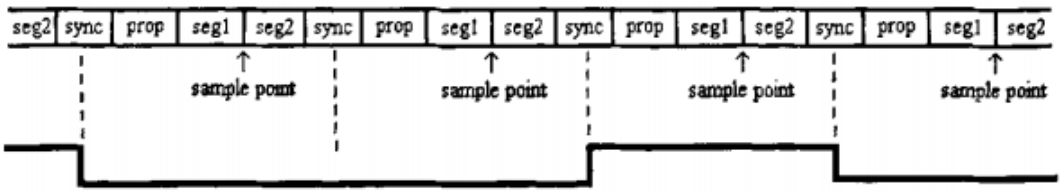

Fig. 34-8 Resynchronization

Resynchronization method:

1. Condition for resynchronization: the receiver is in a mode of receiving data (not inter-frame space or bus idle), and a resynchronization flag signal ‘resync’ is generated when a jump of the bus value '1' to '0' occurs;
2. According to the position of the resynchronization flag signal, it is determined that the abnormal jump is a delay jump or an early jump;
3. Counting the delay or the length of the advance by the counter;
4. In this bit, phase_seg1 is added with a delay time or phase_seg2 is subtracted from the advance time to obtain a new phase buffer time for the bit, thereby achieving synchronization.

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34.2.3.6 Transmitter Delay Compensation

During the data phase of a CAN FD transmission, only one node is transmitting; all others are receiving. Therefore, the propagation delay does not limit the maximum data rate. When transmitting via pin, TXCAN, the CAN FD Controller module receives the transmitted data from its local CAN transceiver via pin, RXCAN. The received data are delayed by the CAN
transceiver's loop delay. In case this delay is greater than 1 + DTSEG1, a bit error will be detected.
In order to enable a data phase bit time that is shorter than the transceiver loop delay, the Transmitter Delay Compensation (TDC) is implemented. Instead of sampling after DTSEG1, a
Secondary Sample Point (SSP) is calculated and used for sampling during the data phase of a
CAN FD message.

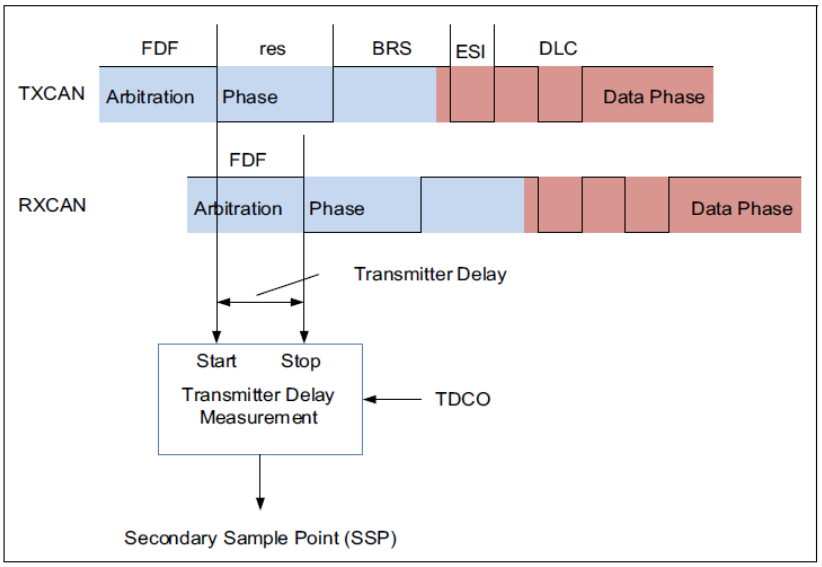

Fig. 34-9 Measurement of Transceiver Delay

34.2.4 RXSTORE

34.2.4.1 Internal Storage Mode

To store the frame data received by RKCAN only in the internal SRAM, the STR_CTL.stm needs to be configured as 0. The frame data received by RKCAN will only be stored in the internal SRAM. The size of the internal SRAM is 256x32bit. The CPU can query the remaining amount of data in the internal SRAM through the STR_STAT.intm_left_cnt register. After the CPU reads the data, the STR_STAT.intm_left_cnt will decrease accordingly. At the same time, the way the internal SRAM stores data can be divided into four data storage formats: Flexible, CAN Fixed, CANFD Fixed, and Mixed. Use STR_CTL_ism_sel[1:0] to select among the four formats, the specific explanations are as follows:

(1) Flexible: The data of each frame is seamlessly stored in the SRAM according to its volume.

(2) CAN Fixed: A fixed 4 words are used to store a frame of data.

(3) CANFD Fixed: A fixed 18 words are used to store a frame of data.

(4) Mixed: CAN frames use 4 words to store a frame of data, and CANFD frames use 18 words to store a frame of data. It should be noted that when the external storage mode is turned on, the internal SRAM will still be used for data caching, and the STR_CTL_ism_sel[1:0] can still be used to select the format of the data cached in the internal SRAM, but the external memory uses a fixed 18

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words to store a frame of data.

34.2.4.2 External Storage Mode

To store the frame data received by RKCAN in external memory (DDR or System Memory), the STORE_CTL.stm needs to be configured as 1, and registers such as TXTHR, START_ADDR, and EXTM_SIZE need to be configured. RKCAN will first store the received frame data in the internal SRAM. When the amount of data received by RKCAN exceeds the threshold set by TXTHR, it will automatically write the data stored in the internal SRAM to the external memory through AHB Master, and update the WADDR register to the tail address of the part of the external memory that has been written with data. At the same time, it updates the status of the two empty/full flags STR_STAT.extm_empty and STR_STAT.extm_full. RKCAN sends an interrupt to the CPU. The CPU can determine the amount of data that can be read by querying the value of the WADDR register. After the CPU completes the frame data reading, it needs to write the latest CPU_RD_ADDR value into the RADDR register of RKCAN. RKCAN will calculate the empty/full status of the memory based on the values of the RADDR and WADDR registers. The CPU can query the amount of data in the external memory through STR_STAT.extm_left_cnt, and query the remaining amount of data in the internal SRAM through STR_STAT.intm_left_cnt.

This feature is currently only used for debugging. For specific application details, please consult Rockchip.

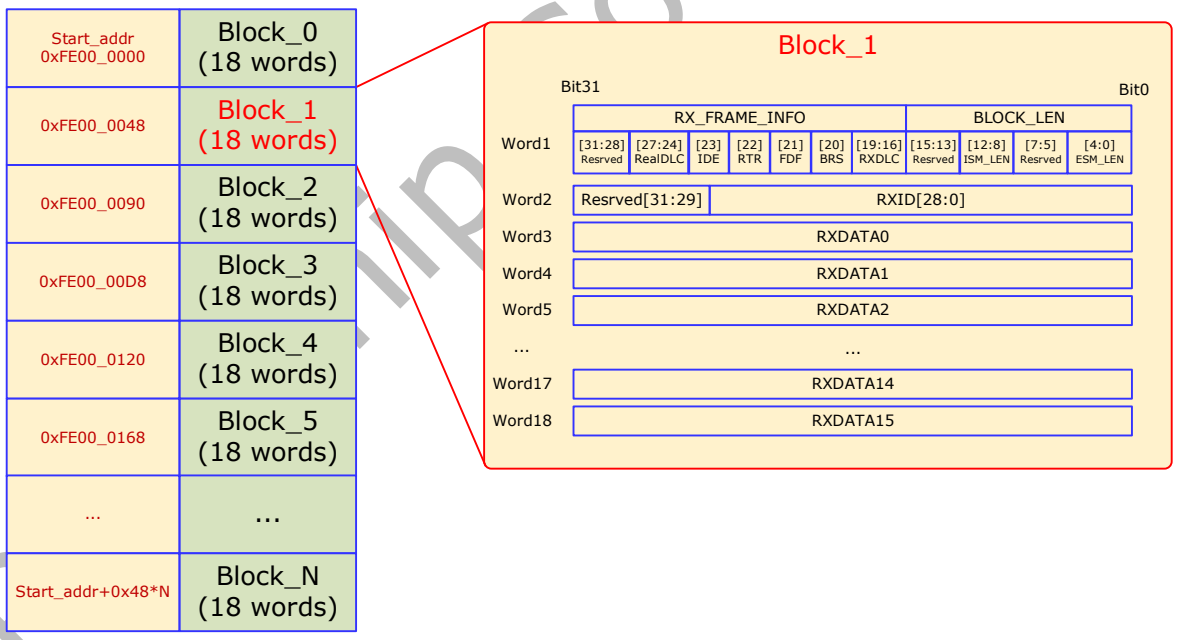

Fig. 34-10 Data storage format under external storage mode

34.2.4.3 ESM Timeout Mechanism

RKCAN also has a timeout mechanism to prevent the RKCAN receive buffer from overflowing when the CPU does not read data for a long time. The timeout threshold is configured through the BUF_TIMEOUT register. In internal storage mode, if the CPU does not read the data in the internal SRAM for a long time, a timeout interrupt will occur; in external storage mode, if the CPU does not update the value of the CPU_RD_ADDR register for a long time, a timeout interrupt will occur. The same interrupt flag is used in both modes.

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34.2.5 ERROR PROCESS

There are five types of errors. Multiple errors can occur at the same time.

- **BIT ERROR**:
  A unit that is sending a bit on the bus also monitors the bus. A BIT ERROR has to be detected at that bit time, when the bit value that is monitored is different form the bit value that is sent. An exception is the sending of a 'recessive' bit during the stuffed bit stream of the ARBITRATION FIELD of during the ACK SLOT. Then no BIT ERROR occurs when a 'dominant' bit is monitored. A TRANSMITTER sending a PASSIVE ERROR FLAG and detecting a 'dominant' bit does not interpret this as a BIT ERROR.
- **BIT STUFF ERROR**:
  A STUFF ERROR has to be detected at the bit time of the 6th consecutive equal bit level in a message field that should be coded by the method of bit stuffing.
- **FORM ERROR**:
  A FORM ERROR has to be detected when a fixed-form bit field contains one or more illegal bits. (Exception is the detection of a dominant bit during the last bit of END OF FRAME by a RECEIVER, or the detection of a dominant bit during the last bit of ERROR DELIMITER or OVERLOAD DELIMITER by any node). When the value of a fixed STUFF-BIT in the CAN FD format CRC SEQUENCE is equal to its preceding bit, this shall also be detected as a FORM-ERROR.
- **ACK ERROR**:
  An ACK ERROR has to be detected by a transmitter whenever it does not monitor a 'dominant' bit during the ACK SLOT.
- **CRC ERROR**:
  The CRC sequence consists of the result of the CRC calculation by the transmitter. The receivers calculate the CRC in the same way as the transmitter. A CRC ERROR has to be detected, if the calculated result is not the same as that received in the CRC sequence.

34.3 Register Description

34.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows. address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
CAN0 base address	0xFF320000
CAN1 base address	0xFF330000

34.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKCAN_MODE	0x0000	W	0x00000000	Mode Configure Register
RKCAN_CMD	0x0004	W	0x00000000	Request Command Register
RKCAN_STATE	0x0008	W	0x00000000	Controller State Register
RKCAN_INT	0x000C	W	0x00000000	Interrupt State Register
RKCAN_INT_MASK	0x0010	W	0x00000000	Interrupt Mask Registers
RKCAN_FD_NOMINAL_BIT_TIMING	0x0100	W	0x00000000	CANFD Nominal Bit Timing Configure Register
RKCAN_FD_DATA_BITTIMING	0x0104	W	0x00000000	CANFD Data Bit Timing Configure Register
RKCAN_FD_TDC	0x0108	W	0x00000000	Transmitter Delay Compensation Configure Register
RKCAN_FD_BRS_CFG	0x010C	W	0x0000000B	Transmitter Delay Compensation Configure Register
RKCAN_FD_LOOP_CNT	0x0110	W	0x00000000	Transmitter Delay Compensation Configure Register

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Name	Offset	Size	Reset Value	Description
RKCAN_DMA_CTRL	0x011C	W	0x00000000	DMA Mode Control Register
RKCAN_FD_TXFRAMEINFO	0x0200	W	0x00000000	CANFD TX Frame Information Configuration Register
RKCAN_FD_TXID	0x0204	W	0x00000000	CANFD Transmit ID Register
RKCAN_FD_TXDATA0	0x0208	W	0x00000000	CANFD Transmit DATA0
RKCAN_FD_TXDATA1	0x020C	W	0x00000000	CANFD Transmit DATA1
RKCAN_FD_TXDATA2	0x0210	W	0x00000000	CANFD Transmit DATA2
RKCAN_FD_TXDATA3	0x0214	W	0x00000000	CANFD Transmit DATA3
RKCAN_FD_TXDATA4	0x0218	W	0x00000000	CANFD Transmit DATA4
RKCAN_FD_TXDATA5	0x021C	W	0x00000000	CANFD Transmit DATA5
RKCAN_FD_TXDATA6	0x0220	W	0x00000000	CANFD Transmit DATA6
RKCAN_FD_TXDATA7	0x0224	W	0x00000000	CANFD Transmit DATA7
RKCAN_FD_TXDATA8	0x0228	W	0x00000000	CANFD Transmit DATA8
RKCAN_FD_TXDATA9	0x022C	W	0x00000000	CANFD Transmit DATA9
RKCAN_FD_TXDATA10	0x0230	W	0x00000000	CANFD Transmit DATA10
RKCAN_FD_TXDATA11	0x0234	W	0x00000000	CANFD Transmit DATA11
RKCAN_FD_TXDATA12	0x0238	W	0x00000000	CANFD Transmit DATA12
RKCAN_FD_TXDATA13	0x023C	W	0x00000000	CANFD Transmit DATA13
RKCAN_FD_TXDATA14	0x0240	W	0x00000000	CANFD Transmit DATA14
RKCAN_FD_TXDATA15	0x0244	W	0x00000000	CANFD Transmit DATA15
RKCAN_FD_RXFRAMEINFO	0x0300	W	0x00000000	CANFD RX Frame Information Configuration Register
RKCAN_FD_RXID	0x0304	W	0x00000000	CANFD Receive ID
RKCAN_FD_RXTIMESTAMP	0x0308	W	0x00000000	CANFD Receive Timestamp Reserved
RKCAN_FD_RXDATA0	0x030C	W	0x00000000	CANFD Receive Data Reg0
RKCAN_FD_RXDATA1	0x0310	W	0x00000000	CANFD Receive Data Reg1
RKCAN_FD_RXDATA2	0x0314	W	0x00000000	CANFD Receive Data Reg2
RKCAN_FD_RXDATA3	0x0318	W	0x00000000	CANFD Receive Data Reg3
RKCAN_FD_RXDATA4	0x031C	W	0x00000000	CANFD Receive Data Reg4
RKCAN_FD_RXDATA5	0x0320	W	0x00000000	CANFD Receive Data Reg5
RKCAN_FD_RXDATA6	0x0324	W	0x00000000	CANFD Receive Data Reg6
RKCAN_FD_RXDATA7	0x0328	W	0x00000000	CANFD Receive Data Reg7
RKCAN_FD_RXDATA8	0x032C	W	0x00000000	CANFD Receive Data Reg8
RKCAN_FD_RXDATA9	0x0330	W	0x00000000	CANFD Receive Data Reg9
RKCAN_FD_RXDATA10	0x0334	W	0x00000000	CANFD Receive Data Reg10
RKCAN_FD_RXDATA11	0x0338	W	0x00000000	CANFD Receive Data Reg11
RKCAN_FD_RXDATA12	0x033C	W	0x00000000	CANFD Receive Data Reg12
RKCAN_FD_RXDATA13	0x0340	W	0x00000000	CANFD Receive Data Reg13
RKCAN_FD_RXDATA14	0x0344	W	0x00000000	CANFD Receive Data Reg14
RKCAN_FD_RXDATA15	0x0348	W	0x00000000	CANFD Receive Data Reg15
RKCAN_RX_STR_RDATA	0x0400	W	0x00000000	RX Storage Read Data
RKCAN_STR_CTL	0x0600	W	0x00000080	Storage Ctrl Register
RKCAN_STR_STATE	0x0604	W	0x00000000	Storage Ctrl Register
RKCAN_STR_TIMEOUT	0x0608	W	0x00002710	Storage Timeout Threshold Register
RKCAN_STR_WTM	0x060C	W	0x000168ED	Storage Water Mark Register
RKCAN_EXTM_START_ADDR	0x0610	W	0x00000000	External Memory Start Address
RKCAN_EXTM_SIZE	0x0614	W	0x000001F8	External Memory Size Register
RKCAN_EXTM_WADDR	0x0618	W	0x00000000	External Memory AHB Write Address

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Name	Offset	Size	Reset Value	Description
RKCAN_EXTM_RADDR	0x061C	W	0x00000000	External Memory Soft Read Address
RKCAN_EXTM_AHB_TXTHR	0x0620	W	0x00000000	AHB Master Transmit Threshold Level
RKCAN_EXTM_LEFT_CNT	0x0624	W	0x00000000	External Memory Left Counter
RKCAN_ATF0	0x0700	W	0x00000000	Acceptance Filter 0 Code Register
RKCAN_ATF1	0x0704	W	0x00000000	Acceptance Filter 1 Code Register
RKCAN_ATF2	0x0708	W	0x00000000	Acceptance Filter 2 Code Register
RKCAN_ATF3	0x070C	W	0x00000000	Acceptance Filter 3 Code Register
RKCAN_ATF4	0x0710	W	0x00000000	Acceptance Filter 4 Code Register
RKCAN_ATFM0	0x0714	W	0x1FFFFFFF	Acceptance Filter 0 Mask Register
RKCAN_ATFM1	0x0718	W	0x1FFFFFFF	Acceptance Filter 1 Mask Register
RKCAN_ATFM2	0x071C	W	0x1FFFFFFF	Acceptance Filter 2 Mask Register
RKCAN_ATFM3	0x0720	W	0x1FFFFFFF	Acceptance Filter 3 Mask Register
RKCAN_ATFM4	0x0724	W	0x1FFFFFFF	Acceptance Filter 4 Mask Register
RKCAN_ATF_DLC	0x0728	W	0x00000000	Acceptance DLC Filter Function
RKCAN_ATF_CTL	0x072C	W	0x00000000	Acceptance Filter Configure Register
RKCAN_AUTO_RETX_CFG	0x0808	W	0x00000320	Configure Register for Auto Retransmission Function
RKCAN_AUTO_RETX_STATE0	0x080C	W	0x00000000	Auto Retransmission Status Register 0
RKCAN_AUTO_RETX_STATE1	0x0810	W	0x00000000	Auto Retransmission Status Register 0
RKCAN_OLF_CFG	0x0814	W	0x00000000	Overload Frame Configuration Register
RKCAN_RXINT_CTRL	0x0818	W	0x00000100	Multi Frame Interrupt(MFI) Configure Register
RKCAN_RXINT_TIMEOUT	0x081C	W	0x0000FFFF	MFI Timeout Threshold Register
RKCAN_ERROR_CODE	0x0900	W	0x00000000	RX Error Code Register
RKCAN_ERROR_MASK	0x0904	W	0x00000000	Error Mask Register
RKCAN_RXERRORCNT	0x0910	W	0x00000000	Receive Error Counter Register
RKCAN_TXERRORCNT	0x0914	W	0x00000000	Transmit Error Counter Register
RKCAN_ARBIT_FAIL_STATE	0x0918	W	0x00000000	Arbiter Fail Code Register
RKCAN_RTL_VERSION	0x0F0C	W	0xCFDBA0EB	CAN RTL version

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

34.3.3 Detail Registers Description

RKCAN_MODE

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	noack_mode When noack_mode is enabled, if the internal receive buffer of RKCAN is full and a new frame is received, RKCAN will no longer respond with an ACK. 1'b0: Disable 1'b1: Enable
14	RW	0x0	force_passive_err Force RKCAN into error passive station 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
13	RW	0x0	force_active_err Force RKCAN into error active station 1'b0: Disable 1'b1: Enable
12	RW	0x0	crcerr_pass_mode 1'b0: Send Passive Error when CRC Error detected 1'b1: Not send Passive Error when CRC Error detected
11	RW	0x0	crcerr_ack_mode 1'b0: Not send ACK when CRC Error detected 1'b1: Send ACK when CRC Error detected
10	RW	0x0	pass_err_mode 1'b0: PASSIVE Error Flag use recessive bits 1'b1: PASSIVE Error Flag use dominant bits
9	RW	0x0	dis_pee Disable Protocol Exception Event Detection/Generation 1'b0: PEE detection/generation is enabled. If the CANFD receiver detects the res bit as 1, it goes to Bus Integration state (PEE_config) and waits for Bus Idle condition (11 consecutive nominal recessive bits). The error counter remains unchanged. 1'b1: Disable Protocol Exception Event detection/generation by CANFD receiver if "res" bit in CANFD frame is detected as 1. In this case, CANFD receiver generates Form error.
8	RW	0x0	rett_mode Restricted Operation Mode In Restricted Operation Mode, RKCAN is able to transmit and to receive DATA FRAMES and REMOTE FRAMES and it gives ACKNOWLEDGE to valid frames, but it does not send ACTIVE ERROR FRAMES or OVERLOAD FRAMES. The error counters are not incremented or decremented. 1'b0: Disable 1'b1: Enable
7	RW	0x0	auto_bus_on Auto Bus On Enable 1'b0: After the RKCAN has entered bus_off state, the software can start a bus_off_recovery sequence by resetting the work_mode to 0. 1'b1: Automatic reset TEC/REC to bus_on after 128 occurrence of 11 consecutive recessive bits have been monitored on the bus.
6	RO	0x0	reserved
5	RW	0x0	rxstx_mode Receive Self Transmit data mode 1'b0: Disable 1'b1: Enable. When the RKCAN sends data, it can also receive the data sent by itself.
4	RW	0x0	lback_mode Loopback Mode 1'b0: Disable 1'b1: Enable
3	RW	0x0	silent_mode Silent Mode 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	self_test Reserved Self check ACK slot when TX frame Using ERROR_MASK[4]can achieve the same function When in self_test mode, the receiver does not need to return an ACK signal when receiving data. Therefore, no error ack will occur in self_test mode. When in 'lback_mode' or 'silent_mode', it needs to enable 'self_test' mode when sending frame.
1	RW	0x0	sleep_mode Sleep Mode This is the Sleep mode request bit 1'b0: No such request 1'b1: Request core to be in Sleep mode This bit is cleared when the core wakes up from Sleep mode.
0	RW	0x0	work_mode Work Mode 1'b0: Idle mode, CAN stop transmit and registers can be configured 1'b1: Work mode, CAN enter the working mode, Receive/transmit data

RKCAN_CMD

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/WSC	0x0	tx1_req Transmit request enable 1'b0: Disable 1'b1: Enable When 'tx1_req' is enable, the RKCAN buffer1 is in the transmit mode and cannot receive frames from other CANs. When the RKCAN buffer1 transmission frame complete, 'tx1_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.
0	R/WSC	0x0	tx0_req Transmit request enable 1'b0: Disable 1'b1: Enable When 'tx0_req' is enable, the RKCAN buffer0 is in the transmit mode and cannot receive frames from other CANs. When the RKCAN buffer0 transmission frame complete, 'tx0_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.

RKCAN_STATE

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	sleep_state Sleep state 1'b0: None 1'b1: CAN controller is in the sleep state

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Bit	Attr	Reset Value	Description
4	RO	0x0	bus_off_state Bus off state 1'b0: None 1'b1: Bus off state: When the error counter is incremented to 255, the CAN controller will enter the bus off state, generate an error warning interrupt and enter reset mode, waiting for the CPU to restart. (rx/tx_err_cnt >=32'd255)
3	RO	0x0	error_warning_state Error warning state 1'b0: None 1'b1: Error state: At least one error counter has reached the error warning threshold (rx/tx_err_cnt >=32'd96)
2	RO	0x0	tx_period Transmit state 1'b0: Not in transmit state 1'b1: CAN controller is in the transmit state
1	RO	0x0	rx_period Receive state 1'b0: Not in receive state 1'b1: CAN controller is in the receive state
0	RO	0x0	tx_buffer_full Transmit buffer full flag bit 1'b0: Not full 1'b1: TX buffer is full. There is data in buffer waiting to be sent or being sent.

RKCAN_INT

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	W1C	0x0	busoff_rcy_int BusOff Timer Recovery Interrupt 1'b0: None 1'b1: BusOff timer recovery Write 1 then clear
18	W1C	0x0	esm_wtm_int External Stotage watermark Interrupt 1'b0: None 1'b1: The data in external storage reaches the watermark Write 1 then clear
17	W1C	0x0	ism_wtm_int Internal Stotage watermark Interrupt 1'b0: None 1'b1: The data in internal storage reaches the watermark Write 1 then clear
16	W1C	0x0	busint_int Enter Bus Integration Interrupt 1'b0: None 1'b1: Indicates RKCAN enter the bus integration state. Write 1 then clear
15	W1C	0x0	rxstr_timeout_int RX Storage Timeout Interrupt 1'b0: None 1'b1: Indicates that data remain in rx storage timeout. Write 1 then clear

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Bit	Attr	Reset Value	Description
14	W1C	0x0	mfi_timeout_int Multi Frame Interrupt(MFI) Mode Timeout Interrupt
13	W1C	0x0	mfi_int Multi Frame Interrupt(MFI)
12	W1C	0x0	auto_retx_fail_int Automatic Transmit Failure Interrupt
11	W1C	0x0	wakeup_int Wakeup Interrupt 1'b0: None 1'b1: Indicates that the core entered Normal mode from Sleep mode. Write 1 then clear
10	W1C	0x0	bus_off_recovery_int Bus off Recover Interrupt 1'b0: None 1'b1: Indicates that the core is recovered from Bus-off mode Write 1 then clear
9	W1C	0x0	bus_off_int Bus Off Interrupt 1'b0: None 1'b1: Indicates that the CAN core entered Bus-off mode Write 1 then clear
8	W1C	0x0	rxstr_overflow_int RX Storage Overflow Interrupt. 1'b0: None 1'b1: Indicates that a message has been lost. This condition occurs when a new message with ID matching to Receive Storage is received and the Receive Storage is full. Write 1 then clear
7	W1C	0x0	rxstr_full_int RX Storage full Interrupt. 1'b0: None 1'b1: Indicates that RX Storage is full based on watermark setting Write 1 then clear
6	W1C	0x0	error_int Bus Error Interrupt 1'b0: None 1'b1: CAN bus error interrupt. This interrupt is generated when a bus error is detected. Error details can refer to the ERROR_CODE register. Write 1 then clear
5	W1C	0x0	tx_arbit_fail_int Transmit Arbitration loss Interrupt 1'b0: None 1'b1: Arbitration loss interrupt. This interrupt is generated when the loss of arbitration is turned into a receiver Write 1 then clear
4	W1C	0x0	passive_error_int Passive Error Interrupt 1'b0: None 1'b1: Passive error interrupt. This interrupt is generated when the controller enters an error passive state (at least one error counter reaches 127) or returns from the error passive state to the error active state. Write 1 then clear

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Bit	Attr	Reset Value	Description
3	W1C	0x0	overload_int Overload Frame Interrupt 1'b0: None 1'b1: CAN bus overload interrupt. This interrupt is generated when a overload frame is generated. Write 1 then clear
2	W1C	0x0	error_warning_int Error warning interrupt 1'b0: None 1'b1: Error_warning_int. This interrupt is generated when the error_warning_state bits change. Write 1 then clear
1	W1C	0x0	tx_finish_int Transmit finish interrupt 1'b0: None 1'b1: Transmit finish interrupt. CAN controller sends the message. Write 1 then clear
0	W1C	0x0	rx_finish_int Receive Finish Interrupt 1'b0: None 1'b1: Receive finish int. CAN controller has received the message and the rx_buffer is full. Write 1 then clear

RKCAN_INT_MASK

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	busoff_rcy_int_mask 1'b0: Unmasked 1'b1: Masked
18	RW	0x0	esm_wtm_int_mask 1'b0: Unmasked 1'b1: Masked
17	RW	0x0	ism_wtm_int_mask 1'b0: Unmasked 1'b1: Masked
16	RW	0x0	busint_int_mask 1'b0: Unmasked 1'b1: Masked
15	RW	0x0	rxstr_timeout_int_mask 1'b0: Unmasked 1'b1: Masked
14	RW	0x0	mfi_timeout_int_mask 1'b0: Unmasked 1'b1: Masked
13	RW	0x0	mfi_int_mask 1'b0: Unmasked 1'b1: Masked
12	RW	0x0	auto_retx_fail_int_mask 1'b0: Unmasked 1'b1: Masked

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Bit	Attr	Reset Value	Description
11	RW	0x0	wakeup_int_mask 1'b0: Unmasked 1'b1: Masked
10	RW	0x0	bus_off_recovery_int_mask 1'b0: Unmasked 1'b1: Masked
9	RW	0x0	bus_off_int_mask 1'b0: Unmasked 1'b1: Masked
8	RW	0x0	rxstr_overflow_int_mask 1'b0: Unmasked 1'b1: Masked
7	RW	0x0	rxstr_full_int_mask 1'b0: Unmasked 1'b1: Masked
6	RW	0x0	error_int_mask 1'b0: Unmasked 1'b1: Masked
5	RW	0x0	tx_arbit_fail_int_mask 1'b0: Unmasked 1'b1: Masked
4	RW	0x0	passive_error_int_mask 1'b0: Unmasked 1'b1: Masked
3	RW	0x0	overload_int_mask 1'b0: Unmasked 1'b1: Masked
2	RW	0x0	error_warning_int_mask 1'b0: Unmasked 1'b1: Masked
1	RW	0x0	tx_finish_int_mask 1'b0: Unmasked 1'b1: Masked
0	RW	0x0	rx_finish_int_mask 1'b0: Unmasked 1'b1: Masked

RKCAN_FD_NOMINAL_BITTIMING

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	sample_mode RKCAN controller sampling mode configuration register. When enabling triple sampling, it is necessary to configure the positions of two additional sampling points using the FD_BRS_CFG[30:5] register. 1'b0: Single sample mode 1'b1: Three sample mode
30:24	RW	0x00	sjw SJW: Resynchronization Jump Width Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error.
23:16	RW	0x00	brq brp: system prescale coefficient Tsclk = 2 x Tclk x (brp + 1)

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:8	RW	0x00	tseg2 Phase buffer segment 2 Tphase_seg2 = Tsclk x (tseg2 + 1)
7:0	RW	0x00	tseg1 Phase buffer segment 1 Tphase_seg1 = Tsclk x (tseg1 + 1)

RKCAN_FD_DATA_BITTIMING

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	brs_tseg1 tseg1 for BRS Bit
23	RW	0x0	brs_mode BRS bit sampling point setting 1'b0: Sampling BRS bit according to the position specified in the protocol 1'b1: The sampling point of BRS bit will be advanced
22	RW	0x0	ackslot_sync_dis 1'b0: Enable Hardsync when ACK_SLOT 1'b1: Disable Hardsync when ACK_SLOT
21	RO	0x0	reserved
20:17	RW	0x0	sjw SJW: Resynchronization Jump Width Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error.
16:9	RW	0x00	brq brp: system prescale coefficient Tsclk = 2 x Tclk x (brp + 1)
8:5	RW	0x0	tseg2 Phase buffer segment 2 Tphase_seg2 = Tsclk x (tseg2 + 1)
4:0	RW	0x00	tseg1 Phase buffer segment 1 Tphase_seg1 = Tsclk x (tseg1 + 1)

RKCAN_FD_TDC

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	lcnt_clr Loop Delay Counter Clear
7	RW	0x0	lcnt_meas_en Loop Delay Counter Enable
6:1	RW	0x00	tdc_offset Transmitter Delay Compensation Offset This offset is specified in CAN clock cycles and is added to the measured transmitter delay to place the Secondary Sample Point (SSP) at appropriate position (for example, set this to half data bit time in terms of CAN clock cycles to place SSP in the middle of the data bit).

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Bit	Attr	Reset Value	Description
0	RW	0x0	tdc_enable Transmitter Delay Compensation (TDC) Enable 1'b0: TDC is disabled 1'b1: Enables TDC function as specified in the CAN FD standard

RKCAN_FD_BRS_CFG

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31	RW	0x0	triple_sync_mode ReSync Enable for triple_sample mode.
30:26	RW	0x00	sp2_dtseg2 Sample Point 2 data phase tseg2
25:18	RW	0x00	sp2_ntseg1 Sample Point 2 tseg1
17:13	RW	0x00	sp1_dtseg2 Sample Point 1 data phase tseg2
12:5	RW	0x00	sp1_ntseg1 Sample Point 1 tseg1
4	RO	0x0	reserved
3	RW	0x1	resync_mode Resync Mode. 1'b0: Resynchronization only on the falling edge 1'b1: Resynchronization on both rising and falling edges
2	RO	0x0	reserved
1	RW	0x1	brs_possync_en BRS Bit Posedge Sync Enable
0	RW	0x1	brs_negsync_en BRS Bit negedge Sync Enable

RKCAN_FD_LOOP_CNT

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	loop_delay_cnt Loop Delay Counter

RKCAN_DMA_CTRL

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	dma_rx_en DMA receive request enable 1'b0: Disable 1'b1: Enable When dma_rx_mode is enable, the RKCAN is in the DMA receive mode. Also, when RKCAN is set work_mode to reset_mode, rx_req is clear.
8:0	RW	0x000	dma_thr DMA transfer start threshold

RKCAN_FD_TXFRAMEINFO

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	txframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RW	0x0	tx_rtr 1'b0: Data frame 1'b1: Remote frame
5	RW	0x0	tx_fdf Extended Data Length/FD Frame Format This bit distinguishes between CAN format and CANFD format frames. 1'b0: CAN format frame 1'b1: CAN FD format frame
4	RW	0x0	tx_brs Bit Rate Switch The BRS bit decides whether the bit rate is switched inside a CAN FD format frame or not (provided BRSD bit is not set in MSR register). 1'b0: Bit rate is not switched inside a CAN FD frame. 1'b1: Bit rate is switched from the standard bit rate of the Arbitration phase to the preconfigured alternate bit rate of the Data phase inside a CAN FD frame. Note: BRS does not exist in CAN format frames and should be set to 0.
3:0	RW	0x0	txdata_length Transmit data length configure register(unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

RKCAN_FD_TXID

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	tx_id can_tx_id[28:0]

RKCAN_FD_TXDATA0

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data0 tx_data0[31:0]

RKCAN_FD_TXDATA1

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Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data1 tx_data1[31:0]

RKCAN_FD_TXDATA2

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data2 tx_data2[31:0]

RKCAN_FD_TXDATA3

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data3 tx_data3[31:0]

RKCAN_FD_TXDATA4

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data4 tx_data4[31:0]

RKCAN_FD_TXDATA5

Address: **Operational Base** + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data5 tx_data5[31:0]

RKCAN_FD_TXDATA6

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data6 tx_data6[31:0]

RKCAN_FD_TXDATA7

Address: **Operational Base** + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data7 tx_data7[31:0]

RKCAN_FD_TXDATA8

Address: **Operational Base** + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data8 tx_data8[31:0]

RKCAN_FD_TXDATA9

Address: **Operational Base** + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data9 tx_data9[31:0]

RKCAN_FD_TXDATA10

Address: **Operational Base** + offset (0x0230)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data10 tx_data10[31:0]

RKCAN_FD_TXDATA11

Address: **Operational Base** + offset (0x0234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data11 tx_data11[31:0]

RKCAN_FD_TXDATA12

Address: **Operational Base** + offset (0x0238)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data12 tx_data12[31:0]

RKCAN_FD_TXDATA13

Address: **Operational Base** + offset (0x023C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data13 tx_data13[31:0]

RKCAN_FD_TXDATA14

Address: **Operational Base** + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data14 tx_data14[31:0]

RKCAN_FD_TXDATA15

Address: **Operational Base** + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data15 tx_data15[31:0]

RKCAN_FD_RXFRAMEINFO

Address: **Operational Base** + offset (0x0300)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	rxframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RO	0x0	rx_rtr 1'b0: Data frame 1'b1: Remote frame
5	RO	0x0	rx_fdf Extended Data Length/FD Frame Format This bit distinguishes between CAN format and CAN FD format frames. 1'b1: CAN FD format frame 1'b0: CAN format frame

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Bit	Attr	Reset Value	Description
4	RO	0x0	rx_brs Bit Rate Switch The BRS bit decides whether the bit rate is switched inside a CAN FD format frame or not (provided BRSD bit is not set in MSR register). 1'b0: Bit rate is not switched inside a CAN FD frame. 1'b1: Bit rate is switched from the standard bit rate of the Arbitration phase to the preconfigured alternate bit rate of the Data phase inside a CAN FD frame. Note: BRS does not exist in CAN format frames and should be set
3:0	RO	0x0	rxdata_length Transmit data length configure register (unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

RKCAN_FD_RXID

Address: **Operational Base** + offset (0x0304)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	rx_id can_rx_id[28:0]

RKCAN_FD_RXTIMESTAMP

Address: **Operational Base** + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	timestamp Reserved

RKCAN_FD_RXDATA0

Address: **Operational Base** + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data0 rx_data0[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA1

Address: **Operational Base** + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data1 rx_data1[31:0] This register refresh after receiving the next frame

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RKCAN_FD_RXDATA2

Address: **Operational Base** + offset (0x0314)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data2 rx_data2[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA3

Address: **Operational Base** + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data3 rx_data3[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA4

Address: **Operational Base** + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data4 rx_data4[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA5

Address: **Operational Base** + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data5 rx_data5[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA6

Address: **Operational Base** + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data6 rx_data6[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA7

Address: **Operational Base** + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data7 rx_data7[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA8

Address: **Operational Base** + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data8 rx_data8[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA9

Address: **Operational Base** + offset (0x0330)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data9 rx_data9[31:0] This register refresh after receiving the next frame

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RKCAN_FD_RXDATA10

Address: **Operational Base** + offset (0x0334)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data10 rx_data10[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA11

Address: **Operational Base** + offset (0x0338)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data11 rx_data11[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA12

Address: **Operational Base** + offset (0x033C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data12 rx_data12[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA13

Address: **Operational Base** + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data13 rx_data13[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA14

Address: **Operational Base** + offset (0x0344)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data14 rx_data14[31:0] This register refresh after receiving the next frame

RKCAN_FD_RXDATA15

Address: **Operational Base** + offset (0x0348)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data15 rx_data15[31:0] This register refresh after receiving the next frame

RKCAN_RX_STR_RDATA

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_str_rdata RX strorage read data value

RKCAN_STR_CTL

Address: **Operational Base** + offset (0x0600)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	str_timeout_mode RX storage not read timeout threshold Mode. 1'b0: Disable 1'b1: Enable
7:6	RW	0x2	esm_sel External Storage Mode(ESM) Data Format Select 2'b00: Flexible 2'b01: CAN Fixed 2'b10: CANFD Fixed 2'b11: Mixed
5	RO	0x0	reserved
4	RW	0x0	srst RX Storage Soft Reset Bit 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	ism_sel Internal Storage Mode(ISM) Data Format Select 2'b00: Flexible; cover_mode must disable 2'b01: CAN Fixed 2'b10: CANFD Fixed 2'b11: Mixed. cover_mode must disable
1	RW	0x0	stm Storage Mode 1'b0: Internal Storage Mode 1'b1: External Storage Mode. RKCAN can use AHB Master interface to write the received frame data to External Memory(DDR or System Memory)
0	RW	0x0	buff_mode_en RX Buffer Mode Enable 1'b0: Disable 1'b1: Enable. RKCAN only a set of RXDATA0~15 registers used as buffers to store received data, instead of internal SRAM or external memory.

RKCAN_STR_STATE

Address: **Operational Base** + offset (0x0604)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:17	RO	0x000	intm_frame_cnt Remaining frame count in RXFIFO. Unit: Frame Only Support when cover_mode disable
16:8	RO	0x000	intm_left_cnt The amount of data remaining in the Internal SRAM. Unit:Word
7:4	RO	0x0	reserved
3	RO	0x0	extm_full External Memory Full Flag 1'b0: Not Full 1'b1: Full
2	RO	0x0	extm_empty External Memory Empty Flag 1'b0: Not Empty 1'b1: Empty

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Bit	Attr	Reset Value	Description
1	RO	0x0	intm_full Internal Memory Full Flag 1'b0: Not Full 1'b1: Full
0	RO	0x0	intm_empty Internal Memory Empty Flag 1'b0: Not Empty 1'b1: Empty

RKCAN_STR_TIMEOUT

Address: **Operational Base** + offset (0x0608)

Bit	Attr	Reset Value	Description
31:0	RW	0x00002710	str_timeout_thr RX storage not read timeout threshold value

RKCAN_STR_WTM

Address: **Operational Base** + offset (0x060C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:9	RW	0x0000b4	esm_watermark External Storage Watermark Register. Unit:Word
8:0	RW	0x0ed	ism_watermark Internal Storage Watermark Register. The configurable range is from 0 to 256. Unit:Word In ISM mode, when the amount of valid data in the RXFIFO is greater than the threshold set by ism_watermark, RKCAN will generate an ism_wtm_int interrupt.

RKCAN_EXTM_START_ADDR

Address: **Operational Base** + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	start_addr External Memory Start Address Used as the Start Address of AHB master output rxdata

RKCAN_EXTM_SIZE

Address: **Operational Base** + offset (0x0614)

Bit	Attr	Reset Value	Description
31:0	RW	0x000001f8	ext_mem_size Configuration size of external storage space. Unit:Word Must be power of 18

RKCAN_EXTM_WADDR

Address: **Operational Base** + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	can_waddr RKCAN AHB Write Address

RKCAN_EXTM_RADDR

Address: **Operational Base** + offset (0x061C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cpu_raddr CPU Read Address

RKCAN_EXTM_AHB_TXTHR

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Address: **Operational Base** + offset (0x0620)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ahb_txthr(V2) When the number of RXFIFO entries is greater than or equal to this value, the RKCAN will automatically transfer the data in the RXFIFO to the external via the AHB Master interface. The value ranges is 0~511.(Unit:byte)

RKCAN_EXTM_LEFT_CNT

Address: **Operational Base** + offset (0x0624)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RO	0x000000	extm_left_cnt The amount of remaining data in external storage.(Unit:Word)

RKCAN_ATF0

Address: **Operational Base** + offset (0x0700)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 0 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATF1

Address: **Operational Base** + offset (0x0704)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 1 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATF2

Address: **Operational Base** + offset (0x0708)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
29	RW	0x0	RTR RTR part of the Acceptance Filter 2 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATF3

Address: **Operational Base** + offset (0x070C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 3 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATF4

Address: **Operational Base** + offset (0x0710)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter 4 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0

RKCAN_ATFM0

Address: **Operational Base** + offset (0x0714)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF0M[30:0] is used to configure the mask filed of each rule for ATF0; 1'b1: List Mode, Register ATF0M[30:0] is used as acceptance filter ATF5.
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M0 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)

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Bit	Attr	Reset Value	Description
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM1

Address: **Operational Base** + offset (0x0718)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF1M[30:0] is used to configure the mask filed of each rule for ATF1; 1'b1: List Mode, Register ATF1M[30:0] is used as acceptance filter ATF6;
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M1 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM2

Address: **Operational Base** + offset (0x071C)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF2M[30:0] is used to configure the mask filed of each rule for ATF2; 1'b1: List Mode, Register ATF2M[30:0] is used as acceptance filter ATF7.
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M2 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM3

Address: **Operational Base** + offset (0x0720)

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Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF3M[30:0] is used to configure the mask filed of each rule for ATF3; 1'b1: List Mode, Register ATF3M[30:0] is used as acceptance filter ATF8.
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M3 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM4

Address: **Operational Base** + offset (0x0724)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF4M[30:0] is used to configure the mask filed of each rule for ATF4; 1'b1: List Mode, Register ATF4M[30:0] is used as acceptance filter ATF9.
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable 1'b1: Enable
29	RW	0x0	RTR RTR part of the Acceptance Filter M4 1'b0: Data Frame 1'b1: Remote Frame(Only CAN Mode)
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATF_DLC

Address: **Operational Base** + offset (0x0728)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	atf_dlc_mode 1'b0: Over Mode, DLC filter process is only passed if the DLC value of the message accepted is equal to or higher than the value of ATF_DLC.atf_dlc; 1'b1: Less Mode, DLC filter process is only passed if the DLC value of the message accepted is equal to or less than the value of ATF_DLC.atf_dlc.

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Bit	Attr	Reset Value	Description
4	RW	0x0	atf_dlc_en DLC Filter Enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	atf_dlc Configure DLC value of received message

RKCAN_ATF_CTL

Address: **Operational Base** + offset (0x072C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	atf9_en Acceptance Filter 9 Disable 1'b0: Disable 1'b1: Enable
8	RW	0x0	atf8_en Acceptance Filter 8 Disable 1'b0: Disable 1'b1: Enable
7	RW	0x0	atf7_en Acceptance Filter 7 Disable 1'b0: Disable 1'b1: Enable
6	RW	0x0	atf6_en Acceptance Filter 6 Disable 1'b0: Disable 1'b1: Enable
5	RW	0x0	atf5_en Acceptance Filter 5 Disable 1'b0: Disable 1'b1: Enable
4	RW	0x0	atf4_en Acceptance Filter 4 Disable 1'b0: Disable 1'b1: Enable
3	RW	0x0	atf3_en Acceptance Filter 3 Disable 1'b0: Disable 1'b1: Enable
2	RW	0x0	atf2_en Acceptance Filter 2 Disable 1'b0: Disable 1'b1: Enable
1	RW	0x0	atf1_en Acceptance Filter 1 Disable 1'b0: Disable 1'b1: Enable
0	RW	0x0	atf0_en Acceptance Filter 0 Enable 1'b0: Disable 1'b1: Enable

RKCAN_AUTO_RETX_CFG

Address: **Operational Base** + offset (0x0808)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	retx_cnt_self_clr retx_cnt clear bit
18:3	RO	0x0064	retx_time_limit Auto Retx Time Threshold
2	RW	0x0	auto_retx_cnt_clr Set to 1 to clear the Auto Retransmission Conter(auto_retx_cnt)
1	RW	0x0	retx_limit_en 1'b0: Diable retx_time_limit. Keep resending until the transmission is successful; 1'b1: Enable retx_time_limit. Stop retransmission when the number of retransmissions reaches the threshold.
0	RW	0x0	auto_retx_mode Auto Retransmission Mode 1'b0: Disable 1'b1: Enable

RKCAN_AUTO_RETX_STATE0

Address: **Operational Base** + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	noack_cnt No ACK Counter
15:0	RO	0x0000	auto_retx_cnt Automatic Retransmission Counter

RKCAN_AUTO_RETX_STATE1

Address: **Operational Base** + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	txerr_cnt TX Error Counter
15:0	RO	0x0000	arbit_fail_cnt Arbit Fail Counter

RKCAN_OLF_CFG

Address: **Operational Base** + offset (0x0814)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	tx_wait_thr Used to configure the number of bits for transmission wait.
15:13	RO	0x0	reserved
12	RO	0x0	tx_wait_clr tx_wait_cnt Clear
11	RO	0x0	tx_wait_mode Transmit wait mode. 1'b0: Immediate transmission 1'b1: Wait for "tx_wait_thr" bits before transmitting
10	RW	0x0	ovd_time 1'b0: Transmit one overload frame at a time 1'b1: Continuously transmit two overload frame at a time
9	RW	0x0	auto_ovd_mode Auto transmit Overload frame mode 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	ovd_tx_thr Overload Frame Transmit Threshold Level. The configurable range is from 0 to 256. Unit:Word When the remaining space of the RXFIFO is less than the threshold set by ovd_tx_thr, RKCAN will automatically send an overload frame.

RKCAN_RXINT_CTRL

Address: **Operational Base** + offset (0x0818)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	mfi_timeout_mode Multi Frame Interrupt(MFI) Timeout Mode 1'b0: Disable 1'b1: Enable
16	RW	0x0	mfi_mode Multi Frame Interrupt(MFI) Mode 1'b0: Generate an interrupt when a frame is received; 1'b1: Generate an interrupt when N frames are received, N is configured by RXINT.rxint_num.
15:0	RW	0x0100	rxint_num Used to configure mulit frame interrupt mode

RKCAN_RXINT_TIMEOUT

Address: **Operational Base** + offset (0x081C)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000ffff	threshold Timeout Threshold for MFI Mode

RKCAN_ERROR_CODE

Address: **Operational Base** + offset (0x0900)

Bit	Attr	Reset Value	Description
31	RW	0x0	tx_crc_error_flag When RKCAN is the transmitter, CRC error is detected. 1'b0: No CRC Error 1'b1: An CRC Error has occurred
30	RW	0x0	rx_crc_error_flag When RKCAN is the receiver, CRC error is detected. 1'b0: No CRC Error 1'b1: An CRC Error has occurred
29	RO	0x0	error_phase 1'b0: Arbitration Phase 1'b1: Data Phase
28:26	RO	0x0	error_type Error type: 3'b000: BIT ERROR 3'b001: BIT STUFF ERROR 3'b010: FORM ERROR 3'b011: ACK ERROR 3'b100: CRC ERROR
25	RW	0x0	error_direction 'error_direction' is used to indicate whether RKCAN was in a sending or receiving state when an error occurred. 1'b0: TX Node 1'b1: RX Node

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Bit	Attr	Reset Value	Description
24:19	RO	0x00	tx_state Indicate the status of TX FSM when an error occurs 6'b000001: TRANSMIT_IDLE 6'b000010: TRANSMIT_SOF_DLC 6'b000100: TRANSMIT_DATA 6'b001000: TRANSMIT_STUFF_COUNT 6'b010000: TRANSMIT_CRC 6'b100000: TRANSMIT_ACK_EOF
18:0	RO	0x00000	rx_state Indicate the status of RX FSM when an error occurs 19'b0000000000000000001: RECEIVE_STOP 19'b0000000000000000010: RECEIVE_BUS_INT 19'b0000000000000000100: RECEIVE_BUS_IDLE 19'b0000000000000001000: RECEIVE_SOF_IDE 19'b0000000000000010000: RECEIVE_ID2_RTR 19'b0000000000000100000: RECEIVE_FDF 19'b0000000000001000000: RECEIVE_RES 19'b0000000000010000000: RECEIVE_BRS_ESI 19'b0000000000100000000: RECEIVE_DLC 19'b0000000001000000000: RECEIVE_DATA 19'b0000000010000000000: RECEIVE_STUFF_COUNT 19'b0000000100000000000: RECEIVE_CRC 19'b0000001000000000000: RECEIVE_CRC_LIM 19'b0000010000000000000: RECEIVE_ACK_SLOT 19'b0000100000000000000: RECEIVE_ACK_LIM 19'b0001000000000000000: RECEIVE_EOF 19'b0010000000000000000: RECEIVE_SPACE 19'b0100000000000000000: RECEIVE_OVERLOAD 19'b1000000000000000000: RECEIVE_ERROR

RKCAN_ERROR_MASK

Address: **Operational Base** + offset (0x0904)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ack_error Error mask for ack error 1'b0: Unmasked 1'b1: Masked
3	RW	0x0	form_error Error mask for form error 1'b0: Unmasked 1'b1: Masked
2	RW	0x0	crc_error Error mask for crc error 1'b0: Unmasked 1'b1: Masked
1	RW	0x0	stuff_error Error mask for stuff error 1'b0: Unmasked 1'b1: Masked
0	RW	0x0	bit_error Error mask for bit error 1'b0: Unmasked 1'b1: Masked

RKCAN_RXERRORCNT

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Address: **Operational Base** + offset (0x0910)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	rx_err_cnt Receive Error Counter (REC) Actual state of the Receive Error Counter. Value between 0 and 127.

RKCAN_TXERRORCNT

Address: **Operational Base** + offset (0x0914)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	tx_err_cnt Transmit Error Counter (TEC) Actual state of the Transmit Error Counter. Value between 0 and 255.

RKCAN_ARBIT_FAIL_STATE

Address: **Operational Base** + offset (0x0918)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	arbit_fail_code This register indicates the bit position of arbitration section where the arbitration was lost.

RKCAN_RTL_VERSION

Address: **Operational Base** + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RO	0xcfdba0eb	version RKCAN Version = 32'hCFD_B_A0_E5

34.4 Interface Description

Table 34-1 CAN IO Interface Description

Module Pin	Direction	Rockchip Matrix IO	IOMUX Setting
CAN0 TX	I/O	RM_IO	
CAN0 RX	I/O	RM_IO	
CAN1 TX	I/O	RM_IO	
CAN1 RX	I/O	RM_IO	

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

34.5 Application Notes

34.5.1 Controller initialization flow

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

After the initialization is completed, the controller enters the working mode, sends the frame to be sent to the buffer, and then sets the "send request" flag of the command register to start transmitting.

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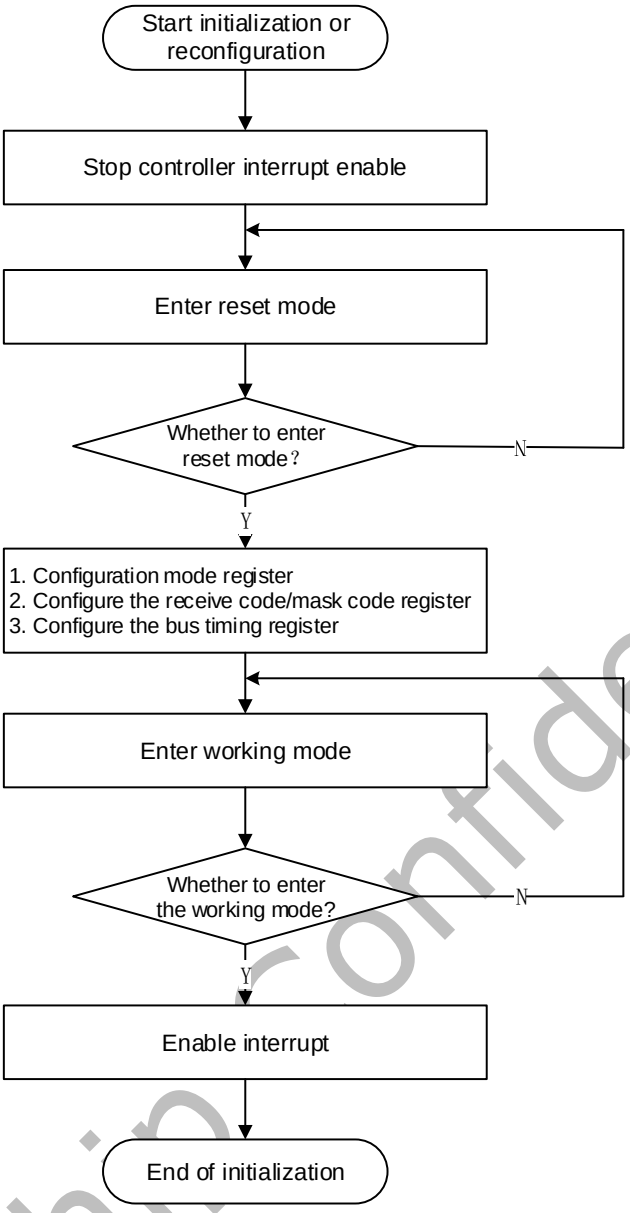

Fig. 34-11 Initialization Flow

34.5.2 Loop-back Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

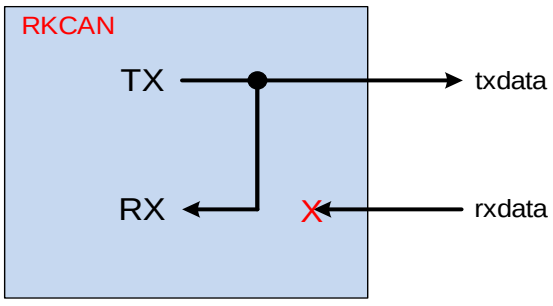

Fig. 34-12 Loop-back Mode

34.5.3 Silent Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

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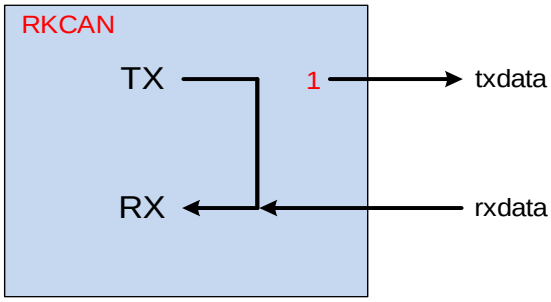

Fig. 34-13 Silent Mode

34.5.4 RXSTX Mode

(1)rxstx_mode=0, RKCAN cannot receive the data sent by itself;
(2)rxstx_mode=1, RKCAN can receive the data sent by itself, and when the ID of the frame is the same as the ID_CODE of RKCAN itself, RKCAN will store the frame information into RX storage.

34.5.5 Auto Retx Mode

RKCAN supports two automatic retransmission modes:

(1) Unlimited Retransmission Mode: There is no limit to the number of retransmissions until the retransmission is successful.

(2) Limited Retransmissions Mode: The threshold for the number of automatic retransmissions can be configured. If the limit threshold is reached and the retransmission is still not successful, the retransmission will stop, and a retransmission failure interrupt will be issued. RKCAN will also count the reasons and corresponding times that cause the transmission failure during the retransmission process, such as arbitration failure, NoACK, or bus error, etc.

34.5.6 Bus Off Recovery Mechanism

RKCAN supports three configurable Bus_off recovery mechanisms, which are:

(1) Automatic Recovery: When the RKCAN node detects 11 recessive bits (no active messages on the CAN bus) appearing consecutively 128 times, it can automatically exit the Bus_off state.

(2) Timed Recovery: The timing length can be set by configuring the register. After the timer expires, RKCAN exits the Bus_off state. The software can implement fast recovery and slow recovery functions using the timed recovery mode.

(3) Manual Recovery: In manual recovery mode, RKCAN will not automatically exit the Bus-off state. It can only exit the Bus-off state by configuring the manual recovery register.

34.5.7 Sleep Mode

After enabling Sleep Mode, RKCAN will automatically enter a low-power mode when the bus is idle, turning off the internal clock. The internal clock will automatically turn on when there is a data frame on the bus or when a data frame needs to be sent.

34.5.8 Multi-frame Mode

RKCAN supports an interrupt being issued upon receiving each frame, and it can also be configured to issue an interrupt only after receiving N frames in multi-frame mode. This can reduce the number of interrupts and reduce software intervention. The related configuration can be found in the register RXINT_CTRL register and RXINT_TIMEOUT.

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Chapter 35 Master Double Data Rate Serial Memory Controller (MASTER DSMC)

35.1 Overview

The DSMC module provides function and operation for interfacing to the DSMC memory devices, and the Rockchip LocalBus devices. The DSMC achieves high speed read/write throughput by double data rate interface.

The main feature is shown below.

- Support the double data rate interface
- Support up to select 4 chips
- Support 8-wire and 16-wire serial transfer mode
- Support configurable write/read contiguous address merging transaction
- Support configurable write/read boundary address splitting transaction
- Support to transform WRAP transfer to INCR transfer
- Support byte access
- Support configurable DQS input clock delay line
- For LocalBus devices, support to assert the selecting signals CS simultaneously in the write transaction
- For LocalBus devices, support 3 clock mode : normal mode, always-on mode, no-edge-clk mode
- For LocalBus devices, support to request DMAC to transfer data when receiving interrupt 0/1
- For LocalBus devices, support configurable serial address width: 16 bits or 32 bits in different region

35.2 Block Diagram

DSMC is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- AXI Interface

The AXI Interface is a XIP interface to access internal device. Its data bus width is 64 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Core

The core module is used to control the data stream of TX/RX datapath.

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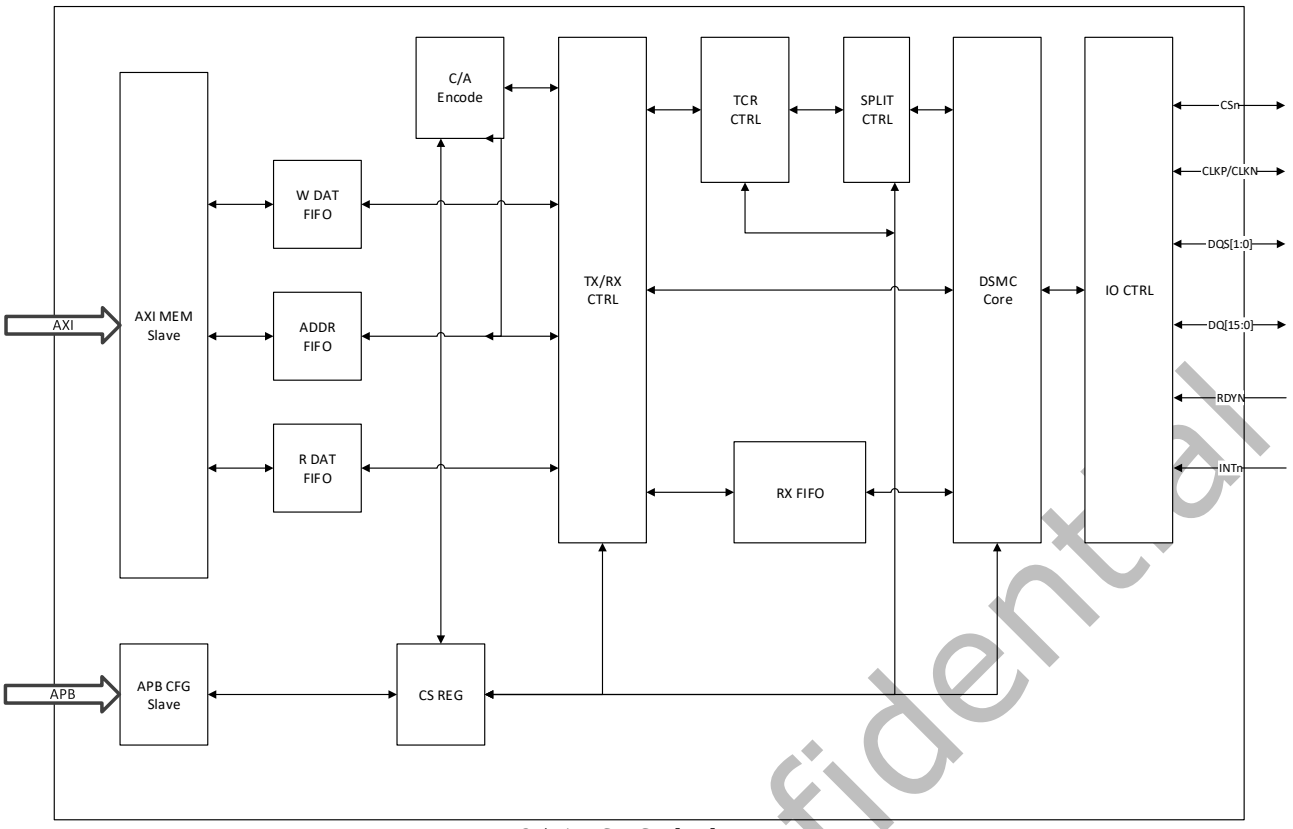

Fig. 35-1 DSMC Block Diagram

35.3 Function Description

The DSMC module is high throughput memory interface. It provides execute in place (XIP) and block copy access to DSMC memory devices (HyperRAM and HyperFlash). The DSMC module is compliant to the Cypress DSMC™ Specification. Meanwhile, it could access Rockchip LocalBus devices, and transfer instructions or bulk data with high speed.

35.3.1 DSMC Core

This section describes physical interface of DSMC module. The DSMC core generates DSMC timing from control signals.

35.3.1.1 Read

DSMC Core module asserts CSn, CLKP/CLKN, and DQ. Then, it outputs 3 words command/address, and reads 1 or more data by the timing of DQS. The DSMC Core puts the transaction request from AXI bus, such as the burst type and the burst length, to the C/A cycle on DSMC as is shown below.

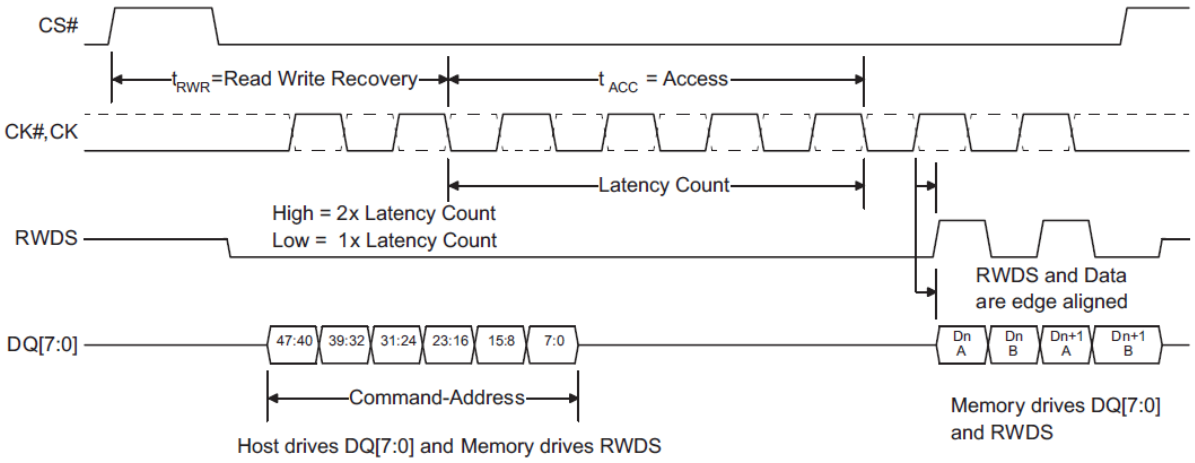

Fig. 35-2 HyperRAM Read Waveform

35.3.1.2 Write

This section describes the write operation of DSMC Core. The DSMC Core asserts CSn,

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CLKP/CLKN, and DQ. Then, it outputs 3 words command/address, and writes 1 or more data. For HyperRAM write operation, there is initial clock latency before writing data.

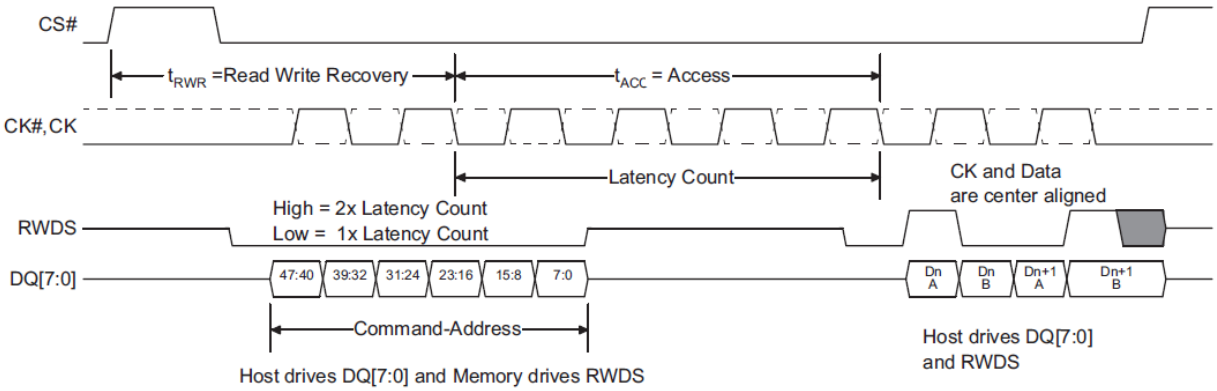

Fig. 35-3 HyperRAM Write Waveform

35.3.1.3 Byte Mask

This DSMC Memory Interface Controller outputs DQS signal as a byte mask during write operation. When byte access is requested from Main Controller, not write data is masked by DQS=HIGH. When target device is HyperFlash, byte masked data is written to device because of only supporting 16-bit access (byte masked data is fill in all 1 bit). In the HyperRAM Write Waveform, the D_n A and D_{n+1} B is invalid data which is masked.

35.3.2 TX/RX Controller

The TX/RX Controller performs operation control by state machine, and flow control of data between AXI bus and DSMC. In addition, when next access address is accepted by multiple outstanding address on AXI bus, it could be merged to the present transaction to improve the bandwidth if the address of subsequent access is continuous address to the present access.

35.3.3 C/A Encoder

DSMC memory device uses 6 bytes of command/address information to define the transactions characteristics. Table below shows the assignments of CA bit in DSMC Memory Interface Controller.

Table 35-1 C/A Format of DSMC for Hyper Device

C/A Bit	Name	Assignment
47	R/W#	0: Write, 1: Read
46	Target	CRT in DSMC_MCRn
45	Burst Type	0: WRAP, 1: INCR
44	RFU	0
43-16	Page Address	Address [31:4]
15	RFU	0
14-13	RFU	3
12-3	RFU	0
2-0	Column Address	Address [3:1]

note: The CA bit function of different devices slightly differs, and the exact meaning nead to be referred to the datasheet of the device.

35.3.4 FIFO

This section describes the FIFO for processing transaction request.

35.3.4.1 ADDR FIFO

ADR FIFO is a synchronizer module from AXI clock domain to DSMC clock domain. This FIFO has 46-bit width. This FIFO stores the control data which includes address, length, burst type and r/w flag. From these data, the control signals are generated for Main Controller.

35.3.4.2 W DAT FIFO

This FIFO is used to store the write data, valid information and strobe information written from the master in order to receive the command sequence of write buffer programming without a wait on AXI interface. The valid information indicates the 8-bit data is valid or not. The strobe information is used for strobe data from AXI interface to DSMC Core. When

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valid and strobe is 1, the 8-bit data is written data.

35.3.4.3 R DAT FIFO

This FIFO is used to store the data read from RX FIFO and the error detection information, and data stored is outputted according to timing of ACLK on AXI interface. This error information is transferred to HOST by RRESP signals.

35.3.5 LocalBus

35.3.5.1 Region division

The internal space of LocalBus device could be divided into different region, and they could be applied in suitable case. The size of regions is configure by DSMC_DEV_SIZE and DSMC_SLV_RGN_DIVn. The attribution of different region could be set to DPRA, REG or FIFO.

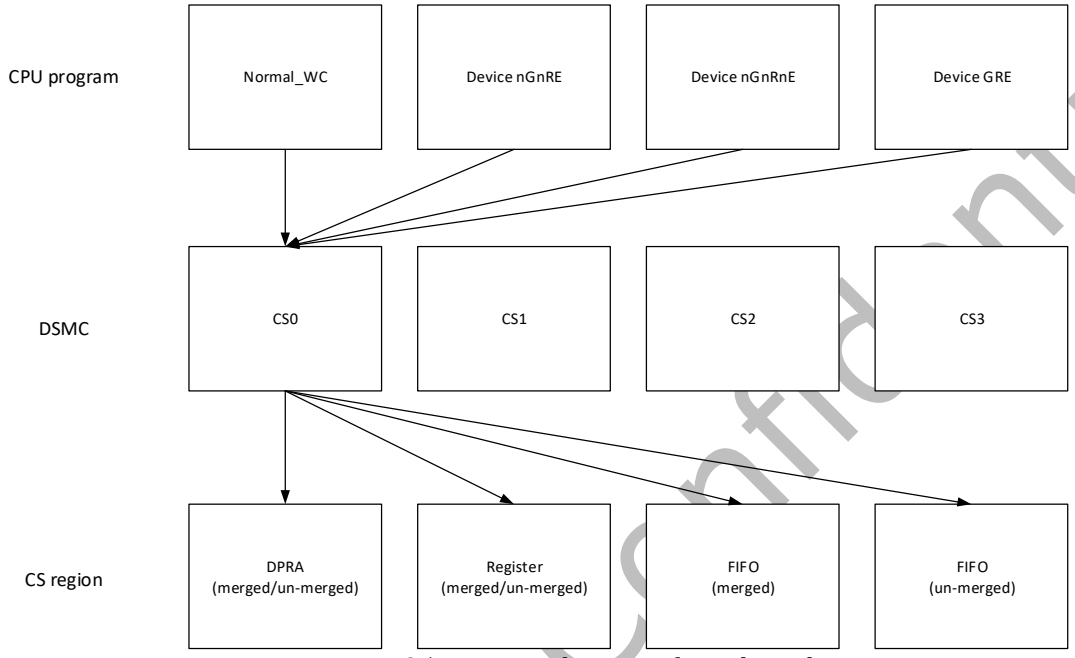

Fig. 35-4 Region division of LocalBus device

35.3.5.2 CA Encoder

Table 35-2 C/A Format of DSMC for LocalBus Device

C/A Bit	Name	Assignment
47	R/W#	0: Read, 1: Write
46	Target	CRT in DSMC_MCRn
45	Burst Type	0: WRAP, 1: INCR
44	Space Type	0: FIFO, 1: DPRA
43	FIFO Merge	0: No Merge, 1: Merge
42	RFU	0
41-40	Region	Region 0/1/2/3
39-32	Length	Burst length
31-0	Address	Address [31:0]

35.3.5.3 Back pressure

The back pressure mechanism is used to make full use of FIFO region space.

In the read transaction, when the FIFO is empty and could not provide data to the DSMC interface, the slave could enter the wait state, in which slave stop to send DQS clock, and latch the output DQ data. When the FIFO is recovered, the slave could continue sending the DQS and DQ, which could save bandwidth comparing to restart another burst.

In the write transaction, when the FIFO is full and could not receive data from the DSMC interface, the asynchronous signal DSMC_RDYN would be asserted. When the DSMC received, it would not send DQ and DSMC_CLK until the DSMC_RDYN is not asserted, which means there are enough space in the slave FIFO to accept data.

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35.4 Register Description

35.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

35.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DSMC_VER	0x0000	W	0x00000100	IP Version Register
DSMC_CSR	0x0008	W	0x00000000	Controller Status Register
DSMC_TAR	0x0010	W	0x00000000	Transaction Allocation Register
DSMC_AXICTL	0x0014	W	0x00000020	AXI Transaction Control Register
DSMC_CLK_MD	0x0020	W	0x00000000	Clock Mode Register
DSMC_DEV_SIZE	0x0030	W	0x00000017	Device Region Size Register
DSMC_INT_EN	0x0040	W	0x00000000	Interrupt Enable Register
DSMC_INT_STATUS	0x0044	W	0x00000000	Interrupt Status Register
DSMC_INT_MASK	0x0048	W	0x00000000	Interrupt Mask Register
DSMC_DMA_EN	0x0050	W	0x00000000	Interrupt Mask Register
DSMC_DMA_REQ_NUM0	0x0054	W	0x00000000	DMA Request Number Register 0
DSMC_DMA_REQ_NUM1	0x0058	W	0x00000000	DMA Request Number Register 1
DSMC_DMA_MUX	0x005C	W	0x00000010	Interrupt to DMA Request Multiplexer Register
DSMC_VDMC0	0x1000	W	0x00000226	Vendor Device Mode Control Register, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MCR0	0x1010	W	0x00000003	CS0# Memory Configuration Register, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MTR0	0x1014	W	0x00000022	CS0# Memory Base Address, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_WAIT_TIME0	0x1018	W	0x000007FF	CS0# Memory Base Address, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_BDRTCR0	0x1020	W	0x00000002	Boundary Transfer Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MRGTCR0	0x1024	W	0x00000000	Merge Transfer Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_WRAP2INCR0	0x1028	W	0x00000000	The function register of changing WRAP to INCR, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000

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Name	Offset	Size	Reset Value	Description
DSMC_RDS_DLL0_CTL0	0x1030	W	0x80000010	RDS Clock DLL Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RDS_DLL1_CTL0	0x1034	W	0x80000010	RDS Clock DLL Control Register 1, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_SLV_RGN_DIV0	0x1040	W	0x00000002	The division of slave region , and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN0_ATTR0	0x1050	W	0x00000000	The attribution of region 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN1_ATTR0	0x1054	W	0x00000000	The attribution of region 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN2_ATTR0	0x1058	W	0x00000000	The attribution of region 2, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN3_ATTR0	0x105C	W	0x00000000	The attribution of region 3, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

35.4.3 Detail Registers Description

DSMC_VER

Address: Operational Base(0xFF8B0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000100	version IP Version

DSMC_CSR

Address: Operational Base(0xFF8B0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	wrstoerr Write RSTO error. This bit indicates whether HyperBus memory is under reset state in the latest write operation. 1'b0: Normal operation 1'b1: HyperBus memory is under reset When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.

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Bit	Attr	Reset Value	Description
25	RO	0x0	wtrserr Write Transaction Error. This bit indicates whether AXI protocol is acceptable by HyperBus Memory Controller IP in the latest write transaction. 1'b0: Normal operation 1'b1: This protocol is not supported When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
24	RO	0x0	wdecerr Write Decode Error. This bit indicates whether access address is acceptable in the latest write transaction. 1'b0: Normal operation 1'b1: Access address is not reachable When this bit is set, HyperBus Memory Controller IP responds by AXI DECERR.
23:17	RO	0x00	reserved
16	RO	0x0	wact Write is Active. This bit indicates whether write transaction is in progress or not. 1'b0: Write is idle 1'b1: Write is active
15:12	RO	0x0	reserved
11	RO	0x0	rdsstall RDS Stall. This bit indicates whether read data transfer from HyperBus memory is stalled (RDS remains LOW) in the latest read transaction. 1'b0: Normal operation 1'b1: RDS is stalled When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
10	RO	0x0	rrstoerr Read RSTO error. This bit indicates whether HyperBus memory is under reset state in the latest read operation. 1'b0: Normal operation 1'b1: HyperBus memory is under reset When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
9	RO	0x0	rtrserr Read Transaction Error. This bit indicates whether AXI protocol is acceptable by HyperBus Memory Controller IP in the latest read transaction. 1'b0: Normal operation 1'b1: This protocol is not supported When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
8	RO	0x0	rdecerr Read Decode Error. This bit indicates whether access address is acceptable in the latest read transaction. 1'b0: Normal operation 1'b1: Access address is not reachable When this bit is set, HyperBus Memory Controller IP responds by AXI DECERR.
7:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	ract Read is Active. This bit indicates whether read transaction is in progress or not. 1'b0: Read is idle 1'b1: Read is active

DSMC_TAR

Address: Operational Base(0xFF8B0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	rta Read Transaction Allocation. 2'b00: 1 read transaction 2'b01: 2 read transactions 2'b10: 3 read transactions 2'b11: 4 read transactions
3:2	RO	0x0	reserved
1:0	RW	0x0	wta Write Transaction Allocation. 2'b00: 1 write transaction 2'b01: 2 write transactions 2'b10: 3 write transactions 2'b11: 4 write transactions

DSMC_AXICTL

Address: Operational Base(0xFF8B0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rd_no_err The axi read response will be tied 0 if this bit is enabled. 1'b0: disable 1'b1: enable
7:6	RO	0x0	reserved
5:4	RW	0x2	write_bvalid_ctl 2'b00: Generate the bvalid after the burst data TX end in IO 2'b01: Generate the bvalid after the TX state machine accept the request FIFO 2'b10: Generate the bvalid after burst write granted by arbiter 2'b11: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	nowait_write_data_done_en 1'b0: Disable 1'b1: Enable Only support "0" in current project

DSMC_CLK_MD

Address: Operational Base(0xFF8B0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	clk_mode This register is only configured in local bus application. 2'b00: Normal-toggle Mode, the ck only toggles when cs is asserted 2'b01: Always-on Mode, the ck is always on 2'b10: No-edge-clk Mode, the ck is always on except for the cs changing edge 2'b11: Reserved

DSMC_DEV_SIZE

Address: Operational Base(0xFF8B0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x17	dev_size Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 2G bytes In Memory-Mapped mode, the CS is controlled by AXI address bus, region size is used to generate CS.

DSMC_INT_EN

Address: Operational Base(0xFF8B0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	rdstall_int_en This bit is used to control the read stall time out interrupt enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en3 This bit is used to control the interrupt3. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
2	RW	0x0	int_en2 This bit is used to control the interrupt2. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
1	RW	0x0	int_en1 This bit is used to control the interrupt1. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
0	RW	0x0	int_en0 This bit is used to control the interrupt0. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable

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DSMC_INT_STATUS

Address: Operational Base(0xFF8B0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	W1C	0x0	rdstall_int_status Read stall time out interrupt status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.
3	W1C	0x0	int_status3 Interrupt 3 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.
2	W1C	0x0	int_status2 Interrupt 2 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.
1	W1C	0x0	int_status1 Interrupt 1 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.
0	W1C	0x0	int_status0 Interrupt 0 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. This register is only valid in local bus application.

DSMC_INT_MASK

Address: Operational Base(0xFF8B0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	rdstall_int_mask This register is used to mask the read stall interrupt. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
3	RW	0x0	int_mask3 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
2	RW	0x0	int_mask2 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
1	RW	0x0	int_mask1 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
0	RW	0x0	int_mask0 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked

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DSMC_DMA_EN

Address: Operational Base(0xFF8B0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dma_req_en1 This bit is used to control the DMA request from interrrupt1. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
0	RW	0x0	dma_req_en0 This bit is used to control the DMA request from interrrupt0. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable

DSMC_DMA_REQ_NUM0

Address: Operational Base(0xFF8B0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	dma_req_num0 This register is used to indicate the dma request number when DSMC accepts the interrupt0 from local bus slave. This register is only valid in local bus application.

DSMC_DMA_REQ_NUM1

Address: Operational Base(0xFF8B0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	dma_req_num1 This register is used to indicate the dma request number when DSMC accepts the interrupt1 from local bus slave. This register is only valid in local bus application.

DSMC_DMA_MUX

Address: Operational Base(0xFF8B0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x1	dma_req1_mux This bit fiele is used to select the interrupt to DMA request1. 2'b00: int0 2'b01: int1 2'h10: int2 2'b11: int3
3:2	RO	0x0	reserved
1:0	RW	0x0	dma_req0_mux This bit fiele is used to select the interrupt to DMA request0. 2'b00: int0 2'b01: int1 2'h10: int2 2'b11: int3

DSMC_VDMC0

Address: Operational Base(0xFF8B0000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x1	latency_fixed Only valid to APM pSRAM Read Memory. 1'b0: Variable 1'b1: Fixed
8	RW	0x0	reset_cmd_mode Generate reset Command to Device. Only valid in APM mid when CR register mode is set. If this bit is set, any write access in CR mode will initiate the FF command sequence.
7:4	RW	0x2	protocol Device Type 4'h0: Reserved 4'h1: OPI_Xccela (reserved) 4'h2: HyperBus (reserved) 4'h3: Local Bus Others: Reserved
3:0	RW	0x6	mid MID 4'h1: Infineon/Cypress 4'h3: ISSI 4'h6: Winbond 4'hd: APM Others: Reserved

DSMC_MCR0

Address: Operational Base(0xFF8B0000) + offset (0x1010)

Bit	Attr	Reset Value	Description
31	RW	0x0	maxen Maximum length Enable 1'b0: No configurable CS# low time 1'b1: Configurable CS# low time When this bit 1, CS# low time can be configurable by MAXLEN bit.
30:27	RO	0x0	reserved
26:18	RW	0x000	maxlen Maximum Length This bit indicates maximum read/write transaction length to memory. This bit is ignored when MAXEN bit is 0. 9'h000: 2 Byte (1 HyperBus CK) 9'h001: 4 Byte (2 HyperBus CK) 9'h002: 6 Byte (3 HyperBus CK) ..... 9'h1ff: 1024 Byte (512 HyperBus CK)
17	RW	0x0	tcmo True Continuous Merge Option. 1'b0: No merging WRAP and INCR 1'b1: Merging WRAP and INCR Note that this function can be used with the HyperBus memory with specific function. Please confirm whether it is corresponding HyperBus memory before enabling this function. If set to 1, it means the controller can merge the Wrap and INCR operation.

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Bit	Attr	Reset Value	Description
16	RW	0x0	acs Asymmetry Cache Support. 1'b0: No asymmetry cache system support. 1'b1: Asymmetry cache system support. This function should be disabled if the HyperBus memory itself supports the asymmetry cache system. If this bit set to 1, then the HyperBus memory interface controller accepts the wrap read transaction, and compares the required wrap size with the wrap size of HyperBus memory in register; When the wrap size is the same, HyperBus memory interface controller requires the wrap burst read to HyperBus memory; When the wrap size differs, HyperBus memory interface controller emulates wrap burst read by requesting two continuous burst read to HyperBus memory.
15:6	RO	0x000	reserved
5	RW	0x0	crt Configuration Register Target. 1'b0: Memory space 1'b1: CR space This bit indicates whether the read or write operation accesses the memory or CR space. This bit is mapped to CA[46] bit in HyperRAM. When using HyperFlash, this bit should be set to 0.
4	RW	0x0	devtype Device Type. 1'b0: HyperFlash 1'b1: HyperRAM Device type for control target. Only support "1" in current project
3	RW	0x0	iowidth IO Width. 1'b0: x8 interface 1'b1: x16 interface Note that "1'b1: x16 interface" can be set when DEVTYPE is set to "1'b1: HyperRAM"
2	RW	0x0	exclusive_dqs This bit field indicates the number of valid dqs bit when iowidth is 16 bits, and it is only valid in local bus application. 1'b0: 2 bits 1'b1: 1 bit
1:0	RW	0x3	wrapsize Wrap Size. 2'b00: Reserved 2'b01: 32(Clocks), 64 bytes for x8 and 128 bytes for x16 2'b10: 8(Clocks), 16 bytes for x8 and 32 bytes for x16 2'b11: 16(Clocks), 32 bytes for x8 and 64 bytes for x16 The wrap burst length of HyperBus memory. This bit is ignored when the asymmetry cache support bit is 0. When the asymmetry cache support is 1, this bit should be set the same as wrap size of configuration register in HyperBus memory.

DSMC_MTR0

Address: Operational Base(0xFF8B0000) + offset (0x1014)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	rcshi Read Chip Select High Between Operations. This bit indicates CS# high time for read between operations. 0x0 corresponds to 1.5 clock cycle, 0xF corresponds to 16.5 clock cycle.
27:24	RW	0x0	wcshi Write Chip Select High Between Operations. This bit indicates CS# high time for write between operations. 0x0 corresponds to 1.5 clock cycle, 0xF corresponds to 16.5 clock cycle.
23:20	RW	0x0	rcss Read Chip Select Setup to next CK rising edge. This bit indicates CS# setup time for read from CS# assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle.
19:16	RW	0x0	wcss Write Chip Select Setup to next CK rising edge. This bit indicates CS# setup time for write from CS# assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle.
15:12	RW	0x0	rcsh Read Chip Select Hold after CK falling edge. This bit indicates CS# hold time for read to CS# de-assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle.
11:8	RW	0x0	wcsh Write Chip Select Hold after CK falling edge. This bit indicates CS# hold time for write to CS# de-assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycle.
7:4	RW	0x2	rltcy Read Latency Cycle. Only uses in HyperRAM. This bit indicates initial latency code for write access. This bit is ignored when MCRX.DEVTYPE is 0 (HyperFlash). 4'h0: 5 clock latency 4'h1: 6 clock latency 4'h2: 7 clock latency 4'h3: 8 clock latency 4'h4: 9 clock latency 4'h5: 10 clock latency 4'hb: 0 clock latency 4'hc: 1 clock latency 4'hd: 2 clock latency 4'he: 3 clock latency 4'hf: 4 clock latency Others: Reserved
3:0	RW	0x2	wltcy Write Latency Cycle. Only uses in HyperRAM. This bit indicates initial latency code for write access. This bit is ignored when MCRX.DEVTYPE is 0 (HyperFlash). 4'h0: 5 clock latency 4'h1: 6 clock latency 4'h2: 7 clock latency 4'h3: 8 clock latency 4'h4: 9 clock latency 4'h5: 10 clock latency

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Bit	Attr	Reset Value	Description
			4'hb: 0 clock latency 4'hc: 1 clock latency 4'hd: 2 clock latency 4'he: 3 clock latency 4'hf: 4 clock latency Others: Reserved

DSMC_WAIT_TIME0

Address: Operational Base(0xFF8B0000) + offset (0x1018)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x7ff	rdstall_wait_time This bit filed is used to configure the max wait time of the read stall status.

DSMC_BDRTCR0

Address: Operational Base(0xFF8B0000) + offset (0x1020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	rd_bdr_xfer_en Enable Cross Row Address Data Read Transfer. 1'b0: Disable 1'b1: Enable
4	RW	0x0	wr_bdr_xfer_en Enable Cross Row Address Data Write Transfer. 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2:0	RW	0x2	col_bit_num The valid column address bit, also the cycle numbers in the port. 3'h0: 6bit 3'h1: 7bit 3'h2: 8bit 3'h3: 9bit 3'h4: 10bit 3'h5: 11bit Others: Reserved

DSMC_MRGTCR0

Address: Operational Base(0xFF8B0000) + offset (0x1024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_merge_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	write_merge_en 1'b0: Disable 1'b1: Enable

DSMC_WRAP2INCR0

Address: Operational Base(0xFF8B0000) + offset (0x1028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	wrap2incr_en This bit is used to enable the function of changing WRAP transfer to INCR transfer. This register is only configured in local bus application. 1'b0: Disable 1'b1: Enable

DSMC_RDS_DLL0_CTL0

Address: Operational Base(0xFF8B0000) + offset (0x1030)

Bit	Attr	Reset Value	Description
31	RW	0x1	rds_0_clk_smp_sel DQ[7:0] Sampling Clock Selection 1'b0: Without DLL 1'b1: With DLL
30:8	RO	0x000000	reserved
7:0	RW	0x10	rds_0_clk_delay_num RDS Clock 0 Delay Line Cell Number

DSMC_RDS_DLL1_CTL0

Address: Operational Base(0xFF8B0000) + offset (0x1034)

Bit	Attr	Reset Value	Description
31	RW	0x1	rds_1_clk_smp_sel DQ[7:0] Sampling Clock Selection 1'b0: Without DLL 1'b1: With DLL
30:8	RO	0x000000	reserved
7:0	RW	0x10	rds_1_clk_delay_num RDS Clock 0 Delay Line Cell Number

DSMC_SLV_RGN_DIV0

Address: Operational Base(0xFF8B0000) + offset (0x1040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x2	slv_rgn_div This register is only valid in local bus application. This bit filed indicate the region division of the slave memory. 2'b00: 1 2'b01: 2 2'b10: 4 Others: Reserved

DSMC_RGN0_ATTR0

Address: Operational Base(0xFF8B0000) + offset (0x1050)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn0_addr_width This bit is used to indicate the address width of the CA phase when access region 0. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn0_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only whe write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles

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Bit	Attr	Reset Value	Description
6	RW	0x0	rgn0_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region0. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn0_be_ctrled The cs0 accessing region0 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn0_ctrl The cs0 accessing region0 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn0_attr This register is only valid in local bus application. The attribution of the region0 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN1_ATTR0

Address: Operational Base(0xFF8B0000) + offset (0x1054)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn1_addr_width This bit is used to indicate the address width of the CA phase when access region 1. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn1_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only whe write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rgn1_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region1. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn1_be_ctrled The cs0 accessing region1 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn1_ctrl The cs0 accessing region1 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	rgn1_attr This register is only valid in local bus application. The attribution of the region1 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN2_ATTR0

Address: Operational Base(0xFF8B0000) + offset (0x1058)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn2_addr_width This bit is used to indicate the address width of the CA phase when access region 2. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn2_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only when write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rgn2_wr_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region2. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn2_be_ctrled The cs0 accessing region2 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn2_ctrl The cs0 accessing region2 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn2_attr This register is only valid in local bus application. The attribution of the region1 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN3_ATTR0

Address: Operational Base(0xFF8B0000) + offset (0x105C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn3_addr_width This bit is used to indicate the address width of the CA phase when access region 3. 1'b0: 32 bits 1'b1: 16 bits

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Bit	Attr	Reset Value	Description
7	RW	0x0	rgn3_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only when write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rng3_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn3_be_ctrled The cs0 accessing region3 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn3_ctrl The cs0 accessing region3 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn3_attr This register is only valid in local bus application. The attribution of the region3 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

35.5 Interface Description

Table 35-3 DSMC interface description

Module Pin	Direction	Pin Name	IOMUX Setting
CLKP	O	GPIO1_A0	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[3:0]=4'h2
CLKN	O	GPIO1_A1	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[7:4]=4'h2
CS0	O	GPIO1_B6	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[11:8]=4'h2
CS1	O	GPIO1_B1	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[7:4]=4'h2
CS2	O	GPIO1_D2	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[11:8]=4'h2
CS3	O	GPIO1_D3	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[15:12]=4'h2
RESETN	O	GPIO1_C0	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[3:0]=4'h2
DQS0	I/O	GPIO1_A2	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[11:8]=4'h2
DQS1	I/O	GPIO1_D1	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[7:4]=4'h2
DQ0	I/O	GPIO1_A3	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[15:12]=4'h2
DQ1	I/O	GPIO1_A4	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[3:0]=4'h2
DQ2	I/O	GPIO1_A5	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[7:4]=4'h2
DQ3	I/O	GPIO1_A6	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[11:8]=4'h2
DQ4	I/O	GPIO1_A7	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[15:12]=4'h2
DQ5	I/O	GPIO1_B0	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[3:0]=4'h2
DQ6	I/O	GPIO1_B4	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[3:0]=4'h2
DQ7	I/O	GPIO1_B5	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[7:4]=4'h2
DQ8	I/O	GPIO1_C1	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[7:4]=4'h2
DQ9	I/O	GPIO1_C2	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[11:8]=4'h2
DQ10	I/O	GPIO1_C3	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[15:12]=4'h2
DQ11	I/O	GPIO1_C4	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[3:0]=4'h2

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Module Pin	Direction	Pin Name	IOMUX Setting
DQ12	I/O	GPIO1_C5	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[7:4]=4'h2
DQ13	I/O	GPIO1_C6	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[11:8]=4'h2
DQ14	I/O	GPIO1_C7	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[15:12]=4'h2
DQ15	I/O	GPIO1_D0	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[3:0]=4'h2
INT0	I	GPIO1_A1	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[7:4]=4'h4
INT1	I	GPIO1_C0	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[3:0]=4'h4
INT2	I	GPIO1_B2	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[11:8]=4'h2
INT3	I	GPIO1_B3	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[15:12]=4'h2
RDYN	I	GPIO1_B7	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[15:12]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional.

35.6 Application Notes

35.6.1 Typical Program Flow for Hyper Device

1. Configure the DSMC_DEV_SIZE according to the size of device applied.
2. Configure the DSMC_MRGTCRx to support merge operation, and the DSMC_BDRTCRx to support crossing the boundary.
3. Configure the DSMC_MTRx to adjust the transfer timing.
4. Configure DSMC_MCRx to access the slave configure register.
5. Set the slave configuration to be consistent with the host, such as write and read latency.
6. Configure DSMC_MCRx to access the slave memory space.

35.6.2 Typical Program Flow for LocalBus Device

1. Configure the DSMC_DEV_SIZE according to the size of device applied.
2. Configure the DSMC_MRGTCRx to support merge operation, and the DSMC_BDRTCRx to support crossing the boundary.
3. Configure the DSMC_MTRx to adjust the transfer timing.
4. Configure the DSMC_VDMCx to LocalBus.
5. Enable the DSMC_WRAP2INCRx function if the slave required.
6. Configure DSMC_MCRx to access the slave configure register.
7. Keep the configuration parameter of the slave is the same as the master.
8. Configure DSMC_MCRx to access the slave memory space.

35.6.3 Chip Select selection

This section describes how to select Chip Select. This controller can’t assert two Chip Select at the same time except for the LocalBus write.

When the device size is configured, the 2 address bits higher than device size are used as chip select signals.

35.6.4 Configurable CS# Low Time

This section describes configurable CS# low time. HyperRAM has a regulation for CS# low time (t_{CSM}). To meet CS# low time, a read/write transaction can be regulated by setting MCRx.MAXLEN bit. By MCRx.MAXLEN bit, one transaction is split multi transactions.

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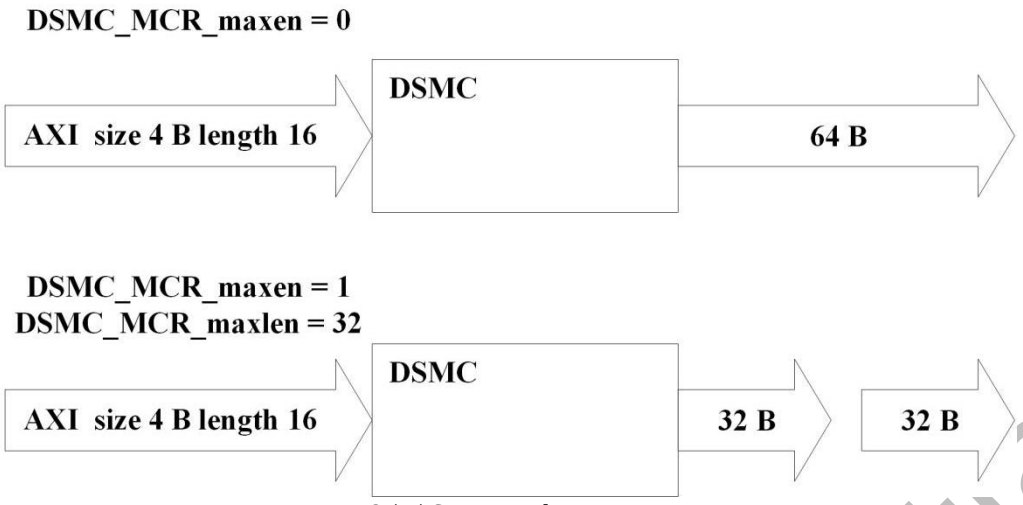

Fig. 35-5 Separated Transaction

35.6.5 Data Map

The data mapping relationship between memory and DSMC interface is shown as below.

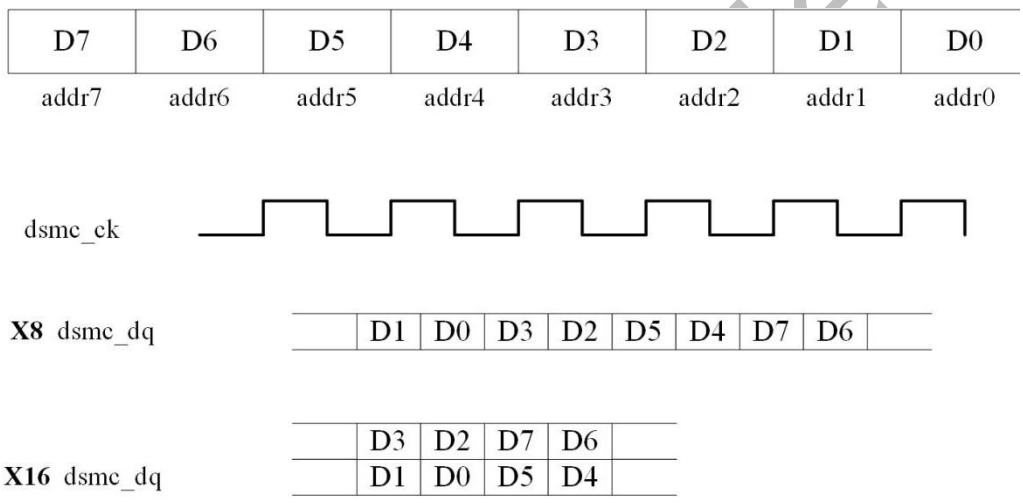

Fig. 35-6 Data mapping relationship between memory and DSMC interface

35.6.6 Merge Operation

The merge operation function supports Hyper device and LocalBus device, and it is configured by the DSMC_MRGTCRx register.

- Merge operation removes address output period and latency cycles for subsequent transaction.
- When DSMC Memory Controller IP accepts subsequent read transaction with continuous address, it is merged to one CS# period on DSMC memory interface.

35.6.7 Timing Adjustment

This section describes the DSMC timing adjustment. DSMC core has timing adjustment circuit and timing adjustment is controlled by DSMC_MTRn. RCSHI, RCSS, and RCSH in DSMC_MTRn are used for the read timing adjustment, and WCSHI, WCSS, and WCSH in DSMC_MTRn are used for the write timing adjustment.

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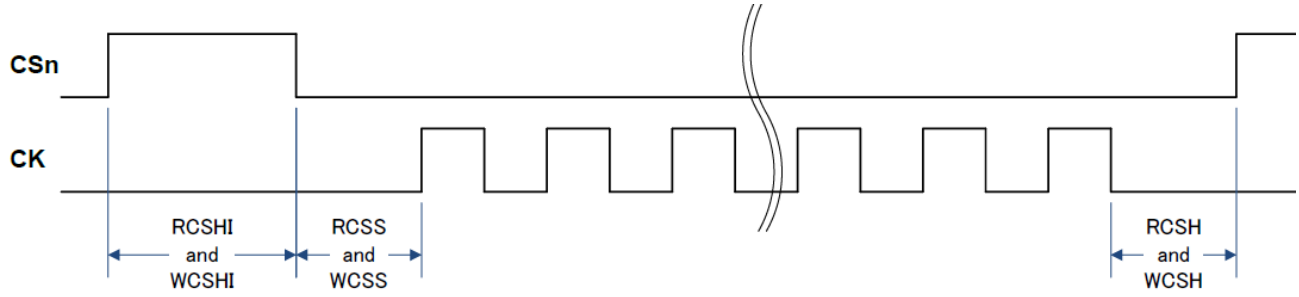

Fig. 35-7 Timing Adjustment

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Chapter 36 Slave Double Date Rate Serial Memory Controller (SLAVE DSMC)

36.1 Overview

The Slave DSMC is the slave controller of Rockchip LocalBus, and it works in combination with DSMC. There are two regions of register and FIFO in the SLAVE DSMC to achieve low latency and high bandwidth.

The main feature is shown below

- Support the double data rate interface
- Support 8-wire serial transfer mode
- Support 2 interrupts of host2slave and slave2host
- Support 2 region attributions of register and FIFO
- Support wait state in FIFO read mode
- Support back pressure in FIFO write mode
- Support configurable serial address width: 16 bits or 32 bits in different region
- Support configurable internal bus accessing address

36.2 Block Diagram

SLAVE DSMC is comprised of:

- AHB Interface

The APB Interface implements the AHB slave operation. Its data bus width is 32 bits.

- AXI Interface

The AXI Interface is a XIP interface to access internal device. Its data bus width is 64 bits.

- LocalBus Control Interface

The interface to transmit data with MASTER DSMC.

- Bus Control

The core module to access internal memory in FIFO region.

- Common Register Bank

The DSMC transfer configuration register bank.

- Application & Control Status Register Bank

The SLAVE DSMC control and status register banks, and they are shadow registers.

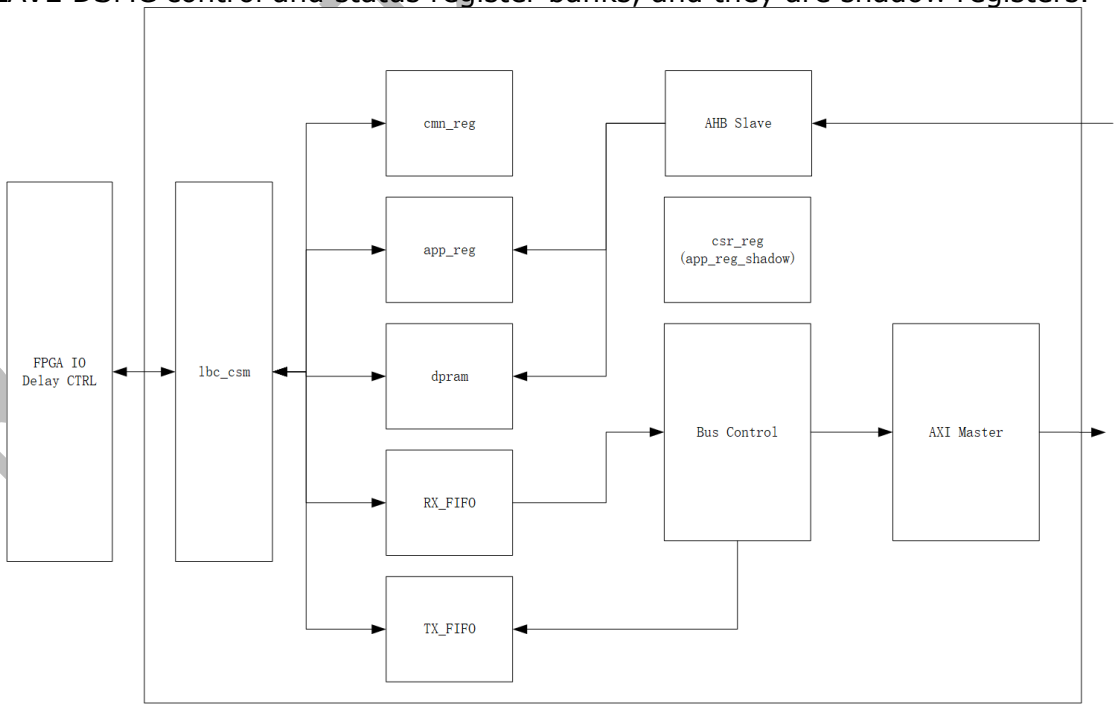

Fig. 36-1 SLAVE DSMC Block Diagram

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36.3 Function Description

The SLAVE DSMC is responsible for transmitting data from the Local Bus to the Register Memory and resolving read/write transmission from the LocalBus to the internal memory space of the slave chip.

The MASTER accesses the CMN_REG and LBC_REG of the LBC_SLAVE through the LocalBus interface, and the slave accesses the APP_REG of the LBC_SLAVE through the AHB interface. The LBC_REG and APP_REG are shadow of each other and can be read but not configured in each other's clock domain.

For data read and write access on the host, the LBC_SLAVE converts the LocalBus transmission to the data transfer of the AXI interface pair on the slave internal memory.

Before the SLAVE DSMC access, the bus must be switch from the flexible bus to the SLAVE DSMC.

36.3.1 DSMC Interface

This section describes physical interface of the SLAVE DSMC module.

36.3.1.1 Read

DSMC asserts cs, dsmc_clk, and dsmc_dq. Then, the SLAVE DSMC receives 3 words command/address, and outputs data by the timing of dqs_clk. The read data is edge aligned with dqs_clk and the read latency is configurable.

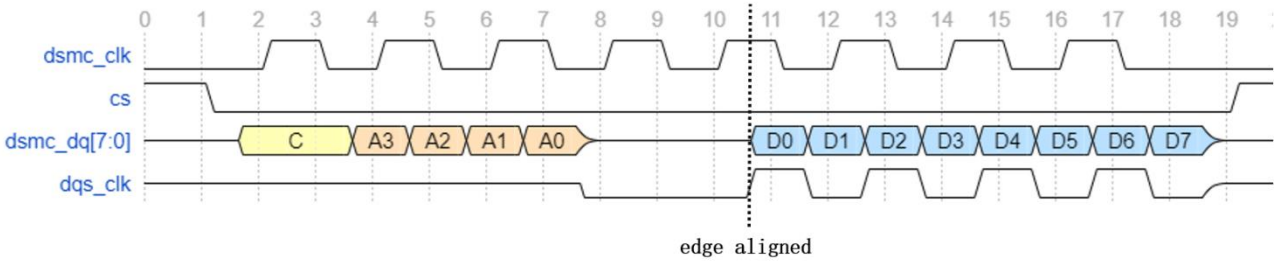

Fig. 36-2 LocalBus Read Waveform

36.3.1.2 Write

This section describes the write operation of LocalBus. The DSMC asserts cs, dsmc_clk, and dsmc_dq. Then, the Slave DSMC receives 3 words command/address, and then the data information. The write data is center aligned with dsmc_clk and the data latency is configurable.

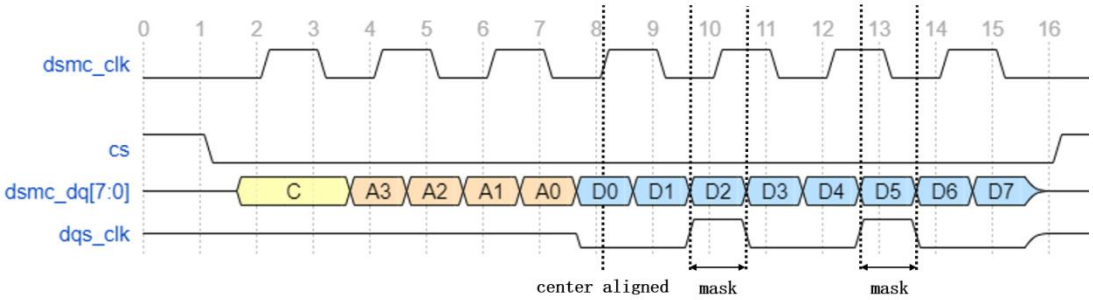

Fig. 36-3 LocalBus Write Waveform

36.3.1.3 Byte Mask

This SLAVE DSMC could also support byte write access as same as the MASTER

36.3.1.4 C/A Encoder

The C/A Encoder could be referred in the corresponding part of the MASTER DSMC.

36.3.2 FIFO Access

The FIFO region could be empty or full due to the bandwidth difference, and the wait state and back pressure is introduced to improve bandwidth.

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36.3.2.1 Read Wait State

In the read transaction, when the FIFO is empty and could not provide data to the DSMC interface, the slave could enter the wait state, in which slave stop to send DQS clock, and latch the output DQ data. When the FIFO is recovered, the slave could continue sending the DQS and DQ, which could save bandwidth comparing to restart another burst.

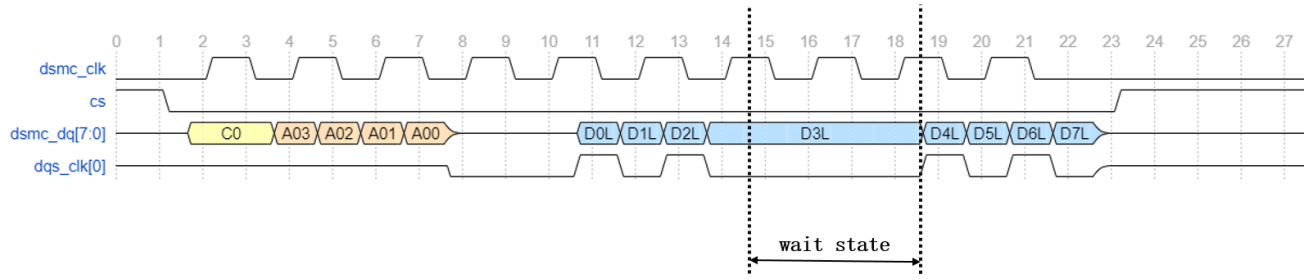

Fig. 36-4 LocalBus Read Waveform

36.3.2.2 Write Back Pressure

In the write transaction, when the FIFO is full and could not receive data from the DSMC interface, the asynchronous signal DSMC_RDYN would be asserted. When the DSMC received, it would not send DQ and DSMC_CLK until the DSMC_RDYN is not asserted, which means there are enough space in the slave FIFO to accept data.

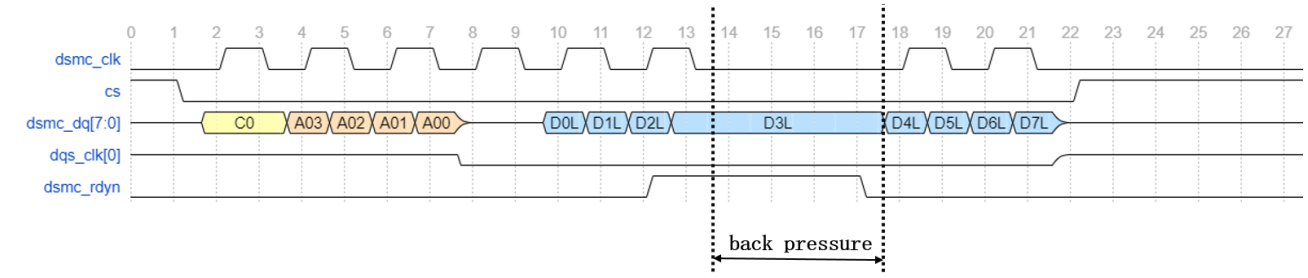

Fig. 36-5 LocalBus Read Waveform

36.4 Register Description

36.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

36.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SLAVE_DSMC_APP_CON0	0x0000	W	0x00000000	Application Control Register 0
SLAVE_DSMC_APP_CON1	0x0004	W	0x00000000	Application Control Register 1
SLAVE_DSMC_APP_CON2	0x0008	W	0x00000000	Application Control Register 2
SLAVE_DSMC_APP_CON3	0x000C	W	0x00000000	Application Control Register 3
SLAVE_DSMC_APP_CON4	0x0010	W	0x00000000	Application Control Register 4
SLAVE_DSMC_APP_CON5	0x0014	W	0x00000000	Application Control Register 5
SLAVE_DSMC_APP_CON6	0x0018	W	0x00000000	Application Control Register 6
SLAVE_DSMC_APP_CON7	0x001C	W	0x00000000	Application Control Register 7
SLAVE_DSMC_APP_CON8	0x0020	W	0x00000000	Application Control Register 8
SLAVE_DSMC_APP_CON9	0x0024	W	0x00000000	Application Control Register 9
SLAVE_DSMC_APP_CON10	0x0028	W	0x00000000	Application Control Register 10
SLAVE_DSMC_APP_CON11	0x002C	W	0x00000000	Application Control Register 11
SLAVE_DSMC_APP_CON12	0x0030	W	0x00000000	Application Control Register 12

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Name	Offset	Size	Reset Value	Description
SLAVE_DSMC_APP_CON13	0x0034	W	0x00000000	Application Control Register 13
SLAVE_DSMC_APP_CON14	0x0038	W	0x00000000	Application Control Register 14
SLAVE_DSMC_APP_CON15	0x003C	W	0x00000000	Application Control Register 15
SLAVE_DSMC_APP_H2S_INT_STA	0x0080	W	0x00000000	Application Host to Slave Interrupt Status
SLAVE_DSMC_APP_H2S_INT_STA_EN	0x0084	W	0x00000000	Application Host to Slave Interrupt Status Enable
SLAVE_DSMC_APP_H2S_INT_STA_SIG_EN	0x0088	W	0x00000000	Application Host to Slave Interrupt Status Signal Enable
SLAVE_DSMC_LBC_CON0	0x0100	W	0x00000000	Local Bus Control Register 0
SLAVE_DSMC_LBC_CON1	0x0104	W	0x00000000	Local Bus Control Register 1
SLAVE_DSMC_LBC_CON2	0x0108	W	0x00000000	Local Bus Control Register 2
SLAVE_DSMC_LBC_CON3	0x010C	W	0x00000000	Local Bus Control Register 3
SLAVE_DSMC_LBC_CON4	0x0110	W	0x00000000	Local Bus Control Register 0
SLAVE_DSMC_LBC_CON5	0x0114	W	0x00000000	Local Bus Control Register 1
SLAVE_DSMC_LBC_CON6	0x0118	W	0x00000000	Local Bus Control Register 2
SLAVE_DSMC_LBC_CON7	0x011C	W	0x00000000	Local Bus Control Register 3
SLAVE_DSMC_LBC_CON8	0x0120	W	0x00000000	Local Bus Control Register 8
SLAVE_DSMC_LBC_CON9	0x0124	W	0x00000000	Local Bus Control Register 9
SLAVE_DSMC_LBC_CON10	0x0128	W	0x00000000	Local Bus Control Register 10
SLAVE_DSMC_LBC_CON11	0x012C	W	0x00000000	Local Bus Control Register 11
SLAVE_DSMC_LBC_CON12	0x0130	W	0x00000000	Local Bus Control Register 12
SLAVE_DSMC_LBC_CON13	0x0134	W	0x00000000	Local Bus Control Register 13
SLAVE_DSMC_LBC_CON14	0x0138	W	0x00000000	Local Bus Control Register 14
SLAVE_DSMC_LBC_CON15	0x013C	W	0x00000000	Local Bus Control Register 15
SLAVE_DSMC_LBC_S2H_INT_STA	0x0180	W	0x00000000	Local Bus Controller Slave to Host Interrupt Status
SLAVE_DSMC_LBC_S2H_INT_STA_EN	0x0184	W	0x00000000	Local Bus Controller Slave to Host Interrupt Status Enable
SLAVE_DSMC_LBC_S2H_INT_STA_SIG_EN	0x0188	W	0x00000000	Local Bus Controller Slave to Host Interrupt Status Signal Enable
SLAVE_DSMC_AXI_WR_ADDR_BASE	0x0800	W	0x00000000	AXI Write Base Address
SLAVE_DSMC_AXI_RD_ADDR_BASE	0x0804	W	0x00000000	AXI Read Base Address
SLAVE_DSMC_DBG_STA_0	0x0900	W	0x00000000	Debug Status 0
SLAVE_DSMC_DBG_STA_1	0x0904	W	0x00000000	Debug Status 1
SLAVE_DSMC_DBG_STA_2	0x0908	W	0x00000000	Debug Status 2
SLAVE_DSMC_VER	0x0A00	W	0x00000100	The version code

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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36.4.3 Detail Registers Description

SLAVE_DSMC_APP_CON0

Address: Operational Base(0xFF880000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con0 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[0]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON1

Address: Operational Base(0xFF880000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con1 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[1]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON2

Address: Operational Base(0xFF880000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con2 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[2]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON3

Address: Operational Base(0xFF880000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con3 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[3]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON4

Address: Operational Base(0xFF880000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con4 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[4]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON5

Address: Operational Base(0xFF880000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con5 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[5]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON6

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Address: Operational Base(0xFF880000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con6 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[6]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON7

Address: Operational Base(0xFF880000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con7 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[7]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON8

Address: Operational Base(0xFF880000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con8 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[8]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON9

Address: Operational Base(0xFF880000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con9 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[9]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON10

Address: Operational Base(0xFF880000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con10 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[10]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON11

Address: Operational Base(0xFF880000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con11 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[11]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON12

Address: Operational Base(0xFF880000) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con12 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[12]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON13

Address: Operational Base(0xFF880000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con13 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[13]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON14

Address: Operational Base(0xFF880000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con14 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[14]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_CON15

Address: Operational Base(0xFF880000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_con15 Write access will trigger interrupt from slave to host, the interrupt status is lbc_s2h_int_sta[15]. The corresponding shadow register could be read through DSMC interface.

SLAVE_DSMC_APP_H2S_INT_STA

Address: Operational Base(0xFF880000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	app_h2s_int_sta The interrupt status from host to slave. The interrupt is originating from the writing of LBC_CON.

SLAVE_DSMC_APP_H2S_INT_STA_EN

Address: Operational Base(0xFF880000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	app_h2s_int_sta_en The interrupt enable registers of 16 h2s interrupt status. 1'b0: disable 1'b1: enable

SLAVE_DSMC_APP_H2S_INT_STA_SIG_EN

Address: Operational Base(0xFF880000) + offset (0x0088)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	app_h2s_int_sta_sig_en The interrupt signal out registers of 16 h2s interrupt status. 1'b0: disable 1'b1: enable

SLAVE_DSMC_LBC_CON0

Address: Operational Base(0xFF880000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con0 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[0]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON1

Address: Operational Base(0xFF880000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con1 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[1]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON2

Address: Operational Base(0xFF880000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con2 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[2]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON3

Address: Operational Base(0xFF880000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con3 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[3]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON4

Address: Operational Base(0xFF880000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con4 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[4]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON5

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Address: Operational Base(0xFF880000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con5 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[5]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON6

Address: Operational Base(0xFF880000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con6 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[6]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON7

Address: Operational Base(0xFF880000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con7 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[7]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON8

Address: Operational Base(0xFF880000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con8 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[8]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON9

Address: Operational Base(0xFF880000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con9 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[9]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON10

Address: Operational Base(0xFF880000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con10 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[10]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON11

Address: Operational Base(0xFF880000) + offset (0x012C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con11 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[11]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON12

Address: Operational Base(0xFF880000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con12 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[12]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON13

Address: Operational Base(0xFF880000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con13 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[13]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON14

Address: Operational Base(0xFF880000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con14 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[14]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_CON15

Address: Operational Base(0xFF880000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lbc_con15 Write access from DSMC will trigger interrupt from host to slave, the interrupt status is app_h2s_int_sta[15]. The corresponding shadow register could be read through Slave AHB interface.

SLAVE_DSMC_LBC_S2H_INT_STA

Address: Operational Base(0xFF880000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	lbc_s2h_int_sta The interrupt status from slave to host. The interrupt is originating from the writing of APP_CON.

SLAVE_DSMC_LBC_S2H_INT_STA_EN

Address: Operational Base(0xFF880000) + offset (0x0184)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RO	0x0000	lbc_s2h_int_sta_en The interrupt enable registers of 16 s2h interrupt status. 1'b0: disable 1'b1: enable

SLAVE_DSMC_LBC_S2H_INT_STA_SIG_EN

Address: Operational Base(0xFF880000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RO	0x0000	lbc_s2h_int_sta_sig_en The interrupt signal out registers of 16 s2h interrupt status. 1'b0: disable 1'b1: enable

SLAVE_DSMC_AXI_WR_ADDR_BASE

Address: Operational Base(0xFF880000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	axi_wr_addr_base The access base address of write transaction in AXI interface.

SLAVE_DSMC_AXI_RD_ADDR_BASE

Address: Operational Base(0xFF880000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	axi_rd_addr_base The access base address of read transaction in AXI interface.

SLAVE_DSMC_DBG_STA_0

Address: Operational Base(0xFF880000) + offset (0x0900)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RO	0x0	axi_wr_resp_error AXI write transaction response error.
1:0	RO	0x0	axi_rd_resp_error AXI read transaction response error.

SLAVE_DSMC_DBG_STA_1

Address: Operational Base(0xFF880000) + offset (0x0904)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	bus_current_state The state machine of slave.

SLAVE_DSMC_DBG_STA_2

Address: Operational Base(0xFF880000) + offset (0x0908)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	tx_dat_fifo_space2empty The remained FIFO space of TX data FIFO.

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:8	RO	0x00	rx_dat_fifo_space2empty The remained FIFO space of RX data FIFO.
7:5	RO	0x0	reserved
4:0	RO	0x00	rx_cmd_fifo_space2empty The remained FIFO space of RX command FIFO.

SLAVE_DSMC_VER

Address: Operational Base(0xFF880000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000100	version_code The version code of the DSMC slave.

36.5 Common Register Description

36.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

36.5.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SLAVE_DSMC_CMN_CMN_CON0	0x0000	W	0x00000211	Common Configuration0
SLAVE_DSMC_CMN_CMN_CON1	0x0004	W	0x00001818	Common Configuration0
SLAVE_DSMC_CMN_CMN_CON2	0x0008	W	0x01010F0F	Common Configuration0
SLAVE_DSMC_CMN_CMN_CON3	0x000C	W	0x00000010	Common Configuration0
SLAVE_DSMC_CMN_RGN0_CMN_CON0	0x0100	W	0x00000221	Region0 Common Configuration0
SLAVE_DSMC_CMN_RGN1_CMN_CON0	0x0200	W	0x00000221	Region1 Common Configuration0
SLAVE_DSMC_CMN_RGN2_CMN_CON0	0x0300	W	0x00000221	Region2 Common Configuration0
SLAVE_DSMC_CMN_RGN3_CMN_CON0	0x0400	W	0x00000221	Region3 Common Configuration0
SLAVE_DSMC_CMN_DBG_STATUS_0	0x0900	W	0x00000000	Debug Status Register0
SLAVE_DSMC_CMN_DBG_STATUS_1	0x0904	W	0x00000000	Debug Status Register1
SLAVE_DSMC_CMN_DBG_STATUS_2	0x0908	W	0x00000000	Debug Status Register2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

36.5.3 Detail Registers Description

SLAVE_DSMC_CMN_CMN_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	wr_data_cyc_extended DSMC will output extended dummy clock cycle in write transaction when accessing CMN register. 1'b0: Normal write cycle mode 1'b1: Extend write cycle mode

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Bit	Attr	Reset Value	Description
10:8	RW	0x2	rd_latency_cyc Read latency cycle when accessing CMN register. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
7	RO	0x0	reserved
6:4	RW	0x1	wr_latency_cyc Write latency cycle when accessing CMN register. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x1	ca_cyc This bit is used to indicate the address width of the CA phase when accessing CMN register. 1'b0: 16bit address 1'b1: 32bit address

SLAVE_DSMC_CMN_CMN_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	tx_almost_empty_watermark Data TX FIFO almost full watermark. When the space of TX FIFO is less than this watermark, the almost_empty of RX FIFO will be asserted.
23:21	RO	0x0	reserved
20:16	RW	0x00	tx_almost_full_watermark Data TX FIFO almost full watermark. When the space of TX FIFO is less than this watermark, the almost_full of RX FIFO will be asserted. If the TX FIFO is almost full, slave will stop to send read transaction from AXI interface.
15:14	RO	0x0	reserved
13:8	RW	0x18	rx_almost_empty_watermark Data RX FIFO almost full watermark. When the space of RX FIFO is less than this watermark, the almost_empty of RX FIFO will be asserted.
7:6	RO	0x0	reserved
5:0	RW	0x18	rx_almost_full_watermark Data RX FIFO almost full watermark. When the RX FIFO is almost full, the DSMC master could not continue writing data in slave.

SLAVE_DSMC_CMN_CMN_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x1	rx_cmd_almost_empty_watermark Data RX command FIFO almost full watermark. When the space of RX command FIFO is less than this watermark, the almost_empty of RX command FIFO will be asserted.
23:20	RO	0x0	reserved
19:16	RW	0x1	rx_cmd_almost_full_watermark Data RX command FIFO almost full watermark. When the space of RX command FIFO is less than this watermark, the almost_full of RX command FIFO will be asserted.

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:8	RW	0xf	axi_burst_rd_len AXI read burst length.
7:4	RO	0x0	reserved
3:0	RW	0xf	axi_burst_wr_len AXI write burst length.

SLAVE_DSMC_CMN_CMN_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	rdyn_gen_ctrl The capacity of RX FIFO will be made full use in enhanced mode. 1'b0: normal 1'b1: enhance
3:1	RO	0x0	reserved
0	RW	0x0	data_width The data width configuration of slave. 1'b0: X8 1'b1: X16

SLAVE_DSMC_CMN_RGN0_CMN_CON0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	wr_data_cyc_extended DSMC will output extended dummy clock cycle in write transaction when accessing region0. 1'b0: Normal write cycle mode 1'b1: Extend write cycle mode
10:8	RW	0x2	rd_latency_cyc Read latency cycle when accessing region0. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
7	RO	0x0	reserved
6:4	RW	0x2	wr_latency_cyc Write latency cycle when accessing region0. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x1	ca_cyc This bit is used to indicate the address width of the CA phase when accessing region0. 1'b0: 16bit address 1'b1: 32bit address

SLAVE_DSMC_CMN_RGN1_CMN_CON0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	wr_data_cyc_extended DSMC will output extended dummy clock cycle in write transaction when accessing region1. 1'b0: Normal write cycle mode 1'b1: Extend write cycle mode
10:8	RW	0x2	rd_latency_cyc Read latency cycle when accessing region1. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
7	RO	0x0	reserved
6:4	RW	0x2	wr_latency_cyc Write latency cycle when accessing region1. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x1	ca_cyc This bit is used to indicate the address width of the CA phase when accessing region1. 1'b0: 16bit address 1'b1: 32bit address

SLAVE_DSMC_CMN_RGN2_CMN_CON0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	wr_data_cyc_extended DSMC will output extended dummy clock cycle in write transaction when accessing region2. 1'b0: Normal write cycle mode 1'b1: Extend write cycle mode
10:8	RW	0x2	rd_latency_cyc Read latency cycle when accessing region2. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
7	RO	0x0	reserved
6:4	RW	0x2	wr_latency_cyc Write latency cycle when accessing region2. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x1	ca_cyc This bit is used to indicate the address width of the CA phase when accessing region2. 1'b0: 16bit address 1'b1: 32bit address

SLAVE_DSMC_CMN_RGN3_CMN_CON0

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	wr_data_cyc_extended DSMC will output extended dummy clock cycle in write transaction when accessing region3. 1'b0: Normal write cycle mode 1'b1: Extend write cycle mode
10:8	RW	0x2	rd_latency_cyc Read latency cycle when accessing region3. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
7	RO	0x0	reserved
6:4	RW	0x2	wr_latency_cyc Write latency cycle when accessing region3. 3'h1: 1 clock latency 3'h2: 2 clock latency Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x1	ca_cyc This bit is used to indicate the address width of the CA phase when accessing region3. 1'b0: 16bit address 1'b1: 32bit address

SLAVE_DSMC_CMN_DBG_STATUS_0

Address: Operational Base + offset (0x0900)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RO	0x0	axi_wr_resp_error AXI write transaction response error.
1:0	RO	0x0	axi_rd_resp_error AXI read transaction response error.

SLAVE_DSMC_CMN_DBG_STATUS_1

Address: Operational Base + offset (0x0904)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	bus_current_state The state machine of slave.

SLAVE_DSMC_CMN_DBG_STATUS_2

Address: Operational Base + offset (0x0908)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	tx_dat_fifo_space2empty The remained FIFO space of TX data FIFO.
15	RO	0x0	reserved
14:8	RO	0x00	rx_dat_fifo_space2empty The remained FIFO space of RX data FIFO.
7:5	RO	0x0	reserved
4:0	RO	0x00	rx_cmd_fifo_space2empty The remained FIFO space of RX command FIFO.

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36.6 Interface Description

Table 36-1 SLAVE DSMC interface description

Module Pin	Direction	Pin Name	IOMUX Setting
CLK	I	GPIO1_C0	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[3:0]=4'h8
CSN	I	GPIO1_D2	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[11:8]=4'h8
DQS0	I/O	GPIO1_C1	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[7:4]=4'h8
D0	I/O	GPIO1_C2	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[11:8]=4'h8
D1	I/O	GPIO1_C3	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[15:12]=4'h8
D2	I/O	GPIO1_C4	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[3:0]=4'h8
D3	I/O	GPIO1_C5	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[7:4]=4'h8
D4	I/O	GPIO1_C6	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[11:8]=4'h8
D5	I/O	GPIO1_C7	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[15:12]=4'h8
D6	I/O	GPIO1_D0	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[3:0]=4'h8
D7	I/O	GPIO1_D1	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[7:4]=4'h8
INT	O	GPIO1_A1	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[7:4]=4'h8
RDYN	O	GPIO1_D3	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[15:12]=4'h8

Notes: I=input, O=output, I/O=input/output, bidirectional.

36.7 Application Notes

36.7.1 Typical Program Flow

7. Configure the SLAVE_DSMC_AXI_WR_ADDR_SIZE and SLAVE_DSMC_AXI_RD_ADDR_SIZE according to Chip Address Map.
8. The MASTER DSMC configures the Common register bank according to the host setting.
9. The MASTER access the register of FIFO region.

36.7.2 Bulk Data Transfer Program Flow

9. Configure the SLAVE_DSMC_AXI_WR_ADDR_SIZE and SLAVE_DSMC_AXI_RD_ADDR_SIZE according to Chip Address Map.
10. Configure the SLAVE_DSMC_LBC_H2S_INT_STA_EN and SLAVE_DSMC_LBC_H2S_INT_STA_SIG_EN to allow the host to interrupt to slave.
11. The MASTER DSMC configures the Common register bank according to the host setting.
12. The slave chip sends DMA request interrupt signal to the host chip, and the host chip start DMA transfer.
13. The host chip access application register bank to generate host2slave interrupt to inform the slave chip that the transfer is finished.

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Chapter 37 Flexible Bus (FlexBUS)

37.1 Overview

FlexBUS is an AHB slave device. FlexBUS can achieve high-speed IO toggle and imitate some irregular or standards protocols. There are four possible combinations for the serial clock phase and polarity. The chip select signal (csn) is held high when the FlexBUS is idle or disabled. There are two channels which are transmission channel and receiving channel in FlexBUS. Therefore, FlexBUS can support both transmitting and receiving simultaneously. The flexbus0_clk, flexbus0_csn and flexbus0_data ports can be used for transmission channel and receiving channel. The flexbus1_clk, flexbus1_csn and flexbus1_data ports can only be used for receiving channel.

FlexBUS Controller supports the following features:

- Support for built-in DMA and ping-pong operation for allocating two address
- Support for filling in all 0 if the last DMA burst is less than 32Bytes or 64Bytes in receiving mode
- Support timeout interrupt of DMA response
- The direction of flexbus0_data port is I/O, flexbus0_data port can be used for transmission and receiving operation. The direction of flexbus1_data port is Input, flexbus1_data port can only be used for receiving operation
- Support for four working modes
  - Flexbus0_data port is used for transmission channel and receiving channel, flexbus0_clk port is used for transmission channel and receiving channel, supporting three mode: transmit only, receive only, transmission then receive
  - Flexbus0_data port is only used for transmission channel, flexbus0_clk port is used for transmission channel and receiving channel, supporting four mode: transmit only, receive only, transmission then receive, transmission and receive
  - Flexbus0_data port is only used for transmission channel, flexbus0_clk port is only used for transmission channel, supporting three mode: transmit only, receive only, transmission and receive
- Support software configuration and following data for csn port
- Support the image format of BT601 YUV422 and RGB565
- Support YUV422 image format conversion of RGB888
- Support image cropping function
- Support clock port two modes, free running and following data mode
  - Free running mode
    - Txfifo is empty and supports the following two processing modes
      1) Stop transmission, pull up csn and send abnormal interruption
      2) Data, csn remain unchanged and clock hold toggle, send abnormal interruption
    - Rxfifo is pre-full
      1) Stop transmission, pull up csn and send abnormal interruption
  - Following data mode
    - Txfifo is empty and supports the following two processing modes
      1) Stop transmission, pull up csn and send abnormal interruption
      2) Data, csn and clock remain unchanged, send abnormal interruption
    - Rxfifo is pre-full and supports the following two processing modes
      1) Stop transmission, pull up csn and send abnormal interruption
      2) Data, csn and clock remain unchanged, send abnormal interruption
- Support single mode and continuous mode. Continuous mode can not support transmission then receive mode
- Support configurable four possible combinations for the clock port polarity and phase
- Support 1,2,4,8,16bits parallel data transfer
- Support clock port masking function
- Support the maximum of clock port up to 100MHz in transmission mode and receive mode
- Support software configuration modification of sampling points

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37.2 Block Diagram

The FlexBUS Controller comprises with:

- **AHB_CFG**

The AHB_CFG contains control registers of transmitters and receiver.

- **AXI Master Interface and DMA Controller**

The AXI Master Interface and DMA Controller implement for reading data from DDR and writing data to DDR.

- **Engine**

The Engine implements control over all modules and monitor the generation of abnormal interrupts.

- **IOBUF**

The IOBUF implements logic of data, csn and clock port.

- **TX and RX FIFO**

The TX FIFO is the buffer to store transmitted data. The TX FIFO is the buffer to store received data. The size of the TX and RX FIFO is 32bits x 256.

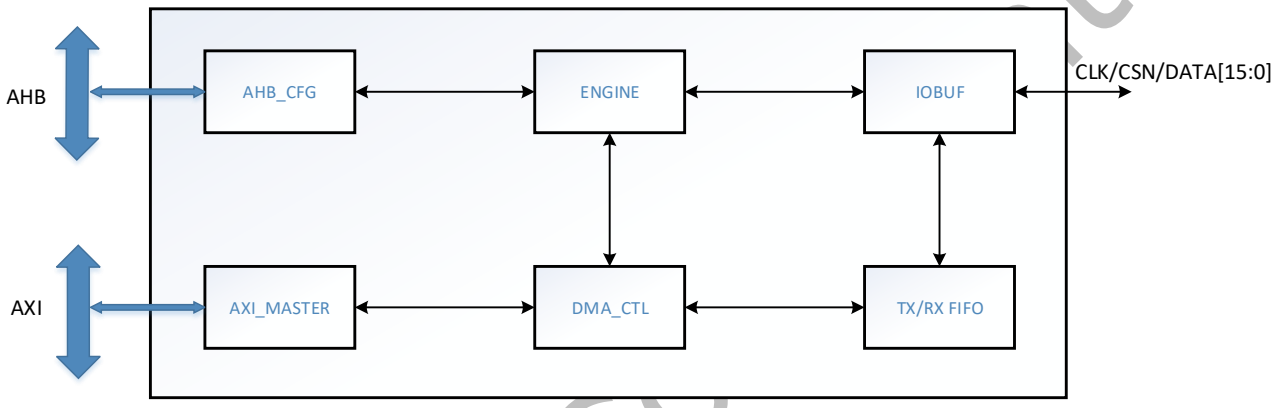

Fig. 37-1 FlexBUS Controller Block diagram

37.3 Function Description

37.3.1 Transfer Modes

According to multiplexed of flexbus0_data and flexbus0_clk ports, FlexBUS can be divided into different working modes. The following table shows the ports in different transfer modes.

Table 37-1 FlexBUS Tranfer Modes Port List

COM_CTL[3:2]	TX Only	RX Only	TX and RX	TX then RX
2'b11	flexbus0_data/ flexbus0_clk/ flexbus0_csn/	flexbus0_data/ flexbus0_clk/ flexbus0_csn/	not support	flexbus0_data/ flexbus0_clk flexbus0_csn
2'b01		flexbus1_data/ flexbus0_clk/ flexbus0_csn	flexbus0_data/flexbus1_data flexbus0_clk/ flexbus0_csn/	flexbus0_data/flexbus1_data flexbus0_clk flexbus0_csn
2'b00		flexbus1_data/ flexbus1_clk/ flexbus1_csn/	flexbus0_data/flexbus1_data flexbus0_clk/flexbus1_clk flexbus0_csn/flexbus1_csn	not support

37.3.2 Free Running

Flexbus0/1_clk can output earlier than csn begin active in free running mode. Flexbus0/1_clk can output as soon as FLEXBUS_FREE_SCLK is configured to 1. When FLEXBUS_FREE_SCLK is configured to 0, Flexbus0/1_clk will follow data after flexbus0/1_csn being active.

37.3.3 Single and Continuous Mode

37.3.3.1 Single Mode

In this mode, the amount of data transmitted or received is determined by FLEXBUS_TX_NUM/RX_NUM. FlexBUS will stop and send interrupt when the amount of data transmitted or received reaches the FLEXBUS_TX_NUM/RX_NUM. The address of

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transmission is FLEXBUS_DMA_SRC_ADDR0/DMA_DST_ADDR0. If the value of FLEXBUS_TX_NUM/RX_NUM is greater than FLEXBUS_DMA_SRC_LEN0/DMA_DST_LEN0, FlexBUS will automatically jump to FLEXBUS_DMA_SRC_ADDR1/DMA_DST_ADDR1 after FLEXBUS_DMA_SRC_ADDR0/ DMA_DST_ADDR0 is full. So it is recommended that the value of FLEXBUS_TX_NUM/RX_NUM is smaller than FLEXBUS_DMA_SRC_LEN0/DMA_DST_LEN0 in single mode.

37.3.3.2 Continuous Mode

In continuous mode, FlexBUS keeps working until the value of FLEXBUS_STOP is set and FLEXBUS_RX_NUM/TX_NUM will be ignored. FlexBUS will send interrupt when FLEXBUS_STOP is set. The user can configures two buffer which buffer0 is configured by FLEXBUS_DMA_SRC_ADDR0/DMA_DST_ADDR0 and FLEXBUS_DMA_SRC_LEN0/DMA_DST_LEN0, buffer1 is configured by FLEXBUS_DMA_SRC_ADDR1/DMA_DST_ADDR1 and FLEXBUS_DMA_SRC_LEN1/DMA_DST_LEN1. After the amount of data transmitted and received reaches the value of buffer0, FlexBUS will automatically jump to buffer1 and the user can configure new address of buffer0 and clear buffer0 interrupt status. Similarly, FlexBUS will automatically jump to buffer0 and the user can configure new address of buffer1 and clear buffer1 interrupt status after the amount of data transmitted and received reaches the value of buffer1.

37.3.4 CPOL and CPHA

The clock polarity (CPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. This is same as SPI. To transmit data, both FlexBUS and peripherals must have identical serial clock phase (CPHA) and clock polarity (CPOL) values. The data frame can be 1/2/4/8/16 bits in length.

When the configuration parameter CPHA = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the data lines prior to the first serial clock edge. The following two figures show a timing diagram for FlexBUS data transfer with CPHA = 0. The serial clock is shown for configuration parameters CPOL = 0 and CPOL = 1.

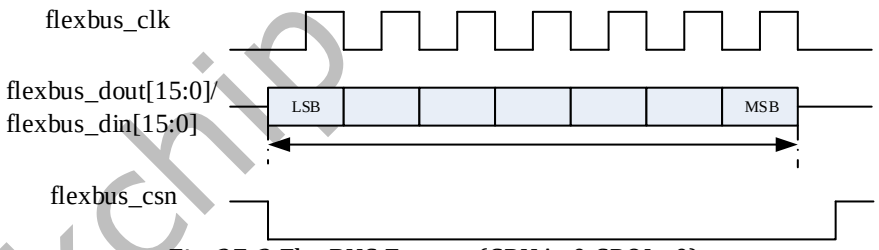

Fig. 37-2 FlexBUS Format (CPHA=0 CPOL=0)

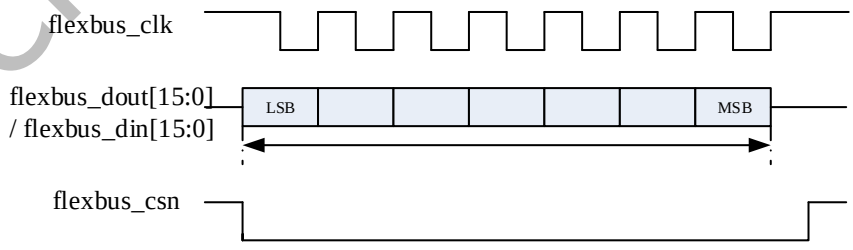

Fig. 37-3 FlexBUS Format (CPHA=0 CPOL=1)

When the configuration parameter CPHA = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select signal may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the FlexBUS format when the configuration parameter CPHA = 1.

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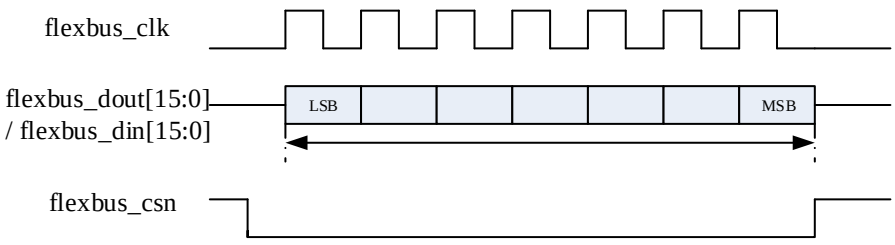

Fig. 37-4 FlexBUS Format (CPHA=1 CPOL=0)

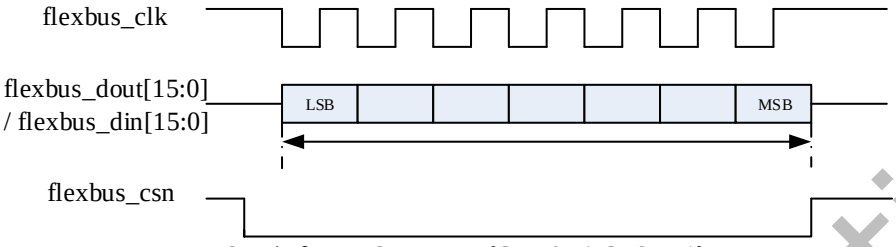

Fig. 37-5 FlexBUS Format (CPHA=1 CPOL=1)

37.3.5 TX Then RX Mode

CPHA=1, CPOL=0, transmit data at the posedge of CLKA and receive data at the negedge of CLKA. At T2, the last data is transmitted, and at T3, data pad would change to input. When FLEXBUS_RXCLK_DUMMY[4:0]=0, at T3 negedge of CLKA, rx channel would sample data; when FLEXBUS_RXCLK_DUMMY[4:0]=1, at T4 negedge of CLKA, rx channel would sample data.

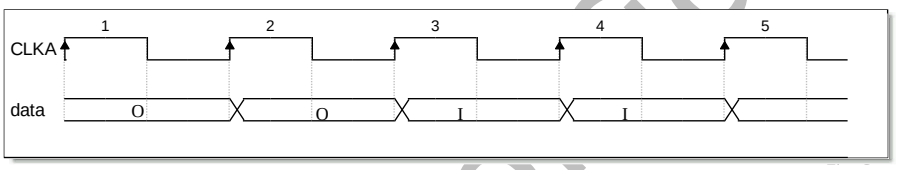

Fig. 37-6 FlexBUS TX Then RX Mode (CPHA=1 CPOL=0)

37.3.6 DVP Slave Mode

37.3.6.1 Support Vsync high active or low active

Vsync Low active

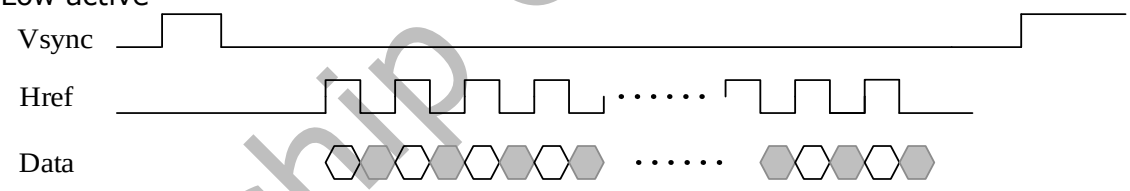

Fig. 37-7 Timing Diagram When VSYNC Low Active

Vsync High active

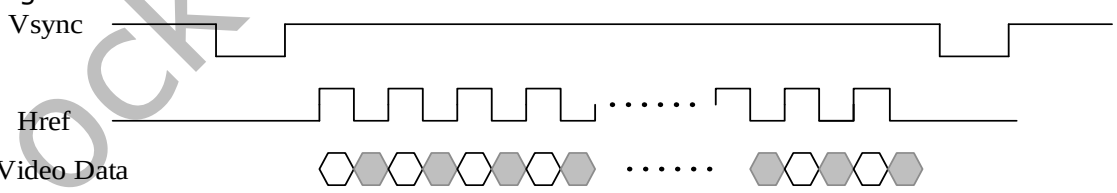

Fig. 37-8 Timing Diagram When VSYNC High Active

37.3.6.2 Support Href High Active or Low Active

Href high active

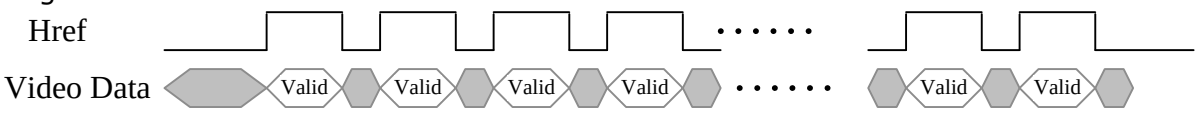

Fig. 37-9 Timing Diagram When HREF High Active

Href Low active

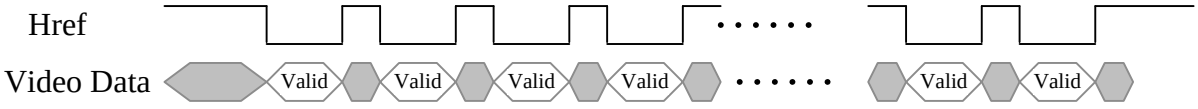

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Fig. 37-10 Timing Diagram When HREF Low Active

37.3.6.3 Data Format

YUV422 For Y first

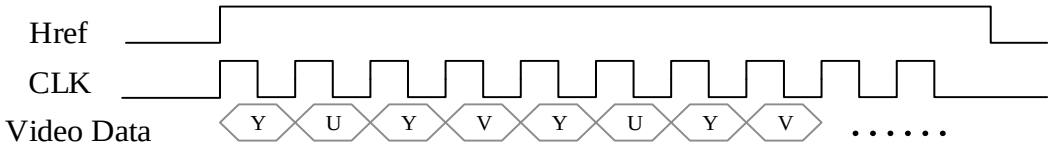

Fig. 37-11 Timing Diagram When Y Data First

YUV422 For U first

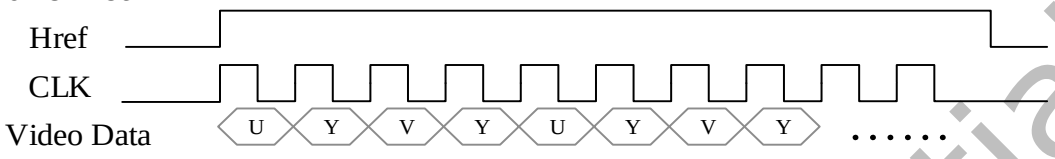

Fig. 37-12 Timing Diagram When U Data First

RGB565 For B first

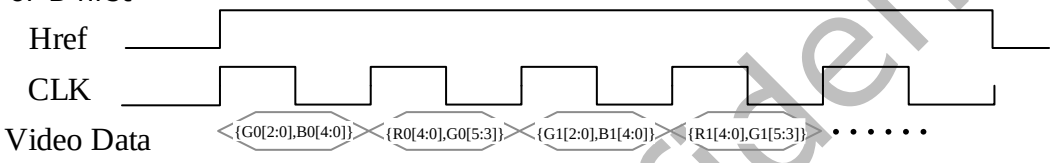

Fig. 37-13 Timing Diagram When B Data First

RGB565 For R first

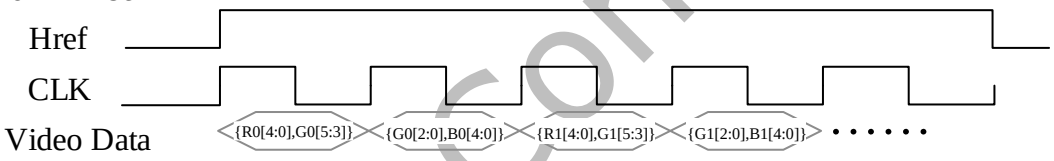

Fig. 37-14 Timing Diagram When R Data First

37.3.6.4 One Frame Stop Mode

In this mode, configure the register FLEXBUS_RX_CTL to one frame stop mode. After one frame captured, FlexBUS will automatic stop and send interrupt. FlexBUS will not capture the sensor data. The address of Y/UV is FLEXBUS_DMA_DST_ADDR0.

37.3.6.5 Frame Ping-Pong Mode

After one frame(F0) captured, FlexBUS will jump to buffer1 and start to capture the next frame(F1) automatically, and host must assign new address pointer of frame0 and clear the frame0 status, thus FlexBUS will capture the third frame automatically(by new F0 address) without any stop and so on for the following frames.

37.3.6.6 Storage

Y/UV data or R/G/B data will be storage in the same buffer. In addition, the amount of data in a row must be an integer multiple of 4Bytes.

37.3.6.7 Crop

The register FLEXBUS_DVP_CROP_START defines the coordinate of crop start point. And the frame size after cropping is following the value of FLEXBUS_DVP_CROP_SIZE. Bypass or crop the source video data to a smaller size destination.

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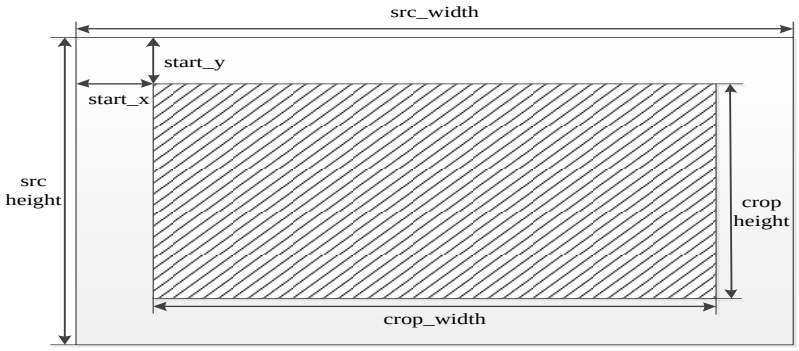

Fig. 37-15 Crop

37.3.7 QSPI

37.3.7.1 Command and Address

There are three phases in QSPI mode, which are command phase, address phase and data phase. The user can configure FLEXBUS_TX_CMD0 and FLEXBUS_TX_CMD1 in command and address phase. The register FLEXBUS_TX_CMD0 and FLEXBUS_TX_CMD1 can store up to 64bits data and data is sent from MSB of TX_CMD0 and TX_CMD1. FlexBUS can support x1 and x4 for command phase and address phase.

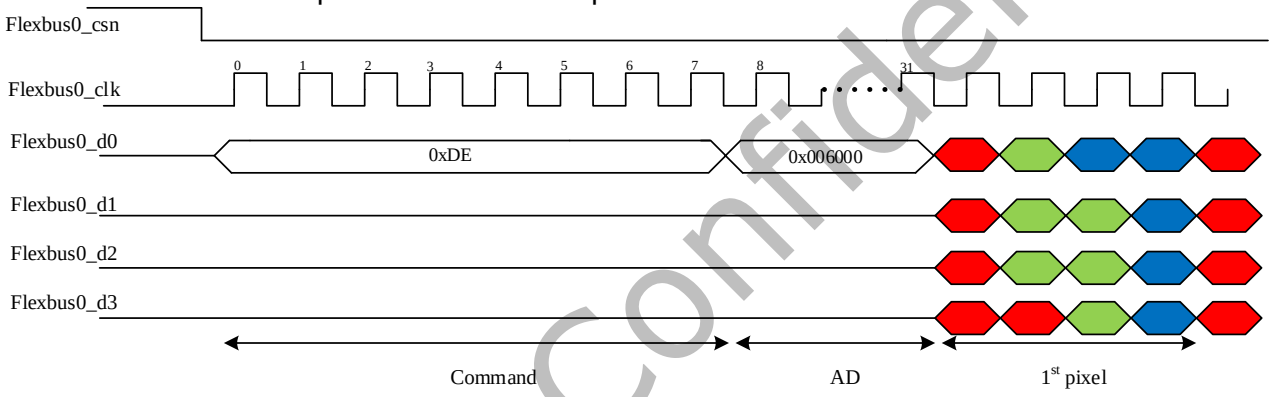

Fig. 37-16 Timing diagram in QSPI Mode

The user can configure FLEXBUS_TX_CMD0 = 0xDE006000 to achieve the timing shown in the figure above.

37.3.7.2 Multi-Line

FlexBUS can support multi-line transfer mode. The command and address should be same on each line of transmission. FLEXBUS_TX_CMD_LEN controls the length of the command and address, which unit is determined by FLEXBUS_TX_CTL[12](1bit or 4bits). FLEXBUS_TX_WIDTH controls the length of pixel data per line, which unit is determined by FLEXBUS_TX_CTL[31:29]. Flexbus0_csn will automatically be switched to high level when a line of pixel data is sent. The duration of high level is determined by FLEXBUS_TX_CSN_DUMMY.

The relation between FLEXBUS_TX_NUM and FLEXBUS_TX_WIDTH/FLEXBUS_TX_CMD_LEN is as follows:

FLEXBUS_TX_NUM = (number of lines) x (FLEXBUS_TX_WIDTH + FLEXBUS_TX_CMD_LEN).

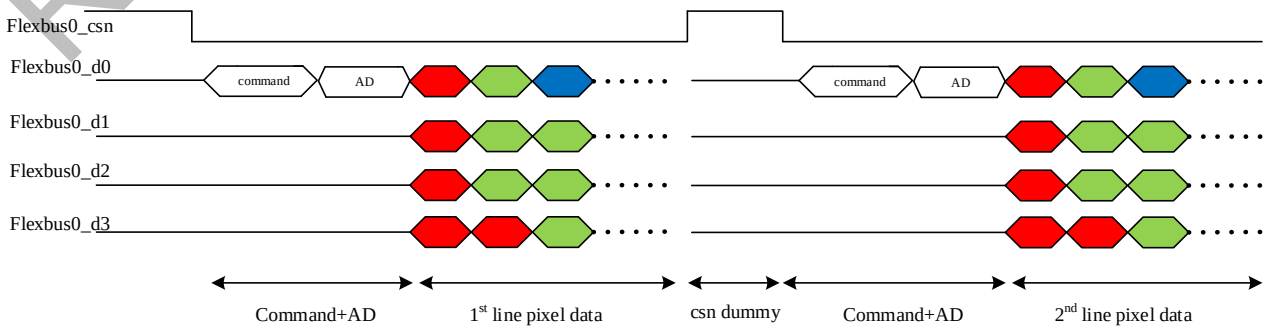

Fig. 37-17 Timing diagram in Multi-line

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37.4 Register Description

37.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

37.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
FLEXBUS_ENR	0x0000	W	0x00000000	Enable Register
FLEXBUS_FREE_SCLK	0x0004	W	0x00000000	Sclk Free Register
FLEXBUS_CSN_CFG	0x0008	W	0x00000000	Csn Config Register
FLEXBUS_COM_CTL	0x000C	W	0x00000004	Common Control Register
FLEXBUS_REMAP	0x0010	W	0x00000000	Data IO Remap Register
FLEXBUS_STOP	0x0014	W	0x00000000	Continue Mode Stop Register
FLEXBUS_SLAVE_MODE	0x0018	W	0x00000001	Slave Mode Register
FLEXBUS_DVP_POL	0x001C	W	0x00000000	DVP Interface Register
FLEXBUS_DVP_CROP_SIZE	0x0020	W	0x00000000	The Expected Width And Height of Received Image
FLEXBUS_DVP_CROP_START	0x0024	W	0x00000000	The Start Point of DVP Path Cropping
FLEXBUS_DVP_ORDER	0x0028	W	0x00000000	YVYU422 Mode Order
FLEXBUS_DVP_YUV2RGB	0x002C	W	0x00000000	YUV2RGB Mode
FLEXBUS_TX_CTL	0x0040	W	0x00000000	Tx Control Register
FLEXBUS_TX_NUM	0x0044	W	0x00000000	Tx Length Register
FLEXBUS_TXWAT_START	0x0048	W	0x00000000	Waterline To Start Transmission Register
FLEXBUS_TXFIFO_DNUM	0x004C	W	0x00000000	Transmit FIFO Level
FLEXBUS_TX_WIDTH	0x0050	W	0x00000000	The Expected Width of Image
FLEXBUS_TX_CSN_DUMMY	0x0054	W	0x00000000	Csn Inactive Counter
FLEXBUS_TX_CMD_LEN	0x0058	W	0x00000000	TX Command Width
FLEXBUS_TX_CMD0	0x005C	W	0x00000000	TX Command0 Register
FLEXBUS_TX_CMD1	0x0060	W	0x00000000	TX Command1 Register
FLEXBUS_RX_CTL	0x0080	W	0x00000000	RX Control Register
FLEXBUS_RX_NUM	0x0084	W	0x00000000	RX Length Register
FLEXBUS_RXFIFO_DNUM	0x0088	W	0x00000000	Receive FIFO Level
FLEXBUS_DLL_EN	0x008C	W	0x00000000	Delayline Enable Register
FLEXBUS_DLL_NUM	0x0090	W	0x00000000	Delayline Number Register
FLEXBUS_RXCLK_DUMMY	0x0094	W	0x00000000	RX CLK Dummy Register
FLEXBUS_RXCLK_CAP_CNT	0x0098	W	0x00000000	RX Capture Counter Register
FLEXBUS_DMA_RD_OUTSTD	0x0100	W	0x0000000F	DMA Read Outstanding Register
FLEXBUS_DMA_WR_OUTSTD	0x0104	W	0x0000000F	DMA Write Outstanding Register
FLEXBUS_DMA_SRC_ADDR0	0x0108	W	0x00000000	DMA Source Address0 Register
FLEXBUS_DMA_DST_ADDR0	0x010C	W	0x00000000	DMA Destination Address0 Register
FLEXBUS_DMA_SRC_ADDR1	0x0110	W	0x00000000	DMA Source Address1 Register
FLEXBUS_DMA_DST_ADDR1	0x0114	W	0x00000000	DMA Destination Address1 Register
FLEXBUS_DMA_SRC_LEN0	0x0118	W	0x00000000	DMA Source Address0 Size Register

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Name	Offset	Size	Reset Value	Description
FLEXBUS_DMA_DST_LEN0	0x011C	W	0x00000000	DMA Destination Address0 Size Register
FLEXBUS_DMA_SRC_LEN1	0x0120	W	0x00000000	DMA Source Address1 Size Register
FLEXBUS_DMA_DST_LEN1	0x0124	W	0x00000000	DMA Source Address0 Size Register
FLEXBUS_DMA_WAT_INT	0x0128	W	0x00000000	DMA Watermark Register
FLEXBUS_DMA_TIMEOUT	0x012C	W	0x00000000	DMA Timeout Register
FLEXBUS_DMA_RD_LEN	0x0130	W	0x00000000	DMA Read Burst Length
FLEXBUS_STATUS	0x0160	W	0x00000000	Status Register
FLEXBUS_IMR	0x0164	W	0x00000000	Interrupt Mask
FLEXBUS_RISR	0x0168	W	0x00000000	Raw Interrupt Status
FLEXBUS_ISR	0x016C	W	0x00000000	Interrupt Status
FLEXBUS_ICR	0x0170	W	0x00000000	Interrupt Clear
FLEXBUS_REVISION	0x01F0	W	0x010D0844	SVN Revision

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

37.4.3 Detail Registers Description

FLEXBUS_ENR

Address: Operational Base(0xFF880000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	rx_enr Enables and disables all rx logic operations. Receive FIFO buffers are cleared when rx logic is disabled. 1'b1: Enable 1'b0: Disable
0	RW	0x0	tx_enr Enables and disables all tx logic operations. Transmit FIFO buffers are cleared when tx logic is disabled. 1'b1: Enable 1'b0: Disable

FLEXBUS_FREE_SCLK

Address: Operational Base(0xFF880000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	rx_free_mode If set to 1, rx 1xclk output in advance, not following data.
0	RW	0x0	tx_free_mode If set to 1, tx 1xclk output in advance, not following data.

FLEXBUS_CSN_CFG

Address: Operational Base(0xFF880000) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	rx_csn_cfg 1'b1: If set to 1, rx csn is active low in advance. 1'b0: Rx csn follows data.
0	RW	0x0	tx_csn_cfg 1'b1: If set to 1, tx csn is active low in advance. 1'b0: Tx csn follows data.

FLEXBUS_COM_CTL

Address: Operational Base(0xFF880000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	rxfifo_expand If set to 1, txfifo would be used for rxfifo in rx only mode. The capacity of rxfifo would be doubled to the original.
4	RW	0x0	txfifo_expand If set to 1, rxfifo would be used for txfifo in tx only mode. The capacity of txfifo would be doubled to the original.
3	RW	0x0	tx_use_rx If set to 1, tx data channel will be used for rx data channel.
2	RW	0x1	sclk_share If set to 1, rx logic and tx logic use the same 2xclk and 1xclk.
1:0	RW	0x0	tx_rx_mode Transmit and receive mode select. 2'b00: Transmit & Receive 2'b01: Transmit Only 2'b10: Receive Only 2'b11: Transmit first, and then change to receive

FLEXBUS_REMAP

Address: Operational Base(0xFF880000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	rx_data_remap When rx_data_width=0, 3'b000: Din[0] PAD input valid. 3'b001: Din[1] PAD input valid. 3'b010: Din[2] PAD input valid. 3'b011: Din[3] PAD input valid. 3'b100: Din[4] PAD input valid. 3'b101: Din[5] PAD input valid. 3'b110: Din[6] PAD input valid. 3'b111: Din[7] PAD input valid. When rx_data_width=1, 3'b000: Din[1:0] PAD input valid. 3'b001: Din[3:2] PAD input valid. 3'b010: Din[5:4] PAD input valid. 3'b011: Din[7:6] PAD input valid. 3'b100: Din[9:8] PAD input valid. 3'b101: Din[11:10] PAD input valid. 3'b110: Din[13:12] PAD input valid. 3'b111: Din[15:14] PAD input valid. When rx_data_width=2, 3'b000: Din[3:0] PAD input valid. 3'b001: Din[7:4] PAD input valid. 3'b010: Din[11:8] PAD input valid. 3'b011: Din[15:12] PAD input valid. Reserved. When rx_data_width=3, 3'b000: Din[7:0] PAD input valid. 3'b001: Din[15:8] PAD input valid. Reserved. When rx_data_width=4, 3'b000: Din[15:0] PAD input valid. Reserved.
3	RO	0x0	reserved
2:0	RW	0x0	tx_data_remap When tx_data_width=0, 3'b000: Dout[0] PAD output valid. 3'b001: Dout[1] PAD output valid. 3'b010: Dout[2] PAD output valid. 3'b011: Dout[3] PAD output valid. 3'b100: Dout[4] PAD output valid. 3'b101: Dout[5] PAD output valid. 3'b110: Dout[6] PAD output valid. 3'b111: Dout[7] PAD output valid. When tx_data_width=1, 3'b000: Dout[1:0] PAD output valid. 3'b001: Dout[3:2] PAD output valid. 3'b010: Dout[5:4] PAD output valid. 3'b011: Dout[7:6] PAD output valid. 3'b100: Dout[9:8] PAD output valid. 3'b101: Dout[11:10] PAD output valid. 3'b110: Dout[13:12] PAD output valid. 3'b111: Dout[15:14] PAD output valid. When tx_data_width=2, 3'b000: Dout[3:0] PAD output valid. 3'b001: Dout[7:4] PAD output valid. 3'b010: Dout[11:8] PAD output valid.

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Bit	Attr	Reset Value	Description
			3'b011: Dout[15:12] PAD output valid. Reserved. When tx_data_width=3, 3'b000: Dout[7:0] PAD output valid. 3'b001: Dout[15:8] PAD output valid. Reserved. When tx_data_width=4, 3'b000: Dout[15:0] PAD output valid. Reserved.

FLEXBUS_STOP

Address: Operational Base(0xFF880000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/WSC	0x0	rx_stop In rx continue mode, used to stop receive.
0	R/WSC	0x0	tx_stop If set to 1, it used to stop transmit in continue mode.

FLEXBUS_SLAVE_MODE

Address: Operational Base(0xFF880000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dvp_sel 1'b0: Work as ADC 1'b1: Work as DVP interface
0	RW	0x1	clk1_in If set to 1, slave mode is enabled and rx logic uses flexbus_clk1_in as the 2xclk.

FLEXBUS_DVP_POL

Address: Operational Base(0xFF880000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	href_pol 1'b1: High active. 1'b0: Low active.
0	RW	0x0	vsync_pol 1'b1: High active. 1'b0: Low active.

FLEXBUS_DVP_CROP_SIZE

Address: Operational Base(0xFF880000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_height The expected height of received image.
15:0	RW	0x0000	sw_width The expected width of received image. The value of the register is equal to the number of bytes. So if one pixel is equal to 2bytes, the value of the register is double to width of image.

FLEXBUS_DVP_CROP_START

Address: Operational Base(0xFF880000) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_start_y The vertical ordinate of the start point.
15:0	RW	0x0000	sw_start_x The horizontal ordinate of the start point. The value of the register is equal to the number of bytes. So if one pixel is equal to 2bytes, the value of the register is double to width of image.

FLEXBUS_DVP_ORDER

Address: Operational Base(0xFF880000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	out_order 2'b00: YVYU(Y is LSB) 2'b01: VYUY(V is LSB) 2'b10: YUYV(Y is LSB) 2'b11: UYVY(U is LSB)
1:0	RW	0x0	in_order 2'b00: YVYU(Y is LSB) 2'b01: VYUY(V is LSB) 2'b10: YUYV(Y is LSB) 2'b11: UYVY(U is LSB)

FLEXBUS_DVP_YUV2RGB

Address: Operational Base(0xFF880000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	rb_swap 1'b1: B is in LSB byte. 1'b0: B is in MSB byte.
2:1	RW	0x0	mode Source bitmap YUV2RGB conversion mode 2'b00,2'b01: BT.601-range0(limit range) 2'b10: BT.601-range1(full range) 2'b11: BT.709-range0(limit range)
0	RW	0x0	enable 1'b1: YUV2RGB mode enable. 1'b0: YUV2RGB mode disable.

FLEXBUS_TX_CTL

Address: Operational Base(0xFF880000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	data_width Selects the data frame length. 3'b000: 1bit data 3'b001: 2bit data 3'b010: 4bit data 3'b011: 8bit data 3'b100: 16bit data
28:17	RO	0x000	reserved
16	RW	0x0	oen_pre To improve the data IO timing of switching from input to output, the application can set this register to switch IO from input to output in advance for one cycle. Unit is 2xclk. 1'b0: Zero 1'b1: One cycle

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Bit	Attr	Reset Value	Description
15	RW	0x0	oen_dly To improve the data IO timing of switching from output to input, the application can set this register to extend data IO output time at the last 1xclk. Unit is 2xclk. 1'b0: One cycle 1'b1: Two cycle
14	RW	0x0	dat_unit 1'b0: Unit is word when shift is 1'b1. 1'b1: Unit is byte when shift is 1'b1.
13	RW	0x0	shift 1'b0: First parallel bit is LSB in shift register. 1'b1: First parallel bit is MSB in shift register.
12	RW	0x0	cmd_width Command and address line width. 1'b0: x1 mode. 1'b1: x4 mode.
11	RW	0x0	multi_line 1'b1: Multi-line transmission and csn auto switching is enable. 1'b0: Multi-line transmission and csn auto switching is disable.
10:9	RW	0x0	csn_pos_cnt_cfg The register should be configured to define the number of the 2xclk cycles between csn inactive and data stop transmission. Unit is 2xclk. 2'b00: 2 cycles delay 2'b01: 3 cycles delay 2'b10: 4 cycles delay 2'b11: 5 cycles delay
8:7	RW	0x0	csn_neg_cnt_cfg The register should be configured to define the number of the 1xclk cycles between csn active and data active. Unit is 1xclk. 2'b00: Do not delay 2'b01: half cycle delay 2'b10: one cycles delay 2'b11: one and half cycles delay
6	RW	0x0	cutoff_cfg Cutoff function enable/disable. When txfifo is empty, tx logic will stop 1xclk until txfifo is not empty. 1'b1: Enable 1'b0: Disable
5	RW	0x0	1xclk_mask 1xclk mask enable/disable. 1'b1: Enable 1'b0: Disable
4	RW	0x0	continue_mode Continue mode enable/disable. 1'b1: Enable 1'b0: Disable
3	RW	0x0	cpol 1'b0: Inactive state of 1xclk is low. 1'b1: Inactive state of 1xclk is high.
2	RW	0x0	cpha 1'b0: 1xclk toggles in middle of first data bit. 1'b1: 1xclk toggles at start of first data bit.
1:0	RO	0x0	reserved

FLEXBUS_TX_NUM

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Address: Operational Base(0xFF880000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	num The register field sets the number of data frames to transmit. The FlexBUS continues to transmit data until the number of data frames transmitted is equal to this register value. Unit is data_width.

FLEXBUS_TXWAT_START

Address: Operational Base(0xFF880000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	txfifo_wat_start When the number of words in transmit FIFO is more than or equal to this value, the transmit logic starts work. Unit is word.

FLEXBUS_TXFIFO_DNUM

Address: Operational Base(0xFF880000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	dnum Contains the number of valid data entries in the transmit FIFO. Unit is word.

FLEXBUS_TX_WIDTH

Address: Operational Base(0xFF880000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	width_size In tx multi-line mode, the number of data will be transmitted when csn is low at one time, excluding command length. Unit is data_width.

FLEXBUS_TX_CSN_DUMMY

Address: Operational Base(0xFF880000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	csn_dummy The register should be configured to define the number of the 2xclk cycles between csn inactive and csn active. Unit is 2xclk.

FLEXBUS_TX_CMD_LEN

Address: Operational Base(0xFF880000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	cmd_len The number of data will be transmitted in one wire mode. Unit is bit. The minimum configured value should be greater than 1.

FLEXBUS_TX_CMD0

Address: Operational Base(0xFF880000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd0 Data used to transmit in one wire mode.

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FLEXBUS_TX_CMD1

Address: Operational Base(0xFF880000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd1 Data used to transmit in one wire mode.

FLEXBUS_RX_CTL

Address: Operational Base(0xFF880000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	data_width Selects the data frame length. 3'b000: 1bit data 3'b001: 2bit data 3'b010: 4bit data 3'b011: 8bit data 3'b100: 16bit data
28:18	RO	0x000	reserved
17	RW	0x0	fill_dummy FlexBUS will automatically fill in dummy 0 when the last data is not enough to make up for 4bytes. 1'b1: Enable 1'b0: Disable
16	RW	0x0	dat_unit 1'b0: Unit is word when shift is 1'b1. 1'b1: Unit is byte when shift is 1'b1.
15	RW	0x0	shift 1'b0: First parallel bit is LSB in shift register. 1'b1: First parallel bit is MSB in shift register.
14	RW	0x0	auto_pad When the remaining number of data entries in rxfifo is less than one burst data of DMA, the DMA request will not be set high, but if this bit set to 1, the DMA request will be raised, and 0 will be automatically added to make up for the data volume.
13:9	RW	0x00	csn_pos_cnt_cfg The register should be configured to define the number of the 2xclk cycles between csn inactive and data stop receiving. Unit is 2xclk. 5'b00: 1 cycle delay 5'b01: 2 cycles delay 5'b10: 3 cycles delay 5'b11: 4 cycles delay 5'h1f: Max 32 cycles delay
8:7	RW	0x0	csn_neg_cnt_cfg The register should be configured to define the number of the 1xclk cycles between csn active and data active. 2'b00: Do not delay 2'b01: half cycle delay 2'b10: one cycles delay 2'b11: one and half cycles delay
6	RW	0x0	cutoff_cfg Cutoff function enable/disable. When rxfifo is full, rx logic will stop 1xclk until rxfifo is not full. 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
5	RW	0x0	rxd_dy If the rxd data cannot be sampled by the sclk edge at the right time, this register should be configured to define the number of the 2xclk cycles after the active 1xclk edge to sample rxd data later when FlexBUS works at high frequency. Unit is 2xclk. 1'b0: Do not delay 1'b1: One cycle delay
4	RW	0x0	continue_mode Continue mode enable/disable. 1'b1: Enable 1'b0: Disable
3	RW	0x0	cpol 1'b0: Inactive state of 1xclk is low. 1'b1: Inactive state of 1xclk is high.
2	RW	0x0	cpha 1'b0: 1xclk toggles in middle of first data bit. 1'b1: 1xclkl clock toggles at start of first data bit.
1:0	RO	0x0	reserved

FLEXBUS_RX_NUM

Address: Operational Base(0xFF880000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	num The register field sets the number of data frames to receive. The FlexBUS continues to receive data until the number of data frames transmitted is equal to this register value. This value contains rx_clk_dummy. Unit is data_width.

FLEXBUS_RXFIFO_DNUM

Address: Operational Base(0xFF880000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	dnum Contains the number of valid data entries in the receive FIFO. Unit is word.

FLEXBUS_DLL_EN

Address: Operational Base(0xFF880000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	enable If set to 1, rx delayline clock is enable.

FLEXBUS_DLL_NUM

Address: Operational Base(0xFF880000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	num The number steps of delayline.

FLEXBUS_RXCLK_DUMMY

Address: Operational Base(0xFF880000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	rx_clk_dummy In transmission then receive mode, this register should be configured to define the number of the 1xclk cycles after transmit operation finish to sample rx data. Unit is 1xclk.

FLEXBUS_RXCLK_CAP_CNT

Address: Operational Base(0xFF880000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	rx_cap_cnt Used to define the position of the first data being captured. Unit is 1xclk.

FLEXBUS_DMA_RD_OUTSTD

Address: Operational Base(0xFF880000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x0f	read_outstanding DMA read outstanding is equal to (register + 1).

FLEXBUS_DMA_WR_OUTSTD

Address: Operational Base(0xFF880000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x0f	write_outstanding DMA write outstanding is equal to (register + 1).

FLEXBUS_DMA_SRC_ADDR0

Address: Operational Base(0xFF880000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	src_addr0 The first source address. The address is 4Byte alignment. Unit is 4Byte. So the register value is equal to 1, DMA source address is equal to 30'h04.

FLEXBUS_DMA_DST_ADDR0

Address: Operational Base(0xFF880000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dst_addr0 The first destination address. Unit is 4Byte.

FLEXBUS_DMA_SRC_ADDR1

Address: Operational Base(0xFF880000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	src_addr1 The second source address. Unit is 4Byte.

FLEXBUS_DMA_DST_ADDR1

Address: Operational Base(0xFF880000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:0	RW	0x00000000	dst_addr1 The second destination address. Unit is 4Byte.

FLEXBUS_DMA_SRC_LEN0

Address: Operational Base(0xFF880000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:6	RW	0x000000	src_len0 The size of first source address. Unit is byte.
5:0	RO	0x00	reserved

FLEXBUS_DMA_DST_LEN0

Address: Operational Base(0xFF880000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:6	RW	0x000000	dst_len0 The size of first destination address. Unit is byte.
5:0	RO	0x00	reserved

FLEXBUS_DMA_SRC_LEN1

Address: Operational Base(0xFF880000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:6	RW	0x000000	src_len1 The size of second source address. Unit is byte.
5:0	RO	0x00	reserved

FLEXBUS_DMA_DST_LEN1

Address: Operational Base(0xFF880000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:6	RW	0x000000	dst_len1 The size of second destination address. Unit is byte.
5:0	RO	0x00	reserved

FLEXBUS_DMA_WAT_INT

Address: Operational Base(0xFF880000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	src_wat_lvl Used to configure the watermark interrupt of read buffer0 and buffer1. 2'b00: The amount of data read from DDR is up to one-quarter of the size of source address. 2'b00: The amount of data read from DDR is up to half of the size of source address. 2'b10 or 2'b11: The amount of data read from DDR is up to the size of source address.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	dst_wat_lvl Used to configure the watermark interrupt of write buffer0 and buffer1. 2'b00: The amount of data written to DDR is up to one-quarter of the size of destination address. 2'b00: The amount of data written to DDR is up to half of the size of destination address. 2'b10 or 2'b11: The amount of data written to DDR is up to the size of destination address.

FLEXBUS_DMA_TIMEOUT

Address: Operational Base(0xFF880000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:1	RW	0x000	counter The register is used to define the time when the timeout interrupt is triggered. The actual internal delay time is x16 the value of register. Unit is 2xclk.
0	RW	0x0	en 1'b1: Timeout function is enable. 1'b0: Timeout function is disable.

FLEXBUS_DMA_RD_LEN

Address: Operational Base(0xFF880000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	burst_len8 1'b1: DMA read burst length is equal to 8. 1'b0: DMA read burst length is equal to 16.

FLEXBUS_STATUS

Address: Operational Base(0xFF880000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	rx_empty 1'b0: Receive FIFO is not empty. 1'b1: Receive FIFO is empty.
4	RO	0x0	rx_full 1'b0: Receive FIFO is not full. 1'b1: Receive FIFO is full.
3	RO	0x0	tx_empty 1'b0: Transmit FIFO is not empty. 1'b1: Transmit FIFO is empty.
2	RO	0x0	tx_full 1'b0: Transmit FIFO is not full. 1'b1: Transmit FIFO is full.
1	RO	0x0	rx_busy When set, indicates that receive transfer is in progress; when cleared, indicates that the receive is idle or disabled.
0	RO	0x0	tx_busy When set, indicates that transmission transfer is in progress; when cleared, indicates that the transmission is idle or disabled.

FLEXBUS_IMR

Address: Operational Base(0xFF880000) + offset (0x0164)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	dma_timeout_im 1'b0: Timeout interrupt is masked. 1'b1: Timeout interrupt is not masked.
12	RW	0x0	dma_err_im 1'b0: DMA error response interrupt is masked. 1'b1: DMA error response interrupt is not masked.
11	RW	0x0	dma_dst1_im 1'b0: DMA write buffer1 interrupt is masked. 1'b1: DMA write buffer1 interrupt is not masked.
10	RW	0x0	dma_dst0_im 1'b0: DMA write buffer0 interrupt is masked. 1'b1: DMA write buffer0 interrupt is not masked.
9	RW	0x0	dma_src1_im 1'b0: DMA read buffer1 interrupt is masked. 1'b1: DMA read buffer1 interrupt is not masked.
8	RW	0x0	dma_src0_im 1'b0: DMA read buffer0 interrupt is masked. 1'b1: DMA read buffer0 interrupt is not masked.
7	RW	0x0	dvp_frame_start_im 1'b0: Frame start interrupt is masked. 1'b1: Frame start interrupt is not masked.
6	RW	0x0	dvp_frame_ab 1'b0: Frame abnormal interrupt is masked. 1'b1: Frame abnormal interrupt is not masked.
5	RW	0x0	rx_done_im 1'b0: Receive finish interrupt is masked. 1'b1: Receive finish interrupt is not masked.
4	RW	0x0	rx_udf_im 1'b0: Rxfifo underflow interrupt is masked. 1'b1: Rxfifo underflow interrupt is not masked.
3	RW	0x0	rx_ovf_im 1'b0: Rxfifo overflow interrupt is masked. 1'b1: Rxfifo overflow interrupt is not masked.
2	RW	0x0	tx_done_im 1'b0: Transmission finish interrupt is masked. 1'b1: Transmission finish interrupt is not masked.
1	RW	0x0	tx_udf_im 1'b0: Txfifo underflow interrupt is masked. 1'b1: Txfifo underflow interrupt is not masked.
0	RW	0x0	tx_ovf_im 1'b0: Txfifo overflow interrupt is masked. 1'b1: Txfifo overflow interrupt is not masked.

FLEXBUS_RISR

Address: Operational Base(0xFF880000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	dma_timeout_ris 1'b0: DMA timeout interrupt is not active prior to masking. 1'b1: DMA timeout interrupt is active prior to masking.
12	RO	0x0	dma_err_ris 1'b0: DMA error response interrupt is not active prior to masking. 1'b1: DMA error response interrupt is active prior to masking.

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Bit	Attr	Reset Value	Description
11	RO	0x0	dma_dst1_ris 1'b0: DMA write buffer1 interrupt is not active prior to masking. 1'b1: DMA write buffer1 interrupt is active prior to masking.
10	RO	0x0	dma_dst0_ris 1'b0: DMA write buffer0 interrupt is not active prior to masking. 1'b1: DMA write buffer0 interrupt is active prior to masking.
9	RO	0x0	dma_src1_ris 1'b0: DMA read buffer1 interrupt is not active prior to masking. 1'b1: DMA read buffer1 interrupt is active prior to masking.
8	RO	0x0	dma_src0_ris 1'b0: DMA read buffer0 interrupt is not active prior to masking. 1'b1: DMA read buffer0 interrupt is active prior to masking.
7	RO	0x0	dvp_frame_start_ris 1'b0: Frame start interrupt is not active prior to masking. 1'b1: Frame start interrupt is active prior to masking.
6	RO	0x0	dvp_frame_ab_ris 1'b0: Frame abnormal interrupt is not active prior to masking. 1'b1: Frame abnormal interrupt is active prior to masking.
5	RO	0x0	rx_done_ris 1'b0: Receive finish interrupt is not active prior to masking. 1'b1: Receive finish interrupt is active prior to masking.
4	RO	0x0	rx_udf_ris 1'b0: Rxfifo underflow interrupt is not active prior to masking. 1'b1: Rxfifo underflow interrupt is active prior to masking.
3	RO	0x0	rx_ovf_ris 1'b0: Rxfifo overflow interrupt is not active prior to masking. 1'b1: Rxfifo overflow interrupt is active prior to masking.
2	RO	0x0	tx_done_ris 1'b0: Transmission finish interrupt is not active prior to masking. 1'b1: Transmission finish interrupt is active prior to masking.
1	RO	0x0	tx_udf_ris 1'b0: Txfifo underflow interrupt is not active prior to masking. 1'b1: Txfifo underflow interrupt is active prior to masking.
0	RO	0x0	tx_ovf_ris 1'b0: Txfifo overflow interrupt is not active prior to masking. 1'b1: Txfifo overflow interrupt is active prior to masking.

FLEXBUS_ISR

Address: Operational Base(0xFF880000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	dma_timeout_is 1'b0: DMA timeout interrupt is not active after masking. 1'b1: DMA timeout interrupt is active after masking.
12	RO	0x0	dma_err_is 1'b0: DMA error response interrupt is not active after masking. 1'b1: DMA error response interrupt is active after masking.
11	RO	0x0	dma_dst1_is 1'b0: DMA write buffer1 interrupt is not active after masking. 1'b1: DMA write buffer1 interrupt is active after masking.
10	RO	0x0	dma_dst0_is 1'b0: DMA write buffer0 interrupt is not active after masking. 1'b1: DMA write buffer0 interrupt is active after masking.

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Bit	Attr	Reset Value	Description
9	RO	0x0	dma_src1_is 1'b0: DMA read buffer1 interrupt is not active after masking. 1'b1: DMA read buffer1 interrupt is active after masking.
8	RO	0x0	dma_src0_is 1'b0: DMA read buffer0 interrupt is not active after masking. 1'b1: DMA read buffer0 interrupt is active after masking.
7	RO	0x0	dvp_frame_start_is 1'b0: Frame start interrupt is not active after masking. 1'b1: Frame start interrupt is active after masking.
6	RO	0x0	dvp_frame_ab_is 1'b0: Frame abnormal interrupt is not active after masking. 1'b1: Frame abnormal interrupt is active after masking.
5	RO	0x0	rx_done_is 1'b0: Receive finish interrupt is not active after masking. 1'b1: Receive finish interrupt is active after masking.
4	RO	0x0	rx_udf_is 1'b0: Rxfifo underflow interrupt is not active after masking. 1'b1: Rxfifo underflow interrupt is active after masking.
3	RO	0x0	rx_ovf_is 1'b0: Rxfifo overflow interrupt is not active after masking. 1'b1: Rxfifo overflow interrupt is active after masking.
2	RO	0x0	tx_done_is 1'b0: Transmission finish interrupt is not active after masking. 1'b1: Transmission finish interrupt active after masking.
1	RO	0x0	tx_udf_is 1'b0: Txfifo underflow interrupt is not active after masking. 1'b1: Txfifo underflow interrupt is active after masking.
0	RO	0x0	tx_ovf_is 1'b0: Txfifo overflow interrupt is not active after masking. 1'b1: Txfifo overflow interrupt is active after masking.

FLEXBUS_ICR

Address: Operational Base(0xFF880000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	cci Write 1 to Clear Combined Interrupt.
30:14	RO	0x00000	reserved
13	R/W SC	0x0	ctimeout Write 1 to clear DMA timeout interrupt.
12	R/W SC	0x0	cdma_err Write 1 to clear DMA error response interrupt.
11	R/W SC	0x0	cdst1 Write 1 to clear DMA write buffer1 interrupt.
10	R/W SC	0x0	cdst0 Write 1 to clear DMA write buffer0 interrupt.
9	R/W SC	0x0	csrc1 Write 1 to clear DMA read buffer1 interrupt.
8	R/W SC	0x0	csrc0 Write 1 to clear DMA read buffer0 interrupt.
7	R/W SC	0x0	cframe_start Write 1 to clear DVP frame start interrupt.
6	R/W SC	0x0	crx_dvp_frame_ab Write 1 to clear frame abnormal interrupt.
5	R/W SC	0x0	crx_done Write 1 to clear receive finish interrupt.

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Bit	Attr	Reset Value	Description
4	R/W SC	0x0	crx_udf Write 1 to clear rxfifo underflow Interrupt.
3	R/W SC	0x0	crx_ovf Write 1 to clear rxfifo overflow Interrupt.
2	R/W SC	0x0	ctx_done Write 1 to clear transmission finish interrupt.
1	R/W SC	0x0	ctx_udf Write 1 to clear txfifo underflow Interrupt.
0	R/W SC	0x0	ctx_ovf Write 1 to clear txfifo overflow Interrupt.

FLEXBUS_REVISION

Address: Operational Base(0xFF880000) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:16	RO	0x010d	revision [31:24]: Large version number [23:16]: Minor version number
15:0	RO	0x0844	svn SVN revision.

37.5 Interface Description

Table 37-2 Flexbus Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
flexbus0_clk	O	GPIO1_C1	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[7:4]=0x3
flexbus0_csn_m0	O	GPIO1_B0	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[3:0]=0x5
flexbus0_csn_m1	O	GPIO1_B2	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[11:8]=0x5
flexbus0_csn_m2	O	GPIO1_B4	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[3:0]=0x5
flexbus0_csn_m3	O	GPIO1_B6	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[11:8]=0x5
flexbus0_csn_m4	O	GPIO1_C0	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[3:0]=0x5
flexbus0_csn_m5	O	GPIO1_C2	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[11:8]=0x5
flexbus0_d0	I/O	GPIO1_D3	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[15:12]=0x3
flexbus0_d1	I/O	GPIO1_D2	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[11:8]=0x3
flexbus0_d2	I/O	GPIO1_D1	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[7:4]=0x3
flexbus0_d3	I/O	GPIO1_D0	GPIO1_IOC_GPIO1D_IOMUX_SEL_0[3:0]=0x3
flexbus0_d4	I/O	GPIO1_C7	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[15:12]=0x3

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Module Pin	Direction	Pin Name	IOMUX Setting
flexbus0_d5	I/O	GPIO1_C6	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[11:8]=0x3
flexbus0_d6	I/O	GPIO1_C5	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[7:4]=0x3
flexbus0_d7	I/O	GPIO1_C4	GPIO1_IOC_GPIO1C_IOMUX_SEL_1[3:0]=0x3
flexbus0_d8	I/O	GPIO1_C3	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[15:12]=0x3
flexbus0_d9	I/O	GPIO1_C2	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[11:8]=0x3
flexbus0_d10	I/O	GPIO1_B7	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[15:12]=0x4
flexbus0_d11	I/O	GPIO1_B6	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[11:8]=0x4
flexbus0_d12	I/O	GPIO1_B5	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[7:4]=0x4
flexbus0_d13	I/O	GPIO1_B4	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[3:0]=0x4
flexbus0_d14	I/O	GPIO1_B3	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[15:12]=0x4
flexbus0_d15	I/O	GPIO1_B2	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[11:8]=0x4
flexbus1_clk	I/O	GPIO1_C0	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[3:0]=0x3
flexbus1_csn_m0	O	GPIO1_B1	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[7:4]=0x5
flexbus1_csn_m1	O	GPIO1_B3	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[15:12]=0x5
flexbus1_csn_m2	O	GPIO1_B5	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[7:4]=0x5
flexbus1_csn_m3	O	GPIO1_B7	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[15:12]=0x5
flexbus1_csn_m4	O	GPIO1_C1	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[7:4]=0x5
flexbus1_csn_m5	O	GPIO1_C3	GPIO1_IOC_GPIO1C_IOMUX_SEL_0[15:12]=0x5
flexbus1_d0	I	GPIO1_A0	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[3:0]=0x3
flexbus1_d1	I	GPIO1_A1	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[7:4]=0x3
flexbus1_d2	I	GPIO1_A2	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[11:8]=0x3
flexbus1_d3	I	GPIO1_A3	GPIO1_IOC_GPIO1A_IOMUX_SEL_0[15:12]=0x3

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Module Pin	Direction	Pin Name	IOMUX Setting
flexbus1_d4	I	GPIO1_A4	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[3:0]=0x3
flexbus1_d5	I	GPIO1_A5	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[7:4]=0x3
flexbus1_d6	I	GPIO1_A6	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[11:8]=0x3
flexbus1_d7	I	GPIO1_A7	GPIO1_IOC_GPIO1A_IOMUX_SEL_1[15:12]=0x3
flexbus1_d8	I	GPIO1_B0	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[3:0]=0x3
flexbus1_d9	I	GPIO1_B1	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[7:4]=0x3
flexbus1_d10	I	GPIO1_B2	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[11:8]=0x3
flexbus1_d11	I	GPIO1_B3	GPIO1_IOC_GPIO1B_IOMUX_SEL_0[15:12]=0x3
flexbus1_d12	I	GPIO1_B4	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[3:0]=0x3
flexbus1_d13	I	GPIO1_B5	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[7:4]=0x3
flexbus1_d14	I	GPIO1_B6	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[11:8]=0x3
flexbus1_d15	I	GPIO1_B7	GPIO1_IOC_GPIO1B_IOMUX_SEL_1[15:12]=0x3

Notes: I=input, O=output, I/O=input/output, bidirectional.

37.6 Application Notes

Clock Ratios

The frequency of PAD is half of FlexBUS operation clock. When FlexBUS operation clock is 200MHz, the frequency of flexbus0_clk and flexbus1_clk is 100MHz.

FSPI Transfer Flow

If want to support FSPI feature, the configuration is showing as below:

A. Set GRF_SOC_CON1[1]=1 to as master; set modes, transmit then receive, FLEXBUS_COM_CTL[3:0]=4'hf;
B. Set RX CLK dummy counter, FLEXBUS_RXCLK_DUMMY;
C. Set Interrupt mask, FLEXBUS_IMR;
D. Set format of transmit data, FLEXBUS_TX_CTL;
E. Set tx start water line, FLEXBUS_TXWAT_START;
F. Set tx length, FLEXBUS_TX_NUM;
G. Set format of receive data, FLEXBUS_RX_CTL;
H. Set rx length, FLEXBUS_RX_NUM;
I. Set DMA,FLEXBUS_DMA_SRC_ADDR0/DST_ADDR0/SRC_LEN0/DST_LEN0;
J. Set FlexBUS enable, FLEXBUS_ENR[1:0]=2'b11;

Wait Interrupt and clear interrupt;
Final, disable FlexBUS.

ADC with Sync CLKIN Transfer Flow

A. Set GRF_SOC_CON1[1] based on ADC interface timing and set GRF_SOC_CON1[1]=0 to

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as slave;
B. Set modes, rx only mode, FLEXBUS_COM_CTL[3:0]=4'h2;
C. Set Interrupt mask, FLEXBUS_IMR;
D. Set format of receive data, FLEXBUS_RX_CTL[4]=1, data frame configuration according to actual usage;
E. Set FLEXBUS_SLAVE_MODE=2'b01;
F. Set DMA;
G. Set FlexBUS enable, FLEXBUS_ENR[1]=1'b1;
H. Wait interrupt, if dma_dst0 is active indicating that buffer0 has finished and clear interrupt, FlexBUS can set new buffer0 address. FlexBUS will automatically jump to buffer1 address and capture new data; If don't want to receive data, set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
I. Wait interrupt, if dma_dst1 is active indicating that buffer1 has finished and clear interrupt, FlexBUS can set new buffer1 address. FlexBUS will automatically jump to buffer0 address and capture new data; If don't want to receive new data, Set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
J. If want to stop receiving data , set FlexBUS.STOP[1]=1 at any time and wait rx_done interrupt; final disable FlexBUS;
K. If want to continue to receive data, repeat H-I.

ADC without CLKIN Transfer Flow
A. Set GRF_SOC_CON1[1]=1;
B. Set modes, rx only mode, FLEXBUS_COM_CTL[3:0]=4'h2;
C. Set Interrupt mask, FLEXBUS_IMR;
D. Set format of receive data, FLEXBUS_RX_CTL[4]=1, data frame configuration according to actual usage;
E. Set DMA;
F. Set FlexBUS enable, FLEXBUS_ENR[1]=1'b1;
G. Wait interrupt, if dma_dst0 is active indicating that buffer0 has finished and clear interrupt, FlexBUS can set new buffer0 address. FlexBUS will automatically jump to buffer1 address and capture new data; If don't want to receive data, set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
H. Wait interrupt, if dma_dst1 is active indicating that buffer1 has finished and clear interrupt, FlexBUS can set new buffer1 address. FlexBUS will automatically jump to buffer0 address and capture new data; If don't want to receive new data, Set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
I. If want to stop receiving data , set FlexBUS.STOP[1]=1 at any time and wait rx_done interrupt; final disable FlexBUS;
J. If want to continue to receive data, repeat G-H-I.

DAC Transfer Flow
If want to support DAC feature, the configuration is showing as below:
A. Set modes, tx only, FLEXBUS_COM_CTL[3:0]=4'h1;
B. Set Interrupt mask, FLEXBUS_IMR;
C. Set format of transmit data, FLEXBUS_TX_CTL and continue_mode =1;
D. Set tx start water line, FLEXBUS_TXWAT_START;
E. Set DMA;
F. Set FlexBUS enable, FLEXBUS_ENR[1:0]=2'b01;
G. Wait interrupt, if dma_src0 is active indicating that buffer0 has finished and clear interrupt, FlexBUS can set new buffer0 address. FlexBUS will automatically jump to buffer1 address and send new data; If don't want to send data, set FLEXBUS_STOP[0]=1, and then disable FlexBUS;
H. Wait interrupt, if dma_src1 is active indicating that buffer1 has finished and clear interrupt, FlexBUS can set new buffer1 address. FlexBUS will automatically jump to buffer0 address and send new data; If don't want to send new data, Set FLEXBUS_STOP[0]=1, and then disable FlexBUS;
I. If want to stop sending data , set FlexBUS.STOP[0]=1 at any time and wait tx_done

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interrupt; final disable FlexBUS;
J. If want to continue to receive data, repeat G-H-I.

DVP Mode Transfer Flow
A. Set GRF_SOC_CON1[1] based on cif interface timing and set GRF_SOC_CON1[1]=0 to as slave;
B. Set modes, rx only mode, FLEXBUS_COM_CTL[3:0]=4'h2;
C. Set Interrupt mask, FLEXBUS_IMR;
D. Set format of receive data, FLEXBUS_RX_CTL.rx_data_width=2 and rx_continue_mode=1;
E. Set FLEXBUS_SLAVE_MODE=2'b11;
F. Set FLEXBUS_DVP_CROP_SIZE, if want to support cropping function, need to Set FLEXBUS_DVP_CROP_START.
G. Set FLEXBUS_DVP_POL based on CIF interface of VSYNC and HREF;
H. Set FLEXBUS_DVP_ORDER and DMA, FLEXBUS_DMA_DST_ADD0/1, used to ping-pang operation;
I. Set FlexBUS enable, FLEXBUS_ENR[1]=1'b1;
J. Wait interrupt, if dma_dst0 is active indicating that a frame has finished and clear interrupt, FlexBUS can set new buffer0 address. FlexBUS will automatically jump to buffer1 address and capture new frame; If dvp_frame_ab is active, need to clear interrupt and FlexBUS will automatically continue to capture the next frame using buffer0 address; If don't want to receive new frame, Set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
K. Wait interrupt, if dma_dst1 is active indicating that a frame has finished and clear interrupt, FlexBUS can set new buffer1 address. FlexBUS will automatically jump to buffer0 address and capture new frame; If dvp_frame_ab is active, need to clear interrupt and FlexBUS will automatically continue to capture the next frame using buffer1 address; If don't want to receive new frame, Set FLEXBUS_STOP[1]=1, and then disable FlexBUS;
L. If want to receive new frame pixel, repeat J-K.

QSPI Transfer Flow
If want to support QSPI feature, the configuration is showing as below:
A. Set modes, tx only, FLEXBUS_COM_CTL[3:0]=4'h1;
B. Set Interrupt mask, FLEXBUS_IMR;
C. Set format of transmit data, FLEXBUS_TX_CTL.mult_line =1;
D. Set tx start water line, FLEXBUS_TXWAT_START;
E. Set the length of data and command, FLEXBUS_TX_NUM, FLEXBUS_TX_CMD0/1, FLEXBUS_TX_CMD_WIDTH, FLEXBUS_TX_CSN_DUMMY, FLEXBUS_TX_WIDTH;
F. Set DMA configuration;
G. Set FlexBUS enable, FLEXBUS_ENR[0]=1'b1;
H. Wait tx_done interrupt and clear interrupt, disable FlexBUS.

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Chapter 38 MAC Ethernet Interface (MAC)

38.1 Overview

The Ethernet Quality-of-Service controller (EQOS is commonly referred to as MAC in this document) provides a complete Ethernet interface from processor to a Reduced Media Independent Interface (RMII) compliant Ethernet PHY. The MAC includes a DMA controller. The DMA controller efficiently moves packet data from microprocessor's RAM, formats the data for an IEEE 802.3-2002 compliant packet and transmits the data to an Ethernet Physical Interface (PHY). It also efficiently moves packet data from RXFIFO to microprocessor's RAM.
The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.

38.1.1 MAC Features

38.1.1.1 MAC Tx and Rx Common Features

- Supports 10/100-Mbps data transfer rates with the RMII interfaces
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using back-pressure support (based on implementation-specific white papers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
- 64-bit data transfer interface on the application side
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- network statistics with RMON or MIB Counters (RFC2819/RFC2665)
- Media clock generation and recovery
- MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

38.1.1.2 MAC Tx Features

- Preamble and start of packet data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-packet basis
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flow control input transitions from assertion to de-assertion (in full-duplex mode)
- Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
- Insertion, replacement, or deletion of up to two VLAN tags
- Frame Preemption for MAC Tx

38.1.1.3 MAC Rx Features

- Automatic Pad and CRC Stripping options
- Option to disable Automatic CRC checking
- Preamble and SFD deletion
- Separate 112-bit or 128-bit status
- Programmable watchdog timeout limit
- Flexible address filtering modes:
  - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
  - Up to 96 additional 48-bit perfect (DA) address filters that can be selected in blocks of 32 and 64 registers
  - Up to 31 48-bit SA address comparison check with masks for each byte
  - 32 bit, 64 bit, 128 bit, or 256 bit Hash filter (optional) for multicast and unicast (DA) addresses
  - Option to pass all multi-cast addressed packets
  - Promiscuous mode to pass all packets without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report

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- Additional packet filtering:
  - VLAN tag-based: Perfect match and Hash-based (optional) filtering. Filtering based on either outer or inner VLAN tag is possible
  - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
  - Extended VLAN tag based filtering 4, 8, 16, or 32 filter selection
- IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- Optional module to detect remote wake-up packets and AMD magic packets
- Optional forwarding of received Pause packets to the application (in full-duplex mode)
- Frame Preemption for MAC Rx

38.1.2 MTL Features

38.1.2.1 MTL Tx and Rx Common Features

- 32-bit, 64-bit, or 128-bit Transaction Layer block (bridges the application and the MAC)
- Data transfers executed using simple FIFO protocol
- Synchronization for all clocks in the design (Transmit, Receive, and Application clocks)
- Optimization for packet-oriented transfers with packets delimiters
- Option to have dual-port RAM based asynchronous FIFO controllers or Single-port RAM based synchronous FIFO controllers
- RAM memory instantiation outside the top-level module to facilitate memory testing or instantiation
- Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size, to support burst data transfer in the EQOS-MTL configuration
- Programmable threshold capability for each queue (default of 64 bytes)
- Optional Debug and slave mode operation on Queue 0 (default queue)

38.1.2.2 MTL Tx Features

- TX FIFO sizes on transmission is 4 KB
- Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- Programmable queue size in configurations with multiple queues. Each queue size can be programmed in terms of 256 bytes
- Automatic re-transmission of collision packets in half-duplex mode
- Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- Disabling of Data Memory RAM chip-select when inactive to reduce power consumption
- Optional module to calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksum
- Programmable interrupt options for different operational conditions
- Statistics by generating pulses for packets dropped (because of underflow) in the Tx FIFO
- Optional packet-level control for
  - VLAN tag insertion or replacement
  - Ethernet source address insertion
  - Layer3/Layer4 Checksum insertion control
  - Timestamp control
  - CRC and pad control

38.1.2.3 MTL Rx Features

- Rx queue sizes in the Receive path is 8 KB
- Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in Store-and-Forward mode) in EQOS-MTL configuration
- Programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- Option to filter all error packets on reception and not forward them to the application in the store-and-forward mode
- Option to forward the undersized good packets
- Statistics by generating pulses for packets dropped (because of overflow) in the Rx

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FIFO

- Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level
- Arbitration among queues when multiple queues are present. The following arbitration schemes are supported:
  - Weighted Round Robin (WRR)
  - Weighted Strict priority (WSP)
  - Strict Priority (SP)
- Option to replicate received multicast packets for transfer by multiple Rx DMA channels
- Option to have a programmable lookup table based flexible Parser for filtering and steering the Rx packets

38.1.3 DMA Block Features

- 64-bit data transfers
- Separate DMA channel in the Transmit path for each queue in MTL
- Single or multiple DMA channels for any number of queues in MTL Receive path
- Fully synchronous design operating on a single application clock (except for CSR module, when a separate CSR clock is configured)
- Optimization for packet-oriented DMA transfers with packet delimiters
- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) descriptor support
- Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-packet Transmit or Receive Complete Interrupt control
- Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- Start and Stop modes
- Separate ports for host CSR access and host data interface
- support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO)
- Selectable number of Tx DMA channels with TSO/USO feature enabled
- Routing of received packets to the DMA channels based on the DA or VLAN Priority in multi-channel DMA configurations
- Option to split the packet header (Layer 3 and Layer 4) and payload in a different buffers
- Programmable control for Transmit Descriptor posted writes to improve the throughput
- Sideband signals to control starting and stopping of DMA channels

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38.2 Block Diagram

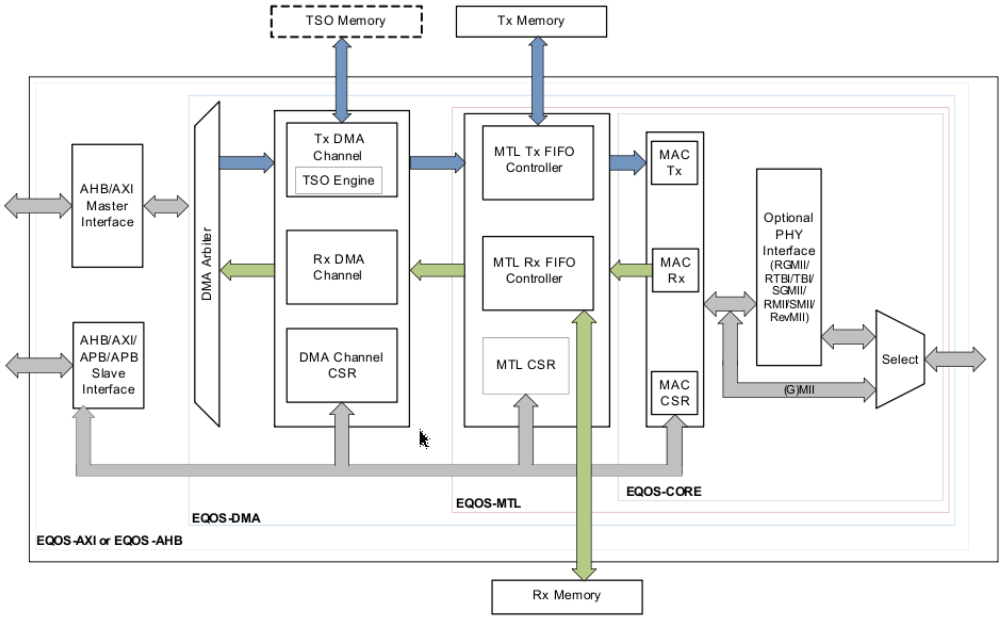

Fig. 38-1 MAC Block Diagram

The MAC is broken up into multiple separate functional units. These blocks are interconnected in the MAC module. The block diagram shows the general flow of data and control signals between these blocks.
The MAC transfers data to system memory through the AXI master interface. The host CPU uses the APB Slave interface to access the MAC subsystem's control and status registers (CSRs).
The MAC only supports the PHY interfaces of reduced MII (RMII).
The Transmit FIFO (Tx FIFO) buffers data read from system memory by the DMA before transmission by the MAC Core. Similarly, the Receive FIFO (Rx FIFO) stores the Ethernet frames received from the line until they are transferred to system memory by the DMA. These are asynchronous FIFOs, as they also transfer the data between the application clock and the MAC line clocks.

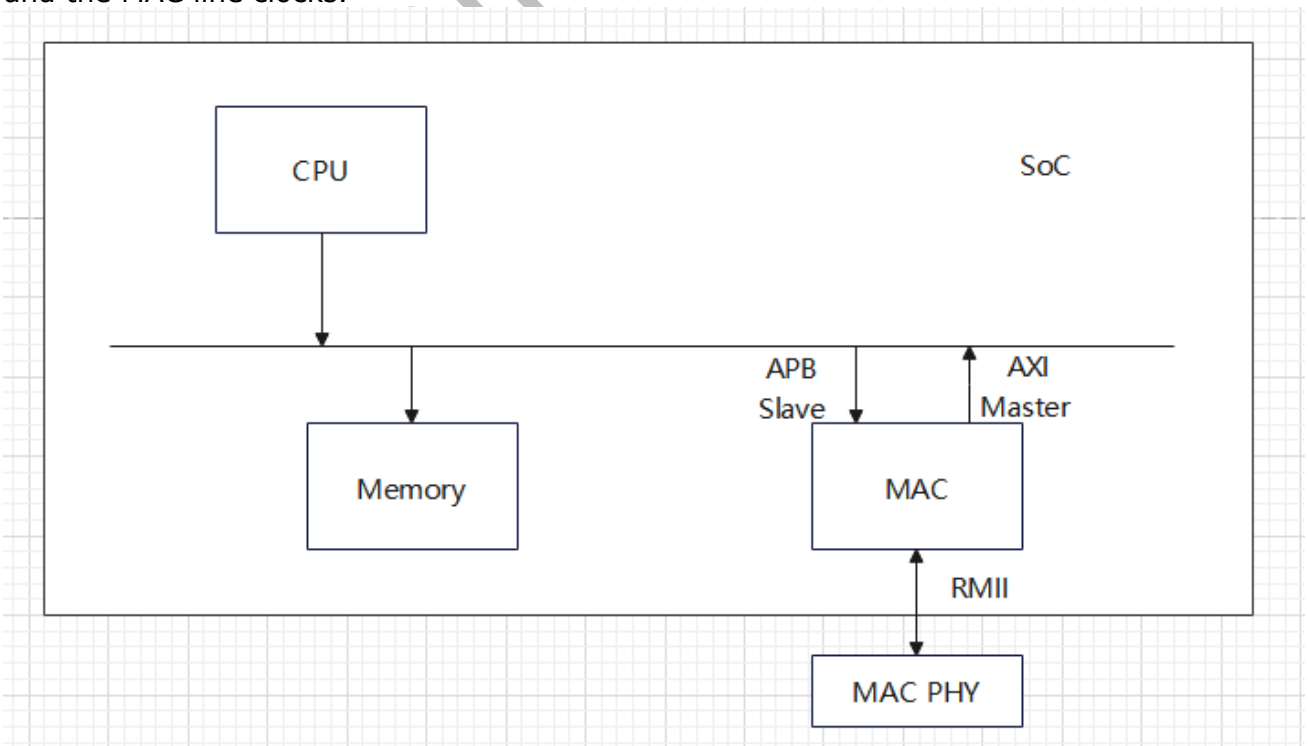

Fig. 38-2 MAC in SOC

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MAC Supports 10/100-Mbps data transfer rates with the RMII interfaces.

38.3 Function Description

38.3.1 Frame Structure

Data frames transmitted shall have the frame format shown in figure below.

Fig. 38-3 Frame Format

The preamble <preamble> begins a frame transmission. The bit value of the preamble field consists of 7 octets with the following bit values:
10101010 10101010 10101010 10101010 10101010 10101010 10101010
The SFD (start frame delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value is 10101011.The data in a well formed frame shall consist of N octet's data.

38.3.1.1 RMII Interface timing diagram

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. In devices incorporating multiple MAC or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port - a 62.5% decrease in pin count.
The RMII module is instantiated between the MAC and the PHY. This helps translation of the MAC's MII into the RMII. The RMII block has the following characteristics:
Supports 10-Mbps and 100-Mbps operating rates. It does not support 1000-Mbps operation. Two clock references are sourced externally or CRU, providing independent, 2-bit wide transmit and receive paths.

38.3.1.2 Transmit Bit Ordering

Each nibble from the MII must be transmitted on the RMII a di-bit at a time with the order of di-bit transmission shown in Fig.1-4. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

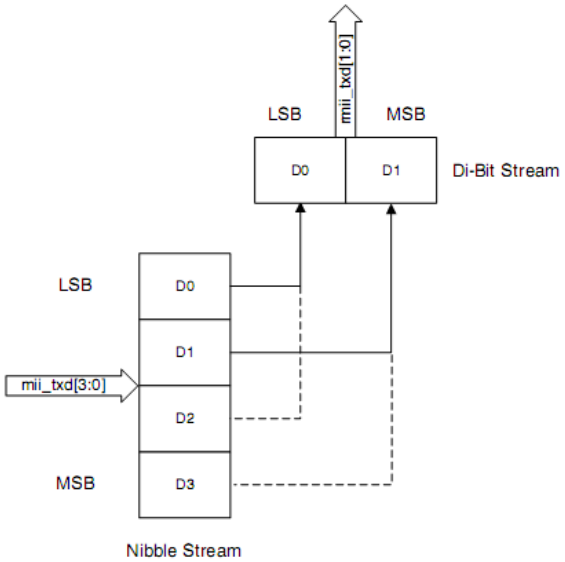

Fig. 38-4 RMII Transmission Bit Ordering

38.3.1.3 RMII Transmit Timing Diagrams

The follow figures show MII-to-RMII transaction timing. The clk_rmii_i (REF_CLK) frequency is 50MHz in RMII interface. In 10Mb/s mode, as the REF_CLK frequency is 10 times as the data rate, the value on rmii_txd_o[1:0] (TXD[1:0]) shall be valid such that TXD[1:0] may be sampled every 10th cycle, regard-less of the starting cycle within the

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group and yield the correct frame data.

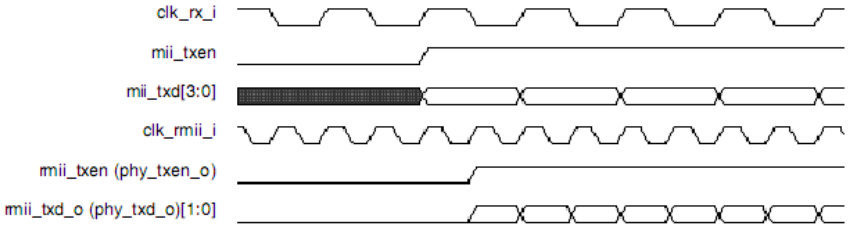

Fig. 38-5 Start of MII and RMII Transmission in 100-Mbps Mode

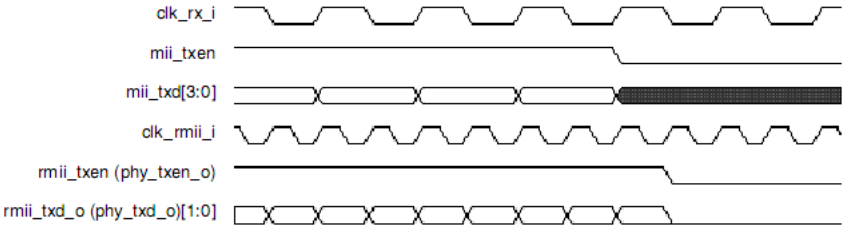

Fig. 38-6 End of MII and RMII Transmission in 100-Mbps Mode

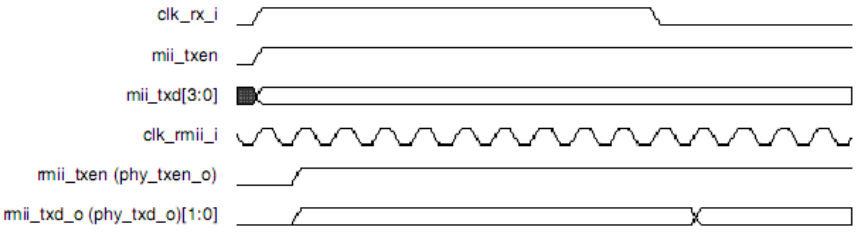

Fig. 38-7 Start of MII and RMII Transmission in 10-Mbps Mode

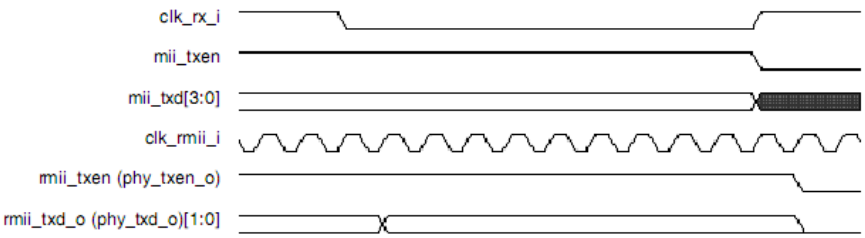

Fig. 38-8 End of MII and RMII Transmission in 10-Mbps Mode

38.3.1.4 Receive Bit Ordering

Each nibble is transmitted to the MII from the di-bit received from the RMII in the nibble transmission order shown in figure below. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

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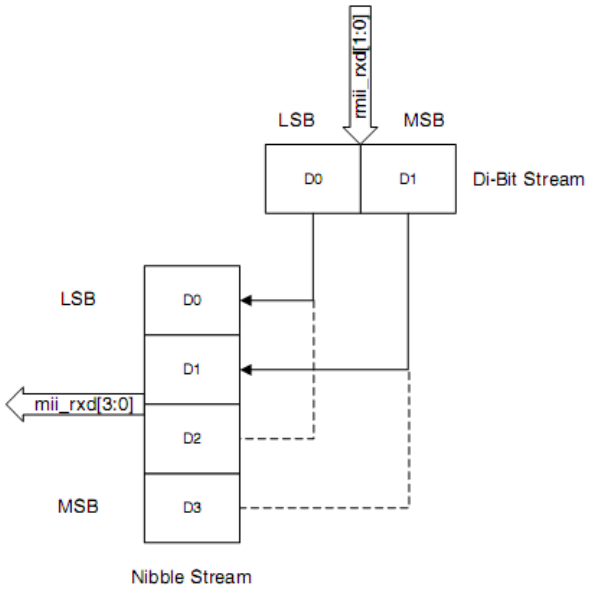

Fig. 38-9 RMII Receive Bit Ordering

38.3.2 Station Management Agent

The application can access the PHY registers through the Station Management Agent (SMA) module. SMA is a two-wire Station Management interface (MIM).

For MIM accesses, the maximum operating frequency of the MDC (gmii_mdc_o) is 2.5 MHz, as specified in the IEEE 802.3. In the MAC core, the gmii_mdc_o clock is derived from the application clock or clk_csr_i, using a divider-counter. The divide factor depends on the clock range setting (CR field) in the MAC_MDIO_Address register Select the clock divide factor as mentioned in the description of CR field of MAC_MDIO_Address register, to meet IEEE specifications. However, if your system supports higher clock frequencies on the MIM interface, there is a provision to select a different divider.

The MDIO frame structure is as follows:

Table 38-1 MDIO Clause 45 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b00
OPCODE	■ 2'b00 ■ 2'b01 ■ 2'b10 ■ 2'b11
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address select for one of 32 devices
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	16-bit value: For an address cycle (OPCODE = 2'b00), this frame contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, this field contains the data to be written to the register. For read or post-read increment address frames, this field contains the contents of the register read from the PHY. ■ In address and data write cycles, the MAC drives the MDIO line during the transfer of these 16 bits. ■ In read and post-read increment address cycles, the PHY drives the MDIO line during the transfer of these 16 bits.

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The frame structure for Clause 22 frames is also supported. The C45E bit in the MAC_MDIO_Address register can be programmed to enable Clause 22 or Clause 45 mode of operation. Table.1-2 shows the Clause 22 frame format.

Table 38-2 MDIO Clause 22 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b01
OPCODE	■ 2'b01 : Write ■ 2'b10 : Read
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address to select the register within each MMD
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	Any 16-bit value: ■ In a write operation, the MAC drives MDIO ■ In read operation, the PHY drives MDIO

In addition to normal read and write operations, the SMA also supports post-read increment address while operating in Clause 45 mode.

38.3.3 TCP/IP Segmentation Offload (TSO) Engine

The TCP Segmentation Offload (TSO) engine is useful in offloading the TCP segmentation functions to the hardware.

It also supports UDP Segmentation Offload (USO) in which the UDP payload is segmented in the hardware. There are no sequencing/ordering controls available or updated in the segments, so it can be used in point to point applications in which out of order packets are not expected by the receiver. The description and flow of TSO mentioned in this section is same as USO, any deviation is provided as notes.

In the TCP segmentation offload (TSO) feature, the DMA splits a large TCP packet into multiple small packets and passes these packets to the MTL Tx Queue.

38.3.4 MAC Management Counters

The MAC supports storing the statistics about the received and transmitted packets in registers that are accessible through the application.

The counters in the MAC Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted packets. The register set includes a control register for controlling the behavior of the registers, two status registers containing interrupts generated (receive and transmit), and Interrupt Enable registers (receive and transmit). These registers are accessible from the Application through the MAC Control Interface (MCI). Each register is 32-bits wide. The write data is qualified with the corresponding mci_be_i signals. Therefore, non-32-bit accesses are allowed as long as the address is word-aligned. The MMCs are accessed using transactions, in the same way the CSR address space is accessed.

The MMC counters are free running. There is no separate enable for the counters to start. If a particular MMC counter is present in the RTL, it starts counting when corresponding packet is received or transmitted. The Receive MMC counters are updated for packets that are passed by the Address Filter (AFM) block. The statistics of packets, dropped by the AFM module, are not updated unless they are runt packets of less than 6 bytes (DA bytes are not received fully). To get statistics of all packets, set Bit 0 in the "MAC_Packet_Filter" register.

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The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet packets.

38.4 Register Description

38.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
MAC0	0xFF4C8000
MAC1	0xFF4D0000

38.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GMAC_MAC_CONFIGURATION	0x0000	W	0x00008000	The MAC Configuration Register establishes the operating mode of the MAC
GMAC_MAC_EXT_CONFIGURATION	0x0004	W	0x00000000	The MAC Extended Configuration Register establishes the operating mode of the MAC
GMAC_MAC_PACKET_FILTER	0x0008	W	0x00000000	The MAC Packet Filter Register contains the filter controls for receiving packets
GMAC_MAC_WATCHDOG_TIMEOUT	0x000C	W	0x00000000	The Watchdog Timeout Register controls the watchdog timeout for received packets
GMAC_MAC_HASH_TABLE_REG0	0x0010	W	0x00000000	The Hash Table Register 0 contains the first 32 bits of the hash table
GMAC_MAC_HASH_TABLE_REG1	0x0014	W	0x00000000	The Hash Table Register 1 contains the second 32 bits of the hash table
GMAC_MAC_VLAN_TAG	0x0050	W	0x00000000	The VLAN Tag Register identifies the IEEE 802.1Q VLAN type packets
GMAC_MAC_VLAN_HASH_TABLE	0x0058	W	0x00000000	When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag
GMAC_MAC_Q0_TX_FLOW_CTRL	0x0070	W	0x00000000	The Flow Control Register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC
GMAC_MAC_RX_FLOW_CTRL	0x0090	W	0x00000000	The Receive Flow Control Register controls the pausing of MAC Transmit based on the received Pause packet
GMAC_MAC_INTERRUPT_STATUS	0x00B0	W	0x00000000	The Interrupt Status Register contains the status of interrupts
GMAC_MAC_INTERRUPT_ENABLE	0x00B4	W	0x00000000	The Interrupt Enable Register contains the masks for generating the interrupts

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_RX_TX_STATUS	0x00B8	W	0x00000000	The Receive Transmit Status Register contains the Receive and Transmit Error status
GMAC_MAC_PMT_CONTROL_STATUS	0x00C0	W	0x00000000	The PMT Control and Status Register
GMAC_MAC_RWK_PACKET_FILTER	0x00C4	W	0x00000000	The Remote Wakeup Filter Registers are implemented as 8, 16, or 32 indirect access registers (wkuppktfilter_reg#i) based on whether 4, 8, or 16 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC_RWK_Packet_Filter register
GMAC_RWK_FILTER0_BYTE_MASK	0x00C4	W	0x00000000	RWK Filter0 Byte Mask
GMAC_RWK_FILTER1_BYTE_MASK	0x00C4	W	0x00000000	RWK Filter1 Byte Mask
GMAC_RWK_FILTER2_BYTE_MASK	0x00C4	W	0x00000000	RWK Filter2 Byte Mask
GMAC_RWK_FILTER3_BYTE_MASK	0x00C4	W	0x00000000	RWK Filter3 Byte Mask
GMAC_RWK_FILTER01_CRC	0x00C4	W	0x00000000	RWK Filter 0/1 CRC-16
GMAC_RWK_FILTER23_CRC	0x00C4	W	0x00000000	RWK Filter 2/3 CRC-16
GMAC_RWK_FILTER_OFFSET	0x00C4	W	0x00000000	RWK Filter Offset
GMAC_RWK_FILTER_COMMAND	0x00C4	W	0x00000000	RWK Filter Command
GMAC_MAC_VERSION	0x0110	W	0x00003051	The Version Register identifies the version of the DWC_ether_qos
GMAC_MAC_DEBUG	0x0114	W	0x00000000	The Debug Register provides the debug status of various MAC blocks
GMAC_MAC_HW_FEATURE0	0x011C	W	0x400113E1	This register indicates the presence of first set of the optional features or functions
GMAC_MAC_HW_FEATURE1	0x0120	W	0x010E4166	This register indicates the presence of second set of the optional features or functions
GMAC_MAC_HW_FEATURE2	0x0124	W	0x11000000	This register indicates the presence of third set of the optional features or functions
GMAC_MAC_HW_FEATURE3	0x0128	W	0x00000000	This register indicates the presence of fourth set the optional features or functions
GMAC_MAC_MDIO_ADDRESS	0x0200	W	0x00000000	The MDIO Address Register controls the management cycles to external PHY through a management interface

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_MDIO_DATA	0x0204	W	0x00000000	The MDIO Data Register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address
GMAC_MAC_ARP_ADDRESS	0x0210	W	0x00000000	The ARP Address Register contains the IPv4 Destination Address of the MAC
GMAC_MAC_CSR_SW_CTRL	0x0230	W	0x00000000	This register contains SW programmable controls for changing the CSR access response and status bits clearing
GMAC_MAC_EXT_CFG1	0x0238	W	0x00000002	This register contains Split mode control field and offset field for Split Header feature
GMAC_MAC_ADDRESS0_HIGH	0x0300	W	0x0000FFFF	The MAC Address0 High Register holds the upper 16 bits of the first 6-byte MAC address of the station
GMAC_MAC_ADDRESS0_LOW	0x0304	W	0xFFFFFFFF	The MAC Address0 Low Register holds the lower 32 bits of the 6-byte first MAC address of the station
GMAC_MMC_CONTROL	0x0700	W	0x00000000	This register establishes the operating mode of MMC
GMAC_MMC_RX_INTERRUPT	0x0704	W	0x00000000	This register maintains the interrupts generated from all Receive statistics counters
GMAC_MMC_TX_INTERRUPT	0x0708	W	0x00000000	This register maintains the interrupts generated from all Transmit statistics counters
GMAC_MMC_RX_INTERRUPT_MASK	0x070C	W	0x00000000	This register maintains the masks for interrupts generated from all Receive statistics counters
GMAC_MMC_TX_INTERRUPT_MASK	0x0710	W	0x00000000	This register maintains the masks for interrupts generated from all Transmit statistics counters
GMAC_TX_OCTET_COUNT_GOOD_BAD	0x0714	W	0x00000000	This register provides the number of bytes transmitted by the DWC_ether_qos, exclusive of preamble and retried bytes, in good and bad packets
GMAC_TX_PACKET_COUNT_GOOD_BAD	0x0718	W	0x00000000	This register provides the number of good and bad packets, exclusive of retried packets
GMAC_TX_UNDERFLOW_ERROR_PACKETS	0x0748	W	0x00000000	This register provides the number of packets aborted because of packets underflow error
GMAC_TX_CARRIER_ERROR_PACKETS	0x0760	W	0x00000000	This register provides the number of packets aborted because of carrier sense error (no carrier or loss of carrier)
GMAC_TX_OCTET_COUNT_GOOD	0x0764	W	0x00000000	This register provides the number of bytes exclusive of preamble, only in good packets

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Name	Offset	Size	Reset Value	Description
GMAC_TX_PACKET_COUNT_GOOD	0x0768	W	0x00000000	This register provides the number of good packets transmitted by DWC_ether_qos
GMAC_TX_PAUSE_PACKETS	0x0770	W	0x00000000	This register provides the number of good Pause packets by DWC_ether_qos
GMAC_RX_PACKETS_COUNT_GOOD_BAD	0x0780	W	0x00000000	This register provides the number of good and bad packets received by DWC_ether_qos
GMAC_RX_OCTET_COUNT_GOOD_BAD	0x0784	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, in good and bad packets
GMAC_RX_OCTET_COUNT_GOOD	0x0788	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, only in good packets
GMAC_RX_MULTICAST_PACKETS_GOOD	0x0790	W	0x00000000	This register provides the number of good multicast packets received by DWC_ether_qos
GMAC_RX_CRC_ERROR_PACKETS	0x0794	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with CRC error
GMAC_RX_LENGTH_ERROR_PACKETS	0x07C8	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with length error (Length Type field not equal to packet size), for all packets with valid length field
GMAC_RX_PAUSE_PACKETS	0x07D0	W	0x00000000	This register provides the number of good and valid Pause packets received by DWC_ether_qos
GMAC_RX_FIFO_OVERFLOW_PACKETS	0x07D4	W	0x00000000	This register provides the number of missed received packets because of FIFO overflow
GMAC_MMC_IPC_RX_INTERRUPT_MASK	0x0800	W	0x00000000	This register maintains the mask for the interrupt generated from the receive IPC statistic counters
GMAC_MMC_IPC_RX_INTERRUPT	0x0808	W	0x00000000	This register maintains the interrupt that the receive IPC statistic counters generate
GMAC_RXIPV4_GOOD_PACKETS	0x0810	W	0x00000000	This register provides the number of good IPv4 datagrams received by DWC_ether_qos with the TCP, UDP, or ICMP payload
GMAC_RXIPV4_HEADER_ERROR_PACKETS	0x0814	W	0x00000000	This register provides the number of IPv4 datagrams received by DWC_ether_qos with header (checksum, length, or version mismatch) errors
GMAC_RXIPV6_GOOD_PACKETS	0x0824	W	0x00000000	This register provides the number of good IPv6 datagrams received by DWC_ether_qos

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Name	Offset	Size	Reset Value	Description
GMAC_RXIPV6_HEADER_ERROR_PACKETS	0x0828	W	0x00000000	This register provides the number of IPv6 datagrams received by DWC_ether_qos with header (length or version mismatch) errors
GMAC_RXUDP_ERROR_PACKETS	0x0834	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose UDP payload has a checksum error
GMAC_RXTCP_ERROR_PACKETS	0x083C	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose TCP payload has a checksum error
GMAC_RXICMP_ERROR_PACKETS	0x0844	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose ICMP payload has a checksum error
GMAC_RXIPV4_HEADER_ERROR_OCTETS	0x0854	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv4 datagrams with header errors (checksum, length, version mismatch)
GMAC_RXIPV6_HEADER_ERROR_OCTETS	0x0868	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv6 datagrams with header errors (length, version mismatch)
GMAC_RXUDP_ERROR_OCTETS	0x0874	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a UDP segment that had checksum errors
GMAC_RXTCP_ERROR_OCTETS	0x087C	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a TCP segment that had checksum errors
GMAC_RXICMP_ERROR_OCTETS	0x0884	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a good ICMP segment
GMAC_MAC_TIMESTAMP_CONTROL	0x0B00	W	0x00000000	This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver
GMAC_MAC_SUB_SECOND_INCREMENT	0x0B04	W	0x00000000	This register specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock
GMAC_MAC_SYSTEM_TIME_SECS	0x0B08	W	0x00000000	The System Time Nanoseconds Register, along with System Time Seconds Register, indicates the current value of the system time maintained by the MAC

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_SYSTEM_TIME_NS	0x0B0C	W	0x00000000	The System Time Nanoseconds Register, along with System Time Seconds Register, indicates the current value of the system time maintained by the MAC
GMAC_MAC_SYS_TIME_SECS_UPDATE	0x0B10	W	0x00000000	The System Time Seconds Update Register, along with the System Time Nanoseconds Update Register, initializes or updates the system time maintained by the MAC
GMAC_MAC_SYS_TIME_NS_UPDATE	0x0B14	W	0x00000000	MAC System Time Nanoseconds Update Register
GMAC_MAC_TIMESTAMP_ADDEND	0x0B18	W	0x00000000	Timestamp Addend Register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register)
GMAC_MAC_TIMESTAMP_STATUS	0x0B20	W	0x00000000	Timestamp Status Register. All bits except Bits[27:25] gets cleared when the application reads this register
GMAC_MAC_TX_TS_STATUS_NS	0x0B30	W	0x00000000	This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled
GMAC_MAC_TX_TS_STATUS_SECS	0x0B34	W	0x00000000	The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted
GMAC_MAC_AUXILIARY_CONTROL	0x0B40	W	0x00000000	The Auxiliary Timestamp Control Register controls the Auxiliary Timestamp snapshot
GMAC_MAC_AUXILIARY_TS_NS	0x0B48	W	0x00000000	The Auxiliary Timestamp Nanoseconds Register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot
GMAC_MAC_AUXILIARY_TS_SECS	0x0B4C	W	0x00000000	The Auxiliary Timestamp Seconds Register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register
GMAC_MAC_TS_INGRESS_CORR_NS	0x0B58	W	0x00000000	This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path
GMAC_MAC_TS_EGRESS_CORR_NS	0x0B5C	W	0x00000000	This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path
GMAC_MAC_TS_INGRESS_LATENCY	0x0B68	W	0x00000000	This register holds the Ingress MAC latency

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_TS_EGRESS_LATENCY	0x0B6C	W	0x00000000	This register holds the Egress MAC latency
GMAC_MAC_PPS_CONTROL	0x0B70	W	0x00000000	PPS Control Register
GMAC_MAC_PPS0_TARGET_TIME_SECONDS	0x0B80	W	0x00000000	The PPS Target Time Seconds Register, along with PPS Target Time Nanoseconds Register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers
GMAC_MAC_PPS0_TARGET_TIME_NS	0x0B84	W	0x00000000	PPS0 Target Time Nanoseconds Register
GMAC_MAC_PPS0_INTERVAL	0x0B88	W	0x00000000	The PPS0 Interval Register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0])
GMAC_MAC_PPS0_WIDTH	0x0B8C	W	0x00000000	The PPS0 Width Register contains the number of units of sub-second increment value
GMAC_MTL_OPERATION_MODE	0x0C00	W	0x00000000	The Operation Mode Register establishes the Transmit and Receive operating modes and commands
GMAC_MTL_DBG_CTL	0x0C08	W	0x00000000	The FIFO Debug Access Control and Status Register controls the operation mode of FIFO debug access
GMAC_MTL_DBG_STS	0x0C0C	W	0x01000000	The FIFO Debug Status Register contains the status of FIFO debug access
GMAC_MTL_FIFO_DEBUG_DATA	0x0C10	W	0x00000000	The FIFO Debug Data Register contains the data to be written to or read from the FIFOs
GMAC_MTL_INTERRUPT_STATUS	0x0C20	W	0x00000000	The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC
GMAC_MTL_TXQ0_OPERATION_MODE	0x0D00	W	0x00000000	The Queue 0 Transmit Operation Mode Register establishes the Transmit queue operating modes and commands
GMAC_MTL_TXQ0_UNDERFLOW	0x0D04	W	0x00000000	The Queue 0 Underflow Counter Register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

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Name	Offset	Size	Reset Value	Description
GMAC_MTL_TXQ0_DEBUG	0x0D08	W	0x00000000	The Queue 0 Transmit Debug Register gives the debug status of various blocks related to the Transmit queue
GMAC_MTL_Q0_INTERRUPT_CTRL_STATUS	0x0D2C	W	0x00000000	This register contains the interrupt enable and status bits for the queue 0 interrupts
GMAC_MTL_RXQ0_OPERATION_MODE	0x0D30	W	0x00000000	The Queue 0 Receive Operation Mode Register establishes the Receive queue operating modes and command
GMAC_MTL_RXQ0_MISS_PKT_OVF_CNT	0x0D34	W	0x00000000	The Queue 0 Missed Packet and Overflow Counter Register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow
GMAC_MTL_RXQ0_DEBUG	0x0D38	W	0x00000000	The Queue 0 Receive Debug Register gives the debug status of various blocks related to the Receive queue
GMAC_DMA_MODE	0x1000	W	0x00000000	The Bus Mode Register establishes the bus operating modes for the DMA
GMAC_DMA_SYSBUS_MODE	0x1004	W	0x00010000	The System Bus mode Register controls the behavior of the AHB or AXI master
GMAC_DMA_INTERRUPT_STATUS	0x1008	W	0x00000000	The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC
GMAC_DMA_DEBUG_STATUS0	0x100C	W	0x00000000	The Debug Status 0 Register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose
GMAC_AXI_LPI_ENTRY_INTERVAL	0x1040	W	0x00000000	This register is used to control the AXI LPI entry interval
GMAC_DMA_CH0_CONTROL	0x1100	W	0x00000000	The register specifies the MSS value for segmentation, length to skip between two descriptors, and 8xPBL mode
GMAC_DMA_CH0_TX_CONTROL	0x1104	W	0x00000000	The register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights
GMAC_DMA_CH0_RX_CONTROL	0x1108	W	0x00000000	The DMA Channel0 Receive Control Register controls the Rx features such as PBL, buffer size, and extended status

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_TXDESC_LIST_HADDRESS	0x1110	W	0x00000000	The Channel0 Tx Descriptor List HAddress Register has the higher 8 or 16 bits of the start address of the Transmit descriptor list
GMAC_DMA_CH0_TXDESC_LIST_ADDRESS	0x1114	W	0x00000000	The Channel0 Tx Descriptor List Address Register points the DMA to the start of Transmit descriptor list
GMAC_DMA_CH0_RXDESC_LIST_HAADDRESS	0x1118	W	0x00000000	The Channel0 Rx Descriptor List HAddress Register has the higher 8 or 16 bits of the start address of the Receive descriptor list
GMAC_DMA_CH0_RXDESC_LIST_ADDRESS	0x111C	W	0x00000000	The Channel0 Rx Descriptor List Address Register points the DMA to the start of Receive descriptor list
GMAC_DMA_CH0_TXDESC_TAIL_POINTER	0x1120	W	0x00000000	The Channel0 Tx Descriptor Tail Pointer Register points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH0_RXDESC_TAIL_POINTER	0x1128	W	0x00000000	The Channel0 Rx Descriptor Tail Pointer Register Points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH0_TXDESC_RING_LENGTH	0x112C	W	0x00000000	The Tx Descriptor Ring Length Register contains the length of the Transmit descriptor ring
GMAC_DMA_CH0_RXDESC_RING_LENGTH	0x1130	W	0x00000000	The Channel0 Rx Descriptor Ring Length Register contains the length of the Receive descriptor circular ring
GMAC_DMA_CH0_INTERRUPT_ENABLE	0x1134	W	0x00000000	The Channel0 Interrupt Enable Register enables the interrupts reported by the Status register
GMAC_DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER	0x1138	W	0x00000000	The Receive Interrupt Watchdog Timer Register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA
GMAC_DMA_CH0_CURRENT_APP_TXDESC	0x1144	W	0x00000000	The Channel0 Current Application Transmit Descriptor Register points to the current Transmit descriptor read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXDESC	0x114C	W	0x00000000	The Channel0 Current Application Receive Descriptor Register points to the current Receive descriptor read by the DMA
GMAC_DMA_CH0_CURREN_APP_TXBUFFER_H	0x1150	W	0x00000000	The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_CURRENT_APP_TXBUFFER	0x1154	W	0x00000000	The Channel0 Current Application Transmit Buffer Address Register points to the current Tx buffer address read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXBUFFER_H	0x1158	W	0x00000000	The Channeli Current Application Receive Buffer Address High Register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXBUFFER	0x115C	W	0x00000000	The Channel0 Current Application Receive Buffer Address Register points to the current Rx buffer address read by the DMA
GMAC_DMA_CH0_STATUS	0x1160	W	0x00000000	The software driver (application) reads the Status Register during interrupt service routine or polling to determine the status of the DMA
GMAC_DMA_CH0_MISS_FRAME_CNT	0x1164	W	0x00000000	This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH$i_Rx_Control register
GMAC_DMA_CH0_RX_ERI_CNT	0x1168	W	0x00000000	The DMA_CH0_RX_ERI_Cnt Registers provides the count of the number of times ERI was asserted

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

38.4.3 Detail Registers Description

GMAC_MAC_CONFIGURATION

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	ARPEN ARP Offload Enable When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. Values: 1'b0: ARP Offload is disabled 1'b1: ARP Offload is enabled
30:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RW	0x0	IPC Checksum Offload When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. Values: 1'b0: IP header/payload checksum checking is disabled 1'b1: IP header/payload checksum checking is enabled
26:24	RW	0x0	IPG Inter-Packet Gap These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. Values: 3'b000: 96 bit times IPG 3'b001: 88 bit times IPG 3'b010: 80 bit times IPG 3'b011: 72 bit times IPG 3'b100: 64 bit times IPG 3'b101: 56 bit times IPG 3'b110: 48 bit times IPG 3'b111: 40 bit times IPG
23	RW	0x0	GPSLCE Giant Packet Size Limit Control Enable When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet).The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. Values: 1'b0: Giant Packet Size Limit Control is disabled 1'b1: Giant Packet Size Limit Control is enabled

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Bit	Attr	Reset Value	Description
22	RW	0x0	S2KP IEEE 802.3as Support for 2K Packets When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. Values: 1'b0: Support up to 2K packet is disabled 1'b1: Support up to 2K packet is Enabled
21	RW	0x0	CST CRC stripping for Type packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. Note: For information about how the settings of the ACS bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bits. Values: 1'b0: CRC stripping for Type packets is disabled 1'b1: CRC stripping for Type packets is enabled
20	RW	0x0	ACS Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming packets to the application, without any modification. Note: For information about how the settings of CST bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bit. Values: 1'b0: Automatic Pad or CRC Stripping is disabled 1'b1: Automatic Pad or CRC Stripping is enabled
19	RW	0x0	WD Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. Values: 1'b0: Watchdog is enabled 1'b1: Watchdog is disabled

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Bit	Attr	Reset Value	Description
18	RW	0x0	BE Packet Burst Enable When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. Values: 0x0 (DISABLE): Packet Burst is disabled 0x1 (ENABLE): Packet Burst is enabled Value After Reset: 0x0
17	RW	0x0	JD Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data(10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. Values: 0x0 (ENABLE): Jabber is enabled 0x1 (DISABLE): Jabber is disabled Value After Reset: 0x0 Exists: Always
16	RW	0x0	JE Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. Values: 1'b0: Jumbo packet is disabled 1'b1: Jumbo packet is enabled
15	RW	0x1	PS Port Select This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). The mac_speed_o[1] signal reflects the value of this bit. Values: 1'b0: For 1000 or 2500 Mbps operations 1'b1: For 10 or 100 Mbps operations
14	RW	0x0	FES Speed This bit selects the speed mode. The mac_speed_o[0] signal reflects the value of this bit. Values: 0x0 (10_1000M): 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0 0x1 (100_2500M): 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0
13	RW	0x0	DM Duplex Mode When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. Values: 1'b0: Half-duplex mode 1'b1: Full-duplex mode

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Bit	Attr	Reset Value	Description
12	RW	0x0	LM Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. Values: 1'b0: Loopback is disabled 1'b1: Loopback is enabled
11:10	RO	0x0	reserved
9	RW	0x0	DCRS Disable Carrier Sense During Transmission When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. Values: 1'b0: Enable Carrier Sense During Transmission 1'b1: Disable Carrier Sense During Transmission
8	RW	0x0	DR Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. Values: 1'b0: Enable Retry 1'b1: Disable Retry
7	RO	0x0	reserved
6:5	RW	0x0	BL Back-Off Limit The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. Values: 2'b00: k = min(n,10) 2'b01: k = min(n,8) 2'b10: k = min(n,4) 2'b11: k = min(n,1)

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Bit	Attr	Reset Value	Description
4	RW	0x0	DC Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. Values: 1'b0: Deferral check function is disabled 1'b1: Deferral check function is enabled
3:2	RW	0x0	PRELEN Preamble Length for Transmit packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. Values: 2'b00: 7 bytes of preamble 2'b01: 5 bytes of preamble 2'b10: 3 bytes of preamble 2'b11: Reserved
1	RW	0x0	TE Transmitter Enable When this bit is set, the Tx state machine of the MAC is enabled fortransmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. Values: 0x0 (DISABLE): Transmitter is disabled 0x1 (ENABLE): Transmitter is enabled Value After Reset: 0x0
0	RW	0x0	RE Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. Values: 1'b0: Receiver is disabled 1'b1: Receiver is enabled

GMAC_MAC_EXT_CONFIGURATION

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Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	EIPG Extended Inter-Packet Gap The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	RW	0x0	EIPGEN Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. Values: 1'b0: Extended Inter-Packet Gap is disabled 1'b1: Extended Inter-Packet Gap is enabled
23	RO	0x0	reserved
22:20	RW	0x0	HDSMS Maximum Size for Splitting the Header Data These bits indicate the maximum header size allowed for splitting the header data in the received packet. Values: 0x0 (64BYTES): Maximum Size for Splitting the Header Data is 64 bytes 0x1 (128BYTES): Maximum Size for Splitting the Header Data is 128 bytes 0x2 (256BYTES): Maximum Size for Splitting the Header Data is 256 bytes 0x3 (512BYTES): Maximum Size for Splitting the Header Data is 512 bytes 0x4 (1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes 0x5 (RSVD): Reserved
19	RO	0x0	reserved
18	RW	0x0	USP Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5.

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Bit	Attr	Reset Value	Description
			Values: 1'b0: Unicast Slow Protocol Packet Detection is disabled 1'b1: Unicast Slow Protocol Packet Detection is enabled
17	RW	0x0	SPEN Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. Values: 1'b0: Slow Protocol Detection is disabled 1'b1: Slow Protocol Detection is enabled
16	RW	0x0	DCRCC Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. Values: 1'b0: CRC Checking is enabled 1'b1: CRC Checking is disabled
15:14	RO	0x0	reserved
13:0	RW	0x0000	GPSL Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

GMAC_MAC_PACKET_FILTER

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	RA Receive All When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled 0x1 (ENABLE): Receive All is enabled
30:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	VTFE VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. Values: 1'b0: VLAN Tag Filter is disabled 1'b1: VLAN Tag Filter is enabled
15:11	RO	0x00	reserved
10	RW	0x0	HPF Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. Values: 1'b0: Hash or Perfect Filter is disabled 2'b1: Hash or Perfect Filter is enabled
9:8	RO	0x0	reserved
7:6	RW	0x0	PCF Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets). Values: 2'b00: MAC filters all control packets from reaching the application 2'b01: MAC forwards all control packets except Pause packets to the application even if they fail the Address filter 2'b10: MAC forwards all control packets to the application even if they fail the Address filter 2'b11: MAC forwards the control packets that pass the Address filter
5	RW	0x0	DBF Disable Broadcast Packets When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. Values: 1'b0: Enable Broadcast Packets 1'b1: Disable Broadcast Packets
4	RW	0x0	PM Pass All Multicast When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. Values: 1'b0: Pass All Multicast is disabled 1'b1: Pass All Multicast is enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	DAIF DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. Values: 1'b0: DA Inverse Filtering is disabled 1'b1: DA Inverse Filtering is enabled
2	RW	0x0	HMC Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. Values: 1'b0: Hash Multicast is disabled 1'b1: Hash Multicast is enabled
1:0	RO	0x0	reserved

GMAC_MAC_WATCHDOG_TIMEOUT

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	PWE Programmable Watchdog Enable When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. Values: 1'b0: Programmable Watchdog is disabled 1'b1: Programmable Watchdog is enabled
7:4	RO	0x0	reserved
3:0	RW	0x0	WTO Watchdog Timeout When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. Values: 4'b0000: 2 KB 4'b0001: 3 KB 4'b0010: 4 KB 4'b0011: 5 KB 4'b0100: 6 KB 4'b0101: 7 KB 4'b0110: 8 KB 4'b0111: 9 KB

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Bit	Attr	Reset Value	Description
			4'b1000: 10 KB 4'b1001: 11 KB 4'b1010: 12 KB 4'b1011: 13 KB 4'b1100: 14 KB 4'b1101: 15 KB 4'b1110: 16383 Bytes 4'b1111: Reserved

GMAC_MAC_HASH_TABLE_REG0

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT31T0 MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way: 1. Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32). 2. Perform bitwise reversal for the value obtained in Step 1. 3. Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written. If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_HASH_TABLE_REG1

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT63T32 MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table.

GMAC_MAC_VLAN_TAG

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	EVLRXS Enable VLAN Tag in Rx status When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. Values: 1'b0: VLAN Tag in Rx status is disabled 1'b1: VLAN Tag in Rx status is enabled
23	RO	0x0	reserved
22:21	RW	0x0	EVLS Enable VLAN Tag Stripping on Receive This field indicates the stripping operation on the outer VLAN Tag in received packet. Values: 2'b00: Do not strip 2'b01: Strip if VLAN filter passes 2'b10: Strip if VLAN filter fails 2'b11: Always strip
20	RW	0x0	DOVLTC Disable VLAN Type Check When this bit is set, the MAC does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. Values: 1'b0: VLAN Type Check is enabled 1'b1: VLAN Type Check is disabled
19	RW	0x0	ERSVLM Enable Receive S-VLAN Match When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for filtering or matching. Values: 1'b0: Receive S-VLAN Match is disabled 1'b1: Receive S-VLAN Match is enabled
18	RW	0x0	ESVL Enable S-VLAN When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. Values: 1'b0: S-VLAN is disabled 1'b1: S-VLAN is enabled
17	RW	0x0	VTIM VLAN Tag Inverse Match Enable When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. Values: 1'b0: VLAN Tag Inverse Match is disabled 1'b1: VLAN Tag Inverse Match is enabled

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Bit	Attr	Reset Value	Description
16	RW	0x0	ETV Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. Similarly, when enabled, only 12 bits of the VLAN tag in the received packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for comparison and VLAN hash filtering. Values: 1'b0: 12-Bit VLAN Tag Comparison is disabled 1'b1: 12-Bit VLAN Tag Comparison is enabled
15:0	RW	0x0000	VL VLAN Tag Identifier for Receive Packets This field contains the 802.1Q VLAN tag to identify the VLAN packets. This VLAN tag identifier is compared to the 15th and 16th bytes of the packets being received for VLAN packets. The following list describes the bits of this field: 1. Bits[15:13]: User Priority 2. Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) 3. Bits[11:0]: VLAN Identifier (VID) field of VLAN tag When the ETV bit is set, only the VID is used for comparison. If this field ([11:0] if ETV is set) is all zeros, the MAC does not check the 15th and 16th bytes for VLAN tag comparison and declares all packets with Type field value of 0x8100 or 0x88a8 as VLAN packets.

GMAC_MAC_VLAN_HASH_TABLE

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	VLHT VLAN Hash Table This field contains the 16-bit VLAN Hash Table. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. When ETV bit of MAC_VLAN_Tag register is set, the upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. When ETV bit of MAC_VLAN_Tag register is reset, the ones-complement of upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. For example, when ETV bit is set a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table, whereas when ETV bit is reset a hash value of 4b'1000 selects Bit 7 of the VLAN Hash table. The hash value of the destination address is calculated in the following way: 1. Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3). 2. Perform bitwise reversal for the value obtained in step 1. 3. Take the upper four bits from the value obtained in step 2. If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] (in little-endian mode) or Bits[7:0] (in big-endian mode) of this register are written. 1.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_Q0_TX_FLOW_CTRL

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PT Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	RO	0x00	reserved
7	RW	0x0	DZPQ Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. Values: 1'b0: Zero-Quanta Pause packet generation is enabled 1'b1: Zero-Quanta Pause packet generation is disabled
6:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	TFE Transmit Flow Control Enable Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. Values: 1'b0: Transmit Flow Control is disabled 1'b1: Transmit Flow Control is enabled
0	RW	0x0	FCB_BPA Flow Control Busy or Backpressure Activate This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flow Control Busy or Backpressure Activate is disabled 1'b1: Flow Control Busy or Backpressure Activate is enabled

GMAC_MAC_RX_FLOW_CTRL

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	UP Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow

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Bit	Attr	Reset Value	Description
			Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. Values: 1'b0: Unicast Pause Packet Detect disabled 1'b1: Unicast Pause Packet Detect enabled
0	RW	0x0	RFE Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. Values: 1'b0: Receive Flow Control is disabled 1'b1: Receive Flow Control is enabled

GMAC_MAC_INTERRUPT_STATUS

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	MDIOIS MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: MDIO Interrupt status not active 1'b1: MDIO Interrupt status active
17:15	RO	0x0	reserved
14	RO	0x0	RXSTSIS Receive Status Interrupt This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Receive Interrupt status not active 1'b1: Receive Interrupt status active

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Bit	Attr	Reset Value	Description
13	RO	0x0	TXSTSIS Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: 1. Excessive Collision (EXCOL) 2. Late Collision (LCOL) 3. Excessive Deferral (EXDEF) 4. Loss of Carrier (LCARR) 5. No Carrier (NCARR) 6. Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Transmit Interrupt status not active 1'b1: Transmit Interrupt status active
12	RO	0x0	reserved
11	RO	0x0	MMCRXIPIS MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. Values: 1'b0: MMC Receive Checksum Offload Interrupt status not active 1'b1: MMC Receive Checksum Offload Interrupt status active
10	RO	0x0	MMCTXIS MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Transmit Interrupt status not active 1'b1: MMC Transmit Interrupt status active
9	RO	0x0	MMCRXIS MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Receive Interrupt status not active 1'b1: MMC Receive Interrupt status active
8	RO	0x0	MMCIS MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Interrupt status not active 1'b1: MMC Interrupt status active

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Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4	RO	0x0	PMTIS PMT Interrupt Status This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. Values: 1'b0: PMT Interrupt status not active 1'b1: PMT Interrupt status active
3	RO	0x0	PHYIS PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: PHY Interrupt not detected 1'b1: PHY Interrupt detected
2:0	RO	0x0	reserved

GMAC_MAC_INTERRUPT_ENABLE

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	MDIOIE MDIO Interrupt Enable When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. Values: 1'b0: MDIO Interrupt is disabled 1'b1: MDIO Interrupt is enabled
17:15	RO	0x0	reserved
14	RW	0x0	RXSTSIE Receive Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Receive Status Interrupt is disabled 1'b1: Receive Status Interrupt is enabled
13	RW	0x0	TXSTSIE Transmit Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Timestamp Status Interrupt is disabled 1'b1: Timestamp Status Interrupt is enabled
12:5	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	PMTIE PMT Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. Values: 1'b0: PMT Interrupt is disabled 1'b1: PMT Interrupt is enabled
3	RW	0x0	PHYIE PHY Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. Values: 1'b0: PHY Interrupt is disabled 1'b1: PHY Interrupt is enabled
2:0	RO	0x0	reserved

GMAC_MAC_RX_TX_STATUS

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	RWT Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No receive watchdog timeout 1'b1: Receive watchdog timed out
7:5	RO	0x0	reserved
4	RO	0x0	LCOL Late Collision When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No collision 1'b1: Late collision is sensed

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Bit	Attr	Reset Value	Description
3	RO	0x0	EXDEF Excessive Deferral When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Excessive deferral 1'b1: Excessive deferral
2	RO	0x0	LCARR Loss of Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: Loss of carrier
1	RO	0x0	NCARR No Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: No carrier
0	RO	0x0	TJT Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Transmit Jabber Timeout 1'b1: Transmit Jabber Timeout occurr

GMAC_MAC_PMT_CONTROL_STATUS

Address: **Operational Base** + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31	RW	0x0	RWKFILTRST Remote Wake-Up Packet Filter Register Pointer Reset When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-Up Packet Filter Register Pointer is not Reset 1'b1: Remote Wake-Up Packet Filter Register Pointer is Reset
30:29	RO	0x0	reserved
28:24	RO	0x00	RWKPTR Remote Wake-up FIFO Pointer This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	RO	0x0000	reserved
10	RW	0x0	RWKPFE Remote Wake-up Packet Forwarding Enable When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-up Packet Forwarding is disabled 1'b1: Remote Wake-up Packet Forwarding is enabled
9	RW	0x0	GLBLUCAST Global Unicast When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. Values: 1'b0: Global unicast is disabled 1'b1: Global unicast is enabled
8:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RO	0x0	RWKPRCVD Remote Wake-Up Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Remote wake-up packet is received 1'b1: Remote wake-up packet is received
5	RO	0x0	MGKPRCVD Magic Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Magic packet is received 1'b1: Magic packet is received
4:3	RO	0x0	reserved
2	RW	0x0	RWKPKTEN Remote Wake-Up Packet Enable When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. Values: 1'b0: Remote wake-up packet is disabled 1'b1: Remote wake-up packet is enabled
1	RW	0x0	MGKPKTEN Magic Packet Enable When this bit is set, a power management event is generated when the MAC receives a magic packet. Values: 1'b0: Magic Packet is disabled 1'b1: Magic Packet is enabled
0	RW	0x0	PWRDWN Power Down When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Power down is disabled 1'b1: Power down is enabled

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GMAC_MAC_RWK_PACKET_FILTER

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	WKUPFRMFTR RWK Packet Filter This field contains the various controls of RWK Packet filter. When the Remote Wakeup Filters are to be programmed, the entire set of wkuppktfilter_reg registers must be written. The wkuppktfilter_reg register is programmed by sequentially writing the eight, sixteen or thirty-two register values in MAC_RWK_Packet_Filter register for wkuppktfilter_reg0, wkuppktfilter_reg1, ..., wkuppktfilter_reg31 respectively. The wkuppktfilter_reg register is read in a similar way. The MAC updates the wkuppktfilter_reg register current pointer value in RWKPTR field of MAC_PMT_Control_Status register. The Remote Wakeup Filters are arranged in blocks of 4 filters each and each such block have eight 32-bit wide registers, viz. wkuppktfilter_reg0-7, wkuppktfilter_reg8-15, wkuppktfilter_reg16-23 and wkuppktfilter_reg24-31.

GMAC_RWK_FILTER0_BYTE_MASK

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter0_Byte_Mask Filter0 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_FILTER1_BYTE_MASK

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter1_Byte_Mask Filter1 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_FILTER2_BYTE_MASK

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter2_Byte_Mask Filter2 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_FILTER3_BYTE_MASK

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter3_Byte_Mask Filter3 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC16 calculation.

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GMAC_RWK_FILTER01_CRC

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Filter1_CRC Filter1 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1
15:0	RW	0x0000	Filter0_CRC Filter0 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1

GMAC_RWK_FILTER23_CRC

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Filter3_CRC Filter3 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1
15:0	RW	0x0000	Filter2_CRC Filter2 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15+ x^2 + 1

GMAC_RWK_FILTER_OFFSET

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Filter3_Offset Filter3 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.
23:16	RW	0x00	Filter2_Offset Filter2 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	Filter1_Offset Filter1 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.
7:0	RW	0x00	Filter0_Offset Filter0 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.

GMAC_RWK_FILTER_COMMAND

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	Filter2_Command Filter2 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.
15:12	RO	0x0	reserved
11:8	RW	0x0	Filter1_Command Filter1 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1

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Bit	Attr	Reset Value	Description
			AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.
7:4	RO	0x0	reserved
3:0	RW	0x0	Filter0_Command Filter0 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.

GMAC_MAC_VERSION

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x30	USERVER User-defined Version
7:0	RW	0x51	RKVER Rockchip-defined Version

GMAC_MAC_DEBUG

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:17	RO	0x0	TFCSTS MAC Transmit Packet Controller Status This field indicates the state of the MAC Transmit Packet Controller module. Values: 2'b00: Idle state 2'b01: Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over 2'b10: Generating and transmitting a Pause control packet (in full-duplex mode) 2'b11: Transferring input packet for transmission

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Bit	Attr	Reset Value	Description
16	RO	0x0	TPESTS MAC GMII or MII Transmit Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. Values: 1'b0: MAC GMII or MII Transmit Protocol Engine Status not detected 1'b1: MAC GMII or MII Transmit Protocol Engine Status detected
15:3	RO	0x0000	reserved
2:1	RO	0x0	RFCFCSTS MAC Receive Packet Controller FIFO Status When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	RO	0x0	RPESTS MAC GMII or MII Receive Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. Values: 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected

GMAC_MAC_HW_FEATURE0

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:28	RO	0x4	ACTPHYSEL Active PHY Selected When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. Values: 4'b0000: GMII or MII 4'b0001: RGMII 4'b0010: SGMII 4'b0011: TBI 4'b0100: RMII 4'b0101: RTBI 4'b0110: SMII 4'b0111: RevMII
27	RO	0x0	SAVLANINS Source Address or VLAN Insertion Enable This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected. Values: 1'b0: Source Address or VLAN Insertion Enable option is not selected 1'b1: Source Address or VLAN Insertion Enable option is selected

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Bit	Attr	Reset Value	Description
26:25	RO	0x0	TSSTSSEL Timestamp System Time Source This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 2'b00: Internal 2'b01: External 2'b10: Both 2'b11: Reserved
24	RO	0x0	reserved
23	RO	0x0	MACADR32SEL MAC Addresses 32-63 Selected This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected. Values: 1'b0: MAC Addresses 32-63 Select option is not selected 1'b1: MAC Addresses 32-63 Select option is selected
22:18	RO	0x00	ADDMACADRSEL MAC Addresses 1-31 Selected This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option.
17	RO	0x0	reserved
16	RO	0x1	RXCOESEL Receive Checksum Offload Enabled This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected. Values: 1'b0: Receive Checksum Offload Enable option is not selected 1'b1: Receive Checksum Offload Enable option is selected
15:14	RO	0x0	reserved
13	RO	0x0	EEESEL Energy Efficient Ethernet Enabled This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected. Values: 1'b0: Energy Efficient Ethernet Enable option is not selected 1'b1: Energy Efficient Ethernet Enable option is selected
12	RO	0x1	TSSEL IEEE 1588-2008 Timestamp Enabled This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 1'b0: IEEE 1588-2008 Timestamp Enable option is not selected. 1'b1: IEEE 1588-2008 Timestamp Enable option is selected.
11:10	RO	0x0	reserved
9	RO	0x1	ARPOFFSEL ARP Offload Enabled This bit is set to 1 when the Enable IPv4 ARP Offload option is selected. Values: 1'b0: ARP Offload Enable option is not selected 1'b1: ARP Offload Enable option is selected

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Bit	Attr	Reset Value	Description
8	RO	0x1	MMCSEL RMON Module Enable This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected. Values: 1'b0: RMON Module Enable option is not selected 1'b1: RMON Module Enable option is selected
7	RO	0x1	MGKSEL PMT Magic Packet Enable This bit is set to 1 when the Enable Magic Packet Detection option is selected. Values: 1'b0: PMT Magic Packet Enable option is not selected 1'b1: PMT Magic Packet Enable option is selected
6	RO	0x1	RWKSEL PMT Remote Wake-up Packet Enable This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected. Values: 1'b0: PMT Remote Wake-up Packet Enable option is not selected 1'b1: PMT Remote Wake-up Packet Enable option is selected
5	RO	0x1	SMASEL SMA (MDIO) Interface This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected. Values: 1'b0: SMA (MDIO) Interface not selected 1'b1: SMA (MDIO) Interface selected
4	RO	0x0	VLHASH VLAN Hash Filter Selected This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected. Values: 1'b0: VLAN Hash Filter not selected 1'b1: VLAN Hash Filter selected
3	RO	0x0	PCSSEL PCS Registers (TBI, SGMII, or RTBI PHY interface) This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected. Values: 1'b0: No PCS Registers (TBI, SGMII, or RTBI PHY interface) 1'b1: PCS Registers (TBI, SGMII, or RTBI PHY interface)
2	RO	0x0	HDSEL Half-duplex Support This bit is set to 1 when the half-duplex mode is selected. Values: 1'b0: No Half-duplex support 1'b1: Half-duplex support
1	RO	0x0	GMIISEL 1000 Mbps Support This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation. Values: 1'b0: No 1000 Mbps support 1'b1: 1000 Mbps support

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Bit	Attr	Reset Value	Description
0	RO	0x1	MIISEL 10 or 100 Mbps Support This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation. Values: 1'b0: No 10 or 100 Mbps support 1'b1: 10 or 100 Mbps support

GMAC_MAC_HW_FEATURE1

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RO	0x0	L3L4FNUM Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters: Values: 4'b0000: No L3 or L4 Filter 4'b0001: 1 L3 or L4 Filter 4'b0010: 2 L3 or L4 Filters 4'b0011: 3 L3 or L4 Filters 4'b0100: 4 L3 or L4 Filters 4'b0101: 5 L3 or L4 Filters 4'b0110: 6 L3 or L4 Filters 4'b0111: 7 L3 or L4 Filters 4'b1000: 8 L3 or L4 Filters
26	RO	0x0	reserved
25:24	RO	0x1	HASHTBLSZ Hash Table Size This field indicates the size of the hash table: Values: 2'b00: No hash table 2'b01: 64 2'b10: 128 2'b11: 256
23	RO	0x0	POUOST One Step for PTP over UDP/IP Feature Enable This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. Values: 1'b0: One Step for PTP over UDP/IP Feature is not selected 1'b1: One Step for PTP over UDP/IP Feature is selected
22	RO	0x0	reserved
21	RO	0x0	RAVSEL Rx Side Only AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. Values: 1'b0: Rx Side Only AV Feature is not selected 1'b1: Rx Side Only AV Feature is selected
20	RO	0x0	AVSEL AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option is selected. Values: 1'b0: AV Feature is not selected 1'b1: AV Feature is selected

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Bit	Attr	Reset Value	Description
19	RO	0x1	DBGMEMA DMA Debug Registers Enable This bit is set to 1 when the Debug Mode Enable option is selected. Values: 1'b0: DMA Debug Registers option is not selected 1'b1: DMA Debug Registers option is selected
18	RO	0x1	TSOEN TCP Segmentation Offload Enable This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected. Values: 1'b0: TCP Segmentation Offload Feature is not selected 1'b1: TCP Segmentation Offload Feature is selected
17	RO	0x1	SPHEN Split Header Feature Enable This bit is set to 1 when the Enable Split Header Structure option is selected. Values: 1'b0: Split Header Feature is not selected 1'b1: Split Header Feature is selected
16	RO	0x0	DCBEN DCB Feature Enable This bit is set to 1 when the Enable Data Center Bridging option is selected. Values: 1'b0: DCB Feature is not selected 1'b1: DCB Feature is selected
15:14	RO	0x1	ADDR64 Address Width This field indicates the configured address width: Values: 2'b00: 32 2'b01: 40 2'b10: 48 2'b11: Reserved
13	RO	0x0	reserved
12	RO	0x0	PTOEN PTP Offload Enable This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. Values: 1'b0: PTP Offload feature is not selected 1'b1: PTP Offload feature is selected
11	RO	0x0	OSTEN One-Step Timestamping Enable This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. Values: 1'b0: One-Step Timestamping feature is not selected 1'b1: One-Step Timestamping feature is selected

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Bit	Attr	Reset Value	Description
10:6	RO	0x05	TXFIFOSIZE MTL Transmit FIFO Size This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: Values: 0x0 (128B): 128 bytes 0x1 (256B): 256 bytes 0x2 (512B): 512 bytes 0x3 (1024B): 1024 bytes 0x4 (2048B): 2048 bytes 0x5 (4096B): 4096 bytes 0x6 (8192B): 8192 bytes 0x7 (16384B): 16384 bytes 0x8 (32KB): 32 KB 0x9 (64KB): 64 KB 0xa (128KB): 128 KB 0xb (RSVD): Reserved
5	RO	0x1	SPRAM Single Port RAM Enable This bit is set to 1 when the Use single port RAM Feature is selected. Values: 1'b0: Single Port RAM feature is not selected 1'b1: Single Port RAM feature is selected
4:0	RO	0x06	RXFIFOSIZE MTL Receive FIFO Size This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: Values: 5'b00000: 128 bytes 5'b00001: 256 bytes 5'b00010: 512 bytes 5'b00011: 1024 bytes 5'b00100: 2048 bytes 5'b00101: 4096 bytes 5'b00110: 8192 bytes 5'b00111: 16384 bytes 5'b01000: 32 KB 5'b01001: 64 KB 5'b01010: 128 KB 5'b01011: 256 KB 5'b01100: Reserved

GMAC_MAC_HW_FEATURE2

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:28	RO	0x1	AUXSNAPNUM Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs: Values: 3'b000: No auxiliary input 3'b001: 1 auxiliary input 3'b010: 2 auxiliary input 3'b011: 3 auxiliary input 3'b100: 4 auxiliary input 3'b101: Reserved
27	RO	0x0	reserved
26:24	RO	0x1	PPSOUTNUM Number of PPS Outputs This field indicates the number of PPS outputs: Values: 3'b000: No PPS output 3'b001: 1 PPS output 3'b010: 2 PPS output 3'b011: 3 PPS output 3'b100: 4 PPS output 3'b101: Reserved
23:22	RO	0x0	reserved
21:18	RO	0x0	TXCHCNT Number of DMA Transmit Channels This field indicates the number of DMA Transmit channels: Values: 4'b0000: 1 MTL Tx Channel 4'b0001: 2 MTL Tx Channels 4'b0010: 3 MTL Tx Channels 4'b0011: 4 MTL Tx Channels 4'b0100: 5 MTL Tx Channels 4'b0101: 6 MTL Tx Channels 4'b0110: 7 MTL Tx Channels 4'b0111: 8 MTL Tx Channels
17:16	RO	0x0	reserved
15:12	RO	0x0	RXCHCNT Number of DMA Receive Channels This field indicates the number of DMA Receive channels: Values: 4'b0000: 1 MTL Rx Channel 4'b0001: 2 MTL Rx Channels 4'b0010: 3 MTL Rx Channels 4'b0011: 4 MTL Rx Channels 4'b0100: 5 MTL Rx Channels 4'b0101: 6 MTL Rx Channels 4'b0110: 7 MTL Rx Channels 4'b0111: 8 MTL Rx Channels
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:6	RO	0x0	TXQCNT Number of MTL Transmit Queues This field indicates the number of MTL Transmit queues: Values: 4'b0000: 1 MTL Tx Queue 4'b0001: 2 MTL Tx Queues 4'b0010: 3 MTL Tx Queues 4'b0011: 4 MTL Tx Queues 4'b0100: 5 MTL Tx Queues 4'b0101: 6 MTL Tx Queues 4'b0110: 7 MTL Tx Queues 4'b0111: 8 MTL Tx Queues
5:4	RO	0x0	reserved
3:0	RO	0x0	RXQCNT Number of MTL Receive Queues This field indicates the number of MTL Receive queues: Values: 4'b0000: 1 MTL Rx Queue 4'b0001: 2 MTL Rx Queues 4'b0010: 3 MTL Rx Queues 4'b0011: 4 MTL Rx Queues 4'b0100: 5 MTL Rx Queues 4'b0101: 6 MTL Rx Queues 4'b0110: 7 MTL Rx Queues 4'b0111: 8 MTL Rx Queues

GMAC_MAC_HW_FEATURE3

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RO	0x0	ASP Automotive Safety Package Following are the encoding for the different Safety features. Values: 2'b00: No Safety features selected 2'b01: Only "ECC protection for external memory" feature is selected 2'b10: All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature 2'b11: All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature
27	RO	0x0	TBSSEL Time Based Scheduling Enable This bit is set to 1 when the Time Based Scheduling feature is selected. Values: 1'b0: Time Based Scheduling Enable feature is not selected 1'b1: Time Based Scheduling Enable feature is selected
26	RO	0x0	FPESEL Frame Preemption Enable This bit is set to 1 when the Enable Frame preemption feature is selected. Values: 1'b0: Frame Preemption Enable feature is not selected 1'b1: Frame Preemption Enable feature is selected
25:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:20	RO	0x0	ESTWID Width of the Time Interval field in the Gate Control List This field indicates the width of the Configured Time Interval Field. Values: 2'b00: Width not configured 2'b01: 16 2'b10: 20 2'b11: 24
19:17	RW	0x0	ESTDEP Depth of the Gate Control List This field indicates the depth of Gate Control list expressed as Log2(DWC_EQOS_EST_DEP)-5. Values: 3'b000: No Depth configured 3'b001: 64 3'b010: 128 3'b011: 256 3'b100: 512 3'b101: 1024 3'b110: Reserved
16	RO	0x0	ESTSEL Enhancements to Scheduling Traffic Enable This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. Values: 1'b0: Enable Enhancements to Scheduling Traffic feature is not selected 1'b1: Enable Enhancements to Scheduling Traffic feature is selected
15	RO	0x0	reserved
14:13	RO	0x0	FRPES Flexible Receive Parser Table Entries size This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. Values: 2'b00: 64 Entries 2'b01: 128 Entries 2'b10: 256 Entries 2'b11: Reserved
12:11	RO	0x0	FRPBS Flexible Receive Parser Buffer size This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. Values: 2'b00: 64 Bytes 2'b01: 128 Bytes 2'b10: 256 Bytes 2'b11: Reserved
10:6	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
5	RO	0x0	DVLAN Double VLAN Tag Processing Selected This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. Values: 1'b0: Double VLAN option is not selected 1'b1: Double VLAN option is selected
4	RO	0x0	CBTISEL Queue/Channel based VLAN tag insertion on Tx Enable This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. Values: 1'b0: Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected 1'b1: Enable Queue/Channel based VLAN tag insertion on Tx feature is selected
3	RO	0x0	reserved
2:0	RO	0x0	NRVF Number of Extended VLAN Tag Filters Enabled This field indicates the Number of Extended VLAN Tag Filters selected: Values: 3'b000: No Extended Rx VLAN Filters 3'b001: 4 Extended Rx VLAN Filters 3'b010: 8 Extended Rx VLAN Filters 3'b011: 16 Extended Rx VLAN Filters 3'b100: 24 Extended Rx VLAN Filters 3'b101: 32 Extended Rx VLAN Filters 3'b110: Reserved

GMAC_MAC_MDIO_ADDRESS

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	PSE Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. Values: 1'b0: Preamble Suppression disabled 1'b1: Preamble Suppression enabled
26	RW	0x0	BTB Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. Values:

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Bit	Attr	Reset Value	Description
			1'b0: Back to Back transactions disabled 1'b1: Back to Back transactions enabled
25:21	RW	0x00	PA Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. For RevMII, this field gives the PHY Address of the RevMII module. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	RW	0x00	RDA Register/Device Address These bits select the PHY register in selected Clause 22 PHY device. For RevMII, these bits select the CSR register in the RevMII Registers set. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	RO	0x0	reserved
14:12	RW	0x0	NTC Number of Trailing Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.
11:8	RW	0x0	CR CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: 4'b0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 4'b0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 4'b0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 4'b0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 4'b0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 4'b0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 4'b0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 4'b0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: 4'b1000: CSR clock/4 4'b1001: CSR clock/6 4'b1010: CSR clock/8 4'b1011: CSR clock/10 4'b1100: CSR clock/12 4'b1101: CSR clock/14 4'b1110: CSR clock/16 4'b1111: CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY

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Bit	Attr	Reset Value	Description
			interface.
7:5	RO	0x0	reserved
4	RW	0x0	SKAP Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. Values: 1'b0: Skip Address Packet is disabled 1'b1: Skip Address Packet is enabled
3	RW	0x0	GOC_1 GMII Operation Command 1 This bit is higher bit of the operation command to the PHY or RevMII, GOC_1 and GOC_O is encoded as follows: 2'b00: Reserved 2'b01: Write 2'b10: Post Read Increment Address for Clause 45 PHY 2'b11: Read When Clause 22 PHY or RevMII is enabled, only Write and Read commands are valid. Values: 1'b0: GMII Operation Command 1 is disabled 1'b1: GMII Operation Command 1 is enabled
2	RW	0x0	GOC_0 GMII Operation Command 0 This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. When only RevMII is selected in configuration this bit is read-only and tied to 1. Values: 1'b0: GMII Operation Command 0 is disabled 1'b1: GMII Operation Command 0 is enabled
1	RW	0x0	C45E Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. Values: 1'b0: Clause 45 PHY is disabled 1'b1: Clause 45 PHY is enabled
0	RW	0x0	GB GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no

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Bit	Attr	Reset Value	Description
			change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: GMII Busy is disabled 1'b1: GMII Busy is enabled

GMAC_MAC_MDIO_DATA

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	RA Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	RW	0x0000	GD GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

GMAC_MAC_ARP_ADDRESS

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARPPA ARP Protocol Address This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

GMAC_MAC_CSR_SW_CTRL

Address: **Operational Base** + offset (0x0230)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	RCWE Register Clear on Write 1 Enable When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. Values: 1'b0: Register Clear on Write 1 is disabled 1'b1: Register Clear on Write 1 is enabled

GMAC_MAC_EXT_CFG1

Address: **Operational Base** + offset (0x0238)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	SPLM Split Mode These bits indicate the mode of splitting the incoming Rx packets. They are Values: 0x0 (L3L4): Split at L3/L4 header 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped 0x3 (RSVD): Reserved
7	RO	0x0	reserved
6:0	RW	0x02	SPLOFST Split Offset These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

GMAC_MAC_ADDRESS0_HIGH

Address: **Operational Base** + offset (0x0300)

Bit	Attr	Reset Value	Description
31	RO	0x0	AE Address Enable This bit is always set to 1. Values: 1'b0: This bit must be always set to 1 1'b1: This bit is always set to 1
30:16	RO	0x0000	reserved
15:0	RW	0xffff	ADDRHI MAC Address0[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_ADDRESS0_LOW

Address: **Operational Base** + offset (0x0304)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	ADDRLO MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MMC_CONTROL

Address: **Operational Base** + offset (0x0700)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	UCDBC Update MMC Counters for Dropped Broadcast Packets Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. Values: 1'b0: Update MMC Counters for Dropped Broadcast Packets is disabled 1'b1: Update MMC Counters for Dropped Broadcast Packets is enabled
7:6	RO	0x0	reserved
5	RW	0x0	CNTPRSTLVL Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. Values: 1'b0: Full-Half Preset is disabled 1'b1: Full-Half Preset is enabled
4	RW	0x0	CNTPRST Counters Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters Preset is disabled 1'b1: Counters Preset is enabled
3	RW	0x0	CNTFREEZ MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. Values: 1'b0: MMC Counter Freeze is disabled 1'b1: MMC Counter Freeze is enabled

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Bit	Attr	Reset Value	Description
2	RW	0x0	RSTONRD Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. Values: 1'b0: Reset on Read is disabled 1'b1: Reset on Read is enabled
1	RW	0x0	CNTSTOPRO Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value. Values: 1'b0: Counter Stop Rollover is disabled 1'b1: Counter Stop Rollover is enabled
0	RW	0x0	CNTRST Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters are not reset 1'b1: All counters are reset

GMAC_MMC_RX_INTERRUPT

Address: **Operational Base** + offset (0x0704)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	RXFOVPIS MMC Receive FIFO Overflow Packet Counter Interrupt Status This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Status detected
20	RO	0x0	RXPAUSPIS MMC Receive Pause Packet Counter Interrupt Status This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18	RO	0x0	RXLENERPIS MMC Receive Length Error Packet Counter Interrupt Status This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive Length Error Packet Counter Interrupt Status detected
17:6	RO	0x000	reserved
5	RO	0x0	RXCRCERPIS MMC Receive CRC Error Packet Counter Interrupt Status This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Status not detecte 1'b1: MMC Receive CRC Error Packet Counter Interrupt Status detected
4	RO	0x0	RXMCGPIS MMC Receive Multicast Good Packet Counter Interrupt Status This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Status detected
3	RO	0x0	reserved
2	RO	0x0	RXGOCTIS MMC Receive Good Octet Counter Interrupt Status This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Octet Counter Interrupt Status detected
1	RO	0x0	RXGBOCTIS MMC Receive Good Bad Octet Counter Interrupt Status This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Octet Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
0	RO	0x0	RXGBPKTIS MMC Receive Good Bad Packet Counter Interrupt Status This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Packet Counter Interrupt Status detected

GMAC_MMC_TX_INTERRUPT

Address: **Operational Base** + offset (0x0708)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RO	0x0	TXPAUSPIS MMC Transmit Pause Packet Counter Interrupt Status This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected
22	RO	0x0	reserved
21	RO	0x0	TXGPKTIS MMC Transmit Good Packet Counter Interrupt Status This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Packet Counter Interrupt Status detected
20	RO	0x0	TXGOCTIS MMC Transmit Good Octet Counter Interrupt Status This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Octet Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
19	RO	0x0	TXCARERPIS MMC Transmit Carrier Error Packet Counter Interrupt Status This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Status detected
18:14	RO	0x00	reserved
13	RO	0x0	TXUFLOWERPIS MMC Transmit Underflow Error Packet Counter Interrupt Status This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Status detected
12:2	RO	0x000	reserved
1	RO	0x0	TXGBPKTIS MMC Transmit Good Bad Packet Counter Interrupt Status This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Status detected
0	RO	0x0	TXGBOCTIS MMC Transmit Good Bad Octet Counter Interrupt Status This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Status detected

GMAC_MMC_RX_INTERRUPT_MASK

Address: **Operational Base** + offset (0x070C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	RXFOVPIM MMC Receive FIFO Overflow Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled
20:19	RO	0x0	reserved
18	RW	0x0	RXLENERPIM MMC Receive Length Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Length Error Packet Counter Interrupt Mask is enabled
17:11	RO	0x00	reserved
10	RW	0x0	RXPAUSPIM MMC Receive Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled
9:6	RO	0x0	reserved
5	RW	0x0	RXCRCERPIM MMC Receive CRC Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive CRC Error Packet Counter Interrupt Mask is enabled
4	RW	0x0	RXMCGPIM MMC Receive Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	RXGOCTIM MMC Receive Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Octet Counter Interrupt Mask is enabled
1	RW	0x0	RXGBOCTIM MMC Receive Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Octet Counter Interrupt Mask is enabled
0	RW	0x0	RXGBPKTIM MMC Receive Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Packet Counter Interrupt Mask is enabled

GMAC_MMC_TX_INTERRUPT_MASK

Address: **Operational Base** + offset (0x0710)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	TXPAUSPIM MMC Transmit Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled
22	RO	0x0	reserved
21	RW	0x0	TXGPKTIM MMC Transmit Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Packet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
20	RW	0x0	TXGOCTIM MMC Transmit Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Octet Counter Interrupt Mask is enabled
19	RW	0x0	TXCARERPIM MMC Transmit Carrier Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled
18:14	RO	0x00	reserved
13	RW	0x0	TXUFLOWERPIM MMC Transmit Underflow Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled
12:2	RO	0x000	reserved
1	RW	0x0	TXGBPKTIM MMC Transmit Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled
0	RW	0x0	TXGBOCTIM MMC Transmit Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled

GMAC_TX_OCTET_COUNT_GOOD_BAD

Address: **Operational Base** + offset (0x0714)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTGB Tx Octet Count Good Bad This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

GMAC_TX_PACKET_COUNT_GOOD_BAD

Address: **Operational Base** + offset (0x0718)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTGB Tx Packet Count Good Bad This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

GMAC_TX_UNDERFLOW_ERROR_PACKETS

Address: **Operational Base** + offset (0x0748)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXUNDRFLW Tx Underflow Error Packets This field indicates the number of packets aborted because of packets underflow error.

GMAC_TX_CARRIER_ERROR_PACKETS

Address: **Operational Base** + offset (0x0760)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXCARR Tx Carrier Error Packets This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

GMAC_TX_OCTET_COUNT_GOOD

Address: **Operational Base** + offset (0x0764)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTG Tx Octet Count Good This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

GMAC_TX_PACKET_COUNT_GOOD

Address: **Operational Base** + offset (0x0768)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTG Tx Packet Count Good This field indicates the number of good packets transmitted.

GMAC_TX_PAUSE_PACKETS

Address: **Operational Base** + offset (0x0770)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPAUSE Tx Pause Packets This field indicates the number of good Pause packets transmitted.

GMAC_RX_PACKETS_COUNT_GOOD_BAD

Address: **Operational Base** + offset (0x0780)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPKTGB Rx Packets Count Good Bad This field indicates the number of good and bad packets received.

GMAC_RX_OCTET_COUNT_GOOD_BAD

Address: **Operational Base** + offset (0x0784)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTGB Rx Octet Count Good Bad This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

GMAC_RX_OCTET_COUNT_GOOD

Address: **Operational Base** + offset (0x0788)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTG Rx Octet Count Good This field indicates the number of bytes received, exclusive of preamble, only in good packets.

GMAC_RX_MULTICAST_PACKETS_GOOD

Address: **Operational Base** + offset (0x0790)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXMCASTG Rx Multicast Packets Good This field indicates the number of good multicast packets received.

GMAC_RX_CRC_ERROR_PACKETS

Address: **Operational Base** + offset (0x0794)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXCRCERR Rx CRC Error Packets This field indicates the number of packets received with CRC error.

GMAC_RX_LENGTH_ERROR_PACKETS

Address: **Operational Base** + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXLENERR Rx Length Error Packets This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

GMAC_RX_PAUSE_PACKETS

Address: **Operational Base** + offset (0x07D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPAUSEPKT Rx Pause Packets This field indicates the number of good and valid Pause packets received.

GMAC_RX_FIFO_OVERFLOW_PACKETS

Address: **Operational Base** + offset (0x07D4)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXFIFOOVFL Rx FIFO Overflow Packets This field indicates the number of missed received packets because of FIFO overflow.

GMAC_MMC_IPC_RX_INTERRUPT_MASK

Address: **Operational Base** + offset (0x0800)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	RXICMPEROIM MMC Receive ICMP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled
28	RO	0x0	reserved
27	RW	0x0	RXTCPEROIM MMC Receive TCP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Octet Counter Interrupt Mask is enabled
26	RO	0x0	reserved
25	RW	0x0	RXUDPEROIM MMC Receive UDP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Octet Counter Interrupt Mask is enabled
24:23	RO	0x0	reserved
22	RW	0x0	RXIPV6HEROIM MMC Receive IPV6 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Value: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled
21:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17	RW	0x0	RXIPV4HEROIM MMC Receive IPV4 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled
16:14	RO	0x0	reserved
13	RW	0x0	RXICMPERPIM MMC Receive ICMP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled
12	RO	0x0	reserved
11	RW	0x0	RXTCPERPIM MMC Receive TCP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Packet Counter Interrupt Mask is enabled
10	RO	0x0	reserved
9	RW	0x0	RXUDPERPIM MMC Receive UDP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Packet Counter Interrupt Mask is enabled
8:7	RO	0x0	reserved
6	RW	0x0	RXIPV6HERPIM MMC Receive IPV6 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
5	RW	0x0	RXIPV6GPIM MMC Receive IPV6 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled
4:2	RO	0x0	reserved
1	RW	0x0	RXIPV4HERPIM MMC Receive IPV4 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled
0	RW	0x0	RXIPV4GPIM MMC Receive IPV4 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Mask is disable 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled

GMAC_MMC_IPC_RX_INTERRUPT

Address: **Operational Base** + offset (0x0808)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	RXICMPEROIS MMC Receive ICMP Error Octet Counter Interrupt Status This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Status detected
28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RO	0x0	RXTCPEROIS MMC Receive TCP Error Octet Counter Interrupt Status This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Octet Counter Interrupt Status detected
26	RO	0x0	reserved
25	RO	0x0	RXUDPEROIS MMC Receive UDP Error Octet Counter Interrupt Status This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Octet Counter Interrupt Status detected
24:23	RO	0x0	reserved
22	RO	0x0	RXIPV6HEROIS MMC Receive IPV6 Header Error Octet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected
21:18	RO	0x0	reserved
17	RO	0x0	RXIPV4HEROIS MMC Receive IPV4 Header Error Octet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected
16:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RO	0x0	RXICMPERPIS MMC Receive ICMP Error Packet Counter Interrupt Status This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Status detected
12	RO	0x0	reserved
11	RO	0x0	RXTCPERPIS MMC Receive TCP Error Packet Counter Interrupt Status This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Packet Counter Interrupt Status detected
10	RO	0x0	reserved
9	RO	0x0	RXUDPERPIS MMC Receive UDP Error Packet Counter Interrupt Status This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Packet Counter Interrupt Status detected
8:7	RO	0x0	reserved
6	RO	0x0	RXIPV6HERPIS MMC Receive IPV6 Header Error Packet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected
5	RO	0x0	RXIPV6GPIS MMC Receive IPV6 Good Packet Counter Interrupt Status This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Status not detected

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Bit	Attr	Reset Value	Description
			1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Status detected
4:2	RO	0x0	reserved
1	RO	0x0	RXIPV4HERPIS MMC Receive IPV4 Header Error Packet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected
0	RO	0x0	RXIPV4GPIS MMC Receive IPV4 Good Packet Counter Interrupt Status This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Status detected

GMAC_RXIPV4_GOOD_PACKETS

Address: **Operational Base** + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4GDPKT RxIPv4 Good Packets This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RXIPV4_HEADER_ERROR_PACKETS

Address: **Operational Base** + offset (0x0814)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERRPKT RxIPv4 Header Error Packets This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

GMAC_RXIPV6_GOOD_PACKETS

Address: **Operational Base** + offset (0x0824)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6GDPKT RxIPv6 Good Packets This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RXIPV6_HEADER_ERROR_PACKETS

Address: **Operational Base** + offset (0x0828)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERRPKT RxIPv6 Header Error Packets This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

GMAC_RXUDP_ERROR_PACKETS

Address: **Operational Base** + offset (0x0834)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERRPKT RxUDP Error Packets This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

GMAC_RXTCP_ERROR_PACKETS

Address: **Operational Base** + offset (0x083C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERRPKT RxTCP Error Packets This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

GMAC_RXICMP_ERROR_PACKETS

Address: **Operational Base** + offset (0x0844)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERRPKT RxICMP Error Packets This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

GMAC_RXIPV4_HEADER_ERROR_OCTETS

Address: **Operational Base** + offset (0x0854)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERROCT RxIPv4 Header Error Octets This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RXIPV6_HEADER_ERROR_OCTETS

Address: **Operational Base** + offset (0x0868)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERROCT RxIPv6 Header Error Octets This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RXUDP_ERROR_OCTETS

Address: **Operational Base** + offset (0x0874)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERROCT RxUDP Error Octets This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RXTCP_ERROR_OCTETS

Address: **Operational Base** + offset (0x087C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERROCT RxTCP Error Octets This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RXICMP_ERROR_OCTETS

Address: **Operational Base** + offset (0x0884)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERROCT RxICMP Error Octets This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_MAC_TIMESTAMP_CONTROL

Address: **Operational Base** + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	AV8021ASMEN AV 802.1AS Mode Enable When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. Values: 1'b0: AV 802.1AS Mode is disabled 1'b1: AV 802.1AS Mode is enabled
27:25	RO	0x0	reserved
24	RW	0x0	TXTSSTSM Transmit Timestamp Status Mode When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. Values: 1'b0: Transmit Timestamp Status Mode is disabled 1'b1: Transmit Timestamp Status Mode is enabled
23:19	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	TSENMACADDR Enable MAC Address for PTP Packet Filtering When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. Values: 1'b0: MAC Address for PTP Packet Filtering is disabled 1'b1: MAC Address for PTP Packet Filtering is enabled
17:16	RW	0x0	SNAPTYPSEL Select PTP packets for Taking Snapshots These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.
15	RW	0x0	TSMSTRENA Enable Snapshot for Messages Relevant to Master When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. Values: 1'b0: Snapshot for Messages Relevant to Master is disabled 1'b1: Snapshot for Messages Relevant to Master is enabled
14	RW	0x0	TSEVNTENA Enable Timestamp Snapshot for Event Messages When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. Values: 1'b0: Timestamp Snapshot for Event Messages is disabled 1'b1: Timestamp Snapshot for Event Messages is enabled
13	RW	0x0	TSIPV4ENA Enable Processing of PTP Packets Sent over IPv4-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. Values: 1'b0: Processing of PTP Packets Sent over IPv4-UDP is disabled 1'b1: Processing of PTP Packets Sent over IPv4-UDP is enabled

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Bit	Attr	Reset Value	Description
12	RW	0x0	TSIPV6ENA Enable Processing of PTP Packets Sent over IPv6-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. Values: 1'b0: Processing of PTP Packets Sent over IPv6-UDP is disabled 1'b1: Processing of PTP Packets Sent over IPv6-UDP is enabled
11	RW	0x0	TSIPENA Enable Processing of PTP over Ethernet Packets When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. Values: 1'b0: Processing of PTP over Ethernet Packets is disabled 1'b1: Processing of PTP over Ethernet Packets is enabled
10	RW	0x0	TSVER2ENA Enable PTP Packet Processing for Version 2 Format When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. Values: 1'b0: PTP Packet Processing for Version 2 Format is disabled 1'b1: PTP Packet Processing for Version 2 Format is enabled
9	RW	0x0	TSCTRLSSR Timestamp Digital or Binary Rollover Control When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. Values: 1'b0: Timestamp Digital or Binary Rollover Control is disabled 1'b1: Timestamp Digital or Binary Rollover Control is enabled
8	RW	0x0	TSENALL Enable Timestamp for All Packets When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. Values: 1'b0: Timestamp for All Packets disabled 1'b1: Timestamp for All Packets enabled
7	RO	0x0	reserved
6	RW	0x0	PTGE Presentation Time Generation Enable When this bit is set the Presentation Time generation will be enabled. Values: 0x0 (DISABLE): Presentation Time Generation is disabled 0x1 (ENABLE): Presentation Time Generation is enabled

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Bit	Attr	Reset Value	Description
5	RW	0x0	TSADDREG Update Addend Register When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Addend Register is not updated 1'b1: Addend Register is updated
4	RO	0x0	reserved
3	RW	0x0	TSUPDT Update Timestamp When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated.When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp is not updated 1'b1: Timestamp is updated
2	RW	0x0	TSINIT Initialize Timestamp When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized. When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp is not initialized 1'b1: Timestamp is initialized
1	RW	0x0	TSCFUPDT Fine or Coarse Timestamp Update When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. Values: 1'b0: Coarse method is used to update system timestamp 1'b1: Fine method is used to update system timestamp

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Bit	Attr	Reset Value	Description
0	RW	0x0	TSENA Enable Timestamp When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set. Values: 1'b0: Timestamp is disabled 1'b1: Timestamp is enabled

GMAC_MAC_SUB_SECOND_INCREMENT

Address: **Operational Base** + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	SSINC Sub-second Increment Value The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:0	RO	0x0000	reserved

GMAC_MAC_SYSTEM_TIME_SECS

Address: **Operational Base** + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSS Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

GMAC_MAC_SYSTEM_TIME_NS

Address: **Operational Base** + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00000000	TSSS Timestamp Sub Seconds The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

GMAC_MAC_SYS_TIME_SECS_UPDATE

Address: **Operational Base** + offset (0x0B10)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSS Timestamp Seconds The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

GMAC_MAC_SYS_TIME_NS_UPDATE

Address: **Operational Base** + offset (0x0B14)

Bit	Attr	Reset Value	Description
31	RW	0x0	ADDSUB Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. Values: 1'b0: Add time 1'b1: Subtract time
30:0	RW	0x00000000	TSSS Timestamp Sub Seconds The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register.When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

GMAC_MAC_TIMESTAMP_ADDEND

Address: **Operational Base** + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSAR Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

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GMAC_MAC_TIMESTAMP_STATUS

Address: **Operational Base** + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	ATSNS Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.
24	RO	0x0	ATSSTM Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Values: 1'b0: Auxiliary Timestamp Snapshot Trigger Missed status not detected 1'b1: Auxiliary Timestamp Snapshot Trigger Missed status detected
23:16	RO	0x00	reserved
15	RO	0x0	TXTSSIS Tx Timestamp Status Interrupt Status In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: Tx Timestamp Status Interrupt status not detected 1'b1: Tx Timestamp Status Interrupt status detected
14:4	RO	0x000	reserved
3	RO	0x0	TSTRGTERR0 Timestamp Target Time Error This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Target Time Error status not detected 1'b1: Timestamp Target Time Error status detected

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Bit	Attr	Reset Value	Description
2	RO	0x0	AUXTSTRIG Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Auxiliary Timestamp Trigger Snapshot status not detected 1'b1: Auxiliary Timestamp Trigger Snapshot status detected
1	RO	0x0	TSTARGT0 Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Target Time Reached status not detected 1'b1: Timestamp Target Time Reached status detected
0	RO	0x0	TSSOVF Timestamp Seconds Overflow When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Seconds Overflow status not detected 1'b1: Timestamp Seconds Overflow status detected

GMAC_MAC_TX_TS_STATUS_NS

Address: **Operational Base** + offset (0x0B30)

Bit	Attr	Reset Value	Description
31	RO	0x0	TXTSSMIS Transmit Timestamp Status Missed When this bit is set, it indicates one of the following: 1. The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset. 2. The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Transmit Timestamp Status Missed status not detected 1'b1: Transmit Timestamp Status Missed status detected
30:0	RO	0x00000000	TXTSSLO Transmit Timestamp Status Low This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

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GMAC_MAC_TX_TS_STATUS_SECS

Address: **Operational Base** + offset (0x0B34)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXTSSHI Transmit Timestamp Status High This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

GMAC_MAC_AUXILIARY_CONTROL

Address: **Operational Base** + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ATSEN0 Auxiliary Snapshot 0 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. Values: 0x0 (DISABLE): Auxiliary Snapshot 0 is disabled 0x1 (ENABLE): Auxiliary Snapshot 0 is enabled
3:1	RO	0x0	reserved
0	RW	0x0	ATSFC Auxiliary Snapshot FIFO Clear When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Auxiliary Snapshot FIFO Clear is disabled 1'b1: Auxiliary Snapshot FIFO Clear is enabled

GMAC_MAC_AUXILIARY_TS_NS

Address: **Operational Base** + offset (0x0B48)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RO	0x00000000	AUXTSLO Auxiliary Timestamp Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

GMAC_MAC_AUXILIARY_TS_SECS

Address: **Operational Base** + offset (0x0B4C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AUXTSHI Auxiliary Timestamp Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

GMAC_MAC_TS_INGRESS_CORR_NS

Address: **Operational Base** + offset (0x0B58)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSIC Timestamp Ingress Correction This field contains the ingress path correction value as defined by the Ingress Correction expression.

GMAC_MAC_TS_EGRESS_CORR_NS

Address: **Operational Base** + offset (0x0B5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSEC Timestamp Egress Correction This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

GMAC_MAC_TS_INGRESS_LATENCY

Address: **Operational Base** + offset (0x0B68)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ITLNS Ingress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
15:8	RO	0x00	ITLSNS Ingress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	RO	0x00	reserved

GMAC_MAC_TS_EGRESS_LATENCY

Address: **Operational Base** + offset (0x0B6C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ETLNS Egress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
15:8	RO	0x00	ETLSNS Egress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	RO	0x00	reserved

GMAC_MAC_PPS_CONTROL

Address: **Operational Base** + offset (0x0B70)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	MCGREN0 MCGR Mode Enable for PPS0 Output This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. Values: 0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode 0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode
6:5	RW	0x0	TRGTMODSEL0 Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal: Values: 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding ptp_pps_o output port 0x1 (RSVD): Reserved 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted
4	RW	0x0	PPSEN0 Flexible PPS Output Mode Enable When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode). Values: 0x0 (DISABLE): Flexible PPS Output Mode is disabled 0x1 (ENABLE): Flexible PPS Output Mode is enabled
3:0	RW	0x0	PPSCTRL_PPSCMD PPS Output Frequency Control This field controls the frequency of the PPS0 output (ptp_pps_o[0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: 4'b0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. 4'b0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. 4'b0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. 4'b0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. ... 4'b1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number.

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Bit	Attr	Reset Value	Description
			The actual clock is of different frequency that gets synchronized every second. For example: 1. When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms. 2. When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high). 3. When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high). This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register.

GMAC_MAC_PPS0_TARGET_TIME_SECONDS

Address: **Operational Base** + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSTRH0 PPS Target Time Seconds Register This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

GMAC_MAC_PPS0_TARGET_TIME_NS

Address: **Operational Base** + offset (0x0B84)

Bit	Attr	Reset Value	Description
31	RW	0x0	TRGTBUSY0 PPS Target Time Register Busy The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. Values: 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected 0x1 (ACTIVE): PPS Target Time Register Busy is detected

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Bit	Attr	Reset Value	Description
30:0	RW	0x00000000	TTSL0 Target Time Low for PPS Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

GMAC_MAC_PPS0_INTERVAL

Address: **Operational Base** + offset (0x0B88)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PPSINT0 PPS Output Signal Interval These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

GMAC_MAC_PPS0_WIDTH

Address: **Operational Base** + offset (0x0B8C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PPSWIDTH0 PPS Output Signal Width These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

GMAC_MTL_OPERATION_MODE

Address: **Operational Base** + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	CNTCLR Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Counters are not reset 0x1 (ENABLE): All counters are reset
8	RW	0x0	CNTPRST Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Counters are not reset 0x1 (ENABLE): All counters are reset
7:2	RO	0x00	reserved
1	RW	0x0	DTXSTS Drop Transmit Status When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. Values: 0x0 (DISABLE): Drop Transmit Status is disabled 0x1 (ENABLE): Drop Transmit Status is enabled
0	RO	0x0	reserved

GMAC_MTL_DBG_CTL

Address: **Operational Base** + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	STSIE Transmit Status Available Interrupt Status Enable When this bit is set, an interrupt is generated when Transmit status is available in slave mode. Values: 1'b0: Transmit Packet Available Interrupt Status is disabled 1'b1: Transmit Packet Available Interrupt Status is enabled
14	RW	0x0	PKTIE Receive Packet Available Interrupt Status Enable When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. Values: 1'b0: Receive Packet Available Interrupt Status is disabled 1'b1: Receive Packet Available Interrupt Status is enabled

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	FIFOSEL FIFO Selected for Access This field indicates the FIFO selected for debug access: Values: 2'b00: Tx FIFO 2'b01: Tx Status FIFO (only read access when SLVMOD is set) 2'b10: TSO FIFO (cannot be accessed when SLVMOD is set) 2'b11: Rx FIFO
11	RW	0x0	FIFOWREN FIFO Write Enable When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Write is disabled 1'b1: FIFO Write is enabled
10	RW	0x0	FIFORDEN FIFO Read Enable When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Read is disabled 1'b1: FIFO Read is enabled
9	RW	0x0	RSTSEL Reset Pointers of Selected FIFO When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset Pointers of Selected FIFO is disabled 1'b1: Reset Pointers of Selected FIFO is enabled
8	RW	0x0	RSTALL Reset All Pointers When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset All Pointers is disabled 1'b1: Reset All Pointers is enabled
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	PKTSTATE Encoded Packet State This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
4	RO	0x0	reserved
3:2	RW	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid
1	RW	0x0	DBGMOD Debug Mode Access to FIFO When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: 1. Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO 2. Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: 1. Write access to the Tx FIFO 2. Read access to the Rx FIFO and Tx Status FIFO Values: 1'b0: Debug Mode Access to FIFO is disabled 1'b1: Debug Mode Access to FIFO is enabled
0	RW	0x0	FDBGEN FIFO Debug Access Enable When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. Values: 1'b0: FIFO Debug Access is disabled 1'b1: FIFO Debug Access is enabled

GMAC_MTL_DBG_STS

Address: **Operational Base** + offset (0x0C0C)

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Bit	Attr	Reset Value	Description
31:15	RO	0x00200	LOCR Remaining Locations in the FIFO Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively. Reset: In single Tx Queue configurations, (DWC_EQOS_TXFIFO_SIZE/(DWC_EQOS_DATAWIDTH/8)), Otherwise 0000H.
14:10	RO	0x00	reserved
9	RW	0x0	STSI Transmit Status Available Interrupt Status When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Transmit Status Available Interrupt Status not detected 1'b1: Transmit Status Available Interrupt Status detected
8	RW	0x0	PKTI Receive Packet Available Interrupt Status When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Receive Packet Available Interrupt Status not detected 1'b1: Receive Packet Available Interrupt Status detected
7:5	RO	0x0	reserved
4:3	RO	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid
2:1	RO	0x0	PKTSTATE Encoded Packet State This field is used to get the control or status information of the selected FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. Values: 2'b00: Packet Data

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Bit	Attr	Reset Value	Description
			2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
0	RO	0x0	FIFOBUSY FIFO Busy When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: 1. All other fields of this register 2. All fields of the MTL_FIFO_Debug_Data register Values: 1'b0: FIFO Busy not detected 1'b1: FIFO Busy detected

GMAC_MTL_FIFO_DEBUG_DATA

Address: **Operational Base** + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FDBGDATA FIFO Debug Data During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

GMAC_MTL_INTERRUPT_STATUS

Address: **Operational Base** + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	DBGIS Debug Interrupt status This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Debug Interrupt status not detected 1'b1: Debug Interrupt status detected
16:1	RO	0x0000	reserved
0	RO	0x0	Q0IS Queue 0 Interrupt status This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Queue 0 Interrupt status not detected 1'b1: Queue 0 Interrupt status detected

GMAC_MTL_TXQ0_OPERATION_MODE

Address: **Operational Base** + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	TTC Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. Values: 3'b000: 32 bytes 3'b001: 64 bytes 3'b010: 96 bytes 3'b011: 128 bytes 3'b100: 192 bytes 3'b101: 256 bytes 3'b110: 384 bytes 3'b111: 512 bytes
3:2	RO	0x0	reserved
1	RW	0x0	TSF Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. Values: 1'b0: Transmit Store and Forward is disabled 1'b1: Transmit Store and Forward is enabled
0	RW	0x0	FTQ Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flush Transmit Queue is disabled 1'b1: Flush Transmit Queue is enabled

GMAC_MTL_TXQ0_UNDERFLOW

Address: **Operational Base** + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11	RO	0x0	UFCNTOVF Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow not detected for Underflow Packet Counter 1'b1: Overflow detected for Underflow Packet Counter
10:0	RO	0x000	UFFRMCNT Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_TXQ0_DEBUG

Address: **Operational Base** + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RO	0x0	STXSTSF Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	RO	0x0	reserved
18:16	RO	0x0	PTXQ Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	RO	0x000	reserved
5	RO	0x0	TXSTSFSTS MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. Values: 1'b0: MTL Tx Status FIFO Full status is not detected 1'b1: MTL Tx Status FIFO Full status is detected
4	RO	0x0	TXQSTS MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. Values: 1'b0: MTL Tx Queue Not Empty status is not detected 1'b1: MTL Tx Queue Not Empty status is detected

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Bit	Attr	Reset Value	Description
3	RO	0x0	TWCSTS MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. Values: 1'b0: MTL Tx Queue Write Controller status is not detected 1'b1: MTL Tx Queue Write Controller status is detected
2:1	RO	0x0	TRCSTS MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller: Values: 2'b00: Idle state 2'b01: Read state (transferring data to the MAC transmitter) 2'b10: Waiting for pending Tx Status from the MAC transmitter 2'b11: Flushing the Tx queue because of the Packet Abort request from the MAC
0	RO	0x0	TXQPAUSED Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: 1. Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled 2. Reception of 802.3x Pause packet when PFC is disabled Values: 1'b0: Transmit Queue in Pause status is not detected 1'b1: Transmit Queue in Pause status is detected

GMAC_MTL_Q0_INTERRUPT_CTRL_STATUS

Address: **Operational Base** + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	RXOIE Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. Values: 1'b0: Receive Queue Overflow Interrupt is disabled 1'b1: Receive Queue Overflow Interrupt is enabled
23:17	RO	0x00	reserved
16	RW	0x0	RXOVFIS Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Receive Queue Overflow Interrupt Status not detected 1'b1: Receive Queue Overflow Interrupt Status detected
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	TXUIE Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. Values: 1'b0: Transmit Queue Underflow Interrupt Status is disabled 1'b1: Transmit Queue Underflow Interrupt Status is enabled
7:1	RO	0x00	reserved
0	RW	0x0	TXUNFIS Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Transmit Queue Underflow Interrupt Status not detected 1'b1: Transmit Queue Underflow Interrupt Status detected

GMAC_MTL_RXQ0_OPERATION_MODE

Address: **Operational Base** + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:14	RW	0x0	RFD Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ... 62: Full minus 32 KB, that is, FULL 32 KB 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:12	RO	0x0	reserved
11:8	RW	0x0	RFA Threshold for Activating Flow Control (in half-duplex and full-duplex) These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.

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Bit	Attr	Reset Value	Description
7	RW	0x0	EHFC Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. Values: 1'b0: Hardware Flow Control is disabled 1'b1: Hardware Flow Control is enabled
6	RW	0x0	DIS_TCP_EF Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. Values: 1'b0: Dropping of TCP/IP Checksum Error Packets is enabled 1'b1: Dropping of TCP/IP Checksum Error Packets is disabled
5	RW	0x0	RSF Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. Values: 1'b0: Receive Queue Store and Forward is disabled 1'b1: Receive Queue Store and Forward is enabled
4	RW	0x0	FEP Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA. Values: 1'b0: Forward Error Packets is disabled 1'b1: Forward Error Packets is enabled
3	RW	0x0	FUP Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. Values: 1'b0: Forward Undersized Good Packets is disabled

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Bit	Attr	Reset Value	Description
			1'b1: Forward Undersized Good Packets is enabled
2	RO	0x0	reserved
1:0	RW	0x0	RTC Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.

GMAC_MTL_RXQ0_MISS_PKT_OVF_CNT

Address: **Operational Base** + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	MISCNTOVF Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Missed Packet Counter overflow not detected 1'b1: Missed Packet Counter overflow detected
26:16	RO	0x000	MISPKTCNT Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is incremented each time the application issues ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. In EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations, This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	RO	0x0	reserved
11	RO	0x0	OVFCNTOVF Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow Counter overflow not detected 1'b1: Overflow Counter overflow detected
10:0	RO	0x000	OVFPKTCNT Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

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GMAC_MTL_RXQ0_DEBUG

Address: **Operational Base** + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	PRXQ Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	RO	0x000	reserved
5:4	RO	0x0	RXQSTS MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue: Values: 2'b00: Rx Queue empty 2'b01: Rx Queue fill-level below flow-control deactivate threshold 2'b10: Rx Queue fill-level above flow-control activate threshold 2'b11: Rx Queue full
3	RO	0x0	reserved
2:1	RO	0x0	RRCSTS MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller: Values: 2'b00: Idle state 2'b01: Reading packet data 2'b10: Reading packet status (or timestamp) 2'b11: Flushing the packet data and status
0	RO	0x0	RWCSTS MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. Values: 1'b0: MTL Rx Queue Write Controller Active Status not detected 1'b1: MTL Rx Queue Write Controller Active Status detected

GMAC_DMA_MODE

Address: **Operational Base** + offset (0x1000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	INTM Interrupt Mode This field defines the interrupt mode of DWC_ether_qos. The behavior of the following outputs changes depending on the following settings: 1. sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) 2. sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) 3. sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. 2'b00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the

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Bit	Attr	Reset Value	Description
			corresponding RI/TI status bits. 2'b01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b11: Reserved Values: 2'b00: See above description 2'b01: See above description 2'b10: See above description 2'b11: Reserved
15:9	RO	0x00	reserved
8	RW	0x0	DSPW Descriptor Posted Write When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. Values: 1'b0: Descriptor Posted Write is disabled 1'b1: Descriptor Posted Write is enabled
7:1	RO	0x00	reserved
0	RW	0x0	SWR Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all DWC_ether_qos clock domains. Before reprogramming any DWC_ether_qos register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Software Reset is disabled 1'b1: Software Reset is enabled

GMAC_DMA_SYSBUS_MODE

Address: **Operational Base** + offset (0x1004)

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Bit	Attr	Reset Value	Description
31	RW	0x0	EN_LPI Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. Values: 1'b0: Low Power Interface (LPI) is disabled 1'b1: Low Power Interface (LPI) is enabled
30	RW	0x0	LPI_XIT_PKT Unlock on Magic Packet or Remote Wake-Up Packet When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. Values: 1'b0: Unlock on Magic Packet or Remote Wake-Up Packet is disabled 1'b1: Unlock on Magic Packet or Remote Wake-Up Packet is enabled
29:26	RO	0x0	reserved
25:24	RW	0x0	WR_OSR_LMT AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Note: 1. Bit 26 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ = 4 2. Bit 27 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ!= 16
23:19	RO	0x00	reserved
18:16	RW	0x1	RD_OSR_LMT AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1 Note: 1. Bit 18 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ = 4 2. Bit 19 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ!= 16
15:13	RO	0x0	reserved
12	RW	0x0	AAL Address-Aligned Beats When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels. Values: 1'b0: Address-Aligned Beats is disabled 1'b1: Address-Aligned Beats is enabled

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Bit	Attr	Reset Value	Description
11	RW	0x0	EAME Enhanced Address Mode Enable. When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration. Values: 0x0 (DISABLE): Enhanced Address Mode is disabled 0x1 (ENABLE): Enhanced Address Mode is enabled
10	RW	0x0	AALE Automatic AXI LPI enable When set to 1, enables the AXI master to enter into LPI state when there is no activity in the DWC_ether_qos for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. Values: 1'b0: Automatic AXI LPI is disabled 1'b1: Automatic AXI LPI is enabled
9:4	RO	0x00	reserved
3	RW	0x0	BLEN16 AXI Burst Length 16 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 16
2	RW	0x0	BLEN8 AXI Burst Length 8 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 8
1	RW	0x0	BLEN4 AXI Burst Length 4 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 4
0	RW	0x0	FB Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. 1. Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field 2. Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. Values: 1'b0: Fixed Burst Length is disabled

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Bit	Attr	Reset Value	Description
			1'b1: Fixed Burst Length is enabled

GMAC_DMA_INTERRUPT_STATUS

Address: **Operational Base** + offset (0x1008)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	MACIS MAC Interrupt Status This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. Values: 1'b0: MAC Interrupt Status not detected 1'b1: MAC Interrupt Status detected
16	RO	0x0	MTLIS MTL Interrupt Status This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. Values: 1'b0: MTL Interrupt Status not detected 1'b1: MTL Interrupt Status detected
15:1	RO	0x0000	reserved
0	RO	0x0	DC0IS DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. Values: 1'b0: DMA Channel 0 Interrupt Status not detected 1'b1: DMA Channel 0 Interrupt Status detected

GMAC_DMA_DEBUG_STATUS0

Address: **Operational Base** + offset (0x100C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	TPS0 DMA Channel 0 Transmit Process State This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Transmit Command issued) 4'b0001: Running (Fetching Tx Transfer Descriptor) 4'b0010: Running (Waiting for status) 4'b0011: Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 4'b0100: Timestamp write state 4'b0101: Reserved for future use 4'b0110: Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 4'b0111: Running (Closing Tx Descriptor)

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Bit	Attr	Reset Value	Description
11:8	RO	0x0	RPS0 DMA Channel 0 Receive Process State This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Receive Command issued) 4'b0001: Running (Fetching Rx Transfer Descriptor) 4'b0010: Reserved for future use 4'b0011: Running (Waiting for Rx packet) 4'b0100: Suspended (Rx Descriptor Unavailable) 4'b0101: Running (Closing the Rx Descriptor) 4'b0110: Timestamp write state 4'b0111: Running (Transferring the received packet data from the Rx buffer to the system memory)
7:2	RO	0x00	reserved
1	RO	0x0	AXRHSTS AXI Master Read Channel Status When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. Values: 1'b0: AXI Master Read Channel Status not detected 1'b1: AXI Master Read Channel Status detected
0	RO	0x0	AXWHSTS AXI Master Write Channel or AHB Master Status EQOS-AXI Configuration: When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. EQOS-AHB Configuration: When high, this bit indicates that the AHB master FSMs are in the non-idle state. Values: 1'b0: AXI Master Write Channel or AHB Master Status not detected 1'b1: AXI Master Write Channel or AHB Master Status detected

GMAC_AXI_LPI_ENTRY_INTERVAL

Address: **Operational Base** + offset (0x1040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	LPIEI LPI Entry Interval Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the DWC_ether_qos to enter into the AXI low power state. 0 indicates 64 clock cycles.

GMAC_DMA_CH0_CONTROL

Address: **Operational Base** + offset (0x1100)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	SPH Split Headers When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. Values: 0x0 (DISABLE): Split Headers feature is disabled 0x1 (ENABLE): Split Headers feature is enabled
23:21	RO	0x0	reserved
20:18	RW	0x0	DSL Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	RO	0x0	reserved
16	RW	0x0	PBLx8 8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH0_Tx_Control and Bits[21:16] in DMA_CH0_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled 0x1 (ENABLE): 8xPBL mode is enabled
15:14	RO	0x0	reserved
13:0	RW	0x0000	MSS Maximum Segment Size This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

GMAC_DMA_CH0_TX_CONTROL

Address: **Operational Base** + offset (0x1104)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	TxPBL Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps:

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Bit	Attr	Reset Value	Description
			1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RW	0x0	IPBL Ignore PBL Requirement When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled 0x1 (ENABLE): Ignore PBL Requirement is enabled
14:13	RW	0x0	TSE_MODE TSE Mode 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. 11: Reserved 0x0 (TSO_USO): TSO/USO 0x1 (UFOWC): UFO with Checksum 0x2 (UFOWOC): UFO without Checksum 0x3 (RSVD): Reserved
12	RW	0x0	TSE TCP Segmentation Enabled When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled 0x1 (ENABLE): TCP Segmentation is enabled
11:5	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	OSF Operate on Second Packet When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled 0x1 (ENABLE): Operate on Second Packet enabled
3:1	RO	0x0	reserved
0	RW	0x0	ST Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. 2.The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command 0x1 (START): Start Transmission Command

GMAC_DMA_CH0_RX_CONTROL

Address: **Operational Base** + offset (0x1108)

Bit	Attr	Reset Value	Description
31	RW	0x0	RPF Rx Packet Flush When this bit is set to 1, then DWC_ether_qos automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the DWC_ether_qos not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This may in turn cause head-of-line blocking in the

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Bit	Attr	Reset Value	Description
			corresponding RxQueue. 0x0 (DISABLE): Rx Packet Flush is disabled 0x1 (ENABLE): Rx Packet Flush is enabled
30:22	RO	0x000	reserved
21:16	RW	0x00	RxPBL Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RO	0x0	reserved
14:4	RW	0x000	RBSZ_13_y Receive Buffer size High RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_3_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_3_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	RO	0x0	RBSZ_3_0 Receive Buffer size Low RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_3_0. The RBSZ_3_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO)

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Bit	Attr	Reset Value	Description
0	RW	0x0	SR Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. 2.The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive 0x1 (START): Start Receive

GMAC_DMA_CH0_TXDESC_LIST_HADDRESS

Address: **Operational Base** + offset (0x1110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	TDESHA Start of Transmit List This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

GMAC_DMA_CH0_TXDESC_LIST_ADDRESS

Address: **Operational Base** + offset (0x1114)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDESLA Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_RXDESC_LIST_HAADDRESS

Address: **Operational Base** + offset (0x1118)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	RDESHA Start of Receive List This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

GMAC_DMA_CH0_RXDESC_LIST_ADDRESS

Address: **Operational Base** + offset (0x111C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDESLA Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_TXDESC_TAIL_POINTER

Address: **Operational Base** + offset (0x1120)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDTP Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_RXDESC_TAIL_POINTER

Address: **Operational Base** + offset (0x1128)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDRT Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_TXDESC_RING_LENGTH

Address: **Operational Base** + offset (0x112C)

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Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	TDRL Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. We recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH0_RXDESC_RING_LENGTH

Address: **Operational Base** + offset (0x1130)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	RDRL Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH0_INTERRUPT_ENABLE

Address: **Operational Base** + offset (0x1134)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	NIE Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled 0x1 (ENABLE): Normal Interrupt Summary is enabled
14	RW	0x0	AIE Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 1: Transmit Process Stopped Bit 7: Rx Buffer Unavailable Bit 8: Receive Process Stopped Bit 9: Receive Watchdog Timeout Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled 0x1 (ENABLE): Abnormal Interrupt Summary is enabled

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Bit	Attr	Reset Value	Description
13	RW	0x0	CDEE Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled 0x1 (ENABLE): Context Descriptor Error is enabled
12	RW	0x0	FBEE Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled 0x1 (ENABLE): Fatal Bus Error is enabled
11	RW	0x0	ERIE Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled 0x1 (ENABLE): Early Receive Interrupt is enabled
10	RW	0x0	ETIE Early Transmit Interrupt Enable When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled 0x1 (ENABLE): Early Transmit Interrupt is enabled
9	RW	0x0	RWTE Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled 0x1 (ENABLE): Receive Watchdog Timeout is enabled
8	RW	0x0	RSE Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.
7	RW	0x0	RBUE Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled 0x1 (ENABLE): Receive Buffer Unavailable is enabled
6	RW	0x0	RIE Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled 0x1 (ENABLE): Receive Interrupt is enabled
5:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	TBUE Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled 0x1 (ENABLE): Transmit Buffer Unavailable is enabled
1	RW	0x0	TXSE Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled 0x1 (ENABLE): Transmit Stopped is enabled
0	RW	0x0	TIE Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled 0x1 (ENABLE): Transmit Interrupt is enabled

GMAC_DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER

Address: **Operational Base** + offset (0x1138)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	RWTU Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. 2'b00: 256 2'b01: 512 2'b10: 1024 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	RO	0x00	reserved
7:0	RW	0x00	RWT Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH0_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

GMAC_DMA_CH0_CURRENT_APP_TXDESC

Address: **Operational Base** + offset (0x1144)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTDESAPTR Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_RXDESC

Address: **Operational Base** + offset (0x114C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRDESAPTR Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURREN_APP_TXBUFFER_H

Address: **Operational Base** + offset (0x1150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURTBUFAPTRH Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_TXBUFFER

Address: **Operational Base** + offset (0x1154)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTBUFAPTR Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_RXBUFFER_H

Address: **Operational Base** + offset (0x1158)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURRBUFAPTRH Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_RXBUFFER

Address: **Operational Base** + offset (0x115C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRBUFAPTR Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_STATUS

Address: **Operational Base** + offset (0x1160)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:19	RO	0x0	REB Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 21 1'b1: Error during data transfer by Rx DMA 1'b0: No Error during data transfer by Rx DMA 2.Bit 20 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 19 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	RO	0x0	TEB Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 18 1'b1: Error during data transfer by Tx DMA 1'b0: No Error during data transfer by Tx DMA 2.Bit 17 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 16 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	RW	0x0	NIS Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected 0x1 (ACTIVE): Normal Interrupt Summary status detected

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Bit	Attr	Reset Value	Description
14	RW	0x0	AIS Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 1: Transmit Process Stopped Bit 7: Receive Buffer Unavailable Bit 8: Receive Process Stopped Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected 0x1 (ACTIVE): Abnormal Interrupt Summary status
13	RW	0x0	CDE Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected 0x1 (ACTIVE): Context Descriptor Error status detected
12	RW	0x0	FBE Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected 0x1 (ACTIVE): Fatal Bus Error status detected
11	RW	0x0	ERI Early Receive Interrupt This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected 0x1 (ACTIVE): Early Receive Interrupt status detected

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Bit	Attr	Reset Value	Description
10	RW	0x0	ETI Early Transmit Interrupt This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected 0x1 (ACTIVE): Early Transmit Interrupt status detected
9	RW	0x0	RWT Receive Watchdog Timeout This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. Values: 0x0 (INACTIVE): Receive Watchdog Timeout status not detected 0x1 (ACTIVE): Receive Watchdog Timeout status detected Value After Reset: 0x0 Exists: Always Testable: untestable
8	RW	0x0	RPS Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected 0x1 (ACTIVE): Receive Process Stopped status detected
7	RW	0x0	RBU Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected 0x1 (ACTIVE): Receive Buffer Unavailable status detected
6	RW	0x0	RI Receive Interrupt This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

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Bit	Attr	Reset Value	Description
			0x0 (INACTIVE): Receive Interrupt status not detected 0x1 (ACTIVE): Receive Interrupt status detected
5:3	RO	0x0	reserved
2	RW	0x0	TBU Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected 0x1 (ACTIVE): Transmit Buffer Unavailable status
1	RW	0x0	TPS Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected 0x1 (ACTIVE): Transmit Process Stopped status detected
0	RW	0x0	TI Transmit Interrupt This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected 0x1 (ACTIVE): Transmit Interrupt status detected

GMAC_DMA_CH0_MISS_FRAME_CNT

Address: **Operational Base** + offset (0x1164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	MFC0 Overflow status of the MFC Counter When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred 0x1 (ACTIVE): Miss Frame Counter overflow occurred
14:11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RO	0x000	MFC Dropped Packet Counters This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programming RPF field in DMA_CH0_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_DMA_CH0_RX_ERI_CNT

Address: **Operational Base** + offset (0x1168)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ECNT ERI Counter When ERIC bit of DMA_CH0_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter will get reset at the start of new packet.

38.5 Interface Description

There are two MAC Controllers in RK3506, and each has one set of IO interface, but some pins are also connected with Rockchip Matrix IO, as shown below tables. In addition, the schmitt trigger of mac0_rxd0/1 and mac1_rxd0/1 IO must be disabled.

Table 38-3 MAC Interface

Module Pin	Direction	Pad Name	IOMUX Setting
mac0_clk	I/O	GPIO2_B2	GPIO2_IOC_GPIO2B_IOMUX_SEL_0[11:8]=4'h1
mac0_txen	O	GPIO2_B5	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[7:4]=4'h1
mac0_txd1	O	GPIO2_B4	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[3:0]=4'h1
mac0_txd0	O	GPIO2_B3	GPIO2_IOC_GPIO2B_IOMUX_SEL_0[15:12]=4'h1
mac0_rxdv	I	GPIO2_C0	GPIO2_IOC_GPIO2C_IOMUX_SEL_0[3:0]=4'h1
mac0_rxd1	I	GPIO2_B1	GPIO2_IOC_GPIO2B_IOMUX_SEL_0[7:4]=4'h1
mac0_rxd0	I	GPIO2_B0	GPIO2_IOC_GPIO2B_IOMUX_SEL_0[3:0]=4'h1
eth0_refclko25m	O	GPIO0_C4	GPIO0_IOC_GPIO0C_IOMUX_SEL_1[3:0]=4'h1
mac0_mdio	I/O	GPIO2_B7	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[15:12]=4'h1
mac0_mdc	O	GPIO2_B6	GPIO2_IOC_GPIO2B_IOMUX_SEL_1[11:8]=4'h1
mac1_clk	I/O	GPIO3_B0	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[3:0]=4'h2
mac1_txen	O	GPIO3_B3	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[15:12]=4'h2
mac1_txd1	O	GPIO3_B2	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[11:8]=4'h2

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mac1_txd0	O	GPIO3_B1	GPIO3_IOC_GPIO3B_IOMUX_SEL_0[7:4]=4'h2
mac1_rxdv	I	GPIO3_B6	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[11:8]=4'h2
mac1_rxd1	I	GPIO3_A7	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[15:12]=4'h2
mac1_rxd0	I	GPIO3_A6	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[11:8]=4'h2
eth1_refclko25m	O	GPIO0_C3	GPIO0_IOC_GPIO0C_IOMUX_SEL_0[15:12]=4'h1
mac1_mdio	I/O	GPIO3_B5	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[7:4]=4'h2
mac1_mdc	O	GPIO3_B4	GPIO3_IOC_GPIO3B_IOMUX_SEL_1[3:0]=4'h2

Table 38-4 MAC Rockchip Matrix IO Interface

Module Pin	Direction	Pad Name	IOMUX Setting
mac0_ppstrig	I	RM_IO	GRF_SOC_CON8[6]=1'b1
mac0_ppsclk	O	RM_IO	NA
mac1_ppstrig	I	RM_IO	GRF_SOC_CON11[6]=1'b1
mac1_ppsclk	O	RM_IO	NA

Notes: I=input, O=output, I/O=input/output, bidirectional. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO"

38.6 Application Note

38.6.1 Descriptors

The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention. The DMA is designed for packet-oriented data transfers such as packets in Ethernet. The DMA controller can be programmed to interrupt the application CPU for situations such as Packet Transmit and Receive Transfer completion, and other normal or error conditions.

The DMA and the application communicate through the following two data structures:

- Control and Status registers (CSR)
- Descriptor lists and data buffers

The base address of each list is written to the respective Tx Descriptor List Address register and Rx Descriptor List Address register. The descriptor list is forward linked and the next descriptor is always considered at a fixed offset to the current one. The offset is controlled by the DSL field of DMA_Ch[n]_Control register. The number of descriptors in the list is programmed in the respective Tx (or Rx) Descriptor Ring Length register. Once the DMA processes the last descriptor in the list, it automatically jumps back to the descriptor in the List Address register to create a descriptor ring.

The descriptor lists reside in the physical memory address space of the application. Each descriptor can point to a maximum of two buffers in the system memory. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.

A data buffer resides in the application physical memory space and consists of an entire packet or part of a packet but cannot exceed a single packet. Buffers contain only data. Buffer status is maintained in the descriptor. Data chaining refers to packets that span multiple data buffers. However, a single descriptor cannot span multiple packets. The DMA skips to the data buffer of next packet when EOP is detected.

The MAC supports the following two types of descriptors:

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- Normal Descriptor: Normal descriptors are used for packet data and to provide control information applicable to the packets to be transmitted
- Context Descriptor: Context descriptors are used to provide control information applicable to the packet to be transmitted

The MAC supports the ring structure for the DMA descriptor.

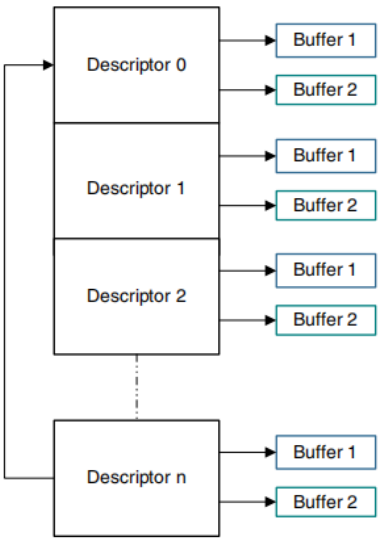

Fig. 38-10 Descriptor Ring Structure

In Ring structure, descriptors are separated by the Word, DWord, or LWord number programmed in the DSL field of the DMA_CH#_Control register. The application needs to program the total ring length, that is, the total number of descriptors in ring span in the following registers of a DMA channel:

- Transmit Descriptor Ring Length Register (DMA_CH#_TxDesc_Ring_Length)
- Receive Descriptor Ring Length Register (DMA_CH#_RxDesc_Ring_Length)

The Descriptor Tail Pointer Register contains the pointer to the descriptor address (N). The base address and the current descriptor pointer decide the address of the current descriptor that the DMA can process.

The descriptors up to one location less than the one indicated by the descriptor tail pointer (N – 1) are owned by the DMA. The DMA continues to process the descriptors until the following condition occurs:

Current Descriptor Pointer == Descriptor Tail Pointer

The DMA goes into the Suspend mode when this condition occurs. The application must perform a write to the Descriptor Tail pointer register and update the tail pointer so that the following condition is true:

Current Descriptor Pointer < Descriptor Tail Pointer

The DMA automatically wraps around the base address when the end of ring is reached. For descriptors owned by the application, the OWN bit of DES3 is reset to 0. For descriptors owned by the DMA, the OWN bit is set to 1. If the application has only one descriptor in the beginning, the application sets the last descriptor address (tail pointer) to Descriptor Base Address + 1. The DMA processes the first descriptor and then waits for the application to advance the tail pointer.

38.6.2 Transmit Descriptors

The DMA in MAC requires at least one descriptor for a transmit packet. In addition to two buffers, two byte-count buffers, and two address pointers, the transmit descriptor has control fields which can be used to control the MAC operation on per-transmit packet basis. The Transmit Normal descriptor has two formats: Read format and Write-Back format.

38.6.3 Transmit Normal Descriptor (Read Format)

Table 38-5 TDES0 Normal Descriptor (Read Format)

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Bit	Name	Description
31:0	BUF1AP	Buffer 1 Address Pointer or TSO Header Address Pointer These bits indicate the physical address of Buffer 1. These bits indicate the TSO Header Address pointer when the following bits are set: ■ TSE bit of TDES3 ■ FD bit of TDES3

Table 38-6 TDES1 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF2AP	Buffer 2 or Buffer 1 Address Pointer This bit indicates the physical address of Buffer 2 when a descriptor ring structure is used. There is no limitation for the buffer address alignment. In 40- or 48-bit addressing mode, these bits indicate the most-significant 8- or 16- bits of the Buffer 1 Address Pointer.

Table 38-7 TDES2 Normal Descriptor (Read Format)

Bit	Name	Description
31	IOC	Interrupt on Completion This bit controls the setting of TI and ETI status bits in the DMA_CH#_Status register. When ETIC = 1 and TDES2[LD] = 0, this bit sets the ETI bit. When TDES3[LD] = 1, this bit sets the TI status bit.
30	TTSE/TMWD	Transmit Timestamp Enable or External TSO Memory Write Enable This bit enables the IEEE1588 time stamping for Transmit packet referenced by the descriptor, if TSE bit is not set. If TSE bit is set and external TSO memory is enabled, setting this bit disables external TSO memory writing for this packet.
29:16	B2L	Buffer 2 Length The driver sets this field. When set, this field indicates Buffer 2 length
15:14	VTIR	VLAN Tag Insertion or Replacement These bits request the MAC to perform VLAN tagging or untagging before transmitting the packets. The application must set the CRC Pad Control bits appropriately when VLAN Tag Insertion, Replacement, or Deletion is enabled for the packet. The following list describes the values of these bits: ■ 2'b00: Do not add a VLAN tag. ■ 2'b01: Remove the VLAN tag from the packets before transmission. This option should be used only with the VLAN packets. ■ 2'b10: Insert a VLAN tag with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the VLAN tag in packets with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. This option should be used only with the VLAN packets. These bits are valid when the Enable SA and VLAN Insertion on Tx option is selected while configuring the

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Bit	Name	Description
		core
13:0	HL or B1L	Header Length or Buffer 1 Length For Header length only bits [9:0] are taken. The size 13:0 is applicable only when interpreting buffer 1 length. If the TCP Segmentation Offload feature is enabled through the TSE bit of TDES3, this field is equal to the header length. When the TSE bit is set in TDES3, the header length includes the length in bytes from Ethernet Source address till the end of the TCP header. The maximum header length supported for TSO feature is 1023 bytes. The maximum header length supported for TSO feature is 1023 bytes. If the TCP Segmentation Offload feature is not enabled, this field is equal to Buffer 1 length.

Table 38-8 TDES3 Normal Descriptor (Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:26	CPC	CRC Pad Control This field controls the CRC and Pad Insertion for Tx packet. This field is valid only when the first descriptor bit (TDES3[29]) is set. The following list describes the values of Bits[27:26]: ■ 2'b00: CRC and Pad Insertion. The MAC appends the cyclic redundancy check (CRC) at the end of the transmitted packet of length greater than or equal to 60 bytes. The MAC automatically appends padding and CRC to a packet with length less than 60 bytes. ■ 2'b01: CRC Insertion (Disable Pad Insertion). The MAC appends the CRC at the end of the transmitted packet but it does not append padding. The application should ensure that the padding bytes are present in the packet being transferred from the Transmit Buffer, that is, the packet being transferred from the Transmit Buffer is of length greater than or equal to 60 bytes. ■ 2'b10: Disable CRC Insertion. The MAC does not append the CRC at the end of the transmitted packet. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer.

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Bit	Name	Description
		■ 2'b11: CRC Replacement. The MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. This field is valid only for the first descriptor. Note: When the TSE bit is set, the MAC ignores this field because the CRC and pad insertion is always done for segmentation.
25:23	SAIC	SA Insertion Control These bits request the MAC to add or replace the Source Address field in the Ethernet packet with the value given in the MAC Address 0 register. The application must set the CRC Pad Control bits appropriately when SA Insertion Control is enabled for the packet. Bit 25 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement. The following list describes the values of Bits[24:23]: ■ 2'b00: Do not include the source address ■ 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. ■ 2'b10: Replace the source address. For reliable transmission, the application must provide frames with source addresses. ■ 2'b11: Reserved These bits are valid in the EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core and when the First Segment control bit (TDES3 [29]) is set. This field is valid only for the first descriptor.
22:19	SLOTNUM or THL	SLOTNUM: Slot Number Control Bits in AV Mode These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES0 or TDES1. When the Transmit descriptor is fetched, the DMA compares the slot number value in this field with the slot interval maintained in the RSN field DMA_CH#_Slot_Function_Control_Status. It fetches the data from the buffers only if a value matches. These bits are valid only for the AV channels. THL: TCP/UDP Header Length If the TSE bit is set, this field contains the length of the TCP/UDP header. The minimum value of this field must be 5 for TCP header. The value must be equal to 2 for UDP header. This field is valid only for the first descriptor.
18	TSE	TCP Segmentation Enable When this bit is set, the DMA performs the TCP/UDP segmentation or UDP fragmentation for a packet depending on the TSE_MODE[1:0] bit of the DMA_CH(#i)_Tx_Control Register. This bit is valid only if the FD bit is set.
17:16	CIC/TPL	Checksum Insertion Control or TCP Payload Length

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Bit	Name	Description
		These bits control the checksum calculation and insertion. The following list describes the bit encoding: ■ 2'b00: Checksum Insertion Disabled. ■ 2'b01: Only IP header checksum calculation and insertion are enabled. ■ 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. ■ 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit TCP/IP Checksum Offload option is selected and the TSE bit is reset. When the TSE bit is set, this field contains the upper bits [17:16] of the TCP Payload (or IP Payload for UDP fragmentation). This allows the TCP/UDP packet length field to be spanned across TDES3[17:0] to provide 256 KB packet length support. This field is valid only for the first descriptor.
15	TPL	Reserved or TCP Payload Length When the TSE bit is reset, this bit is reserved. When the TSE bit is set, this is Bit 15 of the TCP payload length [17:0]. This field is valid only when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected while configuring the core.
14:0	FL/TPL	Frame Length or TCP Payload Length This field is equal to the length of the packet to be transmitted in bytes. When the TSE bit is not set, this field is equal to the total length of the packet to be transmitted: Ethernet Header Length + TCP /IP Header Length – Preamble Length – SFD Length + Ethernet Payload Length When the TSE bit is set, this field is equal to the lower 15 bits of the TCP payload length in case of segmentation and IP payload in case of UDP fragmentation. In case of segmentation, this length does not include Ethernet header or TCP/UDP/IP header length. In case of fragmentation, this length does not include Ethernet header and IP header. When DWRR/WFQ algorithm is NOT enabled, value written into this field is not used when TSE = 0.

38.6.4 Transmit Normal Descriptor (Write-back Format)

The write-back format of the Transmit Descriptor includes timestamp low, timestamp high, OWN, and Status bits. The write-back format is applicable only for the last descriptor of the corresponding packet. The LD bit (TDES3[28]) is set in the descriptor where the DMA writes back the status and timestamp information for the corresponding Transmit packet. This format is only applicable to the last descriptor of a packet.

Table 38-9 TDES0 Normal Descriptor (Write-Back Format)

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Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for the corresponding Transmit packet. The DMA writes the timestamp only if TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and the Timestamp status (TTSS) bit is set

Table 38-10 TDES1 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High The DMA updates this field with the most significant 32 bits of the timestamp captured for corresponding transmit packet. The DMA writes the timestamp only if the TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

Table 38-11 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	Reserved	Reserved

Table 38-12 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:24	Reserved	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location after the first descriptor for a packet ■ All 1s ■ CTXT, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1.

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Bit	Name	Description
		When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status register. Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:18	Reserved	Reserved
17	TTSS	Tx Timestamp Status This status bit indicates that a timestamp has been captured for the corresponding transmit packet. When this bit is set, TDES0 and TDES1 have timestamp values that were captured for the Transmit packet. This field is valid only when the Last Segment control bit (TDES3 [28]) in a descriptor is set. This bit is valid only when IEEE1588 timestamping feature is enabled; otherwise, it is reserved.
16	EUE	ECC Uncorrectable Error Status Indicates the ECC uncorrectable error in the TSO memory. Note: Uncorrectable error in Transmit FIFO memory is reported with (Bit 13) FF = 1. This is because, all such packets are flushed by MAC.
15	ES	Error Summary This bit indicates the logical OR of the following bits: ■ TDES3[0]: IP Header Error ■ TDES3[14]: Jabber Timeout ■ TDES3[13]: Packet Flush ■ TDES3[12]: Payload Checksum Error ■ TDES3[11]: Loss of Carrier ■ TDES3[10]: No Carrier ■ TDES3[9]: Late Collision ■ TDES3[8]: Excessive Collision ■ TDES3[3]: Excessive Deferral ■ TDES3[2]: Underflow Error This bit is also set when EUE (bit 16) is set
14	JT	Jabber Timeout This bit indicates that the MAC transmitter has experienced a jabber time-out. This bit is set only when the JD bit of the MAC_Configuration register is not set.
13	PF	Packet Flushed This bit indicates that the DMA or MTL flushed the packet because of a software flush command given by the CPU.
12	PCE	Payload Checksum Error This bit indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either because of insufficient bytes, as indicated by the Payload Length field of the IP Header or the MTL starting to forward the packet to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet packet being transmitted to

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Bit	Name	Description
		avoid deadlock, the MTL starts forwarding the packet when the FIFO is full, even in the store-and-forward mode. This error can also occur when Bus Error is detected during packet transfer. When the Full Checksum Offload engine is not enabled, this bit is reserved.
11	LoC	Loss of Carrier This bit indicates that Loss of Carrier occurred during packet transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during packet transmission). This is valid only for the packets transmitted without collision and when the MAC operates in the half-duplex mode.
10	NC	No Carrier This bit indicates that the carrier sense signal form the PHY was not asserted during transmission.
9	LC	Late Collision This bit indicates that packet transmission was aborted because a collision occurred after the collision window (64 byte times including Preamble in MII mode and 512 byte times including Preamble and Carrier Extension in GMII mode). This bit is not valid if Underflow Error is set.
8	EC	Excessive Collision This bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after first collision and the transmission of the packet is aborted.
7:4	CC	Collision Count This 4-bit counter value indicates the number of collisions occurred before the packet was transmitted. The count is not valid when the EC bit is set.
3	ED	Excessive Deferral This bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000 Mbps mode or Jumbo Packet enabled mode) if DC bit is set in the MAC_Configuration register. When TBS is enabled in full duplex mode and this bit is set, it indicates that the frame has been dropped after the expiry time has reached.
2	UF	Underflow Error This bit indicates that the MAC aborted the packet because the data arrived late from the system memory. The underflow error can occur because of either of the following conditions: ■ The DMA encountered an empty Transmit Buffer while transmitting the packet ■ The application filled the MTL Tx FIFO slower than the MAC transmit rate The transmission process enter the suspended state and sets the underflow bit corresponding to a queue in the MTL_Interrupt_Status register.
1	DB	Deferred Bit

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Bit	Name	Description
		This bit indicates that the MAC deferred before transmitting because of presence of carrier. This bit is valid only in the half-duplex mode.
0	IHE	IP Header Error When IP Header Error is set, this bit indicates that the Checksum Offload engine detected an IP header error. This bit is valid only when Tx Checksum Offload is enabled. Otherwise, it is reserved. If COE detects an IP header error, it still inserts an IPv4 header checksum if the Ethernet Type field indicates an IPv4 payload. In full duplex mode, when EST/Qbv is enabled and this bit is set, it indicates the frame drop status due to Frame Size error or Schedule Error.

38.6.5 Programming Guide

38.6.5.1 Initializing DMA

Complete the following steps to initialize the DMA:

1. Provide a software reset. This resets all of the MAC internal registers and logic (bit-0 of DMA_Mode).
2. Wait for the completion of the reset process (poll bit 0 of the DMA_Mode, which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the DMA_SysBus_Mode register:

a. AAL

b. Fixed burst or undefined burst

c. Burst mode values in case of AHB bus interface, OSR_LMT in case of AXI bus interface.

d. If fixed length value is enabled, select the maximum burst length possible on the AXI Bus (bits [7:1])

4. Create a descriptor list for transmit and receive. In addition, ensure that the descriptors are owned by DMA (set bit 31 of descriptor TDES3/RDES3). For more information about descriptors, see section "Descriptors".
5. Program the Transmit and Receive Ring length registers (DMA_CH(#i)_TxDesc_Ring_Length (for i = 0; i <= MAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Ring_Length (for i = 0; i <= MAC_NUM_DMA_RX_CH-1)). The ring length programmed must be at least 4.
6. Initialize receive and transmit descriptor list address with the base address of the transmit and receive descriptor (DMA_CH(#i)_TxDesc_List_Address (for i = 0; i <= MAC_NUM_DMA_TX_CH-1), DMA_CH(#i)_RxDesc_List_Address (for i = 0; i <= MAC_NUM_DMA_RX_CH-1)). Also, program transmit and receive tail pointer registers indicating to the DMA about the available descriptors (DMA_CH(#i)_TxDesc_Tail_Pointer (for i = 0; i <= MAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Tail_Pointer (for i = 0; i <= MAC_NUM_DMA_RX_CH-1)).
7. Program the settings of the following registers for the parameters like maximum burst-length (PBL) initiated by DMA, descriptor skip lengths, OSP in case of TxDMA, RBSZ in case of RxDMA, and so on:

- DMA_CH(#i)_Control (for i = 0; i <= MAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_TX_Control (for i = 0; i <= MAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_RX_Control (for i = 0; i <= MAC_NUM_DMA_RX_CH-1)

8. Enable the interrupts by programming the DMA_CH(#i)_Interrupt_Enable (for i = 0; i <= MAC_NUM_DMA_TX_CH-1) register.
9. Start the Receive and Transmit DMAs by setting SR (bit 0) of the DMA_CH(#i)_RX_Control (for i = 0; i <= MAC_NUM_DMA_RX_CH-1) and ST (bit 0) of the DMA_CH(#i)_TX_Control (for i = 0; i <= MAC_NUM_DMA_TX_CH-1) register.
10. Repeat steps 4 to 9 for all the Tx DMA and Rx DMA channels selected in the hardware.

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38.6.5.2 Initializing MTL Registers

The Transaction Layer (MTL) registers must be initialized to establish the transmit and receive operating modes and commands.
Complete the following steps to initialize the MTL registers:
1. Program the Tx Scheduling (SCHALG) and Receive Arbitration Algorithm (RAA) fields in MTL_Operation_Mode to initialize the MTL operation in case of multiple Tx and Rx queues.
2. Program the Receive Queue to DMA mapping in MTL_RxQ_DMA_Map0 and MTL_RxQ_DMA_Map1 registers.
3. Program the following fields to initialize the mode of operation in the MTL_TxQ0_Operation_Mode register.
a. Transmit Store And Forward (TSF) or Transmit Threshold Control (TTC) in case of threshold mode
b. Transmit Queue Enable (TXQEN) to value 2'b10 to enable Transmit Queue0
c. Transmit Queue Size (TQS)
4. Program the following fields to initialize the mode of operation in the MTL_RxQ0_Operation_Mode register:
a. Receive Store and Forward (RSF) or RTC in case of Threshold mode
b. Flow Control Activation and De-activation thresholds for MTL Receive FIFO (RFA and RFD)
c. Error Packet and undersized good Packet forwarding enable (FEP and FUP)
d. Receive Queue Size (RQS)
5. Repeat previous two steps for all MTL Tx and Rx queues selected in the configuration.

38.6.5.3 Initializing MAC

The MAC configuration registers establish the operating mode of the MAC. These registers must be initialized before initializing the DMA.
The following MAC Initialization operations can be performed after DMA initialization. If the MAC initialization is completed before the DMA is configured, enable the MAC receiver (last step in the following sequence) only after the DMA is active. Otherwise, received frames fill the Rx FIFO and overflow.
1. Provide the MAC address registers: MAC_Address0_High and MAC_Address0_Low. If more than one MAC address is enabled in your configuration, program the MAC addresses appropriately.
2. Program the following fields to set the appropriate filters for the incoming frames in the MAC_Packet_Filter register:
a. Receive All
b. Promiscuous mode
c. Hash or Perfect Filter
d. Unicast, multicast, broadcast, and control frames filter settings
3. Program the following fields for proper flow control in the MAC_Q0_Tx_Flow_Ctrl register:
a. Pause time and other Pause frame control bits
b. Transmit Flow control bits
c. Flow Control Busy
4. Program the MAC_Interrupt_Enable register, as required, and if applicable, for your configuration.
5. Program the appropriate fields in the MAC_Configuration register. For ex: Inter-packet gap while transmission and jabber disable.
6. Set bit 0 and 1 in MAC_Configuration registers to start the MAC transmitter and receiver.

38.6.5.4 Performing Normal Receive and Transmit Operation

During normal operation of the MAC, normal and transmit interrupts are read, descriptors polled, the DMA is suspended (if it does not own descriptors), and values of current host transmitter or receiver descriptor pointers are read for debugging.
For normal operation, complete the following steps:

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1. For normal transmit and receive interrupts, read the interrupt status. Then, poll the descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).
2. Set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
3. If the descriptors are not owned by the DMA (or no descriptor is available), the DMA goes into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and writing the descriptor tail pointer to Tx/Rx tail pointer register (DMA_CH[n]_TxDesc_Tail_Pointer and DMA_CH[n]_RxDesc_Tail_Pointer).
4. The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (DMA_CH[n]_Current_App_TxDesc and DMA_CH[n]_Current_App_RxDesc).
5. The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (Register DMA_CH[n]_Current_App_TxBuffer and DMA_CH[n]_Current_App_RxBuffer)

38.6.5.5 Stopping and Starting Transmission

Complete the following steps to pause the transmission for some time.
1. Disable the Transmit DMA (if applicable) by clearing Bit 0 (ST) of DMA_CH(#i)_TX_Control (for i = 0; i <= MAC_NUM_DMA_TX_CH-1) Register.
2. Wait for any previous frame transmissions to complete. You can check this by reading the appropriate bits of MTL_TxQ0_Debug Register (TRCSTS is not 01 and TXQSTS=0).
3. Disable the MAC transmitter and MAC receiver by clearing Bit (RE) and Bit 1(TE) of the MAC_Configuration Register.
4. Disable the Receive DMA (if applicable), after making sure that the data in the Rx FIFO is transferred to the system memory (by reading the appropriate bits of MTL_TxQ0_Debug Register, PRXQ=0 and RXQSTS=00).
5. Make sure that both Tx Queue and Rx Queue are empty (TXQSTS is 0 in MTL_TxQ0_Debug Register and RXQSTS is 0 in MTL_RxQ0_Debug Register).
6. To restart the operation, first start the DMAs, and then enable the MAC Transmitter and Receiver.

38.6.5.6 Initialization Guidelines for System Time Generation

You can enable the timestamp feature by setting Bit 0 of the MAC_Timestamp_Control Register. However, it is essential that the timestamp counter be initialized after this bit is set. Complete the following steps during MAC initialization:
1. Mask the Timestamp Trigger interrupt by clearing the bit 16 of MAC_Interrupt_Enable Register.
2. Set Bit 0 of MAC_Timestamp_Control Register to enable timestamping.
3. Program MAC_Sub_Second_Increment Register based on the PTP clock frequency.
4. If you are using the Fine Correction approach, program MAC_Timestamp_Addend and set Bit 5 of MAC_Timestamp_Control Register.
5. Poll the MAC_Timestamp_Control Register until Bit 5 is cleared.
6. Program Bit 1 of MAC_Timestamp_Control Register to select the Fine Update method (if required).
7. Program MAC_System_Time_Seconds_Update Register and MAC_System_Time_Nanoseconds_Update Register with the appropriate time value.
8. Set Bit 2 in MAC_Timestamp_Control Register.
The timestamp counter starts operation as soon as it is initialized with the value written in the Timestamp Update registers. If one-step timestamping is enabled
a. To enable one-step timestamping, program Bit 27 of the TDES3 Context Descriptor.
b. Program registers MAC_Timestamp_Ingress_Asym_Corr and MAC_Timestamp_Egress_Asym_Corr to update the correction field in PDelay_Req PTP messages.
9. Enable the MAC receiver and transmitter for proper timestamping.

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38.6.5.7 Coarse Correction Method

To synchronize or update the system time in one process (coarse correction method), complete the following steps:
1. Set the offset (positive or negative) in the Timestamp Update registers (MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update).
2. Set Bit 3 (TSUPDT) of MAC_Timestamp_Control Register. The value in the Timestamp Update registers is added to or subtracted from the system time when the TSUPDT bit is cleared.

38.6.5.8 Programming Guidelines for TSO

The TCP Segmentation Offload (TSO) engine is used to offload the TCP segmentation functions to the hardware. To program the TSO, set the TSE bit to enable TCP packet segmentation, and program descriptor fields to enable TSO for the current packet. Complete the following steps to program TSO:
1. Program the TSE bit of corresponding DMA_CH[n]_Tx_Control register to enable TCP packet segmentation in that DMA.
2. In addition to the normal transfer descriptor setting, the following descriptor fields must be programmed to enable TSO for the current packet:
a. Enable TSE in Bit 18 of TDES3
b. Program the length of the un-segmented TCP/IP packet payload in bits [17:0] of TDES3 and the TCP header in bits [22:19] of TDES3.
c. Program the maximum size of the segment in MSS of DMA_CH[n]_Control register or MSS in the context descriptor. If MSS field is programmed in both DMA_CH[n]_Control register and in the context descriptor, the latest software programmed sequence is considered.
3. The header of the unsegmented TCP/IP packet should be in Buffer 1 of the first descriptor and this buffer must not hold any payload bytes. The payload is allocated to Buffer 2 and the buffers of the subsequent descriptors.

38.6.5.9 Programming Guidelines for Multi-Channel Multi-Queuing

Transmit

1. Program the Transmit queue size in the TQS field of MTL_TxQ[n]_Operation_Mode register. Based on the value programmed in the TQS field, the size of the queue is determined.
In the Transmit operation, the number of channels is equal to the number of the queues. Due to this reason, the Channel-to-Queue mapping is fixed.
2. For a queue to be used, the queue needs to be enabled in TXQEN in the corresponding MTL_TxQ[n]_Operation_Mode Register. In DMA configurations, the ST bit of DMA_CH[n]_Tx_Control Register and corresponding TXQEN in MTL_TxQ[n]_Operation Mode Register needs to be enabled.
3. The scheduling method needs to be programmed in SCHALG of MTL_Operation_Mode register.
4. Program the MTL_TxQ[n]_Quantum_Weight for DCB queue as per the selected algorithm. In case of CBS algorithm in AVB queues, the MTL_TxQ[n]_ETS_Control, MTL_TxQ[n]_SendSlopeCredit, MTL_TxQ[n]_HiCredit and MTL_TxQ[n]_LoCredit registers also need to be programmed as required.
5. If DCB is enabled and PFC function is required, program MAC_TxQ_Prty_Map0 Register to assign a fixed priority to the queue. This priority assigned is used for determining if the corresponding queue should stop transmitting packet based on the received PFC packet.

Receive

1. Program the Receive queue size in the RQS field of MTL_RxQ[n]_Operation_Mode Register. Based on the value programmed in RQS field, the size of the queue is determined.
2. Enable the Receive Queues 0 to 7 in the fields RXQ0EN to RXQ7EN in MAC_RxQ_Ctrl0 Register for AV or DCB. In DMA configurations, SR bit of statically or dynamically mapped DMA_CH[n]_Rx_Control Register and corresponding RXQ[n]_EN in MAC_RxQ_Ctrl0 Register needs to be enabled.

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3. The MAC routes the Rx packets to the Rx Queues based on following packet types:
   a. AV PTP Packets: Based on the programming of AVPTPQ in MAC_RxQ_Ctrl1 Register.
   b. AV Untagged Control packets: Based on the programming of AVCPQ in MAC_RxQ_Ctrl1 Register.
   c. Data Center Bridging (DCB) related Link Layer Discovery Protocol (LLDP) packets. Program
   DCBCPQ in MAC_RxQ_Ctrl1 Register to indicate to MAC which queue should get the DCB packets.
   d. VLAN Tag Priority field in VLAN Tagged packets: Program PSRQ7-0 of the MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 Register for the routing of tagged packets based on the USP (user Priority) field of the received packets to the Rx Queues 0 to 7.
   e. The AV tagged control and data packets are also routed based on PSRQ field of the MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers.
4. If multiple RX DMA channels are enabled, the following programming should be done for proper arbitration and mapping:
   a. Program the RAA field of MTL_Operation_Mode register to select the arbitration algorithm to decide which RxQ is read out from the RxFIFO memory.
   b. Program the MTL_RxQ[n]_Control to decide the weights and the packet arbitration for each RxQ.
   c. If static mapping is programmed in MTL_RxQ_DMA_Map[n] register (RXQ[n]DADMACH is reset to 0), bits RXQx2DMA and others need to be programmed to select the channel for which each queue is mapped.
   d. Set RXQ[n]DADMACH bit in MTL_RxQ_DMA_Map0 Register to select dynamic mapping of
   packets in each RxQueue.
   e. In dynamic channel mapping, the routing of a packet to a specific RxDMA channel is decided by the value of DCS field in the lowest MAC Address Register.

38.6.6 Transmit Context Descriptor

The context descriptor is used to provide the timestamps for one-step timestamp correction, VLAN Tag ID for VLAN insertion feature. The Transmit Context descriptor can be provided any time before a packet descriptor. The context is valid for the current packet and subsequent packets. The context descriptor is used to provide the timestamps for one-step timestamp correction and VLAN Tag ID for VLAN insertion feature. Write back is done on a context descriptor only to reset the OWN bit.

Table 38-13 TDES0 Context Descriptor

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low For one-step correction, the driver can provide the lower 32 bits of timestamp in this descriptor word. The DMA uses this value as the low word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 38-14 TDES1 Context Descriptor

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High For one-step correction, the driver can provide the upper 32 bits of timestamp in this descriptor. The DMA uses this value as the high word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

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Table 38-15 TDES2 Context Descriptor

Bit	Name	Description
31:16	IVT	Inner VLAN Tag When the IVLTV bit of TDES3 context descriptor is set and the TCMSSV and OSTC bits of TDES3 context descriptor are reset, TDES2[31:16] contains the inner VLAN Tag to be inserted in the subsequent Transmit packets.
15:14	Reserved	Reserved
13:0	MSS	Maximum Segment Size When the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected, the driver can provide maximum segment size in this field. This segment size is used while segmenting the TCP/IP payload. This field is valid only if the TCMSSV bit of TDES3 context descriptor is set and the OSTC bit of the TDES3 context descriptor is reset.

Table 38-16 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the MAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit immediately after the read.
30	CTXT	Context Type This bit should be set to 1'b1 for Context descriptor.
29:28	Reserved	Reserved
27	OSTC	One-Step Timestamp Correction Enable When this bit is set, the DMA performs a one-step timestamp correction with reference to the timestamp values provided in TDES0 and TDES1.
26	TCMSSV	One-Step Timestamp Correction Input or MSS Valid When this bit and the OSTC bit are set, it indicates that the Timestamp Correction input provided in TDES0 and TDES1 is valid. When the OSTC bit is reset and this bit and the TSE bit of TDES3 are set in subsequent normal descriptor, it indicates that the MSS input in TDES2 is valid.
25:24	Reserved	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect.The DMA sets this bit during write-back while closing the context descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location before the first descriptor for a packet ■ All 1s ■ CD, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status Register.

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Bit	Name	Description
		Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:20	Reserved	Reserved
19:18	IVTIR	Inner VLAN Tag Insert or Replace When this bit is set, these bits request the MAC to perform Inner VLAN tagging or un-tagging before transmitting the packets. If the packet is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits: ■ 2'b00: Do not add the inner VLAN tag. ■ 2'b01: Remove the inner VLAN tag from the packets before transmission. This option should be used only with the VLAN frames. ■ 2'b10: Insert an inner VLAN tag with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the inner VLAN tag in packets with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. This option should be used only with the VLAN frames. These bits are valid when the Enable SA and VLAN Insertion on Tx and Enable Double VLAN Processing options are selected.
17	IVLTV	Inner VLAN Tag Valid When this bit is set, it indicates that the IVT field of TDES2 is valid.
16	VLTV	VLAN Tag Valid When this bit is set, it indicates that the VT field of TDES3 is valid.
15:0	VT	VLAN Tag This field contains the VLAN Tag to be inserted or replaced in the packet. This field is used as VLAN Tag only when the VLTI bit of the MAC_VLAN_Incl register is reset.

38.6.7 Receive Descriptors

The DMA in MAC attempts to read a descriptor only if the Tail Pointer is different from the Base Pointer or current pointer. It is recommended to have a descriptor ring with a length that can accommodate at least two complete packets received by the MAC. Otherwise, the performance of the DMA is impacted greatly because of the unavailability of the descriptors. In such situations, the RxFIFO in MTL becomes full and starts dropping packets.

The following Receive Descriptors are present:

- Normal descriptors
- Context descriptors

All RX descriptors are prepared by the software and given to the DMA as "Normal" Descriptors with the content as shown in Receive Normal Descriptor (Read Format). The DMA reads this descriptor and after transferring a received packet (or part of) to the buffers indicated by the descriptor, the Rx DMA will close the descriptor with the corresponding packet status. The format of this status is given in the "Receive Normal Descriptor (Write-Back Format)". For some packets, the normal descriptor bits are not enough to write the complete status. For such packets, the RX DMA writes the extended status to the next descriptor (without processing or using the Buffers/ Pointers embedded

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in that descriptor). The format and content of the descriptor write back is described in "Receive Context Descriptor".

38.6.8 Receive Normal Descriptors (Read Format)

Table 38-17 TDES0 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF1AP	Header or Buffer 1 Address Pointer When the SPH bit of Control register of a channel is reset, these bits indicate the physical address of Buffer 1. When the SPH bit is set, these bits indicate the physical address of Header Buffer where the Rx DMA writes the L2/L3/L4 header bytes of the received packet. The application can program a byte-aligned address for this buffer which means that the LS bits of this field can be non-zero. However, while transferring the start of packet, the DMA performs a Write operation with RDES0[1:0] (or RDES0[2:0]/[3:0] in case of 64-/128-bit configuration) as zero. However, the packet data is shifted as per actual offset as given by buffer address pointer. If the address pointer points to a buffer where the middle or last part of the packet is stored, the DMA ignores the offset address and writes to the full location as indicated by the data-width.

Table 38-18 TDES1 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 38-19 TDES2 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 38-20 TDES3 Normal Descriptor(Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the MAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	IOC	Interrupt Enabled on Completion When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor.
29:26	Reserved	Reserved
25	BUF2V	Buffer 2 Address Valid When this bit is set, it indicates to the DMA that the buffer 2 address specified in RDES2 is valid.

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Bit	Name	Description
		The application must set this bit so that the DMA can use the address, to which the Buffer 2 address in RDES2 is pointing, to write received packet data.
24	BUF1V	Buffer 1 Address Valid When set, this indicates to the DMA that the buffer 1 address specified in RDES1 is valid. The application must set this value if the address pointed to by Buffer 1 address in RDES1 can be used by the DMA to write received packet data.
23:0	Reserved	Reserved

38.6.9 Receive Normal Descriptors (Write-Back Format)

Table 38-21 TDES0 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:16	IVT	Inner VLAN Tag This field contains the Inner VLAN tag of the received packet if the RS0V bit of RDES3 is set. This is valid only when Double VLAN tag processing and VLAN tag stripping are enabled.
15:0	OVT	Outer VLAN Tag This field contains the Outer VLAN tag of the received packet if the RS0V bit of RDES3 is set.

Table 38-22 TDES1 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	OPC	OAM Sub-Type Code, or MAC Control Packet opcode OAM Sub-Type Code If Bits[18:16] of RDES3 are set to 3'b111, this field contains the OAM sub-type and code fields. MAC Control Packet opcode If Bits[18:16] of RDES3 are set to 3'b110, this field contains the MAC Control packet opcode field.
15	TD	Timestamp Dropped This bit indicates that the timestamp was captured for this packet but it got dropped in the MTL Rx FIFO because of overflow. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
14	TSA	Timestamp Available When Timestamp is present, this bit indicates that the timestamp value is available in a context descriptor word 2 (RDES2) and word 1(RDES1). This is valid only when the Last Descriptor bit (RDES3 [28]) is set. The context descriptor is written in the next descriptor just after the last normal descriptor for a packet.
13	PV	PTP Version This bit indicates that the received PTP message has the IEEE 1588 version 2 format. When this bit is reset, it indicates the IEEE 1588 version 1 format. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
12	PFT	PTP Packet Type This bit indicates that the PTP message is sent directly over Ethernet. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.

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Bit	Name	Description
11:8	PMT	PTP Message Type These bits are encoded to give the type of the message received: ■ 0000: No PTP message received ■ 0001: SYNC (all clock types) ■ 0010: Follow_Up (all clock types) ■ 0011: Delay_Req (all clock types) ■ 0100: Delay_Resp (all clock types) ■ 0101: Pdelay_Req (in peer-to-peer transparent clock) ■ 0110: Pdelay_Resp (in peer-to-peer transparent clock) ■ 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) ■ 1000: Announce ■ 1001: Management ■ 1010: Signaling ■ 1011–1110: Reserved ■ 1111: PTP packet with Reserved message type These bits are available only when you select the Timestamp feature.
7	IPCE	IP Payload Error When this bit is set, it indicates either of the following: ■ The 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) calculated by the MAC does not match the corresponding checksum field in the received segment. ■ The TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. ■ The TCP, UDP, or ICMP segment length is less than minimum allowed segment length for TCP, UDP, or ICMP. Bit 15 (ES) of RDES3 is not set when this bit is set.
6	IPCB	IP Checksum Bypassed This bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
5	IPV6	IPv6 header Present This bit indicates that an IPV6 header is detected. When the Enable Split Header Feature option is selected and the SPH bit of Control Register of a channel is set, the IPV6 header is available in the header buffer area to which RDES0 is pointing.
4	IPV4	IPV4 Header Present This bit indicates that an IPV4 header is detected. When the SPH bit of RDES3 is set, the IPV4 header is available in the header buffer area to which RDES0 is pointing.
3	IPHE	IP Header Error When this bit is set, it indicates either of the following: ■ The 16-bit IPv4 header checksum calculated by the MAC does not match the received checksum bytes.

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Bit	Name	Description
		■ The IP datagram version is not consistent with the Ethernet Type value. ■ Ethernet packet does not have the expected number of IP header bytes. This bit is valid when either Bit 5 or Bit 4 is set. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
2:0	PT	Payload Type These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE): ■ 3'b000: Unknown type or IP/AV payload not processed ■ 3'b001: UDP ■ 3'b010: TCP ■ 3'b011: ICMP ■ 3'b110: AV Tagged Data Packet ■ 3'b111: AV Tagged Control Packet ■ 3'b101: AV Untagged Control Packet ■ 3'b100: IGMP if IPV4 Header Present bit is set else DCB (LLDP) Control Packet If the COE does not process the payload of an IP datagram because there is an IP header error or fragmented IP, it sets these bits to 3'b000.

Table 38-23 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:29	L3L4FM	Layer 3 and Layer 4 Filter Number Matched These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received packet: ■ 000: Filter 0 ■ 001: Filter 1 ■ 010: Filter 2 ■ 011: Filter 3 ■ 100: Filter 4 ■ 101: Filter 5 ■ 110: Filter 6 ■ 111: Filter 7 This field is valid only when Bit 28 or Bit 27 is set high. When more than one filter matches, these bits give the number of lowest filter. Note: This status is not available when Flexible RX Parser is enabled.
28	L4FM	Layer 4 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true: ■ Layer 3 fields are not enabled and all enabled Layer 4 fields match ■ All enabled Layer 3 and Layer 4 filter fields match When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.
27	L3FM	Layer 3 Filter Match

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Bit	Name	Description
		When this bit is set, it indicates that the received packet matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true: ■ All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed ■ All enabled filter fields match When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.
26:19	MADRM	MAC Address Match or Hash Value When the HF bit is reset, this field contains the MAC address register number that matched the Destination address of the received packet. This field is valid only if the DAF bit is reset. When the HF bit is set, this field contains the hash value computed by the MAC. A packet passes the hash filter when the bit corresponding to the hash value is set in the hash filter register. Note: This status is not available when Flexible RX Parser is enabled.
18	HF	Hash Filter Status When this bit is set, it indicates that the packet passed the MAC address hash filter. Bits[26:19] indicate the hash value. Note: This status is not available when Flexible RX Parser is enabled.
17	DAF/RXPI	Destination Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the DA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet parsing is incomplete (RXPI) due to ECC error. Note: When this bit is set, ES bit of RDES3 is also set.
16	SAF/RXPD	SA Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the SA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet is dropped (RXPD) by the parser. Note: When this bit is set, ES bit of RDES3 is also set.
15	OTS	VLAN Filter Status When set, this bit indicates that the VLAN Tag of the received packed passed the VLAN filter. This bit is valid only when MAC_ERVFE is not enabled. If MAC_ERVFE is enabled, the bit is redefined as Outer VLAN Tag Filter Status (OTS). This bit is valid for both Single and Double VLAN Tagged frames.
14	ITS	Inner VLAN Tag Filter Status (ITS) This bit is valid only when MAC_ERVFE is enabled. This bit is valid only for Double VLAN Tagged frames, when Double VLAN Processing is enabled.

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Bit	Name	Description
		For more information, see the Filter Status topic.
13:11	Reserved	Reserved
10	ARPNR	ARP Reply Not Generated When this bit is set, it indicates that the MAC did not generate the ARP Reply for received ARP Request packet. This bit is set when the MAC is busy transmitting ARP reply to earlier ARP request (only one ARP request is processed at a time). This bit is reserved when the Enable IPv4 ARP Offload option is not selected.
9:0	HL	L3/L4 Header Length This field contains the length of the header of the packet split by the MAC at L3 or L4 header boundary as identified by the MAC receiver. This field is valid only when the first descriptor bit is set (FD = 1). The header data is written to the Buffer 1 address of corresponding descriptor. If header length is zero, this field is not valid. It implies that the MAC did not identify and split the header. This field is valid when the Enable Split Header Feature option is selected.

Table 38-24 TDES3 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the MAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context type descriptor. The DMA writes 1'b0 to this bit for normal receive descriptor. When CTXT and FD bits are used together, {CTXT, FD} ■ 2’b00: Intermediate Descriptor ■ 2’b01: First Descriptor ■ 2’b10: Reserved ■ 2’b11: Descriptor Error (due to all 1s) Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	FD	First Descriptor When this bit is set, it indicates that this descriptor contains the first buffer of the packet. If the size of the first buffer is 0, the second buffer contains the beginning of the packet. If the size of the second

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Bit	Name	Description
		buffer is also 0, the next descriptor contains the beginning of the packet. See the CTXT bit description for details of using the CTXT bit and FD bit together.
28	LD	Last Descriptor When this bit is set, it indicates that the buffers to which this descriptor is pointing are the last buffers of the packet.
27	RS2V	Receive Status RDES2 Valid When this bit is set, it indicates that the status in RDES2 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
26	RS1V	Receive Status RDES1 Valid When this bit is set, it indicates that the status in RDES1 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
25	RS0V	Receive Status RDES0 Valid When this bit is set, it indicates that the status in RDES0 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
24	CE	CRC Error When this bit is set, it indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received packet. This field is valid only when the LD bit of RDES3 is set.
23	GP	Giant Packet When this bit is set, it indicates that the packet length exceeds the specified maximum Ethernet size of 1518, 1522, or 2000 bytes (9018 or 9022 bytes if jumbo packet enable is set). Note: Giant packet indicates only the packet length. It does not cause any packet truncation.
22	RWT	Receive Watchdog Timeout When this bit is set, it indicates that the Receive Watchdog Timer has expired while receiving the current packet. The current packet is truncated after watchdog timeout.
21	OE	Overflow Error When this bit is set, it indicates that the received packet is damaged because of buffer overflow in Rx FIFO. Note: This bit is set only when the DMA transfers a partial packet to the application. This happens only when the Rx FIFO is operating in the threshold mode. In the store-and-forward mode, all partial packets are dropped completely in Rx FIFO.
20	RE	Receive Error When this bit is set, it indicates that the gmii_rxer_i signal is asserted while the gmii_rxdv_i signal is asserted during packet reception. This error also includes carrier extension error in the GMII and half-duplex mode. Error can be of less or no extension, or error (rxd!= 0f) during extension.
19	DE	Dribble Bit Error

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Bit	Name	Description
		When this bit is set, it indicates that the received packet has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.
18:16	LT	Length/Type Field This field indicates if the packet received is a length packet or a type packet. The encoding of the 3 bits is as follows: ■ 3'b000: The packet is a length packet ■ 3'b001: The packet is a type packet. ■ 3'b011: The packet is a ARP Request packet type ■ 3'b100: The packet is a type packet with VLAN Tag ■ 3'b101: The packet is a type packet with Double VLAN Tag ■ 3'b110: The packet is a MAC Control packet type ■ 3'b111: The packet is a OAM packet type ■ 3'b010: Reserved
15	ES	Error Summary When this bit is set, it indicates the logical OR of the following bits: ■ RDES3[24]: CRC Error ■ RDES3[19]: Dribble Error ■ RDES3[20]: Receive Error ■ RDES3[22]: Watchdog Timeout ■ RDES3[21]: Overflow Error ■ RDES3[23]: Giant Packet ■ RDES2[17]: Destination Address Filter Fail, when Flexible RX Parser is enabled ■ RDES2[16]: SA Address Filter Fail, when Flexible RX Parser is enabled This field is valid only when the LD bit of RDES3 is set.
14	PL	Packet Length These bits indicate the byte length of the received packet that was transferred to system memory (including CRC). This field is valid when the LD bit of RDES3 is set and Overflow Error bits are reset. The packet length also includes the two bytes appended to the Ethernet packet when IP checksum calculation is enabled and the received packet is not a MAC control packet. This field is valid when the LD bit of RDES3 is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current packet.

38.6.10 Receive Context Descriptor

This descriptor is read-only for the application. Only the DMA can write to this descriptor. The context descriptor provides information about the extended status related to the last received packet. The Bit 30 of RDES3 indicates the context type descriptor.

Table 38-25 TDES0 Context Descriptor

Bit	Name	Description
31:0	RSTL	Receive Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for corresponding

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Bit	Name	Description
		Receive packet. When this field and the RTSH field of RDES1 show all-ones value, the timestamp must be considered as corrupt.

Table 38-26 TDES1 Context Descriptor

Bit	Name	Description
31:0	RSTH	Receive Packet Timestamp High The DMA updates this field with most significant 32 bits of the timestamp captured for corresponding receive packet. When this field and the RTSL field of RDES0 show all-ones value, the timestamp must be considered as corrupt.

Table 38-27 TDES2 Context Descriptor

Bit	Name	Description
31:0	Reserved	Reserved

Table 38-28 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context descriptor. The DMA writes 1'b1 to this bit for context descriptor. DMA writes 2’b11 to indicate a descriptor error due to all 1s. When CTXT and DE bits are used together, {CTXT, DE} ■ 2’b00: Reserved ■ 2’b01: Reserved ■ 2’b10: Context Descriptor ■ 2’b11: Descriptor Error Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	DE	Descriptor Error See the CTXT bit description for details of using theDE bit along with CTXT bit.
28:0	Reserved	Reserved

38.6.11 Clock Architecture

In RMII mode, reference clock and TX/RX clock be from PHY as following figure. The mux of selecting rmii_speed is GRF_SOC_CON8[3]/GRF_SOC_CON11[3].

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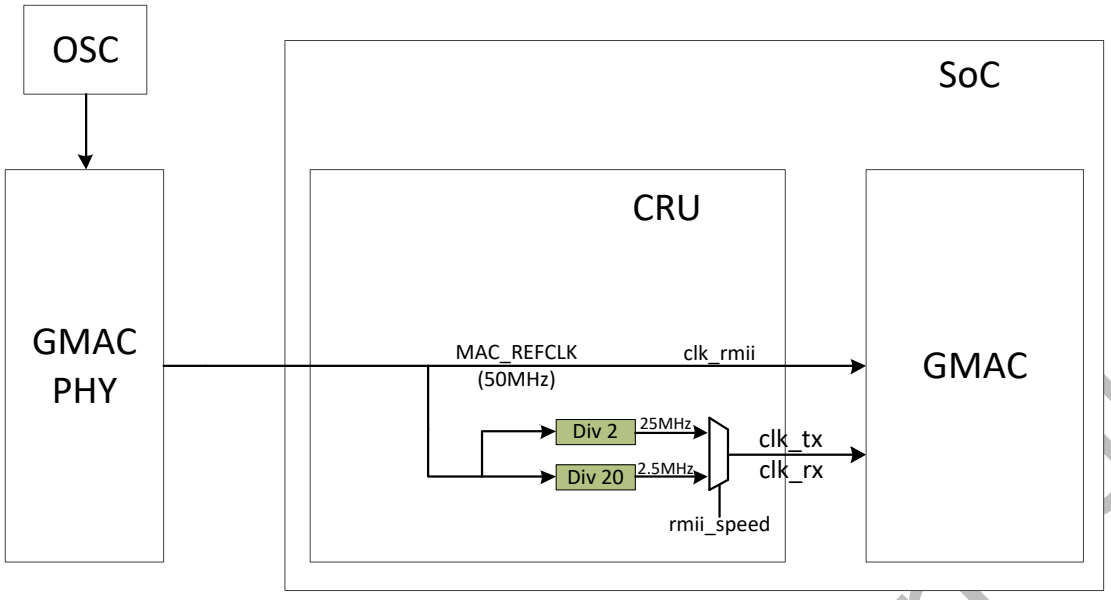

Fig. 38-11 RMII Clock Architecture When Clock Source From PHY

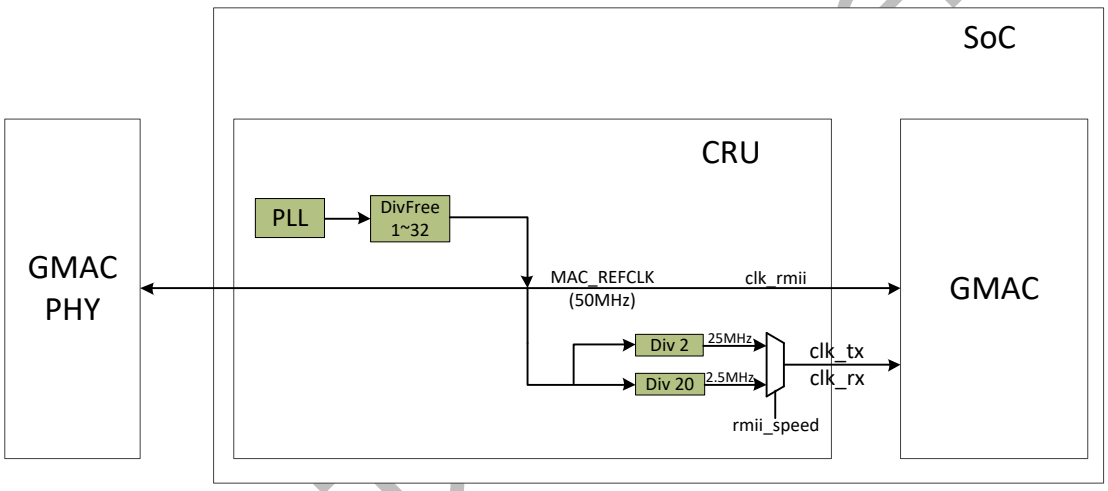

Fig. 38-12 RMII Clock Architecture When Clock Source From CRU

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Chapter 39 Mobile Storage Host Controller (SDMMC&EMMC)

39.1 Overview

The Mobile Storage Host Controller is designed to support Secure Digital memory (SD-max version 3.01) with 1 bits or 4 bits data width, Multimedia Card (MMC-max version 4.51) with 1 bits or 4 bits data width.
The Host Controller is instantiated for SDMMC, EMMC. The interface difference between these instances is shown in "Interface Description".
The Host Controller supports following features:

- Bus Interface Features:
  - Support AMBA AHB interface for master and slave
  - Supports internal DMA interface(IDMAC)
    - Supports 16/32-bit data transfers
    - Single engine used for transmit and receive, which are mutually exclusive
    - Dual-buffer and chained descriptor linked list
    - Each descriptor can transfer up to 4KB of data in chained mode and 8KB of data in dual-buffer mode
    - Programmable burst size for optimal host bus utilization
  - Support combined single FIFO for both transmit and receive operations
  - Support FIFO size of 256x32
  - Support FIFO over-run and under-run prevention by stopping card clock
- Card Interface Features:
  - Support secure digital memory protocol commands
  - Support secure digital I/O protocol commands
  - Support Multimedia Card protocol commands
  - Support command completion signal and interrupts to host
  - Support CRC generation and error detection
  - Support programmable baud rate
  - Support power management and power switch
  - Support write protection
  - Support hardware reset
  - Support SDIO interrupts in 1-bit and 4-bit modes
  - Support 4-bit mode in SDIO3.0
  - Support SDIO suspend and resume operation
  - Support SDIO read wait
  - Support block size of 1 to 65,535 bytes
  - Support 1-bit and 4-bit SDR modes
  - Supports 4-bit DDR
  - Support boot in 1-bit and 4-bit SDR modes
- Clock Interface Features:
  - Support 0/90/180/270-degree phase shift operation for sample clock (cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock(cclk_in) respectively
  - Support phase tuning using delay line for sample clock(cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock (cclk_in) respectively.
  - The max number of delay element is 128. The average delay for every delay element is 29ps~61ps, the total delay is 3.7ns~7.8ns, varies with VT.

39.2 Block Diagram

The controller consists of the following main functional blocks.

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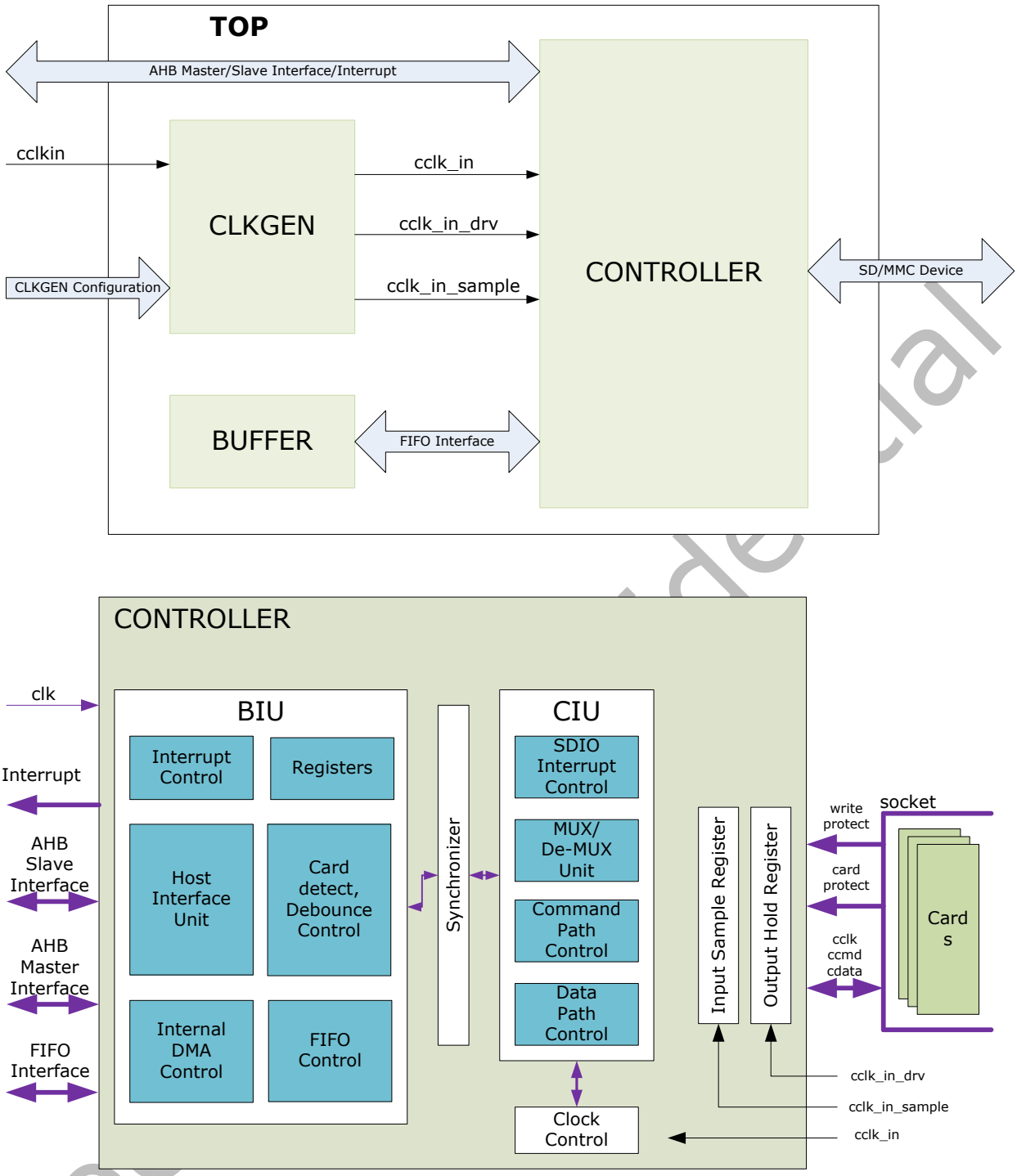

Fig.39-1 Mobile Storage Host Control Block Diagram

- Clock Generate Unit (CLKGEN): Generates card interface clock cclk_in/ cclk_sample/cclk_drv based on cclkin and configuration information.
  - cclkin: original clock
  - cclk_in: functional clock
  - cclk_sample: sample clock
  - cclk_drv: driver clock
- Asynchronous dual-port memory (BUFFER): Use a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, and the other port is connected to the card clock.
- Bus Interface Unit (BIU): Provides AMBA AHB interfaces for register and data read/write.
- Card Interface Unit (CIU): Takes care of the SD/MMC protocols and provides clock management.

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39.3 Function Description

39.3.1 Bus Interface Unit

The Bus Interface Unit provides the following functions:

- Host interface
- Interrupt control
- Register access
- External FIFO access

39.3.1.1 Host Interface Unit

The Host Interface Unit is an AHB slave interface, which provides the interface between the SD/MMC card and the host bus.

39.3.1.2 Register Unit

The register unit is part of the bus interface unit; it provides read and write access to the registers.

All registers reside in the Bus Interface Unit clock domain. When a command is sent to a card by setting the start_bit, which is bit[31] of the SDMMC_CMD register, all relevant registers needed for the CIU operation are transferred to the CIU block. During this time, the registers that are transferred from the BIU to the CIU should not be written. The software should wait for the hardware to clear the start bit before writing to these registers again. The register unit has a hardware locking feature to prevent illegal writes to registers. The lock is necessary in order to avoid metastability violations, both because the host and card clock domains are different and to prevent illegal software operations.

Once a command start is issued by setting the start_bit of the SDMMC_CMD register, the following registers cannot be reprogrammed until the command is accepted by the card interface unit:

- SDMMC_CMD
- SDMMC_CMDARG
- SDMMC_BYTCNT
- SDMMC_BLKSIZ
- SDMMC_CLKDIV
- SDMMC_CLKENA
- SDMMC_CLKSRC
- SDMMC_TMOUT
- SDMMC_CTYPE

The hardware resets the start_bit once the CIU accepts the command. If a host write to any of these registers is attempted during this locked time, then the write is ignored and the hardware lock error bit is set in the raw interrupt status register. Additionally, if the interrupt is enabled and not masked for a hardware lock error, then an interrupt is sent to the host.

When the Card Interface Unit is in an idle state, it typically takes the following number of clocks for the command handshake, where clk is the BIU clock and cclk_in is the CIU clock:
3 (clk) + 3 (cclk_in)

Once a command is accepted, you can send another command to the CIU-which has a one-deep command queue-under the following conditions:

- If the previous command was not a data transfer command, the new command is sent to the SD/MMC card once the previous command completes.
- If the previous command is a data transfer command and if wait_prvdata_complete (bit[13]) of the SDMMC_CMD register is set for the new command, the new command is sent to the SD/MMC card only when the data transfer completes.

If the wait_prvdata_complete is 0, then the new command is sent to the SD/MMC card as soon as the previous command is sent. Typically, you should use this only to stop or abort a previous data transfer or query the card status in the middle of a data transfer.

39.3.1.3 Interrupt Controller Unit

The interrupt controller unit generates an interrupt that depends on the controller raw interrupt status, the interrupt-mask register, and the global interrupt-enable register bit. Once an interrupt condition is detected, it sets the corresponding interrupt bit in the raw

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interrupt status register SDMMC_RINTSTS. The raw interrupt status bit stays on until the software clears the bit by writing a 1 to the interrupt bit; a 0 leaves the bit untouched.
The interrupt port is an active-high, level-sensitive interrupt. The interrupt port is active only when any bit in the raw interrupt status register is active, the corresponding interrupt mask bit is 1, and the global interrupt enable bit is 1. The interrupt port is registered in order to avoid any combinational glitches.
The int_enable is reset to 0 on power-on, and the interrupt mask bits are set to 32'h0, which masks all the interrupts.

Notes:

Before enabling the interrupt, it is always recommended that you write 32'hffff_ffff to the raw interrupt status register in order to clear any pending unserviced interrupts. When clearing interrupts during normal operation, ensure that you clear only the interrupt bits that you serviced.

The SDIO Interrupts, Receive FIFO Data Request (RXDR), and Transmit FIFO Data Request (TXDR) are set by level-sensitive interrupt sources. Therefore, the interrupt source should be first cleared before you can clear the interrupt bit of the Raw Interrupt register. For example, on seeing the Receive FIFO Data Request (RXDR) interrupt, the FIFO should be emptied so that the "FIFO count greater than the RX-Watermark" condition, which triggers the interrupt, becomes inactive. The rest of the interrupts are triggered by a single clock-pulse-width source.

Table 39-1 Bits in Interrupt Status Register

Bits	Interrupt	Description
24	sdio_interrupt	Interrupt from SDIO card. In MMC-Ver3.3-only mode, these bits are always 0.
16	Card no-busy	If card exit busy status, the interrupt happened.
15	End Bit Error (read) / Write no CRC (EBE)	Error in end-bit during read operation, or no data CRC received during write operation. For MMC CMD19, there may be no CRC status returned by the card. Hence, EBE is set for CMD19. The application should not treat this as an error.
14	Auto Command Done (ACD)	Stop/abort commands automatically sent by card unit and not initiated by host; similar to Command Done (CD) interrupt. Recommendation: Software typically need not enable this for non CE-ATA accesses; Data Transfer Over (DTO) interrupt that comes after this interrupt determines whether data transfer has correctly competed.
13	Start Bit Error (SBE)	Error in data start bit when data is read from a card. In 4-bit mode, if DAT[0] line indicates start bit-that is, 0-and any of the other data bits do not have start bit, then this error is set. Busy Complete Interrupt when data is written to the card. This interrupt is generated after completion of busy driven by the card after the last data block is written into the card.
12	Hardware Locked write Error (HLE)	During hardware-lock period, write attempted to one of locked registers. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
11	FIFO Underrun/ Overrun Error (FRUN)	Host tried to push data when FIFO was full, or host tried to read data when FIFO was empty. Typically this should not happen, except due to error in software. Card unit never pushes data into FIFO when FIFO is full, and pop data when FIFO is empty. If IDMAC is enabled, FIFO under-run/over-run can occur due to a programming error on MSIZE and

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Bits	Interrupt	Description
		watermark values in SDMMC_FIFOTH register.
10	Data Starvation by Host Timeout (HTO)	To avoid data loss, card clock out is stopped if FIFO is empty when writing to card, or FIFO is full when reading from card. Whenever card clock is stopped to avoid data loss, data-starvation timeout counter is started with data-timeout value. This interrupt is set if host does not fill data into FIFO during write to card, or does not read from FIFO during read from card before timeout period. Even after timeout, card clock stays in stopped state, with CIU state machines waiting. It is responsibility of host to push or pop data into FIFO upon interrupt, which automatically restarts cclk_out and card state machines. Even if host wants to send stop/abort command, it still needs to ensure it has to push or pop FIFO so that clock starts in order for stop/abort command to send on command signal along with data that is sent or received on data line.
9	Data Read Timeout (DRTO)	In Normal functioning mode: Data read timeout (DRTO) Data timeout occurred. Data Transfer Over (DTO) also set if data timeout occurs. In Boot Mode: Boot Data Start (BDS) When set, indicates that Host Controller has started to receive boot data from the card. A write to this register with a value of 1 clears this interrupt.
8	Response Timeout (RTO)	In normal functioning mode: Response timeout (RTO) Response timeout occurred. Command Done (CD) also set if response timeout occurs. If command involves data transfer and when response times out, no data transfer is attempted by Host Controller. In Boot Mode: Boot Ack Received (BAR) When expect_boot_ack is set, on reception of a boot acknowledge pattern—0-1-0—this interrupt is asserted. A write to this register with a value of 1 clears this interrupt.
7	Data CRC Error (DCRC)	Received Data CRC does not match with locally-generated CRC in CIU. Can also occur if the Write CRC status is incorrectly sampled by the Host.
6	Response CRC Error (RCRC)	Response CRC does not match with locally-generated CRC in CIU.
5	Receive FIFO Data Request (RXDR)	Interrupt set during read operation from card when FIFO level is greater than Receive-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode: pop RX_WMark + 1 data from FIFO.
4	Transmit FIFO Data Request (TXDR)	Interrupt set during write operation to card when FIFO level reaches less than or equal to Transmit-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode: if (pending_bytes > (FIFO_DEPTH - TX_WMark))

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Bits	Interrupt	Description
		push (FIFO_DEPTH - TX_WMark) data into FIFO else push pending_bytes data into FIFO
3	Data Transfer Over (DTO)	Indicates Data transfer completed. Though on detection of errors-Start Bit Error, Data CRC error, and so on, DTO may or may not be set; the application must issue CMD12, which ensures that DTO is set. Recommendation: In non-DMA mode, when data is read from card, on seeing interrupt, host should read any pending data from FIFO. In DMA mode, DMA controllers guarantee FIFO is flushed before interrupt. DTO bit is set at the end of the last data block, even if the device asserts MMC busy after the last data block.
2	Command Done(CD)	Command sent to card and got response from card, even if Response Error or CRC error occurs.
1	Response Error (RE)	Error in received response set if one of following occurs: ● Transmission bit != 0 ● Command index mismatch ● End-bit != 1
0	Card-Detect (CDT)	When one or more cards inserted or removed, this interrupt occurs. Software should read card-detect register to determine current card status. Recommendation: After power-on and before enabling interrupts, software should read card detect register and store it in memory. When interrupt occurs, it should read card detect register and compare it with value stored in memory to determine which card(s) were removed/inserted. Before exiting ISR, software should update memory with new card-detect value.

39.3.1.4 FIFO Controller Unit

The FIFO controller interfaces the external FIFO to the host interface and the card controller unit. When FIFO overrun and under-run conditions occur, the card clock stops in order to avoid data loss.

The FIFO uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock(clk), and the second port is connected to the card clock(cclk_in).

39.3.2 Card Interface Unit

The Card Interface Unit (CIU) interfaces with the Bus Interface Unit (BIU) and the external devices. The host writes command parameters to the BIU control registers, and these parameters are then passed to the CIU. Depending on control register values, the CIU generates SD/MMC command and data traffic on a selected card bus according to SD/MMC protocol. The Host Controller accordingly controls the command and data path.

The following software restrictions should be met for proper CIU operation:

- Only one data transfer command can be issued at a time.
- During an open-ended card write operation, if the card clock is stopped because the FIFO is empty, the software must first fill the data into the FIFO and start the card clock. It can then issue only a stop/abort command to the card.
- When issuing card reset commands (CMD0, CMD15 or CMD52_reset) while a card data

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transfer is in progress, the software must set the stop_abort_cmd bit in the SDMMC_CMD register so that the Host Controller can stop the data transfer after issuing the card reset command.
- When the data end bit error is set in the SDMMC_RINTSTS register, the Host Controller does not guarantee SDIO interrupts. The software should ignore the SDIO interrupts and issue the stop/abort command to the card, so that the card stops sending the read data.
- If the card clock is stopped because the FIFO is full during a card read, the software should read at least two FIFO locations to start the card clock.

The CIU block consists of the following primary functional blocks:
- Command path
- Data path
- SDIO interrupt control
- Clock control
- Error detection

39.3.2.1 Command Path

The command path performs the following functions:
- Loads clock parameters
- Loads card command parameters
- Sends commands to card bus (ccmd_out line)
- Receives responses from card bus (ccmd_in line)
- Sends responses to BIU
- Drives the P-bit on command line

A new command is issued to the Host Controller by programming the BIU registers and setting the start_cmd bit in the SDMMC_CMD register. The BIU asserts start_cmd, which indicates that a new command is issued to the SD/MMC device. The command path loads this new command (command, command argument, timeout) and sends acknowledge to the BIU by asserting cmd_taken.

Once the new command is loaded, the command path state machine sends a command to the device bus-including the internally generated CRC7-and receives a response, if any. The state machine then sends the received response and signals to the BIU that the command is done, and then waits for eight clocks before loading a new command.

Load Command Parameters

One of the following commands or responses is loaded in the command path:
- New command from BIU – When start_cmd is asserted, then the start_cmd bit is set in the SDMMC_CMD register.
- Internally generated auto-stop command – When the data path ends, the stop command request is loaded.
- IRQ response with RCA 0x000 – When the command path is waiting for an IRQ response from the MMC card and a "send irq response" request is signaled by the BIU, then the send_irq_response bit is set in the SDMMC_CTRL register.

Loading a new command from the BIU in the command path depends on the following SDMMC_CMD register bit settings:
- update_clock_registers_only – If this bit is set in the SDMMC_CMD register, the command path updates only the clock enable, clock divider, and clock source registers. If this bit is not set, the command path loads the command, command argument, and timeout registers; it then starts processing the new command.
- wait_prvdata_complete – If this bit is set, the command path loads the new command under one of the following conditions:
  - Immediately, if the data path is free (that is, there is no data transfer in progress), or if an open-ended data transfer is in progress (byte_count = 0).
  - After completion of the current data transfer, if a predefined data transfer is in progress.

Send Command and Receive Response

Once a new command is loaded in the command path, update_clock_registers_only bit is unset – the command path state machine sends out a command on the device bus; the command path state machine is illustrated in following figure.

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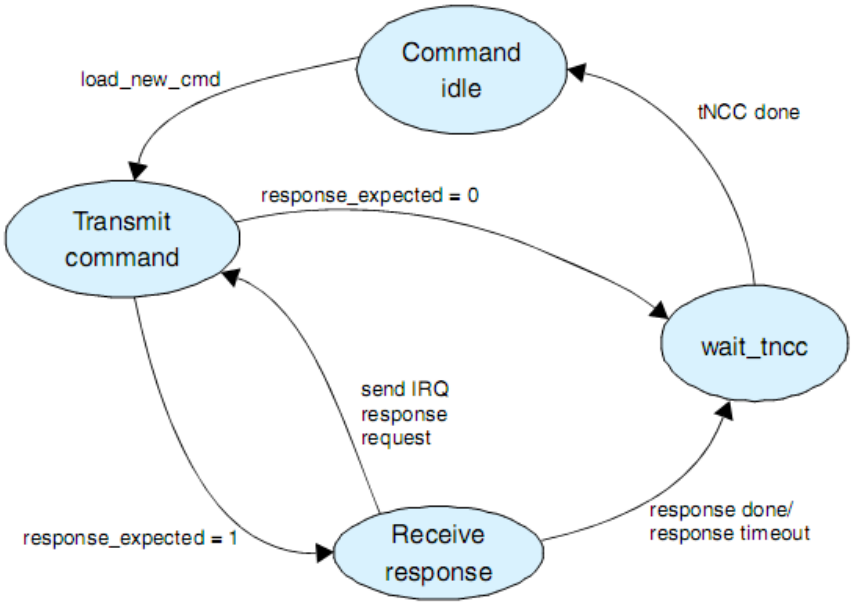

Fig. 39-2 Host Controller Command Path State Machine

The command path state machine performs the following functions, according to SDMMC_CMD register bit values:

- send_initialization – Initialization sequence of 80 clocks is sent before sending the command.
- response_expected – Response is expected for the command. After the command is sent out, the command path state machine receives a 48-bit or 136-bit response and sends it to the BIU. If the start bit of the card response is not received within the number of clocks programmed in the timeout register, then the response timeout and command done bit is set in the Raw Interrupt Status register as a signal to the BIU. If the response-expected bit is not set, the command path sends out a command and signals a response done to the BIU; that is, the command done bit is set in the Raw Interrupt Status register.
- response_length – If this bit is set, a 136-bit response is received; if it is not set, a 48-bit response is received.
- check_response_crc – If this bit is set, the command path compares CRC7 received in the response with the internally-generated CRC7. If the two do not match, the response CRC error is signaled to the BIU; that is, the response CRC error bit is set in the Raw Interrupt Status register SDMMC_RINTSTS.

Send Response to BIU

If the response_expected bit is set in the SDMMC_CMD register, the received response is sent to the BIU. The Response0 register is updated for a short response, and the Response3, Response2, Response1, and Response0 registers are updated on a long response, after which the Command Done bit is set. If the response is for an auto_stop command sent by the CIU, the response is saved in the Response1 register, after which the Auto Command Done bit is set.

Additionally, the command path checks for the following:

- Transmission bit = 0
- Command index matches command index of the sent command
- End bit = 1 in received card response

The command index is not checked for a 136-bit response or if the check_response_crc bit is unset. For a 136-bit response and reserved CRC 48-bit responses, the command index is reserved-that is, 111111.

Polling Command Completion Signal

The device generates the Command Completion Signal in order to notify the host controller of the normal command completion or command termination.

Command Completion Signal Detection and Interrupt to Host Processor

If the ccs_expected bit is set in the SDMMC_CMD register, the Command Completion Signal (CCS) from the device is indicated by setting the Data Transfer Over (DTO) bit in the

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SDMMC_RINTSTS register. The Host Controller generates a Data Transfer Over (DTO) interrupt if this interrupt is not masked.

Command Completion Signal Timeout

If the command expects a CCS from the device—if the ccs_expected bit is set in the SDMMC_CMD register—the command state machine waits for the CCS and remains in a wait_CCSS state. If the device fails to send out the CCS, the host software should implement a timeout mechanism to free the command and data path. The host controller does not implement a hardware timer; it is the responsibility of the host software to maintain a software timer.

In the event of a CCS timeout, the host should issue a CCSD by setting the send_ccsd bit in the CTRL register. The host controller command state machine sends the CCSD to the device and exits to an idle state. After sending the CCSD, the host should also send a CMD12 to the device in order to abort the outstanding command.

Send Command Completion Signal Disable

If the send_ccsd bit is set in the SDMMC_CTRL register, the host sends a Command Completion Signal Disable (CCSD) pattern on the CMD line. The host can send the CCSD while waiting for the CCS or after a CCS timeout happens.

After sending the CCSD pattern, the host sets the Command Done (CD) bit in SDMMC_RINTSTS and also generates an interrupt to the host if the Command Done interrupt is not masked.

39.3.2.2 Data Path

The data path block pops the data FIFO and transmits data on cdata_out during a write data transfer, or it receives data on cdata_in and pushes it into the FIFO during a read data transfer. The data path loads new data parameters—that is, data expected, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers—whenever a data transfer command is not in progress.

If the data_expected bit is set in the SDMMC_CMD register, the new command is a data transfer command and the data path starts one of the following:

- Transmit data if the read/write bit = 1
- Data receive if read/write bit = 0

Data Transmit

The data transmit state machine, illustrated in following figure, starts data transmission two clocks after a response for the data write command is received; this occurs even if the command path detects a response error or response CRC error. If a response is not received from the card because of a response timeout, data is not transmitted. Depending upon the value of the transfer_mode bit in the SDMMC_CMD register, the data transmit state machine puts data on the card data bus in a stream or in block(s).

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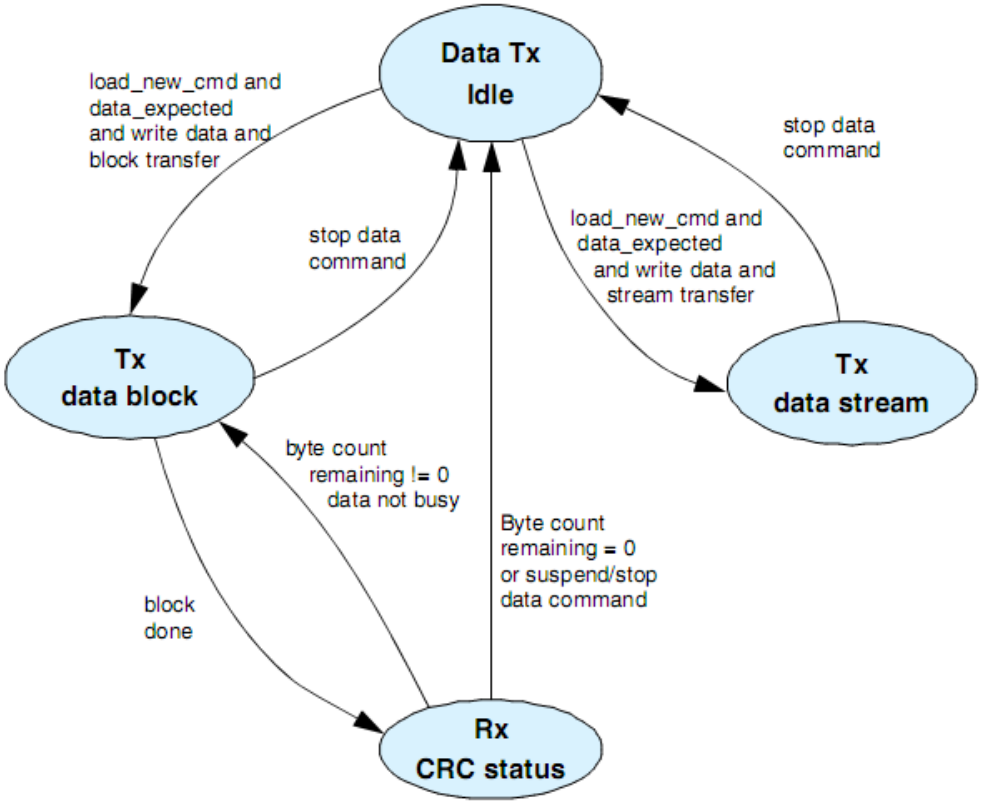

Fig. 39-3 Host Controller Data Transmit State Machine

Stream Data Transmit

If the transfer_mode bit in the SDMMC_CMD register is set to 1, it is a stream-write data transfer. The data path pops the FIFO from the BIU and transmits in a stream to the card data bus. If the FIFO becomes empty, the card clock is stopped and restarted once data is available in the FIFO.

If the byte_count register is programmed to 0, it is an open-ended stream-write data transfer. During this data transfer, the data path continuously transmits data in a stream until the host software issues a stop command. A stream data transfer is terminated when the end bit of the stop command and end bit of the data match over two clocks.

If the byte_count register is programmed with a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated and loaded in the command path when the end bit of the stop command occurs after the last byte of the stream write transfer matches.

This data transfer can also terminate if the host issues a stop command before all the data bytes are transferred to the card bus.

Single Block Data

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the byte_count register value is equal to the value of the block_size register, a single-block write-data transfer occurs. The data transmit state machine sends data in a single block, where the number of bytes equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set for a 1-bit, 4-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted for 1, 4, or 8 data lines, respectively.

After a single data block is transmitted, the data transmit state machine receives the CRC status from the card and signals a data transfer to the BIU; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register.

Additionally, if the start bit of the CRC status is not received by two clocks after the end of the data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register.

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Multiple Block Data

A multiple-block write-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value in the byte_count register is not equal to the value of the block_size register. The data transmit state machine sends data in blocks, where the number of bytes in a block equals the block size, including the internally-generated CRC16. If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to 1-bit, 4-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted on 1, 4, or 8 data lines, respectively.

After one data block is transmitted, the data transmit state machine receives the CRC status from the card. If the remaining byte_count becomes 0, the data path signals to the BIU that the data transfer is done; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If the remaining data bytes are greater than 0, the data path state machine starts to transmit another data block.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register, and continues further data transmission until all the bytes are transmitted.

Additionally, if the CRC status start bit is not received by two clocks after the end of a data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register; further data transfer is terminated.

If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated during the transfer of the last data block, where no extra bytes are transferred to the card. The end bit of the stop command may not exactly match the end bit of the CRC status in the last data block.

If the block size is less than 4, 16, or 32 for card data widths of 1 bit, 4 bits, respectively, the data transmit state machine terminates the data transfer when all the data is transferred, at which time the internally generated stop command is loaded in the command path.

If the byte_count is 0 – the block size must be greater than 0 – it is an open-ended block transfer. The data transmit state machine for this type of data transfer continues the block-write data transfer until the host software issues a stop or abort command.

Data Receive

The data-receive state machine, illustrated in following figure, receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or response CRC error. If a response is not received from the card because a response timeout occurs, the BIU does not receive a signal that the data transfer is complete; this happens if the command sent by the Host Controller is an illegal operation for the card, which keeps the card from starting a read data transfer.

If data is not received before the data timeout, the data path signals a data timeout to the BIU and an end to the data transfer done. Based on the value of the transfer_mode bit in the SDMMC_CMD register, the data-receive state machine gets data from the card data bus in a stream or block(s).

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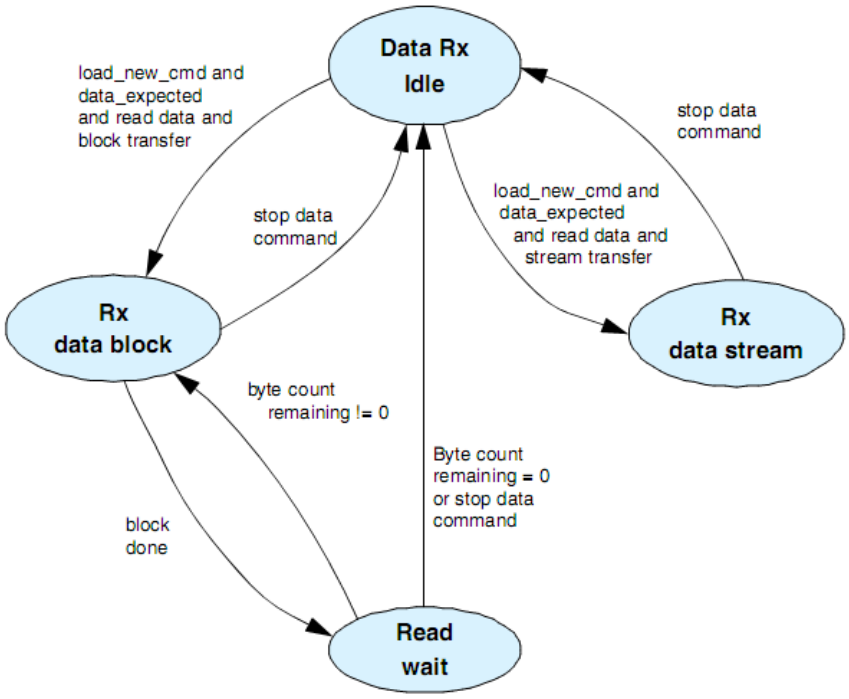

Fig. 39-4 Host Controller Data Receive State Machine

Stream Data Read

A stream-read data transfer occurs if the transfer_mode bit in the SDMMC_CMD register equals 1, at which time the data path receives data from the card and pushes it to the FIFO. If the FIFO becomes full, the card clock stops and restarts once the FIFO is no longer full.

An open-ended stream-read data transfer occurs if the byte_count register equals 0. During this type of data transfer, the data path continuously receives data in a stream until the host software issues a stop command. A stream data transfer terminates two clock cycles after the end bit of the stop command.

If the byte_count register contains a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, a stop command is internally generated and loaded into the command path, where the end bit of the stop command occurs after the last byte of the stream data transfer is received. This data transfer can terminate if the host issues a stop or abort command before all the data bytes are received from the card.

Single-Block Data Read

A single-block read-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is equal to the value of the block_size register. When a start bit is received before the data times out, data bytes equal to the block size and CRC16 are received and checked with the internally-generated CRC16. If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively. If there is a CRC16 mismatch, the data path signals a data CRC error to the BIU. If the received end bit is not 1, the BIU receives an end-bit error.

Multiple-Block Data Read

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is not equal to the value of the block_size register, it is a multiple-block read-data transfer. The data-receive state machine receives data in blocks, where the number of bytes in a block is equal to the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit data transfer, data is received from 1, 4 data lines, respectively, and CRC16 is separately generated and checked for 1, 4 data lines, respectively.

After a data block is received, if the remaining byte_count becomes 0, the data path signals a data transfer to the BIU.

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If the remaining data bytes are greater than 0, the data path state machine causes another data block to be received. If CRC16 of a received data block does not match the internally-generated CRC16, a data CRC error to the BIU and data reception continue further data transmission until all bytes are transmitted.
Additionally, if the end of a received data block is not 1, data on the data path signals terminate the bit error to the CIU and the data-receive state machine terminates data reception, waits for data timeout, and signals to the BIU that the data transfer is complete.
If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated when the last data block is transferred, where no extra bytes are transferred from the card; the end bit of the stop command may not exactly match the end bit of the last data block.
If the requested block size for data transfers to cards is less than 4, 16, or 32 bytes for 1-bit, 4-bit, or 8-bit data transfer modes, respectively, the data-transmit state machine terminates the data transfer when all data is transferred, at which point the internally-generated stop command is loaded in the command path. Data received from the card after that are then ignored by the data path.
If the byte_count is 0—the block size must be greater than 0—it is an open-ended block transfer. For this type of data transfer, the data-receive state machine continues the block-read data transfer until the host software issues a stop or abort command.

Auto-Stop

The Host Controller internally generates a stop command and is loaded in the command path when the send_auto_stop bit is set in the SDMMC_CMD register.
The software should set the send_auto_stop bit according to details listed in following table.

Table 39-2 Auto-Stop Generation

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count =0 is illegal
MMC	Single-block write	>0	No	Byte count =0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes①	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes①	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count =0 is illegal
SDMEM	Single-block write	>0	No	Byte count =0 illegal
SDMEM	Multiple-block read	0	No	Open-ended multiple block
SDMEM	Multiple-block read	>0	Yes	Auto-stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open-ended multiple block
SDMEM	Multiple-block write	>0	Yes	Auto-stop after all bytes transfer
SDIO	Single-block read	>0	No	Byte count =0 is illegal
SDIO	Single-block write	>0	No	Byte count =0 illegal
SDIO	Multiple-block read	0	No	Open-ended multiple block

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Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
SDIO	Multiple-block read	>0	No	Pre-defined multiple block
SDIO	Multiple-block write	0	No	Open-ended multiple block
SDIO	Multiple-block write	>0	No	Pre-defined multiple block

*①:The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.*

The following list conditions for the auto-stop command.

- Stream read for MMC card with byte count greater than 0 – The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent out when the last byte of data is read from the card and no extra data byte is received. If the byte count is less than 6 (48 bits), a few extra data bytes are received from the card before the end bit of the stop command is sent.
- Stream write for MMC card with byte count greater than 0 - The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent when the last byte of data is transmitted on the card bus and no extra data byte is transmitted. If the byte count is less than 6 (48 bits), the data path transmits the data last in order to meet the above condition.
- Multiple-block read memory for SD card with byte count greater than 0 – If the block size is less than 4 (single-bit data bus), 16 (4-bit data bus), or 32 (8-bit data bus), the auto-stop command is loaded in the command path after all the bytes are read. Otherwise, the top command is loaded in the command path so that the end bit of the stop command is sent after the last data block is received.
- Multiple-block write memory for SD card with byte count greater than 0 – If the block size is less than 3 (single-bit data bus), 12 (4-bit data bus), or 24 (8-bit data bus), the auto-stop command is loaded in the command path after all data blocks are transmitted. Otherwise, the stop command is loaded in the command path so that the end bit of the stop command is sent after the end bit of the CRC status is received.

Precaution for host software during auto-stop – Whenever an auto-stop command is issued, the host software should not issue a new command to the SD/MMC device until the auto-stop is sent by the Host Controller and the data transfer is complete. If the host issues a new command during a data transfer with the auto-stop in progress, an auto-stop command may be sent after the new command is sent and its response is received; this can delay sending the stop command, which transfers extra data bytes. For a stream write, extra data bytes are erroneous data that can corrupt the card data. If the host wants to terminate the data transfer before the data transfer is complete, it can issue a stop or abort command, in which case the Host Controller does not generate an auto-stop command.

39.3.2.3 Non-Data Transfer Commands that Use Data Path

Some non-data transfer commands (non-read/write commands) also use the data path. Following table lists the commands and register programming requirements for them.

Table 39-3 Non-data Transfer Commands and Requirements

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
SDMMC_CMD register programming						
cmd_index	6'h1B	6'h1E	6'h2A	6'h0D	6'h16	6'h33
response_expect	1	1	1	1	1	1
rResponse_length	0	0	0	0	0	0

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Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
check_response_crc	1	1	1	1	1	1
data_expected	1	1	1	1	1	1
read/write	1	0	1	0	0	0
transfer_mode	0	0	0	0	0	0
send_auto_stop	0	0	0	0	0	0
wait_prevdata_complete	0	0	0	0	0	0
stop_abort_cmd	0	0	0	0	0	0
Command Argument register programming						
	stuff bits	32-bit write protect data address	stuff bits	stuff bits	stuff bits	stuff bits
Block Size register programming						
	16	4	Num_bytes①	64	4	8
Byte Count register programming						
	16	4	Num_bytes①	64	4	8

①: Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)

39.3.2.4 SDIO Interrupt Control

Interrupts for SD cards are reported to the BIU by asserting an interrupt signal for two clock cycles. SDIO cards signal an interrupt by asserting cdata_in low during the interrupt period; an interrupt period for the selected card is determined by the interrupt control state machine. An interrupt period is always valid for non-active or non-selected cards, and 1-bit data mode for the selected card. An interrupt period for a wide-bus active or selected card is valid for the following conditions:

- Card is idle
- Non-data transfer command in progress
- Third clock after end bit of data block between two data blocks
- From two clocks after end bit of last data until end bit of next data transfer command

Bear in mind that, in the following situations, the controller does not sample the SDIO interrupt of the selected card when the card data width is 4 bits. Since the SDIO interrupt is level-triggered, it is sampled in a further interrupt period and the host does not lose any SDIO interrupt from the card.

- Read/Write Resume – The CIU treats the resume command as a normal data transfer command. SDIO interrupts during the resume command are handled similarly to other data commands. According to the SDIO specification, for the normal data command the interrupt period ends after the command end bit of the data command; for the resume command, it ends after the response end bit. In the case of the resume command, the Controller stops the interrupt sampling period after the resume command end bit, instead of stopping after the response end bit of the resume command.

Suspend during read transfer – If the read data transfer is suspended by the host, the host sets the abort_read_data bit in the controller to reset the data state machine. In the CIU, the SDIO interrupts are handled such that the interrupt sampling starts after the abort_read_data bit is set by the host. In this case the controller does not sample SDIO interrupts between the period from response of the suspend command to setting the abort_read_data bit, and starts sampling after setting the abort_read_data bit.

39.3.2.5 Clock Control

The clock control block provides different clock frequencies required for SD/MMC cards. The cclk_in signal is the source clock (cclk_in >= card max operating frequency) for clock divider of the clock control block. This source clock (cclk_in) is used to generate different card clock frequencies (cclk_out). The card clock can have different clock frequencies, since the card can be a low-speed card or a full-speed card. The Host Controller provides one clock signal (cclk_out).

The clock frequency of a card depends on the following clock control registers:

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- Clock Divider register – Internal clock dividers are used to generate different clock frequencies required for card. The division factor for each clock divider can be programmed by writing to the Clock Divider register. A value of 0 represents a clock-divider bypass, a value of 1 represents a divide by 2.
- Clock Control register – cclk_out can be enabled or disabled for each card under the following conditions:
  - clk_enable – cclk_out for a card is enabled if the clk_enable bit for a card in the Clock Control register is programmed (set to 1) or disabled (set to 0).
  - Low-power mode – Low-power mode of a card can be enabled by setting the low-power mode bit of the Clock Control register to 1. If low-power mode is enabled to save card power, the cclk_out is disabled when the card is idle for at least 8 card clock cycles. It is enabled when a new command is loaded and the command path goes to a non-idle state.

Additionally, cclk_out is disabled when an internal FIFO is full – card read (no more data can be received from card) – or when the FIFO is empty – card write (no data is available for transmission). This helps to avoid FIFO overrun and underrun conditions. It is used by the command and data path to qualify cclk_in for driving outputs and sampling inputs at the programmed clock frequency for the selected card, according to the Clock Divider and Clock Source register values.

Under the following conditions, the card clock is stopped or disabled, along with the active clk_en, for the selected card:

- Clock can be disabled by writing to Clock Enable register (clk_en bit = 1).
- If low-power mode is selected and card is idle, or not selected for 8 clocks.
- FIFO is full and data path cannot accept more data from the card and data transfer is incomplete –to avoid FIFO overrun.

FIFO is empty and data path cannot transmit more data to the card and data transfer is incomplete – to avoid FIFO underrun.

39.3.2.6 Error Detection

- Response
  - Response timeout – Response expected with response start bit is not received within programmed number of clocks in timeout register.
  - Response CRC error – Response is expected and check response CRC requested; response CRC7 does not match with the internally-generated CRC7.
  - Response error – Response transmission bit is not 0, command index does not match with the command index of the send command, or response end bit is not 1.
- Data transmit
  - No CRC status – During a write data transfer, if the CRC status start bit is not received two clocks after the end bit of the data block is sent out, the data path does the following:
    - Signals no CRC status error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to the BIU
  - Negative CRC – If the CRC status received after the write data block is negative (that is, not 010), a data CRC error is signaled to the BIU and further data transfer is continued.
  - Data starvation due to empty FIFO – If the FIFO becomes empty during a write data transmission, or if the card clock is stopped and the FIFO remains empty for data timeout clocks, then a data-starvation error is signaled to the BIU and the data path continues to wait for data in the FIFO.
- Data receive
  - Data timeout – During a read-data transfer, if the data start bit is not received before the number of clocks that were programmed in the timeout register, the data path does the following:
    - Signals data-timeout error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to BIU
  - Data start bit error – During a 4-bit or 8-bit read-data transfer, if the all-bit data

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line does not have a start bit, the data path signals a data start bit error to the BIU and waits for a data timeout, after which it signals that the data transfer is done.

- Data CRC error – During a read-data-block transfer, if the CRC16 received does not match with the internally generated CRC16, the data path signals a data CRC error to the BIU and continues further data transfer.
- Data end-bit error – During a read-data transfer, if the end bit of the received data is not 1, the data path signals an end-bit error to the BIU, terminates further data transfer, and signals to the BIU that the data transfer is done.

Data starvation due to FIFO full – During a read data transmission and when the FIFO becomes full, the card clock is stopped. If the FIFO remains full for data timeout clocks, a data starvation error is signaled to the BIU (Data Starvation by Host Timeout bit is set in SDMMC_RINTSTS register) and the data path continues to wait for the FIFO to start to empty.

39.3.3 Internal Direct Memory Access Controller (IDMAC)

The Internal Direct Memory Access Controller (IDMAC) has a Control and Status Register (CSR) and a single Transmit/Receive engine, which transfers data from host memory to the device port and vice versa. The controller utilizes a descriptor to efficiently move data from source to destination with minimal Host CPU intervention. You can program the controller to interrupt the Host CPU in situations such as data Transmit and Receive transfer completion from the card, as well as other normal or error conditions.

The IDMAC and the Host driver communicate through a single data structure. CSR addresses 0x80 to 0x98 are reserved for host programming.

The IDMAC transfers the data received from the card to the Data Buffer in the Host memory, and it transfers Transmit data from the Data Buffer in the Host memory to the FIFO. Descriptors that reside in the Host memory act as pointers to these buffers.

A data buffer resides in physical memory space of the Host and consists of complete data or partial data. Buffers contain only data, while buffer status is maintained in the descriptor. Data chaining refers to data that spans multiple data buffers. However, a single descriptor cannot span multiple data.

A single descriptor is used for both reception and transmission. The base address of the list is written into Descriptor List Base Address Register (SDMMC_DBADDR @0x88). A descriptor list is forward linked. The Last Descriptor can point back to the first entry in order to create a ring structure. The descriptor list resides in the physical memory address space of the Host. Each descriptor can point to a maximum of two data buffers.

39.3.3.1 IDMAC CSR Access

When an IDMAC is introduced, an additional CSR space resides in the IDMAC that controls the IDMAC functionality. The host accesses the new CSR space in addition to the existing control register set in the BIU. The IDMAC CSR primarily contains descriptor information. For a write operation to the CSR, the respective CSR logic of the IDMAC and BIU decodes the address before accepting. For a read operation from the CSR, the appropriate CSR read path is enabled.

You can enable or disable the IDMAC operation by programming bit[25] in the SDMMC_CTRL register of the BIU. This allows the data transfer by accessing the slave interface on the AMBA bus if the IDMAC is present but disabled. When IDMAC is enabled, the FIFO cannot be accessed through the slave interface.

39.3.3.2 Descriptors

- Descriptor structures

The IDMAC uses these types of descriptor structures:

- Dual-Buffer Structure – The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (SDMMC_BMOD @0x80).

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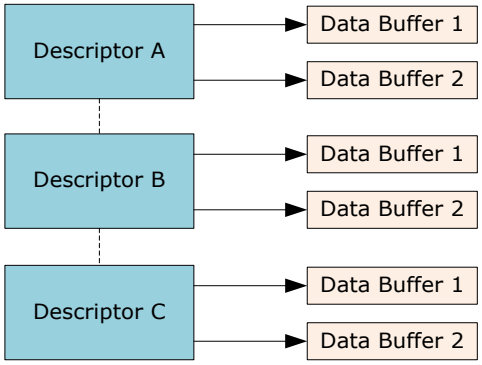

Fig. 39-5 Dual-Buffer Descriptor Structure

- Chain Structure – Each descriptor points to a unique buffer and the next descriptor.

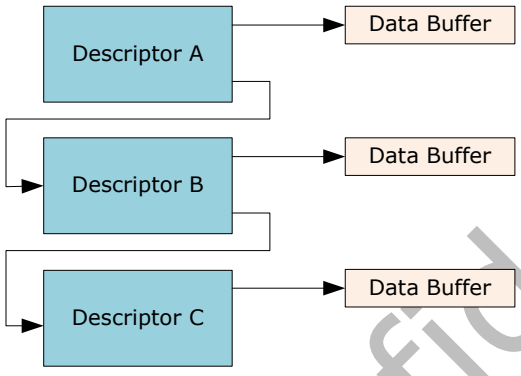

Fig. 39-6 Chain Descriptor Structure

- Descriptor formats

Following figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit AHB data buses. Each descriptor contains 16 bytes of control and status information. DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, DES3 to denote [127:96] bits.

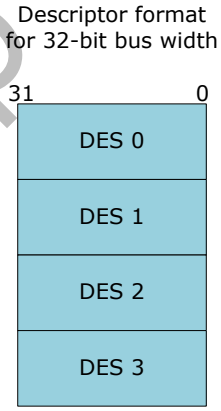

Fig. 39-7 Descriptor Formats for 32-bit AHB Address Bus Width

- The DES0 element in the IDMAC contains control and status information.

Table 39-4 Bits in IDMAC DES0 Element

Bit	Name	Description
31	OWN	When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the Host. The IDMAC clears this bit when it completes the data transfer.
30	Card Error Summary (CES)	These error bits indicate the status of the transaction to or from the card. These bits are also present in SDMMC_RINTSTS Indicates the logical OR of the following bits:

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Bit	Name	Description
		● EBE: End Bit Error ● RTO: Response Time out ● RCRC: Response CRC ● SBE: Start Bit Error ● DRTO: Data Read Timeout ● DCRC: Data CRC for Receive ● RE: Response Error
29:6	Reserved	-
5	End of Ring (ER)	When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.
4	Second Address Chained (CH)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.
3	First Descriptor (FS)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.
2	Last Descriptor (LD)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed to by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	Disable Interrupt on Completion (DIC)	When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in the buffer pointed to by this descriptor.
0	Reserved	-

■ The DES1 element contains the buffer size.

Table 39-5 Bits in IDMAC DES1 Element

Bit	Name	Description
31:26	Reserved	-
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

■ The DES2 element contains the address pointer to the data buffer.

Table 39-6 Bits in IDMAC DES2 Element

Bit	Name	Description
31:26	Reserved	
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the

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Bit	Name	Description
		buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 39-7 Bits in IDMAC DES3 Element

Bit	Name	Description
31:0	Buffer Address Pointer 2/ Next Descriptor Address (BAP2)	These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor address pointer must be bus-width aligned.

39.3.3.3 Initialization

IDMAC initialization occurs as follows:

1) Write to IDMAC Bus Mode Register—SDMMC_BMOD to set Host bus access parameters.
2) Write to IDMAC Interrupt Enable Register—SDMMC_IDINTEN to mask unnecessary interrupt causes.
3) The software driver creates either the Transmit or the Receive descriptor list. Then it writes to IDMAC Descriptor List Base Address Register (SDMMC_DBADDR), providing the IDMAC with the starting address of the list.
4) The IDMAC engine attempts to acquire descriptors from the descriptor lists.

- Host Bus Burst Access

The IDMAC attempts to execute fixed-length burst transfers on the AHB Master interface if configured using the FB bit of the IDMAC Bus Mode register. The maximum burst length is indicated and limited by the PBL field. The descriptors are always accessed in the maximum possible burst-size for the 16-bytes to be read— 16*8/bus-width.

The IDMAC initiates a data transfer only when sufficient space to accommodate the configured burst is available in the FIFO or the number of bytes to the end of data, when less than the configured burst-length.

The IDMAC indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length bursts, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise, in no fixed-length bursts, it transfers data using INCR (undefined length) and SINGLE transactions.

- Host Data Buffer Alignment

The Transmit and Receive data buffers in host memory must be aligned, depending on the data width.

- Buffer Size Calculations

The driver knows the amount of data to transmit or receive. For transmitting to the card, the IDMAC transfers the exact number of bytes to the FIFO, indicated by the buffer size field of DES1.

If a descriptor is not marked as last-LS bit of DES0-then the corresponding buffer(s) of the descriptor are full, and the amount of valid data in a buffer is accurately indicated by its buffer size field. If a descriptor is marked as last, then the buffer cannot be full, as

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indicated by the buffer size in DES1. The driver is aware of the number of locations that are valid in this case.

- Transmission

IDMAC transmission occurs as follows:

1) The Host sets up the elements (DES0-DES3) for transmission and sets the OWN bit (DES0[31]). The Host also prepares the data buffer.
2) The Host programs the write data command in the SDMMC_CMD register in BIU.
3) The Host will also program the required transmit threshold level (TX_WMark field in SDMMC_FIFOTH register).
4) The IDMAC determines that a write data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the IDMAC enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed transmit threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB Master Interface.
8) The IDMAC fetches the Transmit data from the data buffer in the Host memory and transfers to the FIFO for transmission to card.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data transmission is complete, status information is updated in SDMMC_IDSTS register by setting Transmit Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Reception

IDMAC reception occurs as follows:

1) The Host sets up the element (DES0-DES3) for reception, sets the OWN (DES0[31]).
2) The Host programs the read data command in the SDMMC_CMD register in BIU.
3) The Host will program the required receive threshold level (RX_WMark field in FIFOTH register).
4) The IDMAC determines that a read data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the DMA enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed receive threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB.
8) The IDMAC fetches the data from the FIFO and transfer to Host memory.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data reception is complete, status information is updated in SDMMC_IDSTS register by setting Receive Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Interrupts

Interrupts can be generated as a result of various events. SDMMC_IDSTS register contains

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all the bits that might cause an interrupt. SDMMC_IDINTEN register contains an Enable bit for each of the events that can cause an interrupt.
There are two groups of summary interrupts-Normal and Abnormal-as outlined in SDMMC_IDSTS register. Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal dmac_intr_o is de-asserted.
Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, Receive Interrupt—SDMMC_IDSTS[1] indicates that one or more data was transferred to the Host buffer.
An interrupt is generated only once for simultaneous, multiple events. The driver must scan SDMMC_IDSTS register for the interrupt cause.

39.3.3.4 Variable Delay/Clock Generation Unit

Variable delay mechanism for the cclk_in_drv is useful in order to meet a range of hold-time requirements across modes. Variable delay mechanism for the cclk_in_sample is mandatory and is required to achieve the correct sampling point for data.
The Clock Generation Unit (CLKGEN) includes Phase Shift Unit and Delay Line Unit.
The Phase Shift Unit can shift cclk_in_sample/cclk_in_drv by 0/90/180/270-degree relative to cclk_in. The Delay Line Unit can shift cclk_in_sample/cclk_in_drv step by step in the unit of delay element. The delay value range is 21ps~48ps for every delay element; the max delay element number is 128.
The architecture is as follows.

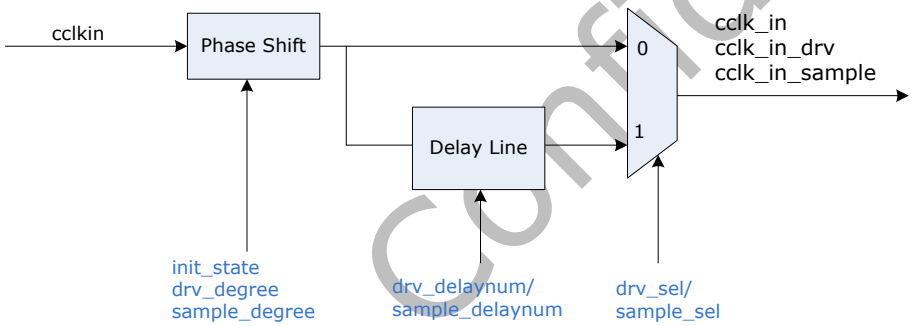

Fig. 39-8 Clock Generation Unit

39.4 Register Description

39.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SDMMC_CTRL	0x0000	W	0x00000000	Control register
SDMMC_PWREN	0x0004	W	0x00000000	Power enable register
SDMMC_CLKDIV	0x0008	W	0x00000000	Clock divider register
SDMMC_CLKSRC	0x000C	W	0x00000000	SD clock source register
SDMMC_CLKENA	0x0010	W	0x00000000	Clock enable register
SDMMC_TMOUT	0x0014	W	0xFFFFFF40	Timeout register
SDMMC_CTYPE	0x0018	W	0x00000000	Card type register
SDMMC_BLKSIZ	0x001C	W	0x00000200	Block size register
SDMMC_BYTCNT	0x0020	W	0x00000200	Byte count register
SDMMC_INTMASK	0x0024	W	0x00000000	Interrupt mask register
SDMMC_CMDARG	0x0028	W	0x00000000	Command argument register
SDMMC_CMD	0x002C	W	0x20000000	Command register
SDMMC_RESP0	0x0030	W	0x00000000	Response register 0
SDMMC_RESP1	0x0034	W	0x00000000	Response register 1
SDMMC_RESP2	0x0038	W	0x00000000	Response register 2
SDMMC_RESP3	0x003C	W	0x00000000	Response register 3
SDMMC_MINTSTS	0x0040	W	0x00000000	Masked interrupt status register
SDMMC_RINTSTS	0x0044	W	0x00000000	Raw interrupt status register

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Name	Offset	Size	Reset Value	Description
SDMMC_STATUS	0x0048	W	0x00000106	Status register
SDMMC_FIFOTH	0x004C	W	0x00FF0000	FIFO threshold register
SDMMC_CDETECT	0x0050	W	0x00000001	Card detect register
SDMMC_WRTPRT	0x0054	W	0x00000000	Write protect register
SDMMC_TCBCNT	0x005C	W	0x00000000	Transferred card byte count register
SDMMC_TBBCNT	0x0060	W	0x00000000	Transferred host to FIFO byte count register
SDMMC_DEBNCE	0x0064	W	0x00FFFFFF	Debounce count register
SDMMC_USRID	0x0068	W	0x00000000	User ID register
SDMMC_VERID	0x006C	W	0x5342270A	Version ID register
SDMMC_HCON	0x0070	W	0x04C434C1	Hardware configuration register
SDMMC_UHSREG	0x0074	W	0x00000000	UHS-1 control register
SDMMC_RSTN	0x0078	W	0x00000001	Hardware reset register
SDMMC_BMOD	0x0080	W	0x00000000	Bus mode register
SDMMC_PLDMND	0x0084	W	0x00000000	Poll demand register
SDMMC_DBADDR	0x0088	W	0x00000000	Descriptor list base address register
SDMMC_IDSTS	0x008C	W	0x00000000	Internal DMAC status register
SDMMC_IDINTEN	0x0090	W	0x00000000	Internal DMAC interrupt enable register
SDMMC_DSCADDR	0x0094	W	0x00000000	Current host descriptor address register
SDMMC_BUFADDR	0x0098	W	0x00000000	Current buffer descriptor address register
SDMMC_CARDTHRCTL	0x0100	W	0x00000000	Card threshold control register
SDMMC_BACKEND_POWER	0x0104	W	0x00000000	Back-end power register
SDMMC_EMMCDDR_REG	0x010C	W	0x00000000	eMMC4.5 DDR start bit detection control register
SDMMC_RDYINT_GEN	0x0120	W	0x00FF0000	Card ready interrupt generation control register
SDMMC_CLKGEN_CON0	0x0130	W	0x00000004	Clock generation control register 0
SDMMC_CLKGEN_CON1	0x0134	W	0x00000000	Clock generation control register 1
SDMMC_MISC_CON	0x0138	W	0x00000000	Miscellaneous control register
SDMMC_FIFO_BASE	0x0200	W	0x00000000	FIFO base address register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

39.4.2 Detail Register Description

SDMMC_CTRL

Address: Operational Base (0xFF480000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	use_internal_dmac Present only for the Internal DMAC configuration; else, it is reserved. 1'b0: The host performs data transfers through the slave interface 1'b1: Internal DMAC used for data transfer
24:12	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	ceata_device_interrupt_status 1'b0: Interrupts not enabled in CE-ATA device 1'b1: Interrupts are enabled in CE-ATA device Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled. If the host enables CE-ATA device interrupt, then software should set this bit.
10	RW	0x0	send_auto_stop_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send internally generated STOP after sending CCSD to CE-ATA device NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together send_auto_stop_ccsd should not be set independent of send_ccsd. When set, the Host Controller automatically sends internally-generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in SDMMC_RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, the Host Controller automatically clears send_auto_stop_ccsd bit.
9	RW	0x0	send_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send Command Completion Signal Disable (CCSD) to CE-ATA device When set, the Host Controller sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, the Host Controller automatically clears send_ccsd bit. It also sets Command Done (CD) bit in SDMMC_RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS.
8	RW	0x0	abort_read_data 1'b0: No change 1'b1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.
7	RW	0x0	send_irq_response 1'b0: No change 1'b1: Send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, software issues CMD40, and the Host Controller waits for interrupt response from MMC card. In meantime, if software wants the Controller to exit waiting for interrupt state, it can set this bit, at which time the Host Controller command state-machine sends CMD40 response on bus and returns to idle state.

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Bit	Attr	Reset Value	Description
6	RW	0x0	read_wait 1'b0: Clear read wait 1'b1: Assert read wait For sending read-wait to SDIO cards.
5	RW	0x0	dma_enable 1'b0: Disable DMA transfer mode 1'b1: Enable DMA transfer mode Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside the controller to prioritize simultaneous host/DMA access.
4	RW	0x0	int_enable Global interrupt enable/disable bit 1'b0: Disable interrupts 1'b1: Enable interrupts The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.
3	RO	0x0	reserved
2	W1C	0x0	dma_reset 1'b0: No change 1'b1: Reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.
1	W1C	0x0	fifo_reset 1'b0: No change 1'b1: Reset to data FIFO to reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.
0	W1C	0x0	controller_reset 1'b0: No change 1'b1: Reset Host Controller To reset Host Controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: a. BIU/CIU interface b. CIU and state machines c. abort_read_data, send_irq_response, and read_wait bits of SDMMC_CTRL register d. start_cmd bit of SDMMC_CMD register Does not affect any registers or DMA interface, or FIFO or controller interrupts.

SDMMC_PWREN

Address: Operational Base (0xFF480000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	power_enable Power on/off switch for the card. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 1'b0: Power off 1'b1: Power on Bit values output to card_power_en port.

SDMMC_CLKDIV

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Address: Operational Base (0xFF480000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_divider0 Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, and so on. The recommended value is 0 or 1.

SDMMC_CLKSRC

Address: Operational Base (0xFF480000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	clk_source Clock divider source. 2'b00: Clock divider 0 The cclk_out is always from clock divider 0, and this register is not implemented.

SDMMC_CLKENA

Address: Operational Base (0xFF480000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	cclk_low_power Low-power control for SD card clock and MMC card clock supported. 1'b0: Non-low-power mode 1'b1: Low-power mode. Stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).
15:1	RO	0x0000	reserved
0	RW	0x0	cclk_enable Clock-enable control for SD card clock and MMC card clock supported. 1'b0: Clock disabled 1'b1: Clock enabled

SDMMC_TMOUT

Address: Operational Base (0xFF480000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RW	0xffffff	data_timeout Value for card data read timeout; same value also used for data starvation by host timeout. Value is in number of card output clock. Note: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.
7:0	RW	0x40	response_timeout Response timeout value. Value is in number of card output clock cclk_out.

SDMMC_CTYPE

Address: Operational Base (0xFF480000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	card_width_8 Indicates if card is 8-bit. 1'b0: Non 8-bit mode 1'b1: 8-bit mode
15:1	RO	0x0000	reserved
0	RW	0x0	card_width Indicates if card is 1-bit or 4-bit. 1'b0: 1-bit mode 1'b1: 4-bit mode

SDMMC_BLKSIZ

Address: Operational Base (0xFF480000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0200	block_size Block size

SDMMC_BYTCNT

Address: Operational Base (0xFF480000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	byte_count Number of bytes to be transferred; should be integer multiple of block size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.

SDMMC_INTMASK

Address: Operational Base (0xFF480000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sdio_int_mask 1'b0: SDIO interrupt not masked 1'b1: SDIO interrupt masked
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_mask 1'b0: Data no busy interrupt not masked 1'b1: Data no busy interrupt masked

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_mask Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_CMDARG

Address: Operational Base (0xFF480000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_arg Value indicates command argument to be passed to card

SDMMC_CMD

Address: Operational Base (0xFF480000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	start_cmd Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD/MMC cards, Command Done bit is set in raw interrupt register.
30	RO	0x0	reserved
29	RW	0x1	use_hold_reg Use hold register. 1'b0: CMD and DATA sent to card bypassing hold register 1'b1: CMD and DATA sent to card through the hold register
28	RW	0x0	volt_switch Voltage switch bit. 1'b0: No voltage switching 1'b1: Voltage switching enabled; must be set for CMD11 only.
27	RW	0x0	boot_mode Boot mode selection. 1'b0: Mandatory boot operation 1'b1: Alternate boot operation
26	RW	0x0	disable_boot Disable boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do not set disable_boot and enable_boot together.

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Bit	Attr	Reset Value	Description
25	RW	0x0	expect_boot_ack Expect boot acknowledge. When software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.
24	RW	0x0	enable_boot Enable boot. This bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do not set disable_boot and enable_boot together.
23	RW	0x0	ccs_expected 1'b0: Interrupts are not enabled in CE-ATA device or command does not expect CCS from device 1'b1: Interrupts are enabled in CE-ATA device and RW_BLK command expects command completion signal from CE-ATA device If the command expects command completion signal (CCS) from the CE-ATA device, the software should set this control bit. The Host Controller sets data transfer over (DTO) bit in SDMMC_RINTSTS register and generates interrupt to host if data transfer over interrupt is not masked.
22	RW	0x0	read_ceata_device 1'b0: Host is not performing read access towards CE-ATA device 1'b1: Host is performing read access towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. The Host Controller should not indicate read data timeout while waiting for data from CE-ATA device.
21	RW	0x0	update_clock_regs_only 1'b0: Normal command sequence 1'b1: Do not send commands, just update clock register value into card clock domain. Following register values transferred into card clock domain: SDMMC_CLKDIV, SDMMC_CLRSRC, SDMMC_CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_regs_only = 0, following control registers are transferred from BIU to CIU: SDMMC_CMD, SDMMC_CMDARG, SDMMC_TMOUT, SDMMC_CTYPE, SDMMC_BLKSIZ, SDMMC_BYTCNT. CIU uses new register values for new command sequence to card. When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.
20:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15	RW	0x0	send_initialization 1'b0: Do not send initialization sequence (80 clocks of 1) before sending this command 1'b1: Send initialization sequence before sending this command After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).
14	RW	0x0	stop_abort_cmd 1'b0: Neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1'b1: Stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with SDMMC_CMD[26]=disable_boot.
13	RW	0x0	wait_prvdata_complete 1'b0: Send command at once, even if previous data transfer has not completed 1'b1: Wait for previous data transfer completion before sending command The wait_prvdata_complete=0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.
12	RW	0x0	send_auto_stop 1'b0: No stop command sent at end of data transfer 1'b1: Send stop command at end of data transfer When set, the Host Controller sends stop command to card at end of data transfer. a. When send_auto_stop bit should be set, since some data transfers do not need explicit stop commands b. Open-ended transfers that software should explicitly send to stop command Additionally, when "resume" is sent to resume-suspended memory access of SD-Combo card, bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.
11	RW	0x0	transfer_mode 1'b0: Block data transfer command 1'b1: Stream data transfer command Don't care if no data expected.
10	RW	0x0	wr 1'b0: Read from card 1'b1: Write to card Don't care if no data expected from card.
9	RW	0x0	data_expected 1'b0: No data transfer expected (read/write) 1'b1: Data transfer expected (read/write)

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Bit	Attr	Reset Value	Description
8	RW	0x0	check_response_crc 1'b0: Do not check response CRC 1'b1: Check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.
7	RW	0x0	response_length 1'b0: Short response expected from card 1'b1: Long response expected from card
6	RW	0x0	response_expect 1'b0: No response expected from card 1'b1: Response expected from card
5:0	RW	0x00	cmd_index Command index

SDMMC_RESP0

Address: Operational Base (0xFF480000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response0 Bit[31:0] of response

SDMMC_RESP1

Address: Operational Base (0xFF480000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response1 Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always "short" for them.

SDMMC_RESP2

Address: **Operational Base (0xFF480000)** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response2 Bit[95:64] of long response

SDMMC_RESP3

Address: **Operational Base (0xFF480000)** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response3 Bit[127:96] of long response

SDMMC_MINTSTS

Address: Operational Base (0xFF480000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	sdio_interrupt SDIO interrupt status when sdio_int_mask is set
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_status Data no busy interrupt status when data_nobusy_int_mask is set

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	int_status Interrupt enabled only if corresponding bit in interrupt mask register is set. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_RINTSTS

Address: Operational Base (0xFF480000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	R/WSC	0x0	sdio_interrupt Raw SDIO interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
23:17	RO	0x00	reserved
16	R/WSC	0x0	data_nobusy_int_status Raw data no busy interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
15:0	R/WSC	0x0000	int_status Raw interrupt status. Writes to bits clear status bit. Write value of 1 clears status bit, and value of 0 leaves bit intact. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_STATUS

Address: Operational Base (0xFF480000) + offset (0x0048)

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Bit	Attr	Reset Value	Description
31	RO	0x0	dma_req DMA request signal state
30	RO	0x0	dma_ack DMA acknowledge signal state
29:17	RO	0x0000	fifo_count Number of filled locations in FIFO
16:11	RO	0x00	response_index Index of previous response, including any auto-stop sent by core.
10	RO	0x0	data_state_mc_busy Data transmit or receive state-machine is busy
9	RO	0x0	data_busy Inverted version of raw selected card_data[0]. 1'b0: Card data not busy 1'b1: Card data busy
8	RO	0x1	data_3_status Raw selected card_data[3]; checks whether card is present. 1'b0: Card not present 1'b1: Card present
7:4	RO	0x0	command_fsm_states Command FSM states: 4'h0: Idle 4'h1: Send init sequence 4'h2: Tx cmd start bit 4'h3: Tx cmd tx bit 4'h4: Tx cmd index + arg 4'h5: Tx cmd crc7 4'h6: Tx cmd end bit 4'h7: Tx resp start bit 4'h8: Rx resp IRQ response 4'h9: Rx resp tx bit 4'ha: Rx resp cmd idx 4'hb: Rx resp data 4'hc: Rx resp crc7 4'hd: Rx resp end bit 4'he: Cmd path wait NCC 4'hf: Wait CMD-to-response turnaround The command FSM state is represented using 19 bits. The SDMMC_STATUS register[7:4] has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the SDMMC_STATUS[7:4] register. The three states that are not represented in the SDMMC_STATUS register[7:4] are: Bit 16: Wait for CCS Bit 17: Send CCSD Bit 18: Boot Mode Due to this, while command FSM is in "Wait for CCS state" or "Send CCSD" or "Boot Mode", the SDMMC_STATUS register indicates status as 0 for the bit field [7:4].
3	RO	0x0	fifo_full FIFO is full status
2	RO	0x1	fifo_empty FIFO is empty status
1	RO	0x1	fifo_tx_watermark FIFO reached Transmit watermark level; not qualified with data transfer.

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Bit	Attr	Reset Value	Description
0	RO	0x0	fifo_rx_watermark FIFO reached Receive watermark level; not qualified with data transfer.

SDMMC_FIFOTH

Address: Operational Base (0xFF480000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	dma_mutiple_transaction_size Burst size of multiple transaction; should be programmed same as DMA controller multiple-transaction-size SRC/DEST_MSIZE. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers The unit for transfer is 32bits.
27:16	RW	0x0ff	rx_wmark FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits-1 bit less than FIFO-count of status register, which is 13 bits. Limitation: rx_wmark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.
15:12	RO	0x0	reserved
11:0	RW	0x000	tx_wmark FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes

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Bit	Attr	Reset Value	Description
			(not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits -1 bit less than FIFO-count of status register, which is 13 bits. Limitation: tx_wmark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)

SDMMC_CDETECT

Address: Operational Base (0xFF480000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	card_detect_n Value on card_detect_n input port. 1'b0: Represents presence of card 1'b1: Represents absence of card

SDMMC_WRTPRT

Address: Operational Base (0xFF480000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	write_protect Value on card_write_prt input port. 1 represents write protection.

SDMMC_TCBCNT

Address: Operational Base (0xFF480000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_card_byte_count Number of bytes transferred by CIU unit to card

SDMMC_TBBCNT

Address: Operational Base (0xFF480000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_fifo_byte_count Number of bytes transferred between host/DMA memory and BIU FIFO

SDMMC_DEBNCE

Address: Operational Base (0xFF480000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0xffffff	debounce_count Number of host clock used by debounce filter logic; typical debounce time is 5-25 ms.

SDMMC_USRID

Address: Operational Base (0xFF480000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usrid User identification register

SDMMC_VERID

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Address: Operational Base (0xFF480000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x5342270a	verid Version identification register

SDMMC_HCON

Address: Operational Base (0xFF480000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x1	area_optimized 1'b0: No area optimization 1'b1: Area optimization
25:24	RO	0x0	num_clk_div divider number-1.
23	RO	0x1	set_clk_false_path 1'b0: No false path 1'b1: False path set
22	RO	0x1	impl_hold_reg 1'b0: No hold register 1'b1: Hold register
21	RO	0x0	fifo_ram_inside 1'b0: Outside 1'b1: Inside
20:18	RO	0x1	ge_dma_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved
17:16	RO	0x0	dma_interface 2'b00: None 2'b01: INT_DMA 2'b10: GENERIC_DMA 2'b11: NON_INT_DMA
15:10	RO	0x0d	h_addr_width 6'h8: 9 bits 6'h9: 10 bits ..... 6'h1f: 32 bits Others: Reserved
9:7	RO	0x1	h_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved
6	RO	0x1	h_bus_type 1'b0: APB 1'b1: AHB
5:1	RO	0x00	card_num Card number -1.
0	RO	0x1	card_type Card type. 1'b0: MMC_ONLY 1'b1: SD_MMC

SDMMC_UHSREG

Address: Operational Base (0xFF480000) + offset (0x0074)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	ddr_reg DDR mode. These bits indicate DDR mode of operation to the core for the data transfer. 1'b0: Non-DDR mode 1'b1: DDR mode
15:0	RO	0x0000	reserved

SDMMC_RSTN

Address: Operational Base (0xFF480000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	card_reset Hardware reset. 1'b0: Active mode 1'b1: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

SDMMC_BMOD

Address: Operational Base (0xFF480000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RO	0x0	pbl Programmable burst length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of SDMMC_FIFOTH register. In order to change this value, write the required value to SDMMC_FIFOTH register. This is an encode value as follows. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers Transfer unit is 32 bits. PBL is a read-only value and is applicable only for data access; it does not apply to descriptor accesses.
7	RW	0x0	de IDMAC enable. When set, the IDMAC is enabled.
6:2	RW	0x00	dsl Descriptor skip length. Specifies the number of word to skip between two unchained descriptors. This is applicable only for dual buffer structure.

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Bit	Attr	Reset Value	Description
1	RW	0x0	fb Fixed burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	RW	0x0	swr Software reset. When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle.

SDMMC_PLDMND

Address: Operational Base (0xFF480000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	pd Poll demand. If the OWN bit of a descriptor is not set, the FSM goes to the suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation.

SDMMC_DBADDR

Address: Operational Base (0xFF480000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sbl Start of descriptor list. Contains the base address of the first descriptor. The LSB bits[1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

SDMMC_IDSTS

Address: Operational Base (0xFF480000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:13	RO	0x0	fsm DMAC FSM present state. 4'h0: DMA_IDLE 4'h1: DMA_SUSPEND 4'h2: DESC_RD 4'h3: DESC_CHK 4'h4: DMA_RD_REQ_WAI 4'h5: DMA_WR_REQ_WAI 4'h6: DMA_RD 4'h7: DMA_WR 4'h8: DESC_CLOSE Others: Reserved
12:10	RO	0x0	eb Error bits. Indicates the type of error that caused a bus error. Valid only with fatal bus. 3'h1: Host abort received during transmission 3'h2: Host abort received during reception Others: Reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	ais Abnormal interrupt summary. Logical OR of the following: SDMMC_IDSTS[2] fatal bus interrupt SDMMC_IDSTS[4] du bit interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes ais to be set is cleared. Writing a 1 clears this bit.
8	RW	0x0	nis Normal interrupt summary. Logical OR of the following: SDMMC_IDSTS[0] transmit interrupt SDMMC_IDSTS[1] receive interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes nis to be set is cleared. Writing a 1 clears this bit.
7:6	RO	0x0	reserved
5	RW	0x0	ces Card error summary. Indicates the status of the transaction to/from the card; also present in SDMMC_RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot Ack Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a "response error"; however, it will not abort if the CES bit is cleared.
4	RW	0x0	dui Descriptor unavailable interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error interrupt. Indicates that a bus error occurred (SDMMC_IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	RW	0x0	ri Receive interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	RW	0x0	ti Transmit interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit.

SDMMC_IDINTEN

Address: Operational Base (0xFF480000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	ai Abnormal interrupt summary enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: SDMMC_IDINTEN[2] fatal bus error interrupt SDMMC_IDINTEN[4] du interrupt
8	RW	0x0	ni Normal interrupt summary enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: SDMMC_IDINTEN[0] transmit interrupt SDMMC_IDINTEN[1] receive interrupt
7:6	RO	0x0	reserved
5	RW	0x0	ces Card error summary interrupt enable. When set, it enables the card interrupt summary.
4	RW	0x0	du Descriptor unavailable interrupt. When set along with abnormal interrupt summary enable, the du interrupt is enabled.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error enable. When set with abnormal interrupt summary enable, the fatal bus error interrupt is enabled. When reset, fatal bus error enable interrupt is disabled.
1	RW	0x0	ri Receive interrupt enable. When set with normal interrupt summary enable, receive interrupt is enabled. When reset, receive interrupt is disabled.
0	RW	0x0	ti Transmit interrupt enable. When set with normal interrupt summary enable, transmit interrupt is enabled. When reset, transmit interrupt is disabled.

SDMMC_DSCADDR

Address: Operational Base (0xFF480000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hda Host descriptor address pointer. This register points to the start address of the current descriptor read by the IDMAC. Cleared on reset. Pointer updated by IDMAC during operation.

SDMMC_BUFADDR

Address: Operational Base (0xFF480000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hba Host buffer address pointer. This register points to the current data buffer address being accessed by the IDMAC. Cleared on Reset. Pointer updated by IDMAC during operation.

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SDMMC_CARDTHRCTL

Address: Operational Base (0xFF480000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	card_rd_thres Card read threshold size
15:2	RO	0x0000	reserved
1	RW	0x0	busy_clr_int_en Busy clear interrupt. 1'b0: Busy clear interrupt disabled 1'b1: Busy clear interrupt enabled Note: The application can disable this feature if it does not want to wait for a busy clear interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.
0	RW	0x0	card_rd_thres_en Card read threshold enable. 1'b0: Card read threshold disabled 1'b1: Card read threshold enabled. The host initiates read transfer only if card_rd_thres amount of space is available in receive FIFO.

SDMMC_BACKEND_POWER

Address: Operational Base (0xFF480000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	back_end_power Back end power. 1'b0: Off; Reset 1'b1: Back-end power supplied to card application

SDMMC_EMMCDDR_REG

Address: Operational Base (0xFF480000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	half_start_bit Control for start bit detection mechanism inside Host Controller based on duration of start bit. For eMMC 4.5, start bit can be: 1'b0: Full cycle (half_start_bit=0) 1'b1: Less than one full cycle (half_start_bit=1) Set half_start_bit=1 for eMMC 4.5 and above; set to 0 for SD applications.

SDMMC_RDYINT_GEN

Address: Operational Base (0xFF480000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	rdyint_cnt_finish Counter finish indication. When high, it indicates that the rdyint counter is finished.

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Bit	Attr	Reset Value	Description
23:16	RO	0xff	rdyint_cnt_status Couner status, reflect internal counter value.
15:9	RO	0x00	reserved
8	RW	0x0	rdyint_gen_working Working indication for rdyint generator. When high, Host Controller start to count and generate one rdyint trigger. After the rdyint trigger is generated, this bit will be set to 0 by Host Controller. So software should set it to 1 before detecting next interrupt.
7:0	RW	0x00	rdyint_gen_maxval Max counter value to detect cdata_in0 high value for generating rdyint, based on internal clock frequency.

SDMMC_CLKGEN_CON0

Address: Operational Base (0xFF480000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	drv_sel Selection for drive clock. 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
10	RO	0x0	reserved
9:3	RW	0x00	drv_delaynum Delay element number configuration for drive clock. It can be modified when init_state=1 and should be stable when init_state=0.
2:1	RW	0x2	drv_degree Phase selection for drive clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
0	RW	0x0	init_state Enable initialization for clock source. 1'b0: Disable 1'b1: Enable When init_state=1, the host clocks including drive clock and sample clock are inactive.

SDMMC_CLKGEN_CON1

Address: Operational Base (0xFF480000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	sample_sel Selection for sample clock. 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
10	RO	0x0	reserved
9:3	RW	0x00	sample_delaynum Delay element number configuration for sample clock. It can be modified when init_state=1 and should be stable when init_state=0.
2:1	RW	0x0	sample_degree Phase selection for sample clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
0	RO	0x0	reserved

SDMMC_MISC_CON

Address: Operational Base (0xFF480000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	mem_clkgat_enable Memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
4:0	RO	0x0	reserved

SDMMC_FIFO_BASE

Address: Operational Base (0xFF480000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_base_addr FIFO base address

39.5 Interface Description

39.5.1 SDMMC Interface Description

Table 39-8 SDMMC 1bit mode Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc_cclk	O	GPIO3_A0	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[3:0]=4'h1
sdmmc _ccmd	I/O	GPIO3_A1	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[7:4]=4'h1
sdmmc _cdata0	I/O	GPIO3_A2	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[11:8]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 39-9 SDMMC 4 bits mode Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc_cclk	O	GPIO3_A0	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[3:0]=4'h1

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Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc _ccmd	I/O	GPIO3_A1	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[7:4]=4'h1
sdmmc _cdata0	I/O	GPIO3_A2	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[11:8]=4'h1
sdmmc _cdata1	I/O	GPIO3_A3	GPIO3_IOC_GPIO3A_IOMUX_SEL_0[15:12]=4'h1
sdmmc _cdata2	I/O	GPIO3_A4	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[3:0]=4'h1
sdmmc _cdata3	I/O	GPIO3_A5	GPIO3_IOC_GPIO3A_IOMUX_SEL_1[7:4]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

39.6 Application Notes

39.6.1 Software/Hardware Restriction

Before issuing a new data transfer command, the software should ensure that the card is not busy due to any previous data transfer command. Before changing the card clock frequency, the software must ensure that there are no data or command transfers in progress.

To avoid glitches in the card clock outputs, the software should use the following steps when changing the card clock frequency:

1) Before disable the clocks, ensure that the card is not busy due to any previous data command. To determine this, check for 0 in bit9 of SDMMC_STATUS register.
2) Update the Clock Enable register to disable clock. To ensure completion of any previous command before this update, send a command to the CIU to update the clock registers by setting:

- start_cmd bit
- "update clock registers only" bits
- "wait_previous data complete" bit

  Wait for the CIU to take the command by polling for 0 on the start_cmd bit.

3) Set the start_cmd bit to update the Clock Divider and/or Clock Source register, and send a command to the CIU in order to update the clock registers; wait for the CIU to take the command.
4) Set start_cmd to update the Clock Enable register in order to enable the required clocks and send a command to the CIU to update the clock registers; wait for the CIU to take the command.

In non-DMA mode, while reading from a card, the Data Transfer Over (SDMMC_RINTSTS[3]) interrupt occurs as soon as the data transfer from the card is over. There still could be some data left in the FIFO, and the RX_WMark interrupt may or may not occur, depending on the remaining bytes in the FIFO. Software should read any remaining bytes upon seeing the Data Transfer Over (DTO) interrupt. While using the external DMA interface for reading from a card, the DTO interrupt occurs only after all the data is flushed to memory by the DMA interface unit.

While writing to a card in external DMA mode, if an undefined-length transfer is selected by setting the Byte Count Register to 0, the DMA logic will likely request more data than it will send to the card, since it has no way of knowing at which point the software will stop the transfer. The DMA request stops as soon as the DTO is set by the CIU.

If the software issues a controller_reset command by setting control register bit[0] to 1, all the CIU state machines are reset; the FIFO is not cleared. The DMA sends all remaining bytes to the host. In addition to a card-reset, if a FIFO reset is also issued, then:

- Any pending DMA transfer on the bus completes correctly
- DMA data read is ignored
- Write data is unknown(x)

Additionally, if dma_reset is also issued, any pending DMA transfer is abruptly terminated. When the DMA is used, the DMA controller channel should also be reset and reprogrammed.

If any of the previous data commands do not properly terminate, then the software should issue the FIFO reset in order to remove any residual data, if any, in the FIFO. After asserting the FIFO reset, you should wait until this bit is cleared.

One data-transfer requirement between the FIFO and host is that the number of transfers should be a multiple of the FIFO data width (32bits). For example, you want to write only

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15 bytes to an SD/MMC card (SDMMC_BYTCNT), the host should write 16 bytes to the FIFO or program the DMA to do 16-byte transfers. The software can still program the Byte Count register to only 15, at which point only 15 bytes will be transferred to the card. Similarly, when 15 bytes are read from a card, the host should still read all 16 bytes from the FIFO. It is recommended that you not change the FIFO threshold register in the middle of data transfers.

39.6.2 Programming Sequence

39.6.2.1 Initialization

Following figure illustrates the initialization flow.

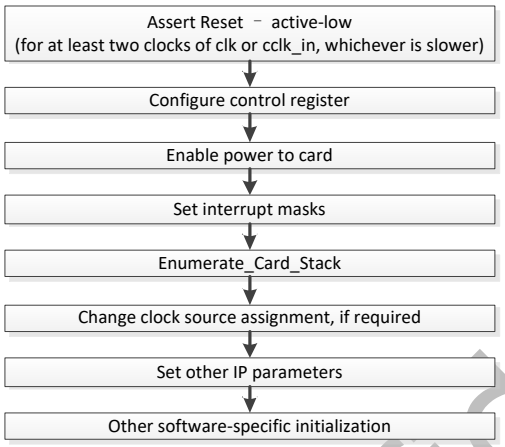

Fig. 39-9 Host Controller Initialization Sequence

Once the power and clocks are stable, reset_n should be asserted(active-low) for at least two cycles of clk or cclk_in, whichever is slower. The reset initializes the registers, ports, FIFO-pointers, DMA interface controls, and state-machines in the design. After power-on reset, the software should do the following:

1) Configure control register – For MMC mode, enable the open-drain pullup by setting enable_OD_pullup(bit24) in the SDMMC_CTRL register.
2) Enable power to cards – Before enabling the power, confirm that the voltage setting to the voltage regulators is correct. Enable power to the connected cards by setting the corresponding bit to 1 in the Power Enable register. Wait for the power ramp-up time.
3) Set masks for interrupts by clearing appropriate bits in the Interrupt Mask register. Set the global int_enable bit of the SDMMC_CTRL register. It is recommended that you write 0xffff_ffff to the Raw Interrupt register in order to clear any pending interrupts before setting the int_enable bit.
4) Enumerate card stack – Each card is enumerated according to card type; for details, refer to "Enumerated Card Stack". For enumeration, you should restrict the clock frequency to 400KHz.
5) Changing clock source assignment – set the card frequency using the clock-divider and clock-source registers; for details, refer to "Clock Programming". MMC cards operate at a maximum of 20MHz (at maximum of 52MHz in high-speed mode). SD mode operates at a maximum of 25MHz (at maximum of 50MHz in high-speed mode).
6) Set other parameters, which normally do not need to be changed with every command, with a typical value such as timeout values in cclk_out according to SD/MMC specifications.

- ResponseTimeOut = 0x64
- DataTimeOut = highest of one of the following:
- (10*((TAAC*Fop)+(100*NSAC))
- Host FIFO read/write latency from FIFO empty/full
- Set the debounce value to 25ms(default:0x0fffff) in host clock cycle units in the SDMMC_DEBNCE register.

FIFO threshold value in bytes in the SDMMC_FIFOTH register.

39.6.2.2 Enumerated Card Stack

The card stack does the following:

- Enumerates all connected cards
- Sets the RCA for the connected cards

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- Reads card-specific information
- Stores card-specific information locally

Enumeration depends on the operating mode of the SD/MMC card; the card type is first identified and the appropriate card enumeration routine is called.

1) Check if the card is connected.
2) Clear the card type register to set the card width as a single bit. For the given card number, clear the corresponding bits in the card_type register. Clear the register bit for a 1-bit, 4-bit bus width. For example, for card number=1, clear bit 0 and bit 16 of the card_type register.
3) Set clock frequency to FOD=400KHz, maximum – Program clock divider0 (bits 0-7 in the SDMMC_CLKDIV register) value to one-half of the cclk_in frequency divided by 400KHz. For example, if cclk_in is 20MHz, then the value is 20, 000/(2*400)=25.
4) Identify the card type; that is, SD, MMC, or SDIO.
   a. Send CMD5 first. If a response is received, then the card is SDIO
   b. If not, send CMD8 with the following Argument
      Bit[31:12] = 20'h0 //reserved bits
      Bit[11:8] = 4'b0001 //VHS value
      Bit[7:0] = 8'b10101010 //Preferred Check Pattern by SD2.0
   c. If Response is received the card supports High Capacity SD2.0 then send ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b1; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
   d. If Response is received for ACMD41 then the card is SD. Otherwise the card is MMC.
   e. If response is not received for initial CMD8 then card does not support High Capacity SD2.0, then issue CMD0 followed by ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b0; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
5) Enumerate the card according to the card type.
6) Use a clock source with a frequency = Fod (that is, 400KHz) and use the following enumeration command sequence:

- SD card – Send CMD0, CMD8, ACMD41, CMD2, CMD3.
- MMC – Send CMD0, CMD1, CMD2, CMD3.

39.6.2.3 Clock Programming

The Host Controller supports one clock source. The clock to an individual card can be enabled or disabled. Registers that support this are:

- SDMMC_CLKDIV – Programs individual clock source frequency. SDMMC_CLKDIV limited to 0 or 1 is recommended.
- SDMMC_CLKSRC – Assign clock source for each card.
- SDMMC_CLKENA – Enables or disables clock for individual card and enables low-power mode, which automatically stops the clock to a card when the card is idle for more than 8 clocks.

The Host Controller loads each of these registers only when the start_cmd bit and the update_clk_regs_only bit in the SDMMC_CMD register are set. When a command is successfully loaded, the Host Controller clears this bit, unless the Host Controller already has another command in the queue, at which point it gives an HLE(Hardware Locked Error). Software should look for the start_cmd and the update_clk_regs_only bits, and should also set the wait_prvdata_complete bit to ensure that clock parameters do not change during data transfer. Note that even though start_cmd is set for updating clock registers, the Host Controller does not raise a command_done signal upon command completion.

The following shows how to program these registers:

1) Confirm that no card is engaged in any transaction; if there is a transaction, wait until it finishes.
2) Stop all clocks by writing 0 to the SDMMC_CLKENA register. Set the start_cmd,

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Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

3) Program the SDMMC_CLKDIV and SDMMC_CLKSRC registers, as required. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

Re-enable all clocks by programming the SDMMC_CLKENA register. Set the start_cmd, update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

39.6.2.4 No-Data Command With or Without Response Sequence

To send any non-data command, the software needs to program the SDMMC_CMD register @0x2C and the SDMMC_CMDARG register @0x28 with appropriate parameters. Using these two registers, the Host Controller forms the command and sends it to the command bus. The Host Controller reflects the errors in the command response through the error bits of the SDMMC_RINTSTS register.

When a response is received – either erroneous or valid – the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. A short response is copied in Response Register0, while along response is copied to all four response registers @0x30, 0x34, 0x38, and 0x3C. The Response3 register bit 31 represents the MSB, and the Response0 register bit 0 represents the LSB of a long response.

For basic commands or non-data commands, follow these steps:

1) Program the Command register @0x28 with the appropriate command argument parameter.
2) Program the Command register @0x2C with the settings in following table.

Table 39-10 Command Settings for No-Data Command

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used; ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
data_expected	0	No data command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
cmd_index	command-index	-
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
wait_prvdata_complete	1	Before sending command on command line, host should wait for completion of any

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Parameter	Value	Description
		data command in process, if any (recommended to always set this bit, unless the current command is to query status or stop data transfer when transfer is in progress)
check_response_crc	1	If host should crosscheck CRC of response received

3) Wait for command acceptance by host. The following happens when the command is loaded into the Host Controller:
- Host Controller accepts the command for execution and clears the start_cmd bit in the SDMMC_CMD register, unless one command is in process, at which point the Host Controller can load and keep the second command in the buffer.
- If the Host Controller is unable to load the command – that is, a command is already in progress, a second command is in the buffer, and a third command is attempted – then it generates an HLE (hardware-locked error).

4) Check if there is an HLE.
5) Wait for command execution to complete. After receiving either a response from a card or response timeout, the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. Software can either poll for this bit or respond to a generated interrupt.
6) Check if response_timeout error, response_CRC error, or response error is set. This can be done either by responding to an interrupt raised by these errors or by polling bits 1, 6, and 8 from the SDMMC_RINTSTS register @0x44. If no response error is received, then the response is valid. If required, the software can copy the response from the response registers @0x30-0x3C.

Software should not modify clock parameters while a command is being executed.

39.6.2.5 Data Transfer Commands

Data transfer commands transfer data between the memory card and the Host Controller. To send a data command, the Host Controller needs a command argument, total data size, and block size. Software can receive or send data through the FIFO.

Before a data transfer command, software should confirm that the card is not busy and is in a transfer state, which can be done using the CMD13 and CMD7 commands, respectively. For the data transfer commands, it is important that the same bus width that is programmed in the card should be set in the card type register @0x18.

The Host Controller generates an interrupt for different conditions during data transfer, which are reflected in the SDMMC_RINTSTS register @0x44 as:

1) Data_Transfer_Over (bit 3) – When data transfer is over or terminated. If there is a response timeout error, then the Host Controller does not attempt any data transfer and the "Data Transfer Over" bit is never set.
2) Transmit_FIFO_Data_request (bit 4) – FIFO threshold for transmitting data was reached; software is expected to write data, if available, in FIFO.
3) Receive_FIFO_Data_request (bit 5) – FIFO threshold for receiving data was reached; software is expected to read data from FIFO.
4) Data starvation by Host timeout (bit 10) – FIFO is empty during transmission or is full during reception. Unless software writes data for empty condition or reads data for full condition, the Host Controller cannot continue with data transfer. The clock to the card has been stopped.
5) Data read timeout error (bit 9) – Card has not sent data within the timeout period.
6) Data CRC error (bit 7) – CRC error occurred during data reception.
7) Start bit error (bit 13) – Start bit was not received during data reception.
8) End bit error (bit 15) – End bit was not received during data reception or for a write operation; a CRC error is indicated by the card.

Conditions 6), 7), and 8) indicate that the received data may have errors. If there was a response timeout, then no data transfer occurred.

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39.6.2.6 Single-Block or Multiple-Block Read

Steps involved in a single-block or multiple-block read are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C. The Host Controller expects data from the card in blocks of size SDMMC_BLKSIZ each.
3) Program the SDMMC_CMDARG register @0x28 with the data address of the beginning of a data read.
4) Program the Command register with the parameters listed in following table. For SD and MMC cards, use CMD17 for a single-block read and CMD18 for a multiple-block read. For SDIO cards, use CMD53 for both single-block and multiple-block transfers.

Table 39-11 Command Setting for Single or Multiple-Block Read

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used; ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No.0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	0	Read from card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, the Host Controller starts executing the command; when the command is sent to the bus, the command_done interrupt is generated.

- Software should look for data error interrupts; that is, bits 7, 9, 13, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending a STOP command.
- Software should look for Receive_FIFO_Data_request and/or data starvation by host

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timeout conditions. In both cases, the software should read data from the FIFO and make space in the FIFO for receiving more data.

When a Data_Transfer_Over interrupt is received, the software should read the remaining data from the FIFO.

39.6.2.7 Single-Block or Multiple-Block Write

Steps involved in a single-block or multiple-block write are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C; the Host Controller sends data in blocks of size SDMMC_BLKSIZ each.
3) Program SDMMC_CMDARG register @0x28 with the data address to which data should be written.
4) Write data in the FIFO; it is usually best to start filling data the full depth of the FIFO.
5) Program the Command register with the parameters listed in following table.

Table 39-12 Command Settings for Single or Multiple-Block Write

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used; ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	1	Write to card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, Host Controller starts executing a command; when the command is sent to the bus, a command_done interrupt is generated.

- Software should look for data error interrupts; that is, for bits 7, 9, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by

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sending the STOP command.
- Software should look for Transmit_FIFO_Data_Request and/or timeout conditions from data starvation by the host. In both cases, the software should write data into the FIFO.

When a Data_Transfer_Over interrupt is received, the data command is over. For an open-ended block transfer, if the byte count is 0, the software must send the STOP command. If the byte count is not 0, then upon completion of a transfer of a given number of bytes, the Host Controller should send the STOP command, if necessary. Completion of the AUTO-STOP command is reflected by the Auto_command_done interrupt – bit 14 of the SDMMC_RINTSTS register. A response to AUTO_STOP is stored in SDMMC_RESP1 @0x34.

39.6.2.8 Sending Stop or Abort in Middle of Transfer

The STOP command can terminate a data transfer between a memory card and the Controller, while the ABORT command can terminate an I/O data transfer for only the SDIO_IOONLY and SDIO_COMBO cards.
- Send STOP command – Can be sent on the command line while a data transfer is in progress; this command can be sent at any time during a data transfer.

You can also use an additional setting for this command in order to set the Command register bits (5-0) to CMD12 and set bit 14 (stop_abort_cmd) to 1. If stop_abort_cmd is not set to 1, the Controller does not know that the user stopped a data transfer. Reset bit 13 of the Command register (wait_prvdata_complete) to 0 in order to make the Controller send the command at once, even though there is a data transfer in progress.
Send ABORT command – Can be used with only an SDIO_IOONLY or SDIO_COMBO card. To abort the function that is transferring data, program the function number in ASx bits (CCCR register of card, address 0x06, bits (0-2) using CMD52.

39.6.2.9 Read_Wait Sequence

Read_wait is used with only the SDIO card and can temporarily stall the data transfer—either from function or memory—and allow the host to send commands to any function within the SDIO device. The host can stall this transfer for as long as required. The Host Controller provides the facility to signal this stall transfer to the card. The steps for doing this are:

1) Check if the card supports the read_wait facility; read SRW (bit 2) of the CCCR register @0x08. If this bit is 1, then all functions in the card support the read_wait facility. Use CMD52 to read this bit.
2) If the card supports the read_wait signal, then assert it by setting the read_wait (bit 6) in the SDMMC_CTRL register @0x00.

Clear the read_wait bit in the SDMMC_CTRL register.

39.6.2.10 Controller/DMA/FIFO Reset Usage

- Controller reset – Resets the controller by setting the controller_reset bit (bit 0) in the SDMMC_CTRL register; this resets the CIU and state machines, and also resets the BIU-to-CIU interface. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.
- FIFO reset - Resets the FIFO by setting the fifo_reset bit (bit 1) in the SDMMC_CTRL register; this resets the FIFO pointers and counters of the FIFO. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

In external DMA transfer mode, even when the FIFO pointers are reset, if there is a DMA transfer in progress, it could push or pop data to or from the FIFO; the DMA itself completes correctly. In order to clear the FIFO, the software should issue an additional FIFO reset and clear any FIFO under-run or overrun errors in the SDMMC_RAWINTS register caused by the DMA transfers after the FIFO was reset.

39.6.2.11 Card Read Threshold

When an application needs to perform a Single or Multiple Block Read command, the application must program the SDMMC_CARDTHRCTL register with the appropriate Card Read Threshold size (CardRdThreshold) and set the Card Read Threshold Enable

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(CardRdThrEnable) bit to 1'b1. This additional programming ensures that the Host controller sends a Read Command only if there is space equal to the Card Read Threshold available in the Rx FIFO. This in turn ensures that the card clock is not stopped in the middle a block of data being transmitted from the card. The Card Read Threshold can be set to the block size of the transfer, which guarantees that there is a minimum of one block size of space in the RxFIFO before the controller enables the card clock. The Card Read Threshold is required when the Round Trip Delay is greater than 0.5cclk_in period.

39.6.2.12 Error Handling

The Host Controller implements error checking; errors are reflected in the SDMMC_RAWINTS register@0x44 and can be communicated to the software through an interrupt, or the software can poll for these bits. Upon power-on, interrupts are disabled (int_enable in the SDMMC_CTRL register is 0), and all the interrupts are masked (bits 0-31 of the SDMMC_INTMASK register; default is 0).
Error handling:

- Response and data timeout errors – For response timeout, software can retry the command. For data timeout, the Host Controller has not received the data start bit – either for the first block or the intermediate block – within the timeout period, so software can either retry the whole data transfer again or retry from a specified block onwards. By reading the contents of the SDMMC_TCBCNT later, the software can decide how many bytes remain to be copied.
- Response errors – Set when an error is received during response reception. In this case, the response that copied in the response registers is invalid. Software can retry the command.
- Data errors – Set when error in data reception are observed; for example, data CRC, start bit not found, end bit not found, and so on. These errors could be set for any block-first block, intermediate block, or last block. On receipt of an error, the software can issue a STOP or ABORT command and retry the command for either whole data or partial data.
- Hardware locked error – Set when the Host Controller cannot load a command issued by software. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
- FIFO under-run/overrun error – If the FIFO is full and software tries to write data in the FIFO, then an overrun error is set. Conversely, if the FIFO is empty and the software tries to read data from the FIFO, an under-run error is set. Before reading or writing data in the FIFO, the software should read the fifo_empty or fifo_full bits in the Status register.
- Data starvation by host timeout – Raised when the Host Controller is waiting for software intervention to transfer the data to or from the FIFO, but the software does not transfer within the stipulated timeout period. Under this condition and when a read transfer is in process, the software should read data from the FIFO and create space for further data reception. When a transmit operation is in process, the software should fill data in the FIFO in order to start transferring data to the card.
- CRC Error on Command – If a CRC error is detected for a command, the CE-ATA device does not send a response, and a response timeout is expected from the Host Controller. The ATA layer is notified that an MMC transport layer error occurred.

Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register. It then continues further data transmission until all the bytes are transmitted.

39.6.2.13 Voltage Switching

The Host Controller supports SD 3.0 Ultra High Speed (UHS-1) and is capable of voltage switching in SD-mode, which can be applied to SD High-Capacity (SDHC) and SD Extended Capacity (SDXC) cards. UHS-1 supports only 4-bit mode.
However, whether the IO voltage of 1.8v supported or not is depended on the SoC design.
SD 3.0 UHS-1 supports the following transfer speed modes for UHS-50 and/or UHS-104 cards:

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- DS – default-speed up to 25MHz, 3.3V signaling
- HS – high-speed up to 50MHz, 3.3V signaling
- SDR12 – SDR up to SDR 25MHz, 1.8V signaling
- SDR25 – SDR up to 50MHz, 1.8V signaling
- SDR50 – SDR up to 100MHz, 1.8V signaling
- DDR50 – DDR up to 50MHz, 1.8V signaling

Voltage selection can be done in only SD mode. The first CMD0 selects the bus mode-either SD mode or SPI mode. The card must be in SD mode in order for 1.8V signaling mode to apply, during which time the card cannot be switched to SPI mode or 3.3V signaling without a power cycle.

If the System BIOS in an embedded system already knows that it is connected to an SD 3.0 card, then the driver programs the Controller to initiate ACMD41. The software knows from the response of ACMD41 whether or not the card supports voltage switching to 1.8V.

- If bit 32 of ACMD41 response is 1'b1: card supports voltage switching and next command-CMD11-invokes voltage switching sequence. After CMD11 is started, the software must program the IO voltage selection register based on the soc architecture.
- If bit 32 of ACMD41 response is 1'b0: card does not support voltage switching and CMD11 should not be started.

If the card and host controller accept voltage switching, then they support UHS-1 modes of data transfer. After the voltage switch to 1.8V, SDR12 is the default speed.

Since the UHS-1 can be used in only 4-bit mode, the software must start ACMD6 and change the card data width to 4-bit mode; ACMD6 is driven in any of the UHS-1 speeds. If the host wants to select the DDR mode of data transfer, then the software must program the SDMMC_DDR_REG register in the CSR space with the appropriate card number.

To choose from any of the SDR or DDR modes, appropriate values should be programmed in the SDMMC_CLKDIV register.

39.6.2.14 Voltage Switch Operation

The Voltage Switch operation must be performed in SD mode only.

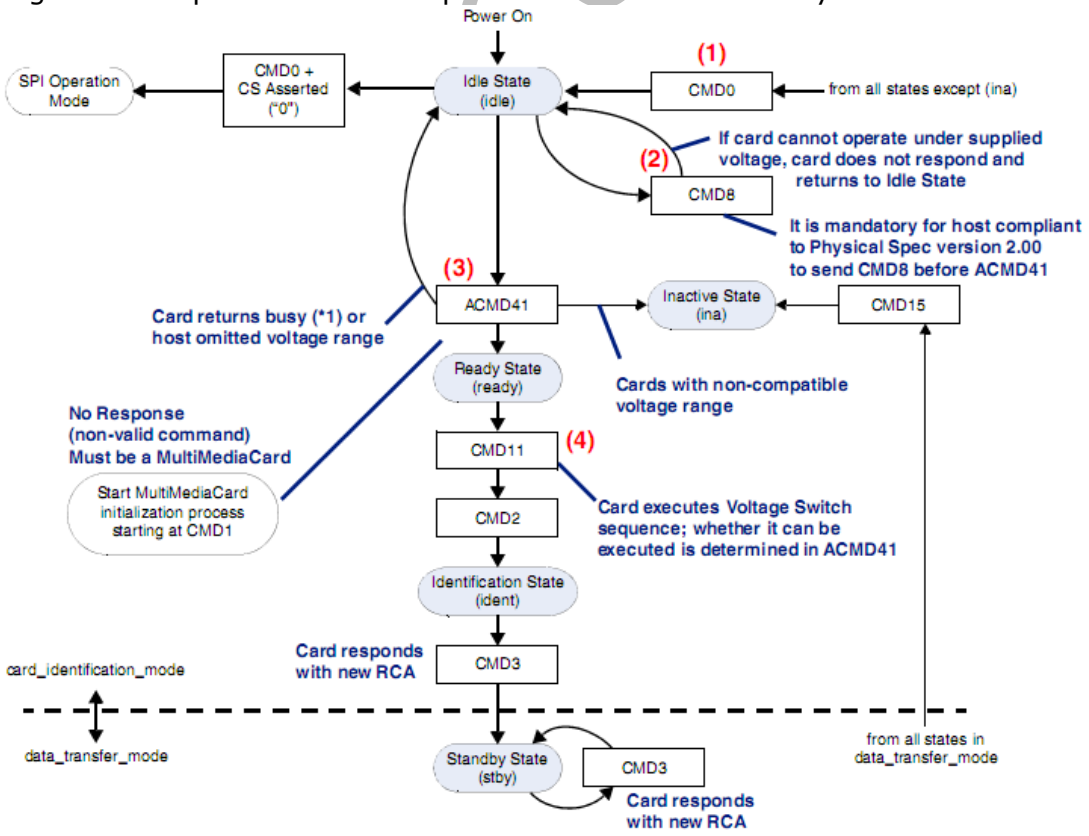

Fig. 39-10 Voltage Switching Command Flow Diagram

The following outlines the steps for the voltage switch programming sequence

1) Software Driver starts CMD0, which selects the bus mode as SD.
2) After the bus is in SD card mode, CMD8 is started in order to verify if the card is

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compatible with the SD Memory Card Specification, Version 2. 00. CMD8 determines if the card is capable of working within the host supply voltage specified in the VHS (19:16) field of the CMD; the card supports the current host voltage if a response to CMD8 is received.

3) ACMD 41 is started. The response to this command informs the software if the card supports voltage switching; bits 38, 36, and 32 are checked by the card argument of ACMD41; refer to following figure.

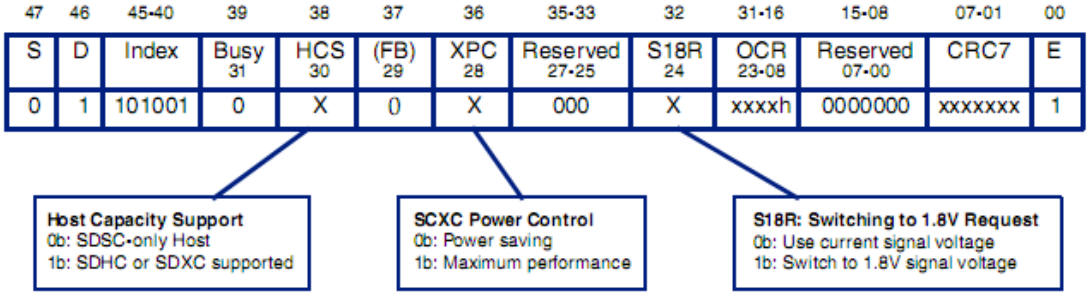

Fig. 39-11 ACMD41 Argument

- Bit 30 informs the card if host supports SDHC/SDXC or not; this bit should be set to 1'b1.
- Bit 28 can be either 1 or 0.
- Bit 24 should be set to 1'b1, indicating that the host is capable of voltage switching; refer to following figure.

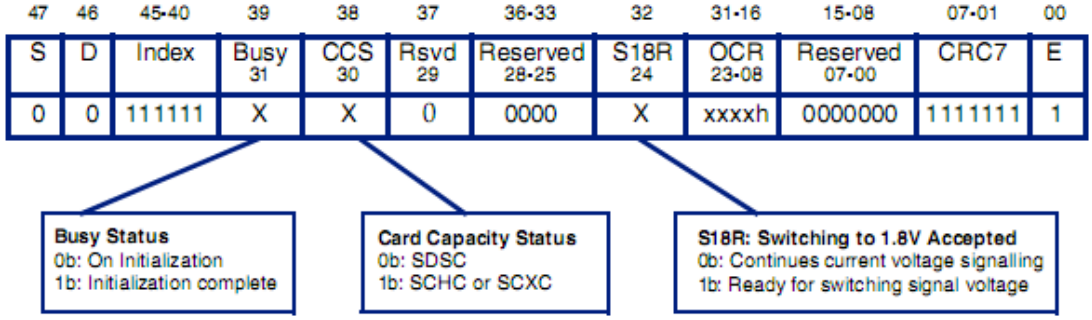

Fig. 39-12 ACMD41 Response(R3)

- Bit 30 – If set to 1'b1, card supports SDHC/SDXC; if set to 1'b0, card supports only SDSC
- Bit 24 – If set to 1'b1, card supports voltage switching and is ready for the switch
- Bit 31 – If set to 1'b1, initialization is over; if set to 1'b0, means initialization in process

If the card supports voltage switching, then the software must perform the steps discussed for either the "Voltage Switch Normal Scenario" or the "Voltage Switch Error Scenario".

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39.6.2.15 Voltage Switch Normal Scenario

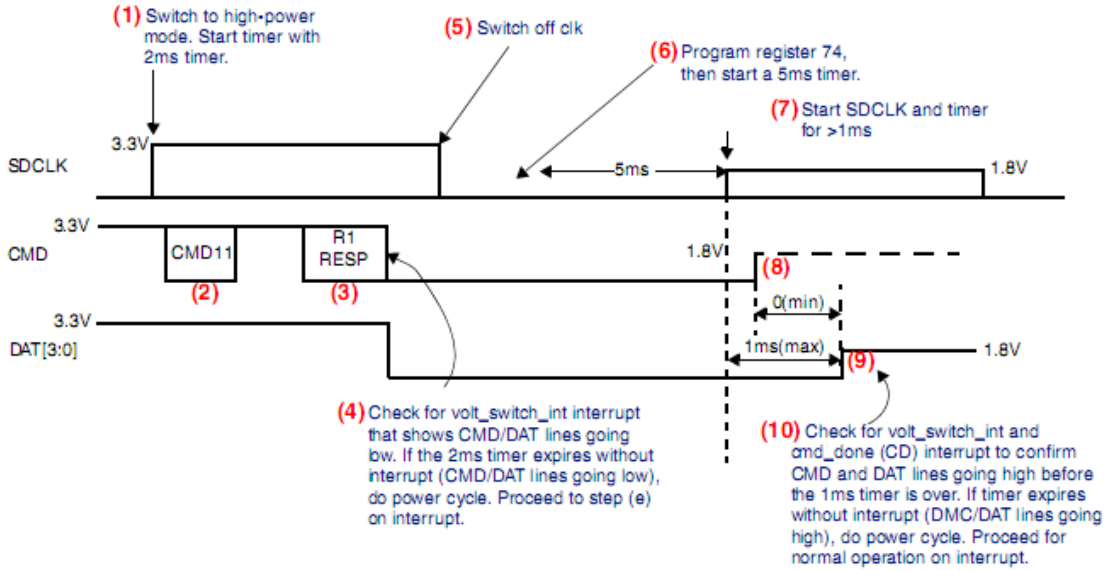

Fig. 39-13 Voltage Switch Normal Scenario

1) The host programs SDMMC_CLKENA—cclk_low_power register—with zero (0) for the corresponding card, which makes the host controller move to high-power mode. The application should start a timer with a recommended value of 2ms; this value of 2ms is determined as below: Total cycles required for CMD11 = 48 cycles
   Total cycles required for RESP R1 = 48 cycles
   Maximum clock delay between MCD11 end to start of RESP1 = 60 cycles
   Total = 48+48 + 60 = 160
   Minimum frequency during enumeration is 100KHz; that is, 10us
   Total time = 160 * 10us = 1600us = 1. 6ms ~ 2ms
2) The host issues CMD11 to start the voltage switch sequence. Set bit 28 to 1'b1 in CMD when setting CMD11; for more information on setting bits, refer to “Boot Operation”.
3) The card returns R1 response; the host controller does not generate cmd_done interrupt on receiving R1 response.
4) The card drives CMD and DAT [3:0] to low immediately after the response. The host controller generates interrupt (VOLT_SWITCH_INT) once the CMD or DAT [3:0] line goes low. The application should wait for this interrupt. If the 2ms timer expires without an interrupt (CMD/DAT lines going low), do a power cycle.

Note: Before doing a power cycle, switch off the card clock by programming SDMMC_CLKENA register

Proceed to step (5) on getting an interrupt (VOLT_SWITCH_INT).

Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be masked during the voltage switch sequence.

If the timer expires without interrupt (CMD/DAT lines going low), perform a power cycle. Proceed to step (5) on interrupt.

1) Program the SDMMC_CLKENA register, with 0 for the corresponding card; the host stops supplying SDCLK.
2) Program Voltage register to the required values for the corresponding card. The application should start a timer > 5ms.
3) After the 5ms timer expires, the host voltage regulator is stable. Program SDMMC_CLKENA register, with 1 for the corresponding card; the host starts providing SDCLK at 1. 8V; this can be at zero time after Voltage register has been programmed. When the SDMMC_CLKENA register is programmed, the application should start another timer > 1ms.
4) By detecting SDCLK, the card drives CMD to high at 1. 8V for at least one clock and then stops driving (tri-state); CMD is triggered by the rising edge of SDCLK (SDR timing).
5) If switching to 1. 8V signaling is completed successfully, the card drives DAT [3:0] to high at 1. 8V for at least one clock and then stops driving (tri-state); DAT [3:0] is triggered by the rising edge of SDCLK (SDR timing). DAT[3:0] must be high within 1ms

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from the start of SDCLK.

6) The host controller generates a voltage switch interrupt (VOLT_SWITCH_INT) and a command done (CD) interrupt once the CMD and DAT[3:0] lines go high. The application should wait for this interrupt to confirm CMD and DAT lines going high before the 1ms timer is done.

If the timer expires without the voltage switch interrupt (VOLT_SWITCH_INT), a power cycle should be performed. Program the SDMMC_CLKENA register to stop the clock for the corresponding card number. Wait for the cmd_done (CD) interrupt. Proceed for normal operation on interrupt. After the sequence is completed, the host and the card start communication in SDR12 timing.

39.6.2.16 Voltage Switch Error Scenario

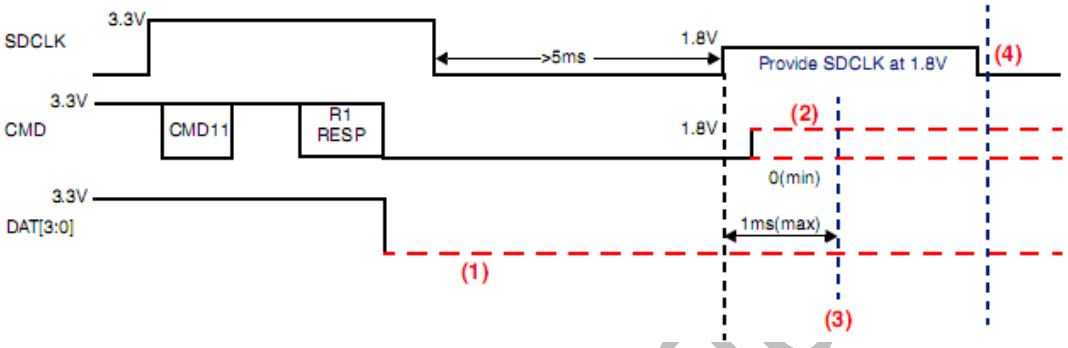

Fig. 39-14 Voltage Switch Error Scenario

1) If the interrupt (VOLT_SWITCH_INT) does not come, then the 2ms timer should time out and a power cycle should be initiated.

Note: Before performing a power cycle, switch off the card clock by programming SDMMC_CLKENA register; no cmd_done (CD) interrupt is generated.

Additionally, if the card detects a voltage error at any point in between steps (5) and (7) in the card keeps driving DAT[3:0] to low until card power off.

2) CMD can be low or tri-state.
3) The host controller generates a voltage switch interrupt once the CMD and DAT[3:0] lines go high. The application should check for an interrupt to confirm CMD and DAT lines going high before the 1 ms timer is done.

If the 1 ms timer expires without interrupt (VOLT_SWITCH_INT) and cmd_done (CD), a power cycle should be performed. Program the SDMMC_CLKENA register to stop SDCLK of the corresponding card. Wait for the cmd_done interrupt. Proceed for normal operation on interrupt.

4) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2. 5V. Errors are indicated by (1) and (2).

- If voltage switching is accepted by the card, the default speed is SDR12.
- Command Done is given:
  - If voltage switching is properly done, CMD and DAT line goes high.
  - If switching is not complete, the 1ms timer expires, and the card clock is switched off.

Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

- The application should use CMD6 to check and select the particular function; the function appropriate-speed should be selected.

After the function switches, the application should program the correct value in the CLKDIV register, depending on the function chosen. Additionally, if Function 0x4 of the Access mode is chosen—that is, DDR50, then the application should also program 1'b1 in DDR_REG for the card number that has been selected for DDR50 mode.

39.6.3 DDR Operation

39.6.3.1 4-bit DDR Programming Sequence

DDR programming should be done only after the voltage switch operation has completed. The following outlines the steps for the DDR programming sequence:

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1) Once the voltage switch operation is complete, the user must program voltage selection register to the required values for the corresponding card.

- To start a card to work in DDR mode, the application must program a bit of the newly defined SDMMC_UHSREG[16] register with a value of 1'b1.
- The bit that the user programs depends on which card is to be accessed in DDR mode.

To move back to SDR mode, a power cycle should be run on the card—putting the card in SDR12 mode—and only then should SDMMC_UHSREG[16]be set back to 1'b0 for the appropriate card.

39.6.3.2 eMMC4.5 DDR START Bit

The eMMC4.5 changes the START bit definition in the following manner:

1) Receiver samples the START bit on the rising edge.
2) On the next rising edge after sampling the START bit, the receiver must sample the data.
3) Removes requirement of the START bit and END bit to be high for one full cycle.

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the EMMC_DDR_REG register.

39.6.3.3 Reset Command/Moving From DDR50 to SDR12

To reset the mode of operation from DDR50 to SDR12, the following sequence of operations has to be done by the application:

1) Issue CMD0.
2) When CMD0 is received, the card changes from DDR50 to SDR12.
3) Program the SDMMC_CLKDIV register with an appropriate value.
4) Set ddr_reg to 0.

Note: The Voltage register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

39.6.4 H/W Reset Operation

When the RST_n signal goes low, the card enters a pre-idle state from any state other than the inactive state.

The following outlines the steps for the H/W reset programming sequence:

1) Program CMD12 to end any transfer in process.
2) Wait for DTO, even if no response is sent back by the card.
3) Set the following resets:

- DMA reset–SDMMC_CTRL [2] bit
- FIFO reset–SDMMC_CTRL [1] bit

Note: The above steps are required only if a transfer is in process.

4) Program the SDMMC_RSTN register with a value of 0; this can be done at any time when the card is connected to the controller. This programming asserts the RST_n signal and resets the card.
5) Wait for minimum of 1 µs or cclk_in period, whichever is greater
6) After a minimum of 1 µs, the application should program a value of 0 into the SDMMC_RSTN register. This de-asserts the RST_n signal and takes the card out of reset.
7) The application can program a new CMD only after a minimum of 200µs after the de-assertion of the RST_n signal, as per the MMC 4.41 standard.

Note: For backward compatibility, the RST_n signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

39.6.5 FBE Scenarios

An FBE occurs due to an AHB error response on the AHB bus. This is a system error, so the software driver should not perform any further programming to the Host. The only recovery mechanism from such scenarios is to do one of the following:

- Issue a hard reset by asserting the reset_n signal
- Do a program controller reset by writing to the SDMMC_CTRL[0] bit

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39.6.5.1 FIFO Overflow and Underflow

During normal data transfer conditions, FIFO overflow and underflow will not occur. However if there is a programming error, then FIFO overflow/underflow can result. For example, consider the following scenarios.

- For transmit: PBL=4, Tx watermark = 1. For the above programming values, if the FIFO has only one location empty, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pushes into the FIFO. This will result in a FIFO overflow interrupt.
- For receive: PBL=4, Rx watermark = 1. For the above programming values, if the FIFO has only one location filled, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pops to the FIFO. This will result in a FIFO underflow interrupt.

The driver should ensure that the number of bytes to be transferred as indicated in the descriptor should be a multiple of 4bytes with respect to H_DATA_WIDTH=32. For example, if the SDMMC_BYTCNT=13, the number of bytes indicated in the descriptor should be 16 for H_DATA_WIDTH=32.

39.6.5.2 Programming of PBL and Watermark Levels

The DMAC performs data transfers depending on the programmed PBL and threshold values.

Table 39-13 PBL and Watermark Levels

PBL (Number of transfers)	Tx/Rx Watermark Value
1	Greater than or equal to 1
4	Greater than or equal to 4
8	Greater than or equal to 8
16	Greater than or equal to 16
32	Greater than or equal to 32
64	Greater than or equal to 64
128	Greater than or equal to 128
256	Greater than or equal to 256

39.6.6 Variable Delay Usage

The control signals for variable delay element usage are described in SDMMC_CLKGEN_CON0 and SDMMC_CLKGEN_CON1.

The following outlines the steps for clock generation sequence:

1) Assert init_state to soft reset the CLKGEN.
2) Configure drv_degree/sample_degree.
3) If fine adjustment required, delay line can be used by configuring drv_delaynum/sample_delaynum and drv_sel/sample_sel.
4) Dis-assert init_state to start CLKGEN.

39.6.7 Variable Delay Tuning

Tuning is defined by SD and MMC cards to determine the correct sampling point required for the host, especially for the speed modes SDR104 and HS200 where the output delays from the cards can be up to 2 UI. Tuning is required for other speed modes-such as DDR50-even though the output delay from the card is less than one cycle.

Command for tuning is different for different cards.

- SD Memory Card:
  - CMD19 – SD card for SDR50 and SDR104 speed modes. Tuning data is defined by card specifications.
  - CMD6 – SD card for speed modes not supporting CMD19. Tuning data is the 64byte SD status.
- Multimedia Card:
  - CMD21 – MMC card for HS200 speed mode. Tuning data is defined by card specifications.
  - CMD8 – MMC card for speed modes not supporting CMD21. Tuning data is 512 byte ExtCSD data.

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The following is the procedure for variable delay tuning:

1) Set a phase shift of 0-degree on cclk_in_sample.
2) Send the Tuning command to the card; the card in turn sends an R1 response on the CMD line and tuning data on the DAT line.
3) If the host sees any of the errors—start bit error, data CRC error, end bit error, data read time-out, response CRC error, response error—then the sampling point is incorrect.
4) Send CMD12 to bring the host controller state machines to idle.
   - The card may treat CMD12 as an invalid command because the card has successfully sent the tuning data, and it cannot send a response.
   - The host controller may generate a response time-out interrupt that must be cleared by software.
5) Repeat steps 2) to 4) by increasing the phase shift value or delay element number on cclk_in_sample until the correct sampling point is received such that the host does not see any of the errors.
6) Mark this phase shift value as the starting point of the sampling window.
7) Repeat steps 2 to 4 by increasing the phase shift value or delay element number on cclk_in_sample until the host sees the errors starting to come again or the phase shift value reaches 360-degree.
8) Mark the last successful phase shift value as the ending point of the sampling window.

A window is established where the tuning block is matched. For example, for a scenario where the tuning block is received correctly for a phase shift window of 90-degree and 180-degree, then an appropriate sampling point is established as 135-degree. Once a sampling point is established, no errors should be visible in the tuning block.

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