Rockchip RK812 Datasheet

Revision 1.0
Nov.2019

Revision History

Date	Revision	Description
2019-11-11	1.0	Initial release

Table of Content

Figure Index

Table Index

Warranty Disclaimer

Rockchip Electronics Co.,Ltd makes no warranty, representation or guarantee (expressed, implied, statutory, or otherwise) by or with respect to anything in this document, and shall not be liable for any implied warranties of non-infringement, merchantability or fitness for a particular purpose or for any indirect, special or consequential damages.

Information furnished is believed to be accurate and reliable. However, Rockchip Electronics Co., Ltd assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties that may result from its use.

Rockchip Electronics Co.,Ltd's products are not designed, intended, or authorized for using as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Rockchip Electronics Co.,Ltd's product could create a situation where personal injury or death may occur, should buyer purchase or use Rockchip Electronics Co.,Ltd's products for any such unintended or unauthorized application, buyers shall indemnify and hold Rockchip Electronics Co.,Ltd and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Rockchip Electronics Co.,Ltd was negligent regarding the design or manufacture of the part.

Copyright and Patent Right

Information in this document is provided solely to enable system and software implementers to use Rockchip Electronics Co., Ltd 's products. There are no expressed or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Rockchip Electronics Co.,Ltd does not convey any license under its patent rights nor the rights of others.
All copyright and patent rights referenced in this document belong to their respective owners and shall be subject to corresponding copyright and patent licensing requirements.

Trademarks

Rockchip and Rockchip™ logo and the name of Rockchip Electronics Co.,Ltd's products are trademarks of Rockchip Electronics Co.,Ltd. and are exclusively owned by Rockchip Electronics Co.,Ltd. References to other companies and their products use trademarks owned by the respective companies and are for reference purpose only.

Confidentiality

The information contained herein (including any attachments) is confidential. The recipient hereby acknowledges the confidentiality of this document, and except for the specific purpose, this document shall not be disclosed to any third party.

Reverse engineering or disassembly is prohibited.

ROCKCHIP ELECTRONICS CO.,LTD. RESERVES THE RIGHT TO MAKE CHANGES IN ITS PRODUCTS OR PRODUCT SPECIFICATIONS WITH THE INTENT TO IMPROVE FUNCTION OR DESIGN AT ANY TIME AND WITHOUT NOTICE AND IS NOT REQUIRED TO UNDATE THIS DOCUMENTATION TO REFLECT SUCH CHANGES.

Copyright ©2019 Rockchip Electronics Co., Ltd.

Chapter 1 Introduction

1.1 Overview

The RK812 is a complex power-management integrated circuit (PMIC) integrated CODEC for multi-core system applications powered by a Li-ion or a Li-ion polymer battery cell, or by a 5V input either from an USB port or from an adaptor. The RK812 can provide a complete power management solution with very few external components.

The RK812 provides one configurable synchronous step-down converter. The device also contains 4 LDO regulators, one Linear-mode charger. Power-up/power-down controller is configurable and can support any customized power-up/power-down sequences (OTP based). It also includes Audio CODEC, Left/Right channel line out driver, Class-D driver, and 3 channel differential mode Micro-phone input.

The RK812 integrates one channel step-down DC-DC converter. It adopt ripple base control to achieve very fast load transient response. Meanwhile, the output voltage can be configured through the I2C interface. The inputs of BUCK have soft start function, which greatly reduces the inrush current at the startup. 2.0MHz switching frequency and good control method decrease the external inductance and capacitance.

The RK812 integrates 4 channels LDO regulators. The inputs of all LDO regulators could be decrease to 2V for high convert efficiency. The output voltages of all LDO regulators can be configured through the I2C interface.

The linear-mode charger in the RK812, allows supplying power to the loads while it is charging the battery. The charger provides functions such as trickle current charging, constant current (CC)/constant voltage (CV) charging, charging termination, charging over time protection, etc. All these functions can be conveniently configured through the I2C digital interface. Also, the temperature of RK812 could be feedback to reduce charge current automatically.

The RK812 also integrates complete audio system. Three channels differential mode Micro-phone can be connected to RK812 through AC-couple capacitors. 24-bits ADC and gain adjustable PGA would convert the micro-phone signal to digital signal. The sound recording path has very low THD (-70dB @1KHz@580mV source). 24 bits DAC would convert digital signal to analog signal, and Class-AB line-out driver for loudspeaker box application has very low THD (-85dB @1KHz@-8dBFS source). Meanwhile, Class-D driver integrated for speaker application. The speaker and loudspeaker box can be used at the same time. Special interface is integrated to communicate with Rockchip processor.

The RK812 is available in a QFN36 4.0 mm x 4.0 mm package, with a 0.35-mm pin pitch.

1.2 Feature

- Input range: 3.8V – 5.5V for USB input； 2.7V - 5.5V for BAT input
- Low shutdown current of 10uA (keep some registers data)
- Power channels:
  - BUCK: 0.5V~2.4V, 1.5A max, very fast transient response
  - LDO1: 0.6V~3.4V, 600mA max
  - LDO2: 0.6V~2.0V, 400mA max
  - LDO4: 0.6V~3.4V, 100mA max
  - LDO5: 1.8V~3.4V, 100mA max

- OTP Programmable power up/down sequences and voltage
- Linear mode Li-ion battery charger
  - Charger to battery current: 0.1A~1A
  - Charger termination voltage: 4.1V~4.45V
  - Constant temperature charge function
  - Charge time out protection
- Audio System
  - Audio codec: 24bits for both ADC and DAC
  - Support 3 channels differential mode Micro-phone input
  - Support class-AB PA to drive loudspeaker box, 600 Ohm Load
  - Support class-D PA to drive speaker, 1.7W @ 4V input
  - Support Special interface for both DAC and ADC path
  - Support programmable digital and analog gains
- Package:4mmx4mm QFN36, 0.35-mm pin pitch

1.3 Typical Application Diagrams

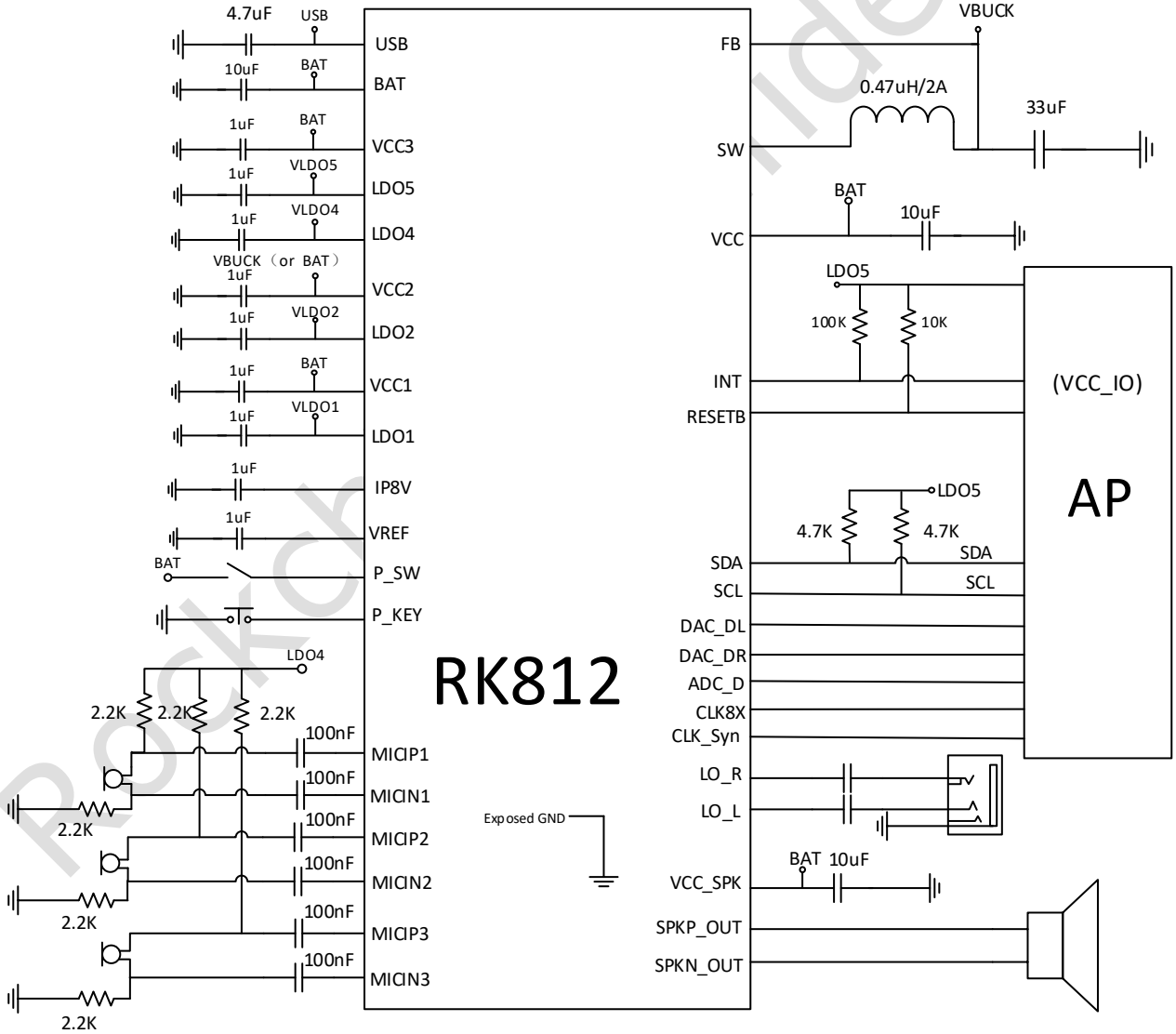


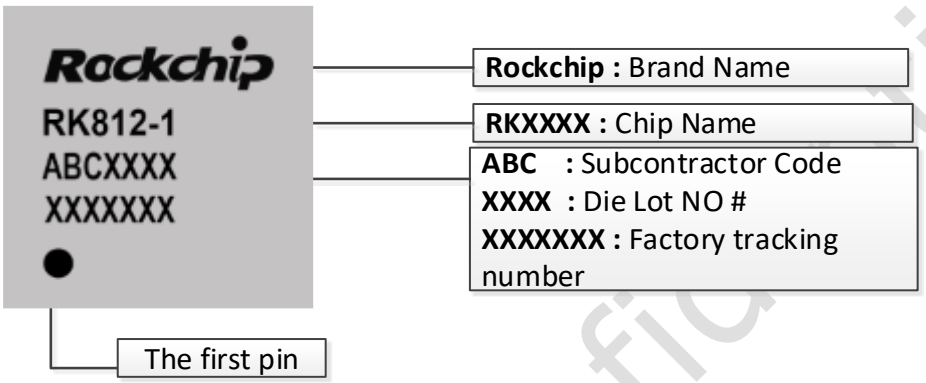
Fig. 1-1 RK812 Typical Application Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty
RK812-1	RoHS	QFN36(4X4)	3000pcs by reel

2.2 Top Marking



2.3 Dimension

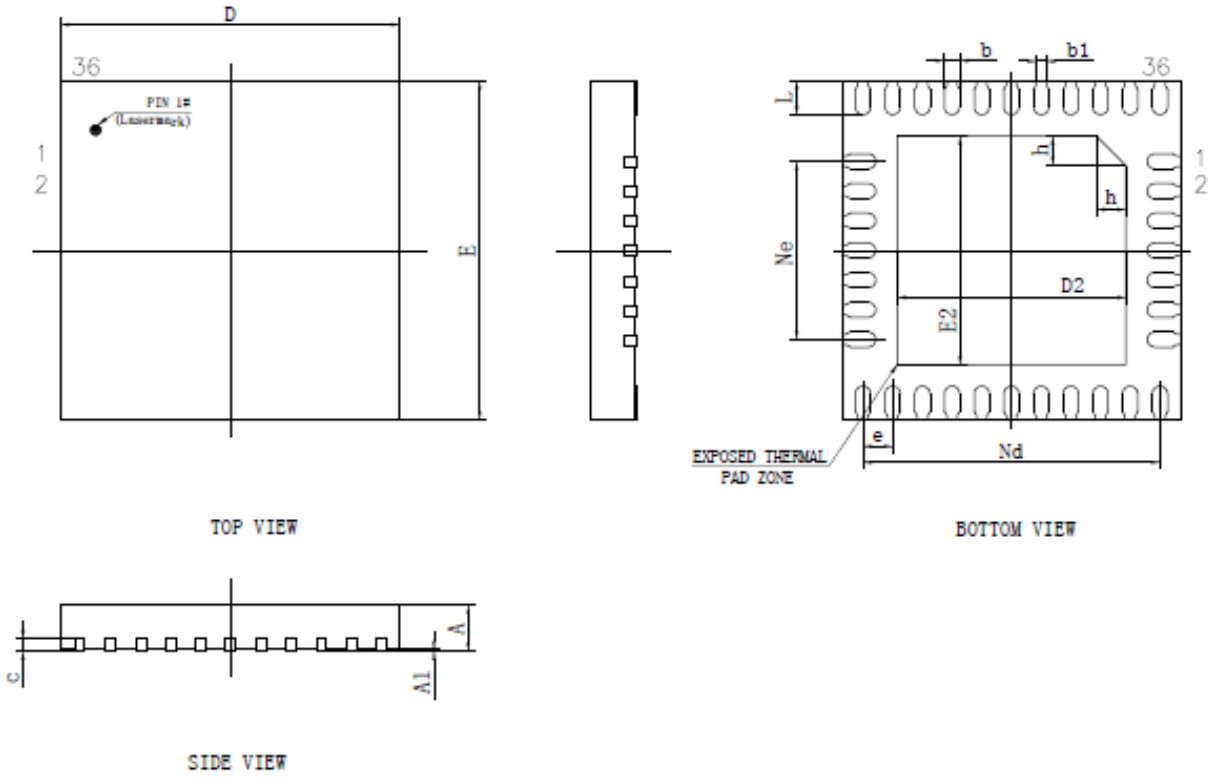


Fig. 2-1 QFN36 4mm x 4mm

DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1		0.02	0.05
MATERIAL THICKNESS	c	0.10	0.15	0.2
PACKAGE SIZE	D	3.90	4.00	4.10
	E	3.90	4.00	4.10
EP SIZE	D2	2.60	2.70	2.80
	E2	2.60	2.70	2.80
LEAD LENGTH	L	0.35	0.4	0.45
LEAD WIDTH	b	0.13	0.18	0.23
LEAD PITCH	e	0.35BSC		
LEAD WIDTH	b1	0.12REF		
PIN PITCH	Ne	2.10BSC		
PIN PITCH	Nd	3.50BSC		
SIZE	h	0.30	0.35	0.4

Note:

1. *Coplanarity applies to leads, corner leads and die attach pad.*
2. *Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.*

2.4 Pin Assignment

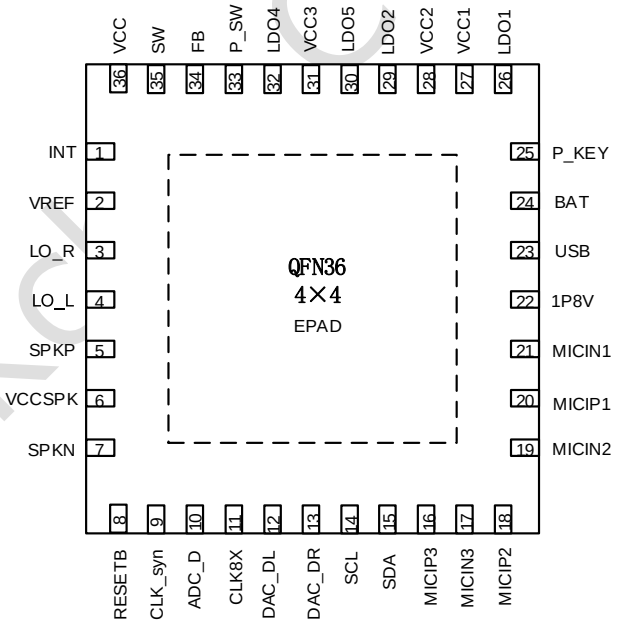


Fig. 2-2 Pin Assignment QFN4x4-36(Pitch=0.35mm)

2.5 Pinout Number Order

PIN NO	PIN NAME	I/O DESCRIPTION	PIN DESCRIPTION
1	INT	Output	Interrupt request pin, open drain
2	VREF	Output	Reference voltage, ties a filter cap.
3	LO_R	Output	Right channel Line out output
4	LO_L	Output	Left channel Line out output
5	SPKP	Output	Positive speaker driver output.
6	VCCSPK	Input	Power supply for speaker
7	SPKN	Output	Negative speaker driver output
8	RESETB	Input / Output	Reset pin after power on, active low;
9	CLK_syn	Input	Synchronous clock for Codec
10	ADC_D	Output	Codec ADC Output Data
11	CLK8X	Input	Sample Clock for Codec 6.144MHz*8
12	DAC_DL	Input	Codec Input Data for left channel
13	DAC_DR	Input	Codec Input Data for right channel
14	SCL	Input	I2C clock input
15	SDA	Input/ Output	I2C data input and output(Open drain output)
16	MICIP3	Input	Positive input of the Microphone3
17	MICIN3	Input	Negative input of the Microphone3
18	MICIP2	Input	Positive input of the Microphone2
19	MICIN2	Input	Negative input of the Microphone2
20	MICIP1	Input	Positive input of the Microphone1
21	MICIN1	Input	Negative input of the Microphone1
22	1P8V	Output	1.8V LDO Output for codec and digital block use
23	USB	Input	USB input
24	BAT	Input	Positive Battery Terminal
25	P_KEY	Input	Power on/power down key input, active low, internal 12k resistor pull up. Connect this pin with a mechanical key to GND.
26	LDO1	Output	LDO1 output
27	VCC1	Input	Power supply of LDO1
28	VCC2	Input	Power supply of LDO2
29	LDO2	Output	LDO2 output
30	LDO5	Output	LDO5 output
31	VCC3	Input	Power supply of LDO4,5
32	LDO4	Output	LDO4 output
33	P_SW	Input	Connect this pin with a mechanical switch to BAT. Power on or power down switch.
34	FB	Input	Output feedback voltage of BUCK
35	SW	Output	Switching node of BUCK
36	VCC	Input	Power supply of BUCK
EPAD	EPAD		Ground

Chapter 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
Voltage range on pins USB, VCC, SW, VCC1~3,VCC_SPK,LDOx, BAT, FB, SPKP_OUT, SPKN_OUT, P_SW, PKEY, CLK_syn, CLK8X,DAC_DR, DAC_DL, ADC_D	-0.3	6.5	V
Voltage range on pin RESETB, SCL,SDA,INT	-0.3	6.5	V
Voltage range on pins VREF, 1P8V, MIC1N,MIC1P, MIC2N,MIC2P,MIC3P,MIC3N, LO_L, LO_R,	-0.2	1.98	V
Storage temperature range, T_S	-40	150	℃
Operating temperature range, T_J	-40	125	℃
Maximum Soldering Temperature, T_{SOLDER}		300	℃

Note：

Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

3.2 Recommended Operating Conditions

Parameter	Min	TYP	Max	Units
Voltage range on pins USB	4	5	5.5	V
Voltage range on pins BAT	3	4.2	4.6	V
Power Dissipation			TBD	W

3.3 DC Characteristics

Test conditions: BAT=4.0V,TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Power dissipation						
Shut down Current	Isd			10		uA
Power on current 1: All BUCKs, LDOs, Null load	Iq1			0.35		mA
Power on and sleep current: All BUCKs, LDOs, Null load, low power mode, sleep mode	Isleep			0.22		mA
System Characteristics						
VB_OK threshold, the battery voltage should be higher than it to power on the PMIC.	Vok	2.8V~3.6V by OTP programmed. Typical is 3.3V.	3.234	3.3	3.366	V
VB_UV threshold, when the SYS voltage is lower than it, The PMIC would be shutdown.	Vuv	2.7V~3.4V by I2C programmed. Typical is 2.7V.	2.646	2.7	2.754	V
VB_LO threshold, when the SYS voltage is lower than it, The PMIC would be shut down or interrupt happen.	Vlo	2.8V~3.5V by I2C programmed. Typical is 3.2V.	3.136	3.2	3.264	V
TSD threshold, when the temperature is higher than it, The PMIC would be shutdown.	Tsd	140/160° C by I2C programmed. Typical is 160° C.	155	160	165	° C
T warning threshold, when the temperature is higher than it, interrupt happen.	Twa	85/115° C by I2C programmed.	110	115	120	° C

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
		Typical is 115° C.				
Long press P_KEY time	Tlp	0.1S~16S by I2C programmed. Typical is 8S.		8		S
Short press P_KEY time	Tst	20mS/500mS by I2C programmed and OTP programed. Typical is 20mS.		20		mS
P_SW falling edge shutdown PMIC de-bounce time	Tfs	0.1S~16S by I2C programmed. Typical is 0.5S.		0.5		S
P_SW rising edge start PMIC de-bounce time	Trs	0.1mS~60mS by I2C programmed and OTP programed. Typical is 1mS.		1		mS

Test conditions: BAT=VCCx=4.0V, TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
BUCK: Fast load transient response step-down converter						
Input supply voltage range	Vcc		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb	0.5V~2.4V by I2C programmed. Typical is 1.8V. Step=12.5mV(0.5 V~1.5V) Step=100mV(1.5 V~2.4V)	1.773	1.8	1.827	V
Load Transient Response L=0.47uH ,Cout=33uF	Vdrop(peak to peak)	0.1A to0.75A, Vout=1.8V AUTO PFM mode Reg_BA: 77H		17.6		mV
		0.1A to1.5A, Vout=1.8V AUTO PFM mode Reg_BA: 77H		34.4		mV
Rated output current	Imax	0.5A~1.5A by OTP, Step=125mA	0.5	1.0	1.5	A
Switching Frequency when CCM mode	Fsw	Vin-Vout>1.5V	1.85	2.0	2.25	MHz
Conversion Efficiency(Vin=4.2V,Vout=1.8V) Iout=1.5A Iout=1A Iout=0.3A		L=0.47uH, Cout=33uF. AUTO PFM mode		83.4 86.5 87		%
LDO1						
Input supply voltage range	Vcc1		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo1	0.6V~3.4V by I2C programmed. Typical is 3.3V. Step=25mV	3.234	3.3	3.336	V
Rated output current	Imaxl1	Vcc1- Vldo1>0.3V		600		mA
		Vcc1- Vldo1>0.2V		400		mA
		Vcc1- Vldo1>0.1V		200		mA
Drop-out voltage	Vdrop-out1	@ 600mA		400		mV
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
LDO2						
Input supply voltage range	Vcc2		1.8		5.5	V

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Output Voltage Accuracy @ all load @ all input voltage range	Vldo2	0.6V~2V by I2C programmed. Typical is 1.1V. Step=12.5mV	1.078	1.1	1.122	V
Rated output current	Imaxl2			400		mA
Drop-out voltage	Vdrop-out2	@ 400mA		300		mV
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
LDO4						
Input supply voltage range	Vcc3		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo4	0.6V~3.4V by I2C programmed. Typical is 1.8V. Step=25mV	1.764	1.8	1.836	V
Rated output current	Imaxl4			100		mA
Drop-out voltage	Vdrop-out3	@100mA		200		mV
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
LDO5						
Input supply voltage range	Vcc3		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo5	1.8V~3.4V by I2C programmed. Typical is 1.8V. Step=25mV	1.764	1.8	1.836	V
Rated output current	Imaxl5			100		mA
Drop-out voltage	Vdrop-out4	@ 100mA		200		mV
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB

Test conditions: VUSB=5V, BAT=4.0V, TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Line mode charger						
USB Operating Range	Vusb		3.8	5	5.5	V
Drop-out voltage	Vdrop-out	@1000mA		300		mV
Charge constant current	Ichrg_cc	0.1A~1A by I2C programmed. Typical is 0.45A.	0.432	0.45	0.468	A
Charge constant voltage	Vchrg_cv	4.1V~4.45V by I2C programmed. Typical is 4.2V.	4.18	4.2	4.22	V
Trickle charge current	Ichrg_trick	10% Ichrg_cc	40	45	50	mA
Charge terminal current	Ichrg_term	.10%/20% Ichrg_cc by I2C programmed. Typical is 10%.	40	45	50	mA
Charge time out @CCCV mode	Tchrg_cccv	4H~8H by I2C programmed. Typical is 6H.		6		H
Charge time out @Trickle mode	Tchrg_trick	30min~90min by I2C programmed. Typical is 60min.		60		Min
Trickle charge Maximum Voltage: when battery voltage is higher than it, charge state goes to CCCV mode	Vchrg_trick			3		V
Trickle charge Voltage hysteresis (falling)	Vchrg_trick_hys			0.2		V

Test conditions: VCC_SPK=4V, BAT=4.0V, TA=25°C for typical values, unless

otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
ClassD Audio PA						
Input supply voltage range	Vccspk	VCC_SPK	2.7		5.5	V
THD+N		1KHz, Po=0.4Wrms, VCC_SPK =4V		0.1		%
RMS Power		4 ohm load, VCC_SPK =4V, THD+N=1%		1000		mW
		4 ohm load, VCC_SPK =4V, THD+N=10%		1700		mW
PSRR		217Hz, VCC_SPK =200mVpk-pk+3.8 V,		65		dB
Output Offset Voltage		VCC_SPK=4V	- 15		+ 15	mV
Noise Level		VCC_SPK =4V 0dB Gain, 4ohm, A-weighted		100		uV
Efficiency		VCC_SPK=4V,0.4W, 4ohm with 68uH, 1KHz		88		%
Quiescent current		No load, VCC_SPK =4V		1.5		mA
DAC to Line-out outputs						
Resolution				24		bit
DAC Digital Filter Pass Band			20		20K	Hz
DAC Digital Filter Pass Band Ripple				0.1		dB
Line-out outputs						
Load resistance				600	10K	Ohm
Load capacitance				22		uF
Output Amplitude				0.38		Vrms
Gain Range			0		-16	dB
Gain Step				-1		dB
Dynamic Range		A-Weight filter open, No boost in Line Out stage，-60dBFs input, 20~20K Bandwidth		90		dB
Total Harmonic Distortion + Noise	THD+N	A-weighted RL=600ohm -8dBFS Fs=1KHz		85		dB
Signal to Noise Ratio	SNR	A-weighted RL=600ohm，-60dBFS，Fs=1KHz		90		dB
Crosstalk		One channel drive 100mVrms signal		90		dB
ADC @48k sample						
Full sale input voltage		Vpp		1.4(±0.7)		V
Resolution				16		bit
SNR		A-weighted，-3dBFS,Fs=1KHz		80		dB
THD+N		A-weighted 997Hz -3dBFS Differential input signal, Fs=1KHz		-70		dB
Dynamic Range		A-Weight filter open, No boost in PGA stage，-60dBFs input, 20~20K		90		dB

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
		Bandwidth				
Digital Filter Pass Band			20		20K	Hz
Digital Filter Pass Band Ripple				0.1		dB
Crosstalk		One channel drive 100mVrms signal		80		dB
Power Consumption		1.8V power supply, one channel			1.36	mW
PGA（MIC INPUT）						
Input Resistor				50K		Ohm
Input Cap				10		pF
Gain Range			0		30	dB
Gain Step		4bit Control		2		dB/ step
Gain Shrink		Another gain stage at input port	-9		0	dB
Gain Step		2bit Control		3		dB/ step

Test conditions: BAT=4.0V, TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
I2C interface (7bits I2C address is 0x24)						
SCL clock frequency	f_{SCL}			400	1000	KHz
LOGIC INPUT: SCL, SDA, RESETB，DAC_D, DAC_DR，CLKX8，CLK_Sync, P_KEY, P_SW						
Input LOW-Level Voltage	V_{IL}				0.3*VLDO5	V
Input HIGH-Level Voltage:	V_{IH}		0.7* VLDO5			V
LOGIC OUTPUT: ADC_D						
LOW-Level Output Voltage, 3.0 mA sink current	V_{OL}				0.3*VLDO5	V
HIGH-Level Output Voltage, 3.0 mA source current:	V_{OH}		0.8* VLDO5			V
OPEN DRAIN OUTPUT PIN						
RESETB,INT,SDA						
Output resistor				10		Ohm

Chapter 4 Function Description

4.1 Top State Machine

4.1.1 State Machine Description

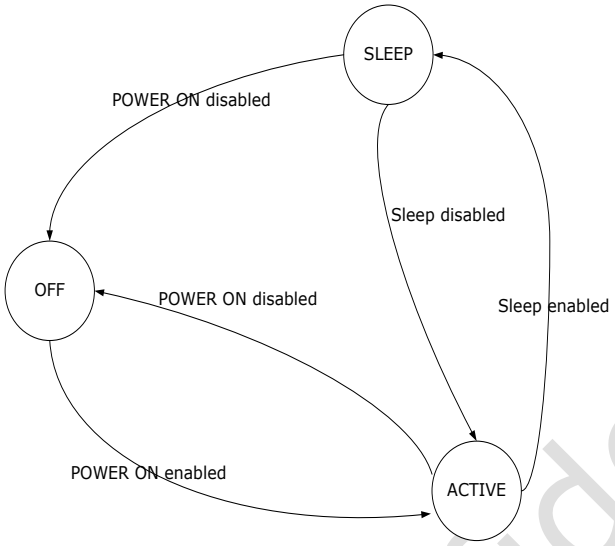


Fig. 4-1 State Machine

The RK812 state machine shown as above. The state shift by "power on", "power down", "reset", "active to sleep" and "sleep to active".

4.1.2 Power on Description

There are three kinds of method to power on the PMIC.

1. Press "P_KEY" key

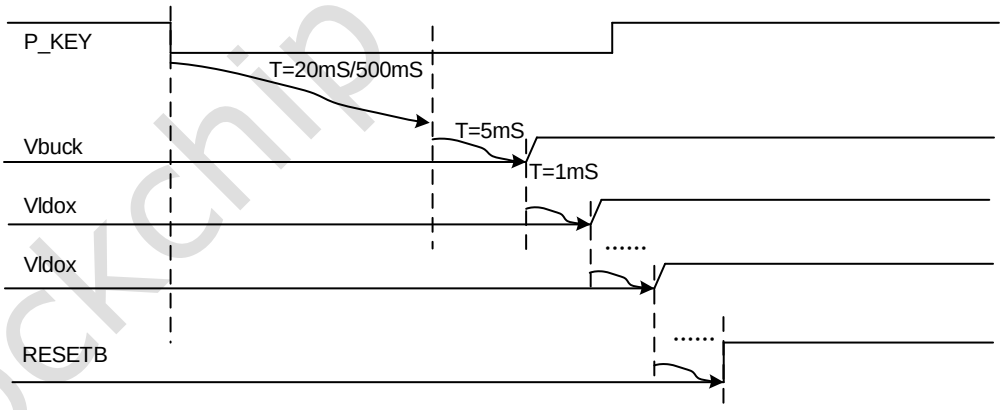


Fig. 4-2 Press "P_KEY" key to turn on the PMIC

When the PMIC powered by a battery which voltage is higher than "VB_OK" threshold (typical 3.3V), keeping low level at "P_KEY" pin for 20mS /500mS would turn on the PMIC. The "P_KEY" pin de-bounce time (20mS/500mS) can be adjusted by I2C or OTP.

All the power channels start up at the default output voltages with a preset power up sequence, which has 1mS intervals between the channels. When the power up process is done, the RESETB turns to high logic level to inform the processor that all the power rails are up and stable.

2. "P_SW" Rising edge

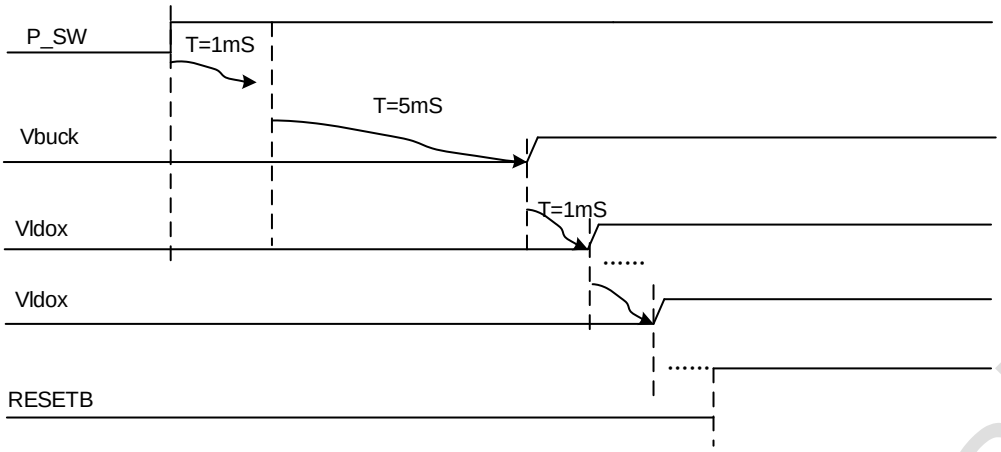


Fig. 4-3 Press "P_SW" key to turn on the PMIC

When the PMIC powered by a battery which voltage is higher than "VB_OK" threshold (typical 3.3V),The "P_SW" pin rising edge for 1mS would turn on the PMIC. The "P_SW" pin de-bounce time (0.2mS~60mS) can be adjusted by I2C or OTP.

3. USB Plug in

When USB plug in（VUSB>3.8V）,linear charger will be work,if the BAT voltage is higher than "VB_OK" threshold (typical 3.3V), the PMIC would be turn on, The power on sequence shown as below.

Note: If when USB keep attached, and then the PMIC is turn off, the PMIC would NOT turn on again. This is a function that charging in "OFF" state. Users must plug out the USB, and then plug in again to turn on the PMIC.

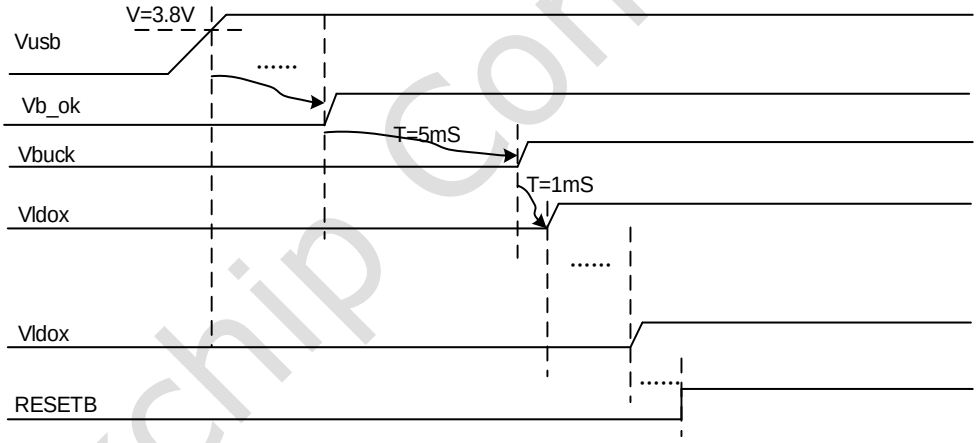


Fig. 4-4 USB plug in to turn on the PMIC

4.1.3 Power down Description

There are 6 kinds of method to power down the PMIC.

1. Long press "P_KEY" key

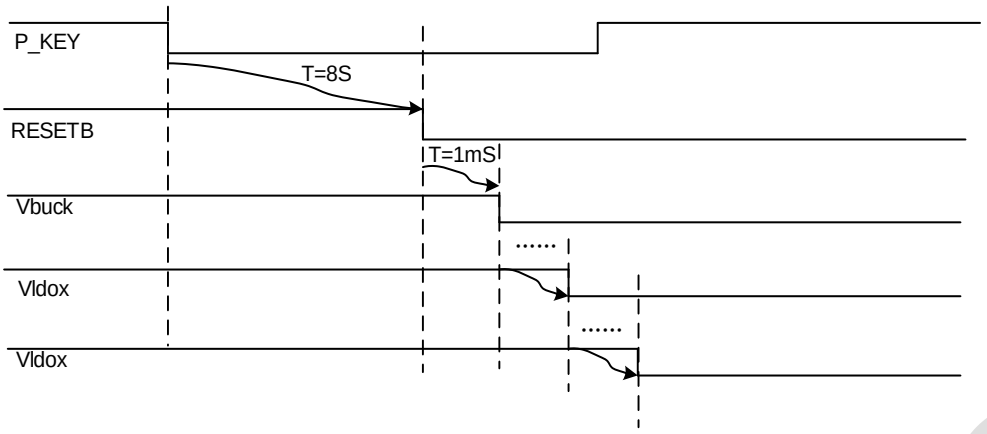


Fig. 4-5 Long press "P_KEY" key to turn off the PMIC

When the PMIC work in the "ON" state or "SLEEP" state, and then keeping low level at "P_KEY" pin for 8S would turn off the PMIC. The "P_KEY" pin de-bounce time (0.5~16S) can be adjusted by I2C.

When power down enable, The RESETB pin would be pulled low to reset the processor. And then 1ms later, the power channels start to be turned off opposite to start-up. In the other mode, the power channels start to be turned off at the same time.

2. Write shutdown Register

When the PMIC work in the "ON" state or "SLEEP" state, writing register bit 0xF4<0>="1" would turn off the PMIC. The power off sequence is the same with the first one.

3. P_SW falling edge

When the PMIC work in the "ON" state or "SLEEP" state, if "P_SW" pin falling edge occurs, the PMIC would be turn off. The power off sequence is the same with the first one.

4. BAT under-voltage

When the PMIC work in the "ON" state or "SLEEP" state, if VBAT lower than VB_UV threshold (typical 2.7V) for 30uS, the PMIC would be turn off. For safe attention, the BUCK converter would be shut down immediately when detect VB_UV.

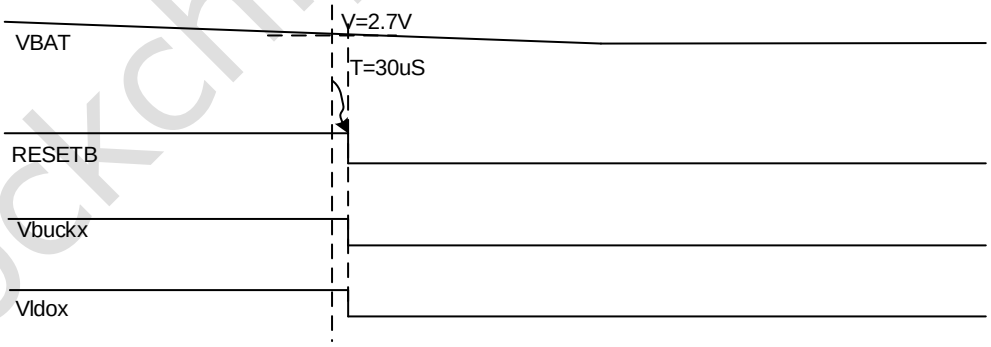


Fig. 4-6 VSYS under-voltage to turn off the PMIC

5. BAT low-voltage

When the PMIC work in the "ON" state or "SLEEP" state, if VBAT lower than VB_LO threshold (typical 3.2V) for 2mS and Register bit 0XF1<3>="0", the PMIC would be turn off. The power off sequence is the same with the first one.

6. TSD protection

When the PMIC work in the "ON" state or "SLEEP" state, if the temperature is higher than TSD threshold (typical 160 degree), the PMIC would be turn off. The power off sequence is the same with the first one.

4.1.4 Reset Description

There are 2 kinds of method to reset the PMIC. If register bits 0xF4<7:6>="00", reset function means restart PMIC. If register bits 0xF4<7:6>="01", reset function means reset registers, all channels of power would be reset to default state.

1. RESETB pin pull low

When the PMIC work in the "ON" state or "SLEEP" state, if "RESETB" pin is pull down, the PMIC would restart immediately. The restart sequence is the same with the first one.

Note: If the battery voltage is lower than VB_OK threshold, the PMIC would be shut down.

2. Write reset register

When the PMIC work in the "ON" state or "SLEEP" state, writing register bit 0xF4<2>="1" would reset the PMIC. The power off sequence is the same with the first one.

4.1.5 Power Sequence Description

			RK812-1	
	Range of output voltage	Maximum output current	Default voltage	Startup sequence
BUCK	0.5V-2.4V	1.5A	1.8V	1
LDO1	0.6V-3.4V	600mA	3.3V	3
LDO2	0.6V-2.0V	400mA	1.1V	2
LDO4	0.6V-3.4V	100mA	1.8V	3
LDO5	1.8V-3.4V	100mA	1.8V	3
RESETB			IO	7

Table 4-1 Power up/down sequence

4.1.6 Sleep Description

The RK812 could be set to SLEEP mode by write register bits 0xF4<4:3>="01", 0xF4<1>="1"

When sleep mode, the power dissipation of RK812 would be decreased. Writing register bits 0xB9<0>="1", 0xB9<7>="1" would be decrease quiescent current further.

4.2 Power Channels

4.2.1 BUCK Description

The RK812 provides one high current synchronous BUCK converters, which deliver up to 1.5A. An enhanced COT architecture is used, which improves the transient response significantly. 2.0MHz switching frequency and good control method decrease the external inductance and capacitance. The output voltages can be adjusted dynamically during operation through I2C interface. A complete set of protection functions, such as short circuit protection, is implemented in the BUCK converters too.

For example, At the AUTO PFM mode, the BUCK:Vout =1.8V,Vin=4V, L=0.47uH, Cout=33uF, Reg_BA: 77H, Load Current transient from 0.1A to1.5A, the peak to peak of output voltage is 34.4 mV. And load Current transient from 0.1A to 0.75A, the peak to peak of output voltage is 17.6 mV, that is very good characteristics.

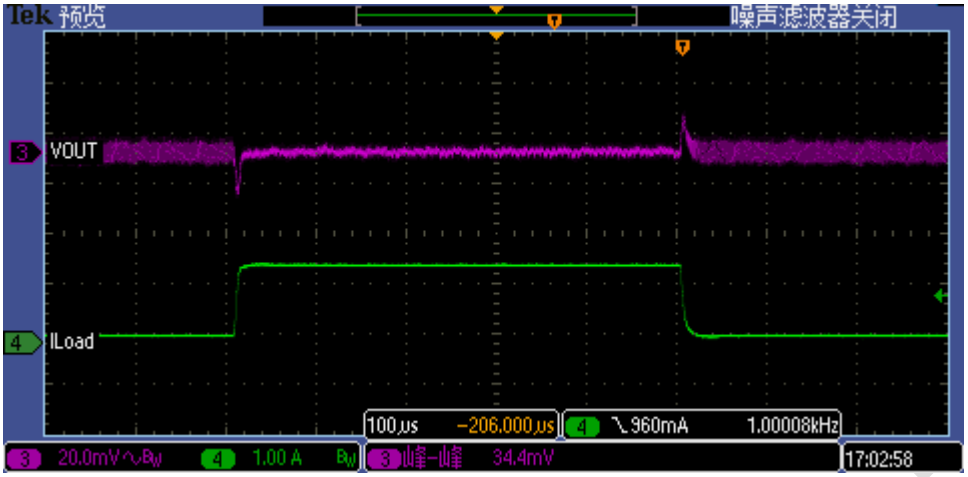


Fig. 4-7 BUCK load transient from 0.1A to 1.5A

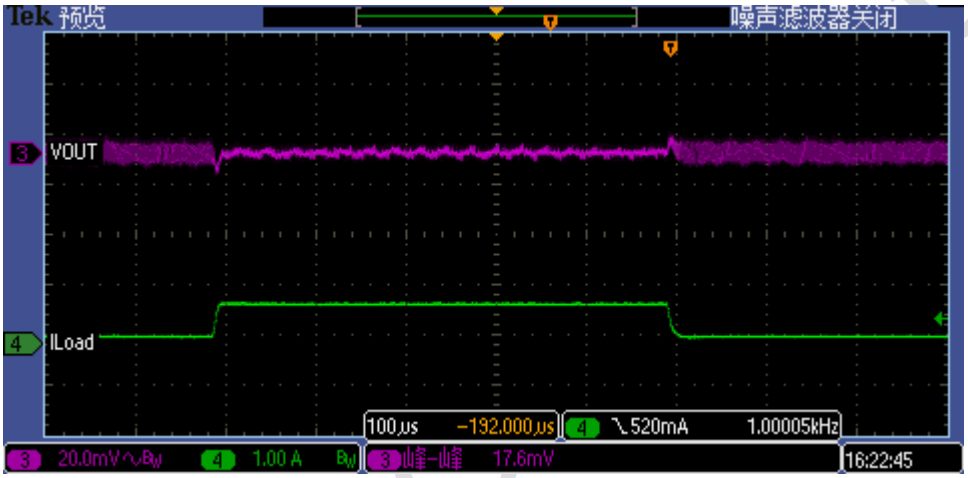


Fig. 4-8 BUCK load transient from 0.1A to 0.75A

Meanwhile, BUCK converters have good efficiency characteristics. The test data shown as below. The channel of BUCK output voltage set to default.

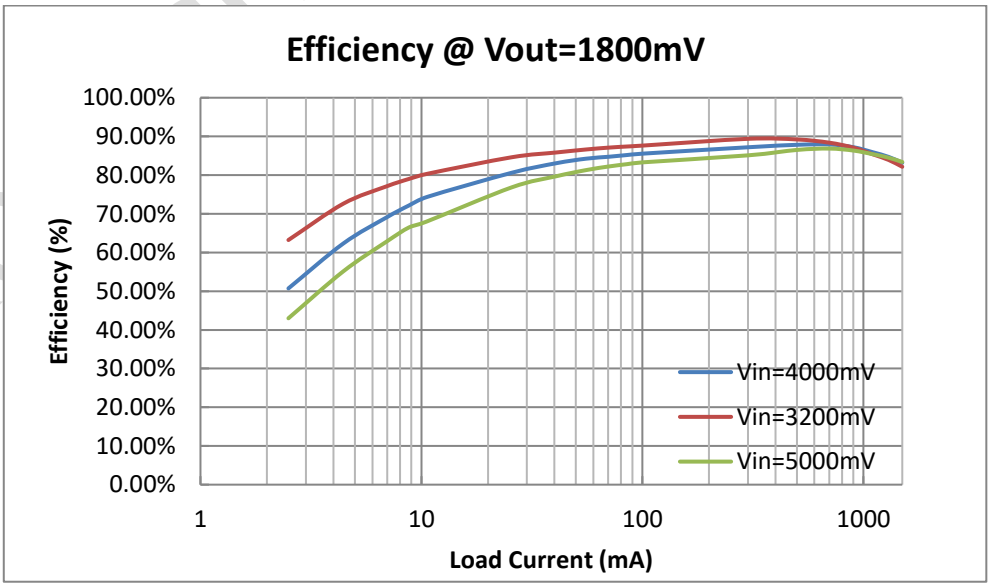


Fig. 4-9 BUCK efficiency curve when different input voltage

4.2.2 LDO Description

The RK812 also integrates LDO1,LDO2,LAO4,LAO5, with capable of providing up to 600mA/400mA/ 100mA/ 100mA respectively. The PSRR is about 65dB @1KHz. All channels of LDO output capacitance could be 1.0uF that decreases the system cost. The parameters such as output voltage in the different operating modes can be adjusted through the I^2C interface.

4.3 Linear Charger

4.3.1 Charger Description

This charger which provides the functions like trickle current charging, constant current charging, constant voltage charging, charging termination, automatic recharging, battery temperature monitoring, charging timer and thermal feedback protection. The values of constant current and constant voltage charging can be set through I^2C interface.

The charger also has a timer function which sets the maximum charging time for trickle, constant current and constant voltage charging, respectively. If the charging does not complete when a preset maximum charging time is reached, the charging will be terminated.

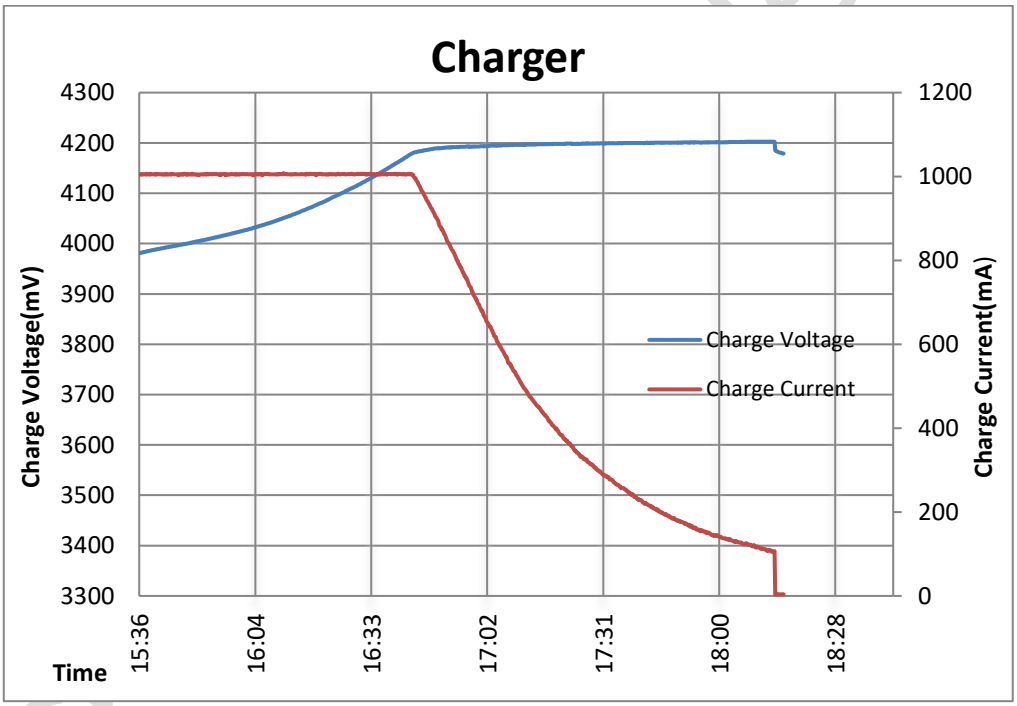


Fig. 4-10 Charge curve

4.4 Audio System

4.4.1 General Description

The RK812 integrates three high performance 24 bits ADC and three high performance 24 bits DAC. The audio recording path is composed of MIC_PGA and audio ADC. DAC would convert digital signal to analog signal, and Class-AB driver for loudspeaker box application, has very low THD (-85dB @1KHz@-8dBFS source). Meanwhile, Class-D driver integrated for speaker application. The speaker and loudspeaker box can be used at the same time.

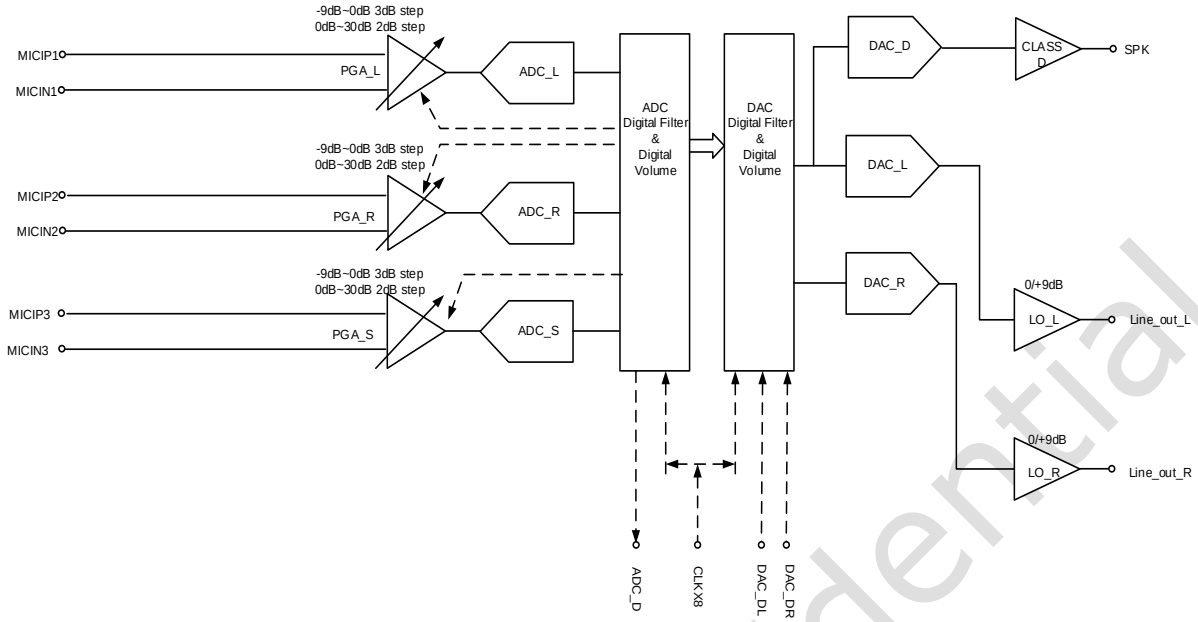


Fig. 4-11 Audio system architecture

4.4.2 Audio Recording Path Description

The RK812 integrate complete audio recording path solution. Users should set registers as below to configure audio recording path. For example, sample rate is 48K, CLK8X=6.144MHz*8；and CLK_syn=6.144MHz.

1. ADC_mode_en: 0x1E=21H.
2. Enable ADC bias and vag: 0x21=00H
3. Enable ADC_L 0x24=10H、 0x22=48H
4. Enable ADC_R 0x24=20H、0x22=88H
5. Enable ADC_S 0x25=10H、0x23=48H
6. Enable ADC_B 0x25=20H、0x23=88H (RK802 application only)

(if need all three ADCs open, write 0x24=00H 0x25=00H)

The audio recording path THD+N ratio test data shown as below: typical case is -70dB.

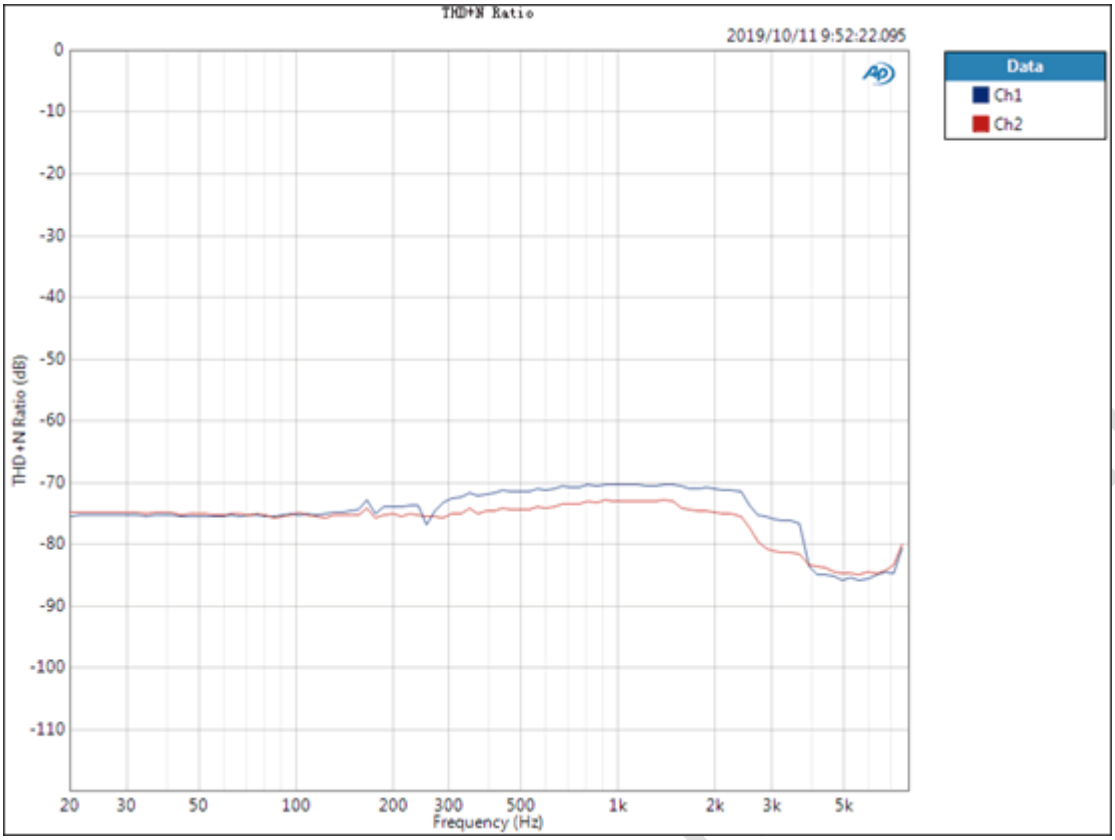


Fig. 4-12 Audio recording path THD+N ratio at ADC1 and ADC2

4.4.3 Loudspeaker box Path Description

The RK812 integrates a stereo output and with cap-free type loudspeaker box. It doesn't need to connect external capacitance, and can connect to loudspeaker box directly.

Users should set registers as below to configure loudspeaker box. For example, sample rate is 48K, CLK8X=6.144MHz*8.

1. Enable reference: 0x21=00H.
2. Enable DAC: 0x1E=04H, 0x2B=04H.
3. Enable Line-out: 0x2F=86H.

The loudspeaker box THD+N ratio test data shown as below: typical case is -85dB.

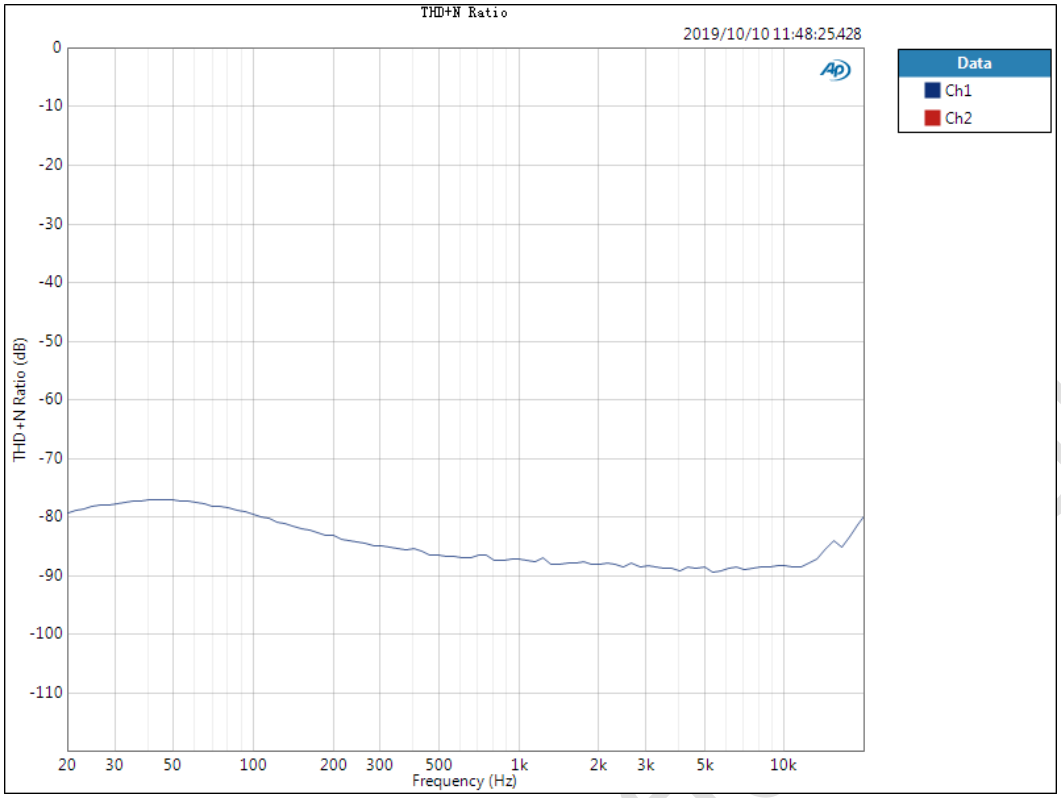


Fig. 4-13 loudspeaker box THD+N ratio

4.4.4 Speaker Path Description

The RK812 integrates a high efficiency stereo Class-D type amplifier capable of delivering 1.7W of power on a 4ohm BTL load from a 4V power supply. It integrates over-current protection.

Users should set registers as below to configure Speaker path. For example, sample rate is 48K, CLKX8=6.144MHz*8.

1. Enable reference: 0x21=00H.
2. Enable DAC: 0x1E=04H, 0x2B=03H.
3. Enable Class D: 0x31=a1H.

The Speaker path THD+N ratio test data shown as below: typical case is -60dB.

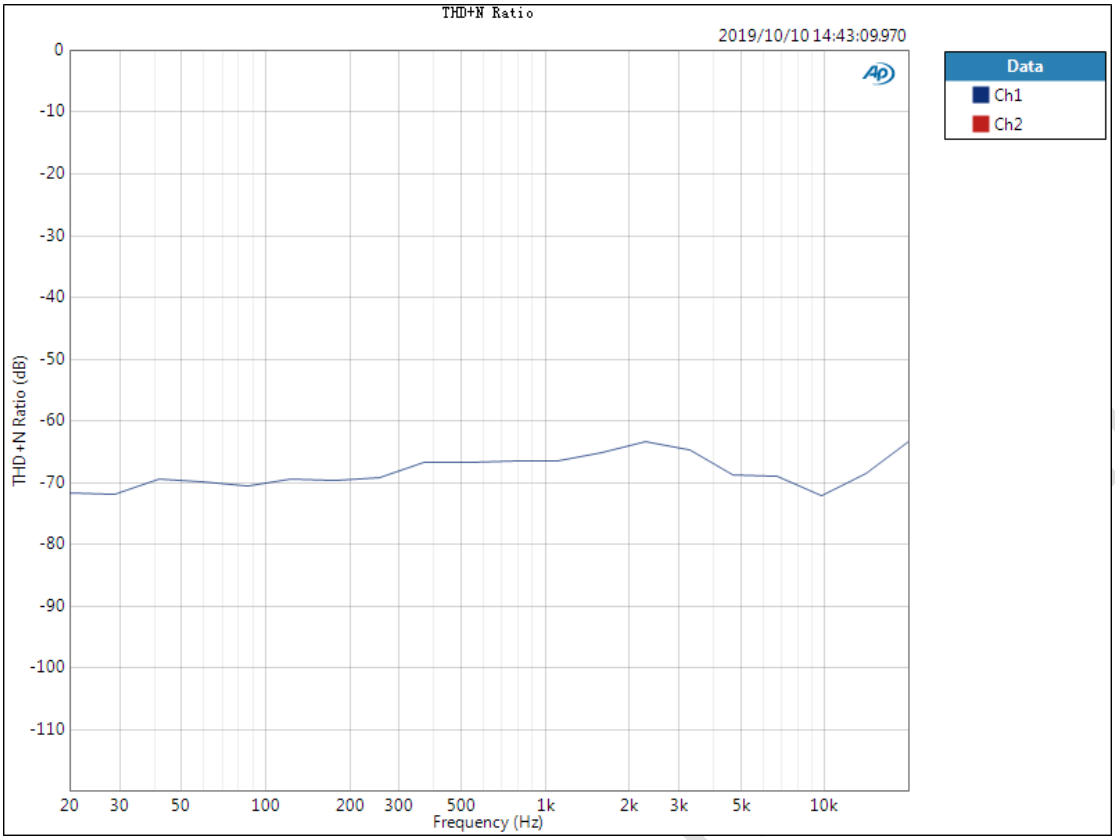


Fig. 4-14 Speaker path THD+N ratio

Chapter 5 Register Description

5.1 Register Summary

Name	Offset	Size	Reset Value	Description
CODEC_DTOP1	0x001e	B	0x00	
CODEC_DTOP2	0x001f	B	0x77	
CODEC_AREF_CFG0	0x0020	B	0x00	
CODEC_AREF_CFG1	0x0021	B	0x06	
CODEC_ADC_CFG0	0x0022	B	0xc8	
CODEC_ADC_CFG1	0x0023	B	0xc0	
CODEC_PGA_CFG0	0x0024	B	0x30	
CODEC_PGA_CFG1	0x0025	B	0x30	
CODEC_PGA_CFG2	0x0026	B	0x00	
CODEC_PGA_GAIN1	0x0028	B	0x00	
CODEC_PGA_GAIN2	0x0029	B	0x00	
CODEC_DAC_CFG0	0x002a	B	0x00	
CODEC_DAC_CFG1	0x002b	B	0x0f	
CODEC_DDAC_POPD_DACST	0x002c	B	0x00	
CODEC_LO_CFG0	0x002f	B	0Xe6	
CODEC_LO_CFG1	0x0030	B	0x0f	
CODEC_CLASSD_CFG1	0x0031	B	0x61	
CODEC_CLASSD_CFG2	0x0032	B	0x44	
CODEC_RESEV_PIN_REG1	0x0050	B	0x00	
CODEC_RESEV_PIN_REG2	0x0051	B	0x00	
CODEC_RESEV_DATA_REG1	0x0052	B	0x00	
CODEC_RESEV_DATA_REG2	0x0053	B	0x00	
PMIC_POWER_EN0	0x00b1	B	0x01	
PMIC_POWER_EN1	0x00b2	B	0x0b	
PMIC_POWER_EN2	0x00b3	B	0x01	
PMIC_POWER_SLP_EN0	0x00b5	B	0x01	
PMIC_POWER_SLP_EN1	0x00b6	B	0x1b	
PMIC_POWER_DISCHRG_EN0	0x00b7	B	0x01	
PMIC_POWER_DISCHRG_EN1	0x00b8	B	0x1b	
PMIC_POWER_CONFIG	0x00b9	B	0x00	
PMIC_BUCK1_CONFIG	0x00ba	B	0x00	
PMIC_BUCK1_ON_VSEL	0x00bb	B	0x53	
PMIC_BUCK1_SLP_VSEL	0x00bc	B	0x53	
PMIC_BUCK_ZCD_REG1	0x00c7	B	0x07	
PMIC_BUCK_NCP_REG2	0x00c8	B	0x70	
PMIC_BUCK_GMC_REG	0x00ca	B	0x03	
PMIC_BUCK_RAMP_REG	0x00cb	B	0x03	
PMIC_LDO1_ON_VSEL	0x00cc	B	0x6c	
PMIC_LDO1_SLP_VSEL	0x00cd	B	0x6c	
PMIC_LDO2_ON_VSEL	0x00ce	B	0x28	
PMIC_LDO2_SLP_VSEL	0x00cf	B	0x28	
PMIC_LDO4_ON_VSEL	0x00d2	B	0x30	
PMIC_LDO4_SLP_VSEL	0x00d3	B	0x30	
PMIC_LDO5_ON_VSEL	0x00d4	B	0x30	
PMIC_LDO5_SLP_VSEL	0x00d5	B	0x30	
PMIC_CHRG_DEBUG_REG	0x00e2	B	0x00	
PMIC_CHRG_OUT	0x00e4	B	0xa0	

Name	Offset	Size	Reset Value	Description
PMIC_CHRG_TERM	0x00e6	B	0x00	
PMIC_CHRG_TO	0x00ea	B	0x22	
PMIC_CHRG_STS	0x00eb	B	0x40	
PMIC_CHIP_NAME	0x00ed	B	0x81	
PMIC_CHIP_VER	0x00ee	B	0x20	
PMIC_OTP_VER	0x00ef	B	0x00	
PMIC_SYS_STS	0x00f0	B	0x00	
PMIC_SYS_CFG0	0x00f1	B	0x8c	
PMIC_SYS_CFG1	0x00f2	B	0x00	
PMIC_SYS_CFG2	0x00f3	B	0x00	
PMIC_SYS_CFG3	0x00f4	B	0x20	
PMIC_ON_SOURCE	0x00f5	B	0x00	
PMIC_OFF_SOURCE	0x00f6	B	0x00	
PMIC_PWRON_KEY	0x00f7	B	0x02	
PMIC_INT_STS0	0x00f8	B	0x00	
PMIC_INT_MSK0	0x00f9	B	0x00	
PMIC_INT_STS1	0x00fa	B	0x00	
PMIC_INT_MSK1	0x00fb	B	0x00	
PMIC_GPIO_INT_CONFIG	0x00fe	B	0x02	
PMIC_PWRON_SW	0x00ff	B	0x00	

Notes:Size:B- Byte (8 bits) access, HW- Half WORD (16 bits) access, W-WORD (32 bits) access

5.2 Register Description

CODEC_DTOP1
Address: Operational Base + offset (0x001E)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved
5	RW	0x0	DAC_PATH_SEL dac_path_sel: select the signal of clock 0:select DAC pad clock 1: select ADC pad clock
4	RW	0x0	ADC_PATH_SEL adc_path_sel: select the signal of clock 0:select ADC pad clock 1: select DAC pad clock
3	RW	0x0	DIFF_SAMP_EN_DAC diff_samp_en_dac: When ADC/DAC works in the same time, if the sample rate of DAC is different from the one of ADC, this bit set 1; else set to 0.
2	RW	0x0	MOD_DAC_EN mod_dac_en: enable DAC digital circuit.
1	RW	0x0	DIFF_SAMP_EN_ADC diff_samp_en_adc: When ADC/DAC works in the same time, if the sample rate of ADC is different from the one of DAC, this bit set 1; else set to 0.
0	RW	0x0	MOD_ADC_EN mod_adc_en: enable ADC digital circuit.

CODEC_DTOP2
Address: Operational Base + offset (0x001F)

Bit	Attr	Reset Value	Description
7:4	RW	0x7	DIV_CON_DAC div_con_dac: DAC CLK divider, it should be set to 7 for 1/8 divider; or 11 for 1/12 divider.
3:0	RW	0x7	DIV_CON_ADC div_con_adc: ADC CLK divider, it should be set to 7 for 1/8 divider; or 11 for 1/12 divider.

CODEC_AREF_CFG1
Address: Operational Base + offset (0x0021)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved
5	RW	0x0	REF_ADC_SEL Select the ADC reference voltage 0: 1.2V 1: 1.4V
4:3	RW	0x0	VAG_SEL[1:0] Select the VAG voltage 00:0.9V 01:0.72V 10:1.08V 11:1.26V
2	RW	0x1	PWD_IBIAS Power down the ibias block in REF_TOP 0:IBIAS block power on 1:IBIAS block power down
1	RW	0x1	PWD_VAG_BUF Power down the Vag buffer in REF_TOP 0:Vag buffer block power on 1:Vag buffer block power down
0	RW	0x0	RESEV Reserved

CODEC_ADC_CFG0
Address: Operational Base + offset (0x0022)

Bit	Attr	Reset Value	Description
7	RW	0x1	ADC_1_PWD Power down ADC 1 channel 0: ADC left channel power on 1: ADC left channel power down
6	RW	0x1	ADC_2_PWD Power down ADC 2 channel 0: ADC right channel power on 1: ADC right channel power down
5	RW	0x0	ADC_CLK_EDGE_SEL Select the ADC output data and clock edge relationship 0: using the ADC falling edge to send the ADC data 1: using the ADC rising edge to send the ADC data
4	RW	0x0	Reserved
3	RW	0x1	ADC_DITH_OFF Disable the dither function of ADC 0: enable the ADC dither 1:disable the ADC dither

Bit	Attr	Reset Value	Description
2:0	RW	0x0	ADC_DITH_SEL[2:0] Select the dither frequency of ADC 000: 1/50 of ADC clock 001: 1/33 of ADC clock 010: 1/20 of ADC clock 011: 1/15 of ADC clock 100: 1/10 of ADC clock 101: 1/8 of ADC clock 110: 1/6 of ADC clock 111: 1/4 of ADC clock

CODEC_ADC_CFG1
Address: Operational Base + offset (0x0023)

Bit	Attr	Reset Value	Description
7	RW	0x1	ADC_3_PWD ADC_3_PWD: power down ADC 3 channel
6	RW	0x1	ADC_4_PWD ADC_4_PWD: power down ADC 4 channel only for RK802
5	RW	0x0	ADC_ATTN_ALLIBIAS ADC_ATTN_ALLIBIAS: decrease the total ADC ibias current
4	RW	0x0	ADC_ATTN_OPBIAS ADC_ATTN_OPBIAS: decrease the opamp bias current in ADC
3	RW	0x0	ADC_DLY_INC ADC_DLY_INC: increase the delay time of ADC clock signal
2	RW	0x0	ADC_OVERLAP_INC ADC_OVERLAP_INC: increase the non-overlap time of ADC clock signal
1	RW	0x0	ADC_BOOST_OPAMP ADC_BOOST_OPAMP: increase the opamp bias current in ADC
0	RW	0x0	ADC_BOOST_VAGOP ADC_BOOST_VAGOP: increase the vag buffer bias current in ADC

CODEC_PGA_CFG0
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESEV Reserved
5	RW	0x1	PWD_PGA_1 PWD_PGA_1:PGA1 Power Down
4	RW	0x1	PWD_PGA_2 PWD_PGA_2:PGA2 Power Down
3:2	RW	0x0	PGA1_IN_GAIN PGA1_IN_GAIN: PGA INPUT GAIN, 0~-9dB,Step=-3dB 00:0dB 01: -3dB 10:-6dB 11: -9dB
1:0	RW	0x0	PGA2_IN_GAIN<1:0> PGA2_IN_GAIN<1:0>: PGA INPUT GAIN, 0~-9dB,Step=-3dB 00:0dB 01: -3dB 10:-6dB 11: -9dB

CODEC_PGA_CFG1
Address: Operational Base + offset (0x0025)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved
5	RW	0x1	PWD_PGA_3 PWD_PGA_3:PGA3 Power Down
4	RW	0x1	PWD_PGA_4 PWD_PGA_4:PGA4 Power Down
3:2	RW	0x0	PGA3_IN_GAIN<1:0> PGA3_IN_GAIN<1:0>: PGA INPUT GAIN, 0~-9dB,Step=-3dB 00:0dB 01: -3dB 10:-6dB 11: -9dB
1:0	RW	0x0	PGA4_IN_GAIN<1:0> PGA4_IN_GAIN<1:0>:PGA INPUT GAIN, 0~-9dB,Step=-3dB 00:0dB 01: -3dB 10:-6dB 11: -9dB

CODEC_PGA_CFG2
Address: Operational Base + offset (0x0026)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV Reserved
4	RW	0x0	PGA_CHOP_EN Enable the chopping function of PGA 0:disable 1:enable
3:2	RW	0x0	RESV Reserved
1:0	RW	0x0	PGA_CHOP_SEL[1:0] 00:1.6M, 01:800K, 10:400k, 11:200K

CODEC_PGA_GAIN1
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	PGA_1_GAIN[3:0] Change the gain of PGA block, the value changed from 0dB to 30dB. 0000:0dB; 1111:30dB, 2dB/step
3:0	RW	0x0	PGA_2_GAIN[3:0] Change the gain of PGA block, the value changed from 0dB to 30dB. 0000:0dB; 1111:30dB, 2dB/step

CODEC_PGA_GAIN2
Address: Operational Base + offset (0x0029)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:4	RW	0x0	PGA_3_GAIN[3:0] Change the gain of PGA block, the value changed from 0dB to 30dB. 0000:0dB; 1111:30dB, 2dB/step
3:0	RW	0x0	PGA_4_GAIN[3:0] Change the gain of PGA block, the value changed from 0dB to 30dB. 0000:0dB; 1111:30dB, 2dB/step

CODEC_DAC_CFG0
Address: Operational Base + offset (0x002a)

Bit	Attr	Reset Value	Description
7	RW	0x0	DAC_AMP_INC2DB DAC_AMP_INC2DB:increase the DAC differential output about 2dB
6	RW	0x0	DAC_CLK_EDGE_SEL DAC_CLK_EDGE_SEL: select the DAC input DFF clock edge
5	RW	0x0	DAC_MAX_OUT DAC_MAX_OUT: make the DAC output to the max value
4	RW	0x0	INC_DAC_RSTB INC_DAC_RSTB: increase the DAC internal RSTB control time
3:2	RW	0x0	DAC_NBIAS_SEL[1:0] DAC_NBIAS_SEL[1:0]:select the DAC internal NMOS bias voltage 00-> 100%, 01-> 80% 10->120% 11-> 140%
1:0	RW	0x0	DAC_PBIAS_SEL[1:0] DAC_PBIAS_SEL[1:0]:select the DAC internal PMOS bias voltage

CODEC_DAC_CFG1
Address: Operational Base + offset (0x002b)

Bit	Attr	Reset Value	Description
7	RW	0x0	DOUBLE_DACIBIAS double DAC internal current resource
6	RW	0x0	INC_DAC_SWITCH increase the DAC internal switch signal control time
5	RW	0x0	STOP_DAC_RSTB stop the RSTB clock
4	RW	0x0	STOP_DAC_SWITCH stop the switch clock in DAC
3	RW	0x1	PWD_DACIBIAS power down the DAC internal current resource 0: DACIBIAS power up 1: DACIBIAS power down
2	RW	0x1	PWD_DACD Class D DAC power down 0: Class D DAC power up 1: Class D DAC power down

Bit	Attr	Reset Value	Description
1	RW	0x1	PWD_DACL L channel DAC power down 0: L channel DAC power up 1: L channel DAC power down
0	RW	0x1	PWD_DACR R channel DAC power down 0: R channel DAC power up 1: R channel DAC power down

CODEC_DDAC_POPD_DACST
Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	Reserved
0	R	0x0	LO_ANTIPOP_STS:

CODEC_LO_CFG0
Address: Operational Base + offset (0x002f)

Bit	Attr	Reset Value	Description
7	RW	0x1	PWD_LO_CHG
6	RW	0x1	PWD_LO_OSTAGE power down the Line-out OSTAGE 0:power up 1:power down
5	RW	0x1	PWD_LO_BUF power down the Line-out pre amp stage 0:power up 1:power down
4:3	RW	0x0	INC_LO_AMP[1:0] INC_LO_AMP: Increase the Line-out amplitude from 3dB to 9dB, 00-> 0dB 01-> 3dB 10-> 6dB 11-> 9dB
2	RW	0x1	PWD_LO_SW: 0:power up 1:power down
1	RW	0x1	PWD_LO_CMPMD: 0:power up 1:power down
0	RW	0x0	RESV Reserved

CODEC_LO_CFG1
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	LO_CHG_SEL<1:0>:
5	RW	0x0	LO_EN_VIN_VAG:
4	RW	0x0	LO_ANTIPOP_EN LO_ANTIPOP_EN: enable the Line-out antipop function
3:0	RW	0xf	LO_ANTIPOP_BIT[3:0] LO_ANTIPOP_BIT: control the Line-out antipop gain from -16dB to 0dB

CODEC_CLASSD_CFG1
Address: Operational Base + offset (0x0031)

Bit	Attr	Reset Value	Description
7	RW	0x0	CLASSD_EN CLASS D enable 0:disable 1:enable
6	RW	0x1	CLASSD_MUTE_EN CLASSD_MUTE_EN:CLASS D mute_ramp enable.
5	RW	0x1	CLASSD_SSC_EN CLASS D Spread-Spectrum enable 0:disable 1:enable
4	RW	0x0	CLASSD_SSC_SEL CLASS D Spread-Spectrum steps select 0: 8 steps 1:16 step
3:2	RW	0x2	Reserved
1:0	RW	0x1	CLASSD_SW_RATE 00:2.5ns;01:5ns;10:7.5ns;11:10ns

CODEC_CLASSD_CFG2
Address: Operational Base + offset (0x0032)

Bit	Attr	Reset Value	Description
7	RO	0x0	CLASSD_OCP_STS IF this bit is high, it need to restart CLASS D.
6:4	RW	0x4	CLASSD_OCPP CLASSD_OCPP：CLASS D PFET OCP Select：000: 1.0A; 001: 1.25A；010: 1.5A；011: 1.75A；100：2A（Default）;101: 2.25A；110: 2.5A；111: 2.75A
3	RO	0x0	Reserved
2:0	RW	0x4	CLASSD_OCPN CLASSD_OCPN：CLASS D NFET OCP Select：000: 1.0A; 001: 1.25A；010: 1.5A；011: 1.75A；100：2A（Default）;101: 2.25A；110: 2.5A；111: 2.75A

RESEV_PIN_REG1
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	RESEV_PIN1 RESEV
3	RW	0x0	LO_EN_DISCHRG: Line out discharge enable. RESEV
2:1	RW	0x0	RESEV
0	RW	0x0	RESETB_EN: RESEV

RESEV_PIN_REG2
Address: Operational Base + offset (0x0051)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	RESEV_PIN2 RESEV

RESEV_DATA_REG1
Address: Operational Base + offset (0x0052)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA1 DATA1: System data.

RESEV_DATA_REG2
Address: Operational Base + offset (0x0053)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA2 DATA2: System data.

PMIC_POWER_EN0
Address: Operational Base + offset (0x00b1)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4	RW	0x0	BUCK_EN_MASK BUCK_EN_MASK: MUST write them to "1" if want to change corresponding BUCK1_EN bit，The BUCK_EN_MASK bits should be clear when BUCK1_EN bits have been written.
3:1	RW	0x0	Reserved
0	RW	OTP	BUCK_EN BUCK_EN: BUCK enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_EN1
Address: Operational Base + offset (0x00b2)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO4_EN_MASK LDO4_EN_MASK: MUST write them to "1" if want to change corresponding LDO4_EN bit，The LDO4_EN_MASK bits should be clear when LDO4_EN bits have been written.
6	RW	0x0	Reserved
5	RW	0x0	LDO2_EN_MASK LDO2_EN_MASK: MUST write them to "1" if want to change corresponding LDO2_EN bit，The LDO2_EN_MASK bits should be clear when LDO2_EN bits have been written.
4	RW	0x0	LDO1_EN_MASK LDO1_EN_MASK: MUST write them to "1" if want to change corresponding LDO1_EN bit，The LDO1_EN_MASK bits should be clear when LDO1_EN bits have been written.

Bit	Attr	Reset Value	Description
3	RW	OTP	LDO4_EN LDO4_EN: LDO4 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
2	RW	0x0	Reserved
1	RW	OTP	LDO2_EN LDO2_EN: LDO2 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
0	RW	OTP	LDO1_EN LDO1_EN: LDO1 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_EN2
Address: Operational Base + offset (0x00b3)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4	RW	0x0	LDO5_EN_MASK LDO5_EN_MASK: MUST write them to "1" if want to change corresponding LDO5_EN bit，The LDO5_EN_MASK bits should be clear when LDO5_EN bits have been written.
3:1	RW	0x0	Reserved
0	RW	OTP	LDO5_EN LDO5_EN: LDO5 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_SLP_EN0
Address: Operational Base + offset (0x00b5)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	Reserved
0	RW	OTP	BUCK_SLP_EN BUCK_SLP_EN: BUCK1 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_SLP_EN1
Address: Operational Base + offset (0x00b6)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4	RW	OTP	LDO5_SLP_EN LDO5_SLP_EN: LDO5 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
3	RW	OTP	LDO4_SLP_EN LDO4_SLP_EN: LDO4 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
2	RW	0x0	Reserved
1	RW	OTP	LDO2_SLP_EN LDO2_SLP_EN: LDO2 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
0	RW	OTP	LDO1_SLP_EN LDO1_SLP_EN: LDO1 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_DISCHRG_EN0
Address: Operational Base + offset (0x00b7)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	
0	RW	0x1	BUCK_DISCHG_EN BUCK_DISCHG_EN: BUCK discharge enable when the channel is off 0: Disable 1:enable

PMIC_POWER_DISCHRG_EN1
Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4	RW	0x1	LDO5_DISCHG_EN LDO5_DISCHG_EN: LDO5 discharge enable when the channel is off 0: Disable 1:enable:
3	RW	0x1	LDO4_DISCHG_EN LDO4_DISCHG_EN: LDO4 discharge enable when the channel is off 0: Disable 1:enable:
2	RW	0x0	Reserved

Bit	Attr	Reset Value	Description
1	RW	0x1	LDO2_DISCHG_EN LDO2_DISCHG_EN: LDO2 discharge enable when the channel is off 0: Disable 1:enable:
0	RW	0x1	LDO1_DISCHG_EN LDO1_DISCHG_EN: LDO1 discharge enable when the channel is off 0: Disable 1:enable

PMIC_POWER_CONFIG
Address: Operational Base + offset (0x00b9)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO_SLP_LP_EN LDO_SLP_LP_EN: Low power function enable bit of LDO 0: disable 1:enable
6	RW	0x0	BUCK_LDO_50U_EN BUCK_LDO_50U_EN: 50uA loading 0: disable 1:enable
5	RW	0x0	Reserved
4	RW	0x0	Reserved
3:1	RW	0x0	Reserved
0	RW	0x0	BUCK_LP_EN BUCK_LP_EN: Low power function enable bit of BUCK1 0: disable 1:enable

PMIC_BUCK_CONFIG
Address: Operational Base + offset (0x00ba)

Bit	Attr	Reset Value	Description
7	RW	0x0	Reserved
6:4	RW	OTP	BUCK_ILPK BUCK_ILPK: BUCK peak current limit select, MUST linkage adjustment with the BUCK_ILVL<2:0>(write the same code) 000:1A 001:1.25A 010:1.5A 011:1.75A 100:2A 101:2.25A 110:2.5A 111:2.75A Reset by power down or RST.
3	RW	0x0	Reserved
2:0	RW	OTP	BUCK_ILVL BUCK_ILVL: BUCK valley current limit select, linkage adjustment with the BUCK_ILVL<2:0>(write the same code) 000:1A 001:1.25A 010:1.5A 011:1.75A 100:2A 101:2.25A 110:2.5A 111:2.75A Reset by power down or RST.

PMIC_BUCK_ON_VSEL
Address: Operational Base + offset (0x00bb)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK_ON_FPWM BUCK_ON_FPWM: BUCK Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode Reset by power down or RST.
6:0	RW	OTP	BUCK_ON_VSEL BUCK_ON_VSEL<6:0>: BUCK active mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1011000:2.3V 1011001~1111111:2.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK_SLP_VSEL
Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK_SLP_FPWM BUCK_SLP_FPWM: 1, Forced PWM mode in sleep mode. 0, PWM/PFM auto change mode. reset by power down or RST.
6:0	RW	OTP	BUCK_SLP_VSEL BUCK_SLP_VSEL<6:0>: BUCK SLEEP mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1011000:2.3V 1011001~1111111:2.4V the default value is set by otp reset by power down or RST.

PMIC_LDO1_ON_VSEL
Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO1_IMAX LDO1_IMAX:LDO1 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.

Bit	Attr	Reset Value	Description
6:0	RW	OTP	LDO1_ON_VSEL LDO1_ON_VSEL: LDO1 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO1_SLP_VSEL
Address: Operational Base + offset (0x00cd)

Bit	Attr	Reset Value	Description
7	RW	0x0	Reserved
6:0	RW	OTP	LDO1_SLP_VSEL LDO1_SLP_VSEL:LDO1 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO2_ON_VSEL
Address: Operational Base + offset (0x00ce)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO2_IMAX LDO2_IMAX:LDO2 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO2_ON_VSEL LDO2_ON_VSEL: LDO2 active mode voltage select, 0.6V~2V(step=12.5mV) 0000000:0.6V 0000001:0.6125V 0000010:0.625V ... 1101111~1111111:2V the default value is set by otp reset by power down or RST.

PMIC_LDO2_SLP_VSEL
Address: Operational Base + offset (0x00cf)

Bit	Attr	Reset Value	Description
7	RW	0x0	Reserved

Bit	Attr	Reset Value	Description
6:0	RW	OTP	LDO2_SLP_VSEL LDO2_SLP_VSEL:LDO2 SLEEP mode voltage select, 0.6V~2V(step=12.5mV) 0000000:0.6V 0000001:0.6125V 0000010:0.625V ... 1101111~1111111:2V the default value is set by otp reset by power down or RST.

PMIC_LDO4_ON_VSEL
Address: Operational Base + offset (0x00d2)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO4_IMAX LDO4_IMAX:LDO4 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO4_ON_VSEL LDO4_ON_VSEL: LDO4 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO4_SLP_VSEL
Address: Operational Base + offset (0x00d3)

Bit	Attr	Reset Value	Description
7	RW	0x0	
6:0	RW	OTP	LDO4_SLP_VSEL LDO4_SLP_VSEL:LDO4 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO5_ON_VSEL
Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO5_IMAX LDO5_IMAX:LDO5current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO5_ON_VSEL LDO5_ON_VSEL: LDO5 active mode voltage select, 0.6V~3.4V(step=25mV) 0110000:1.8V 0110001:1.825V 0110010:1.85V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO5_SLP_VSEL
Address: Operational Base + offset (0x00d5)

Bit	Attr	Reset Value	Description
7	RW	0x0	
6:0	RW	OTP	LDO5_SLP_VSEL LDO5_SLP_VSEL:LDO5 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0110000:1.8V 0110001:1.825V 0110010:1.85V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_CHRG_OUT
Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
7	RW	0x1	CHRG_EN: charger enable. 0: charger disable 1: if I_PLUGIN=1, charger enable
6:4	RW	0x2	CHRG_VOL_SEL: charger voltage selection 000:4.1V 001:4.15V 010:4.2V 011:4.25V 100:4.3V 101:4.35; 110:4.4V; 111:4.45V
3:0	RW	OTP	CHRG_CUR_SEL: charger current selection 0000:450mA; 0001:150mA; 0010:200mA；0011:250mA； 0100:300mA； 0101:350mA； 0110:400mA； 0111:100mA；1000:500mA; 1001:550mA；1010:600mA； 1011:650mA； 1100:700mA； 1101:800mA； 1110:900mA； 1111:1000mA

PMIC_CHRG_TERM
Address: Operational Base + offset (0x00e6)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
7:1	RW	0x0	Reserved
0	RW	0x1	CHRG_TERM_ANA_SEL: analog charging termination selection 0:10% ICC; 1:20% ICC

PMIC_CHRG_TO
Address: Operational Base + offset (0x00ea)

Bit	Attr	Reset Value	Description
7	RW	0x0	CHRG_CT_EN CHRG_CT_EN: Charger Thermal foldback enable 0:disable 1:enable
6	RW	0x0	CHRG_TIMER_TRIKL_EN CHRG_TIMER_TRIKL_EN: trickle charging timer enable, 0:disable 1:enable
5:4	RW	0x2	CHRG_TIMER_TRIKL CHRG_TIMER_TRIKL: trickle charge timer selection 00:30min 01:45min 10:60min 11:90min
3	RW	0x0	BAT_OVP_EN BAT_OVP_EN: VB_OV ENABLE 0:disable 1:enable
2	RW	0x0	CHRG_TIMER_CCCV_EN CHRG_TIMER_CCCV_EN: Constant current and Constant voltage charging timer enable, 0:disable 1:enable
1:0	RW	0x2	CHRG_TIMER_CCCV CHRG_TIMER_CCCV:CC CV charge timer selection 00:4h 01:5h 10:6h 11:8h

PMIC_CHRG_STS
Address: Operational Base + offset (0x00eb)

Bit	Attr	Reset Value	Description
7	RO	0x0	CHRG_BAT_OV_STS CHRG_BAT_OV_STS: 0:higher than CHRG_CV*104% set to high 1: higher than 6V set to high
6	RO	0x0	Reserved
5	RO	0x0	CCCV_CHRG_STS CCCV_CHRG_STS: constant current and constant voltage charging state
4	RO	0x0	TIME_OUT_CHRG_STS TIME_OUT_CHRG_STS: charge over time protection state
3	RO	0x0	Reserved
2	RO	0x0	TERM_CHRG_STS TERM_CHRG_STS: terminal charging state
1	RO	0x0	CHRG_CT_STS CHRG_CT_STS: constant temperature charging state
0	RO	0x0	USB_OV_STS USB_OV_STS:USB voltage higher than 6V

PMIC_CHIP_NAME
Address: Operational Base + offset (0x00ed)

Bit	Attr	Reset Value	Description
7:0	RO	0x81	CHIP_NAME<11:4>: RK812 or RK802 0:RK812 1:RK802

PMIC_CHIP_VER
Address: Operational Base + offset (0x00ee)

Bit	Attr	Reset Value	Description
7:4	RO	0x2	CHIP_NAME
3:0	RO	I_CHIP_VER	RESV RESV: Reserve

PMIC_OTP_VER
Address: Operational Base + offset (0x00ef)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	
3:0	RO	OTP	OTP_VER OTP_VER: OTP revize version. default OTP.

PMIC_SYS_STS
Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
7	RO	0x0	PKEY_STS PKEY_STS: PWRON key status
6	RO	0x0	PLUG_IN_STS PLUG_IN_STS: USB plug-in event occurs(USB voltage >3.8V after pull down 20mA current) 0: no USB plug in 1: USB plugged in
5	RO	0x0	VB_UV_STS VB_UV_STS: Battery under voltage lockout status(shut down system if the bit=1)
4	RO	0x0	VB_LO_STS VB_LO_STS: Battery low voltage status 0: VBAT>VB_LO_SEL 1: VBAT<VB_LO_SEL
3	RO	0x0	HOTDIE_STS HOTDIE_STS: Hot-die warning
2	RO	0x0	TSD_STS TSD_STS: Thermal shut down
1	RO	0x0	BAT_HI_STS BAT_HI_STS:battery higher than USB status bit
0	RO	0x0	PSW_STS PSW_STS:PWRON SW status

PMIC_SYS_CFG0
Address: Operational Base + offset (0x00f1)

Bit	Attr	Reset Value	Description
7	RW	0x1	Reserved
6:4	RW	0x0	VB_UV_SEL VB_UV_SEL:SYS shut down voltage select, 2.7V~3.4V, step=100mV 000:2.7V; 001:2.8V; 010:2.9V; 011:3.0V 100:3.1V; 101:3.2V; 110:3.3V; 111:3.4V reset by power down or RST
3	RW	0x1	VB_LO_ACT VB_LO_ACT: VBAT low action 0: shut down system 1: insert interrupt reset by power down or RST
2:0	RW	0x4	VB_LO_SEL VB_LO_SEL: Battery low voltage threshold threshold,2.8V~3.5V, step=100mV 000:2.8V; 001:2.9V; 010:3.0V; 011:3.1V 100:3.2V; 101:3.3V; 110:3.4V; 111:3.5V reset by power down or RST

PMIC_SYS_CFG1
Address: Operational Base + offset (0x00f2)

Bit	Attr	Reset Value	Description
7	RW	0x0	USB_OV_SEL USB_OV_SEL: USB over voltage threshold. 0:5.8V, 1:6V
6	RW	0x0	TSD_TEMP TSD_TEMP: Thermal shutdown temperature threshold 0: 140℃; 1: 160℃ reset by power down or RST
5:4	RW	0x0	HOTDIE_TEMP HOTDIE_TEMP: Hot-die temperature threshold 00:85℃ 01:95℃ 10:105℃ 11:115℃ reset by power down or RST
3	RW	0x0	VB_OV_SD_ENB VB_OV_SD_ENB: Shut down the PMIC if the VB OV happens 0:Enable 1:Disable
2	RW	0x0	Reserved
1	RW	0x0	USB_OV_SD_ENB USB_OV_SD_ENB: Shut down the charger if the USB OV happens 0:Enable 1:Disable
0	RW	0x0	Reserved

PMIC_SYS_CFG3
Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RST_FUN RST_FUN: 00：Restart PMU；01: Reset PMIC register.

Bit	Attr	Reset Value	Description
5	RW	0x0	SLP_POL SLP_POL: SLEEP pin polarity。 0: active low 1:active high
4:3	RW	0x0	SLP_FUN SLP_FUN: SLEEP PIN function selection: 00: not effect; 01: sleep function; 10:shutdown function; 11:restart pmu function.
2	RW	0x0	DEV_RST DEV_RST: reset PMU (according RST_FUN)
1	RW	0x0	DEV_SLP DEV_SLP: Write 1 start a ACTIVE to SLEEP state transition state (if DEV_OFF = 0 and DEV_RST = 0). Write '0' will start a SLEEP to ACTIVE device state transition (wake-up event) (if DEV_OFF = 0 and DEV_RST = 0). This bit is cleared in OFF state. reset by power down or RST
0	RW	0x0	DEV_OFF DEV_OFF: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event). This bit is cleared in OFF state. reset by power down or RST

PMIC_ON_SOURCE
Address: Operational Base + offset (0x00f5)

Bit	Attr	Reset Value	Description
7	RO	0x0	ON_PKEY ON_PKEY:PRESS PKEY to turn on PMU after reset.
6:5	RO	0x0	Reserved
4	RO	0x0	Reserved
3	RO	0x0	ON_PLUG_IN ON_PLUG_IN:USB PLUG IN to turn on PMU reset by power down or RST
2	RO	0x0	RESTART_RESETB RESTART_RESETB:PULL LOW the resetb PIN to restart the PMU reset by power down or RST
1	RO	0x0	RESTART_DEV_RST RESTART_DEV_RST: DEV_RST=1 to restart the PMU reset by power down or RST
0	RO	0x0	ON_PSW_RISE ON_PSW_RISE: PSW rising edge to turn on PMU

PMIC_OFF_SOURCE
Address: Operational Base + offset (0x00f6)

Bit	Attr	Reset Value	Description
7	RO	0x0	Reserved
6	RO	0x0	OFF_PSW_FALL OFF_PSW_FALL: PSW falling edge to turn off PMU reset by power down or RST, and load this bit after reset.

Bit	Attr	Reset Value	Description
5	RO	0x0	OFF_TSD OFF_TSD:TSD to turn off PMU reset by power down or RST, and load this bit after reset.
4	RO	0x0	OFF_VB_UV OFF_VB_UV:SYS UV to turn off PMU reset by power down or RST, and load this bit after reset.
3	RO	0x0	OFF_DEV_OFF OFF_DEV_OFF:I2C write DEV_OFF to turn off PMU reset by power down or RST, and load this bit after reset.
2	RO	0x0	OFF_PKEY_LP OFF_PKEY_LP:long press PKEY to turn off PMU reset by power down or RST, and load this bit after reset.
1	RO	0x0	Reserved
0	RO	0x0	OFF_VB_LO OFF_VB_LO:SYSTEM Low (if Reg21<4>vb_lo_act=0)to turn off PMU reset by power down or RST, and load this bit after reset.

PMIC_PWRON_KEY
Address: Operational Base + offset (0x00f7)

Bit	Attr	Reset Value	Description
7	RW	OTP	PKEY_ON_TIME PKEY_ON_TIME:0：20mS; 1:500mS default OTP.
6:4	RW	0x0	PKEY_LP_OFF_TIME PKEY_LP_OFF_TIME:PKEY long press act mode and time select 000: 8S; 001: 0.5S;010: 1S; 011:4S; 100:0.1S;101:16S;11x:don’t shut down
3:2	RW	0x0	PKEY_LP_INT_TIME PKEY_LP_INT_TIME:PKEY long press interrupt time selection: 00: 0.5S 01:1S 10:1.5S 11:2S
1:0	RW	0x2	PKEY_INT_TIME PKEY_INT_TIME:PKEY interrupt debounce time selection: 00: 200uS 01:10mS 10:20mS 11:40mS

PMIC_INT_STS0
Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
7	RW	0x0	VB_LO_INT VB_LO_INT: Battery under voltage alarm event interrupt status. 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.
6	RW	0x0	CLASSD_OCP_INT 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.

Bit	Attr	Reset Value	Description
5	RW	0x0	PSW_FALL_INT 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.
4	RW	0x0	HOTDIE_INT HOTDIE_INT: Hot die event interrupt status. 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.
3	RW	0x0	PKEY_LP_INT PKEY_LP_INT: PKEY PIN long press event interrupt status. 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.
2	RW	0x0	PKEY_INT PKEY_INT: PKEY event interrupt status. 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.
1	RW	0x0	PKEY_RISE_INT PKEY_RISE_INT: PKEY rising event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.
0	RW	0x0	PKEY_FALL_INT PKEY_FALL_INT: PKEY falling event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.

PMIC_INT_MSK0
Address: Operational Base + offset (0x00f9)

Bit	Attr	Reset Value	Description
7	RW	0x0	VB_LO_IM VB_LO_IM: Battery under voltage alarm event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.
6	RW	0x0	CLASSD_OCP_INT_IM 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.
5	RW	0x0	PSW_FALL_IM 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.
4	RW	0x0	HOTDIE_IM HOTDIE_IM: Hot die event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.

Bit	Attr	Reset Value	Description
3	RW	0x0	PKEY_LP_IM PKEY_LP_IM: PKEY PIN long press event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.
2	RW	0x0	PKEY_IM PKEY_IM: PKEY event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.
1	RW	0x0	PKEY_RISE_INT_IM PKEY_RISE_INT_IM: PKEY rising event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.
0	RW	0x0	PKEY_FALL_INT_IM PKEY_FALL_INT_IM: PKEY falling event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.

PMIC_INT_STS1
Address: Operational Base + offset (0x00fa)

Bit	Attr	Reset Value	Description
7	RW	0x0	CHRG_BAT_HI_INT 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.
6	RW	0x0	VB_OV_INT 1, Interrupt asserted, write "1" to clear 0, No interrupt
5	RW	0x0	USB_OV_INT USB_OV_INT:USB over voltage event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt
4	RW	0x0	CHRG_CT_INT 1, Interrupt asserted, write "1" to clear 0, No interrupt
3	RW	0x0	CHRG_TIME_INT CHRG_TIME_INT: Charger time error event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt
2	RW	0x0	CHRG_TERM_INT CHRG_TERM__INT: Charger finished event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt
1	RW	0x0	PLUG_OUT_INT PLUG_OUT_INT: USB plug out event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.

Bit	Attr	Reset Value	Description
0	RW	0x0	PLUG_IN_INT PLUG_IN_INT: USB plug in event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt reset by power down or RST.

PMIC_INT_MSK1
Address: Operational Base + offset (0x00fb)

Bit	Attr	Reset Value	Description
7	RW	0x0	CHRG_BAT_HI_INT_IM BAT_DIS_ILIM_INT_IM: Battery discharge current over the setting value event interrupt mask. reset by power down or RST.
6	RW	0x0	VB_OV_INT_IM 1, Mask specified interrupt 0, Do not mask specified interrupt
5	RW	0x0	USB_OV_INT _IM:USB over voltage event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt
4	RW	0x0	CHRG_CT_INT_IM 1, Mask specified interrupt 0, Do not mask specified interrupt
3	RW	0x0	CHRG_TIME_INT_IM CHRG_TIME_INT_IM: Charger time error event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt
2	RW	0x0	CHRG_TERM_INT_IM CHRG_TERM_INT_IM: Charger finished event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt
1	RW	0x0	PLUG_OUT_INT_IM PLUG_OUT_INT_IM: USB plug out event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.
0	RW	0x0	PLUG_IN_INT_IM PLUG_IN_INT_IM: USB plug in event interrupt mask 1, Mask specified interrupt 0, Do not mask specified interrupt reset by power down or RST.

PMIC_GPIO_INT_CONFIG
Address: Operational Base + offset (0x00fe)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	Reserved

Bit	Attr	Reset Value	Description
1	RW	0x1	INT_POL INT_POL: INT pin polarity 0: active low 1: active high reset by power down or RST.
0	RW	0x0	Reserved

PMIC_PWRON_SW
Address: Operational Base + offset (0x00ff)

Bit	Attr	Reset Value	Description
7	RW	0x0	Reserved
6:4	RW	0X0	PSW_FALL_OFF_TIME PSW_FALL_OFF_TIME:PSW OFF act mode and time select 000: 0.5S; 001: 0.1S;010: 1S; 011:4S; 100:8S;101:16S;11x:don't shut down
3:2	RW	0x0	PSW_FALL_INT_TIME PSW_FALL_INT_TIME:PSW falling edge interrupt time selection: 00: 0.5S 01:10mS 10:1.5S 11:2S
1:0	RW	OTP	PSW_RISE_ON_TIME PSW_RISE_ON_TIME:00：1mS; 01:20mS；10:60ms；11：100uS

Chapter 6 Thermal Management

6.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK812 has to be below 125ºC.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

6.2 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1 Thermal Resistance Characteristics

PACKAGE (QFN4X4-36)	**POWER(W)**	$\boldsymbol{\theta_{JA}}(℃/\boldsymbol{W})$	$\boldsymbol{\theta_{JB}}(℃/\boldsymbol{W})$	$\boldsymbol{\theta_{JC}}(℃/\boldsymbol{W})$
RK812	TBD	39.7	TBD	51.2

Note: The testing PCB is based on 4 layers, 114mm x 76 mm, 1.6mm thickness, Ambient temperature is 85°C.

