RK2818
Technical Reference Manual
Brief

Revision 1.0
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Chapter 1 Introduction

1.1 Overview

RK2818 is a highly-integrated, high-performance, low-power digital multimedia processor which is based on Dual Core (DSP+CPU) architecture with hardware accelerator. It is designed for high-end multimedia product applications such as MID, AP, GPS and Mobile TV etc.

RK2818 can support decode for various types of video standards such as H.264 /RMVB/MPEG-4/AVS/VC1/MPEG-2 by software and dedicated coprocessors, and encode for some video standards by software. Specially, highest performace for video decode will reach fluent replay for video with H.264 @ 1280x720 formats. RK2818 also provides strong graphics/image ability with embedded GPU. By providing a complete set of peripheral interface, RK2818 can support very flexible applications, including SDRAM/ Mobile SDRAM/DDRII/Mobile DDR, Nor Flash, Nand Flash, LCDC, Sensor, USB OTG 2.0/USB Host 1.0, SD/MMC/SDIO, Wi-Fi, High-speed ADC, I2C, I2S, UART, SPI, PWM etc.

1.2 Features

- **System Operation**
  - Dual Core Architecture (ARM9 + DSP) , including hardware accelerator
  - Support system boot sequentially from ARM to DSP
  - Support address remap function
  - For two cores, all modules have unified address space
  - Selectable JTAG debug method
    - ARM9 debug only (default)
    - DSP debug only
    - ARM9+DSP dual core debug
  - Selectable CPU booting method
    - Boot from NOR Flash
    - Boot from Nand Flash
    - Boot from SPI nor flash
    - Boot from UART device
    - Boot from Host interface

- **Memory Organization**
  - Internal memory space for ARM processor
    - Internal 16KB SRAM for ARM9 ICache
    - Internal 16KB SRAM for ARM9 DCache
    - Internal 8KB SRAM for ARM9 ITCM
    - Internal 16KB SRAM for ARM9 DTCM
  - Internal memory space for DSP processor
    - Internal 96KB SRAM for DSP Instruction L1 Memory (Also config as 32KB Memory+32KB ICache by software, another 32KB is switched by software)
    - Internal 64KB SRAM for DSP Data L1 Memory
    - Internal 48KB SRAM for DSP Instruction L2 Memory
    - Internal 32KB SRAM for DSP Data L2 Memory
  - Embedded 8KB ROM for CPU Boot
  - Embedded 4KB SRAM for communication between two cores
  - Embedded 48KB SRAM for share among CPU,DSP and LCDC rotator

- **Processors**
  - ARM926EJC
    - RISC architecture with 32bit ARM and 16bit Thumb instruction sets
    - Include efficient execution of Java byte codes

- Built-in MMU to provide flexible memory management needed by many mainstream OS
- Harvard cached architecture , separate ICache and DCache
- Separate instruction and data TCM interfaces
- Separate instruction and data AHB bus interface
- Support ARM debug architecture

- DSP
  - Based on VLIW instructions with SIMD concepts , reach high level of parallelism and high code density
  - Support 16bits and 32bits variable instruction sets
  - Based on a load/store architecture, have two load-store units
  - Support Nine-stage pipeline
  - Built-in two 16x16bit MAC units

- **Communication between two cores**
  - Support share memory and interactive interrupt method to complete communication
  - Processor Interface Unit (PIU)
    - Built-in three Command/reply protocols registers and three Semaphore registers to accessed by two cores
    - Support three semaphore-related interrupts and one command-reply-related interrupt between two cores

- **Clock & Power Management**
  - Three on-chip PLLs for ARM9 subsystem, DSP subsystem and Other logic
  - Support different DSP Core and internal AHB Bus clock ratio : 1:1, 1:2, 1:3, 1:4, up to 1:16 mode
  - Support different DSP internal AHB Bus and internal APB Bus clock ratio : 1:1 , 1:2 , 1:3 , 1:4 , up to 1:16 mode
  - Support different ARM9 core and AHB Bus clock ratio : 1:1 , 1:2 , 1:3 and 1:4 mode
  - Support different ARM AHB Bus and ARM APB Bus clock ratio : 1:1 , 1:2 and 1:4 mode
  - Max frequency of every key clock domain
    - 560MHz Max frequency for DSP Core
    - 600MHz Max frequency for ARM Core
  - 6 types of work modes by clock gating to save power :
    - Normal mode : Normal operating mode
    - Slow mode : Low frequency clock (24MHz) without PLL
    - Deep Slow mode : More Low frequency clock (32.768KHz) without PLL
    - Idle mode : The clock for only CPU is stopped, Wake up by any interrupts to CPU from idle mode
    - Sleep mode : The clock for only DSP is stopped, Wake up from sleep mode by some interrupts to DSP or register set from CPU
    - Stop mode : All clocks will be stopped , and SDRAM into Self-refresh, all PLLs into power-down mode, Wake up from stop mode by external pin or RTC Alarm interrupt
  - Support power supply shut down for 4 domain separately

- **Video hardware accellerator**
  - Deblocking
    - Support RMVB and H.264 video format
    - Support embedded DMA function with on-the-fly mode
  - CABAC
    - Support H.264 video format

- Support embedded DMA function
- Tightly coprocessor in dsp system

- **Graphics hardware accellerator (GPU)**
  - 3D feature
    - Four times and 16 times Full Scene Anti-Aliasing (FSAA).
    - Lines, squares, triangles and points.
    - Flat and Gouraud shading.
    - Perspective correct texturing.
    - Point sampling, bilinear, and trilinear filtering.
    - Programmable mipmap level-of-detail biasing.
    - Multitexturing, with three textures.
    - Dot3 bump mapping.
    - Alpha blending.
    - Stencil buffering.
    - Point sprites.
    - 4-bit per texel texture compression, Ericsson Texture Compression (ETC)
  - 2D features
    - Lines, squares, triangles and points
    - ROP3/4
    - Arbitrary rotation and scaling
    - Alpha blending
    - Multitexture BitBLT

- **External Memory Interface**
  - Support SDRAM/Mobile SDRAM/DDRII/Mobile DDR separately
  - Support special SDRAM controller for high-performance video data transfer
  - Support Nor Flash/Nand Flash/SD/MMC/SDIO interface, Nor Flash interface is only available when use SDRAM or Mobile SDRAM
  - Static/SDRAM Memory controller
    - Dynamic memory interface support , including SDR-SDRAM and Mobile SDRAM
    - Asynchronous static memory device support including SRAM, ROM and Nor Flash with or without asynchronous page mode
    - Support 2 chip selects for (Mobile) SDRAM and 2 chip selects for static memory
    - Support 16bits or 32bits width data bus (Mobile) SDRAM and 8/16 bits data bus static memory, it is programmable.
    - Support industrial standard (Mobile) SDRAM with a maximum of 256MB of address space per chip select
    - 4Mbytes access space per static memory support
    - Support (Mobile) SDRAM and Static Memory power-down mode
    - Support (Mobile) SDRAM self-refresh mode
    - Programmable arbitration priority for 6 slave data ports
  - DDRII/Mobile DDR Memory controller
    - Programmable select for DDRII or Mobile DDR function
    - Fully pipelined command, read and write data interface
    - Advanced bank look-ahead features for high memory throughput
    - Support one slave port for register set and 6 slave ports for data access
    - Separate asynchronous FIFOs for every slave ports to support different frequency between AHB bus and DDR controller, and improve utility for

bandwidth
- Support 32bit/16bit data width
- Support 2 chip selects , with a maximum of 256MB of address space per chip select
- DDRII data rate is 533M x 32bits , Mobile DDR data rate is 400M x 32bits

- Customized SDRAM controller for video
  - Support 32bit SDRAM data width
  - Special mechanism to improve little-block data transfer efficiency for video, especially when use together with MCDMA
  - Support one slave for register set and six data slave ports
- Nand Flash controller
  - Standard AMBA2.0 Slave interface
  - Support 8 chip selects for nand flash
  - Only support 8bit data width
  - Flexible CPU interface support
  - Embedded 2x1KB size buffer for DMA mode to improve performace
  - 512B, 2KB, 4KB page size support
  - Support hardware 24bit ECC
  - Support LBA nand
  - Support FF code auto correct process
- SD/MMC controller
  - Two Embedded SD/MMC Controllers, one is 4bit data bus , another is 8bit data bus
  - Compliant with SD Memory/SDIO with 1bit and 4bit data bus
  - Compliant with MMC V3.3 and V4.0 with 1/4/8bit data bus
  - Support combined single 32x32bits FIFO for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock
  - Variable SD/MMC card clock rate 0 – 52 MHz which depends on AHB clock frequency
  - Controllable SD/MMC card clock to save power consumption
  - Support card detection and initialization , and write protection
  - Support transfer block size of 1 to 65365Bytes
  - DMA based or Interrupt based operation

- **VIDEO/Image interface**
  - Sensor controller
    - Embedded DMA function
    - Support 24MHz 、48MHz、27MHz clock input
    - Support CCIR656 PAL/NTSC input
    - Support YUYV and UYVY format input
    - Support YUV 4:2:2 and YUV 4:2:0 format output
    - Programmable Hsync and Vsync porality
    - Support 10bit or 12bit raw data input
    - Support sensor bypass to LCDC interface
    - Support 8 MegaPixels
  - LCD controller
    - Embedded DMA function
    - Programmable transfer mode to meet different bus bandwidth and transfer efficiency.
    - Support two window with scale function
    - YUV422/YUV420/RGB565/RGB888 input format are supported in window0
    - RGB565/RGB888 input format and 4 areas are supported in window1
    - Support virtual display
    - Built-in scaler engine from 1/8 to 8
    - Support 16 level alpha blending and transparent operation.
    - Support Blank/Black Function

- Support LCD Pannel resolution up to 1280x720
- Compatible with MCU pannel
- Compatible with 8/16/18/24bits RGB Delta/no-Delta Pannel
- Compatible with 8/16/18/24bits RGB Series/Parallel Output
- Support Interlace and Progressive Output
- Support hardware cursor
- Support rotation display
- Support video dither operation
- Support Interlace to progressive change for MPEG-2
- Support LCDC interface bypass from Host interface or VIP interface

- **DMA Controller**
  - Three DMA Controllers in chip
  - DW_DMA Controller integrated inside ARM9 subsystem
    - Six DMA Channels support to use by audio , sd/mmc and system data transfer
    - 8 hardware request handshaking support
    - Support hardware and software trigger DMA transfer mode
    - Build-in 6 data FIFO: 64B/32B/16B/32B/16B/16B
    - Channel 0 & 1 support Scatter/Gather transfer
    - Channel 0 & 1 support LLP transfer
    - Two masters for on-the-fly support
    - The master interface only support defined length INCR transfer
  - 3D-DMA Controller(XDMA) integrated inside DSP subsystem
    - This DMA focus on data transfer for video process and mobile TV application
    - 16 configurable DMA channels , 4 channels support 3-dimensional data transfer
    - 8/16/32/64bit data transfer support and configurable burst length (INCR/INCR4/INCR8)
    - Programmable source and destination addresses with a post-modification option
    - Configurable external channel triggering (edge or level)
    - Support chaining-channels ,linked list-transfer and auto-channel initialization operating mode
    - Pause and resume operations supported to save power
    - Eight-stage memory buffer FIFO
  - MCDMA controller integrated inside ARM subsystem
    - This DMA focus on data transfer for video
    - Embedded DMA with one channel and three master interface
    - one master interface is directly for writing data to L1 Memory of DSP, which is fixed data transfer direction, two another master interface is general one
    - Support high-performance data transfer between ARM system and DSP system with asynchronous FIFO

- **Interrupt Controller**
  - Two Interrupt Controller in chip
  - DW_INTC integrated inside ARM9 subsystem
    - Support 48 IRQ normal interrupt sources and 2 FIQ fast interrupt sources
    - Vectored interrupts support
    - Software interrupts support
    - Programmable interrupt priorities
    - Fixed High Level sensitive triggered interrupts
  - ICU (Interrupt Control unit) integrated inside DSP subsystem
    - 48 interrupt sources , each may be linked to different interrupt inputs for DSP core
    - Software triggering to all 48 interrupt sources

- Configurable source interrupt polarity (low/high)
- External interrupt source with software configuration to edge/level sensitive

- **USB interface**
  - USB OTG 2.0 interface
    - Complies with the OTG Supplement to the USB2.0 Specification
    - Operates in High-Speed and Full-Speed mode
    - Support Session Request Protocol(SRP) and Host Negotiation Protocol(HNP)
    - Support 6 channels in host mode
    - 6 endpoints , 3 in and 3 out
    - Built-in one 1777 x 35bits FIFO
  - USB HOST 1.0 interface
    - Complies with the USB1.1 Specfication
    - Operates in Full-Speed mode
    - Operates in host mode
    - Support 2 channels in host mode
    - Built-in one 70 x 35 bits FIFO

- **High-speed ADC interface**
  - Max frequency is 64MHz
  - Standard AMBA2.0 Slave interface
  - Dual 8/10 bits A/D converter Interface
  - Support 2bit data bus from GPS tunner
  - Support TS stream data transfer

- **HOST interface**
  - Programmable 8bit/16bit data width
  - Embedded 4KB dual-port buffer for data transfer
  - Compatible with MCU interface timing
  - Interrupt request for data exchange
  - Support Host interface function disable
  - Support address self-increment when accessing buffer by MCU interface
  - Support LCD bypass function with 18bit data bus, ,bypass IO mapping relationship is programmable (totally 4 types)
  - Software or hardware control for LCD bypass enable

- **Low_speed Peripheral interface**
  - Serial Peripheral Interface (SPI) Master Controller
    - Support two slave devices connection
    - Compatible with Motorola SPI , TI Synchronous Serial Protocol or National Semiconductor Microwire interface
    - Dynamic control of serial bit rate of data transfer by programmable sclk_out frequency, which is half of PCLK in max mode
    - FIFO depth for transmit and receive are also 32x16bits
    - Programmable data item size ,from 4 to 16bits
    - Support DMA based and interrupt based operation
  - Serial Peripheral Interface (SPI) Slave Controller
    - Compatible with Motorola SPI , TI Synchronous Serial Protocol or National Semiconductor Microwire interface
    - Dynamic control of serial bit rate of data transfer by sclk_in from master device
    - FIFO depth for transmit and receive are also 32x16bits
    - Programmable data item size ,from 4 to 16bits

- DMA based and interrupt based operation
- UART
  - 4 UART support in chip
  - UART0 support modem function and Irdn function
  - UART1 support IrDA 1.0 SIR mode and Serial data transfer without auto flow-control function
  - UART2 only for Serial data transfer without auto flow-control function
  - UART3 only for Serial data transfer with auto flow-control function
  - Based on the 16550 industry standard
  - Programmable serial data baud rate, up to 3Mbps baud-rate , and main clock is 48MHz in max mode
  - Programmable baud rate generator. This enables division of the internal clock by (1 ~ 65535 x 16) and generates an internal x16 clock
  - Standard asynchronous communication bits (start, stop and parity).
  - DMA based and interrupt based operation
  - FIFO depth for data transfer is always 32x8bits
  - For UART1, In IrDA SIR mode, support configurable baud data rate up to 115.2K and a pulse duration as specified in the IrDA physical layer specification
- I2C controller
  - 2 I2C controllers integrated in chip
  - Multi masters operation support
  - Software programmable clock frequency and transfer rate up to 100Kbit/s in standard mode or up to 400Kbit/s in Fast mode
  - Supports 7 bits and 10 bits addressing modes
- I2S
  - Support mono/stereo audio file
  - Support audio resolution: 8, 16 bits
  - Support audio sample rate from 32KHz to 96 KHz
  - Support I2S, Left-Justified and Right-Justified digital serial data format
- PWM
  - Built-in three 32 bit timer modulers
  - Programmable counter
  - Chained timer for long period purpose
  - 4-channel 32-bit timer with Pulse Width Modulation (PWM)
  - Programmable duty-cycle, and frequency output
- General Purpose IO (GPIO)
  - Support 96 individually programmable input/output pins
  - 16 GPIOs with external interrupt capability
- Timers in CPU system
  - Built-in Three 32 bits timer modules
  - Support for two operation modes : free-running and user-defined count
- Timers in DSP system
  - Built-in two 32 bits timer modules
  - Support for 5 various counting modes : Single Count mode, Auto-restart mode , Free-running , Event Count mode and Watchdog Timer mode
  - Pulse Width Modulation(PWM) mechanism
  - Three possible input clock signals: internal , external and cascaded
- Watchdog Timer (WDT)
  - Watchdog function (Generate a system reset or an interrupt)
  - Built-in 32 bits programmable counter
- Real Time Clock (RTC)
  - Support perpetual RTC core power
  - Programmable alarm with interrupt for system power wake up
  - System power off sequence with output control pin

- **Analog IP interface**
  - ADC Converter

- 4-channel single-ended 10-bit 1MSPS Successive Approximation Register (SAR) analog-to-digital converter
- No off-chip components required
- DNL less than +/-1 LSB , INL less than +/-1.5 LSB
- Supply 2.8V to 3.6V for analog interface

- eFuse
  - 64-bit serial eFuse macro
  - Be programmed one bit at a time, but all 64bits can be read at the same time.
  - 2.9V (+/-200mV) & 2.5V(+/-50mV) Programm voltage
  - 3.3V & 0V Sense voltage

- **Package Type**
  - RK2818 BGA324

1.3 Block Diagram

The following figure shows block diagram of RK2818.
RK2818 can be divided into two sub system : DSP System and CPU System.

- DSP System
  - XDMA : three-dimensional DMA , used to data transfer for video decoder or other algorithm
  - High-Speed ADC Interface : focus on completing data reveiver from tuner in DVB-T,DAB, T-DMB,GPS application with software method.
  - Video hardware accelerator: work together with software algorithm to generate high-performance H.264 video decoder
  - ICU : Interrupt controller for DSP processor
  - PIU : processor interface unit, used to complete communication between DSP and CPU
  - PMU ：power management unit, used to control clock and reset to save power for modules inside DSP system
  - General reg file : focus on general control on DSP system by software method, composed of some register groups
- CPU System
  - DW_DMA : used to data transfer for audio and low-speed peripheral
  - MC_DMA: used for general data transfer, especially one data path from external memory directly to DSP L1 DMEM to improve video decoder efficiency
  - SCU : focus on clock gating , clock frequency switch, reset control , power on/off and system mode switch for CPU system to save power
  - PMU : used to complete power on/off switch control for RK2818
  - INTC : Interrupt controller for CPU processor
  - General reg file : focus on general control on CPU system by software method, composed of some register groups, including IO mux control,IO PAD pull up/down control and other system control signals .

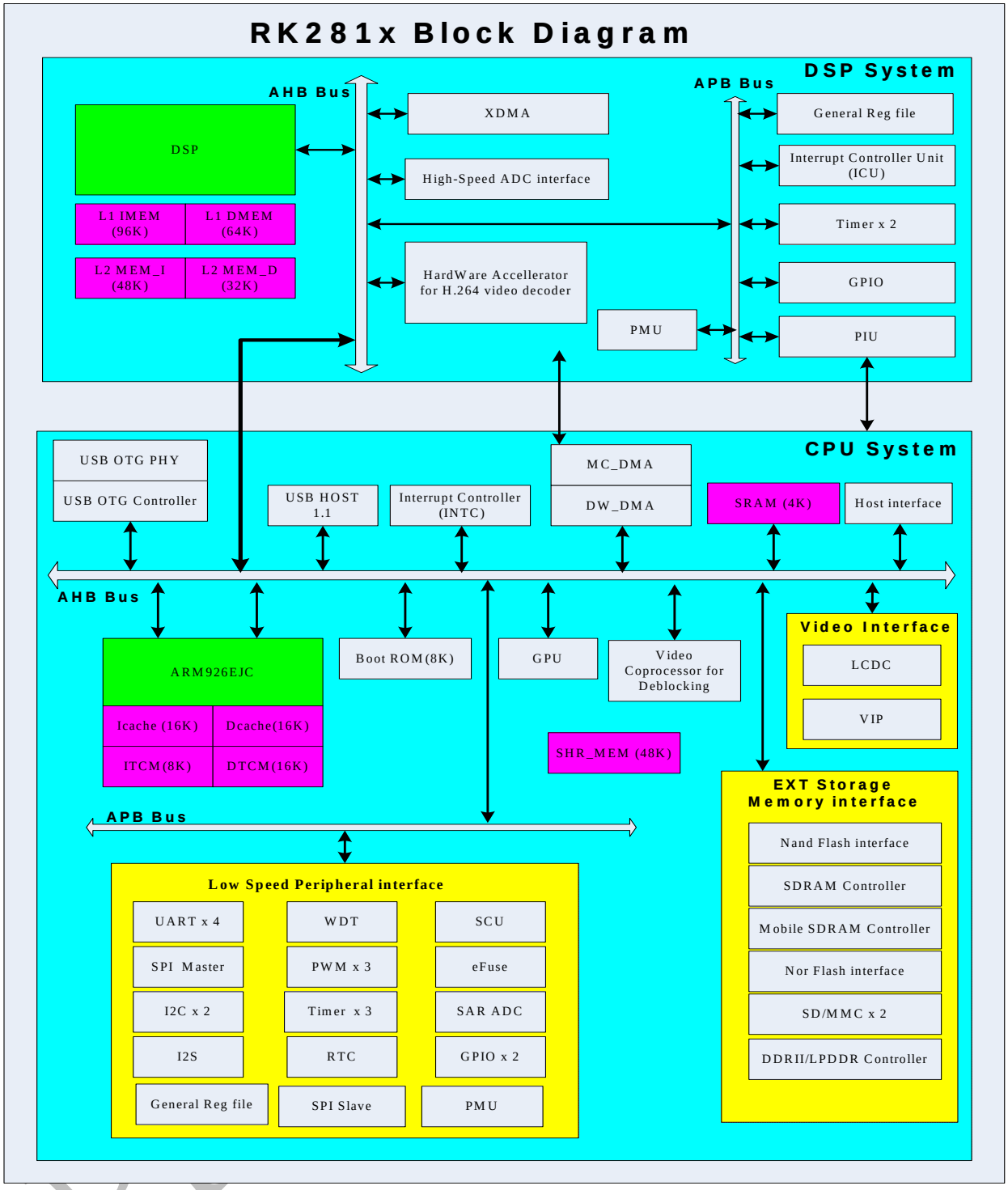


Fig. 1-1 RK2818 Block Diagram

Chapter 2 Pin Description

2.1 PIN Placement

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	MEM_D0	LCD_D6	PD3/LCD_D11	PC6/LCD_D22	PC5/LCD_D21	PD4/LCD_D12	PC0/LCD_D16	LCD_HSYNC	SM_A15	TDO	PA3	PA2	PB1/SM_CS1/SDMMC0_PCA	USB11_DVDD	USB11_DM	RTC_DVDD33	RTC_AVDD	VIP_CLKI	A
B	MEM_D3	MEM_D1	LCD_D4	LCD_D3	LCD_D7	PD1/LCD_D9	PD6/LCD_D14	LCD_DEN	LCDBP	TCK	ST0_CSN	VIP_D6	PF6/VIP_CLKO	USB11_DVSS	USB11_DP	RTCINT_OUT	PWR_GOOD	VCC_VIP_1	B
C	MEM_DQS0P	MEM_DQS0M	MEM_D2	PC2/LCD_D18	LCD_D5	PD0/LCD_D8	PD7/LCD_D15	LCD_DCLK	SM_A10	OPMODE1	TDI	VCC_VIP_2	VIP_VSYNC	PH7/VIP_LD3	PF5/PWM3/VIP_LD1	PE0/VIP_LD0	XIN32K	XOUT32K	C
D	MEM_D9	MEM_D7	MEM_D4	MEM_DM0	LCD_D0	LCD_D2	PD2/LCD_D10	PC1/LCD_D17	RTCK	TMS	PF4/PWM2/SDMMC0_WP	VIP_D7	VIP_D4	PH6/VIP_LD2	HOST_D0	HOST_D4	VSSA_CODECPLL	VDDA_CODECPLL	D
E	MEM_D11	MEM_D8	MEM_DM1	MEM_D6	MEM_VSSQ0	PC3/LCD_D19	VCC_LCD_2	PD5/LCD_D13	OPMODE0	TRSTN	VIP_D3	VIP_D5	VIP_D2	HOST_D2	HOST_D6	AP2BB_INT	VSSA_ARMPLL	VDDA_ARMPLL	E
F	MEM_DQS1P	MEM_DQS1M	MEM_D5	MEM_D10	MEM_A14	MEM_VDDQ0	PC4/LCD_D20	LCD_D1	LCD_VSYNC	VCC_LCD_1	VIP_D1	VIP_D0	HOST_D1	HOST_A0	HOST_D7	HOST_A1	VSSA_DSPPLL	VDDA_DSPPLL	F
G	MEM_D14	MEM_D12	MEM_D15	MEM_D13	MEM_A13	MEM_VSSQ1	VDDCORE	VDDCORE	VCCIO	PC7/LCD_D23	PF2/PWM0	VIP_HREF	HOST_D3	EXTDDR_SEL	NPOR	EXTMSDR_SEL	EWAKEUP_STOP	TEST	G
H	MEM_A9	MEM_A12	MEM_A6	MEM_A5	MEM_VDDQ1	GND	GND	GND	GND	VCCIO	VCCIO	HOST_D5	EXTCLK	EWAKEUP_POWER	BTMODE	HSADC_ID1	HSADC_QD1/HOST_D9	HSADC_ID0	H
J	MEM_A3	MEM_A4	MEM_A8	MEM_VDDQ2	VDDCORE	GND	GND	GND	GND	VDDCORE	VCCIO	HSADC_QD0/HOST_D8	HSADC_QD2/HOST_D10	HSADC_ID5	HSADC_QD4/HOST_D12	HSADC_ID3	HSADC_QD5/HOST_D13	HSADC_ID2	J
K	MEM_A1	MEM_A2	MEM_A7	MEM_VSSQ2	VDDCORE	GND	GND	GND	GND	VDDCORE	VCCIO	HSADC_QD7/HOST_D15	HOST_RDN	HSADC_QD9/SM_OEN	HSADC_ID7	HSADC_ID9	HSADC_QD8/SM_WEN	HSADC_QD3/HOST_D11	K
L	MEM_CLK	MEM_CLKN	MEM_A11	MEM_A10	MEM_VREF	GND	GND	GND	GND	VCCIO	PB7/SPI0_RXD/SDMMC0_D7	PE6/UART1_SIR_IN/I2C1_SDA	PF0/UART1_RX/CX_T0_PWM	GPS_CLK/HSADC_CLKOUT	PB3/UART0_RTSN	HSADC_ID6	HOST_CSN	HSADC_ID4	L
M	MEM_A0	MEM_BA2	MEM_CSN0	MEM_RASN	MEM_VSSQ3	MEM_VSSQ4	VDDCORE	VDDCORE	FLASH_D7	FLASH_RDY	PG5/SDMC1_D2	PB5/SPI0_CLKO/SDMMC0_D5	HSADC_ID8	PA0/HOST_D16	PF1/UART1_TX/CX_T1_PWM	PG0/UART0_RX/SDMMC1_DET	HSADC_QD6/HOST_D14	XOUT24M	M
N	MEM_CKE	MEM_BA0	MEM_OPEN1	MEM_D16	MEM_VDDQ3	MEM_VSSQ5	PE3/SPI_RXD/FLASH_CS6	PE2/SPI_SSIN/FLASH_CS5	FLASH_D5	PA5/FLASH_CS1	USBPHY_AVSS1	PH5/SDMC0_CLKO	PG7/SDMC1_CLKO	PG3/SDMC1_D0	PF3/PWM1/SDMMC0_DET	PG1/UART0_TX/SDMMC1_WP	PA1/HOST_D17	XIN24M	N
P	MEM_CKE_LPDDR	MEM_OPEN2	MEM_D19	MEM_D20	MEM_VDDQ4	PE1/SPI_CLKI/FLASH_CS4	FLASH_D0	MEM_VDDQ5	FLASH_D1	FLASH_RDN	USBPHY_DVSS	ID	PE5/I2C0_SCL	I2S_SCLK	PH3/SDMC0_D2	PG6/SDMC1_D3	PB0/SPI0_CS1/SDMMC1_PCA	HOST_WRN	P
R	MEM_BA1	MEM_ODT0	MEM_DM2	MEM_D21	MEM_D22	MEM_D26	MEM_D29	PF7/SPI_TXD/FLASH_CS7	VCC_NAND	FLASH_WP	USBPHY_DVDD	VBUS	VDDA_SARADC	I2S_SDI	PE4/I2C0_SDA	PG4/SDMC1_D1	PB4/SPI0_CSN0/SDMMC0_D4	PE7/UART1_SIR_OUT/I2C1_SCL	R
T	MEM_CASN	MEM_CSN1	MEM_OPEN3	MEM_D18	MEM_D27	MEM_D30	MEM_D17	FLASH_D6	PA6/FLASH_CS2	FLASH_ALE	USBPHY_AVDD25	USBPHY_AVDD33	ADC_AIN0	FSOURCE_EFUSE	OTG_DRVVBUS	PH0/SDMC0_CMD	PG2/SDMC1_CMD	PB2/UART0_CTSN	T
U	MEM_WEN	MEM_DQS2P	MEM_ODT1	MEM_D25	MEM_DQS3P	MEM_D31	MEM_D23	FLASH_D3	FLASH_CS0	FLASH_CLE	DP	RKELVIN	ADC_AIN1	VGATE_EFUSE	I2S_SDO	I2S_CLK	PH1/SDMC0_D0	PB6/SPI0_TXD/SDMMC0_D6	U
V	MEM_DQS2M	MEM_OPEN0	MEM_D24	MEM_DQS3M	MEM_D28	MEM_DM3	FLASH_D2	FLASH_D4	PA7/FLASH_CS3	FLASH_WRN	DM	USBPHY_AVSS0	ADC_AIN2	VSSA_SARADC	I2S_LRCK	PA4/I2S_LRCK_RX	PH2/SDMC0_D1	PH4/SDMC0_D3	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

The following table shows all of the pins for RK2818. According to differenct application, part of pins will be bonded out, or double/triple bonded .

The first column in the pin function description is default function after power on reset, and function in the last two columns will be implemented by software set. The detailed register descriptions are IOMUX_A_CON and IOMUX_B_CON in chapter 34.

As for GPIOm_n[i] (m = 0,1 ; n = A~D ; i = 0~7) , we can control Pull up or Pull Down or no resistor for them by software set. The value for Pull up/down type in the following table is default after power on reset. The detailed register descriptions are in chapter 34.

Notes I --- input pins
O --- output pins
B --- bidirectional pins
P --- power supply pins (digital and analog)
G --- ground supply pins (digital and analog)
A --- Analog IO pins
OSC --- oscillator IO pins

2.2 Table 2-1 RK2818 Pin Description

PIN LOCATION	PIN NAME	PIN Direction	Pin Description
Global signals			
E9	OPMODE0	I Pull Down	00 : ARM9 JTAG 01 : DSP JTAG 10 : ARM9+DSP JTAG 11 : Reserved
C10	OPMODE1	I Pull Down	
H15	BTMODE	I Pull Down	0 : Boot from ROM 1 : Boot from NorFlash
G17	EWAKEUP_STOP	I Pull Down	External wakeup ARM9 from stop mode
H14	EWAKEUP_POWER	I Pull Down	External wakeup power for ARM subsys
G16	EXTMSDR_SEL	I Pull Down	external memory select 00: SDR-SDRAM 01: Mobile SDR-SDRAM 10: DDRII 11: Mobile DDR
G14	EXTDDR_SEL	I Pull Down	
B9	LCDBP	I Pull Down	lcd bypass enable 0 : disable 1 : enable
G15	NPOR	I	Power on Reset
G18	TEST	I Pull Down	Test mode select 0 : Normal function mode 1 : Test mode
N18	XIN24M	I OSC	Crystal 24M input pad
M18	XOUT24M	O OSC	Crystal 24M output pad
H13	EXTCLK	I Pull Down	Ext clock input pad
D11	Nand_SEL	B Pull Down	Nand voltage select when bootup: High: 1.8V NandFlash Low: 3.3V NandFlash
		B Pull Down	GPIO1 PortB[4]
		B	pwm
		I	sdmmc0 write protect
		O	uart3 serial data output
JTAG signals			
B10	TCK	I Pull Up	JTAG TCK
E10	TRSTN	I Pull Down	JTAG TRST
C11	TDI	I Pull Up	JTAG TDI
D10	TMS	I Pull Up	JTAG TMS
A10	TDO	O	JTAG TDO
D9	RTCK	O	JTAG RTCK
I2S			
R14	I2S_SDI	I Pull Down	i2s sdi from codec
		B Pull Down	gpio2[27]

U15	I2S_SDO	O	i2s sdo to codec
		B Pull Down	gpio2[28]
U16	I2S_CLK	O	i2s clock out to codec
		B Pull Down	gpio2[29]
V15	I2S_LRCK	B Pull Down	i2s lrck/i2s_lrck_tx
		B Pull Down	gpio2[30]
V16	PA4/I2S_LRCK_RX	B Pull Up	GPIO0 PortA[4]
		B	i2s_lrck_rx
P14	I2S_SCLK	B Pull Down	i2s serial clock
		B Pull Down	gpio2[31]
UART0			
M16	PG0/UART0_RX/SDMMC1_DET	B Pull Down	GPIO1 PortC[0]
		I	uart0 serial data in
		I	sdmmc1 card detect
N16	PG1/UART0_TX/SDMMC1_WP	B Pull Down	GPIO1 PortC[1]
		O	uart0 serial data out
		I	sdmmc1 card write protect
T18	PB2/UART0_CTSN	B Pull Up	GPIO0 PortB[2]
		I	uart0 modem signal
L15	PB3/UART0_RTSN	B Pull Up	GPIO0 PortB[3]
		O	uart0 modem signal
UART1			
L13	PF0/UART1_RX/CX_T0_PWM	B Pull Down	GPIO1 PortB[0]
		I	uart1 serial data in
		O	pwm out from ceva
M15	PF1/UART1_TX/CX_T1_PWM	B Pull Down	GPIO1 PortB[1]
		O	uart1 serial data out
		O	pwm out from ceva
UART2			
P17	PB0/SPI0_CS1/UART2_RX	B Pull Up	GPIO0 PortB[0]
		O	spi0 second chip select
		O	sdmmc1 power control
		I	uart2 serial data input
A13	PB1/SM_CS1/UART2_TX	B Pull Up	GPIO0 PortB[1]
		O	nor flash second chip select
		O	uart2 serial data output
		O	sdmmc0 power control
A12	PA2/uart2_cts_n	B Pull Up	GPIO0 PortA[2]
		I	uart2 modem signal
A11	PA3/uart2_rts_n	B Pull Up	GPIO0 PortA[3]
		O	uart2 modem signal
SPI0			
R17	PB4/SPI0_CSN0/SDMMC0_D4	B Pull Up	GPIO0 PortB[4]
		O	spi0 first chip select
		B	sdmmc0 data bit4
M12	PB5/SPI0_CLKO/SDMMC0_D5	B Pull Up	GPIO0 PortB[5]
		O	spi0 clk out
		B	sdmmc0 data bit5
U18	PB6/SPI0_TXD/SDMMC0_D6	B Pull Up	GPIO0 PortB[6]
		O	spi0 txd
		B	sdmmc0 data bit6
L11	PB7/SPI0_RXD/SDMMC0_D7	B Pull Up	GPIO0 PortB[7]
		I	spi0 rxd
		B	sdmmc0 data bit7
SPI1			
P6	PE1/SPI_CLKI/FLA	B Pull Down	GPIO1 PortA[1]

	SH_CS4	I	spi1 slave mode clock signal
		O	flash cs 4
N8	PE2/SPI_SSIN/FLASH_CS5	B Pull Down	GPIO1 PortA[2]
		I	spi1 slave mode select signal
		O	flash cs 5
N7	PE3/SPI_RXD/FLASH_CS6	B Pull Down	GPIO1 PortA[3]
		I	spi1 rxd
		O	flash cs 6
R8	PF7/SPI_TXD/FLASH_CS7	B Pull Down	GPIO1 PortB[7]
		O	spi1 txd
		O	flash cs 7
I2C0			
R15	I2C0_SDA/PE4	B Pull Up	i2c0 sda
		B Pull UP	GPIO1 PortA[4]
P13	I2C0_SCL/PE5	B Pull UP	i2c0 scl
		B Pull UP	GPIO1 PortA[5]
I2C1			
L12	PE6/UART1_SIR_IN/I2C1_SDA	B Pull UP	GPIO1 PortA[6]
		I	uart1 IR data in
		B Pull UP	i2c1 sda
R18	PE7/UART1_SIR_OUT/I2C1_SCL	B Pull UP	GPIO1 PortA[7]
		O	uart1 IR data out
		B Pull UP	i2c1 scl
PWM			
G11	PF2/PWM0	B Pull Down	GPIO1 PortB[2]
		B	pwm
N15	PF3/PWM1/SDMMC0_DET	B Pull Down	GPIO1 PortB[3]
		B	pwm
		I	sdmmc0 detect signal
		I	uart3 serial data input
D11	PF4/PWM2/SDMMC0_WP	B Pull Down	GPIO1 PortB[4]
		B	pwm
		I	sdmmc0 write protect
		O	uart3 serial data output
SDMMC0			
T16	PH0/SDMMC0_CMD	B Pull Down	GPIO1 PortD[0]
		B	sdmmc0 command
U17	PH1/SDMMC0_D0	B Pull Down	GPIO1 PortD[1]
		B	sdmmc0 data bit0
V17	PH2/SDMMC0_D1	B Pull Down	GPIO1 PortD[2]
		B	sdmmc0 data bit1
P15	PH3/SDMMC0_D2	B Pull Down	GPIO1 PortD[3]
		B	sdmmc0 data bit2
V18	PH4/SDMMC0_D3	B Pull Down	GPIO1 PortD[4]
		B	sdmmc0 data bit3
N12	PH5/SDMMC0_CLKO	B Pull Down	GPIO1 PortD[5]
		O	sdmmc0 clock out
SDMMC1			
T17	PG2/SDMMC1_CMD	B Pull Down	GPIO1 PortC[2]
		B	sdmmc1 command
N14	PG3/SDMMC1_D0	B Pull Down	GPIO1 PortC[3]
		B	sdmmc1 data bit0
R16	PG4/SDMMC1_D1	B Pull Down	GPIO1 PortC[4]
		B	sdmmc1 data bit1
M11	PG5/SDMMC1_D2	B Pull Down	GPIO1 PortC[5]
		B	sdmmc1 data bit2

P16	PG6/SDMMC1_D3	B Pull Down	GPIO1 PortC[6]
		B	sdmmc1 data bit3
N13	PG7/SDMMC1_CLKO	B Pull Down	GPIO1 PortC[7]
		O	sdmmc1 clk out
HOST INTERFACE			
D15	HOST_D0	B Pull UP	gpio2[0]
		B	host interface data bit0
F13	HOST_D1	B Pull UP	gpio2[1]
		B	host interface data bit1
E14	HOST_D2	B Pull UP	gpio2[2]
		B	host interface data bit2
G13	HOST_D3	B Pull UP	gpio2[3]
		B	host interface data bit3
D16	HOST_D4	B Pull UP	gpio2[4]
		B	host interface data bit4
H12	HOST_D5	B Pull UP	gpio2[5]
		B	host interface data bit5
E15	HOST_D6	B Pull UP	gpio2[6]
		B	host interface data bit6
F15	HOST_D7	B Pull UP	gpio2[7]
		B	host interface data bit7
J12	HSADC_QD0/HOST_D8	B Pull UP	gpio2[14]
		I	hsadc data bit0 for Q path
		B	host interface data bit8
H17	HSADC_QD1/HOST_D9	B Pull UP	gpio2[15]
		I	hsadc data bit1 for Q path
		B	host interface data bit8
J13	HSADC_QD2/HOST_D10	B Pull Down	gpio2[16]
		I	hsadc data bit2 for Q path
		B	host interface data bit8
K18	HSADC_QD3/HOST_D11	B Pull Down	gpio2[17]
		I	hsadc data bit3 for Q path
		B	host interface data bit8
J15	HSADC_QD4/HOST_D12	B Pull Down	gpio2[18]
		I	hsadc data bit4 for Q path
		B	host interface data bit8
J17	HSADC_QD5/HOST_D13	B Pull Down	gpio2[19]
		I	hsadc data bit5 for Q path
		B	host interface data bit8
M17	HSADC_QD6/HOST_D14	B Pull Down	gpio2[20]
		I	hsadc data bit6 for Q path
		B	host interface data bit8
K12	HSADC_QD7/HOST_D15	B Pull Down	gpio2[21]
		I	hsadc data bit7 for Q path
		B	host interface data bit8
M14	PA0/HOST_D16	B Pull Up	GPIO0 PortA[0]
		I	host_data[16]
N17	PA1/HOST_D17	B Pull Up	GPIO0 PortA[1]
		I	host_data[17]
F14	HOST_A0	B Pull UP	gpio2[8]
		I	host interface addr bit0
F16	HOST_A1	B Pull UP	gpio2[9]
		I	host interface addr bit1
L17	HOST_CSN	B Pull UP	gpio2[10]
		I	host interface chip select
K13	HOST_RDN	B Pull UP	gpio2[11]

		I	host interface read valid signal
P18	HOST_WRN	B Pull UP	gpio2[12]
		I	host interface write valid signal
E16	AP2BB_INT	B Pull UP	gpio2[13]
		O	host interface interrupt from chip to host
VIP			
C16	PE0/VIP_LD0	B Pull Down	GPIO1 PortA[0]
		I Pull Down	vip data input0
C15	PF5/PWM3/VIP_LD1	B Pull Down	GPIO1 PortB[5]
		B	pwm 3
		I Pull Down	vip data input1
D14	PH6/VIP_LD2	B Pull Down	GPIO1 PortD[6]
		I Pull Down	vip data input2
C14	PH7/VIP_LD3	B Pull Down	GPIO1 PortD[7]
		I Pull Down	vip data input3
F12	VIP_D0	I Pull Down	vip data input4
F11	VIP_D1	I Pull Down	vip data input5
E13	VIP_D2	I Pull Down	vip data input6
E11	VIP_D3	I Pull Down	vip data input7
D13	VIP_D4	I Pull Down	vip data input8
E12	VIP_D5	I Pull Down	vip data input9
B12	VIP_D6	I Pull Down	vip data input10
D12	VIP_D7	I Pull Down	vip data input11
C13	VIP_VSYNC	I Pull Down	vip vertical sync signal
G12	VIP_HREF	I Pull Down	vip horizontal sync signal
A18	VIP_CLKI	I Pull Down	vip clock input from sensor
B13	PF6/VIP_CLKO	B Pull Down	GPIO1 PortB[6]
		O	sensor clk out
SDT Memory			
C9	SM_A10	O	SRAM addr[10]
A9	SM_A15	O	SRAM addr[15]
	SM_A16	O	SRAM addr[16]
	SM_A17	O	SRAM addr[17]
	SM_A18	O	SRAM addr[18]
	SM_A19	O	SRAM addr[19]
	SM_A20	O	SRAM addr[20]
B11	ST0_CSN	O	SRAM cen0
K14	HSADC_QD9/SM_OEN	B Pull Down	gpio
		I	hsadc data bit9 for Q path
		O	SRAM oen
K17	HSADC_QD8/SM_WEN	B Pull Down	gpio
		I	hsadc data bit8 for Q path
		O	SRAM wen
RTC			
B16	RTCINT_OUT	O	RTC int out
B17	RTC_PWR_GOOD	I Pull Up	RTC power good input
C17	XIN32K	I OSC	Crystal 32K input pad
C18	XOUT32K	O OSC	Crystal 32K output pad
Nand Flash			
P7	FLASH_D0	B	nand flash data[0]
P9	FLASH_D1	B	nand flash data[1]
V7	FLASH_D2	B	nand flash data[2]
U8	FLASH_D3	B	nand flash data[3]
V8	FLASH_D4	B	nand flash data[4]
N9	FLASH_D5	B	nand flash data[5]
T8	FLASH_D6	B	nand flash data[6]

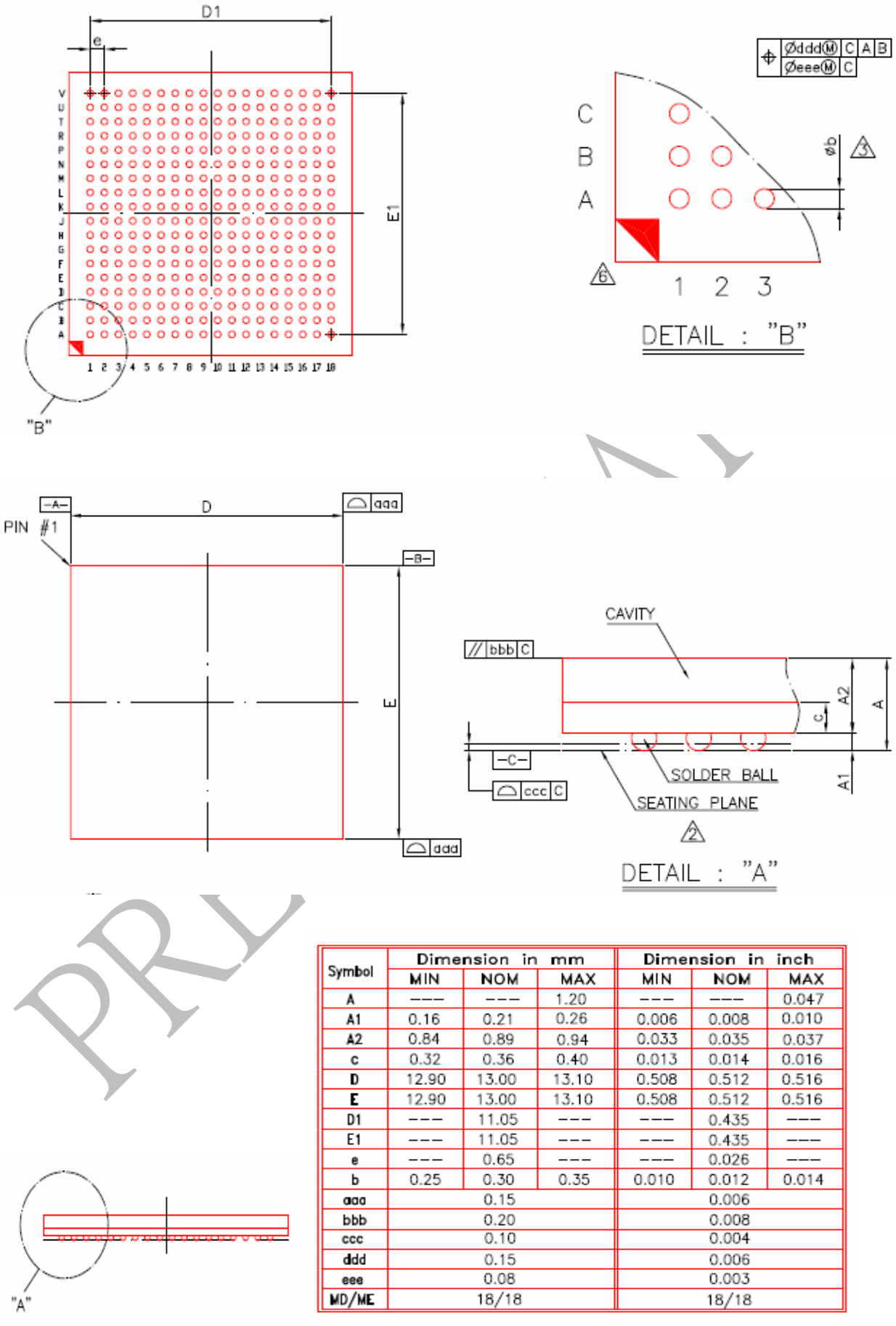
M9	FLASH_D7	B	nand flash data[7]
M10	FLASH_RDY	I Pull Up	nand flash ready/busy
T10	FLASH_ALE	O	nand flash ale
U10	FLASH_CLE	O	nand flash cle
P10	FLASH_RDN	O	nand flash rdn
V10	FLASH_WRN	O	nand flash wrn
R10	FLASH_WP	O	nand flash wp
U9	FLASH_CS0	O	nand flash cs0
N10	PA5/FLASH_CS1	B Pull Up	GPIO0 PortA[5]
		O	nand flash cs1
T9	PA6/FLASH_CS2	B Pull Up	GPIO0 PortA[6]
		O	nand flash cs2
V9	PA7/FLASH_CS3	B Pull Up	GPIO0 PortA[7]
		O	nand flash cs3
LCDC			
D5	LCD_D0	O	lcd data[0]
F8	LCD_D1	O	lcd data[1]
D6	LCD_D2	O	lcd data[2]
B4	LCD_D3	O	lcd data[3]
B3	LCD_D4	O	lcd data[4]
C5	LCD_D5	O	lcd data[5]
A2	LCD_D6	O	lcd data[6]
B5	LCD_D7	O	lcd data[7]
C6	PD0/LCD_D8	B Pull Up	GPIO0 PortD[0]
		O	lcdc data bit8
B6	PD1/LCD_D9	B Pull Up	GPIO0 PortD[1]
		O	lcdc data bit9
D7	PD2/LCD_D10	B Pull Up	GPIO0 PortD[2]
		O	lcdc data bit10
A3	PD3/LCD_D11	B Pull Up	GPIO0 PortD[3]
		O	lcdc data bit11
A6	PD4/LCD_D12	B Pull Up	GPIO0 PortD[4]
		O	lcdc data bit12
E8	PD5/LCD_D13	B Pull Up	GPIO0 PortD[5]
		O	lcdc data bit13
B7	PD6/LCD_D14	B Pull Up	GPIO0 PortD[6]
		O	lcdc data bit14
C7	PD7/LCD_D15	B Pull Up	GPIO0 PortD[7]
		O	lcdc data bit15
A7	PC0/LCD_D16	B Pull Up	GPIO0 PortC[0]
		O	lcdc data bit16
D8	PC1/LCD_D17	B Pull Up	GPIO0 PortC[1]
		O	lcdc data bit17
C4	PC2/LCD_D18	B Pull Up	GPIO0 PortC[2]
		O	lcdc data bit18
E6	PC3/LCD_D19	B Pull Up	GPIO0 PortC[3]
		O	lcdc data bit19
F7	PC4/LCD_D20	B Pull Up	GPIO0 PortC[4]
		O	lcdc data bit20
A5	PC5/LCD_D21	B Pull Up	GPIO0 PortC[5]
		O	lcdc data bit21
A4	PC6/LCD_D22	B Pull Up	GPIO0 PortC[6]
		O	lcdc data bit22
G10	PC7/LCD_D23	B Pull Up	GPIO0 PortC[7]
		O	lcdc data bit23
A8	LCD_HSYNC	O	lcdc horizontal sync signal

C8	LCD_DCLK	O	lcdc data clock
F9	LCD_VSYNC	B Pull Up	gpio2[25]
		O	lcdc vertical sync signal
B8	LCD_DEN	B Pull Down	gpio2[26]
		O	lcdc data valid signal
HS ADC			
H18	HSADC_ID0	I Pull Down	hsadc data bit0 for I Path
H16	HSADC_ID1	I Pull Down	hsadc data bit1 for I Path
J18	HSADC_ID2	I Pull Down	hsadc data bit2 for I Path
J16	HSADC_ID3	I Pull Down	hsadc data bit3 for I Path
L18	HSADC_ID4	I Pull Down	hsadc data bit4 for I Path
J14	HSADC_ID5	I Pull Down	hsadc data bit5 for I Path
L16	HSADC_ID6	I Pull Down	hsadc data bit6 for I Path
K15	HSADC_ID7	I Pull Down	hsadc data bit7 for I Path
M13	HSADC_ID8/ts_valid	I Pull Down	hsadc data bit8 for I Path
		I Pull Down	ts stream valid signal
K16	HSADC_ID9/ts_fail	I Pull Down	hsadc data bit9 for I Path
		I Pull Down	ts stream fail signal
L14	GPS_CLK/HSADC_CLKOUT	B Pull Down	gpio2[24]
		I Pull Down	clock input for gps application
		O	clock out to hsadc analog
SAR ADC			
T13	ADC_AIN0	A	10bit adc channel0 input
U13	ADC_AIN1	A	10bit adc channel1 input
V13	ADC_AIN2	A	10bit adc channel2 input
R13	VDDA_SARADC	P	10bit adc analog power
V14	VSSA_SARADC	P	10bit adc analog ground
eFuse			
U14	VGATE_EFUSE	A	GATE POWER SUPPLY OF EFUSE, CONNECT TO VDD FOR READ OPERATION
T14	FSOURCE_EFUSE	A	SOURCE POWER SUPPLY OF EFUSE, CONNECT TO GROUND FOR READ OPERATION
PLL			
F18	VDDA_DSPPLL	P	DSP PLL Analog power
F17	VSSA_DSPPLL	P	DSP PLL Analog ground
E18	VDDA_ARMPLL	P	ARM PLL Analog power
E17	VSSA_ARMPLL	P	ARM PLL Analog ground
D18	VDDA_CODECPLL	P	CODEC PLL Analog power
D17	VSSA_CODECPLL	P	CODEC PLL Analog ground
USB			
N11	USBPHY_AVSS1	G	USB ANALOG GROUND (0V)
P11	USBPHY_DVSS	G	USB DIGITAL GROUND (0V)
R11	USBPHY_DVDD	P	USB DIGITAL POWER SUPPLY (1.2V)
T11	USBPHY_AVDD25	P	USB ANALOG POWER SUPPLY (2.5V)
U11	DP	A	USB D- SIGNAL
V11	DM	A	USB D+ SIGNAL
P12	ID	I	USB MINNI-RECEPTABLE IDENTIFIER
R12	VBUS	P	USB DEDECT INPUT
T12	USBPHY_AVDD33	P	USB ANALOG POWER SUPPLY (3.3V)
U12	RKELVIN	A	TRANSMITTER RESISTOR TUNE PIN
V12	USBPHY_AVSS0	G	USB ANALOG GROUND (0V)
T15	OTG_DRVVBUS	O	USB DRIVE VBUS POWER CONTROLE SIGNAL
USB11			
A15	USB11_DM	A	USB11 D+ SIGNAL
B15	USB11_DP	A	USB11 D- SIGNAL
A14	USB11_DVDD	P	USB11 POWER SUPPLY (3.3V)

B14	USB11_DVSS	P	USB11 GROUND
SDR/DDRII/MOBILE DRR			
A1	MEM_D0	B	SDR/MSDR/DDRII/MDDR data bit[0]
B2	MEM_D1	B	SDR/MSDR/DDRII/MDDR data bit[1]
C3	MEM_D2	B	SDR/MSDR/DDRII/MDDR data bit[2]
B1	MEM_D3	B	SDR/MSDR/DDRII/MDDR data bit[3]
D3	MEM_D4	B	SDR/MSDR/DDRII/MDDR data bit[4]
F3	MEM_D5	B	SDR/MSDR/DDRII/MDDR data bit[5]
E4	MEM_D6	B	SDR/MSDR/DDRII/MDDR data bit[6]
D2	MEM_D7	B	SDR/MSDR/DDRII/MDDR data bit[7]
E2	MEM_D8	B	SDR/MSDR/DDRII/MDDR data bit[8]
D1	MEM_D9	B	SDR/MSDR/DDRII/MDDR data bit[9]
F4	MEM_D10	B	SDR/MSDR/DDRII/MDDR data bit[10]
E1	MEM_D11	B	SDR/MSDR/DDRII/MDDR data bit[11]
G2	MEM_D12	B	SDR/MSDR/DDRII/MDDR data bit[12]
G4	MEM_D13	B	SDR/MSDR/DDRII/MDDR data bit[13]
G1	MEM_D14	B	SDR/MSDR/DDRII/MDDR data bit[14]
G3	MEM_D15	B	SDR/MSDR/DDRII/MDDR data bit[15]
N4	MEM_D16	B	SDR/MSDR/DDRII/MDDR data bit[16]
T7	MEM_D17	B	SDR/MSDR/DDRII/MDDR data bit[17]
T4	MEM_D18	B	SDR/MSDR/DDRII/MDDR data bit[18]
P3	MEM_D19	B	SDR/MSDR/DDRII/MDDR data bit[19]
P4	MEM_D20	B	SDR/MSDR/DDRII/MDDR data bit[20]
R4	MEM_D21	B	SDR/MSDR/DDRII/MDDR data bit[21]
R5	MEM_D22	B	SDR/MSDR/DDRII/MDDR data bit[22]
U7	MEM_D23	B	SDR/MSDR/DDRII/MDDR data bit[23]
V3	MEM_D24	B	SDR/MSDR/DDRII/MDDR data bit[24]
U4	MEM_D25	B	SDR/MSDR/DDRII/MDDR data bit[25]
R6	MEM_D26	B	SDR/MSDR/DDRII/MDDR data bit[26]
T5	MEM_D27	B	SDR/MSDR/DDRII/MDDR data bit[27]
V5	MEM_D28	B	SDR/MSDR/DDRII/MDDR data bit[28]
R7	MEM_D29	B	SDR/MSDR/DDRII/MDDR data bit[29]
T6	MEM_D30	B	SDR/MSDR/DDRII/MDDR data bit[30]
U6	MEM_D31	B	SDR/MSDR/DDRII/MDDR data bit[31]
M1	MEM_A0	O	SDR/MSDR/DDRII/MDDR address bit[0]
K1	MEM_A1	O	SDR/MSDR/DDRII/MDDR address bit[1]
K2	MEM_A2	O	SDR/MSDR/DDRII/MDDR address bit[2]
J1	MEM_A3	O	SDR/MSDR/DDRII/MDDR address bit[3]
J2	MEM_A4	O	SDR/MSDR/DDRII/MDDR address bit[4]
H4	MEM_A5	O	SDR/MSDR/DDRII/MDDR address bit[5]
H3	MEM_A6	O	SDR/MSDR/DDRII/MDDR address bit[6]
K3	MEM_A7	O	SDR/MSDR/DDRII/MDDR address bit[7]
J3	MEM_A8	O	SDR/MSDR/DDRII/MDDR address bit[8]
H1	MEM_A9	O	SDR/MSDR/DDRII/MDDR address bit[9]
L4	MEM_A10	O	SDR/MSDR/DDRII/MDDR address bit[10]
L3	MEM_A11	O	SDR/MSDR/DDRII/MDDR address bit[11]
H2	MEM_A12	O	SDR/MSDR/DDRII/MDDR address bit[12]
G5	MEM_A13	O	SDR/MSDR/DDRII/MDDR address bit[13]
F5	MEM_A14	O	SDR/MSDR/DDRII/MDDR address bit[14]
D4	MEM_DM0	B	SDR/MSDR/DDRII/MDDR DQM bit[0]
E3	MEM_DM1	B	SDR/MSDR/DDRII/MDDR DQM bit[1]
R3	MEM_DM2	B	SDR/MSDR/DDRII/MDDR DQM bit[2]
V6	MEM_DM3	B	SDR/MSDR/DDRII/MDDR DQM bit[3]
C2	MEM_DQS0M	B	DDRII/MDDR diff DQS bit[0]
C1	MEM_DQS0P	B	DDRII/MDDR diff DQS bit[0]
F2	MEM_DQS1M	B	DDRII/MDDR diff DQS bit[1]

F1	MEM_DQS1P	B	DDRII/MDDR diff DQS bit[1]
V1	MEM_DQS2M	B	DDRII/MDDR diff DQS bit[2]
U2	MEM_DQS2P	B	DDRII/MDDR diff DQS bit[2]
V4	MEM_DQS3M	B	DDRII/MDDR diff DQS bit[3]
U5	MEM_DQS3P	B	DDRII/MDDR diff DQS bit[3]
L1	MEM_CLK	O	SDR/MSDR/DDRII/MDDR clock
L2	MEM_CLKN	O	DDRII/MDDR clock
P1	MEM_CKE_LPDDR	O	MDDR clock enable
N1	MEM_CKE	O	SDR/MSDR/DDRII clock enable
N2	MEM_BA0	O	SDR/MSDR/DDRII/MDDR bank address bit[0]
R1	MEM_BA1	O	SDR/MSDR/DDRII/MDDR bank address bit[1]
M2	MEM_BA2	O	DDRII/MDDR bank address bit[2]
U1	MEM_WEN	O	SDR/MSDR/DDRII/MDDR write enable
T1	MEM_CASN	O	SDR/MSDR/DDRII/MDDR cas select
M4	MEM_RASN	O	SDR/MSDR/DDRII/MDDR ras select
M3	MEM_CSN0	O	SDR/MSDR/DDRII/MDDR chip select
T2	MEM_CSN1	O	DDRII/MDDR chip select
R2	MEM_ODT0	O	DDRII odt bit[0]
U3	MEM_ODT1	O	DDRII odt bit[1]
V2	MEM_OPEN0	B	DDRII open bit[0]
N3	MEM_OPEN1	B	DDRII open bit[1]
P2	MEM_OPEN2	B	DDRII open bit[2]
T3	MEM_OPEN3	B	DDRII open bit[3]
L5	MEM_VREF	A	SSTL reference supply connection，1/2 VDDQ
POWER SUPPLY			
H6,H7,H8,H9,J6,J7,J8,J9,K6,K7,K8,K9,L6,L7,L8,L9	GND	G	DIGITAL GROUND FOR IO AND CORE POWER SUPPLY
G9,H10,H11,J11,K11,L10	VCCIO	P	DIGITAL POWER SUPPLY FOR IO
G7,G8,J5,J10,K5,K10,M7,M8	VDDCORE	P	DIGITAL POWER SUPPLY FOR CORE
F10,E7	VCC_LCD	P	DIGITAL POWER SUPPLY FOR LCD
R9	VCC_NAND	P	DIGITAL POWER SUPPLY FOR NAND
B18,C12	VCC_VIP	P	DIGITAL POWER SUPPLY FOR VIP
A16	RTC_DVDD33	P	RTC IO power (3.3V)
A17	RTC_AVDD	P	RTC Core Power (1.2V)
F6,H5,J4,N5,P5,P8	MEM_VDDQ	P	SDR/MOBILE DDR/DDRII POWER SUPPLY
E5,G6,K4,M5,M6,N6	MEM_VSSQ	G	SDR/MOBILE DDR/DDRII GROUND

2.3 BGA324 package outline



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	12.90	13.00	13.10	0.508	0.512	0.516
E	12.90	13.00	13.10	0.508	0.512	0.516
D1	---	11.05	---	---	0.435	---
E1	---	11.05	---	---	0.435	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	18/18			18/18		

Fig. 2-1 BGA324 package outline

Chapter 3 Port Multiplexer

3.1 Overview

RK2818 has a lot of general purpose IOs which have been described in Chapter 31 and Chapter 32. All of them are set to input mode at reset.

Most of IOs have the multiple functions shared by programmable register set. And can also be pulled-up or pulled-down by reconfigurable register. As for the detailed description for these registers, please refer to register IOMUX_A_CON / IOMUX_B_CON / GPIO0_AB_PU_CON / GPIO0_CD_PU_CON / GPIO1_AB_PU_CON / GPIO1_CD_PU_CON in Chapter 34 .

3.2 Detailed description for IO MUX

The following table shows the detailed multiplexer for all GPIOs.

Table 3-1 RK2818 IO MUX List

PAD NAME	PORT Name	PAD Direction	Pin Description
CPU GPIO0 A			
IO_GPIO0_A[0]	gpio0_a[0]	B Pull Up	gpio
	host_data[16]	I	host data bit16
IO_GPIO0_A[1]	gpio0_a[1]	B Pull Up	gpio
	host_data[17]	I	host data bit17
IO_GPIO0_A[2]	gpio0_a[2]	B Pull Up	gpio
	uart2_cts_n	I	uart2 modem signal
IO_GPIO0_A[3]	gpio0_a[3]	B Pull Up	gpio
	uart2_rts_n	O	uart2 modem signal
IO_GPIO0_A[4]	gpio0_a[4]	B Pull Up	gpio
	i2s_lrck_rx	B	i2s lrck rx
IO_GPIO0_A[5]	gpio0_a[5]	B Pull Up	gpio
	flash_cs1	O	nand flash cs1
IO_GPIO0_A[6]	gpio0_a[6]	B Pull Up	gpio
	flash_cs2	O	nand flash cs2
IO_GPIO0_A[7]	gpio0_a[7]	B Pull Up	gpio
	flash_cs3	O	nand flash cs3
CPU GPIO0 B			
IO_GPIO0_B[0]	gpio0_b[0]	B Pull Up	gpio
	spi0_csn1	O	spi0 second chip select
	sdmmc1_pwr_en	O	sdmmc1 power control
	uart2_sin	I	uart2 serial in
IO_GPIO0_B[1]	gpio0_b[1]	B Pull Up	gpio
	sm_cs1_n	O	nor flash second chip select
	sdmmc0_pwr_en	O	sdmmc0 power control
	uart2_sout	O	uart2 serial out
IO_GPIO0_B[2]	gpio0_b[2]	B Pull Up	gpio
	uart0_cts_n	I	uart0 modem signal
IO_GPIO0_B[3]	gpio0_b[3]	B Pull Up	gpio
	uart0_rts_n	O	uart0 modem signal
IO_GPIO0_B[4]	gpio0_b[4]	B Pull Up	gpio
	spi0_csn0	O	spi0 first chip select
	sdmmc0_data[4]	B	sdmmc0 data bit4

IO_GPIO0_B[5]	gpio0_b[5]	B Pull Up	gpio
	spi0_clkout	O	spi0 clk out
	sdmmc0_data[5]	B	sdmmc0 data bit5
IO_GPIO0_B[6]	gpio0_b[6]	B Pull Up	gpio
	spi0_txd	O	spi0 txd
	sdmmc0_data[6]	B	sdmmc0 data bit6
IO_GPIO0_B[7]	gpio0_b[7]	B Pull Up	gpio
	spi0_rxd	I	spi0 rxd
	sdmmc0_data[7]	B	sdmmc0 data bit7

CPU GPIO0 C

IO_GPIO0_C[0]	gpio0_c[0]	B Pull Up	gpio
	lcdc_data16	O	lcdc data bit16
IO_GPIO0_C[1]	gpio0_c[1]	B Pull Up	gpio
	lcdc_data17	O	lcdc data bit17
IO_GPIO0_C[2]	gpio0_c[2]	B Pull Up	gpio
	lcdc_data18	O	lcdc data bit18
IO_GPIO0_C[3]	gpio0_c[3]	B Pull Up	gpio
	lcdc_data19	O	lcdc data bit19
IO_GPIO0_C[4]	gpio0_c[4]	B Pull Up	gpio
	lcdc_data20	O	lcdc data bit20
IO_GPIO0_C[5]	gpio0_c[5]	B Pull Up	gpio
	lcdc_data21	O	lcdc data bit21
IO_GPIO0_C[6]	gpio0_c[6]	B Pull Up	gpio
	lcdc_data22	O	lcdc data bit22
IO_GPIO0_C[7]	gpio0_c[7]	B Pull Up	gpio
	lcdc_data23	O	lcdc data bit23

CPU GPIO0 D

IO_GPIO0_D[0]	gpio0_d[0]	B Pull Up	gpio
	lcdc_data8	O	lcdc data bit8
IO_GPIO0_D[1]	gpio0_d[1]	B Pull Up	gpio
	lcdc_data9	O	lcdc data bit9
IO_GPIO0_D[2]	gpio0_d[2]	B Pull Up	gpio
	lcdc_data10	O	lcdc data bit10
IO_GPIO0_D[3]	gpio0_d[3]	B Pull Up	gpio
	lcdc_data11	O	lcdc data bit11
IO_GPIO0_D[4]	gpio0_d[4]	B Pull Up	gpio
	lcdc_data12	O	lcdc data bit12
IO_GPIO0_D[5]	gpio0_d[5]	B Pull Up	gpio
	lcdc_data13	O	lcdc data bit13
IO_GPIO0_D[6]	gpio0_d[6]	B Pull Up	gpio
	lcdc_data14	O	lcdc data bit14
IO_GPIO0_D[7]	gpio0_d[7]	B Pull Up	gpio
	lcdc_data15	O	lcdc data bit15

CPU GPIO E

IO_GPIO_E[0]	gpio1_a[1]	B Pull Down	gpio
	vip_data[0]	I Pull Down	vip input data bit0
IO_GPIO_E[1]	gpio1_a[1]	B Pull Down	gpio
	spi1_clkin	I	spi1 slave mode clock signal
	flash_cs4	O	nand flash cs4
IO_GPIO_E[2]	gpio1_a[2]	B Pull Down	gpio
	spi1_ss_n	I	spi1 slave mode select signal
	flash_cs5	O	nand flash cs5

IO_GPIO_E[3]	gpio1_a[3]	B Pull Down	gpio
	spi1_rxd	I	spi1 rxd
	flash_cs6	O	nand flash cs6
IO_GPIO_E[4]	i2c0_sda	B Pull Up	i2c0 sda
	gpio1_a[4]	B Pull UP	gpio
IO_GPIO_E[5]	i2c0_scl	B Pull UP	i2c0 scl
	gpio1_a[5]	B Pull UP	gpio
IO_GPIO_E[6]	gpio1_a[6]	B Pull UP	gpio
	uart1_sir_in	I	uart1 IR data in
	i2c1_sda	B Pull UP	i2c1 sda
IO_GPIO_E[7]	gpio1_a[7]	B Pull UP	gpio
	uart1_sir_out_n	O	uart1 IR data out
	i2c1_scl	B Pull UP	i2c1 scl

CPU GPIO F

IO_GPIO_F[0]	gpio1_b[0]	B Pull Down	gpio
	uart1_sin	I	uart1 serial data in
	cx_timer0_pwm	O	pwm out from dsp
IO_GPIO_F[1]	gpio1_b[1]	B Pull Down	gpio
	uart1_sout	O	uart1 serial data out
	cx_timer1_pwm	O	pwm out from dsp
IO_GPIO_F[2]	gpio1_b[2]	B Pull Down	gpio
	pwm0	B	pwm
IO_GPIO_F[3]	gpio1_b[3]	B Pull Down	gpio
	pwm1	B	pwm
	sdmmc0_detect_n	I	sdmmc0 detect signal
	uart3_sin	I	uart3 serial in
IO_GPIO_F[4]	gpio1_b[4]	B Pull Down	gpio
	pwm2	B	pwm
	sdmmc0_write_prt	I	sdmmc0 write protect
	uart3_sout	O	uart3 serial out
IO_GPIO_F[5]	gpio1_b[5]	B Pull Down	gpio
	pwm3	B	pwm
	vip_data[1]	I Pull Down	vip input data bit1
IO_GPIO_F[6]	gpio1_b[6]	B Pull Down	gpio
	vip_clkout	O	sensor clk out
IO_GPIO_F[7]	gpio1_b[7]	B Pull Down	gpio
	spi1_txd	O	spi1 txd
	flash_cs7	O	nand flash cs7

CPU GPIO G

IO_GPIO_G[0]	gpio1_c[0]	B Pull Down	gpio
	uart0_sin	I	uart0 serial data in
	sdmmc1_detect_n	I	sdmmc1 card detect
IO_GPIO_G[1]	gpio1_c[1]	B Pull Down	gpio
	uart0_sout	O	uart0 serial data out
	sdmmc1_write_prt	I	sdmmc1 card write protect
IO_GPIO_G[2]	gpio1_c[2]	B Pull Down	gpio
	sdmmc1_cmd	B	sdmmc1 command
IO_GPIO_G[3]	gpio1_c[3]	B Pull Down	gpio
	sdmmc1_data[0]	B	sdmmc1 data bit0
IO_GPIO_G[4]	gpio1_c[4]	B Pull Down	gpio
	sdmmc1_data[1]	B	sdmmc1 data bit1
IO_GPIO_G[5]	gpio1_c[5]	B Pull Down	gpio

	sdmmc1_data[2]	B	sdmmc1 data bit2
IO_GPIO_G[6]	gpio1_c[6]	B Pull Down	gpio
	sdmmc1_data[3]	B	sdmmc1 data bit3
IO_GPIO_G[7]	gpio1_c[7]	B Pull Down	gpio
	sdmmc1_clkout	O	sdmmc1 clk out
CPU GPIO H			
IO_GPIO_H[0]	gpio1_d[0]	B Pull Down	gpio
	sdmmc0_cmd	B	sdmmc0 command
IO_GPIO_H[1]	gpio1_d[1]	B Pull Down	gpio
	sdmmc0_data[0]	B	sdmmc0 data bit0
IO_GPIO_H[2]	gpio1_d[2]	B Pull Down	gpio
	sdmmc0_data[1]	B	sdmmc0 data bit1
IO_GPIO_H[3]	gpio1_d[3]	B Pull Down	gpio
	sdmmc0_data[2]	B	sdmmc0 data bit2
IO_GPIO_H[4]	gpio1_d[4]	B Pull Down	gpio
	sdmmc0_data[3]	B	sdmmc0 data bit3
IO_GPIO_H[5]	gpio1_d[5]	B Pull Down	gpio
	sdmmc0_clkout	O	sdmmc0 clock out
IO_GPIO_H[6]	gpio1_d[6]	B Pull Down	gpio
	vip_data[2]	I Pull Down	vip input data bit2
IO_GPIO_H[7]	gpio1_d[7]	B Pull Down	gpio
	vip_data[3]	I Pull Down	vip input data bit3
DSP GPIO			
IO_GPIO2[0]	gpio2[0]	B Pull UP	gpio
	host_data0	B	host interface data bit0
IO_GPIO2[1]	gpio2[1]	B Pull UP	gpio
	host_data1	B	host interface data bit1
IO_GPIO2[2]	gpio2[2]	B Pull UP	gpio
	host_data2	B	host interface data bit2
IO_GPIO2[3]	gpio2[3]	B Pull UP	gpio
	host_data3	B	host interface data bit3
IO_GPIO2[4]	gpio2[4]	B Pull UP	gpio
	host_data4	B	host interface data bit4
IO_GPIO2[5]	gpio2[5]	B Pull UP	gpio
	host_data5	B	host interface data bit5
IO_GPIO2[6]	gpio2[6]	B Pull UP	gpio
	host_data6	B	host interface data bit6
IO_GPIO2[7]	gpio2[7]	B Pull UP	gpio
	host_data7	B	host interface data bit7
IO_GPIO2[8]	gpio2[8]	B Pull UP	gpio
	host_addr0	I	host interface addr bit0
IO_GPIO2[9]	gpio2[9]	B Pull UP	gpio
	host_addr1	I	host interface addr bit1
IO_GPIO2[10]	gpio2[10]	B Pull UP	gpio
	host_csn	I	host interface chip select
IO_GPIO2[11]	gpio2[11]	B Pull UP	gpio
	host_rdn	I	host interface read valid
IO_GPIO2[12]	gpio2[12]	B Pull UP	gpio
	host_wrn	I	host interface write valid
IO_GPIO2[13]	gpio2[13]	B Pull UP	gpio
	ap2bb_int	O	host interface interrupt from

			chip to host
IO_GPIO2[14]	gpio2[14]	B Pull UP	gpio
	host_data[8]	B Pull Down	host interface data bit8
	hsadc_data_q[0]	I	hsadc data bit0 for Q path
IO_GPIO2[15]	gpio2[15]	B Pull UP	gpio
	host_data[9]	B Pull Down	host interface data bit8
	hsadc_data_q[1]	I	hsadc data bit1 for Q path
IO_GPIO2[16]	gpio2[16]	B Pull Down	gpio
	host_data[10]	B Pull Down	host interface data bit8
	hsadc_data_q[2]	I	hsadc data bit2 for Q path
IO_GPIO2[17]	gpio2[17]	B Pull Down	gpio
	host_data[11]	B Pull Down	host interface data bit8
	hsadc_data_q[3]	I	hsadc data bit3 for Q path
IO_GPIO2[18]	gpio2[18]	B Pull Down	gpio
	host_data[12]	B Pull Down	host interface data bit8
	hsadc_data_q[4]	I	hsadc data bit4 for Q path
IO_GPIO2[19]	gpio2[19]	B Pull Down	gpio
	host_data[13]	B Pull Down	host interface data bit8
	hsadc_data_q[5]	I	hsadc data bit5 for Q path
IO_GPIO2[20]	gpio2[20]	B Pull Down	gpio
	host_data[14]	B Pull Down	host interface data bit8
	hsadc_data_q[6]	I	hsadc data bit6 for Q path
IO_GPIO2[21]	gpio2[21]	B Pull Down	gpio
	host_data[15]	B Pull Down	host interface data bit8
	hsadc_data_q[7]	I	hsadc data bit7 for Q path
IO_GPIO2[22]	gpio2[22]	B Pull Down	gpio
	sm_we_n	O	SRAM wen
	hsadc_data_q[8]	I	hsadc data bit8 for Q path
IO_GPIO2[23]	gpio2[23]	B Pull Down	gpio
	sm_oe_n	O	SRAM oen
	hsadc_data_q[9]	I	hsadc data bit9 for Q path
IO_GPIO2[24]	gpio2[24]	B Pull Down	gpio
	gps clk	I Pull Down	clock input for gps application
	hsadc_clkout	O	clock out to hsadc analog
IO_GPIO2[25]	gpio2[25]	B Pull Down	gpio
	lcdc_vsync	O	lcdc vertical sync signal
IO_GPIO2[26]	gpio2[26]	B Pull Down	gpio
	lcdc_denable	O	lcdc data valid signal
IO_GPIO2[27]	i2s_sdi	I Pull Down	i2s sdi from codec
	gpio2[27]	B Pull Down	gpio
IO_GPIO2[28]	i2s_sdo	O	i2s sdo to codec
	gpio2[28]	B Pull Down	gpio
IO_GPIO2[29]	i2s_clk	O	i2s clock out to codec
	gpio2[29]	B Pull Down	gpio
IO_GPIO2[30]	i2s_lrck	B Pull Down	i2s lrck
	gpio2[30]	B Pull Down	gpio
IO_GPIO2[31]	i2s_sclk	B Pull Down	i2s serial clock
	gpio2[31]	B Pull Down	gpio

Notes : B --- Bidirectional IO
I --- Input IO
O --- Output IO

Chapter 4 Hardware Information

31.1 Oscillator Connection

RK2818 will use two oscillators, one is for input of three on-chip PLLs , for USB OTG PHY, and for I2S main clock, which should be 24MHz, another is for RTC function, which should be 32.768KHz. The design for oscillator pad has been optimized for stability and minimum jitter, and characterized to allow a variation of 4pF to 18pF on both XI and XO pins for crystal stability. In the Fig. 39-1 , the variation range for C value is 4pF to 18pF.

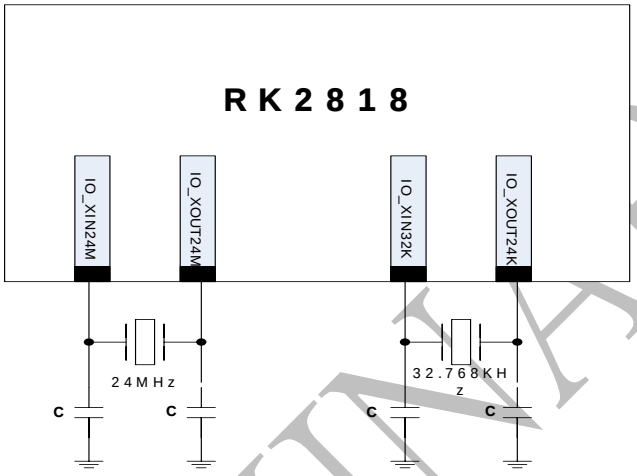


Fig. 4-1 RK2818 external oscillator connection diagram

31.2 USB PHY Connection

USB2.0 OTG PHY is used in RK2818 for USB host, USB device and otg functions. The following figure shows external connection for USB PHY interface.

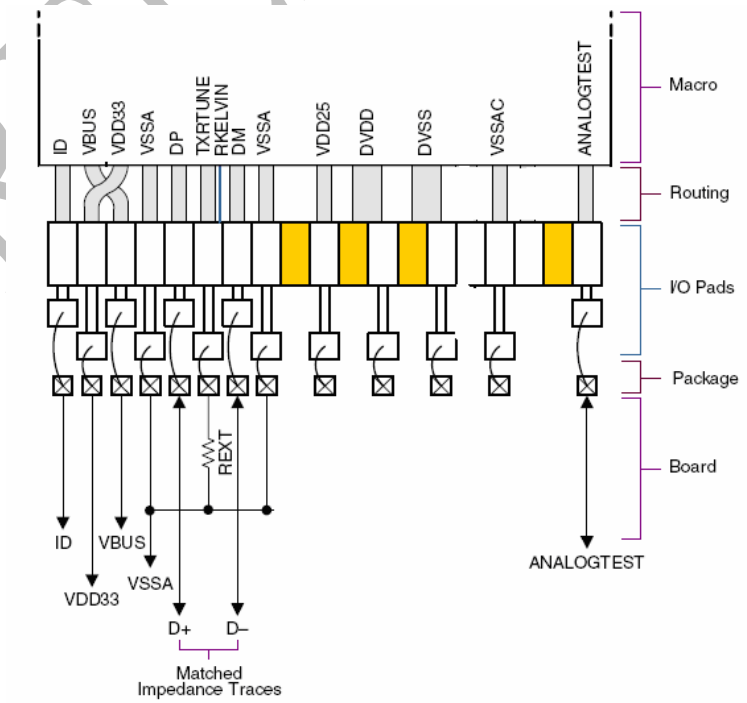


Fig. 4-2 RK2818 USB PHY connection diagram

In the above diagram, some parameters and its viariant will be shown in the following table.

External resistor (REXT)	44.2 Ω (± 1%)
Analog power supplies	3.3 V (+ 10%, – 10%) at the macro pins with respect to VSSA and VSSAC 2.5 V (+ 10%, – 10%) at the macro pins with respect to VSSA and VSSAC
Digital power supply	1.2 V (+ 10%, – 12.5%) at the macro pins with respect to DVSS
Junction temperature	–40º C through +125º C

31.3 Power up Sequence for power supply

For IO and core power supply of RK2818, there are no power sequence requirements, since IO is 3-state when core power is not valid.

31.4 Power on reset Descriptions

The following figure shows power-on-reset sequence and relative clock behavior. When npor (power-on-reset) is released after stabilization of oscillator clock xin24m. After about T1 timing length, power supply for on-chip PLLs will be in stable state and pll_rstn (internal reset signal for PLL) is released. Then after (T2-T1) timing length, chip_rstn (internal reset signal for chip logic) is released. Then clock for IP module inside chip will be valid . After about 15 clocks , ip_rstn (internal reset signal for all IPs) will be released, which can meet some special requirements for some IPs , " reset signal will be kept valid no less than 15 clock cycles" .

Notes : T1 is about 5us ; T2 is about 139us

Another, RK2818 can filter out 5 clock cycles for low pulse of npor, the clock cycle is xin24m clock, so about 208ns low pulse of npor will not be recognized as valid power-on-reset signal for RK2818.

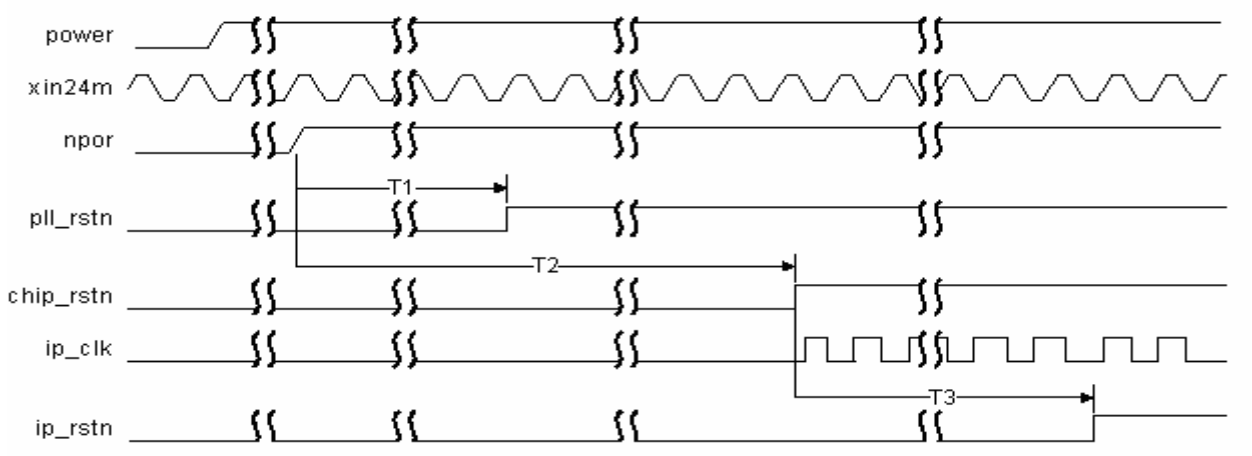


Fig. 4-3 RK2818 reset sequence timing waveform

Chapter 5 Electrical Specification

32.1 Recommended Operating Conditions

Symbol	Paramerters	Min	Typ	Max	Unit
VDD	Power Supply Voltage (Digital Core)	1.08	1.2	1.32	V
VCCIO	Power Supply Voltage (Digital IO)	2.97	3.3	3.63	V
GND	Ground Voltage (Digital Core and IO)	N/A	0	N/A	V
VDDSDR	IO Power Supply Voltage (SDRAM IO)	2.97	3.3	3.63	V
	IO Power Supply Voltage (Mobile SDRAM IO)	1.62	1.8	1.98	V
VSSSDR	Ground Voltage (SDRAM IO)	N/A	0	N/A	V
VDDA_xPLL	Power Supply Voltage (PLL)	1.08	1.2	1.32	V
VSSA_xPLL	Ground Voltage (PLL)	N/A	0	N/A	V
AVDD25_USB	Power Supply Voltage (USB Analog part)	2.25	2.5	2.75	V
AVDD33_USB	Power Supply Voltage (USB Analog part)	2.97	3.3	3.63	V
AVSS_USB	Ground Voltage (USB Analog part)	N/A	0	N/A	V
DVDD_USB	Power Supply Voltage (USB digital part)	1.08	1.2	1.32	V
DVSS_USB	Ground Voltage (USB digital part)	N/A	0	N/A	V
VDDA_ADC	Power Supply Voltage (SAR-ADC Analog)	2.8	3	3.6	V
VSSA_ADC	Ground Voltage (SAR-ADC Analog)	0	0	0	V
XIN24M	PLL Input clock frequency	N/A	24	N/A	MHz
T	Operating Temperature	-10	25	40	0C

32.2 DC Characteristics

Symbol	Paramerters	Min	Typ	Max	Unit
Vil	Input Low Voltage	-0.3	N/A	0.3*VCCIO	V
Vih	Input High Voltage	0.7*VCCIO	N/A	VCCIO+0.3	V
Vol	Output Low Voltage			0.4	V
Voh	Output High Voltage	VCCIO-0.4		3.6	V

32.3 Absolute Maximum Range

Symbol	Paramerters	Min	Max	Unit
Vvdd	Core supply voltage range	-0.5	1.32	V
Vvccio	I/O supply voltage range	-0.5	3.6	V
Vpad	Voltage range at digital IO	-0.5	VCCIO+0.5	V
Vanalog	Voltage range at analog IO	0	VDDanalog(max)	V