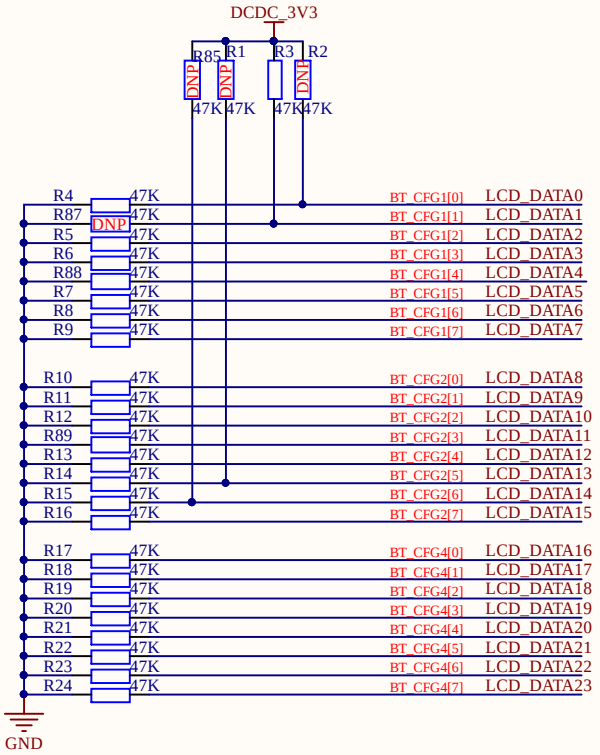
BOOT MAP

	0/1	0/1	0/1	1	0	0	0	0
TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved	DDRSMP: "000" : Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High! 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

	0	0	0	0	1	0	0	0
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS: Half Speed Phase Selection '0' - select sampling at non-inverted clock '1' - select sampling at inverted clock	HSDLY: Half Speed Delay selection '0' - one clock delay '1' - two clock delay	FSPHS: Full Speed Phase Selection '0' - select sampling at non-inverted clock '1' - select sampling at inverted clock	FSDLY: Full Speed Delay selection '0' - one clock delay '1' - two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 12ms '1' - 22ms (LBA Nand)	Reserved

	0	0	0	0	0	0	0	0
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/Emmc
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHC IOMUX SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

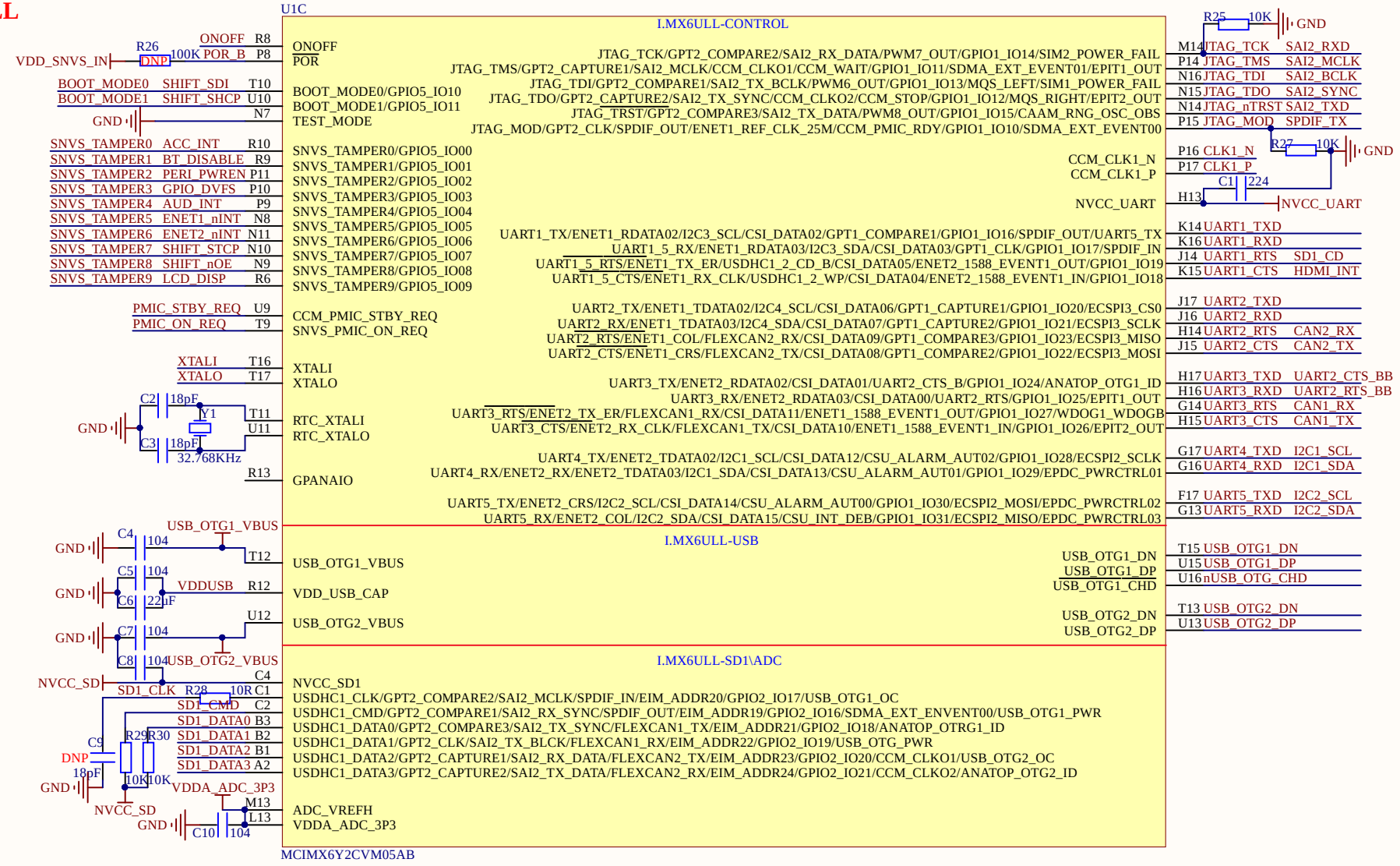
#Boot map pictures reference from the NXP I.MX6ULL EVK Board Schematic



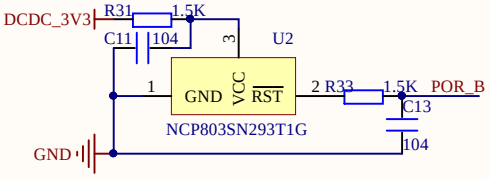
BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot(Development)
11	Reserved

Title: *		
Author: lycreturn@ALIENTEK	Size: A4	Cannot open file D:\Program
Date: 2019-11-11	File: IMX6ULL_CORE_BOOT.SchDoc	
Revision: *	Version: V1.0	

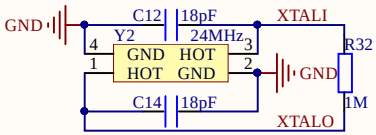
IMX6ULL



RESET

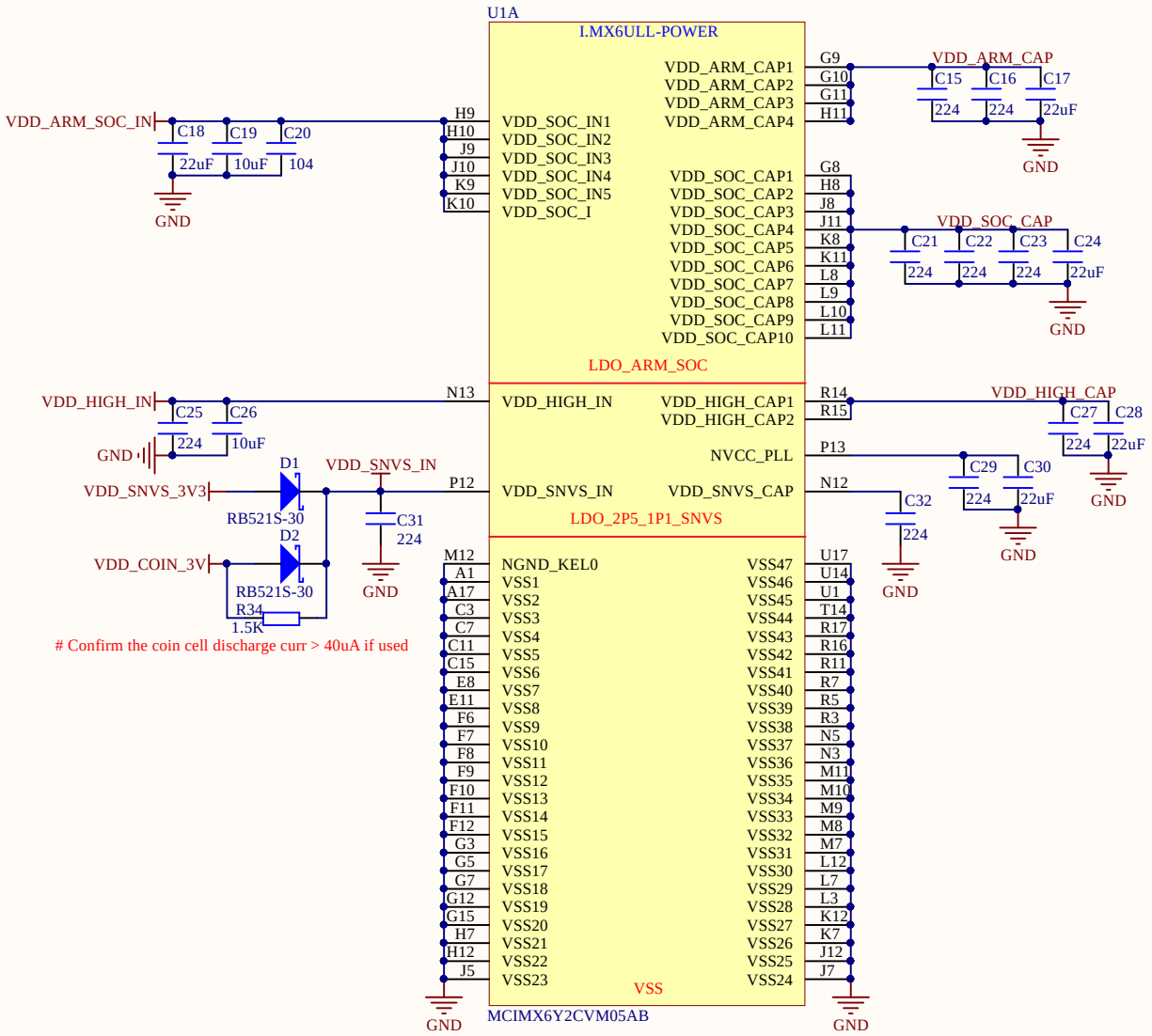


XTAL



Title: *	
Author: lycreturn@ALIENTEK	Size: A3
Date: 2019-11-11	File: IMX6ULL_CORE_CONTROL.SchDoc
Revision: *	Version: V1.0

Cannot open file D:\Program

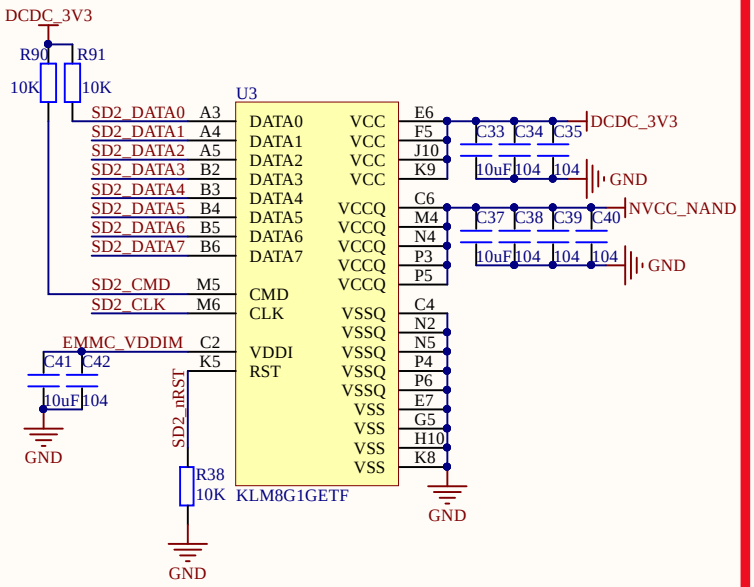


Title: *	
Author: lycreturn@ALIENTEK	Size: A4
Date: 2019-11-11	File: IMX6ULL_CORE_CPUPWR.SchDoc
Revision: *	Version: V1.0

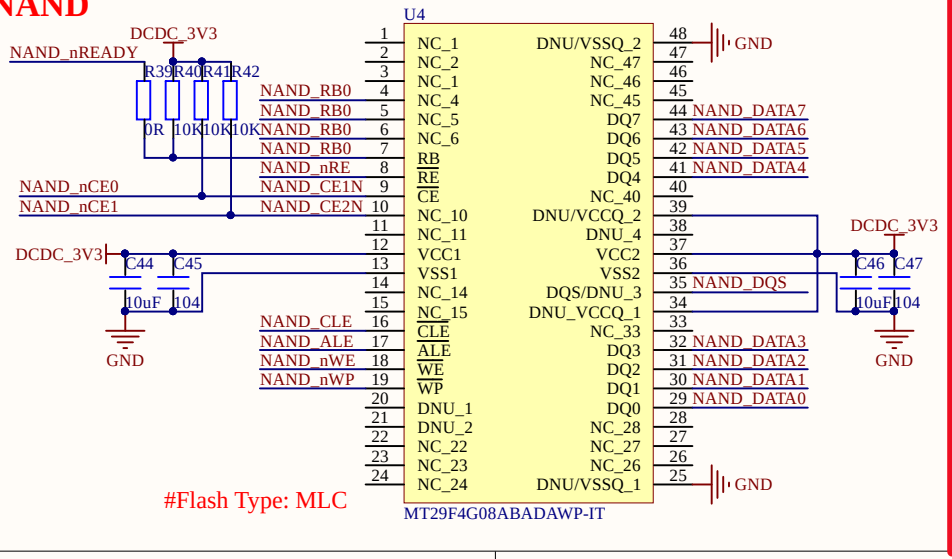
Cannot open file D:\Program

EMMC

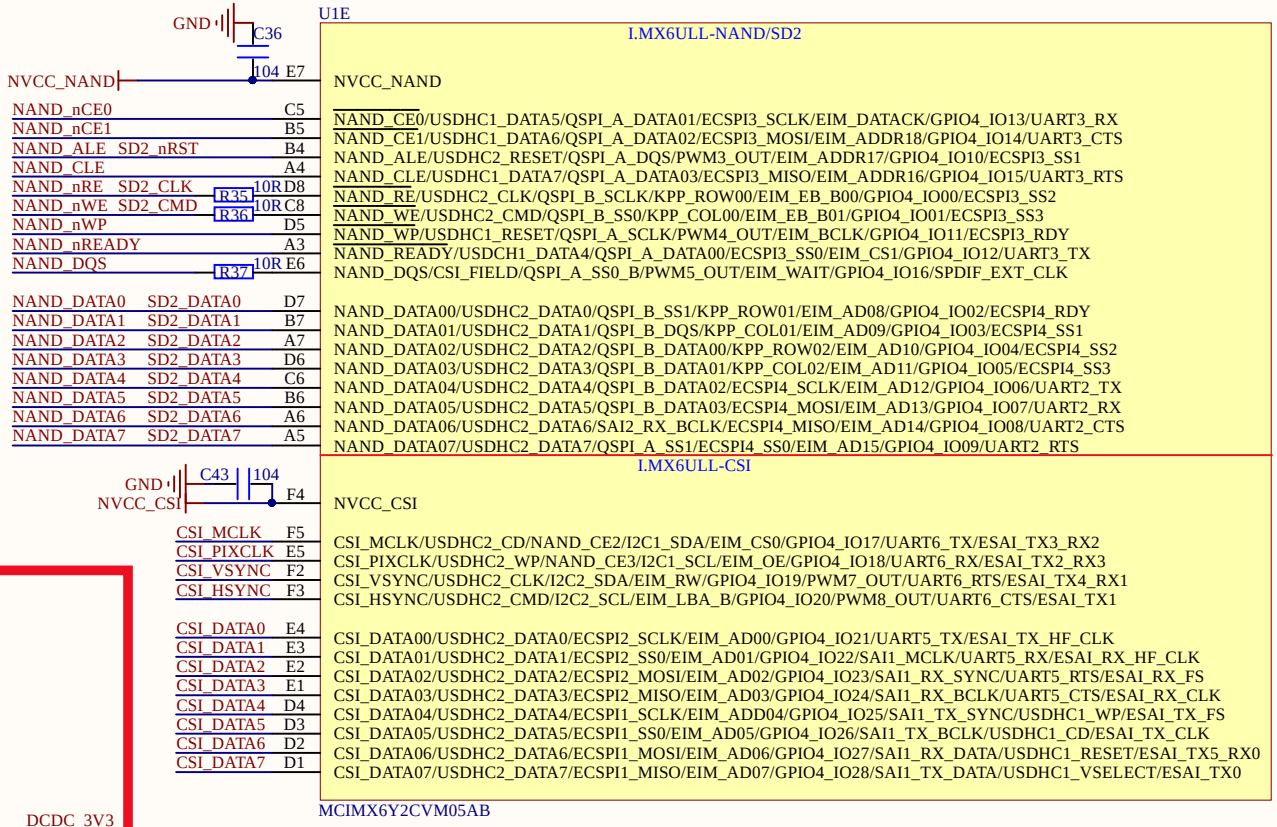
#EMMC Storage<4.51>



NAND



IMX6ULL_NAND



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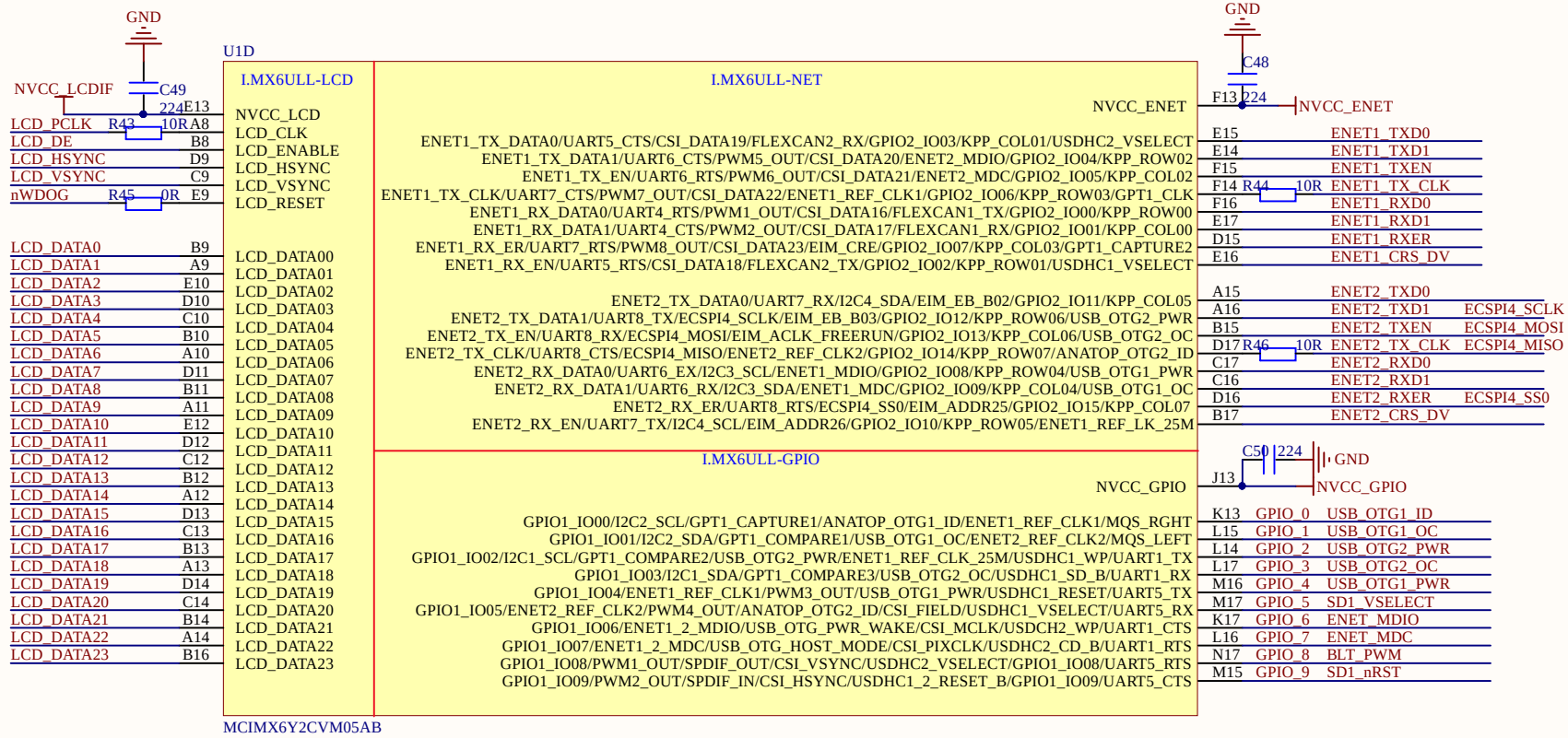
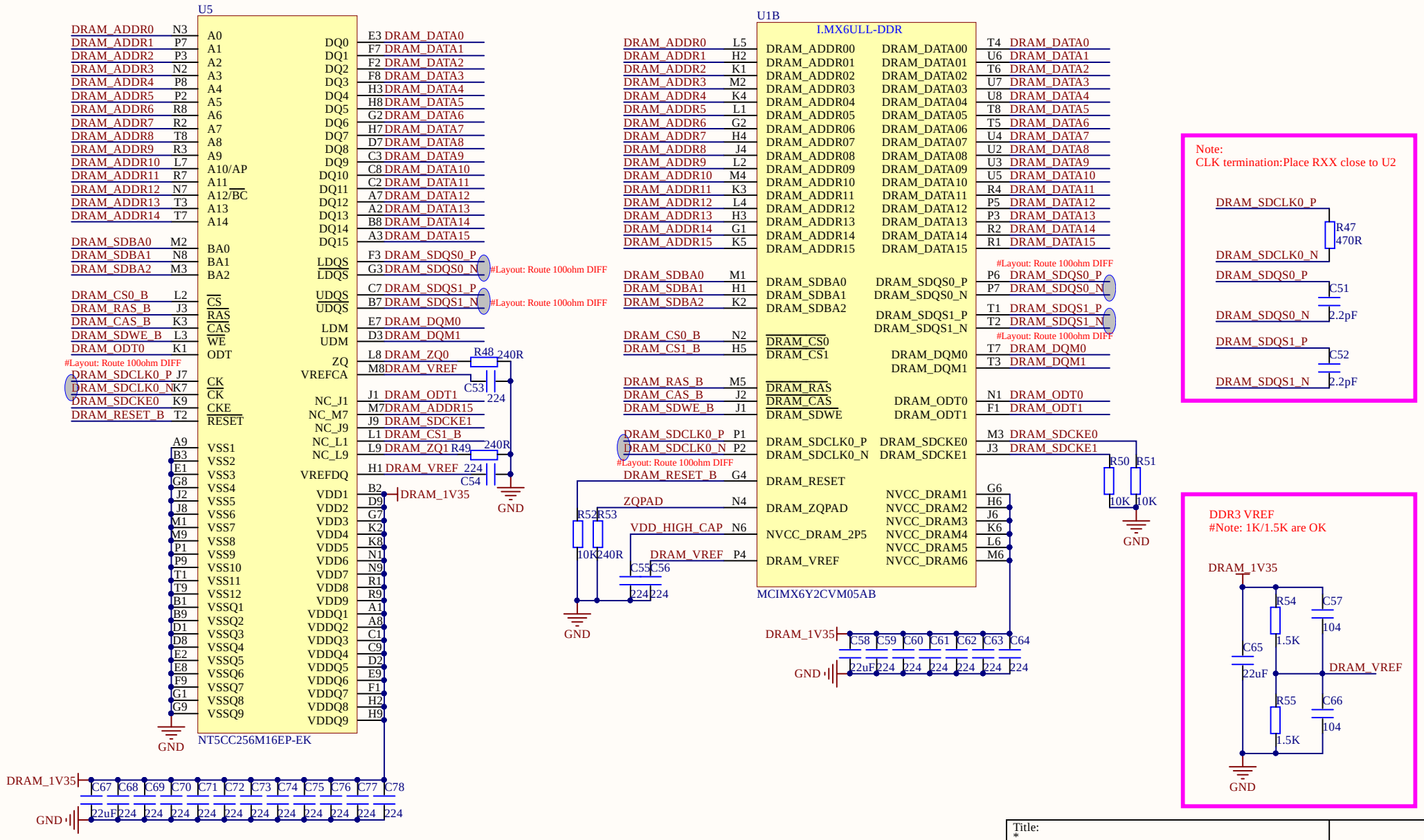
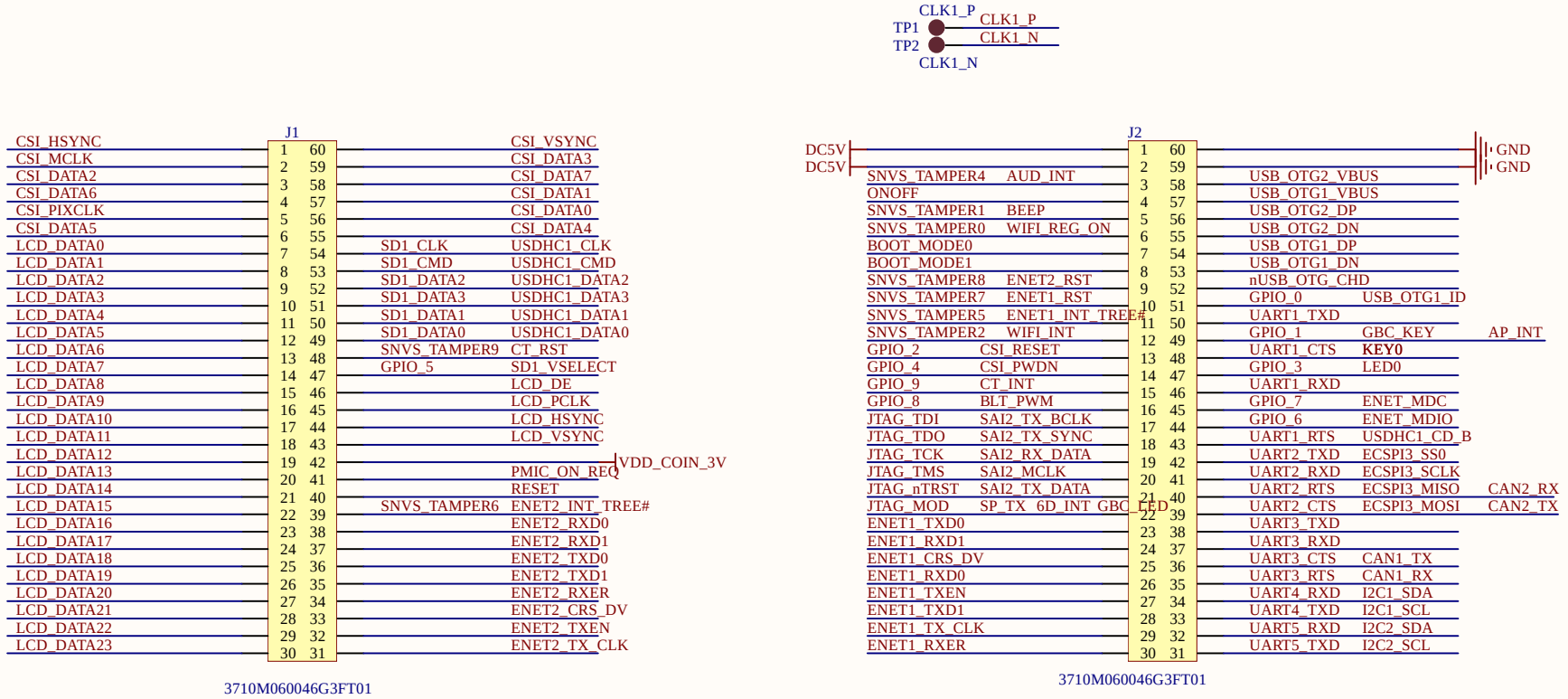
Revision: *	Version: V1.0	



Title: *		Cannot open file D:\Program
Author: lycreturn@ALIENTEK	Size: A4	
Date: 2019-11-11	File: IMX6ULL_CORE_LCDNET.SchDoc	
Revision: *	Version: V1.0	


U5
NT5CC256M16EP-EK
U1B
I.MX6ULL-DDR
MCIMX6Y2CVM05AB
#Layout: Route 100ohm DIFF
Note:
CLK termination:Place RXX close to U2
DDR3 VREF
#Note: 1K/1.5K are OK
Title:
*
Author:
lycreturn@ALIENTEK
Size:
A4
Date:
2019-11-11
File:
IMX6ULL_CORE_LVDDR3.SchDoc
Revision:
*
Version:
V1.0
Cannot open file
D:\Program



Title: *		Cannot open file D:\Program
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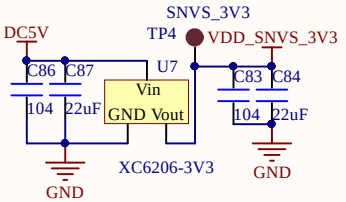
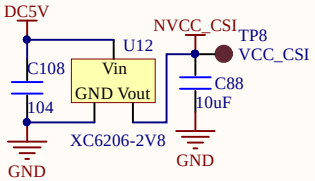
Date: 2019-11-11	File: IMX6ULL_CORE_PIN.SchDoc	
Revision: *	Version: V1.0	

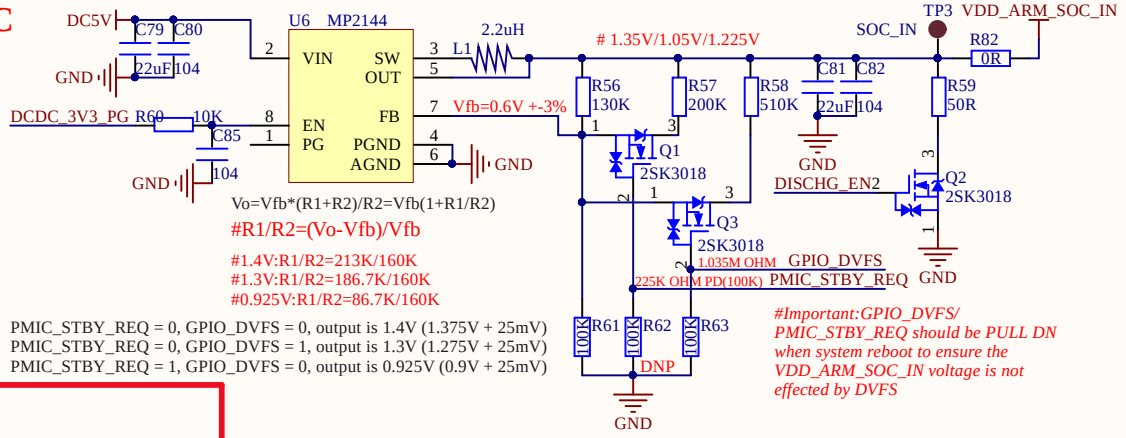
SNVS



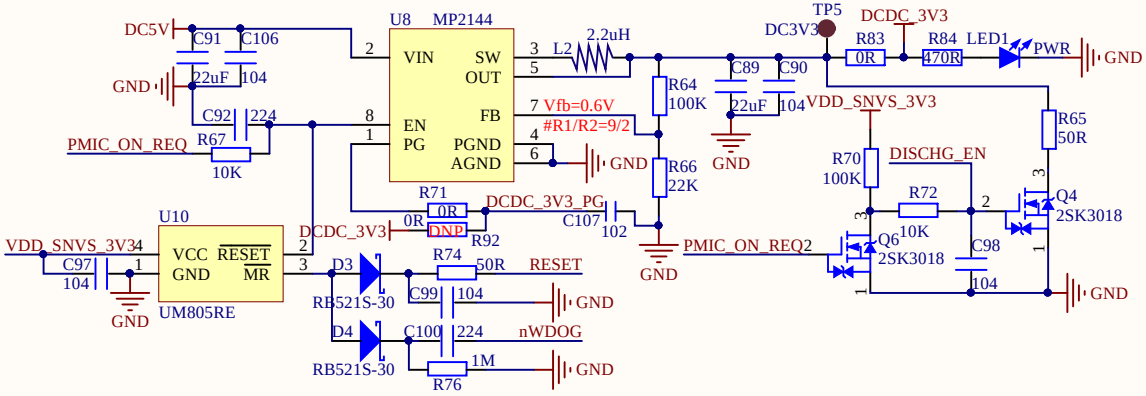
NVCC_CSI



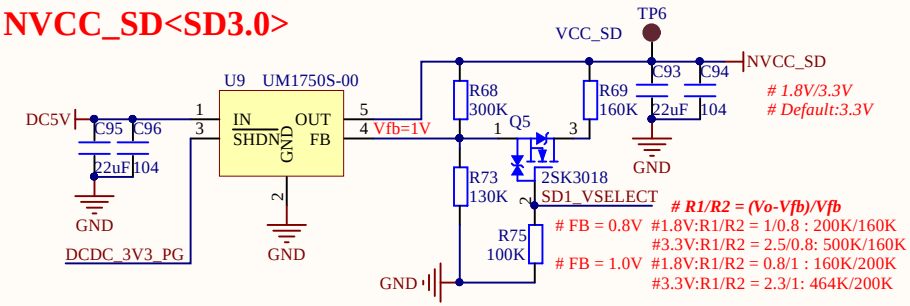
ARM/SOC



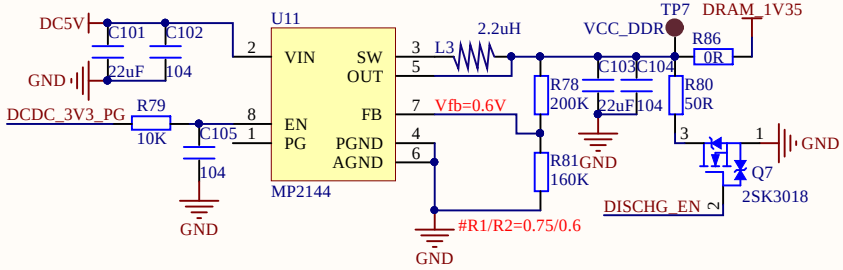
VDDHIGH/DCDC_3V3



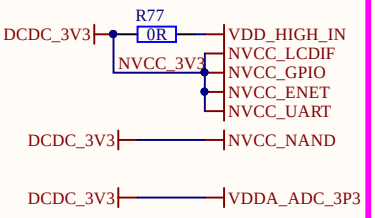
NVCC_SD<SD3.0>



LVDDR3



NVCC_xxx



I.MX6ULL PWR

Power Rail	MIN	TYP	MAX	CURR
VDD_SNVS_IN	2.4	3	3.6	276uA
VDD_HIGH_IN	2.8	3	3.6	125mA
VDD_ARM_IN	0.9	1.275	1.5	400mA
VDD_SOC_IN	0.9	1.275	1.5	500mA
NVCC_DRAM	1.425	1.5	1.575	50mA
	1.283	1.35	1.45	
	1.14	1.2	1.3	
NVCC_xxx	1.65	1.8/2.5/3.3	3.6	
VDDA_ADC_3P3	3	3.3	3.6	
USB_OTG1_VBUS	4.4	5	5.25	50mA
USB_OTG2_VBUS				

Title: *		
Author: lycreturn@ALIENTEK	Size: A4	Cannot open file D:\Program
Date: 2019-11-11	File: IMX6ULL_CORE_POWER.SchDoc	
Revision: *	Version: V1.0	